Design and analysis of a frequency division and duty cycle control circuit for on-chip signal synthesis

Design and Analysis of a Frequency Division and Duty Cycle Control Circuit for On-chip Signal Synthesis

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Abstract

In this article, a complementary metal-oxide-semiconductor (CMOS) frequency and duty cycle controller (FDCC) is presented for on-chip signal synthesis. The circuit consists of a few logic gates and a voltage-controlled oscillator, and is functionally similar to a programmable divide-by-N frequency divider. It is designed for driving integrated sensor and actuator systems. Compared with other frequency dividers with the same control flexibility, the proposed circuit features a compact topology and allows the control over the output signal duty cycle. For the proof-of-concept, a prototype 1×4 array of identical FDCCs has been fabricated on a 0.35 μm Austria Mikro Systeme (AMS) CMOS process. Each FDCC occupies an active area of 0.0051 mm^2, which is area-efficient. The array has been validated to generate 4 synchronized 4 $MHz \sim 64$ MHz outputs with a duty cycle tunning range of $3.125\% \sim 96.875\%$. Although driven by a 5-V power supply, it still provides a relatively high power-efficiency of 1.26 GHz/mW.

Keywords: Frequency control, Duty cycle control, Programmable divide-by-N frequency divider, Clock generation, Signal synthesis

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1. Introduction

In the past decades, for the merit of cost, power consumption and size reduction, considerable efforts have been made on developing integrated sensor and actuator platforms. For such advanced systems, clock and signal sources play an important role for performing diverse analog, digital, mixed-signal functions and driving sensors/transducers. These sources usually operate simultaneously but require dedicated optimizations for the desired performance. As a result, clock generators of integrated platforms are typically implemented as combinations of several independent on-chip phase-locked loops (PLLs) [1, 2] and/or delay-locked loops (DLLs) [3, 4]. However, the design of PLLs and DLLs requires special expertise and multiple of these circuit blocks, while providing high quality domains, inevitably complicates the system and can become costly solutions.

Therefore, clock multiplication from one clean reference is preferred. Elkholy et al. reported a multi-output all-digital clock generator based on open-loop delta–sigma ($\Delta\Sigma$) fractional dividers [5], and there are high-performance dividers that can potentially be implemented for clock multiplication[6, 7, 8]. However, none of these offers tunable duty cycle, which is useful for transducer/sensor excitation and control [9, 10, 11], clock duty cycle calibration, non-overlap signal generation [12] and circuit energy-saving controls [13], etc.

On the other hand, open-loop digitally controlled oscillators (DCOs) can provide tunable duty cycle [14, 15, 16]. However, due to inevitable frequency mismatches, enormous efforts are required to synchronize multiple DCOs and allow multiphase generation. Furthermore, these open-loop DCOs are vulnerable to process-voltage-temperature (PVT) variations.

In view of these drawbacks, we propose the design methodology of an on-chip CMOS FDCC for clock generation/multiplication purposes. By introducing simple circuit blocks to delicately control the oscillation, a relaxation oscillator is enabled to operate in an open-loop manner with enhanced mismatch and

PVT tolerance. The FDCC is functionally similar to a programmable divide-by-N frequency divider. Compared with traditional programmable dividers for clock multiplication, the proposed FDCC can provide tunable duty cycle that is required by many integrated sensor and actuator systems. It is also comparatively power- and area-efficient. Compared with traditional open-loop DCOs, it is robust against PVT variations and allows the generation of multiphase. The FDCC is designed for driving integrated systems such as ultrasonic capsule endoscopy system[10], integrated acoustic imager and tweezer system[11], gas detection system[9, 12] and flow sensing system[13], etc. It is compact and highly flexible and hence is also favored by prototyping systems.

Rest of this article is organized as follows. In Section 2, the proposed FDCC architecture is presented, followed by a digitally controlled FDCC in Section 3. The simulation and measurement results of a prototype 1×4 FDCC array, including the demonstration of functionality and its performance against PVT variations, are presented in Sections 4&5. The main contributions of this article are listed as follows:

1) An FDCC design methodology for on-chip signal synthesis is proposed. The FDCC is compact, flexible, power- and area-efficient and is designed for driving integrated systems and prototyping circuits/systems.

2) The simulation and experimental results of an FDCC implemented in a 0.35 μm AMS process are presented for the validation of the design methodology. This FDCC only occupies an active area of 0.0051 mm^2 and is capable of generating $4MHz \sim 64MHz$ outputs with $3.125\% \sim 96.875\%$ duty cycles. Although driven by a 5-V power supply, it still provides a relatively high power efficiency of 1.26 GHz/mW in comparison with other frequency dividers [5, 6, 17, 18, 19, 20, 21].

3) A digitally controlled FDCC is proposed and examined with simulations based on a 2-V, 0.18 μm Taiwan Semiconductor Manufacturing Company (TSMC) process. The area occupation of this FDCC is 0.001 mm^2 and the power efficiency reaches 4.41. It can generate $3.125\% \sim 96.875\%$ duty-cycle $46.875MHz \sim 750MHz$ square waves.

2. PROPOSED FREQUENCY DIVISION AND DUTY CYCLE CONTROL CIRCUIT

A CMOS relaxation oscillator architecture is shown in Figure 1 [22]. It consists of a charge pump, a Schmitt trigger [23] and an inverter. By tuning V_{biasp} and/or V_{biasn} the signal frequency and duty cycle of the output can be tuned. If (1) is fulfilled, the output signal frequency f_o can be estimated as (2).

$$\begin{cases} V_{tn} < V_{lt} < V_{ut} < V_{dd} - |V_{tp}| \\ V_{dd} - |V_{tp}| - V_{ut} < V_{biasp} \leq V_{dd} - |V_{tp}| \\ V_{tn} \leq V_{biasn} < V_{tn} + V_{lt} \end{cases} \tag{1}$$

$$\begin{cases} f_o = \frac{1}{T_{charging} + T_{discharging}} \\ T_{charging} = \frac{C_1(V_{ut} - V_{lt})}{\frac{\mu_p C_{OX} W_{P1}}{2L_{P1}}(V_{biasp} - V_{dd} - V_{tp})^2} \\ T_{discharging} = \frac{C_1(V_{ut} - V_{lt})}{\frac{\mu_n C_{OX} W_{N1}}{2L_{N1}}(V_{biasn} - V_{tn})^2} \end{cases} \tag{2}$$

where V_{dd} is the supply voltage; V_{tp} is the PMOS threshold voltage and V_{tn} is the NMOS threshold voltage in a specific CMOS process; V_{lt} and V_{ut} are the lower and upper threshold voltages of the Schmitt trigger, respectively; C_1 is the capacitance of capacitor $Cap1$ in Figure 1; C_{OX} is the gate oxide capacitance per unit area; μ_p and μ_n are the effective mobilities of charge-carriers in PMOS and NMOS devices, respectively; W_{P1} and L_{P1} are the gate width and length of the PMOSFET, $P1$; and W_{N1} and L_{N1} are the gate width and length of the NMOSFET, $N1$.

The FDCC proposed in this article is based on an original idea of quantizing the charging and discharging processes of $Cap1$ in oscillation. As a result, a transmission gate is added to the oscillator structure as a quantizer that is controlled by the clock signal CLK, forming the clock-controlled oscillator (CCO) shown in Figure 2. Only when CLK turns on the transmission gate, $Cap1$ can get charged/discharged. In theory, once CLK is fixed, the output is related to it by a factor that can be precisely defined with V_{biasp} and V_{biasn}. However, the same V_{biasp} and V_{biasn} values can result in different oscillation

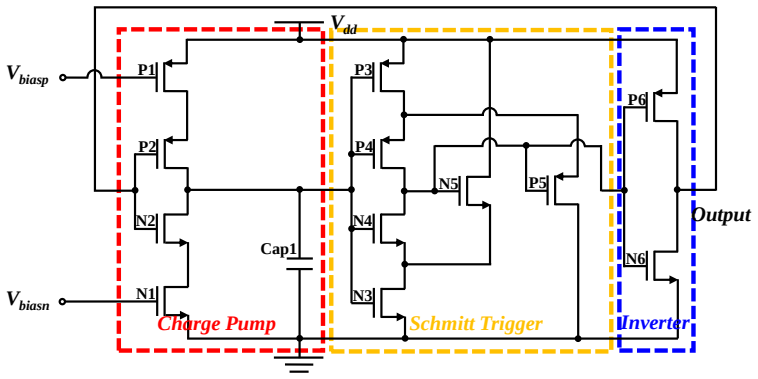


Figure 1: Schematic of a CMOS relaxation oscillator [22].

frequencies between any two of the fabricated CCOs. This is due to device mismatch/variations. Particularly, $P1/N1$ variations can cause different capacitor charging/discharging rates, and $P3 \sim P5 \& N3 \sim N5$ mismatches can result in different Schmitt trigger threshold voltages [23]. An example of the mismatched oscillations between two fabricated CCOs (CCO1&CCO2) is shown in Figure 2 (b).

To cope with the mismatch, an over-charging circuit is first added, as illustrated in Figure 3 (a). Note that the transmission gate is replaced by $P7$ and $N7$ in this architecture to reduce the channel charge injection and clock feedthrough. The threshold voltages of the Schmitt trigger in the over-charging circuit determines the time that the over-charging is enabled and periodically sets or resets the potential across the capacitor $Cap1$. By designing the upper threshold voltage of the Schmitt trigger in the over-charging circuit to be lower than that of the other Schmitt trigger, and designing the lower threshold voltage to be higher than that of the other Schmitt trigger, the over-charging circuit is always triggered prior to the output change. And, once triggered, it fully and quickly sets/resets the potential on the capacitor through a direct capacitor-to-V_{dd}/capacitor-to-ground connection, providing the same starting potential for every discharging/charging period. However, this does not eliminate the time error caused by device mismatch, as shown in Figure 3 (b). As a result, a D flip-

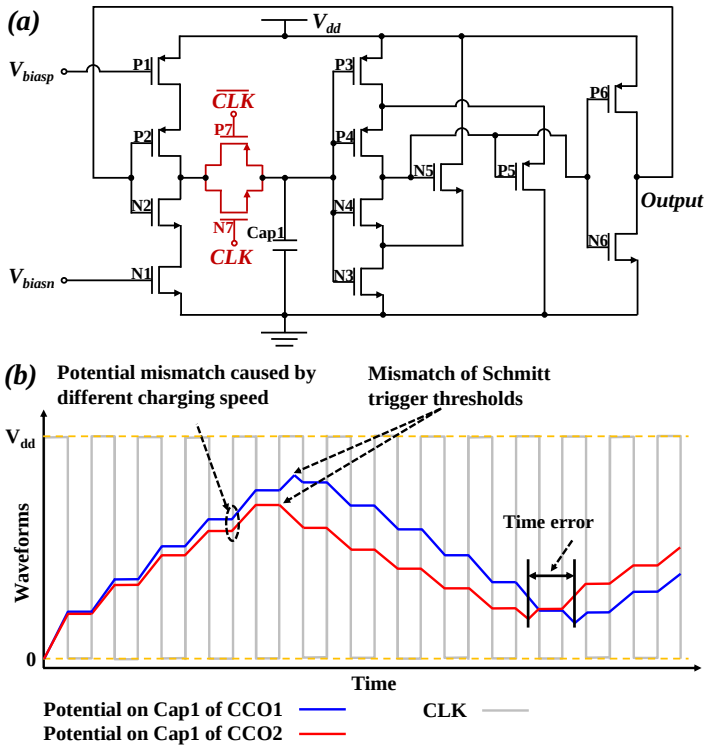


Figure 2: (a) Schematic of the CCO. (b) An example of asynchronous oscillations caused by device mismatch.

flop (DFF) is then implemented as the periodic synchronizer, which is shown in Figure 4 (a), forming the modified clock-controlled oscillator (MCCO). In addition, an NMOSFET is added to allow the Reset signal to zero the potential on $Cap1$ before the MCCO runs.

Once the frequency and the duty cycle of CLK signal are fixed, the circuit oscillation frequency is related to the CLK frequency by an integral modulus defined by V_{biasp} and V_{biasn}. There are four main working states for this MCCO, providing a stable output with PVT variation resistance that allows multiple MCCOs to be synchronized if required. An example of the waveforms generated in two fabricated MCCOs (MCCO1&MCCO2) is shown in Figure 4 (b). State 1 is the discrete charging/discharging state. In this state, the combination of P7 and N7 quantizes the charging and discharging of $Cap1$ according to comple-

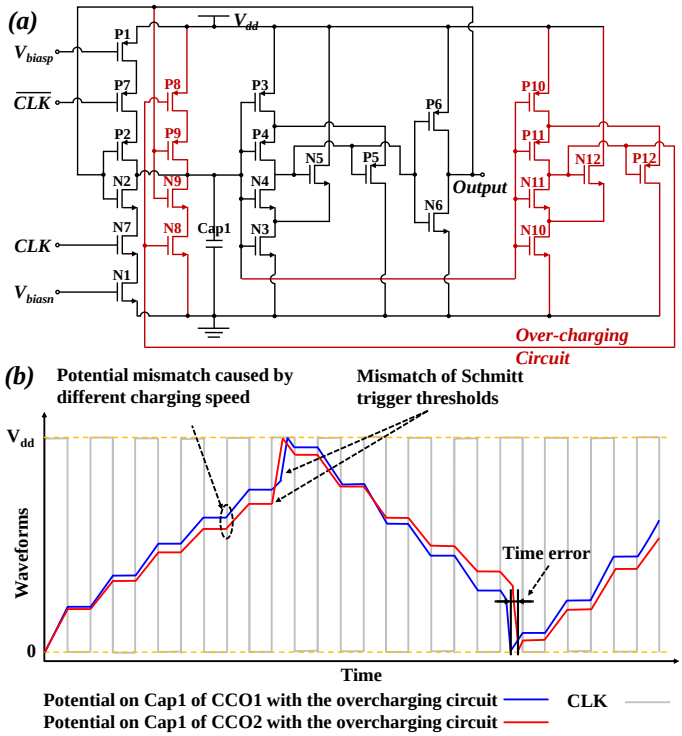


Figure 3: (a) Schematic of the CCO with the over-charging circuit. (b) An example of the waveforms generated in two fabricated CCOs (CCO1&CCO2) with the over-charging circuit.

mentary clock signals, CLK and $\overline{CLK}$. State 2 is the set/reset state in which the potential on the capacitor is rapidly set/reset. This is controlled by Schmitt trigger 2 (ST2) in Figure 4 (a). The upper threshold and the lower threshold of ST2 are recommended to be selected from $0.6V_{dd} \sim 0.8V_{dd}$ and $0.2V_{dd} \sim 0.4V_{dd}$, respectively, to maintain the linearity of charging and discharging in State 1. In State 3, the waiting state, the DFF comes in as the periodic error eliminator. It ends when a CLK signal rising edge arrives and the output of the DFF is toggled, which is State 4. States 3 and 4 together remove the time error accumulated in half the time period. This also leaves enough time for the potential to be fully set/reset, as shown in Figure 4 (b).

While the MCCO can in principle provide the desired charging/discharging controls, it has the disadvantage of having four potential floating nodes. These

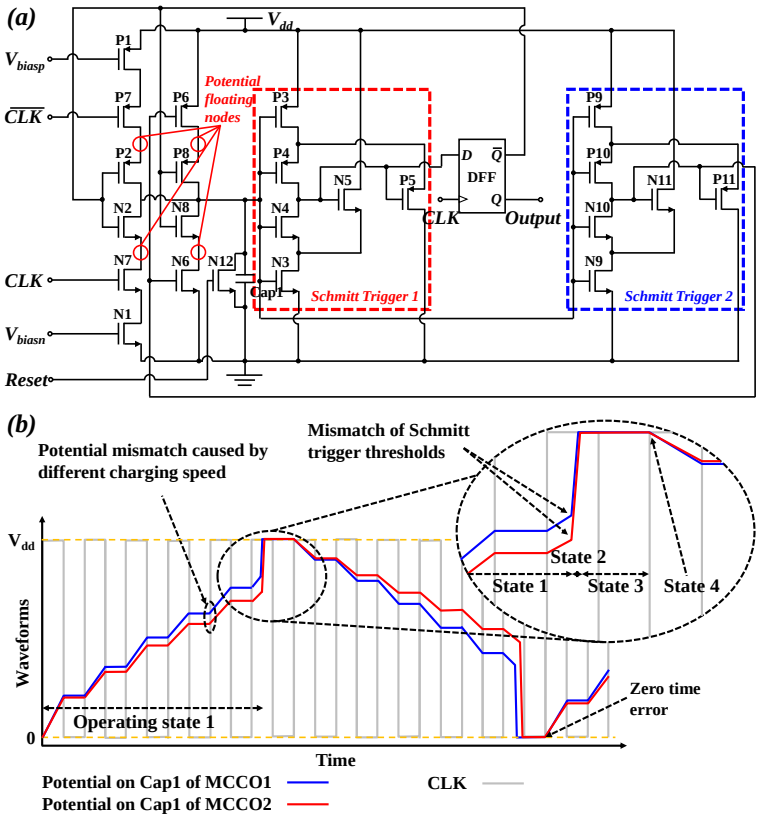


Figure 4: (a) Schematic of the MCCO. (b) An example of the waveforms generated in two fabricated MCCOs (MCCO1&MCCO2) shares the same CLK, V_{biasp} and V_{biasn}.

nodes become floating and accumulate charges if the MOSFETs on both sides are fully turned off.

To solve this problem, the potential control methodologies proposed above are implemented in a different way that uses logic gates to minimize the number of active devices in the charging and discharging routes, as shown in Figure 5 (a), forming the proposed FDDC. OR gates and AND gates are implemented instead of the previous MOS switch combinations. The desired and expected potential waveform on $Cap1$ is similar to the ones shown in Figure 4 (b) and is illustrated in Figure 5 (b). As the DFF is set to enable only the output state change at CLK rising edges, to make sure the capacitor is fully set/reset in

every output signal period, the on-resistances of $P3$ and $N3$ should be designed to allow high enough currents.

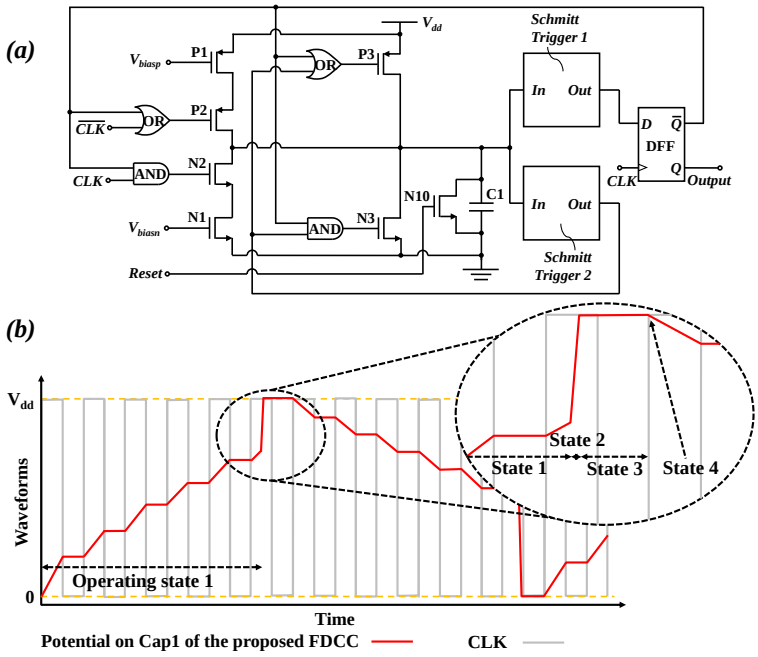


Figure 5: (a) Schematic of the proposed FDCC. (b) An example of the potential waveform of $Cap1$ in an FDCC.

3. Frequency division based on a digitally controlled FDCC

3.1. A digitally controlled FDCC

One way to implement the proposed FDCC as a digitally controlled FDCC is shown in Figure 6. DAC1 and DAC2 are digital-to-analog converters and Control Block can be an on-chip decoder or an (off-chip) external microcontroller that transfers the external control codes to digits/pulses that determine the DAC outputs. The use of DACs builds a bridge between the sophisticated digital control and the FDCC output, it not only can benefit the applications that require fast switching between output frequencies, but also will help the

FDCC to perform fractional division with high output signal quality. This is further discussed in Subsection 3.2.

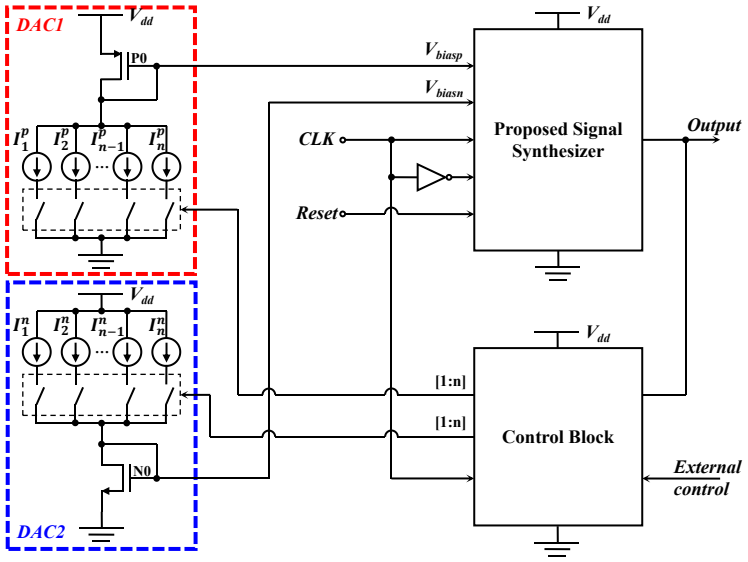


Figure 6: Schematic of a digitally controlled FDCC.

In this case, V_{biasp} is obtained from the current sources in DAC1. Assuming $P0$ in Figure 6 shares the same size with $P1$ in Figure 5, for a charging period covers i ($i = 1, 2, \ldots, n$) CLK cycles (i charging levels/steps), the current I_i^p should theoretically be designed to fulfill:

$$\begin{cases} I_i^p > \frac{C_1 V_{ut2} f_{CLK} \times 105\%}{i \times CLK\ duty\ cycle};\ i \geq 1 \\ I_i^p < \frac{C_1 V_{ut2} f_{CLK} \times 95\%}{(i-1) \times CLK\ duty\ cycle};\ i \geq 2 \end{cases} \tag{3}$$

where V_{ut2} is the upper threshold voltage of ST2; f_{CLK} is the CLK signal frequency and should be a fixed value; and a $\pm 5\%$ variation is allowed for the thresholds, which is conservative enough for most CMOS processes. And the corresponding V_{biasp}^i range can be calculated as:

$$\begin{cases} V_{biasp}^i > \sqrt{\frac{2L_{P1}C_1 V_{ut2} f_{CLK} \times 105\%}{\mu_p C_{OX} W_{P1} i \times CLK\ duty\ cycle}} + V_{dd} + V_{tp};\ i \geq 1 \\ V_{biasp}^i < \sqrt{\frac{2L_{P1}C_1 V_{ut2} f_{CLK} \times 95\%}{\mu_p C_{OX} W_{P1} (i-1) \times CLK\ duty\ cycle}} + V_{dd} + V_{tp};\ i \geq 2 \end{cases} \tag{4}$$

It can be seen from (3) that I_i^p is allowed in a wider range if C_1V_{ut2} is larger, which also relates to an improved PVT tolerance. Furthermore, I_i^p can be designed as the mid-point of its boundaries to provide an optimized performance:

$$\begin{cases} I_i^p = \frac{C_1 V_{ut2} f_{CLK}}{CLK\ duty\ cycle} \times \frac{2i-1.05}{2i(i-1)};\ i \geq 2 \\ I_i^p > \frac{C_1 V_{ut2} f_{CLK} \times 105\%}{CLK\ duty\ cycle};\ i = 1 \end{cases} \tag{5}$$

The current I_k^n for designing DAC2 can be derived by replacing V_{ut2} with $(V_{dd} - V_{lt2})$, where k is the number of discharging levels/steps; V_{lt2} is the lower threshold voltage of ST2.

Note that the DAC noise has to be taken into consideration. Use DAC1 as an example, if the peak-to-peak amplitude of its noise is higher than the minimum voltage range of V_{biasp}^i calculated from (4) (corresponding to the maximum value of i in a specific design), either a DAC architecture with low intrinsic noise or DAC noise shaping techniques should be introduced.

3.2. Frequency division with programmable modulus and output duty cycle control

Frequency division with programmable integral modulus can be directly achieved with the circuit shown in Figure 6. By adjusting V_{biasp} and/or V_{biasn} with DACs, the output signal frequency and duty cycle are tuned. The frequency division modulus (N) and output signal duty cycle can be calculated as:

$$\begin{cases} N = i + k \\ Duty\ cycle = \frac{i}{N};\ Resolution = \frac{1}{N} \end{cases} \tag{6}$$

This is the same as setting V_{biasp} and V_{biasn} to be:

$$\begin{cases} V_{biasp} = \sqrt{\frac{2L_{P1}I_i^p}{\mu_p C_{OX} W_{P1}}} + V_{dd} + V_{tp} \\ V_{biasn} = \sqrt{\frac{2L_{N1}I_k^n}{\mu_n C_{OX} W_{N1}}} + V_{tn} \end{cases} \tag{7}$$

Furthermore, if 50% duty cycle is required for odd moduli, the architecture in Figure 7 can be implemented.

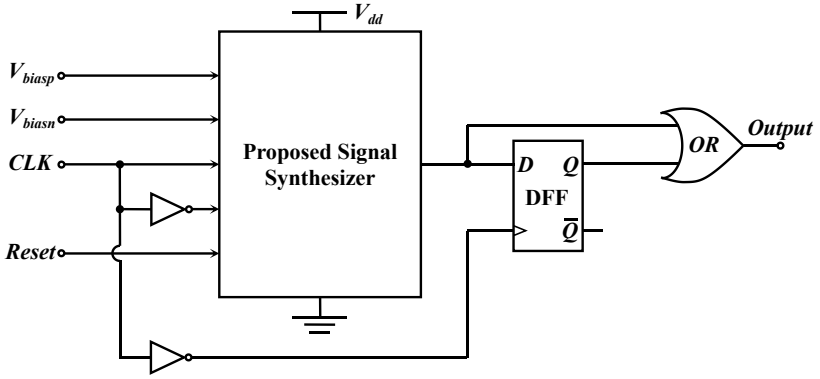


Figure 7: Schematic of an FDCC for 50% duty cycle odd moduli divisions.

3.3. Programmable fractional division

Fractional-N division can be realized by dithering the modulus of the architecture in Figure 6 with a $\Sigma\Delta$ modulator. Noting that the tuning of V_{biasp} should only be done when the output signal is at logic low level, so that the frequency is switched without generating unintended waveforms. On the other hand, the tunning of V_{biasn} should be done in the complimentary manner. A digital-to-time converter [5] can be adopted to improve the phase noise and jitter performance, with the digitally controlled FDCC operating as a multi modulus divider.

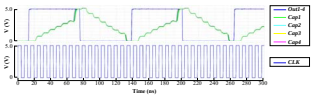
4. Simulation results

The architecture in Figure 5 was implemented on a 5-V, 0.35-μm AMS CMOS process (Table 1) to form a 1×4 FDCC array, and the layout of which was simulated with a Monte Carlo (MC) approach in Cadence. Clocked at 128 MHz, V_{biasp} and V_{biasn} were tuned to allow a divide-by-16 operation with 50% output signal duty cycle. The results of 100 instances of MC simulation are illustrated in Figure 8, which demonstrates the performance of the FDCC against process variations.

$Out1 \sim 4$ waveforms correspond to the output signals from the four FDCCs

Table 1: Specifications of the FDCCs

Technology $[nm]$	V_{dd} $[V]$	Power consumption per FDCC*	Area per FDCC $[mm^2]$	Aspect ratio (W/L)				Threshold voltage $[V]$	
				P1	N1	P3	N3	V_{ut2}	V_{lt2}



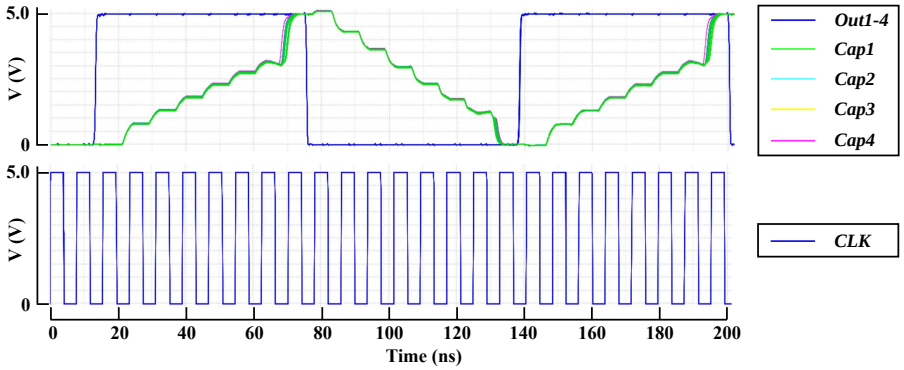


Figure 8: The simulated result of the prototype 1×4 FDCC array clocked at 128 MHz (CLK); $Out1 \sim 4$ are the output waveforms from per-FDCC output pads and $Cap1 \sim 4$ are the potentials on per-FDCC capacitors.

and the $Cap1 \sim 4$ waveforms represent the potential on per-FDCC capacitors. It can be observed that all four outputs are tightly synchronized at 8 MHz despite the variations on potential waveforms due to process variations. The charging and the discharging of the capacitor each start one period after the output state has changed, mainly because the propagation delay of the DFF at the output is comparable with the CLK period. This has a positive effect as one less charging and discharging steps are required to realize the divide-by-16 operation. Higher gate-to-source voltages could then be applied to P1 and N1, which improve the matching performance between current mirrors in different FDCCs. To remove this effect, delay periods equal to the DFF propagation delay should be added to CLK and $\overline{CLK}$ before being input to the OR and

AND gates that control P2 and N2.

From (3), it is clear that a larger C_1, V_{ut2}, a higher CLK frequency and a lower duty cycle can enhance the tolerance of the FDCC to process variations, generally because these lead to a larger charging current for any fixed modulus.

The digitally controlled FDCC architecture in Figure 6 was then simulated with a TSMC 0.18 μm CMOS process design kit. Specifications of the FDCC and DACs are given in Table 1 and 2, respectively. An MC approach was used to find I_i^p and I_k^n values that allow a consistent output in 200 instances of MC simulation for $i, k = 5, 6, 7, 8$. Generally, these values compare higher than the theoretical values determined with (5), and this is mainly due to the parasitic capacitors extracted from the layout.

Table 2: Specifications of the digital-to-analog converters

i		5	6	7	8
I_i^p $[\mu A]$	Actual	13.5	11	8.1	6.4
	Theoretical	5.7	4.6	3.9	3.4
k		5	6	7	8
I_k^n $[\mu A]$	Actual	15.5	13	9.9	8.1
	Theoretical	6.6	5.4	4.5	3.9

5. Experimental setup and test results

5.1. ASIC fabrication and experiment setup

The prototype IC was fabricated on a 0.35 μm CMOS Process at AMS. For validation, test points and additional buffers were set around the circuit, with the 440×80 μm^2 structure at the center of the chip forming the 1×4 array, including the FDCCs and row selecting logics, as shown in Figure 9. The output buffer set on-chip allows the ASIC to provide 5 V square waves with 1 mA drive current and ~ 5 pF output load capacitance.

In order to fully explore the FDCC architecture, the methodology presented in Section 3 was not implemented in this prototype and bias voltage signals

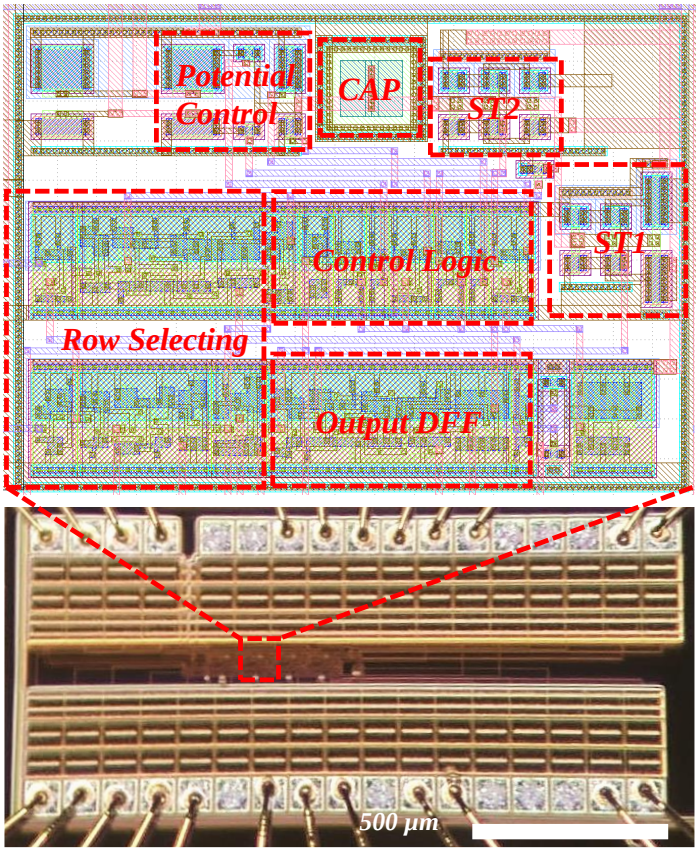


Figure 9: Photomicrograph of the prototype 1×4 FDCC array and detailed layout of an FDCC.

V_{biasp} and V_{biasn} were directly supplied through a precision source/measure unit (B2912A, Keysight technologies). CLK signal was obtained from a PLL device (NB3N502, ON Semiconductor) set on a printed circuit board (PCB) test bench, forming a multi-output signal generator/clock like the architectures presented in [5, 14, 15].

5.2. Electrical testing of the ASIC

To test the frequency division performance, a 128 MHz clock was firstly used to drive the prototype array. By tuning the biasing voltages, divide-by-16 operation was performed in two ways, as shown in Figure 10 (a) (b), with 50%

duty cycle and 56.25% duty cycle, respectively. Figure 11 demonstrates the jitter performance of the 50% duty cycle divide-by-16 operation. It can be calculated that jitter is less than 25 ps_{rms} and this is mainly due to a phase jitter about 24 ps_{rms} from CLK. This proves a stable output frequency from the prototype. A divide-by-14.5 operation (Figure 10 (c)) was realized by periodically tunning V_{biasp}, which proves the methodology proposed in Section 3.3. Furthermore, Figure 10 (c) and Figure 10 (d) demonstrate the instantaneous switching of the output frequency, from 9.14 MHz to 8.53 MHz and 8 MHz, respectively.

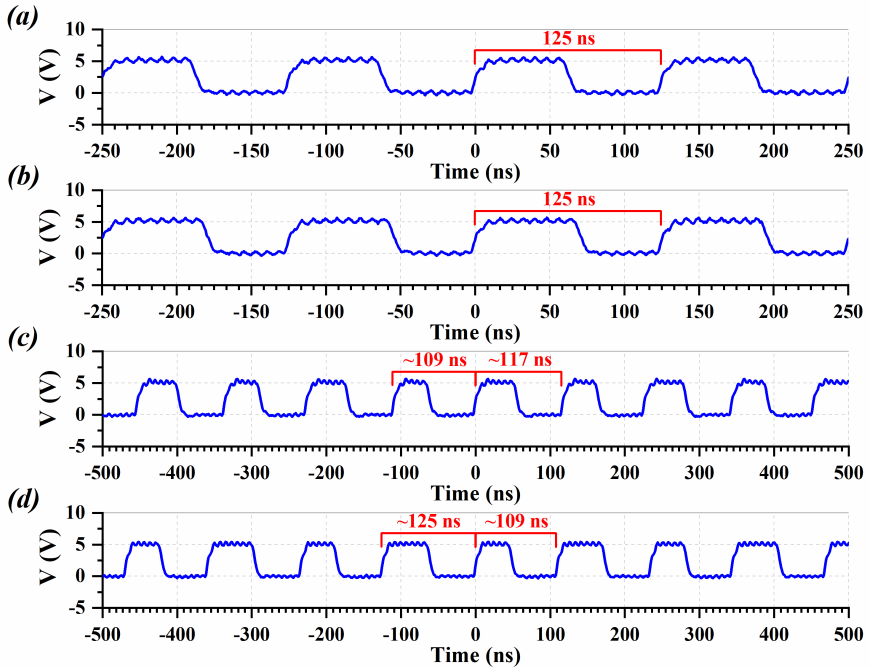


Figure 10: Measured divide-by-16 operations with (a) 50% duty cycle and (b) 56.25% duty cycle. (c) Measured divide-by-14.5 operation. (d) Instantaneous switching of the output frequency from 9.14 MHz to 8 MHz.

Features of the proposed FDCC are further demonstrated in Figure 12. In Figure 12 (a), the number of charging levels is shown as a function of V_{biasp}. The data was obtained by determining the span/range of V_{biasp} that can synchronize all four output signals at virous input and output frequencies, corresponding to

	Max	Min	Mean	RMS	σ (S-dev)	Event count	Wave count
Period	125.1 ns	124.89 ns	124.99 ns	124.99 ns	24.452 ps	100129	100129

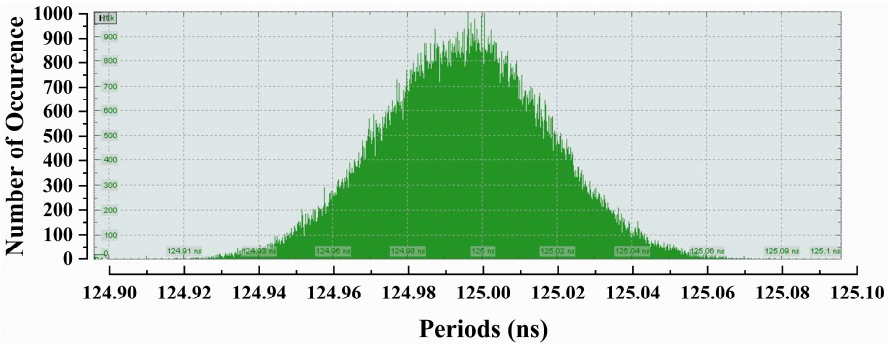


Figure 11: Measured period histogram and period jitter performance.

specific numbers of charging levels. While the measurements were taken for P1, the number of discharging levels was fixed, so that the capability of the driver array to generate asymmetric outputs was validated at the same time. Lower clock frequencies resulted in worse PVT tolerance, as the biasing voltage spans become narrower. The increase in the number of charging/discharging levels also degrades the tolerance for the same reason. This conclusion can also be drawn from (3). The same trend can be observed for the number of discharging levels vs. V_{biasn}, as shown in Figure 12 (b).

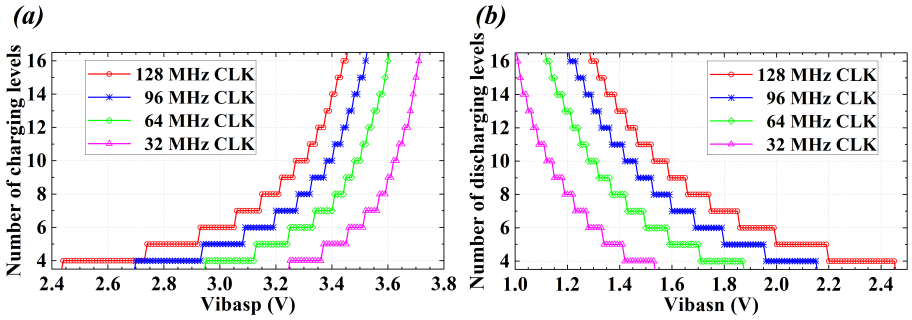


Figure 12: (a) The number of charging levels vs. V_{biasp} values. (b) The number of discharging levels vs. V_{biasn} values. Each point represents a voltage span of 5-mV.

The same testing method was implemented for various power supply voltages

and operating temperatures, with results shown in Figure 13. For this prototype, the real upper and lower thresholds of ST2 can be calculated as $V_{ut2}^r \approx 0.6V_{dd} + 0.4V_{tn} - 0.2|V_{tp}|$ and $V_{lt2}^r \approx 1.25V_{tn} + 0.125|V_{tp}| - 0.125V_{dd}$, respectively [23]. Hence, $+0.5\ V$ change on V_{dd} results in about $+0.3V$ change on upper threshold and about $-0.06\ V$ change on lower threshold. On the other hand, small V_{tn} and $|V_{tp}|$ variations introduced by temperature change are negligible, which meets the output behavior illustrated in Figure 13. For enhanced tolerance, a high-performance Schmitt trigger architecture may be implemented. Table 3 shows the performance summary and comparison to prior frequency dividers. The proposed FDCC offers tunable duty cycle while maintaining high power efficiency and small area occupation. It is also suitable for driving systems that require high-voltage signals ($2 \sim 5\ V$) for transducer excitation, such as acoustic tweezers and imagers. For improved operating frequency, a smaller feature size can be adopted.

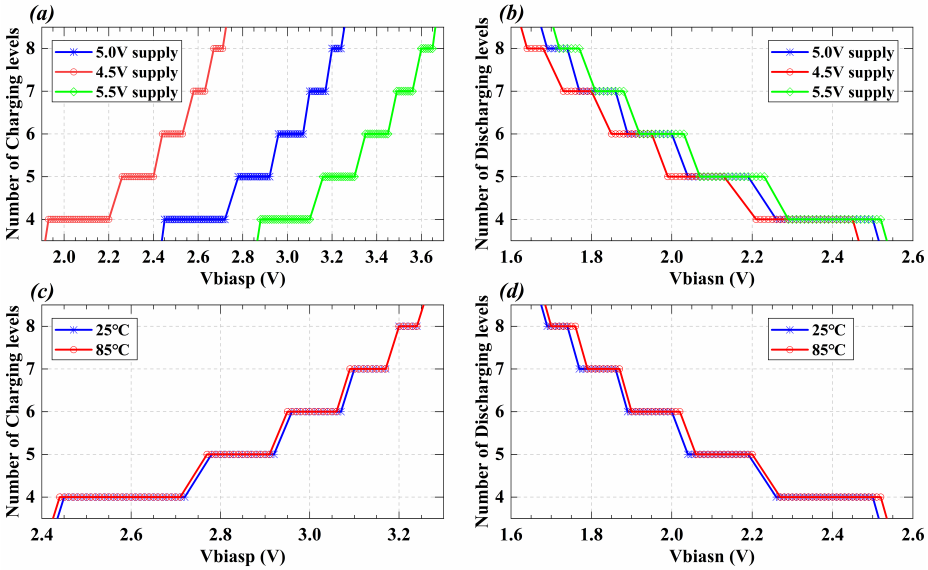


Figure 13: (a) The number of charging levels vs. V_{biasp} values and (b) the number of discharging levels vs. V_{biasn} values for various supply voltages. (c) The number of charging levels vs. V_{biasp} values and (d) the number of discharging levels vs. V_{biasn} values for various operating temperatures.

Table 3: Performance summary and comparisons

Reference	TCAS II'16 [6]	ISCAS '17 [17]	JSSC '18 [5]	TMTT '18 [18]	TCAS II'19 [19]	IEEE Access '20 [20]	TCAS II'20 [21]	**This Work**	
Architecture	Divider based	VCO based	Divider based	VCO based	VCO based	Divider based	Divider based	**VCO based**	**VCO based**
Technology $[nm]$	65	130	65	65	45	180	65	**350**	**180**
Supply $[V]$	0.9	1.2	0.9	1.0	0.5	1.8	1.2	**5.0**	**2.0**
f_{in}, Max $[MHz]$	5325	3000	5000	6500	3040	2300	7140	**128**	**1500**
Modulus Range	–	128-192	5-250	24-80	96-98.5	1-256	5-255	**2-32**	**2-32**
Duty Cycle Range	–	–	–	–	–	–	–	**3.125%-96.875%**	**3.125%-96.875%**
Instantaneous Switching	Yes	No	Yes	No	No	Yes	Yes	**Yes**	**Yes**
Absolute Jitter $[ps_{rms}]$	1.20	1.49	0.93	0.76	2.46	2.25	0.71	**1.45**	**0.73**
Power Consumption	1.2mW @1GHz	1.4mW @12GHz	3.2mW @1GHz	1.03mW @6.5GHz	1.55mW @3.04GHz	3.4mW @2.3GHz	0.68mW @7.14GHz	**0.102mW @0.128GHz**	**0.34mW @1.5GHz**
Power Efficiency $[GHz/mW]$	0.83	8.57	0.31	6.31	1.96	0.68	10.5	**1.26**	**4.41**
Area $[mm^2]$	0.011	–	0.017	0.03136	0.00305	0.0372	0.00373	**0.0051**	**0.001***

*DAC included

5.3. Towards the integration with piezoelectric micromachined ultrasonic transducers (PMUTs)

In order to further demonstrate the functionality of the prototype FDCC array, a PMUT matrix [24] consists of a 2×2 arrangement of acoustic elements was introduced to form an acoustic tweezer. Each element of the PMUT matrix contains nine diaphragms operating at 8 MHz, as shown in Figure 14 (a). The four acoustic elements were driven by four synchronized 8-MHz, 5-V_{pp} unipolar square waves generated from the FDCC array, sending out acoustic waves. To shape the acoustic field, the four FDCCs in the array were set to start at different times (with the help of *Reset*), so that the four signals generated were with different phases. The vibration of the acoustic elements was recorded with a laser Doppler vibrometer, as shown in Fig. Figure 14 (b)&(c). Obvious deflections and four phase quadrants can be clearly observed, which is sufficient

to demonstrate acoustic field shaping and the functional potential of PMUTs

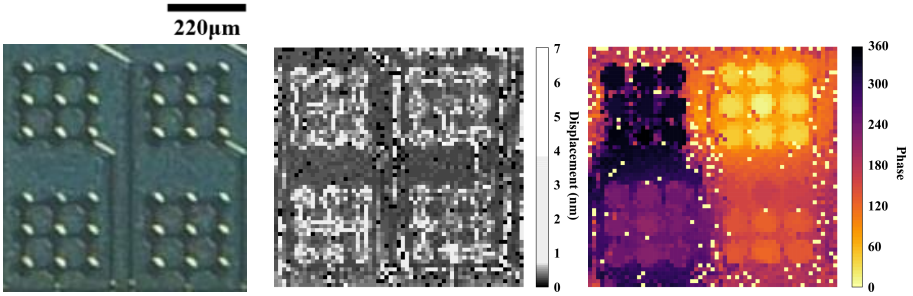


Figure 14: Vibration intensity and phase recorded with a laser vibrometer.

6. Conclusion

This article has reported the design methodology of a CMOS FDCC. The use of such FDCC provides an extra tool of synthesizing signals for system-on-chips and integrated sensor and actuator systems. It also opens up a new way of implementing relaxation oscillator with simple and open-loop topology, which can benefit academic prototyping particularly. Combined with DACs, the proposed FDCC can be implemented as a programmable fractional divider or a digitally controlled FDCC, which allows the control of output duty cycle and the generation of multiphase. A prototype FDCC array has been implemented in a 5-V, 0.35-μm CMOS process. The simulated and experimental results have demonstrated its functionality and shown its performances against PVT variations.

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