Modeling of an Interleaved DC-DC Boost Converter for a Direct Model Predictive Control Strategy

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≪Interleaved converters≫, ≪Modelling≫, ≪MPC (Model-based Predictive Control)≫.

Abstract

This paper presents a model predictive control (MPC) algorithm for interleaved dc-dc boost converters with coupled inductors. The prediction model covers the switching nature of the converter and all possible operating states. The MPC algorithm is realized in MATLAB and designed such to facilitate its real-time implementation on a field programmable gate array (FPGA) using the MATLAB HDL Coder. Open-loop measurement results demonstrate the accuracy of the system model, while the effectiveness of the controller is validated in simulation.

Introduction

The interleaved dc-dc boost converter is a multi-branch converter topology consisting of multiple parallel boost stages, as depicted in Fig. 1. The branches share the input voltage, the output capacitance and—in the case of coupled inductors—the magnetic core, resulting in a compact design. This enables the reduction of the input current ripple and an increase of the output current, as shown in [1], [2]. However, as there is no inherent mechanism to guarantee proper current sharing among the parallel paths a suitable controller is required to address this challenging issue.

Another challenge that a controller needs to deal with is that the output voltage of the boost converter has a non-minimum-phase behavior with respect to the control input, i.e., the switching action. To mask this,

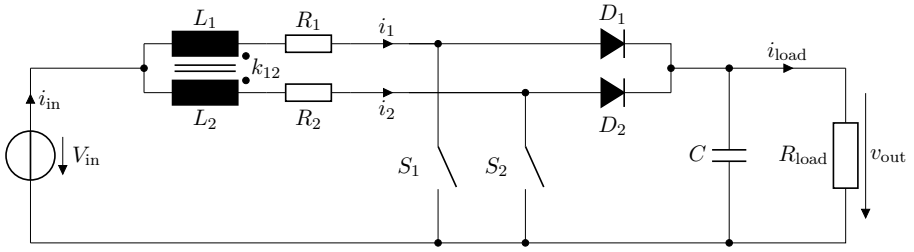


Fig. 1: Interleaved dc-dc boost converter with coupled inductors.

the standard control approach is to design the controller as a current controller, average the continuous-time dynamics associated with the different modes of operation, and to linearize them at the operating point [3], [4]. This, however, complicates the controller design and can potentially deteriorate the dynamic performance.

Direct model predictive control (MPC) with reference tracking—also referred to as finite control set MPC (FCS-MPC)—is a control alternative that can effectively deal with the aforementioned challenges as it allows one to directly include constraints in the design phase and to account for the switching or hybrid nature of dc-dc converters [5]. According to this method, the control inputs are modeled as integers that directly relate to the switch positions of the converter, thus bypassing any modulation stage. Examples of FCS-MPC for dc-dc converters can be found in [6]–[9]. In [6] and [7], FCS-MPC for a dc-dc boost converter is proposed for the direct control of the inductor current and output voltage, respectively. In a similar direction, [8] focuses on FCS-MPC of a single-phase boost converter feeding a constant power load. Finally, an FCS-MPC strategy for an interleaved buck converter with four phases, but without magnetically coupled inductors is presented in [9].

These works clearly demonstrate the advantages of FCS-MPC, such as the great design flexibility and fast dynamic response. Nevertheless, direct manipulation of the converter switches also implies that the optimization problem underlying FCS-MPC is an integer program. A straightforward approach to solve such problems is to use exhaustive enumeration, i.e., to test all candidate solutions before concluding to the optimal one. As integer problems are typically computationally demanding, such a brute-force solution method may not be a realistic option when the number of candidate solutions is not small. To reduce the computational complexity of the associated optimization problem, some methods have been proposed that limit the feasible set [10] or propose nontrivial horizons [11]. Alas, they have been mostly tested on a simulation level [10], [12].

Moreover, considering that the computing time is limited to values smaller than $10\,\mu s$ to achieve a high sampling frequency, and thus enable a high switching granularity [13], a central processing unit (CPU) based control hardware would not be fast enough to test all options in real time within that time interval. A solution is to implement the algorithm on an FPGA, which not only allows for a computationally efficient implementation of the FCS-MPC algorithm, but also facilitates the utilization of a complex model for the interleaved boost converter that fully describes its dynamics.

The above motivates the design of a long-horizon FCS-MPC for the interleaved dc-dc boost converter with coupled inductors that will fully exploit the advantages of FCS-MPC, while facilitating its real-time implementation with a system model covering all physically feasible operating states. To this aim, a detailed model of the converter of interest is first derived that is suitable for all physically feasible operating states. Specifically, the discrete-time model of the converter is designed such that it accurately predicts the plant behavior when operating both in continuous (CCM) and discontinuous conduction mode (DCM). Subsequently, an FCS-MPC strategy is designed as a voltage-mode controller with the main control objectives of regulating the output voltage, balancing the phase leg utilization and limiting the phase currents. Such a control method offers design simplicity as it directly addresses the voltage control problem—and thus non-minimum-phase nature of the converter—without requiring additional control loops, while simultaneously meeting additional control objectives. The presented experimental results based on a low-voltage test bench demonstrate the validity of the proposed model, while simulation results highlight the advantages of the presented control strategy.

System Model

The interleaved boost converter with coupled inductors, shown in Fig. 1, is a dc-dc converter that boosts the input voltage to a higher output voltage. Each converter branch $n \in \{1, 2\}$ consists of a diode D_n and an active switch S_n. Each switch S_n can be controlled actively, whereas diode D_n conducts current depending on the applied voltage. In doing so, the current can be stored in the coupled inductors and, subsequently, deliver energy to the output, thus boosting its voltage value. These coupled inductors L_1 and L_2 and their mutual coupling k_{12} can be modeled by utilizing the equivalent Y-model with mutual

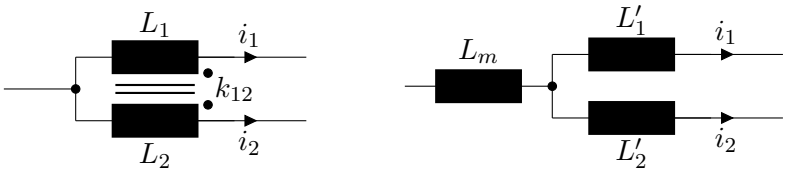


Fig. 2: Coupled inductors and equivalent Y-model.

inductance L_m and uncoupled inductances $L_1' = L_2' = L'$, as shown in Fig. 2. In doing so, the inductances can be mathematically described as follows

$$L_m = k_{12}\sqrt{L_1 L_2}\,, \tag{1a}$$
$$L_1' = L_1 - L_m\,, \tag{1b}$$
$$L_2' = L_2 - L_m\,. \tag{1c}$$

The system model of the interleaved boost converter with coupled inductors differs from the system model of a standard boost converter in two major ways. Firstly, by interleaving, the system state should account for the branch currents, e.g., in the case of two branches, the state vector is chosen to be $\boldsymbol{x} = [i_1\ i_2\ v_{\text{out}}]^T$, with v_{out} being the output voltage. Secondly, by coupling the inductors, a change of the inductor current i_1 induces a voltage in the second winding, thus affecting branch current i_2, and vice versa.

The switch positions of S_1 and S_2 are modeled by the binary variables $u_1, u_2 \in \mathcal{U} = \{0, 1\}$, respectively, together forming the input vector $\boldsymbol{u} = [u_1\, u_2]$. In total, four distinct operating modes can be identified for each branch individually. The state machine in Fig. 3 visualizes the system states and the transitions for a single branch.

Within every discrete time interval T_s each converter branch is in one of the four modes, resulting in a total of 16 possible operating modes. In the following, the operating modes are denoted with a symbolic (XY), where X and Y indicate the operating mode of the first and second converter branch, respectively. With switch S_n on, i.e., $u_n = 1$, the respective branch operates in mode ① with current i_n increasing and always being larger than 0. For all remaining modes it holds that $u_n = 0$. In mode ② the corresponding current is decreasing, still being larger than zero, i.e., $i_n(k+1) > 0$. Mode ③ is an intermediate state of modes ② and ④, in which the branch current falls to 0 A, i.e., $i_n(k+1) = 0$. Finally, in mode ④ the current remains 0. An illustrative example of combined modes for the two-branched system is shown in Fig. 4. In addition, all modes (except mode ③) with the corresponding current paths (—) are depicted in detail in Fig. 5.

The system matrices for mode ③ are calculated by linearly averaging modes ② and ④, weighted with

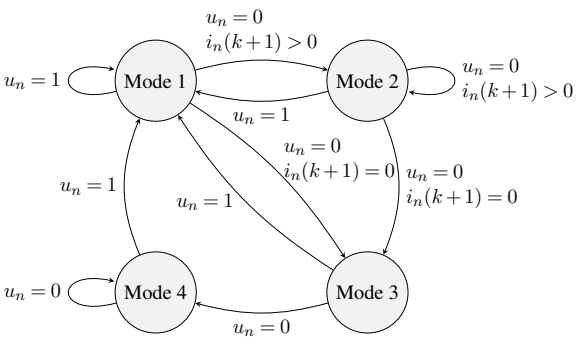


Fig. 3: State machine of branch n [7].

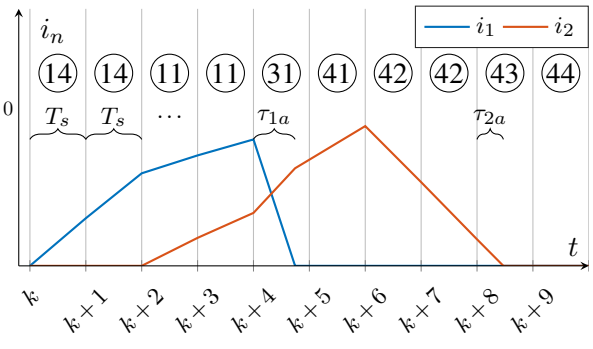
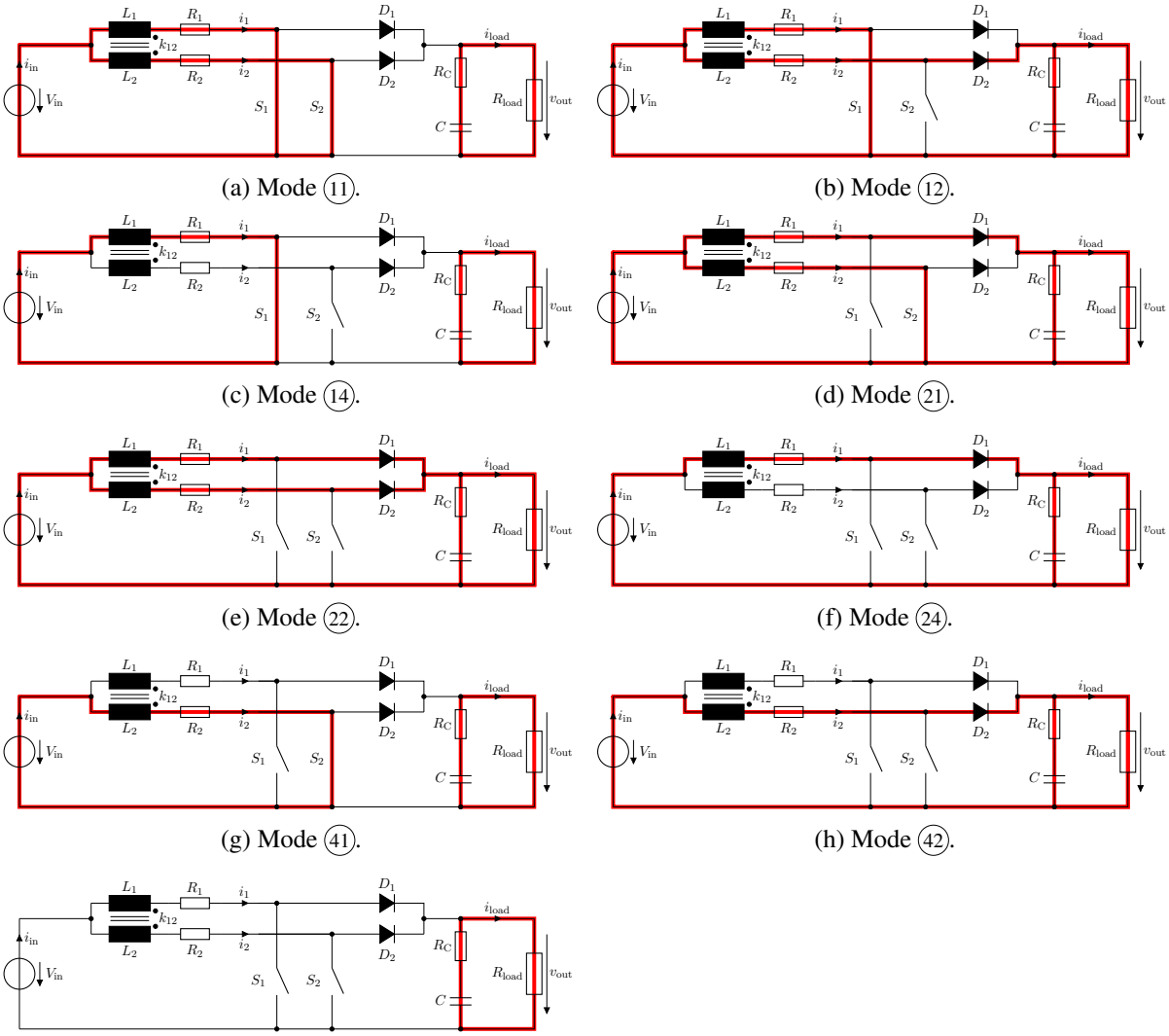


Fig. 4: Illustrative subset of modes of interleaved boost converter.



(a) Mode (11). (b) Mode (12).

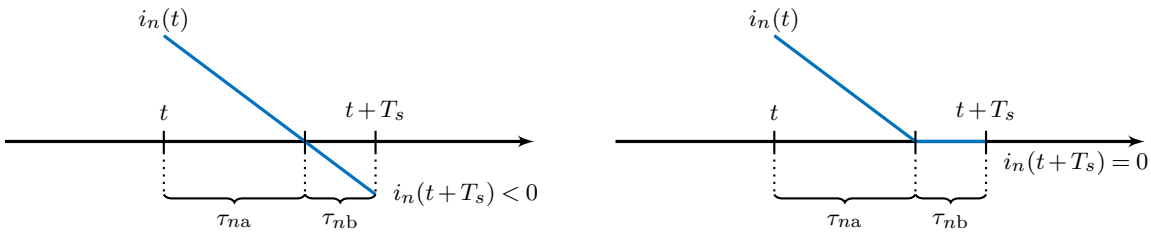
(c) Mode (14). (d) Mode (21).

(e) Mode (22). (f) Mode (24).

(g) Mode (41). (h) Mode (42).

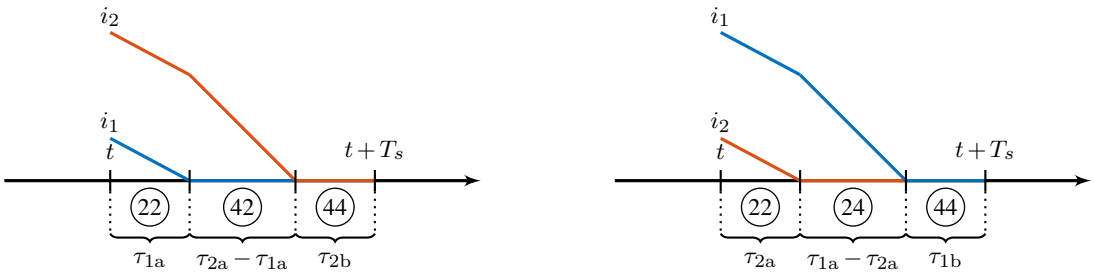
(i) Mode (44).

Fig. 5: Active current paths (—) of the interleaved boost converter in different operating modes.



(a) Current falling below zero in mode (2). (b) Actual current in mode (3).

Fig. 6: Current in mode (3).



(a) Submodes when i_1 reaches 0 A first.

(b) Submodes when i_2 reaches 0 A first.

Fig. 7: Submodes of mode (33).

the duration $\tau_{n\mathrm{a}}$ given by

$$\tau_{n\mathrm{a}} = \frac{i_n(k)}{i_n(k) - i_n(k+1)}\, T_s\,. \tag{2}$$

This interval is the time in which the respective branch current is greater than 0 A, as shown in Fig. 6. Based on that, $\tau_{n\mathrm{b}}$ can be obtained as $\tau_{n\mathrm{b}} = T_s - \tau_{n\mathrm{a}}$. This is calculated online, assuming operation in mode (2). If a zero-crossing of the branch current is detected, the operation mode is changed to mode (3).

To further clarify this point, consider as an example mode (3Y). For this mode it holds that

$$\boldsymbol{A}_{(3Y)} = \left(\boldsymbol{A}_{(4Y)} + \tau_{1a}/T_s \left(\boldsymbol{A}_{(2Y)} - \boldsymbol{A}_{(4Y)}\right)\right). \tag{3}$$

In mode (33), both currents fall to 0 A within the same interval. This leads to three distinct intervals within one sampling period, as illustrated in Fig. 7. It can be seen that there are two variants of mode (33), depending on which branch current falls to 0 A first. For example, for the case depicted in Fig. 7a, it holds that

$$\boldsymbol{A}_{(33)} = \frac{1}{T_s}\left(\tau_{1a}\boldsymbol{A}_{(22)} + (\tau_{2a} - \tau_{1a})\boldsymbol{A}_{(42)} + \tau_{2b}\boldsymbol{A}_{(44)}\right). \tag{4}$$

Given all the above, the system model is derived as a bi-linear state space model of the form

$$\frac{\mathrm{d}\boldsymbol{x}}{\mathrm{d}t} = \boldsymbol{A}(\boldsymbol{x}, \boldsymbol{u})\,\boldsymbol{x}(t) + \boldsymbol{B}(\boldsymbol{u})\,. \tag{5}$$

The state matrix $\boldsymbol{A}$ is given in (6). The individual entries, which depend on the switching state u_n and the branch current i_n are provided in Table I.

$$\boldsymbol{A} = \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \\ A_{31} & A_{32} & A_{33} \end{bmatrix} \tag{6}$$

As for the entries of the input matrix $\boldsymbol{B}$, these are

$$\boldsymbol{B}_{(11)(22)(12)(21)} = \begin{bmatrix} \frac{L'}{D} \\ \frac{L'}{D} \\ 0 \end{bmatrix} V_{\mathrm{in}}, \quad \boldsymbol{B}_{(14)(24)} = \begin{bmatrix} \frac{1}{L_m + L'_1} \\ 0 \\ 0 \end{bmatrix} V_{\mathrm{in}}, \quad \boldsymbol{B}_{(42)(41)} = \begin{bmatrix} 0 \\ \frac{1}{L_m + L'_1} \\ 0 \end{bmatrix} V_{\mathrm{in}}, \quad \boldsymbol{B}_{(44)} = \boldsymbol{0} \tag{7}$$

Finally, as the controller is designed in the discrete-time domain, in a subsequent step, the continuous-

Table I: Entries of matrix $\boldsymbol{A}$ depending on operating mode, with $D = L'(2L_m + L') = (L' + L_m)^2 - L_m^2$.

Mode	A_{11}	A_{12}	A_{13}	A_{21}	A_{22}	A_{23}	A_{31}	A_{32}	A_{33}
(11)	$-\frac{(L_m+L')R}{D}$	$\frac{L_m R}{D}$	0	$\frac{L_m R}{D}$	$-\frac{(L_m+L')R}{D}$	0	0	0	$-\frac{1}{CR_{\text{load}}}$
(22)	$\vdots$	$\vdots$	$-\frac{L'}{D}$	$\vdots$	$\vdots$	$-\frac{L'}{D}$	$\frac{1}{C}$	$\frac{1}{C}$	$\vdots$
(12)	$\vdots$	$\vdots$	$\frac{L_m}{D}$	$\vdots$	$\vdots$	$-\frac{L_m+L'}{D}$	0	$\frac{1}{C}$	$\vdots$
(21)	$-\frac{(L_m+L')R}{D}$	$\frac{L_m R}{D}$	$-\frac{L_m+L'}{D}$	$\frac{L_m R}{D}$	$-\frac{(L_m+L')R}{D}$	$\frac{L_m}{D}$	$\frac{1}{C}$	0	$\vdots$
(14)	$-\frac{R}{L_m+L'}$	0	0	0	0	0	0	0	$\vdots$
(41)	0	0	0	0	$-\frac{R}{L_m+L'}$	0	0	0	$\vdots$
(24)	$-\frac{R}{L_m+L'}$	0	$-\frac{1}{L_m+L'}$	0	0	0	$\frac{1}{C}$	0	$\vdots$
(42)	0	0	0	0	$-\frac{R}{L_m+L'}$	$-\frac{1}{L_m+L'}$	0	$\frac{1}{C}$	$\vdots$
(44)	0	0	0	0	0	0	0	0	$-\frac{1}{CR_{\text{load}}}$

time system matrices are discretized using forward Euler method. This yields

$$\boldsymbol{x}(k+1) = (\boldsymbol{I} + \boldsymbol{A}T_s)\,\boldsymbol{x}(k) + \boldsymbol{B}T_s \tag{8}$$

with T_s being the sampling interval.

In the next section, the proposed converter model is verified experimentally.

Model Verification

The proposed model is tested using the FPGA-based open-source control platform UltraZohm [14], [15], which is depicted in Fig. 8. The platform enables rapid control prototyping of power electronic systems. The calculation unit is a Xilinx Zynq UltraScale+ 9EG MPSoC that consists of several ARM processors and an FPGA on the same silicon chip. The platform is expandable with adapter cards that offer digital and analog interfaces to the converter and sensor. For FPGA hardware development Xilinx Vivado Design Suite is used. The software for the generated hardware processor is programmed with Xilinx Vitis.

Fig. 9 shows the prototype of the coupled inductors, while Table II presents the parameters of the interleaved boost converter. A power inverter board equipped with gallium nitride (GaN) transistors, shown in Figs. 10 and 11, provides the switching cells. The GaN inverter adapter card offers three half-bridges

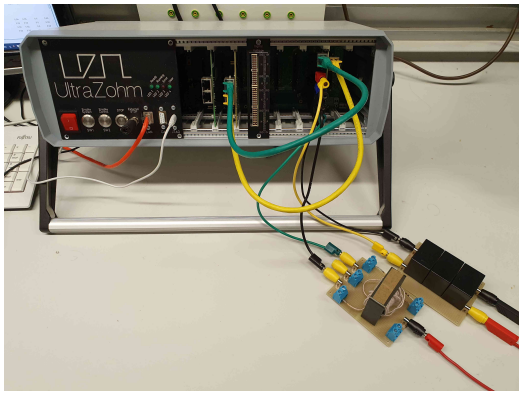


Fig. 8: Experimental setup with UltraZohm.

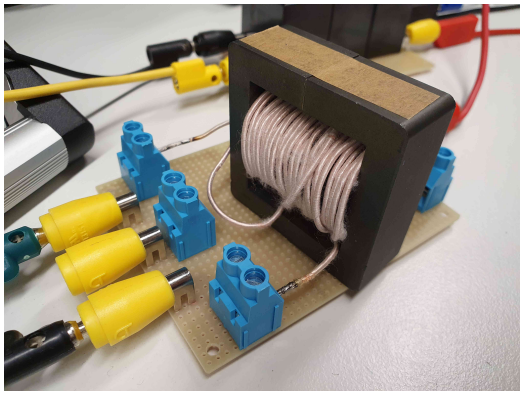


Fig. 9: Coupled inductors prototype.

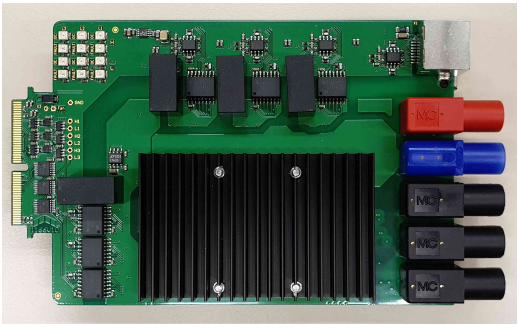


Fig. 10: GaN adapter card top side.

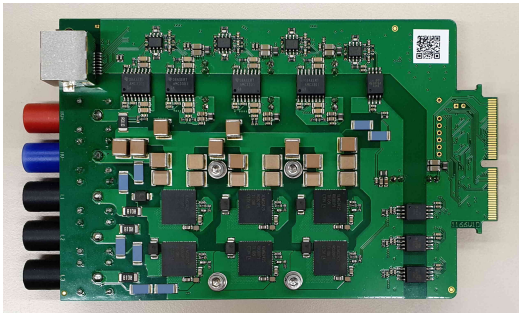


Fig. 11: GaN adapter card bottom side.

with a shared dc-link, originally designed for drive applications. It is compatible with the digital adapter slots of the UltraZohm system, easing the initial setup effort. The power switches are fully integrated with logic level input drivers and protection against over-current. The availability of phase current, phase voltage, and dc-link voltage measurements allows for use with various control schemes.

In the preliminary experimental setup, push-pull stages are used, i.e., D_1 and D_2 are replaced with active switches, limiting the set of operating modes to only ⑪, ⑫, ㉑, and ㉒, leading to a forced CCM type of operation. Here, a more reasonable approach to not drive the top-side switches in each half-bridge, and thus yield a diode-like behavior, was not recommended by the manufacturer of the power switches [16]. As such, the top-side switches are driven with the inverse signal of the respective bottom-side switches, leading to the aforementioned forced CCM.

With this setup, the presented mathematical model is verified by applying a pre-calculated switching sequence directly to the switches, resulting in an open-loop start-up operation. The parameters of the open-loop experiment are provided in Table III. The sampling frequency is chosen to be $50\,\mathrm{kHz}$, resulting in an average switching frequency of $18.625\,\mathrm{kHz}$. A comparison of the simulated start-up with the corresponding measurements is depicted in Fig. 12. As can be seen, there is a close matching between the simulated and experimental output voltage v_{out}, shown in Figs. 12a and 12b, respectively. Moreover, the simulated and experimental input current i_{in} depicted in Figs. 12c and 12d, respectively, shows a comparable pattern that corroborates the validity of the derived model.

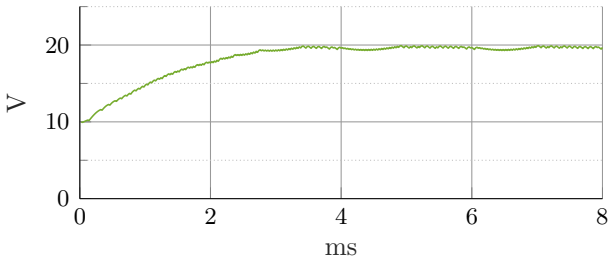
The differences in the branch currents i_1 and i_2, predicted by the simulation compared to the actual current in the test setup is briefly explained in the following. For this, the branch currents, in addition to the input current, are presented over a shorter time interval to allow for insightful observations, see Fig. 13. In simulation (see Fig. 13a) both branch currents match exactly, whereas Fig. 13b depicts drastically different waveforms. This is an effect caused by the peculiarities of the push-pull topology, in which the timing of the "rectifying" switches becomes critical—in comparison to a topology using conventional diodes. Here, even a small delay of one half-bridge—with respect to the other—will cause a steep change in the currents through both inductances L_1' and L_2', which are, with the coupling factor chosen, in the one-digit µH range. For example, at time $3.22\,\mathrm{ms}$, the sequence of commanded modes is ⑪→㉒, where an additional intermediate mode, i.e., mode ㉑, can be identified that stems from an unwanted delay in the gate driving. During the short time mode ㉑ is active, the output voltage is directly applied to L_1' and L_2', in the negative and in the positive direction respectively, forcing a change of the

Table II: Parameters of interleaved boost prototype.

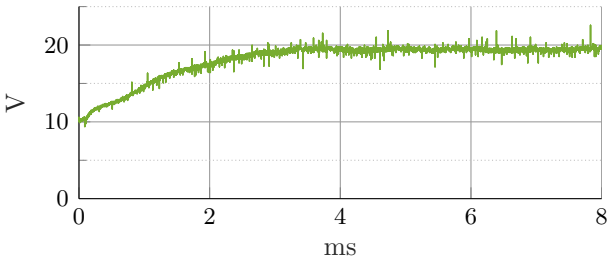
Parameter	Value
L_1, L_2	$190\,\mu\mathrm{H}$
k_{12}	0.993
R_1, R_2	$150\,\mathrm{m}\Omega$
C	$146\,\mu\mathrm{F}$

Table III: Parameters for open-loop measurements.

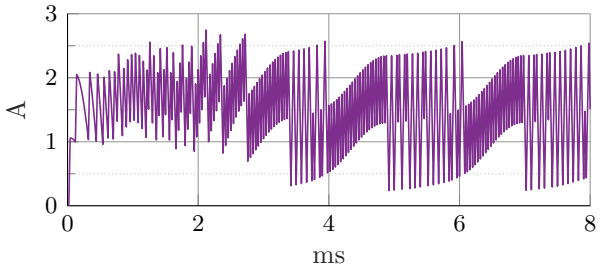
Parameter	Value
V_{in}	$10\,\mathrm{V}$
v_{out}^*	$20\,\mathrm{V}$
R_{load}	$20\,\Omega$



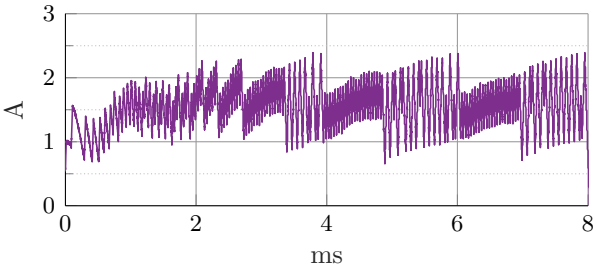
(a) Simulation of v_{out}.



(b) Measurement of v_{out}.

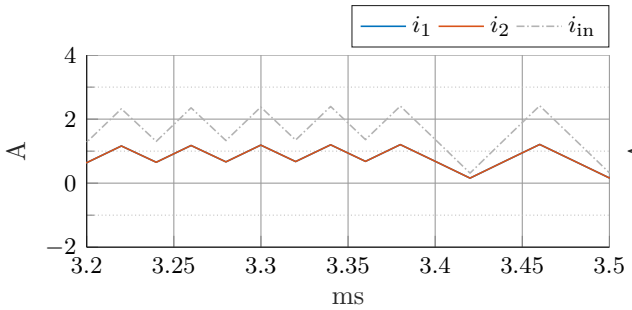


(c) Simulation of i_{in}.

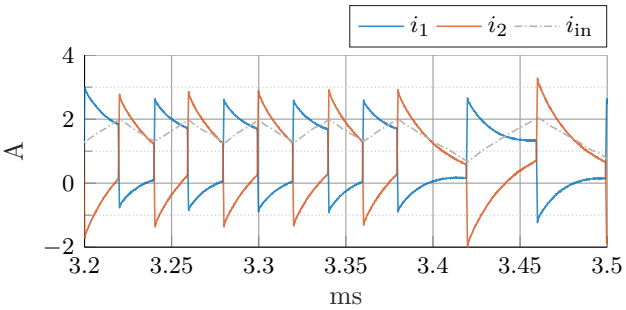


(d) Measurement of i_{in}.

Fig. 12: Comparison between simulation and experimental measurements.



(a) Simulative results.



(b) Experimental results.

Fig. 13: Branch currents i_1 ——, i_2 —— and input current i_{in} ·····.

branch currents according to the voltages applied.

Despite the aforementioned shortcomings of the setup, it can be concluded that the presented results from the *feasible* subset of operating modes clearly demonstrate the validity of the developed model of the converter.

Optimal Control Algorithm

In this section, the previously derived discrete-time model of the converter is leveraged in a direct MPC scheme. In MPC, the control action is obtained online by solving the underlying optimization problem. At each time step, the switching commands are optimized for N time steps ahead in the future, i.e., the prediction horizon, with respect to a given objective function. The formulated optimization problem, besides accounting for the discrete-time model of the system, can account for explicit constraints. The optimal sequence of control inputs is the one that minimizes the objective function. To introduce feedback, and thus deal with model uncertainties and disturbances, only the first element of the optimal sequence of control actions is applied to the converter. The described approach is known in literature as *receding horizon policy* [17]. At the next time step, the optimization problem is solved again with updated measurements.

The objectives of the proposed MPC strategy are the minimization of the difference between the predicted

and the reference output voltage v_{out}^*, i.e., the tracking error, and the minimization of excess branch currents, i.e., currents larger than an upper current bound i_{bnd}. These objectives are mapped into a scalar with the following objective function

$$J(k) = \sum_{\ell=k}^{k+N-1} \left(v_{\mathrm{out}}^*(\ell) - v_{\mathrm{out}}(\ell)\right)^2 + \lambda_i J_i(\ell) + \lambda_b \left| \sum_{m=1}^{k+N-1} i_1(m) - i_2(m) \right| \quad \text{with} \tag{9a}$$

$$J_i(\ell) = \sum_{n=1}^{2} \begin{cases} 0 & i_n(\ell) < i_{\mathrm{bnd}} \\ \left(i_n(\ell) - i_{\mathrm{bnd}}\right)^2 & \text{otherwise.} \end{cases} \tag{9b}$$

It is worth mentioning that in (9a) a third term is added to achieve a balanced utilization of the two converter branches. This term minimizes the difference of the branch currents, $i_1 - i_2$ over the whole operation of the converter, starting from the first time step $m = 1$. Moreover, the weighting factors $\lambda_i, \lambda_b > 0$ are introduced to prioritize among the control goals.

To find the optimal switching sequence that results in the smallest cost $J_{\mathrm{opt}}(k)$ of (9), an exhaustive search is performed at every time step. Algorithm 1 shows the basic structure of the proposed controller with an outer for-loop iterating over all possible switching combinations. An inner loop, that iterates over N, performs the prediction and the cost calculation for each candidate solution. In a final step, the calculated cost is compared with the tentative minimal cost value. If a candidate with a lower associated cost is found, the upper bound of J_{opt} is updated accordingly. Once all candidates have been explored, the switching pattern resulting in J_{opt} is identified as the optimal solution.

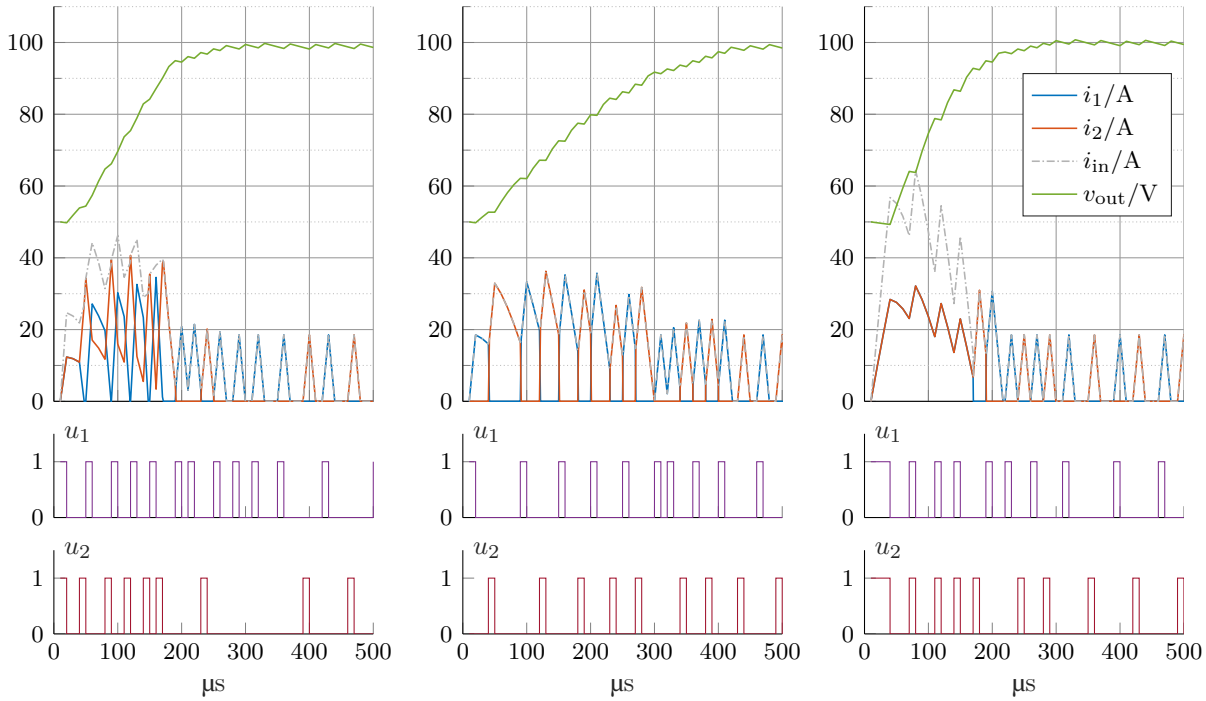
Algorithm 1 Pseudocode of proposed MPC algorithm.

for each $\boldsymbol{U}(k) = \begin{bmatrix} \boldsymbol{u}(k) & \boldsymbol{u}(k+1) & \dots & \boldsymbol{u}(k+N-1) \end{bmatrix}^T \in \mathcal{U}^{2N}$ **do**
    for each step $\ell \in \{1, \dots, N\}$ **do**
        Predict next state based on the operating mode of the converter.
        Calculate intermediate cost.
    end for
    if cost of candidate $\leq J_{\mathrm{opt}}$ **then**
        Update J_{opt}
    end if
end for
return $\boldsymbol{u}^*(k)$

Simulation Results

In this section, the proposed control scheme is scrutinized in a simulation environment. The input voltage of $50\,\mathrm{V}$ is boosted to a reference output voltage of $100\,\mathrm{V}$ at a load of $20\,\Omega$. The sampling and control frequency is $100\,\mathrm{kHz}$, while the switching frequency is variable due to the direct nature of the control scheme. The weighting factors are $\lambda_i = 0.05, \lambda_b = 0.01$, with the soft constraint on the branch current being activated above $i_{\mathrm{bnd}} = 5$. Fig. 14 displays simulation results for a prediction horizon of $N = 3$ and $N = 6$, as well as for two different coupling factors k_{12}. For three exemplary parameter sets, the input current i_{in}, the branch currents i_1 and i_2, and the output voltage v_{out} are plotted. Below, the gate signals u_1 and u_2 are depicted.

It is apparent that the reference output voltage can be tracked accurately in all depicted cases. For $N = 3$, (Figs. 14a and 14b) the algorithm exhibits similar behavior for both coupling factors in steady-state operation. Nevertheless, significant differences can be found when focusing on the output voltage ramp-up section. For $k_{12} = 0.5$, the algorithm chooses operating points that are in CCM, particularly for i_2. This enables a higher input current (with comparable branch currents) and thus speeds up the initial ramp up. For $k_{12} = 0.9$, however, the uncoupled inductances are significantly smaller. As a result, the changes



(a) $N = 3$, $k_{12} = 0.5$. (b) $N = 3$, $k_{12} = 0.9$. (c) $N = 6$, $k_{12} = 0.9$.

Fig. 14: Start-up behavior of the interleaved dc-dc boost converter for different N and k_{12}.

in the current, and thus its ripple, are bigger, leading to a DCM operation. This gives rise to a slower start-up scenario with a slower transient time by a factor of 2. It is noteworthy that the shorter prediction horizon hinders the algorithm to fully align the cost of branch current balancing while achieving output tracking error minimization.

Comparing this behavior with the case where the same coupling factor of 0.9 is used along with a longer prediction horizon of $N = 6$ steps, it can be seen that the proposed direct MPC strategy is able to provide a faster dynamic response. Specifically, the algorithm outputs a symmetric start-up pattern to minimize the cumulative tracking error by means of a faster initial ramp-up, while maintaining perfectly balanced branch currents.

Finally, it is noteworthy that the non-minimum-phase nature of the boost converter is visible in the first simulation steps in Fig.14, where the output voltage drops while the coupled inductors are being magnetized. In simulation, a minimum prediction horizon length of $N = 2$ steps is required to achieve a stable system behavior for the specific problem setting. One possible explanation is that the controller needs to be able to predict past the initial voltage dip caused by the non-minimum-phase behavior [7].

Conclusion

This paper presented a switched model of an interleaved boost converter with coupled inductors that covers all possible operating modes of the two-branched system. To derive an as accurate model as possible, the influence of the coupling of the inductors was included in the model. Based on this model, an FCS-MPC scheme was developed and its effectiveness was validated in a MATLAB simulation. The presented results demonstrate that a favorable operation can be achieved as the horizon length increases, even when the magnetic coupling of the inductors is strong.

In a next step, the experimental setup will be changed with respect to the power switches used to avoid operating limitations and thus enable operation in DCM. Additionally, the controller will be implemented on the FPGA of the open-source control platform UltraZohm. In doing so, the whole control scheme, consisting of the derived model and the presented control algorithm, will be validated in real time.

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