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Epitaxy and characterization of InP/InGaAs tandem solar cells grown by MOVPE on InP and Si substrates

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Abstract. The integration of III-V multi-junction solar cells on Si substrates is currently one of the most promising possibilities to combine high photovoltaic performance with a reduction of the manufacturing costs. In this work, we propose a prospective study for the realization of an InP/InGaAs tandem solar cell lattice-matched to InP on a commercially available Si template by direct MOVPE growth. The InP top cell and the InGaAs bottom cell were firstly separately grown and optimized using InP substrates, which exhibited conversion efficiencies of 13.5% and 11.4%, respectively. The two devices were then combined in a tandem device by introducing an intermediate InP/AlInAs lattice-matched tunnel junction, showing an efficiency of 18.4%. As an intermediate step towards the realization of the tandem device on Si, the InP and InGaAs single junction solar cells were grown on top of a commercial InP/GaP/Si template. This transitional stage enabled to isolate and evaluate the effects of the growth of III-V on Si on the photovoltaic performance through the comparison with the aforementioned devices on InP. Each cell was electrically characterized by external quantum efficiency and dark and illuminated current-voltage under solar simulator. The material quality was also analyzed by means of X-ray diffraction, Atomic-Force Microscopy, Transmission Electron and Scanning Electron Microscopy. The III-V on Si devices showed efficiencies of 3.6% and 2.0% for the InP and InGaAs solar cells, respectively.

Keywords: III-V/Si / NAsP commercial template / InP/InGaAs / MOVPE

1 Introduction

During the last decade, III-V materials based multi-junction solar cells (MJSC) have proven to be one of the most promising efficient solutions to reach high conversion efficiencies. In particular, several records were established for the GaAs technology [1–5] as well as for technologies combining GaAs and InP [6–8].

In comparison, there are only few reports on InP alone [9–11], although it can host a wide range of alloys that are suitable for photovoltaic (PV) use under solar spectrum, covering the whole energy range from 0.76 eV

($In_{0.53}Ga_{0.47}As$) up to 1.42 eV ($Al_{0.48}In_{0.52}As$) [12]. It also presents high electron mobilities at room temperature and high resistance to degradation under high energy irradiation which is particularly appealing for space applications [13,14]. According to Leite et al. [15], an AlInAs/InGaAsP/InGaAs triple-junction device can reach a conversion efficiency larger than 51% for a relatively low 100 suns illumination.

In order to render III-V semiconductors technology competitive at industrial level, a significant cost reduction is required [16]. In this regard, the use of Si substrates as 1.1 eV bandgap bottom cells [17] has already shown excellent results [18,19].

The most efficient III-V/Si PV devices fabricated to date were made by non-epitaxial techniques such as wafer-bonding and mechanical stacking [20,21]. These techniques

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allow to partly overcome the typical III-V/Si epitaxial problems such as lattice and thermal mismatch, as well as the presence of polar/non-polar interfaces. However, they present some limitations related to the use of high-priced III-V substrates, which should be removed and reused in order to make them cost-effective. In addition, these non-epitaxial techniques imply longer and more difficult device processing, which makes them strongly challenging for industrial integration. Moreover, the final dimensions of these devices are limited by the reduced size of the III-V substrates of only a few inches in diameter.

Conversely, direct epitaxial growth guarantees faster and straightforward implementation of larger devices [22]. On this subject, several successful attempts of epitaxial growth of III-V materials on InP substrates for PV applications are reported in literature [23,24]. Lumb et al. [25] reported a grown and optimized InGaAs solar cell lattice matched to InP, for use as a fourth junction in high efficiency InGaP/GaAs/InGaAsNSb triple junction solar cell.

The first works which appear in the literature concerning direct epitaxial growth of InP on Si date back to the 90's when the interest for the developing of solar cells for space applications was substantial. According to Wojtczuk et al. [26] InP-on-Si cells were fabricated to combine the lightweight of Si wafers with the radiation-hardness of InP solar cells to achieve a high end-of life power density.

All the current conversion efficiency records for III-V/Si solar cells were obtained by using III-V materials lattice-matched to GaAs. Nevertheless, this family lacks low-bandgap materials required for high-efficiency double-junction solar cells [27], except for the dilute nitride alloys, which are difficult to grow at high crystalline quality by MOVPE. Consequently, this approach requires the development of a Si bottom cell to absorb the infrared portion of the incident spectrum.

The InP technology has a wide range of possibilities for the realization of a low-bandgap bottom cell at energies significantly lower than Si, which, in turn, can be very useful for PV applications. An InP-based heterostructure, where the individual cells made of ternary or quaternary material are properly chosen from the AlGaInAs or GaInAsP alloy families, can perfectly match the solar spectrum and lead to high-efficiency solar devices [15].

Ideally, this growth could be performed on a metamorphic buffer layer onto large and easily available Si wafers. This would pave the way to a new generation of solar cells combining the advantages of III-V/Si integration, namely an efficient energy band engineering and reduced costs, to the InP technology, which allows the fabrication of bottom cells lattice-matched to the overlying cells, and to direct growth, which would lead to an efficient use of materials and large substrates.

In the first part of this work, the main objective is the experimental demonstration of an InP/InGaAs tandem solar cell (TSC) on an InP wafer as an intermediate step towards the realization of an optimized triple junction solar device. InP/InGaAs TSCs provide a bandgap combination very close to the optimum efficiency for a double-junction solar cell with AM1.5D spectrum at high concentration. Given the bandgaps of InP (1.34 eV) and $In_{0.53}Ga_{0.47}As$ (0.76 eV) constituting the two sub-cells, a

theoretical limiting efficiency of ~32% can be reached for the tandem cell [28].

We have first fabricated and characterized the two single junction cells (SJCs) grown on InP substrates. Then, we have combined them into a tandem device fabricated on an InP substrate, by including an intermediate, transparent InP/AlInAs tunnel junction previously presented in [29].

In the second part, we intended to reproduce the whole process on commercially available InP/GaP/Si templates from NAsP company [30], in order to evaluate the impact of the metamorphic InP buffer relaxation onto device performance. This latter was structurally characterized, and the PV performance of the resulting solar cells was evaluated and compared with the previous devices developed on InP substrates.

A commercially available Si template has been preferred to prove the feasibility of realization of III-V TSCs on low-priced and easily accessible substrates with a view to propose new strategies for the development and reducing the production cost on 300 mm Silicon platform.

2 Design of the structure

Table 1 shows the epitaxial layer structures of the InP and $In_{0.53}Ga_{0.47}As$ p^+n SJCs with the relative doping concentrations. A p^+n structure was chosen since this configuration allows a simpler deposition process and treatment of the back contact with respect to a n^+p structure, as widely described and reported in [31]. The epitaxial layer structures were grown on (n) InP substrates. Both devices present an (n^+) InP layer of 700 nm and 400 nm for the InP and InGaAs SJCs, respectively, which acts both as back surface field (BSF) and as buffer layer. Compared to the literature [32], where typically bases are 5 μm thick, an (n) InP and (n) $In_{0.53}Ga_{0.47}As$ base with a thickness of 3 μm was used. This was intended to reduce the total epitaxial thickness of the future TSC and consequently decreasing the total stress of the structure, despite the negative impact on the overall radiation absorbed by the device and therefore on the produced photocurrent. The emitter consists in (p^+) InP and (p^+) $In_{0.53}Ga_{0.47}As$ layers with a thickness of 150 nm and 200 nm, respectively. A window layer of (p^+) $Al_{0.48}In_{0.52}As$ (1.44 eV) and (p^+) $Al_{0.31}In_{0.53}GaAs$ (1.2 eV) has been included in the InP and InGaAs SJCs structure, respectively. Window layers with higher band gap than the base have been chosen in order to reduce the surface recombination [33]. In both devices, a (p^+) InP etch-stop layer was introduced to protect the window layer during the etch of the (p^{++}) $In0_{.53}Ga_{0.47}As$ contact layer.

On top of InP solar cells is deposited an anti-reflecting coating (ARC) of Si_3N_4 with a thickness of 115 nm. The optimal thickness was calculated in order to minimize the reflection at the wavelength of maximum absorption of InP (925 nm). In the microelectronics field, a SiN_x layer is typically used to passivate and protect the exposed junction surfaces in InP/InGaAs heterojunction bipolar transistors [34]. The passivation layer reduces surface recombination and enhances long-term and thermal stability of InP surfaces, significantly expanding the temperature window for InP device processing [35,36].

Table 1. Structure of the p^+n single junction InP top cell (up) and InGaAs bottom cell (down).

Layer	Material	Thickness (nm)	Doping level (cm^{-3})
Contact	(p^{++}) $In_{0.53}Ga_{0.47}As$	200	$+2 \times 10^{19}$
Etch-stop	(p^+) InP	10	$+1.5 \times 10^{18}$
Window	(p^+) $Al_{0.48}In_{0.52}As$	25	$+1.5 \times 10^{18}$
Emitter	(p^+) InP	150	$+1 \times 10^{18}$
Base	(n) InP	3000	-1×10^{17}
BSF	(n^+) InP	700	-2×10^{18}
Substrate	(n) InP	∞	-2×10^{18}
Layer	Material	Thickness (nm)	Doping level (cm^{-3})
Contact	(p^{++}) $In_{0.53}Ga_{0.47}As$	250	$+2 \times 10^{19}$
Etch-stop	(p^+) InP	10	$+1.5 \times 10^{18}$
Window	(p^+) $Al_{0.31}In_{0.53}Ga_{0.16}As$	30	$+1.5 \times 10^{18}$
Emitter	(p^+) $In_{0.53}Ga_{0.47}As$	200	$+1 \times 10^{18}$
Base	(n) $In_{0.53}Ga_{0.47}As$	3000	-1×10^{17}
BSF	(n^+) InP	400	-2×10^{18}
Substrate	(n) InP	∞	-2×10^{18}
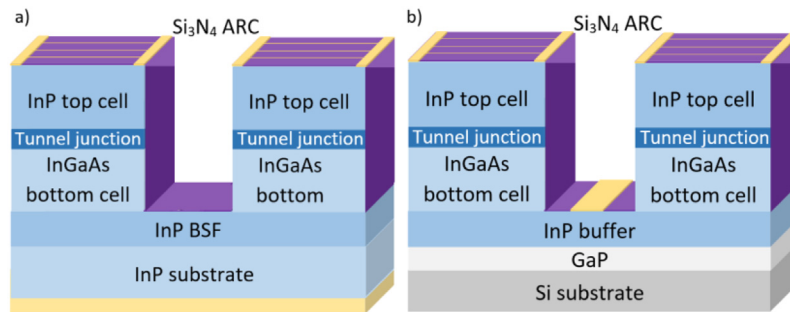
Fig. 1. Sketch of the tandem solar cell fabricated on InP (a) and on Si (b) Substrates, respectively. The tandem on Si back contact is shown as a bus-bar located in the perimeter since the contact cannot be directly made on the back of the sample, it is deposited on the bottom of the mesas (on n^+ InP buffer), between each cell.

The two devices were then combined in a tandem device by introducing an intermediate $(n^{++})InP/(p^{++})Al_{0.48}In_{0.52}As$ tunnel junction. A sketch of the TSCs on InP and Si substrates is reported in Figure 1.

Minor variations have been made on the SJCs for the fabrication of the TSC. In particular, the bottom BSF was increased from 400 to 600 nm to enlarge the buffer zone between the substrate and the base, in order to reduce the surface recombination velocity since a lower crystalline quality was expected in the first layers of the epitaxy. Moreover, the contact and the etch-stop layers of the InGaAs bottom cell were removed since they were no longer necessary thanks to the integration of the top cell. Finally, the top BSF layer was in turn reduced from 700 to 500 nm in order to reduce the total thickness of the epitaxial stack.

3 Experimental

The samples presented in this work were all grown in a vertical MOVPE Aixtron Close-Coupled-Showerhead reactor at a 150 mbar pressure. The substrates were two inches (0 0 1) n-type InP wafers or InP/GaP/Si templates diced from a 300 mm commercial wafer [30,37]. The used precursors were trimethylindium (TMIn), trimethylgallium (TMGa), trimethylaluminum (TMAl), phosphine (PH_3) and arsine (AsH_3) under hydrogen (H_2) flow. The n-type dopant was Si (from disilane, Si_2H_6, precursor), whereas the p-type dopant was Zn (from diethylzinc, DEZn, precursor). For the tunnel junction, the n and p-type dopants were S (from hydrogen sulfide, H_2S, precursor) and C (from carbon tetrabromide, CBr_4, precursor), respectively. The growth temperatures were 630 °C for the n-type layers and 600 °C for the p-type layers. The growth conditions for the tunnel junction are somewhat different from the rest of the cell and they have been thoroughly described elsewhere [29]. The InP/AlInAs tunnel junction allows to reach a high peak tunneling current of 1570 A/cm^2 at voltages between 120 mV and 160 mV, thus suggesting very low losses under tandem cell operation.

A proper device design and processing procedure was developed for the solar cell fabrication. The p-type front contact was obtained using Pt/Au deposited by sputtering.

Table 2. Layer structure of the NAsP template.

Layer	Material	Thickness	Doping level (cm^{-3})
Buffer	lnP	1000 (nm)	-2×10^{18}
Nucleation	GaP	60 (nm)	–
Si buffer	Si	200 (nm)	–
Substrate	Si	775 (µm)	$+1 \times 10^{15}$
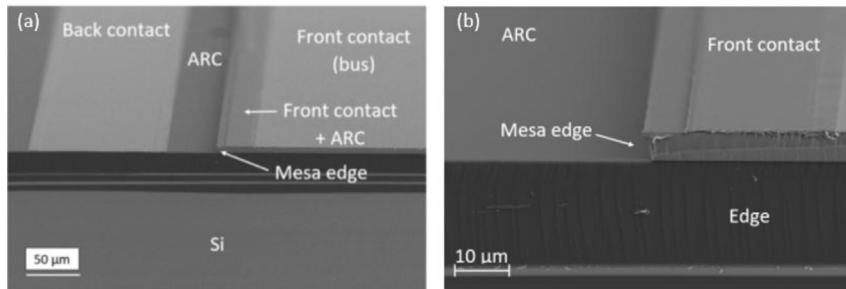
Fig. 2. SEM cross-section (7° tilt) of the InP cell grown on Si template after processing with different magnifications: (a) Shows an overview of top and back contacts together with the mesa edge; (b) zoom on the mesa edge and front contact.

The contact resistivity, evaluated by Transmission Line Measurements (TLM), was $3 \times 10^{-6}\ \Omega\,\mathrm{cm}^2$. Wet etching of the mesas (5 mm side squares) for the cells grown on InP substrates was performed with a $\mathrm{HBr:H_2O_2:H_2O}$ (15:1:15) non-selective solution. The InGaAs contact layer and the InP etch-stop layer were etched by selective $\mathrm{H_3PO_4:H_2O_2:H_2O}$ (3:1:40) and $\mathrm{HCl: H_3PO_4}$ (1:3) solutions.

The $\mathrm{Si_3N_4}$ ARC layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 245 °C.

The Ti/Pt/Au n-type rear metallic contact was directly deposited by sputtering on the back surface of the InP substrate.

The NAsP template, presented in Table 2, was grown on a 300 mm (0 0 1) Si substrate. After a chemical etching followed by a high temperature annealing directly in the VPE chamber to deoxidize the substrate, a 200 nm thick Si buffer was grown on top of the substrate using $\mathrm{SiH_4}$ as a precursor. A 60 nm thick GaP layer was then grown by MOVPE using tertiarybutylphosphine (TBP) and triethylgallium (TEGa) as precursors [37]. The production of a high-quality GaP/Si template opens many interesting possibilities, from the growth of lattice-matched devices [38] to the development of mismatched structures [39]. In the case of a mismatched growth, intermediate metamorphic layers, as well as direct growth, can be used. For our template, a 1 µm thick InP layer was directly grown by the supplier on the GaP layer by MOVPE. The latter was added in order to adapt the lattice parameter of the template to that of InP and aiming to lower the unavoidable threading dislocation density (TDD).

Processing the solar cells grown on the Si template required significant changes with respect to the procedure that has been presented for the devices on InP. In particular, the back contact could not be directly made on the rear side of the Si substrate in order to avoid the current flow through the defective III-V/Si interface. A solution to circumvent such a problem was to directly contact the rear side using a metallic grid around each cell at the bottom of the mesas, on the (n^+) InP buffer, as presented in Figure 1. This required to use the two selective etching solutions mentioned above also for the mesa etching, since they guaranteed a higher control on the etching depth.

In Figure 2 are reported SEM images at different magnifications of the cross-section of the InP cell grown on Si template after processing tilted of 7° towards the surface.

A general overview is presented in Figure 2a, the top right of the image represents a corner of the large bus used as top contact. Moving towards the left side, one can observe that the ARC was etched in order to enable electrical measurements, the bottom of the mesa and the bus acting as a back contact.

Figure 2b presents a zoom on the border of the etched mesa, with particular focus on the front contact. Note that, the grid of the back contact is slightly thicker than that of ARC opening to guarantee a full coverage of the exposed semiconductor. The two images show abrupt interfaces and a general good quality of the process, therefore validating the proposed technology.

All the samples were characterized by X-ray diffraction (XRD) in order to evaluate the quality of the structures. Furthermore, the samples made on Si templates underwent Atomic-Force Microscopy (AFM) and Scanning Electron Microscopy (SEM) characterizations to evaluate the effects of the lattice-mismatched substrate on the morphology.

Cross-sections of solar cells grown on Si template have been prepared by Focused Ion Beam (FIB) on a FEI Strata DB400 system and observed by Transmission Electron Microscopy (TEM) on a FEI Tecnai Osiris 200kV system equipped with X-EDS and a GIF Quantum detectors to assess their structural quality.

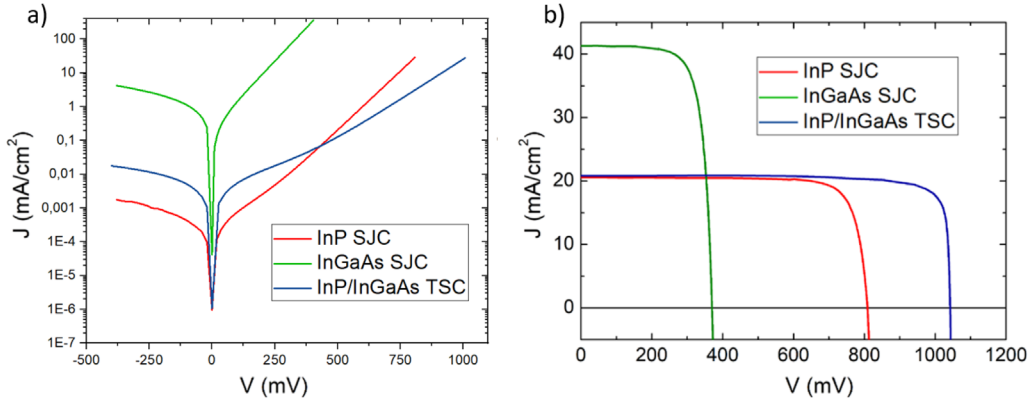Current density–voltage $(J$–$V)$ measurements were performed using 4-wire configurations, using an Oriel

Fig. 3. (a) J–V characteristics under dark conditions of the obtained InP/InGaAs tandem cell (blue line) compared to the single J–V characteristics of InP top cell (red line) and InGaAs bottom cell (green line). (b) J–V characteristics under 1-sun illumination of the obtained InP/InGaAs tandem cell (blue line) compared to the single J–V characteristics of InP top cell (red line) and InGaAs bottom cell (green line).

Table 3. Main PV parameters of the tandem cell compared with those of the two single-junction individual cells.

	InP	InGaAs	Tandem
Jsc (mA/cm^2)	20.6	41.2	20.8
Voc (mV)	809.3	369.9	1045.9
FF (%)	81.4	74.5	83.9
η (%)	13.5	11.4	18.3

Instruments 81192 solar simulator (the maximum illuminated area of the simulator being 100×100 mm^2, with a nominal power of 1 kW and adjusted to provide a solar spectrum similar to AM1.5G.

Before every set of measurements, the simulator configuration was analyzed and corrected, when necessary, with GaAs and Si calibration cells.

The measurements were taken with Keithley 2400 and 2450 SourceMeters. The Spectral Response (SR)/External Quantum Efficiency (EQE) measurements were performed by a modified Fourier Transform InfraRed Spectrometer (FTIR) [40].

4 Results and discussion

4.1 Solar cells on InP substrate

The three solar cells presented in this section refer to the devices fabricated on InP substrates. The J–V characteristics obtained at room temperature in dark conditions and under one-sun AM1.5G illumination for the single junction InP (red line) and InGaAs (green line) cells are presented in Figure 3, together with that of the overall TSC (blue line). Table 3 summarizes the main PV parameters of the devices.

4.2 Single junction cells

The InP cell presented an open-circuit voltage (V_{OC}) of 809.3 mV and a fill factor (FF) of 81.4%, which are

comparable with the best InP cell performance reported so far. Conversely, the short-circuit current density (J_{SC}) of 20.6 mA/cm^2 can be further improved up to 31.15 mA/cm^2 as experimentally reached with the current InP world record cell [41]. The conversion efficiency η was then limited to 13.5%. One of the possible mechanisms that reduces J_{SC} is probably related to the base thickness, limited to 3 μm in this study. In addition, problems in carrier collection, and non-optimized ARC and window layer, could also be responsible for such a reduction. The InGaAs bottom cell showed an excellent PV performance: J_{SC} of 41.2 mA/cm^2, V_{OC} of 369.9 mV and FF of 74.5%, providing an overall η of 11.4% which is close to the theoretical value reported in [42]

The experimental dark J–V curves were then fitted to a two-diode model to have a better insight into the characteristics of the devices [43]. One ideality factor has been fixed equal to 1, so the fit parameters are: one ideality factor, n, the saturation current densities J_{01} and J_{02}, and the series and shunt resistances, R_s and R_{sh}, respectively.

The values obtained for the InP cell are: $n = 2.4$, $J_{01} = 0.19 \times 10^{-6}$ A/cm^2, $J_{02} = 1.6 \times 10^{-8}$ A/cm^2, $R_s = 0.69 \times 10^{-3}$ Ω and $R_{sh} = 0.56 \times 10^{10}$ Ω. The parameters obtained for the InGaAs on InP cell are: $n = 2.2$, $J_{01} = 0.19 \times 10^{-4}$ A/cm^2, $J_{02} = 0.10 \times 10^{-6}$ A/cm^2, $R_s = 4.4$ Ω and $R_{sh} = 0.23 \times 10^{6}$ Ω. The larger saturation current density values could be expected due to the much smaller bandgap of this material compared to InP.

The InP and InGaAs solar cells have demonstrated a bandgap-voltage offset ($W_{OC} = E_g/q - V_{OC}$) of 530.7 mV
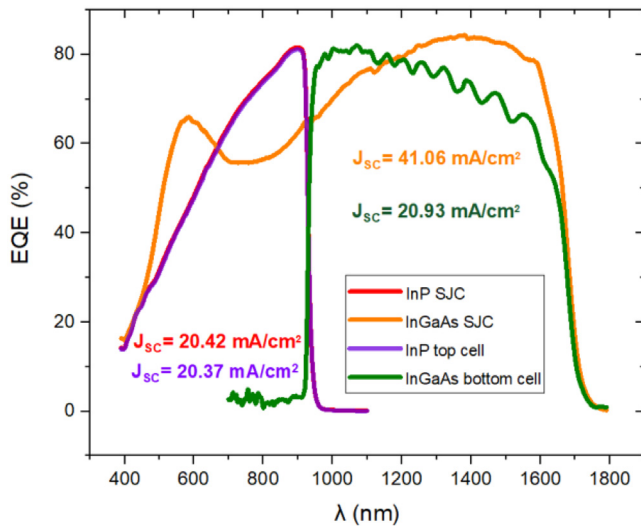
Fig. 4. EQE characteristic of the InP/InGaAs tandem solar cell. It was obtained by separately measuring the contributions of the top (violet line) and bottom (green line) cells. The results are compared with the ones obtained from the single cells (red line for InP and orange line for InGaAs).

and 380.1 mV, respectively. A value ≤ 400 mV is indicative of the excellent material quality [44].

In order to come closer to this threshold for InP devices, the enhancement of material quality will be crucial, namely minimizing the nonradiative recombination by reducing the defects and traps. Nevertheless, for an ideal InGaAs solar cell, the predicted value of W_{oc} is about 235 mV [45] which is close to the one obtained experimentally. This is a further confirmation of the high quality of material and device.

4.3 Tandem solar cell

The TSC, characterized under the same conditions, presented values of J_{SC} of 20.8 mA/cm², V_{OC} of 1.05 V, FF of 83.9% and η of 18.3%. From the comparison with the PV parameters of the SJCs, we can assume that the overall photo-generated current is limited by the InP top cell. The J_{SC} produced by the InGaAs bottom cell cannot be calculated straightforwardly, since the incoming light is filtered by the InP top cell before reaching the bottom one. Further SR analyses will clarify each contribution to the tandem photocurrent. The overall V_{OC} is around 100 mV lower than expected. The V_{OC} loss is most probably caused by a non-optimal passivation of the tandem cell interfaces and by the reduction of the top BSF thickness from 700 to 500 nm. Nevertheless, the excellent quality of the device can be inferred from the noticeably high V_{OC} and FF values. The overall η, although limited by the low J_{SC} of the top cell, is a promising result and comparable to the ones available in the literature [41].

Moreover, the low value of R_s makes these devices an interesting possibility for a concentrator photovoltaics (CPV) application, as well [46].

Figure 4 represents the EQE curve of the TSC, compared to those obtained from the constituting InP

(red line) and InGaAs (orange line) SJCs. In order to evaluate the individual contributions of the top (violet line) and the bottom (green line) cells to the overall EQE, they were separately saturated using a proper bias light source, namely a 785 nm laser source and a properly filtered halogen lamp, for the top and bottom cell, respectively. Note that, the J_{SC} values calculated by integrating the EQE convoluted with the AM1.5G spectrum are comparable with the ones obtained by J–V characterization. As expected, the InP top single junction device and the one integrated in the tandem presented similar behaviors. Conversely, the integrated bottom cell presented a different trend compared to the single junction cell. This is evident in the 1200–1600 nm range, where the clear discrepancy is partially caused by the higher reflectivity of the device at long wavelengths since the ARC thickness is optimized for the InP top cell. More studies will have to be performed to evaluate the effective contribution of the bottom cell to the tandem EQE for long wavelengths. Nevertheless, the characteristic presented here shows that the combination of the two cells guarantees a high coverage of the incident solar spectrum and this confirms the validity of our InP and InGaAs choices as constituting semiconductors [47].

5 Solar cells on Si substrate

5.1 Material characterization of the InP/GaP/Si template

It is well-established that there are two main sources of strain in heteroepitaxial systems. One is lattice mismatch, and the other is discrepancy in the thermal expansion coefficients between the material and substrate. The strain resulting from the divergence of the thermal expansion coefficient causes bending of the wafer and sometimes cracks in the grown films. Nonetheless, in InP the thermally induced tensile strain is partially accommodated during the cooling process after growth by reconfiguration of misfit dislocations at the interface that occurs at a moderately low temperature (≥ 250 °C). Furthermore, the relatively low temperature of InP growth process and the small difference between InP and Si thermal expansion coefficients are also responsible of this low residual strain [48,49].

The full growth process described for the devices on InP substrate was reproduced onto metamorphic buffers grown onto silicon, in a first attempt to evaluate the epitaxial and technological difficulties. These templates were delivered on a commercial basis by NAsP company [30,31] and widely described in Section 3.

The quality of the NAsP template was assessed by performing a series of characterizations such as optical microscopy, XRD, AFM and TEM. Furthermore, in order to evaluate the impact of the initial annealing taking place during the growth of the solar cell structure, the same characterizations were carried out after 10 min annealing at 700 °C/150 mbar and under a flow of phosphine (PH₃) in the MOVPE reactor.

The NAsP template presented a mirror-like surface morphology, not affected by the high temperature annealing, as shown in the images reported in
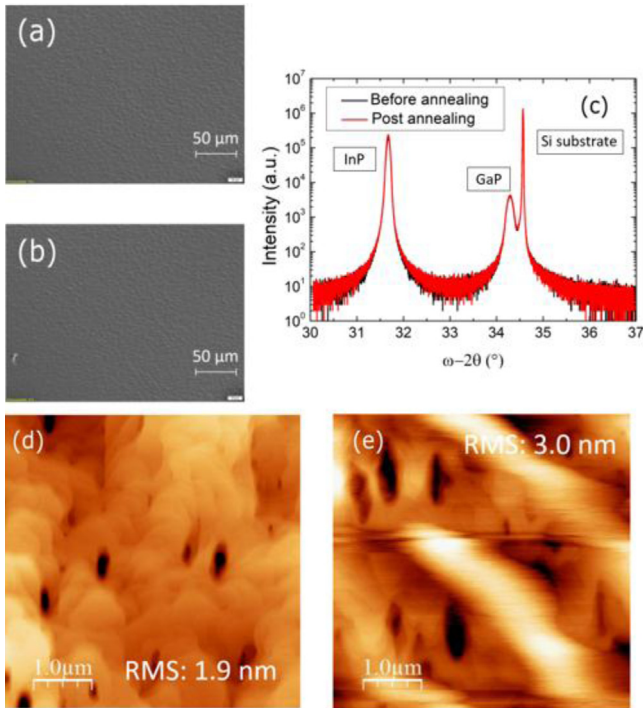
Fig. 5. NAsP sample before and after the 700 °C annealing: morphology (a) before and (b) after from optical microscopy; (c) XRD diffractograms; AFM (d) before and (e) after.

Fig. 6. HAADF-STEM image of the (0 0 1) NAsP template towards the (1 1 0) direction showing the GaP/InP interface.

Figures 5a and 5b acquired from optical microscopy. The XRD scans in Figure 5c present three sharp peaks. The most intense peak corresponds to the silicon substrate around 34.6°; afterwards, the GaP layer growth on the top of the substrate is around 34.3° and the last epitaxied layer of InP is around 31.7°. These three peaks are localized at the same place before and after the annealing step revealing that the crystal quality of the template is not affected by this process. Thanks to the previous values, the peak mismatched compared to the silicon substrate can be extracted: 0.77% corresponds perfectly to fully strained GaP, whereas the one at 8.38% matches with fully relaxed InP. The AFM scans performed on the surface of the template presented a root mean square (RMS) roughness of 1.9 nm before annealing and 3.0 nm after annealing, which is acceptable for our purposes, as reported in Figures 5d and 5e. The AFM scans revealed the presence of surface irregularities which can be visualized as black spots in the topography. Nonetheless, the AFM scan performed on the surface of the InP device, which will be presented in Figure 8c, reveals that the growth of the InP stack tends to mitigate this effect.

A deeper evaluation of crystalline properties of (0 0 1) NAsP templates was carried out by performing a series of STEM and TEM scans towards the (1 1 0) direction. Figure 6 presents HAADF-STEM scans of the GaP/InP interface. The orange arrow indicates the presence of periodical misfit dislocations at the interface which arises from the different lattice parameters of GaP and InP ($a_{\text{GaP}} = 5.4505$ Å and $a_{\text{InP}} = 5.8687$ Å, respectively).

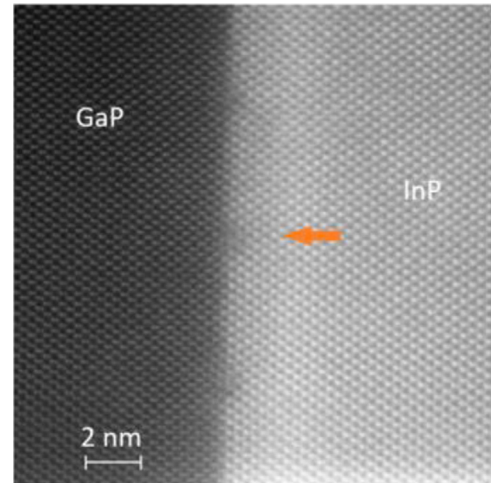The FFT of the image treated with a band-pass filter by ImageJ software allowed the evaluation of a misfit dislocations periodicity of 7.17 nm, within the experimental error limit of the theoretical value of 7.63 nm [50]. The presence of such a misfit periodicity and the absence of irregular rearrangements at the interface tend to confirm the high quality of the template.

Finally, Figure 7 presents two TEM images with different magnifications of the Si/GaP/InP template. Figure 7a shows the excellent crystalline quality of the GaP layer and the presence of the expected periodic misfit dislocations at the GaP/InP interface. An image treatment allowed us to find a misfit periodicity of 7.38 nm, which is in good agreement with the value calculated from the SEM image. Figure 7b presents a larger zone, highlighting the presence of threading dislocations arising from the mismatched structure, the density of which tends to decrease with increasing the thickness.

5.2 SJCs on Si substrate: material characterization and PV performance

Before studying the PV performance in detail, the SJCs on Si were characterized by optical microscopy, XRD, AFM and TEM for the evaluation of the quality of the devices as performed for the NAsP template in the previous section. We primarily focused on the InP device due to the simplicity of the structure compared to the InGaAs one. In particular, the surface morphology, shown in Figure 8, despite being completely mirror like to the naked eye, appears slightly rough at both the center (Fig. 8a) and edges (Fig. 8b). The AFM image in Figure 8c shows that the RMS decreases from 3.0 nm (measured after annealing at 700 °C) to 1.5 nm, a value lower than that we found in the unannealed template since the increasing thickness of the layer tends to level out the roughness. The thermal mismatch induced a series of cracks in the structure which can be visualized as vertical stripes on the whole figure surface.

The XRD diffractogram in Figure 8d demonstrates that a longer and thicker deposition of InP did not affect the overall crystal quality of the structure since the positions of the
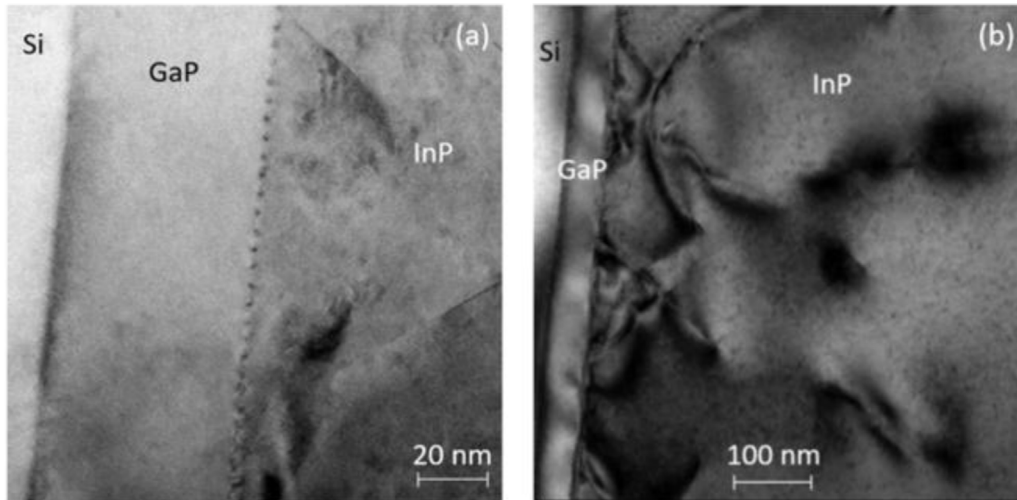
Fig. 7. TEM images of the cross section showing the Si/GaP/InP template; (a) Points out the evaluation of misfits periodicity, (b) Illustrates some crystalline defects arising from the high mismatch.
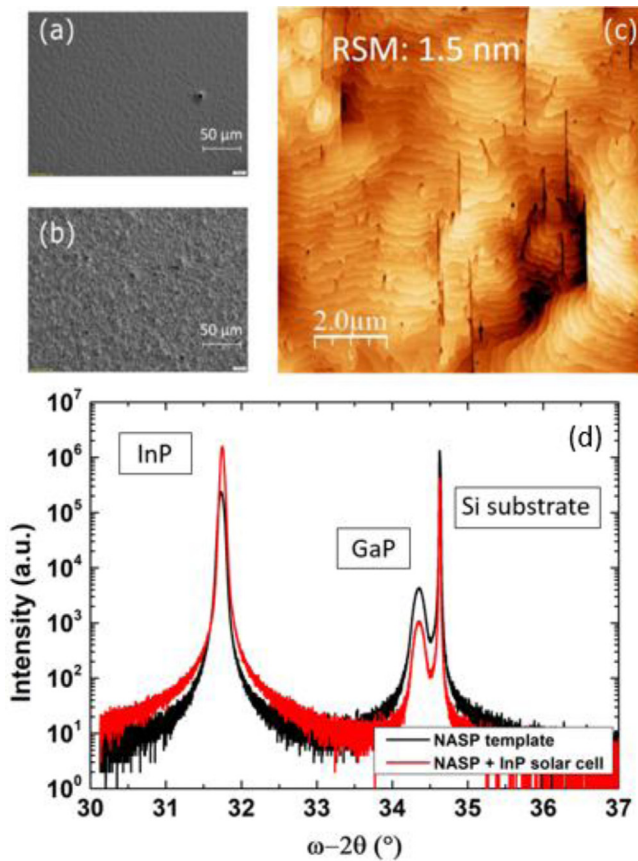

Fig. 8. InP solar cell grown onto NAsP template: morphology (a) At the center and (b) At the edge of the sample from optical microscopy; (c) AFM; (d) XRD scans of NAsP template (black line) and NAsP + InP solar cell (red line).

crystal of the whole structure. Note that, the intensity of the InP related peak is higher since the XRD is now sensing all the InP stack constituting the device and not only the 1 μm InP buffer layer of the template.

The InP and InGaAs cells integrated on Si were characterized under the same conditions presented in Section 4.1. The J–V curves obtained at room temperature in dark conditions and under illumination are presented in Figure 9, whereas the fitted PV parameters are summarized in Table 4.

As expected, the integration on a Si substrate had a limiting effect on the PV performance. By comparing the J–V curves in Figure 9 with that of Figure 3, we can identify a higher influence on both R_{sh} (in particular, for the InGaAs cell) and R_s which has a negative impact on FF. All the electrical parameters decreased; both cells presented a ∼40% J_{SC} reduction, a V_{OC} reduction of 22% and 40% and a FF reduction of 43% and 50%, for the InP and the InGaAs devices, respectively. Consequently, the efficiency dropped to 3.6% and 2.0% for the InP and InGaAs cells, respectively.

The InP and InGaAs solar cells on Si have demonstrated a bandgap-voltage offset (W_{OC}) of 706 mV and 529.8 mV, respectively. These values are far above the threshold limit, evidence of poor-quality devices [40].

The dark J–V curves were fitted to a two-diode model, as described for the devices on InP substrate in Section 4.2.1. Both devices developed on Si, present a significantly higher saturation current, J_{02}. Indeed, this latter increased by almost 3 orders of magnitude for the InP cell with a J_{02} of 2×10^{-5} A/cm^2; the ideality factor has also increased reaching a value around 4. Nonetheless, the ideality factor of the InGaAs stays stable, around 2, and J_{02} is multiplied by a factor of 5 with a value of 9.5×10^{-3} A/cm^2. The increase of J_{02} is consistent with the reduction of the V_{OC} pointed out at the beginning of the section for both solar cells.

Another important difference to highlight is the reduction of R_{sh} with respect to the ones grown on InP, with values of 6.6×10^8 Ω and 5×10^3 Ω for the InP and

peaks are not shifted with respect to the XRD scan on the bare template, also reported in Figure 8d as comparison. Additionally, the InP peaks present a thin and comparable full width at half maximum as further evidence of a good
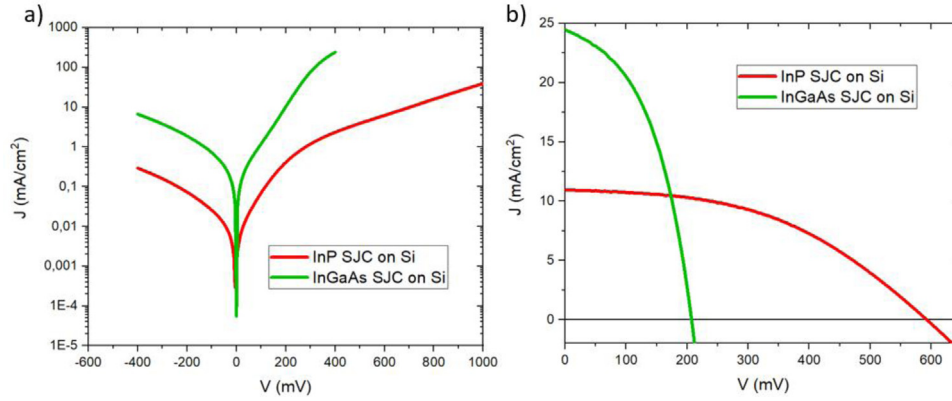
Fig. 9. (a) $J–V$ characteristics under dark conditions of the two solar cells integrated on Si. (b) $J–V$ characteristics under 1-sun illumination of the two single solar cells integrated on Si. The InP cell is represented in red, whereas the InGaAs cell in green.

Table 4. Parameters of the two solar cells integrated on Si.

	InP	InGaAs
Jsc (mA/cm^2)	12.1	24.7
Voc (mV)	634.0	220.2
FF(%)	46.4	36.9
η (%)	3.6	2.0
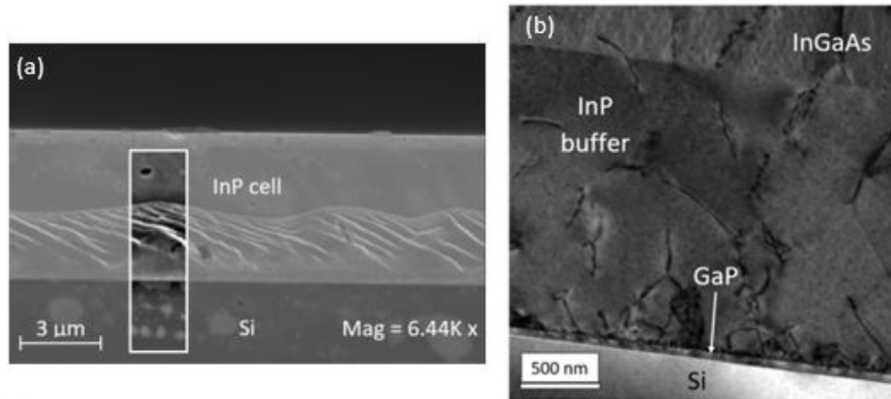
Fig. 10. (a) SEM images of the InP cell cross-section grown onto NAsP template; the image presents an inset showing band-pass filter treatments performed with ImageJ software to highlight the irregularities. (b) TEM images of the cross section of the grown InGaAs single solar cell displaying a part of the InGaAs base with the presence of dislocations.

InGaAs devices, respectively, which also impacted negatively on the PV performance.

There are examples in literature where J_{SC} and V_{OC} have been maintained after the fabrication of the III-V on Si cells [51–53]. Conserving a good FF has been, in general, more challenging, due to the R_s and R_{sh} variation caused by the cell fabrication. In our case, this implies that there is still an important scope for improvement for all our structures.

To get into more details regarding the decrease of the PV performance, in Figure 10 are reported SEM and TEM images for the InP and InGaAs SJCs, respectively. In particular, Figure 10a presents the surface and the cross-section of the InP devices and it allows to distinguish the

InP layer from the Si substrate. The irregularities at the interface on the InP side are probably due to the local disorder induced by the presence of dislocations making the cleaving process challenging. The image presents an inset treated with a bandpass filter by ImageJ to better reveal the irregularities. Figure 10b presents a TEM image of the InGaAs solar cell device grown onto the template. Some dislocations clearly propagate in the InGaAs layer and the evaluation of the TDD along the growth direction indicates a mean TDD of 8.8×10^8 cm^{-2} for the InP buffer that decreases to 2.0×10^8 cm^{-2} in the InGaAs base. This value is higher with respect to similar devices present in literature [54]; it has a direct impact on the minority carrier (electron) lifetime, which is significantly degraded, worsening the PV
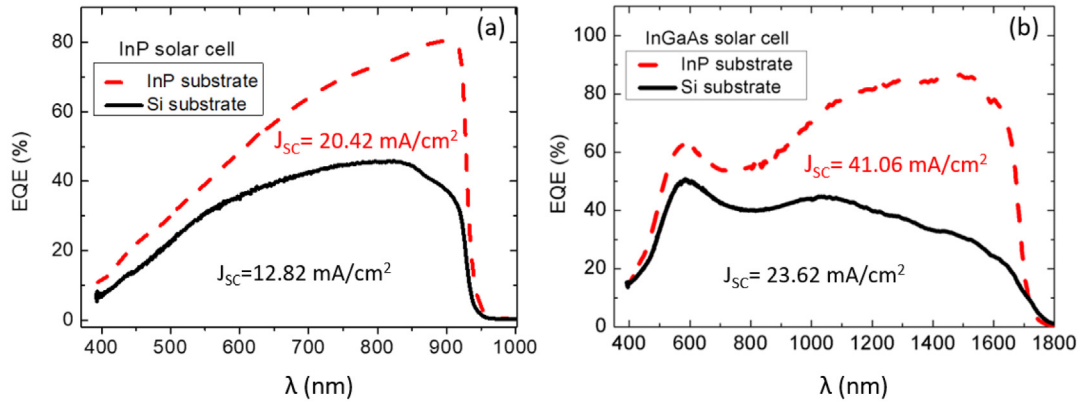
Fig. 11. EQE characteristic of the best InP (a) and InGaAs (b) Solar cells grown on Si template (black line), compared to the same result obtained on a typical InP substrate (dashed red line).

performance. These TEM observations stress the need to evaluate the electrical impact of these defects on the PV performance of the resulting devices.

The most probable explanation for the differences between the PV parameters of the cells grown on InP and on Si template is related to the presence of structural defects due to the lattice mismatch. In particular, as shown in Figure 8c, the thermal mismatch caused cracks in the structure which can act as charge carrier traps and recombination centers. In this sense, the worsening of the quality of the material impacts the minority carriers lifetime and the corresponding diffusion length. This is responsible of increasing the losses, which is in line with the results determined by TEM. A second problem may be related to the n-type back contact. We determined by TLM measurements a contact resistivity of $\sim 5 \times 10^{-7}\,\Omega\,\mathrm{cm}^2$, around one order of magnitude lower than the value obtained for the front p-type contact. Nevertheless, the non-optimal geometry of this contact may reduce the carrier's collection and increase R_s thus decreasing J_{SC} and FF. Finally, in a future analysis, other phenomena must be considered such as a possible emitter degradation due to the higher TDD [55] and an aggravation of the passivation problems already present in the device made using an InP substrate.

Figure 11 presents the EQE characteristic of the best single solar cells grown on the Si template (black full line), compared to the best result obtained for the same device grown on the InP substrate (red dashed line). Figures 11a and 11b illustrate the InP and the InGaAs solar cells, respectively. The J_{SC} values calculated by J–V characterization are comparable with the ones obtained by integrating the EQE convoluted with the AM1.5G spectrum.

Both solar cells show a significant reduction of the overall quantum efficiency, notably in the spectral range associated to the absorption in the base: 700–920 nm and 1000–1700 nm, respectively for the InP and InGaAs devices. This observation clearly points out deficiencies of the diffusion length at the base as well as surface recombination issues at the rear. The rest of the spectral range ($\lambda < 700$ nm for InP and $\lambda < 1000$ nm for InGaAs) also shows a lowering of the EQE due to similar issues taking place this time at the emitter and at the front surface. The EQE spectra confirm a general reduction of

carrier collection compared to the devices fabricated on InP. These results support the aforementioned InP on Si integration problems that impact the material quality and cause a poor-quality back contact. It is worth recalling that TEM characterizations have indeed evidenced the presence of structural defects, because of the lattice mismatch, that are well known to affect the charge carrier transport and the recombination processes. Such defects are often the origin of parallel current paths for the photocurrent causing shunts that reduce FF and V_{OC}. In this sense, the strong increase of the saturation current observed through the dark J–V measurements underlines a degradation of the minority carrier diffusion length affecting J_{SC} and V_{OC}.

6 Conclusions

In this work, we have first presented the realization of high-performance InP and InGaAs solar cells lattice-matched to InP. The InP SJC, which can be used as the top cell in a tandem device, and the InGaAs SJC, which can be used as the bottom cell, showed AM1.5G power conversion efficiencies of 13.5% and a 11.4%, respectively. The combination of the two devices through a InP/Al$_{0.48}$In$_{0.52}$As tunnel junction, allowed the fabrication of a TSC which showed an efficiency of 18.3%, with little influence from shunt and series resistances, which is suitable even for CPV applications. EQE characterizations performed on the TSC demonstrated an efficient coverage of the incident solar radiation.

In a second step, a prospective study in view of integrating the previous III-V single solar cells on Si substrates through direct MOVPE growth has been performed. The commercial InP/GaP/Si template from NAsP company and the MOVPE-grown cells were characterized by XRD, SEM and TEM pointing out specifically a fully relaxed InP buffer and the presence of structural defects that can propagate to the cell grown atop. J–V characterizations demonstrated that these metamorphic cells kept a diode-like trend and produced photocurrent, although the efficiencies were reduced to 3.6% and 2.0% for the InP and InGaAs single junctions, respectively.

These preliminary results demonstrate the potential of the proposed approach although the realization of the final tandem device on the Si substrate was delayed until further improvements in the quality and PV performance of the single junction solar cells will be reached.

Several paths to improve the presented results are possible. For instance, in the epitaxial approach on InP substrates, the thickness of the base for the tandem top cell must be optimized reaching the typical 5 μm reported in literature. Additionally, the integration of a double layer anti reflecting coating (DLARC) will also lead to higher efficiencies. Nonetheless, the fabrication of such a high-performance TSC represents an important step towards the realization of a triple junction device by the introduction of an AlInGaAs or InGaAsP middle cell.

Finally, regarding the integration on Si substrate, the reduction of threading-dislocations at the InP/GaP interface seems a key issue to improve the material quality and the photovoltaic performance of the final device.

Future improvements in this regard may open a new generation of multijunction solar cells on Si substrates both more efficient and more cost-effective.

Author contribution statement

All authors contributed equally to the article based on their knowledge and expertise. In particular, authors from III-V Lab were responsible for the design and realization of the devices. Authors from GeePs were responsible of the electrical characterizations of the solar cells. All authors participated to the writing of the manuscript and all authors read and approved the final manuscript.

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