64 Bit Binary Counter with Minimal Clock Period

Vaishnavi Yadav[1] , P P Bansod[1] and D K Mishra[1]

[1]Department of Electronics and Instrumentation Engineering

Shri G.S. Institute of Technology and Science, Indore, India

vaishnaviy401@gmail.com , ppbansod43@gmail.com , mishradrc@gmail.com

Abstract. Novel rapid formations of synchronous binary counting with single minimum period of counting for practical counters are developed in this project. A synchronous binary counter is required in many applications since it is rapid, also can help a broad bit-width. Basically, because of massive fan-outs and extensive carry chains, earlier counters have a limited counting rate, mainly when size of the counter is not modest. It employs a single bit Johnson counter to decrease whole hardware complications, then copy it to lessen the propagation latency caused by huge fan-outs. In this paper, re programmable the clock utilized in it for various applications functioning at different clock rates and there'll be a variation within the delay values because the clock is reprogrammed the critical may varies for various rates. The counter output results are obtained for various bit up to 64 and therefore the design provides various clock rates with variations in area and delay.

Keywords. Backward Carry propagation, Johnson Counter, Pre scale Enable Signal, Ring counter, Binary counter.

1. Introduction

There are many different uses for the design known as counters, similar as measurement techniques, ADC, frequency divisions, PLL frequency synthesizers etc. Latest advancements in different applications have necessitated the implementation of rapid, broad counters that supports constant rate of counting regardless of counter size. Furthermore, the rate of counting and size of the counter are incompatible as the carry propagated from a lower bit order to a high bit order takes more as size of the counter increases. As a way to obtain one that is substantial speedup, a traditional ripple carry chain was changed by a carry look ahead circuit.

Moreover, a Manchester carry chain basically utilised for carry propagation, and a state look ahead was employed to discontinue the carry chain by summing D flip-flops, getting rid of ripples. The carry chain was developed with a tree topology. Combining an adder with a state register to make a counter, on the other hand, does not result due to the adder delay's lower bound's constant nature, so constant clock period is required. Further attempts for improving flip flop been developed to expedite the counter. The flip flop dependent on genuine single-phase clock, for example, has been used to construct high-speed synchronous counters.

Counter can be made using a state generator a constant clock period if just rapid sync counting is replaced in position of the binary sequence. For instance, a carry propagation chain was created by employing systolic structures, even though it two times in number Flip flops necessary, maximizes

overall hardware complexity. One more carry propagating method termed backward carry propagation (BCP) is shown to accomplish combined constant delay and binary sequence. It takes advantage of the fact that more significant bits go high before less significant bits in a binary sequence. Because only the least significant bit controls carry propagation, this method is used to construct a constant delay counter (LSB). Least significant bit, actually responsible for the entire counters flip flop which results in a significant fan-out issue. Also, the LSB's maximum value is exceeded by the number of input ports attached to it. In addition, a pre-scaling-based synchronous binary counter was presented.

Sub-blocks are created from a large counter. The least significant block determines the clock period of a pre-scaled counter, while a pre-scaled enable signal created by block of lower order which enables the high-order block. But there are still concerns with the massive fan-out and massive distribution of pre scaled enable signal required to get a significant number of F/Fs' enable write input in the upcoming block. In fact, achieving a fast binary counter requires resolving the massive fan-out issue. The fan-out problem becomes more severe as the counter size grows larger, resulting in extended delay in propagation. A binary sync counter for counter of size up to 128 bits practically which runs at a constant delay. The huge fan-out problem is addressed in the suggested counters by doubling the single bit Johnson counter, using the BCP approach for eliminating additional delay introduced by ripple carry propagation. Hence recommended counters achieve greatest pace of counting, regardless of counter size, the rate of counting is governed exclusively by the LSB counter.

Re programmable the clock utilized in it for various applications functioning at different clock rates and there'll be a variation within the delay values because the clock is reprogrammed the critical may varies for various rates. The counter output results are obtained for various bits up to 64 and therefore the design provides various clock rates with variations in area and delay.

2. Existing and Proposed Counters

2.1. Existing Counter

An n-MOD ripple counter is capable of counting up to 2n number of states before resetting to zero. With flip flops, toggle mode is used; the external clock signal reaches to single f/f only. The result of this f/f is utilized as the flip flop's clock signal after it. In the counting series, LSB is the f/f via pulse of an outside clock transmits. A synchronous counter, unlike an asynchronous counter, employs the use of a single world clock to operate all of its flip-flops, leading to simultaneous change in the output. However, because there is no cumulative delay, a sync counter can drive at higher frequency than an asynchronous counter.
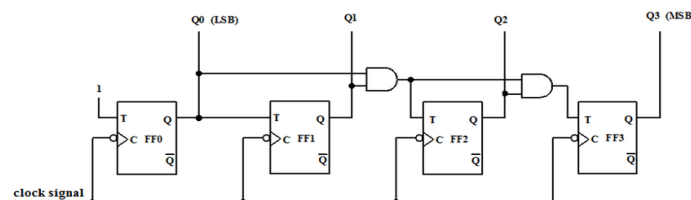

Figure 1 Synchronous Counter.

Shift register is widely used by ring counters. The shift counter and the ring counter are nearly identical. A sole distinction being that the ending f/f's o/p relates to the starting f/f's it functions as an outlet in a shift register but as an input in every ring counter. Other than that, nothing has changed. Total count for f/fs same as that of the total count of states in the ring counter.

By attaching the output of the last shift register's outcome to the source of the first register, it repeatedly outputs a series of 1's followed by 0's around the ring. The schematic of the mentioned counter is shown below.
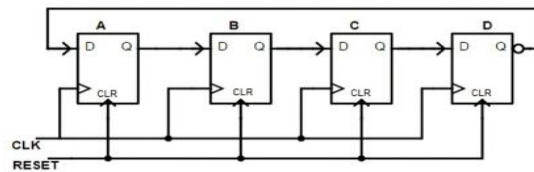

Figure 2 Schematic of Johnson Counter.

Johnson counters frequently called creeping counter, also synchronous. The O/P of the ending f/f is attached to I/P of the starting f/f to make an n-bit Johnson counter. This is a common form of shift counter. The shape of the result is determined by the input it receives from its own source. Basically, the counter is a reversing ring. In an n-bit Johnson counter, amount of both active and inactive stages combined are 2n states were utilized 2n – 2*n.

The ring counter and the Johnson counter have about the same amount of flip flops. However, the number of states would be doubled. The flip flops which can be used for this are J-K flip flop and D flip flop. In a continuous loop, a Johnson ring counter counts the input. The Johnson counter uses self-decoding technology. Some negative aspect of the above described counter: Johnson counter doesn't employ a binary series. Based on it, in comparison with useful states maximum states are unutilized. Only half as many time signals are necessary for flip-flops. It can incorporate any time pattern.

To provide dependable output as binary, a sync binary counter should employs. The ripple carry counter links a one-bit adder's carry-out to the following step's carry-in. The term "ripple carry chain" refers to how continual ripples are introduced into the carry pulse progressing to further stages and extended carry propagation of a sync counter's carry chain is the main bottleneck. Fast adders have been designed in a variety of ways, a few of that are successfully adaptable to quick counters. The ripple carry chain of the conventional binary counter was used to achieve a significant performance gain chain is changed with a carry look ahead design.

Considering a summer and a state register combination as counter, on the other hand, is unsuccessful in establishing the bottom limit of the adder delay does not remain constant, hence a regular interval of time is required. There have been further initiatives to increase the speed of the counter by altering the flip flops. On the basis of real single phase clock, one example is the development of high speed counters, F/F. Through the use of systolic structures, a pipelined chain for carry propagation, for example, has been constructed, despite the fact that it requires twice as many F/Fs and increases complete H/W overhead. One more technique to produce a state generator is by using a LFSR, which involves many additional circuitries modify the sequence in which state from binary, for making the different states to two's power. To do this, a different carry propagation strategy known as BCP was given binary sequence and continuous lag.

Including bcp should be carried out with carry look-ahead and standard propagation should be carried out. The three stages a, b, c is employed to split the counter. To lessen the max depth of logic as illustrated afterwards, the bits in Phase A have their outputs coupled to the carry look ahead design. Thus as a result, the high order bit toggle signal is generated simply attaching these values on each AND gate's I/P. BCP can be seen in proposed section, where operation is as follows- The subsequent clock pulse will trigger b3 to flip, when wb2 is set to high. At initial stage merge b1 & b2 in and gate because before b0, both are high. To create b3 flip signal, couple this with b0. Toggling output is generated by a time sensitive AND gate with a low fan-in, indicating high-speed capability. Phase b

equipment necessitates for each bit a backward ripple chain. A new phase c to the right of bit is proposed, using a regular cheap carry chain ripple. Information from stages a and b at high speeds regrettably, an injection is necessary. Primarily phase c's ripple chain generates then secondary phase b's bits become high and followed by phase a.

Use of backward carry propagation idea yet again, mixing information starting with a rightmost chain's ripple carry chain outputs first, after it is coupled along for each bit in phase c, the values of the phase a, bits create a toggle output. The two cascaded AND gate is used for phase c to create a small bcp sequence for each bit. The ripple carry sequence of a basic counter limits the data transmission time to ti…,T, here T is the clock time of counter, which takes advantage of fact that more significant bits go high before less significant bits in a binary sequence. Because the carry propagation is governed only by LSB, this method may use for constructing a counter with constant delay (LSB).

The LSB, contrasted with, is responsible for all of the counter's F/Fs, resulting in a significant fan-out issue. Also, the Least Significant bits maximum value is exceeded by different input ports connected to it. In addition, a pre-scaling-based synchronous binary counter was presented.

2.2. Proposed Counter

In the existing counter, because of carry propagation the delay is maximum, even the fan out is high. These are the disadvantages for the existing counter. Let's assume $n = \log_2 N$ and $m = (Nn)/L$ for sake of simplicity, in which maximal fan out to be found by simulation is L. It take advantage of pre scaling, a bit counter of size N is partitioned to three sub-counters, with m 1-bit Johnson counters generating m PEN signals for the last sub-counter. When the state changes from 0 to 1 of Johnson counter, the PEN signal is created, allowing the next sub counter to count.
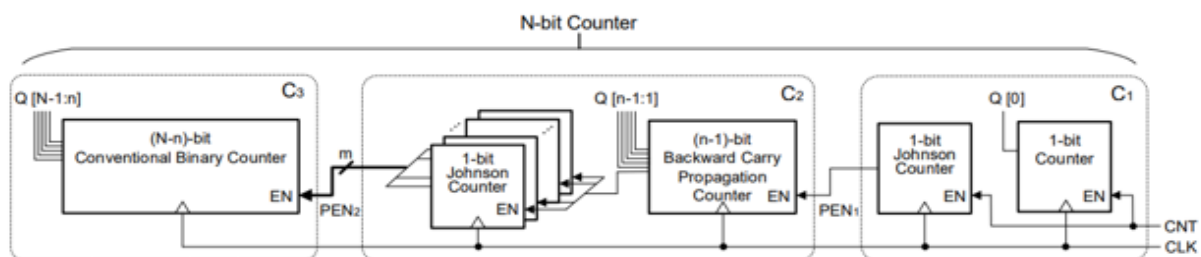

Figure 3. Schematic of proposed N- bit Counter.

Concept of BCP is crucial in the implementation of rapid synchronous counter. It works because binary number system's properties cause an increase in compelling counter bit to hit high before the smallest amount. In a conventional binary counter, instead of a single chain, each counters bit has its own AND chain attached in reverse manner. In a carry chain, available signals that come earlier are evaluated before signals that arrive later.

LSB readily changes pulse should be combined with last AND gate of the carry chains, resulting in the bottom most AND gate defines backward carry propagation critical delay of path. This means that the latency of the final AND gate & a T- flip flop are the two main factors affecting propagation delay. The LSB Q.(0) All the AND chains are connected to the the LSB Q.(0), resulting in massive fan out. Alternatively, LSB's burden is so much to work quickly, relying on fan out for the crucial route delay.
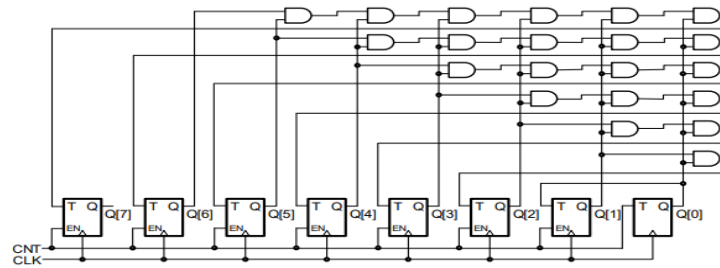
Figure 4. 8bit synchronous counter made with BCP.

Sequence generation is carried out via the block of counter, counting starting as 00...000 to 11...111. In general counter is made up of two parts: a register which saves the current state and a combined incremental which calculates the later value. The increment's computation time is primarily what limits the counting pace. Pre-scaling can help to eliminate the increment's delay. A counter of size N-bit is realized in the proposed counter design by splitting it into three sub counters.

C_1 = single bit counter which alternates among 1 or 0 per clock cycle. The second sub counter C_2 = (n-1) bit counter uses bcp, whereas third sub counter C_3 = binary counter of size (N-n)-bit. When pre-scaling the high-order block, the partitioned counter's basic assumption is to consider the lower order block. The duration of PEN2 created in C_2 three separate N bit counters are created is less than the synchronous ripple carry binary counter C_3's propagation delay which is (N-n)-bits long, that is composed of (N-n-1) AND gates. Because PEN2 has duration of 2n time intervals, before the subsequent PEN2 arrives from C_2, the carry propagation in C_3. The (n-1)-bit carry propagation counter C_2, a sub counter of the 1-bit counter C_1, is enabled which is backwards. Because the lag of lengthy carry chain is shortened to single one AND gate by using bcp and may make sure that C_2's carry propagation takes less time than C_1's PEN1 formation did, in order to ensure this.

C_2 's carry propagation delay results in delayed sum of AND gate and XOR gate, plus time to load the F/F D. Because size (n-1) is minute, the first bit's fan-out effect is minimal. The delayed carry propagation of C_2 is regularly quicker compared to PEN1 period formed at C_1, i.e., is dual clock cycle, if minimum period of clock is resolved considering D F/F setup time as well. As a result, the least important sub counter C_1 does indeed decide the clock period.

Enable Signal Generation at a Predetermined Scale the PEN signal in the presale counter should be synchronized with the clock, with no fan-out delay. Using twisted-tail counter or ring counter is a common way for creating PEN. The ring counter creates a circular structure by connecting the final F/output F's to the first F/input. F's The PEN signal changes to 1 whenever the ring counter of n bit is at 2 n1.

When count value become 2 n1, PEN signal is activated by the n-bit Johnson counter, also known as twisted-tail counter, such that the reverse result for final f/f: coupled to the input of the starting. Because in between absence of combinational circuit and neighbouring f/f, they can run at a high frequency, tolerating PEN signal to be in sync with clock. However, the method is inefficient since it requires n number of F/F to pass through n number of state which results in increase of H/W complication. Furthermore, the signal i.e., PEN must drive every flip flop in the following separation, resulting in high output driving capability and an increase in propagate time, lowering total speed of counting.

So, from a single bit sub counter C_1 64 bit also be constructed, C_2 = 5 bit sub counter, C_3 = 58 bit sub counter, pre scaled enable signal 1 generated from a two bit ring counter, pre scaled enable signal 2 generated from 64 bit ring counter. PEN1 has a small enough fan-out that it can be overlooked. However, because PEN2 controls 58 enable ports in C_3, the design should account for the delay induced by the significant fan-out. As shown the implementation and simulation results, PEN2's propagation delay causes the critical route, which prohibits the counter because of a limited time

frame. In order to prevail fan out problem, a 2n bit ring counter is changed by a bit Johnson counter, so the value of N is 64, and n and m is 6 and 4 respectively are utilized. After being set to 0 at the beginning, single bit Johnson counter experience state of change when triggered. The aim of PEN2 is to pulse every 2n cycles, or 64 cycles in this situation.
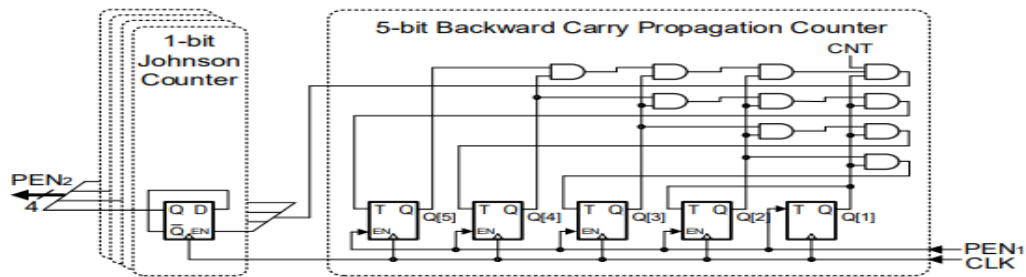

Figure 5. Pre scaled enable signal production having redundant Johnson counter.

The command signal mandatory 1 during both (2n2)th and (2n1) th cycle to make PEN2 one at the (2n1)th cycle and 63rd cycle in the case , the backward carry propagation approach illustrated in Figure 6 can be used to generate such a signal. The AND operation of Q.(5),Q.(4), Q.(3), and Q.(2) may be implemented through reverse AND pipeline. When Q.(2) four cycles journey from minimum to maximum, the signal Q.(5) &Q.(4) &Q.(3) & Q.(2) gets elevated.

Connecting the latest incoming signal Q.(1) to the final AND gate makes AND chain's output dual cycles of high. Compared to the output of, the enable signal of &Q.(5:1) since &Q.(5:2) has been calculated ahead of due to backward carry propagation. Only one AND gate is needed for the computation. Between the 62nd and 63rd cycles, the enable signal is strong, and it occurs 64 times each. Once the enable signal is suspected, pre scaled enable signal 2 is clocked back one cycle.

As a result, once every 64 cycles, PEN2 gets high. To put it another way, PEN2 is the same as &Q [5:0], which is calculated using the counter's least 6 bits. A single bit Johnson counter can be copied twice for dealing with nodes having large fan-out. The formula m = (N n)/L is used to compute the number of redundant Johnson counters, m, where L being the maximum no. of i/p ports that an F/F may drive. With N is between 8 and 128 bits, M is frequently low than 8. Increased complexity produced by the redundancy is a minor percentage of the total counter because the redundant F/Fs are limited to eight at most.
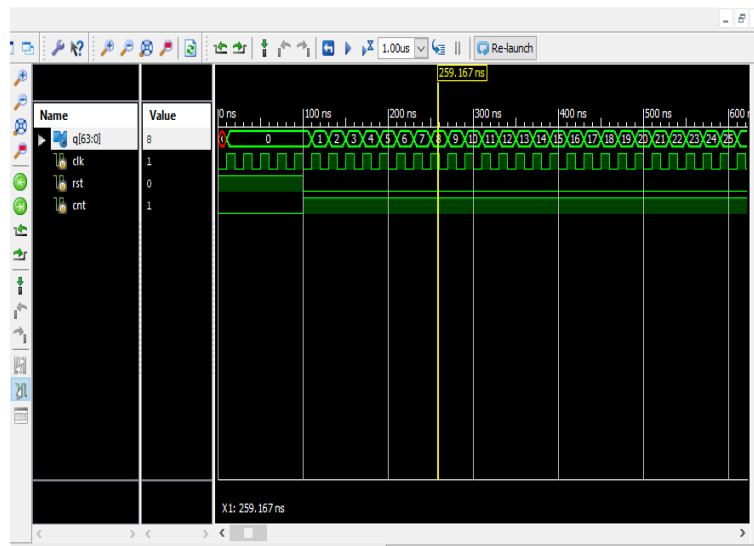
3. Performance Analysis

This section implements a 64bit counter using 3 sub-counters and the schematic and evaluation is given below. The performance analysis between the pre scaled counter employing ring counters [8], backward carry propagation counter [9] and the proposed counter technique which is described above:
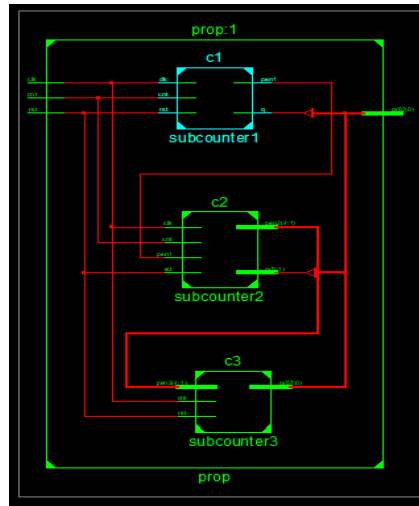
(a)
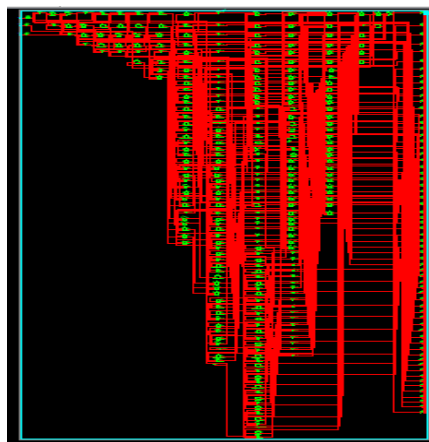
(b)

(c)

Figure 6. (a) RTL Schematic; (b) Technology Schematic; (c) Simulation.

Table 1. Performance analysis and evaluation of the proposed design of the counter.

	Evaluation		
	Area (LUT'S)	Delay(ns)	Counter Size(bits)
prop	104	2.44	64

Table 2. Defines the performance comparison of various techniques used for low number of flip-flops. As it is quite evident from the table above that the proposed counter has few number of flip-flops compared with other techniques.

Various techniques used	Comparison	
	No. of Flip Flops	Overall gate counts
Backward Carry propagation	65	1600
Pre scale counter using ring counter	100	850
Proposed counter	65	800

4. Conclusion

In this study, the novel synchronous binary counter design whose latency is nearly consistent for appropriate counter sizes. The suggested response is frequently accomplished using a few flip-flops, which is almost independent of the size of the counter. Re programmable the clock utilized in it for various applications functioning at different clock rates and there'll be a variation within the delay values because the clock is reprogrammed the critical may varies for various rates. The counter output results are obtained for various bits up to 64 and therefore the design provides various clock rates with variations in area and delay.

5. References

[1] Yuan J.-. 13 Oct. 1988 Efficient CMOS counter circuits *Electronics Letter* vol. 24 no.21 pp. 1311-1313.
[2] Abdel-Hafeez S., Harb S. M. and Eisenstadt W. R. 2008 *IEEE Int. Symp. on Circuits and Systems* (Seattle: WA) pp. 592-595.
[3] Ajane A., Furth P. M., Johnson E. E. and Subramanyam R. L. 2011 *IEEE 54th Int. Midwest Symp.on Circuits and Systems (MWSCAS)* (Seoul) pp. 1-4 doi: 10.1109/MWSCAS2011.6 026392.
[4] Thota P.R. and Mal A.K. 2016 *Int. Conf. on Microelectronics Computing and Communications(MicroCom)* (Durgapur) pp. 1-5.
[5] Pekmestzi K. Z. and Thanasouras N. Nov. 1994 IEEE Transactions on Circuits and Systems II: *Analog and Digital Signal Processing* vol. 41 no. 11 pp. 775-776.
[6] Morrison D., Delic D.,Yuce M. R. and Redouté J. Jan. 2019 *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* vol. 27 no. 1 pp. 103-115.
[7] Hyun Yujin 25 Jan. 2021 Constant-time Synchronous Binary Counter with Minimal Clock Period, in *IEEE Transactions on Circuits and Systems II*.
[8] Ercegovac M. and Lang T. June 1989 *IEEE Transactions on Circuits and Systems* 5. vol. 36 no. 6 pp. 924-926 doi: 10.1109/31.90421.
]9] Larsson P. and Yuan J. 5 Aug. 1993 Novel carry propagation in high-speed synchronous counters and dividers, in *Electronics Letters* vol. 29 no. 16 pp. 1457-1458 doi:10.1049/ el:19930975.