Performance Comparison of Five-Level Active Neutral Point Converter Based on Phase Disposition-PWM and Alternate Phase Opposition Disposition-PWM

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Abstract. The work in this paper presents the performance analysis of the reduced component count converter which is the 5-Level Active Neutral Point Converter (5LANPC). This 5-level converter has been configured by stacking the traditional 3-Level Neutral Point Converter with the Flying Capacitor converter. Two types of control algorithms were considered and compared to explore the performance of the 5LANPC. The first algorithm was based on the Phase-Disposition-Pulse Width Modulation (PD-PWM), while the second one was based on the Alternate Phase Opposition Disposition-Pulse Width Modulation (APOD-PWM). These algorithms are used to determine the required voltage level and according to the required level the state of the switches is selected through a simplified voltage balance algorithm. This voltage balance algorithm deals with the redundant switching states to maintain the voltages of the 5LANPC capacitors at a specified level. The comparison between these two modulation strategies was performed by simulation based on MATLAB/Simulink package. Simulation results showed compelling outcomes involving the two techniques concerning the voltage and current characteristics, as well as the equilibrium in the capacitor voltages. By comparing the simulation results, it was found that the performance of the system is relatively better using the PD-PWM strategy.

1 Introduction

In recent decades, converters with the ability to generate multi-level voltages, which are known as multilevel converters (MLC) have become the most attractive in the academic and industrial fields [1-4]. Their attractiveness resulted from the nature of their structure that qualifies there to work in medium and high voltage applications using switches with low voltage rate [5-9]. Moreover, these converters contribute to improving the quality of voltage and current, which leads to reduced total harmonic distortion (THD) and ease of filter design [6]. For more than a decade, three different MLC structures have emerged which have become the main types of the multilevel converters. These three types are the cascaded H-Bridge Converter (CHBC), Diode Clamped Converter (DCC), and Flying Capacitor

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Converter (FCC) [10-14]. These converters have been used by wide applications such as transformational industries, transmission and improving the quality of electric power, and sustainable energy [15-17].

In any case, the MLC experiences imperative impediments, for example, expanding the quantity of levels prompts increment the exchanging count and control intricacy. Increasing the number of levels for more than three also causes a challenge of maintaining the balance of the capacitor's voltages [6, 13, 18]. To overcomes these limitations and challenges, tremendous reduced switching count topologies of the MLC have been proposed [6, 9, 10, 12, 13, 19-21]. From many others of the reduced switching count MLC topologies, the five-level active neutral point clamped(5LANPC) is the most attractive topology. It merges the 3-level Diode Clamped Converter (DCC) and the 3-level Flying Capacitor Converter (FCC) to obtain merit in operating in each quadrant, simply requires one flying capacitor for each leg and produces high quality waveforms [2, 7, 22-25].

Principally, the Flying Capacitors (FCs) are utilized in the 5LANPC to secure the required voltage across the switching devices. Therefore, the accurate setting of the FCs voltages maintains the reliable operation of the converter and the switching devices adopted [26]. Various control strategies have been appeared in the previous literatures to regulate the voltages of the FCs in the multilevel converter which can be categorized into passive and active control strategies. In the passive category, employing the balance booster structures to control the voltages of the FCs leads to immoderate power losses [27-29]. Moreover, the traditional Proportional Integral (PI) controller was introduced in [30] to regulates the FCs voltages. This approach needs a precise tuning of the PI parameters, it may have undesirable peak overshoot, stability problems, and poor time response. The technique of the space vector modulation (SVM) was significantly utilized for governing different converter structures [31, 32]. Despite its effectiveness, the calculation burden of the SVM increase as the converter number of levels increase. In comparison with the other control strategies, the carrier-based pulse width modulation is the simplest and more compact strategy which is known as multicarrier pulse width modulation. Also, this technique can be ordered into different sub-procedures, for example, Phase Disposition Pulse Width Modulation (PD-PWM), Phase Opposition Disposition PWM (POD-PWM), and Alternate Phase Opposition Disposition PWM (APOD-PWM) [33]. In this paper, a comparison of a simplified control algorithm for balancing the capacitor voltages of the three phase 5LANPC based on PD-PWM and APOD-PWM has been carried out. This paper is organized as follows: in section 2, the basic principles of the 5LANPC was introduced, section 3 presents the details of the control algorithm. The system configuration was explained in section 4, the simulation results was showed in section 5, and section 6 contains the conclusions.

2 Five Level-ANPC Inverter

The one leg configuration structure of the 5LANPC is depicted in Fig.1, it contains eight switching devices, two main capacitors C1 and C2 which are maintain (Vdc/2) volt for each, where Vdc is the voltage of the main DC bus. Moreover, it consists of one Flying Capacitor (FC) Cfa, Vfa is the voltage across the Cfa, the current through Cfa is ifa, and ia is the phase current. The backbone of this topology is the four switching devices pairs ((S1a, S′1a) – (S4a, S′4a).

The operation principles of the one-leg 5LANPC comprises eight switching states to achieve five voltage levels based on the sum of the voltage of C1, C2, and Cfa as depicted in Table 1. Table 1 shows the main switching devices, and the remaining switching devices (S′a1, S′a2, S′a3, and S′a4) are work interchangeably with their peers. It can be seen from Table 1 that some inverter output voltage can be realized by different switching states (redundant states). Despite of producing the same output voltage, these redundant states influence the

direction of the FC current which means an indirect effect on the FC voltage. For the typical activity of the 5LANPC, the voltage across Cf for every leg ought to be kept up with at Vdc/4. Therefore, these redundant states will be taken advantage of for the purpose of maintaining the balance of the FC voltage.
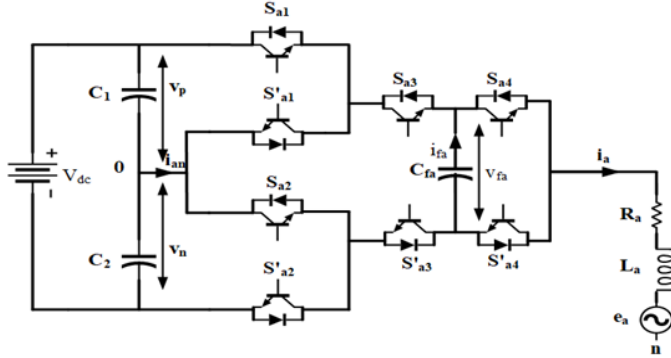
Fig. 1. Structure of the one-leg 5LANPC

TABLE 1. One leg 5LANPC operation principles

S_{a1}	S_{a2}	S_{a3}	S_{a4}	V_{an}	Sign of i_{fa}	Sign of i_a	State
0	0	0	0	$-V_{dc}/2$	N. E	N. E	0
0	0	0	1	$-V_{dc}/4$	+ve	N. E	1
0	0	1	0	$-V_{dc}/4$	-ve	+ve	2
0	0	1	1	0	N. E	+ve	3
1	1	0	0	0	N. E	+ve	4
1	1	0	1	$V_{dc}/4$	+ve	+ve	5
1	1	1	0	$V_{dc}/4$	-ve	N. E	6
1	1	1	1	$V_{dc}/2$	N. E	N. E	7

3 Control Algorithm of the 5LANPC

3.1 PD-PWM strategy

In this strategy, the (n-1) carrier signals shifted in level are compared with the reference sinusoidal signal to produce the required (n) commanded voltage levels. The carrier signals are divided into two groups, the first (n-1/2) group is located above the zero level (positive values), the other (n-1/2) group is below the zero reference (negative values). The following relationships are governed the operation of the proposed strategy for producing the required level:

$$O_i = \begin{cases} 1 & A_m(k) \geq A_{ci}(k) \quad i = \pm1. \pm2...\frac{n-1}{2} \\ 0 & otherwise \end{cases} \tag{1}$$

$$L = \sum_{i=0}^{n-1} O_i \tag{2}$$

Where O_i is the output of the ith comparator, A_m (k) is the magnitude of the reference sinusoidal signal, A_ci (k) is the magnitude of the ith carrier signal, n is the required number of levels, and k is the sampling instant. Equations 1 and 2 rearrange the levels sequence in

ascending order, such as level 0 refers to the output voltage of (-Vdc/2), level 1 refers to (-Vdc/4) and so on.

3.2 APOD-PWM strategy

In this strategy, (1) and (2) are valid, it differs from the PD-PWM strategy only in the alternating the phase of the carrier signal by 180° from its adjacent carrier signals.

3.3 Switching selection algorithm

As shown in Table 1, the effect of the redundant states 1 and 2 on the FC current (ifa) is opposite despite they producing the same output voltage, the same case is true for the redundant states 5 and 6. Therefore, the effect of these states on the FC current leads to its indirect effect on the FC voltage balance. As a result, the proposed switching selection algorithm can be realized depending on the three parameters which are, the required level, the FC voltage, and the direction of the FC current. The switching selection algorithm has been configured as shown in Fig.2, its basis operation is the decision to use a switch state depending on the FC voltage and the direction of its current. This algorithm deals with the cases that have redundant states, i.e., it deals with states 1 and 2 (see, Table 1) for level 1, and states 5 and 6 for level 3. The remaining states in Table 1 have no effect on the voltage balancing of the FC so that they will not be considered in switching selection algorithm.
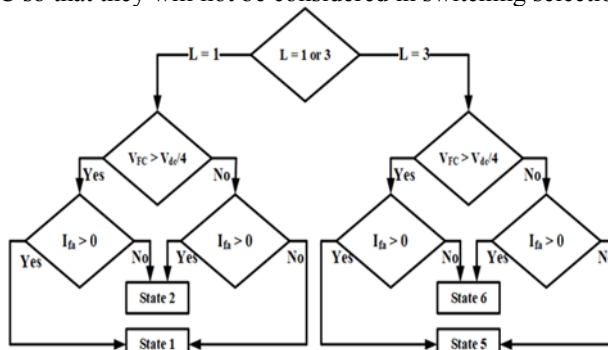

Fig.2. Switching selection algorithm.

4 System Configuration

The 5LANPC and its proposed control strategy are designed and configured using MATLAB/Simulink package as shown in Fig.3. In this figure, the DC Bus block contains the Dc voltage supply with the main capacitors C1 and C2 which are hold voltage of (Vdc/2) for each. The level decision block includes the PD-PWM or the APOD-PWM with the level decision circuit that implemented based on the equations 1 and 2 with n = 5. The switching selection block has been configured according to Fig.2. As stated, only states 1 and 3 need a decision that depends on the value of the FC voltage and the direction of its current, the remaining states are supplied to the 5LANPC directly. The configuration of the switching selection block was performed using MATLAB function block. The Three-Phase 5LANPC block consists of 3-phase 5LANPC, 3-phase L-C-L filter, and 3-phase R-L load.
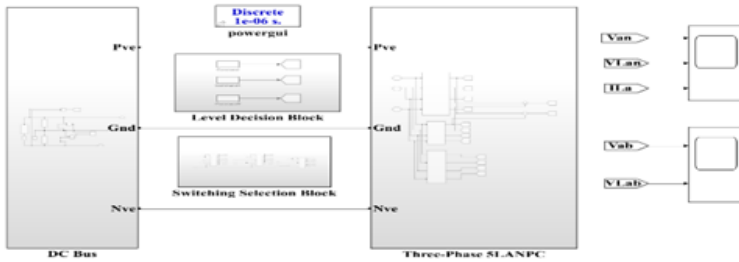
**Fig.3.** 5LANPC with proposed control strategy using Simulink

5 Simulation Results

To verify the effectiveness of 5LANPC based on the proposed control algorithms, simulations were performed using MATLAB/Simulink software package. Table 2 summarizes the system parameters that employed for simulation.

TABLE 2. System Parameters

Parameter	Value
DC Supply Vdc	600 V
DC Bus Capacitors C1 and C2	5000 μF
Flying Capacitor Cf	1500 μF
Fundamental Frequency f	50 Hz
Carrier Frequency	2.5 K Hz

The verification process focused on the performance of the proposed control system and the response of the 5LANPC to command signals. The validity of the level decision block based on PD-PWM and APOD-PWM techniques have been examined and the results are shown in Fig.4. The intersection of the triangle carrier signals with the three-phase sinusoidal reference signals for PD-PWM and APOD-PWM are shown in Fig. 4(a) and Fig. 4(b) respectively. The instantaneous comparison between carrier signals and reference signals result in producing the required level as shown in Fig.4(c).
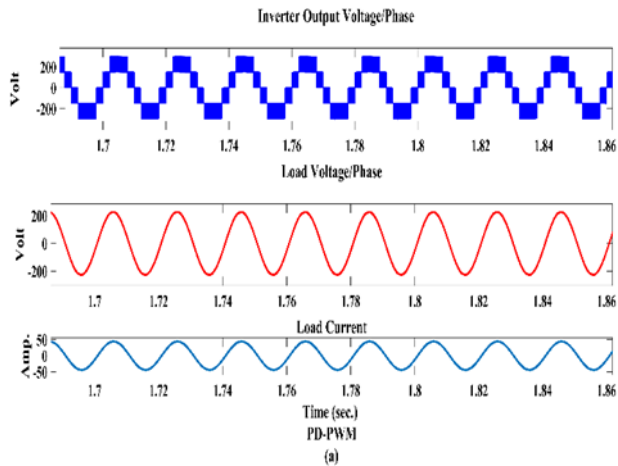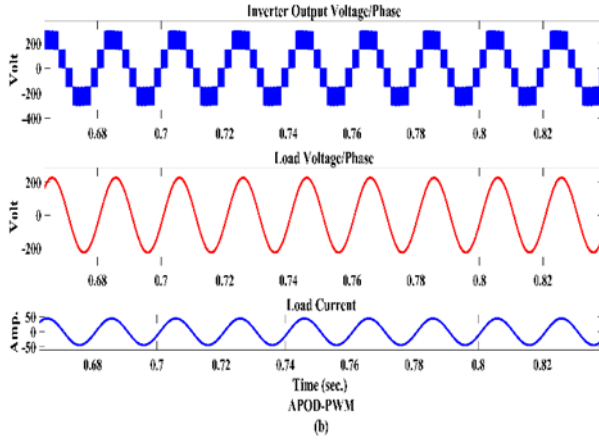

(a)

(b)

(c)
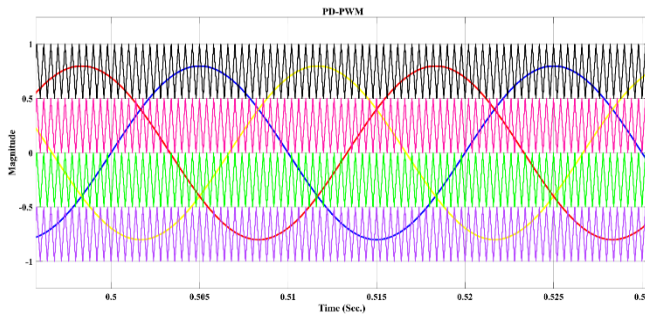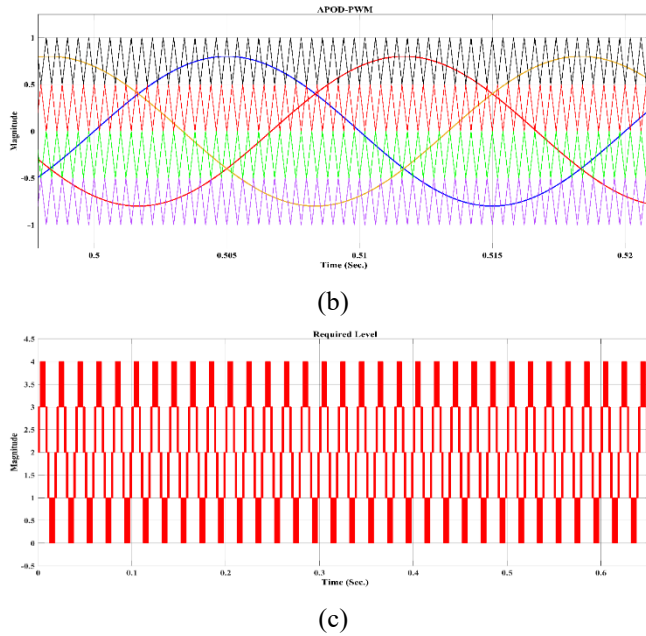
Fig. 4. Simulation Results of the Level Decision Block: (a) PD-PWM, (b)APOD-PWM, (c) Instantaneous Level.

The converter output voltage, filtered load voltage and the load current with PD-PWM and APOD-PWM algorithms are shown in Fig.5. Fig. 5(a) shows the voltages and current with PD-PWM, while the voltages and current with APOD-PWM are shown in Fig. 5(b).

**Fig.5.** output load voltage and current with: (a) PD-PWM, (b) APOD-PWM

Fig. 6 shows the Line-to-Line output voltage from the 5LANPC, these voltages with PD-PWM is in Fig. 6(a), while Fig. 6(b) shows the Line-to-Line output voltage with the APOD-PWM.
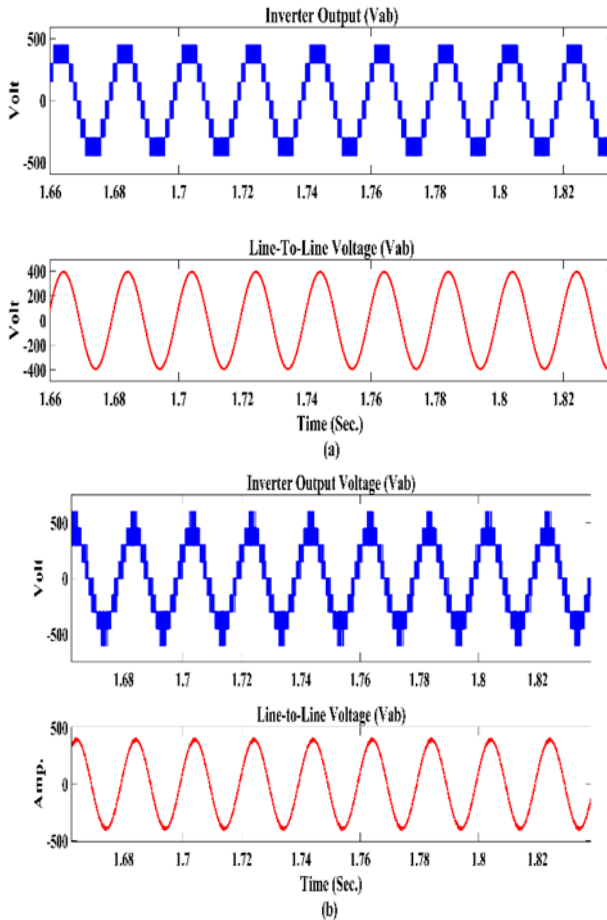
**Fig. 6.** Line-to-Line output voltage with: (a) PD-PWM, (b) APOD-PWM.

An extremely low (THD) for the stage voltage and the line current have been gotten in light of PD-PWM as portrayed in Fig.7. A 0.48% THD is obtained for the phase voltage as shown in Fig.7 (a), and 0.66% THD for the line current as shown in Fig.7 (b). Fig. 8 show the THD measurements of the load voltage and current when the APOD-PWM is adopted.

The voltage balance of the DC bus capacitors C1 and C2 is achieved as shown in Fig.9 for both modulation strategies, the voltages of capacitors C1 and C2 according to PD-PWM are shown in Fig.9(a), and these according to APOD-PWM are shown in Fig. 9(b). Finally, the flying capacitor voltages for two modulation strategies are shown in Fig. 10, where Fig. 10(a) refers to the FC voltages when PD-PWM is employed, Fig. 10(b) refers to FC voltages when APOD-PWM is considered. Table 3 summarizes the performance comparison of the 5LANPC under the DP-PWM and APOD-PWM strategies, it can be noticed that the performance is acceptable with these modulation strategies but the converter behaves best with the PD-PWM
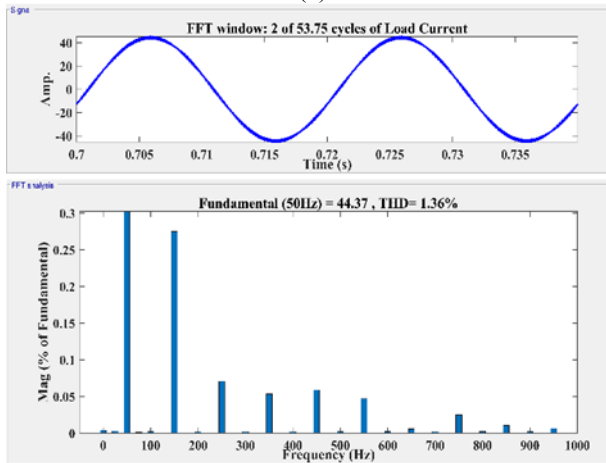

(a)

(b)
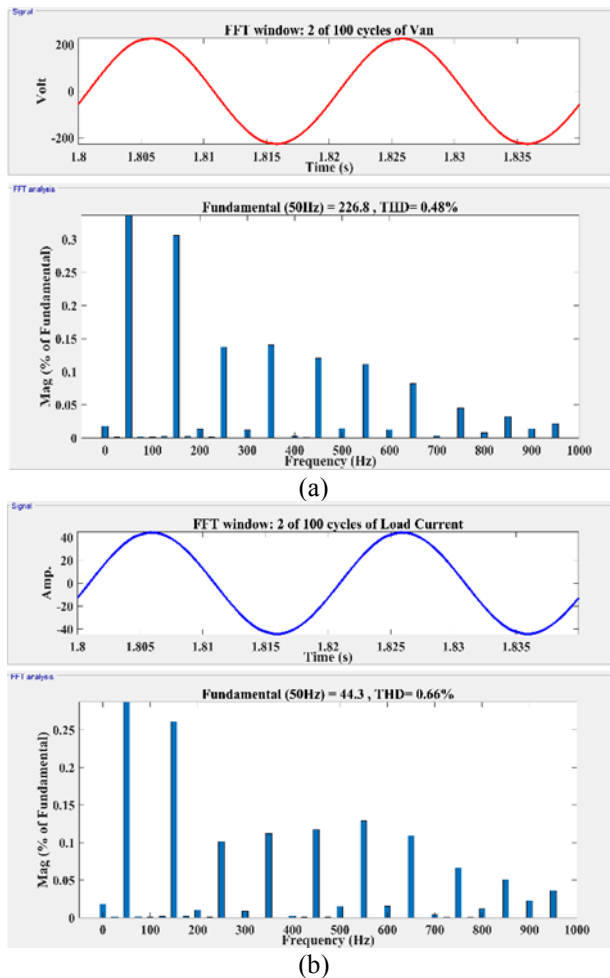
Fig.7. Total Harmonic Distortion of the voltage and current with PD_PWM: (a) THD for phase voltage, (b) THD for line current.
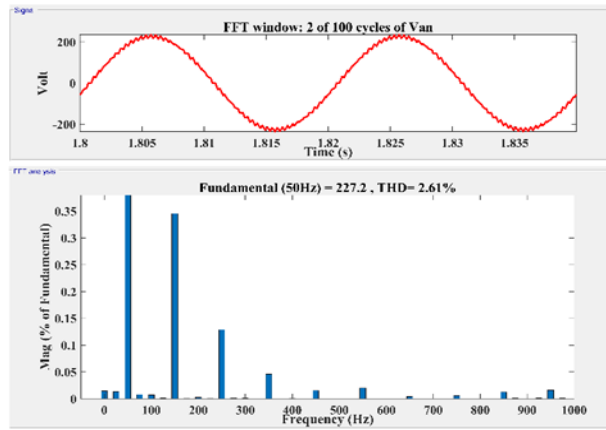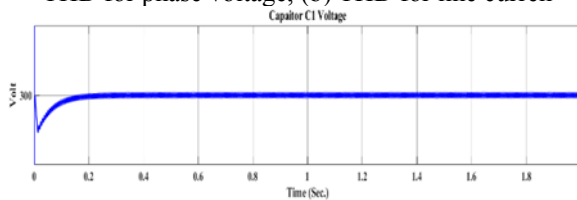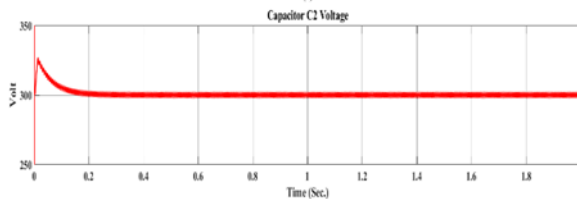
(a)

(b)

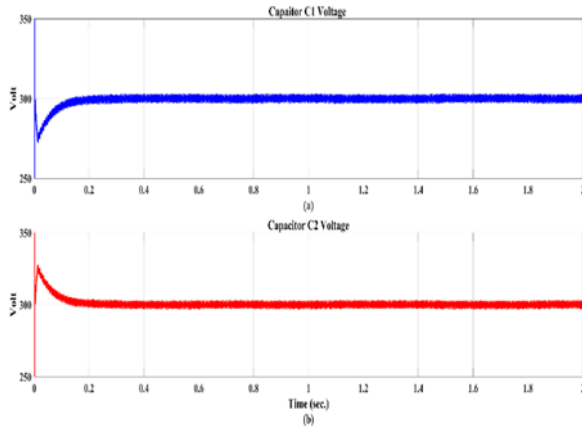**Fig.8.** Complete Harmonic Distortion of the voltage and current with APOD_PWM: (a) THD for phase voltage, (b) THD for line curren

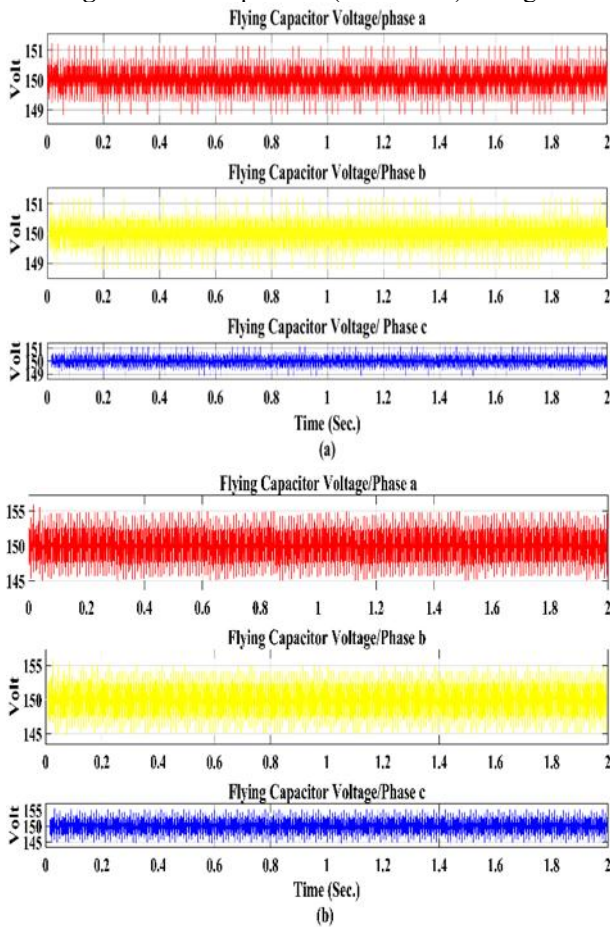**Fig.9.** DC bus capacitors (C1 and C2) voltages.

Fig.10. Flying Capacitors Voltages.

TABLE 3. Performance Comparison

parameter	Value	
	PD-PWM	**APOD-PWM**
Voltages of C1 and C2	$300 \pm 2V$	$300 \pm 2.8\ V$
Voltages of FC	$150 \pm 1.5\ V$	$150 \pm 5.5\ V$
THD of the output voltage	0.48 %	2.61 %
THD of the load current	0.66 %	1.36 %

6 Conclusion

In this work two types of pulse width modulation techniques which are PD-PWM and APOD-PWM were employed and compared for driving 5LANPC. The comparison has been performed from the quality of the output voltage, output current, and the capacitor voltages balance points of view. Moreover, a simplified algorithm is built to keep the capacitor voltages in balance by selecting the appropriate switching state according to the capacitor voltages and the required voltage level. Verification and comparison were carried out by simulation using MATLAB/Simulink software package. Through simulation it can be concluded that the installation of the 5LANPC, which is characterized by a small number of switches and capacitors, leads to a significant simplification of the control system. In confirmation of this, the simulation results showed a high performance of the system using the above two modulation methods, with a better result in favor of the PD-PWM method.

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