Master's Thesis

Design of LC PLL for DDR5 Clock Buffer Application

DDR5 클락 버퍼를 위한 LC PLL 의 설계

by

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August, 2022

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for DDR5 Clock Buffer Application

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Abstract

This thesis describes a wide-range, fast-locking LC PLL for DDR5 clock buffer application. To operate LC PLL at wide range of input frequency, proposed PLL uses LC VCO with 28GHz center frequency and calculates appropriate division ratio of programmable divider for certain input frequency at transient state. Calculating division ratio is achieved by using integer counter and fractional counter, detecting frequency of input clock at transient state. After calculating division ratio, proposed PLL operates as 3rd order charge pump PLL with optimum current value to lock fast.

Proposed PLL is described with Systemverilog and simulation results shows that proposed LC PLL operates at 1 ~ 4.2GHz input frequency, while successfully acquires to lock at under 1μs. Also, LC-VCO is designed in a 40nm CMOS and simulation results shows that tuning range of VCO is ±9.25% with respect to center frequency of 28.2GHz, and VCO dissipates 26.4mW and phase noise is –104.86dBc/Hz at 1MHz offset, operating at center frequency with 1.1V supply voltage.

Keywords : PLL, LC VCO, Fractional counter, Programmable divider, Clock buffer, DDR5, Systemverilog

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Chapter 1

Introduction

1.1 Motivation

As degree of integration of transistor is dramatically increased by Moore's law, a bandwidth of memory is required to be increased as well. Especially, key signal to increase bandwidth of memory is clock, and its frequency range is demand to be widen. Therefore, operating frequency range of clock buffer that filters noise before transmitting clock to memory should be widen. Also, when frequency of clock changes, PLL used in clock buffer should be lock fast not to degrade the overall performance of memory. For example, operating frequency range and stabilization time of DDR5 clock buffer is specified as 1 ~ 4.2GHz and under 1us in JEDEC.

Generally, wide range of PLL is implemented by using ring-type voltage controlled Oscillator(VCO). However, jitter performance of Ring type VCO is worse than that

of LC type VCO, and its frequency range should be wide to meet the specification of frequency range of input clock, which results in slow lock time of PLL.

To address this challenge, this thesis proposes PLL which consists of LC type VCO, programmable divider, frequency detector, and controller that calculates appropriate division ratio of programmable divider at certain input frequency. Integer counter and fractional counter is used as frequency detector and a novel scheme to avoid error due to time skew between integer counter and frequency counter is proposed. After division ratio is calculated, proposed PLL operates as 3rd order charge pump PLL with optimum current value to lock fast.

Also, this thesis shows the design of LC VCO, key component of proposed PLL. The thesis shows overall structure of LC VCO, and analyzes start-up margin of oscillator. Lastly, overall performance of LC VCO is listed by simulating the circuit by SPICE.

1.2 Thesis Organization

This thesis is organized as follows. In Chapter 2, the background of PLL is explained. The basic operations of the general PLL are described. Mainly, Two key performance metric of PLL, which is frequency range and lock time of general PLL is analyzed.

In Chapter 3, LC PLL for DDR5 clock buffer is proposed. Overall structure of proposed PLL, which is described with Systemverilog is explained. Also, Structure of LC VCO is explained and consideration of designing LC VCO is presented in this chapter.

In Chapter 4, Simulation results of proposed PLL are shown. Transient simulation is performed to check the operation of PLL and measure frequency range and lock time of PLL. SPICE simulation of LC-VCO are presented, such as start-up margin, power, phase noise, tuning range.

Chapter 5 summarizes the proposed works and concludes this thesis.

Chapter 2

Background on LC PLL

2.1 Basis of Phase Locked Loop

Phase locked loop(PLL) is used in diverse application. PLL is a feedback system that compares the output phase of signal with the input phase of signal [1]. Its main role is to align output phase of signal to input phase of signal, effectively working as

zero-delay buffer. And well-designed PLL filters the phase noise of the input signal, generating low-jitter output. Also, PLL can be work as frequency multiplier using frequency divider as component of PLL. This characteristic enables PLL to be used in High-speed serial interface, memory interface, RF application and etc.

General architecture of PLL is shown in Fig. 2.1. PLL is composed of Phase-Frequency detector(PFD), Loop Filter(LF), Voltage-Controlled Oscillator(VCO) and Frequency divider. Frequency Divider is optional block since it is necessary when PLL has to be work as frequency multiplier. If frequency divider is removed, PLL generates the frequency of output same as input frequency of signal.

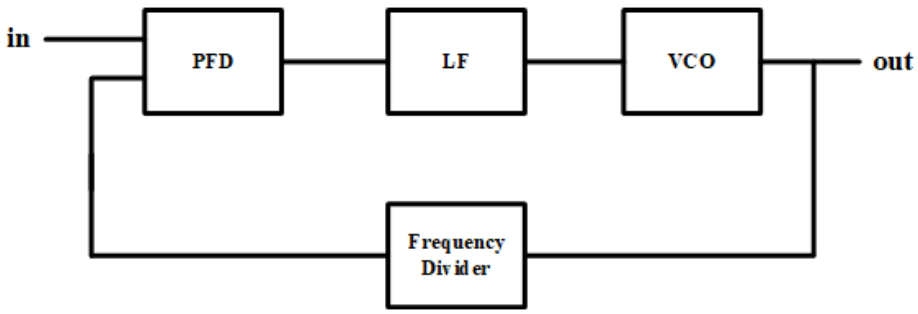


Fig. 2.1 Architecture of general PLL.

PFD compares phase of input signal and phase of feedback signal and generates the output that is proportional to phase difference between input signal and feedback signal (Fig 2.2). The output of PFD is used to LF to control the VCO. In ideal case, output of PFD and phase difference is linear. However, in most cases, linear relationship between phase difference and output of PFD is limited to certain range of phase difference when it is implemented as a circuit. Fig 2.3 is the typical circuit of PFD, which is composed of 2 D Flip-Flop(DFF), and 1 AND gate to reset DFFs. Its linear relationship is limited to ±2π of input phase difference. When input phase difference is larger than 2π, the output of PFD is no longer proportional to the input phase difference and this causes so-called 'Cycle Slipping' [2].

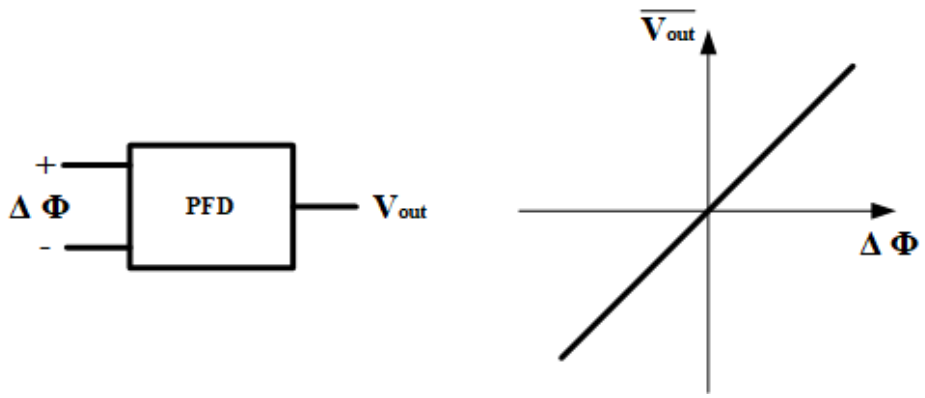


Fig. 2.2 Phase-Frequency Detector and its characteristic curve.

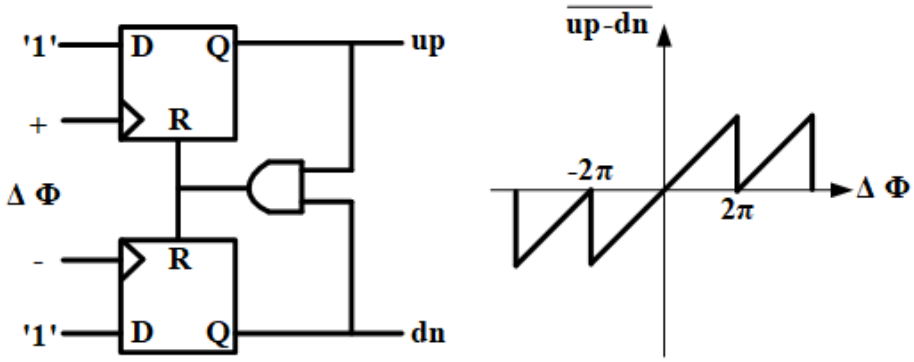


Fig. 2.3 Implementation of Phase-Frequency Detector and its characteristic curve.

VCO is a producer that generates output of signal, and its frequency is proportional to the input voltage (Fig 2.4). There are 2 typical type of VCO, one is Ring type VCO, and the other is LC type VCO. Ring type VCO consists of a number of delay stages with positive feedback to sustain oscillation indefinitely. LC type VCO consists of inductor(L) and Capacitor(C) and negative resistance to cancel out the parasitic resistance of LC tank to sustain oscillation. While output frequency of Ring type VCO is determined by delay of the unit stage, output frequency of LC type VCO is determined by inductance and capacitance. By controlling the delay of unit stage of Ring type VCO or capacitance of LC type VCO with input voltage, proportional relationship between input voltage and output frequency is achieved. This key difference of controlling output frequency between Ring type VCO and LC type VCO results in different characteristic, as shown in Table 2.1.

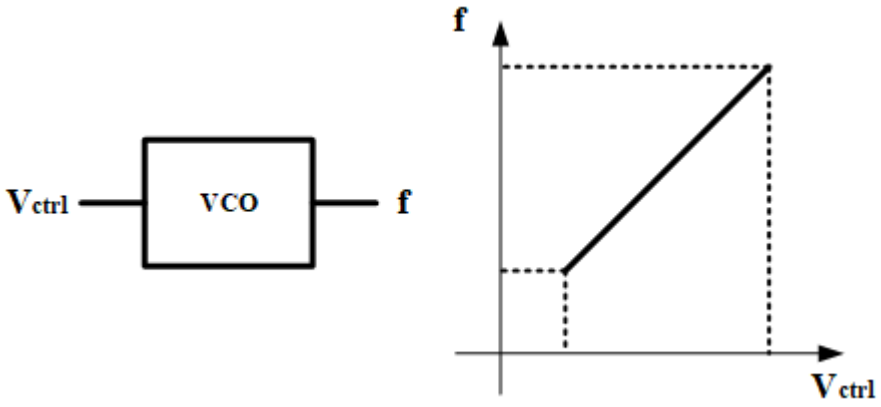


Fig. 2.4 Voltage Controlled Oscillator and its characteristic curve.

Characteristic	LC	Ring
Center freq.	High	Low
Tuning range	Narrow	Wide
Phase noise	Good	Bad
Power dissipation	High	Low
Area	Large	Small

Table. 2.1 Comparison of Ring type VCO and LC type VCO.

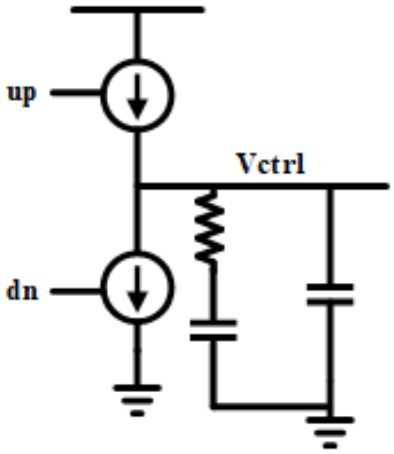


Fig. 2.5 Typical Implementation of Loop Filter with Charge Pump.

Loop filter(LF) is controller that calculates output voltage to control VCO by input which is generated by PFD. LF is a key block of PLL, since it determines overall performance of PLL such as stability, output jitter, lock time, and etc. Usual implementation of LF is by using resistance and capacitance as shown in Fig 2.5, and PLL that uses this LF is Charge Pump PLL (CP PLL) [3].

Fig 2.6. shows the linear model of CP PLL. Overall transfer function of CP PLL of input to output is (assuming $C_1 >> 10C_2$),

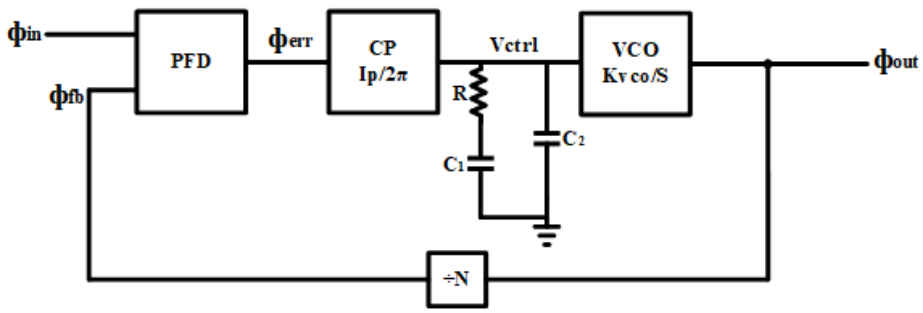


Fig. 2.6 Linear Model of Charge Pump PLL.

$$H(s) = N\frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.1}$$

$$Where\ \ \omega_n = \sqrt{\frac{I_{cp}K_{vco}}{2\pi NC_1}},\ \ \zeta = \frac{\omega_n}{2}RC_1 \tag{2.2}$$

By (2.1) and (2.2), It is able to analyze the loop dynamics of CP PLL, such as stability (phase margin), loop bandwidth, settling time, and etc.

2.2 Frequency Range and Lock Time of PLL

2.2.1 Frequency Range

Operating frequency of PLL is limited by various reasons. First, it is limited by frequency range (or equivalently, tuning range) of VCO. As mentioned in section 2.1, tuning range of Ring type VCO is wider than LC type VCO, in most cases. Therefore, simple way to operate PLL at wide range of input frequency is to use Ring type VCO. However, Ring type VCO has worse phase noise performance than LC type VCO and wide tuning range of VCO results in slow lock time, which will be explained at section 2.2.2. So, trade-off between tuning range, phase noise, lock time should be considered when choosing type of VCO for designing PLL.

Second, operating frequency of PLL is also limited by other components of PLL. For example, PFD is usually implemented to have enough delay on reset path intentionally, to remove 'Dead Zone' problem – phenomena that PFD doesn't respond to small phase errors. So mainly, operating frequency of PFD is limited by the delay of reset path. Also, frequency divider is bottleneck of operating frequency of PLL. Frequency divider that operates at high frequency has to be implemented as CML divider, or injection-locked frequency divider, which consumes large power and its sensitivity to input has to be considered, making IC designer hard to implement it.

This thesis widen the frequency range of PLL by dynamically changing division ratio of programmable divider with respect to input frequency, while using LC type VCO, which has narrow tuning range than that of Ring type VCO. By doing so, the proposed design does not violate the operating frequency of all components of PLL, while successfully operates at desired frequency range of input, which is 1 ~ 4.2GHz.

2.2.2 Lock Time

Lock time of PLL is mainly depend on loop dynamics of PLL. It is well known that in equation (2.1.), settling time of 2nd order linear system strongly depends on ζ [4]. So simplest way to make short lock time is to design CP PLL with $\zeta = 0.707$, which makes transfer function have the smallest peaking at frequency domain.

ζ is not only variable that affects the lock time of PLL. Designer should consider the effect of nonlinear behavior of PLL. As mentioned in 2.1, ‘Cycle Slipping’ is the typical effect that increases the lock time of PLL. If phase error exceeds the input range of PFD, the PFD can’t produce the output proportional to the phase error, and it makes loop filter not be able to compensate the phase error enough. This effect causes overall loop dynamics slow, especially when PLL is at transient state.

This 'Cycle Slipping’ effect happens more frequently at transient state when tuning range of VCO is large. At transient state, if frequency difference between VCO and input is large, PFD receives phase error that is larger than 2π frequently, exhibiting 'Cycle Slipping’ frequently. Therefore, there is a trade-off between lock time of PLL and tuning range of VCO, which makes IC designer hard to implement wide-range AND fast-lock PLL.

Alternative way to make lock time short is to design loop filter of PLL that makes peaking-free transfer function [5]. By making transfer function of PLL to have peak-ingless characteristics, overall lock time of PLL is dramatically reduced, However, it generates additional design challenges, resulting in additional power dissipation, in-creasing design complexity, and etc.

This thesis reduces the lock time of PLL by dynamically changing division ratio of programmable divider with respect to input frequency, which is equivalent effect of output frequency of PLL to reach near to the input frequency instantaneously. While the proposed PLL uses LC type VCO, which has narrow tuning range than that of Ring type VCO, the proposed PLL less exhibits 'Cycle Slipping' effect, such that the output phase of PLL settles fast to the input phase.

2.3 Basis of LC VCO

Fig 2.7 shows the model for a parallel LC oscillator in steady state. L and C are inductance and capacitance of the LC oscillator, respectively. g_{tank} is the conductance of LC tank, due to parasitic components of L and C. Lastly, $-g_{active}$ is the negative conductance of the active device which compensates the loss of tank to sustain the oscillation. The oscillation frequency the LC oscillator is,

$$\omega_{osc} = \frac{1}{\sqrt{LC}} \tag{2.3}$$

By controlling capacitance or inductance, oscillation frequency can be changed. In most cases, controlling capacitance is easier to implement, using varactor or capacitor bank with mosfet switch.

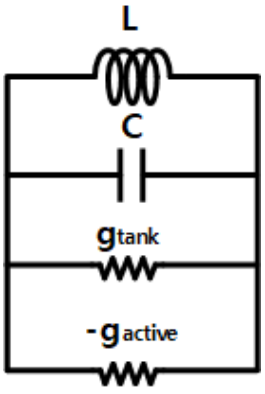


Fig. 2.7 LC oscillator model.

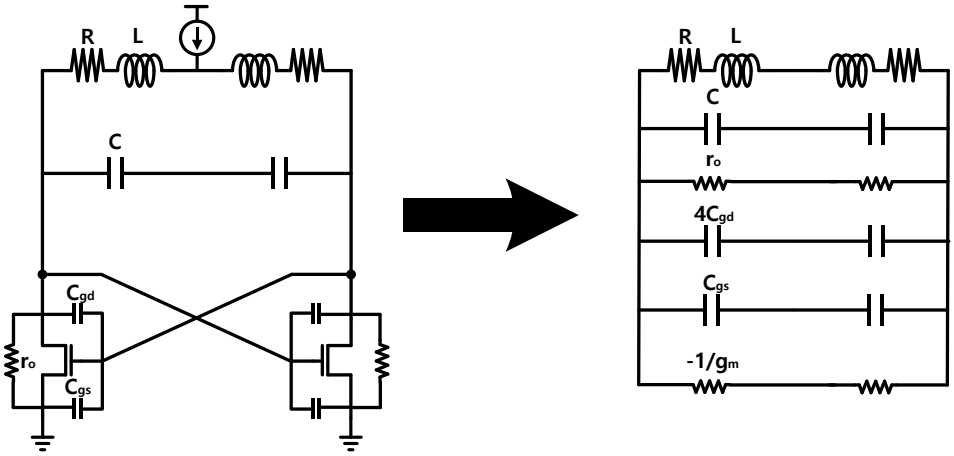


Fig. 2.8 LC oscillator with NMOS pair and its equivalent model.

As mentioned earlier, the loss of LC tank should be compensated by the active device to sustain oscillation, or equivalently the oscillator can start up when the active device compensates the loss of the circuit. The start-up condition for LC oscillator [6] is,

$$g_{active} \geq \alpha g_{tank} \ , \alpha \geq 1 \tag{2.4}$$

Theoretically, $\alpha = 1$ is enough to sustain the oscillation. However, there can be possible error in g_{tank} due to PVT variation, layout effect and etc., so in practical case, it is safe to design LC oscillator to have $\alpha > 1$ to sustain oscillation.

In this thesis, pair of NMOS are used as the active device to compensate the loss of LC tank. To consider all parasitic components of the circuit as shown in Fig 2.8, g_{tank} and g_{active} can be computed as,

$$g_{tank} = \frac{1}{2r_o} + \frac{R\left(C + C_{gs} + 4C_{gd}\right)}{2L}, \qquad g_{active} = \frac{g_m}{2} \tag{2.5}$$

Equation (2.5) states that not only resistance (or conductance) of the circuit matters in the start-up condition, but also inductance and capacitance of the circuit affects to the start-up condition of the LC oscillator. Since parasitic components of the active device are not negligible, designer should consider the parasitic components when computing start up condition of the LC oscillator.

Chapter 3

Design of LC PLL For DDR5 Clock Buffer

3.1 Design Consideration

2 main specification of DDR5 Clock Buffer that JEDEC mentioned are frequency range of input clock and stabilization time. DDR5 clock buffer receives the input clock and produces output clock whose frequency and phase are equal to those of the input. JEDEC specified frequency range of the input clock as 1GHz to 4.2GHz. Also, when the frequency of input clock changes, JEDEC specified that output of the clock buffer should be stabilize under 1us, requiring PLL to lock fast.

As mentioned in Chapter 2, trade-off between frequency range and lock time of PLL makes challenging issues to implement DDR5 clock buffer. For example, by designing PLL with Ring type of VCO whose frequency range is 1GHz to 4.2GHz, The PLL can't lock under 1us without any novel techniques. Also, Ring type of VCO has worse jitter performance than LC type of VCO, makes designer hesitate to use Ring type of VCO to implement for DDR5 clock buffer.

3.2 Overall Architecture

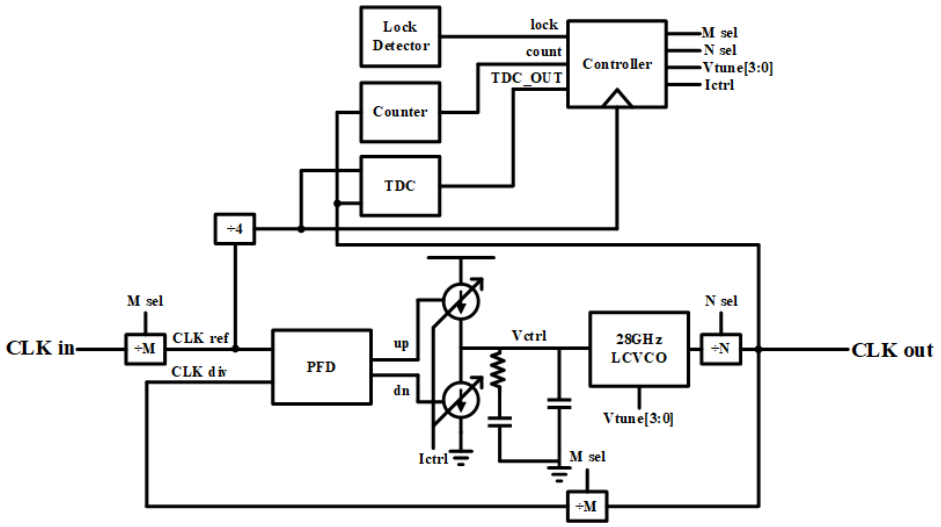


Fig. 3.1 Overall Architecture of the proposed LC PLL.

The overall architecture of the proposed LC PLL is depicted in Fig 3.1. The proposed PLL is composed of 3 programmable divider (÷M, ÷N), PFD, Charge pump and 3rd order loop filter, LC VCO, ÷4 divider, lock detector, counter, Time-to-Digital Converter(TDC), and controller.

Assuming the center frequency of LC VCO is 28GHz, and the tuning range is ±10%, the frequency range of LC VCO is 25.2GHz ~ 30.8GHz. The operation frequency of the VCO is decided by Vctrl, which is calculated by loop filter, and by 4 bit signal Vtune, which is calculated by controller. Detailed implementation of LC VCO is discussed in 3.4.

Division Ratio(N)	Division Ratio(M)	Output Freq. Range = Input Freq. Range (GHz)
7	5	3.6 ~ 4.2
8	4	3.15 ~ 3.85
9	4	2.8 ~ 3.42
10	4	2.52 ~ 3.08
12	3	2.1 ~ 2.57
14	3	1.8 ~ 2.2
16	2	1.575 ~ 1.925
18	2	1.4 ~ 1.711
21	2	1.2 ~ 1.466
24	2	1.05 ~ 1.283
27	2	1 ~ 1.14

Table. 3.1 Relationship between operation frequency of PLL and division ratio of programmable divider(N, M).

The proposed PLL uses 2 kind of programmable divider. ÷N divider can be programmed to use division ratio as 7, 8, 9, 10, 12, 14, 16, 18, 21, 24, 27. This diverse selection of division ratio of ÷N divider allows the proposed PLL to produce output frequency range of 1 ~ 4.2GHz, using LC VCO of center frequency 28GHz with tuning range of ±10%. ÷M divider can be programmed to use division ratio as 2, 3, 4, 5. By selecting division ratio of ÷M divider, ÷M divider limits the input frequency of the

PFD under 1GHz. Table 3.1 shows the detailed relationship of output frequency and division ratio(N, M) of programmable divider.

PFD is implemented as Fig 2.3. its input comes from 2 ÷M programmable dividers. It compares phase error between two inputs and produces output of up and dn signal to enable current source of charge pump.

Charge pump receives up and dn signal from PFD and produces net current to loop filter. The value of current can be controlled by controller with 3bit signal Ictrl. When N and M are decided by input frequency of PLL, overall transfer function of PLL can be determined so that current of charge pump can be decided to make ζ = 0.707 to achieve fast transient response. Table 3.2 shows the relationship between division ratio N and M and current of charge pump for ζ = 0.707. By Table 3.2, current of charge pump is computed as the following equation with $I_{pump,0} = 220\mu A, I_{gain} = 20\mu A$.

$$I_{pump} = I_{pump,0} + I_{gain} I_{ctrl} \tag{3.1}$$

Loop filter is designed as conventional 3rd order filter, using 1 resistor and 2 capacitors, one is connected with resistor in series and the other is connected in parallel with series connection of resistor and capacitor. In this design, the value of R_1, C_1, and C_2 is 4kΩ, 41pF, 4.1pF is chosen, respectively.

Integer counter and Time to Digital Converter(TDC) are to detect input frequency of clock [7]. Integer counter counts the number of positive edge of output clock for 20 cycle of input clock. TDC is used as a fractional counter to compute the residual

Division Ratio(N)	Division Ratio(M)	Ipump (μA) for ζ = 0.707	Ictrl
7	5	240	1
8	4	220	0
9	4	240	1
10	4	280	3
12	3	240	1
14	3	280	3
16	2	220	0
18	2	240	1
21	2	280	3
24	2	340	6
27	2	360	7

Table. 3.2 Relationship between division ratio of programmable divider(N, M) and current of charge pump for ζ = 0.707.

time distance that integer counter can't compute, whose output is phase difference between output clock and the input clock divided by 20 with using 31bit thermometer code, and its resolution t_{LSB} is 30ps/bit.

Lastly, the controller receives the output of counter, TDC, Lock detector as inputs, produces appropriate division ratio(N, M), I_{ctrl}, V_{tune} as outputs. The operating clock of controller is the input clock of PLL divided by 4M sampled by output clock.

3.3 Operation Principle

The proposed LC PLL operates by dividing a total of 3 states, as shown in Fig 3.2. At state 0, The PLL detects the input frequency by integer counter and fractional counter, and calculates the appropriate value of division ratio(N, M), Ictrl, and Vtune. At state 1, Charge pump and loop filter is enable and the PLL operates as conventional CP PLL, calculating Vctrl. If the PLL acquires to lock (Lock detector produces ‘Lock’ signal to controller), the state of PLL transit to state 2. At state 2, Controller monitors the value of Vctrl and if Vctrl is stuck at 0 or Vdd, the state changes to State 0, and performs overall calculation again.

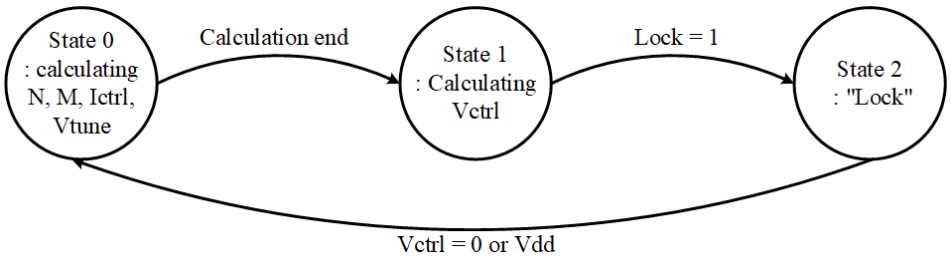
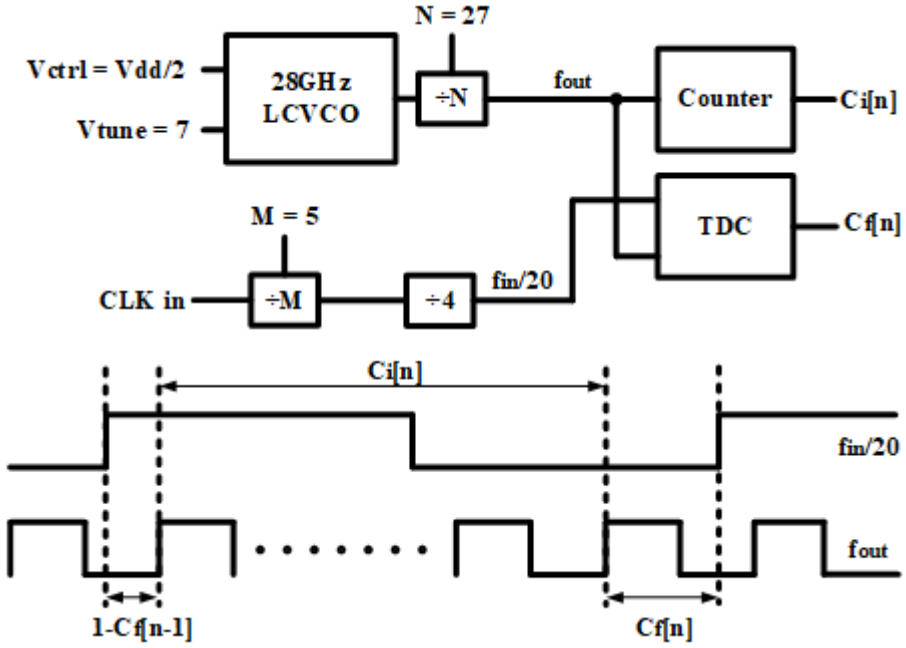


Fig. 3.2 State diagram of the proposed PLL.



$$\frac{f_{out}}{(f_{in}/20)} = C_i[n] + 1 + \left(C_f[n] - C_f[n-1]\right)\frac{t_{LSB}}{T_{out}}$$

Fig. 3.3 Detecting input frequency by counter and TDC.

At state 0, controller detect the input frequency by setting the value of N, M, Vtune, Vctrl as 27, 5, 7, Vdd/2, respectively. The values set by the controller make output frequency approximately 1GHz, so TDC receives inputs as 1GHz clock and input clock of PLL divided by 20. Since the input frequency range is 1 ~ 4.2GHz,

$$\frac{f_{in}}{20} = 50 \sim 210[MHz],\ \frac{f_{out}}{(f_{in}/20)} = 4.76 \sim 20 \qquad (3.2)$$

Thus, by counting the number of cycle of 1GHz output clock for 1 cycle of input clock divided by 20, it is able to detect the frequency of input clock as shown in Fig 3.3, and

calculate the appropriate value of N, M, Ictrl. Table 3.3 shows detailed relationship between counted value and input frequency range, and N.

However, time skew between the integer counter and the TDC inputs may cause error of the counted value, resulting in wrong division ratio [8, 9]. This problem happens when the output of integer counter and the TDC are triggered by different clock when time skew exists. Thus, the simplest solution to prevent the issue is to use the same triggering clock of counter and TDC. For example, by implementing TDC as

Input Frequency Range(GHz)	Counted Value	Division Ratio(N)
3.6 ~ 4.2	4.76 ~ 5.74	7
3.15 ~ 3.85	5.37 ~ 6.56	8
2.8 ~ 3.42	6.04 ~ 7.38	9
2.52 ~ 3.08	6.71 ~ 8.2	10
2.1 ~ 2.57	8.06 ~ 9.85	12
1.8 ~ 2.2	9.4 ~ 11.49	14
1.575 ~ 1.925	10.74 ~ 13.13	16
1.4 ~ 1.711	12.08 ~ 14.77	18
1.2 ~ 1.466	14.1 ~ 17.23	21
1.05 ~ 1.283	16.11 ~ 19.69	24
1 ~ 1.14	18.13 ~ 20	27

Table. 3.3 Relationship between counted value, input frequency range, and division ratio(N).

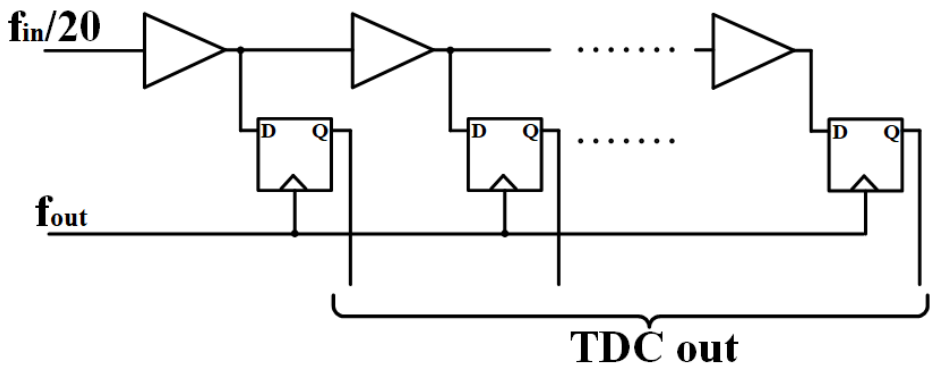


Fig 3.4 Implementation example of TDC synchronized to fout.

shown in Fig 3.4, output of the TDC is synchronized to output clock, which is the triggering clock of integer counter.

Since the output of the TDC and counter are both synchronized to output clock, controller should be synchronized to output clock to get enough timing margin as well. But the frequency range of output clock is 1 ~ 4.2GHz, it is unrealistic to use output clock as operating clock of controller, since the operation of controller is too complex to design manually rather than synthesizing RTL code of controller. To resolve the issue, proposed PLL generates the operating clock of controller by using sampled input clock divided by 20 by positive edge of output clock with delay added. As illustrated in Fig 3.5, using sampled clock with delay doesn't change the calculation result of division ratio, since output of counter and TDC that are generated between the positive edges of fin/20 are useless. The outputs that are generated right after the positive edge of fin/20 are necessary values to calculate division ratio.

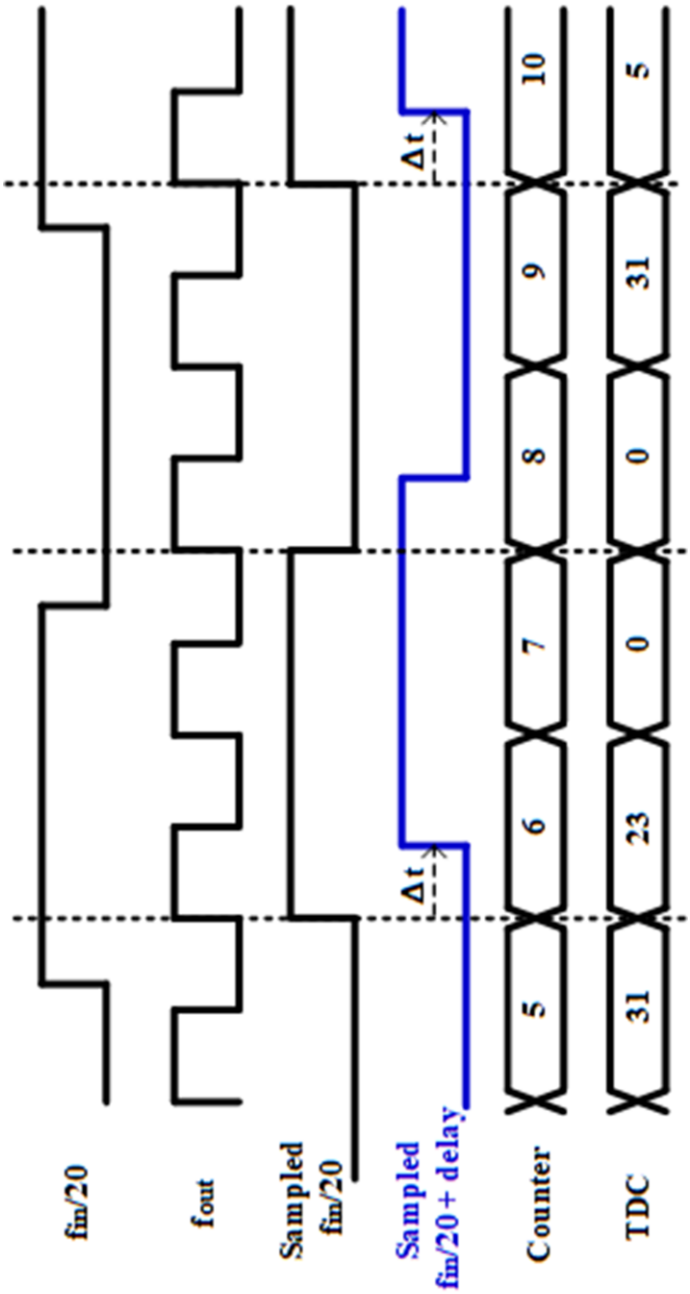


Fig 3.5 Timing diagram of detecting input frequency.

However, there may be a failure to sample input clock divided by 20 by positive edge of output clock, when both positive edges of clock are aligned so that timing violation occurs. For example, if $f_{out}/(f_{in}/20) = 4.25$, both clocks can be aligned every 4 cycles of fin/20. In this situation, the system fails to generate the positive edge of operating clock of controller at right timing and makes wrong value of division ratio. To resolve the issue, the controller doesn't sample the output of counter and TDC and bypass 1 cycle when output of the TDC is 0, as illustrated in Fig 3.6. Then controller measures counted value of 2 cycle of fin/20 and divides the counted value by 2 by using the information that bypass happened or not. The proposed PLL ruled out the situation that positive edges of fin/20 and fout are aligned again after bypassing, which means that PLL is at locked state.

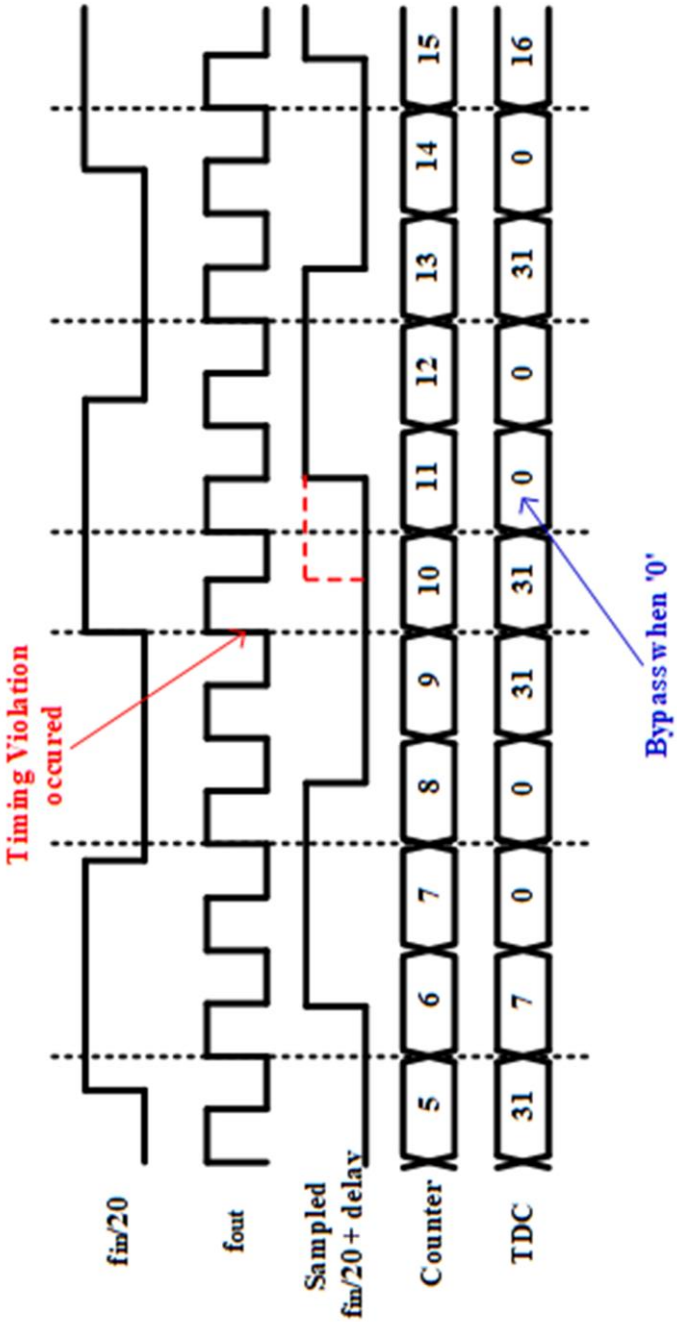


Fig 3.6 Timing diagram of detecting input frequency when fout/(fin/20)=4.25.

By detecting input frequency by counted value, the proposed PLL also calculates Vtune of LC VCO. By defining f_{min} as the minimum oscillation frequency of VCO, K_{vco} as the gain of the VCO with respect to V_{ctrl}, K_{DCO} as the gain of the VCO with respect to V_{tune}, frequency of LC VCO is determined by following equation,

$$f_{vco} = f_{min} + K_{vco}V_{Ctrl} + K_{DCO}V_{tune} \quad (3.3)$$

Since $\frac{f_{vco}}{N} = f_{out}$, Therefore,

$$V_{tune} = \frac{1}{K_{DCO}}\left(\frac{N}{(C_i[n]+1)T_{1GHz} + (c_f[n] - c_f[n-1])t_{lsb}} - K_{vco}V_{ctrl} - f_{min}\right) \quad (3.4)$$

To stay in lock state when supply voltage or temperature vary in time, the proposed PLL calculates Vtune by equation (3.4) with Vctrl = Vdd/2. Direct calculation of Vtune by (3.4) is impossible to implement as digital circuit, thus, in this design, look-up table of Vtune with respect to counted value is implemented in the controller.

After calculating division ratio N, M, Ictrl, Vtune, the state of the controller changes to state 1. At state 1, the conventional 3rd order CP PLL operates and calculates Vctrl, heading to phase and frequency lock. Since controller configured the current of charge pump to make ζ = 0.707, the proposed PLL performs fast transient response and acquires to lock fast.

After the proposed PLL successfully acquires to lock, Lock detector generates 'Lock' signal and the state of the controller changes to state 2. At state 2, controller monitors the value of Vctrl. if Vctrl is stuck at 0 or Vdd, which means the frequency of input clock is out of range to track with present division ratio, the state of controller

changes to State 0, and performs overall calculation again. Also, to reduce jitter of output clock, controller reduces current of charge pump.

3.4 Implementation of LC VCO

LC VCO, the key block of the proposed PLL, is designed at 40nm CMOS technology, as shown in Fig 3. 7. Designed LC VCO is consists of nmos pair for negative resistance, 2 varactors whose capacitance are controlled by Vctrl, capacitor bank whose capacitance is controlled by digital 4bit input Vtune, a single inductor provided by PDK with inductance of 63.738pH and Q factor of 33, and current mirror that multiplies the reference current 1mA with ratio of 15 and provides the current to the core of the circuit.

A pair of nmos is chosen to compensate the loss of LC tank rather than adding pair of pmos. Adding pair of pmos increases g_{active}, but parasitic components due to active device also increases resulting in increase of g_{tank}. In this design, increase of g_{tank} is higher than increase of g_{active} by adding pair of pmos, making start-up condition of LC VCO worse. Therefore, a pair of nmos is employed rather adding pair of pmos. This choice of design degrades the phase noise performance of VCO, since the circuit lacks of pull-up device resulting in difference between rising time and falling time of output of VCO.

Controlling oscillation frequency is achieved by controlling Vctrl, voltage of varactor, and by controlling Vtune, digital input of capacitor bank. The combination of analog and digital fashion of controlling oscillation frequency widen the tuning range of oscillator. Detailed performance of LC VCO will be discussed in section 4.2.

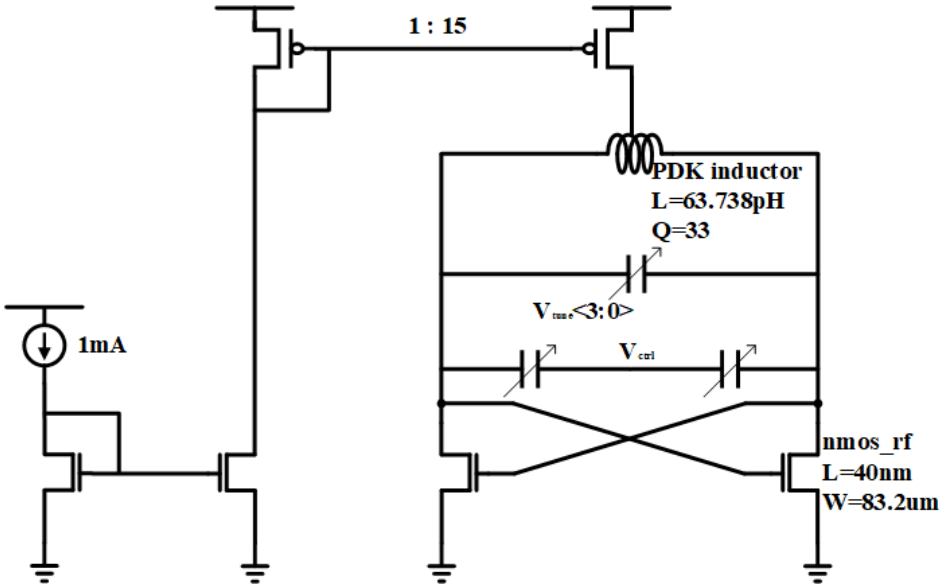


Fig. 3.7 Circuit implementation of LC VCO.

3.5 Alternative Design Choice of LC PLL for DDR5 Clock Buffer

The thesis showed how to implement LC PLL for DDR5 clock buffer by using LC VCO with center frequency of 28GHz and tuning range of ±10%. However, it is still challenging issue to implement LC VCO with center frequency of 28GHz in other CMOS technology. Also, it is hard to implement programmable divider that divides near 28GHz directly. As mentioned in chapter 2, high-speed frequency divider can be implemented as CML type divider or injection locked frequency divider that has more challenging design issues than CMOS type divider.

To avoid complex design issues of implementing LC VCO and programmable divider, alternative design choice is to use LC VCO having lower center frequency than 28GHz and wide tuning range than ±10%. For example, by using LC VCO with center frequency of 24GHz and tuning range of ±15%, the number of division ratio(N) of programmable divider is reduced than previously described design, as shown in Table 3.4. But implementing LC VCO having wide tuning range also challenging, thus, designer should consider the trade-off of design complexity between wide tuning range of LC VCO, high center of LC VCO and high speed programmable divider.

Input Frequency Range(GHz)	Division Ratio(N)
3.4 ~ 4.2	6
2.55 ~ 3.45	8
2.27 ~ 3.06	9
1.7 ~ 2.3	12
1.275 ~ 1.725	16
1.133 ~ 1.533	18
1 ~ 1.15	24

Table. 3.4 Relationship between input frequency range, and division ratio(N), when employing LC VCO of center freq. = 24GHz, tuning range = ± 15%.

Chapter 4

Simulation Result

4.1 PLL

The proposed PLL is described with Systemverilog to verify the operation with the range of input frequency 1 ~ 4.2GHz, and to check whether the PLL successfully acquires to lock under 1μs when input frequency changes.

Fig 4.1 shows the transient simulation of the proposed PLL when input frequency changes from 1.71GHz to 2.07GHz. When input frequency changes, the PLL increases Vctrl due to frequency error between input clock and output clock. After Vctrl reaches Vdd, controller changes the state from 2 to 0, calculating division ratio(N, M),

Vtune. After Calculation is done, controller changes the state from 0 to 1, and CP PLL operates to acquire lock by calculating Vctrl. After PLL successfully acquires to lock, controller changes the state from 1 to 2. The example shows that overall lock time when input frequency changes from 1.71GHz to 2.07GHz is about 0.406us.

Fig 4.2 shows the transient simulation of the proposed PLL at state 0. As described in Chapter 3, controller is operated by the clock which is sampled version of input clock divided by 20 with additional delay. The controller samples the outputs of counter and TDC by operating clock. By sampling the outputs of counter and TDC, controller calculates the ratio, fout/(fin/20), which is the counted value. By counted value, the controller calculates appropriate value of N, M, Ictrl, Vtune, and adopts the calculated value at state 1.

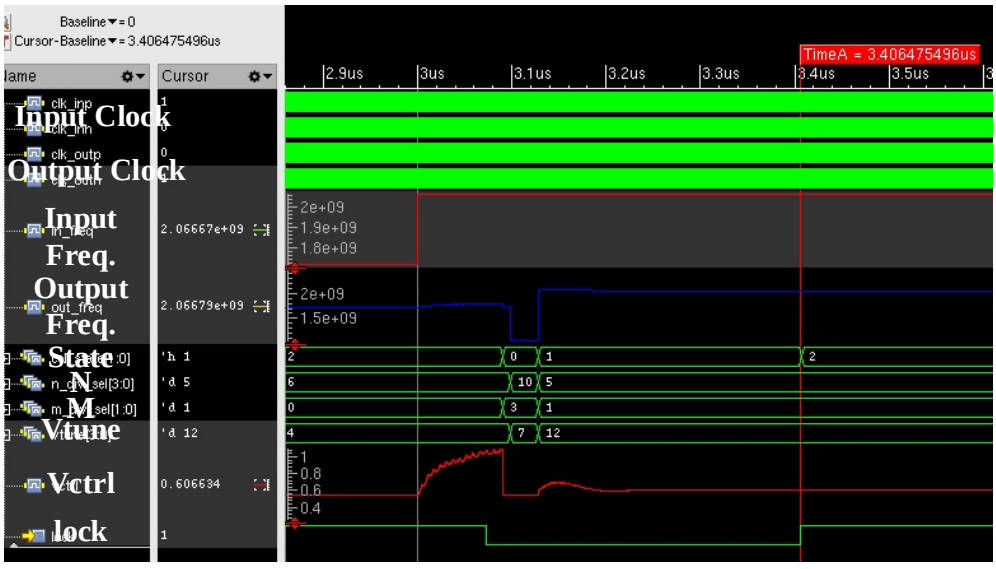


Fig. 4.1 Transient simulation of proposed PLL when input frequency changes from 1.71GHz to 2.07GHz.

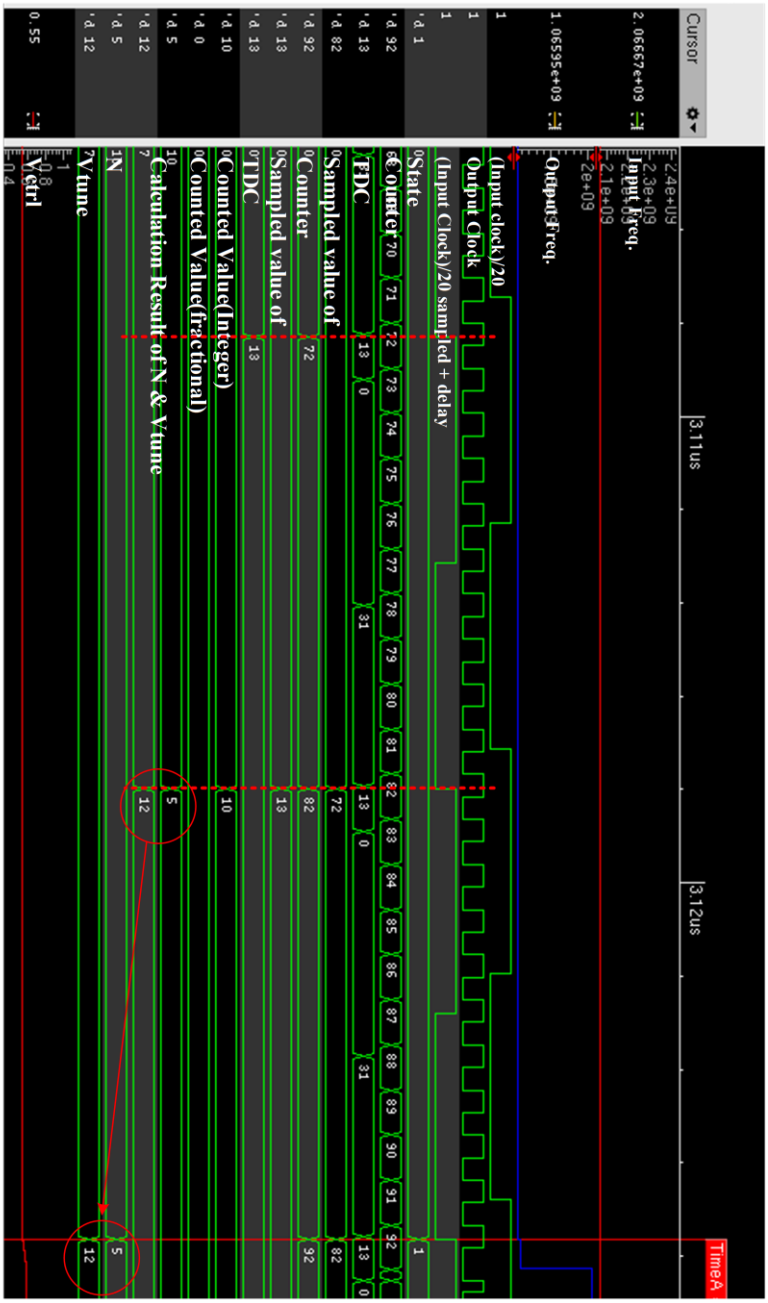


Fig. 4.2 Transient simulation of the proposed PLL at state 0.

Fig 4.3 shows the transient simulation of the proposed PLL sweeping input frequency from 1GHz to 4.2GHz by increasing the frequency by 0.356GHz at every 1μs. The simulation result shows that the proposed PLL successfully acquires to lock under 0.5μs while input frequency changes from 1GHz to 4.2GHz. division ratio (N, M), Vtune are correctly calculated and Vctrl stays near Vdd/2 when the PLL is locked to track transient variation of supply voltage and temperature.

Table 4.1 summarizes the comparison with recently reported PLL. Although the proposed PLL hasn't been fabricated to the IC, it is worth to notice that the proposed PLL is the only design that meets the specification of DDR5 clock buffer of JEDEC while composing PLL with LC oscillator.

	This Work	[10] ISSCC '22	[11] JSSC '19	[12] CICC '20
Technology	- (40nm CMOS)	28nm CMOS	65nm CMOS	22nm FinFET CMOS
PLL Architecture	Digitally -Assisted CP PLL	BB DPLL	ADPLL	Digitally -Assisted CP PLL
Oscillator Type	LC	LC	Ring	Ring
Reference Frequency	1-4.2GHz	250MHz	50MHz	20-200MHz
Output Frequency Range	1-4.2GHz	8.5-10GHz	1-2GHz	0.2-5GHz
Lock Time	<0.5μs	<1.56μs	<0.7μs	<0.2μs

Table. 4.1 Comparison with State-Of-The-Art Design.

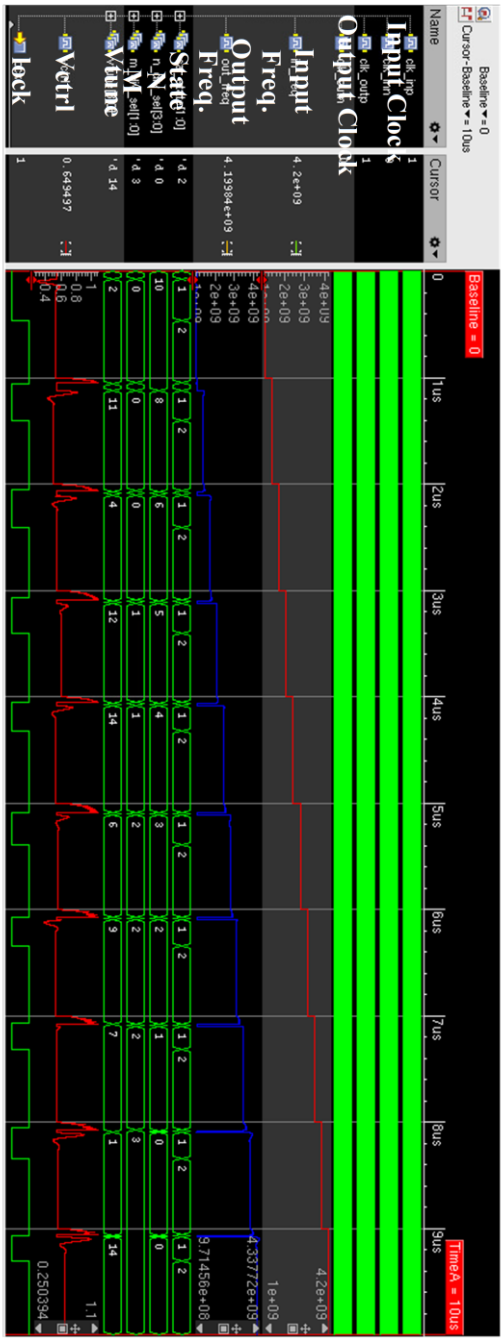


Fig. 4.3 Transient simulation of proposed PLL sweeping input frequency from 1GHz to 4.2GHz at every 1µs.

4.2 LC VCO

Fig 4. 4 shows the transient simulation result of LC VCO, when vctrl = Vdd/2, Vtune = 7. The simulation result shows that designed LC VCO oscillates at 28.2GHz at center of the range of Vctrl and Vtune. Also, designed LC VCO has about 500mV voltage swing. By sweeping Vctrl and Vtune, gain and tuning range of LC VCO can be obtained, as shown in Fig 4.5 and 4.6. The result shows that K_{VCO}, K_{DCO}, and tuning range of the designed LC VCO are 2.725GHz/V, 0.1735GHz/bit, ±9.25% respectively.

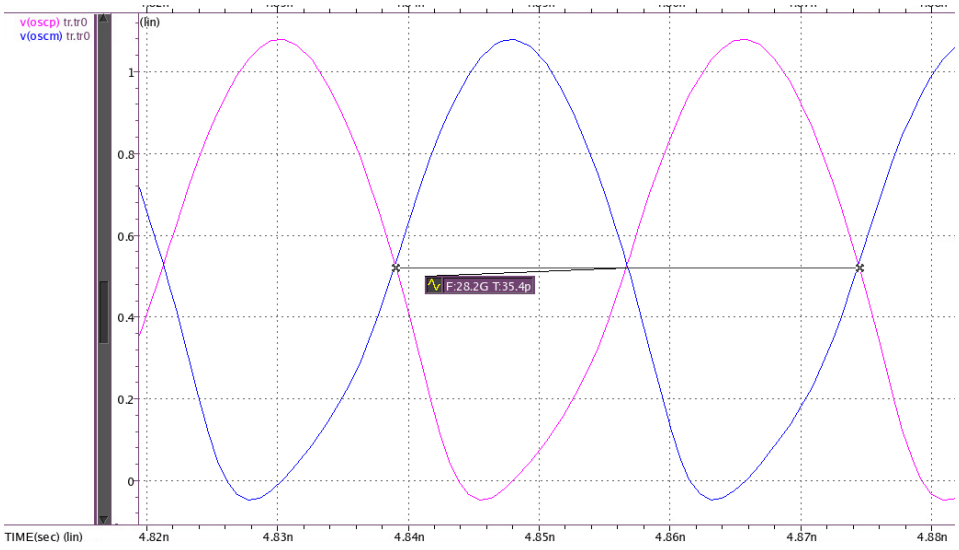


Fig. 4.4 Transient simulation result of LC VCO.

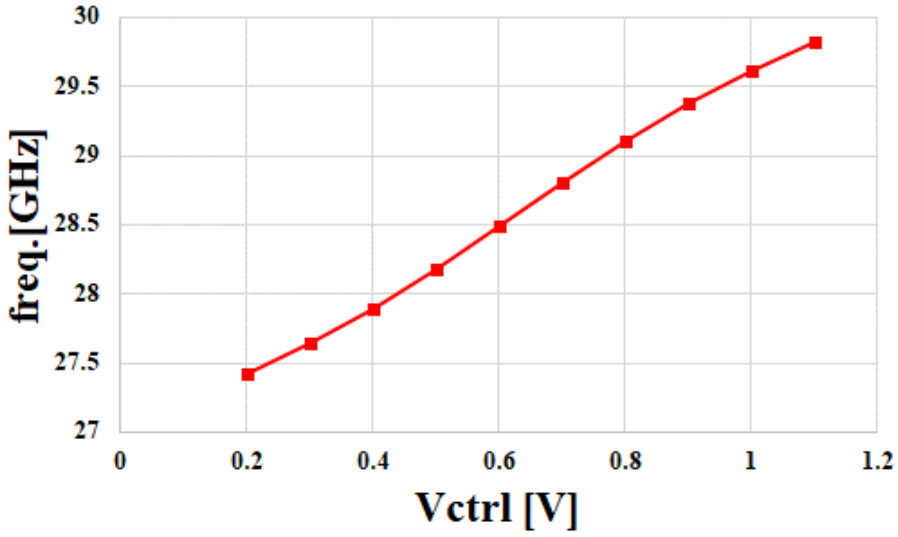


Fig. 4.5 Vctrl – Frequency curve with Vtune = 7.

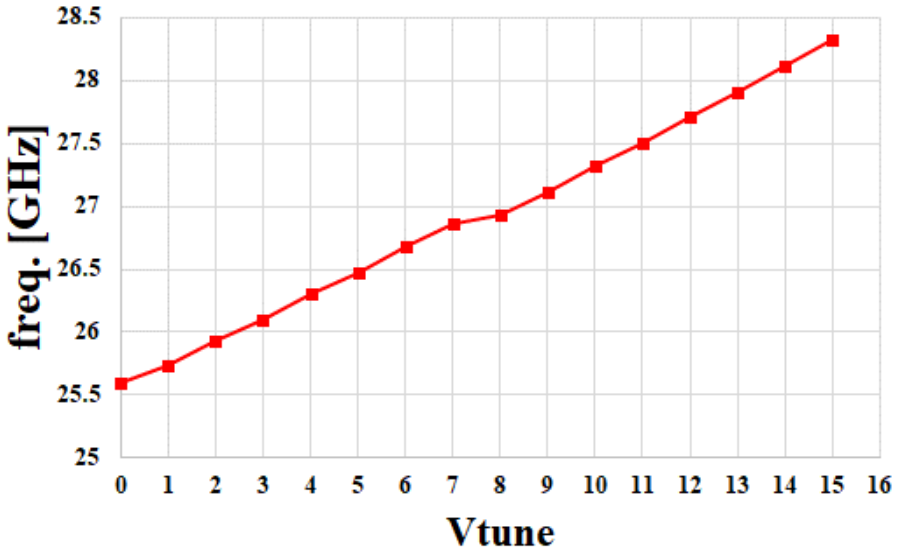


Fig. 4.6 Vtune – Frequency curve with Vctrl = Vdd/2.

Fig 4. 7 shows the AC simulation of LC VCO, plotting impedance between oscillation node and conductance of active device. Since, $Z_{eff} = -Z_{acitve} || Z_{tank}$ is minimum at oscillation frequency due to the fact that the imaginary part of the Z_{eff} is 0. Thus, by simulating the impedance of LC VCO, $\alpha = \frac{g_{active}}{g_{tank}} = \frac{g_{active}}{g_{eff}+g_{active}}$ can be obtained. The simulation results shows that is 3.15.

Fig 4. 8 shows phase noise simulation result of LC VCO. The simulation result shows that the designed VCO has phase noise of -104.86dBc/Hz at 1MHz offset. Table 4. 1 summarizes the performance of designed LC VCO.

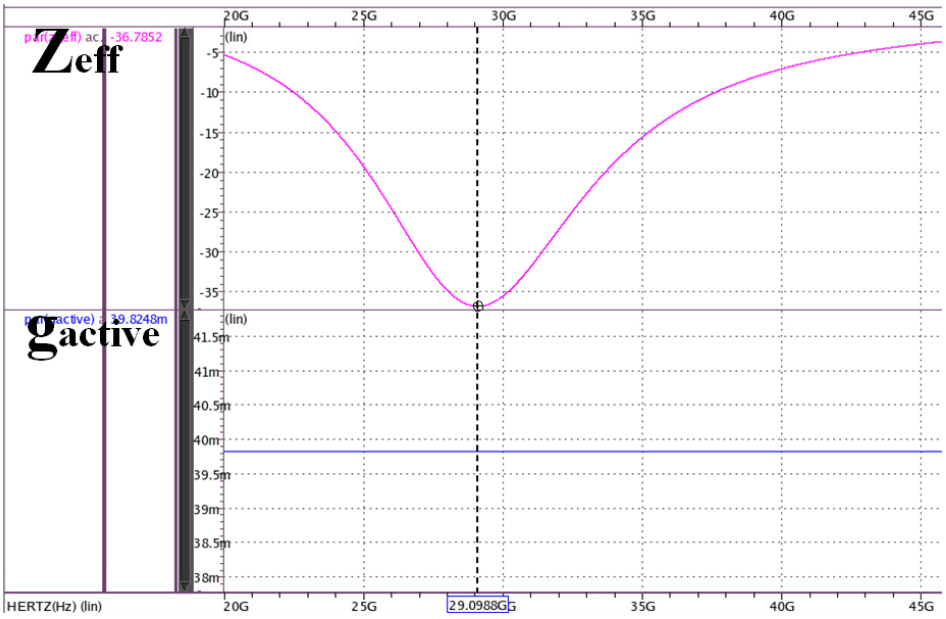


Fig. 4.7 AC simulation result of LC VCO.

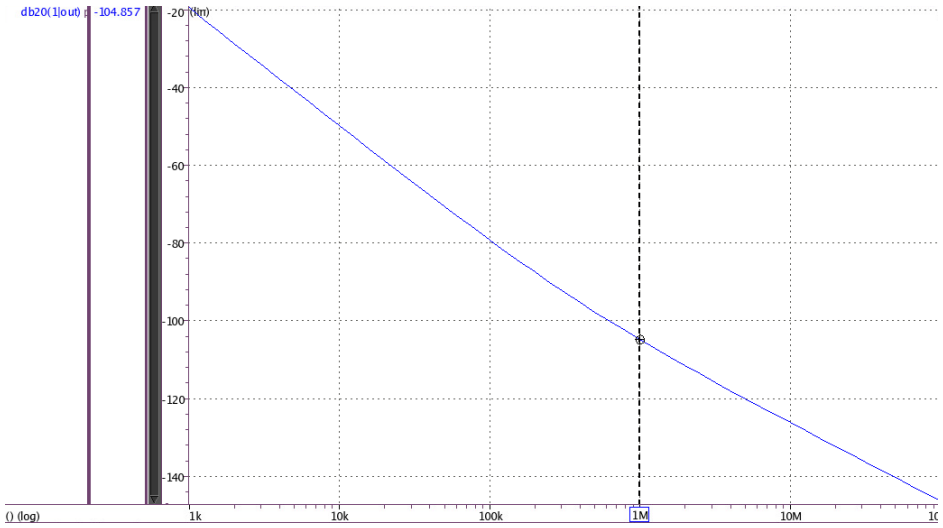


Fig. 4.8 Phase noise simulation result of LC VCO.

Center freq.	28.2 GHz
Kvco	2.725GHz/V
Kdco	0.1735GHz/bit
Tuning Range	±9.25%
Output voltage swing	500mV
Start-up Condition(α)	3.15
Power (@ cen. freq.)	26.4mW
Phase noise	-104.86dbc/Hz @ 1MHz -126.19dBc/Hz @ 10MHz

Table. 4.2 Performance summary of designed LC VCO.

Chapter 5

Conclusion

In this thesis, wide-range, fast-locking LC PLL for DDR5 clock buffer application is proposed. The proposed PLL detects the frequency of input clock at transient state, and calculates appropriate division ratio of programmable divider, current of charge pump, digital tuning voltage of LC VCO. After calculation, the proposed PLL operates as conventional 3rd order charge pump PLL. After the proposed PLL successfully acquires to lock, the proposed PLL monitors analog tuning voltage of LC VCO and re-calculate the parameters when analog tuning voltage stuck to supply voltage or ground.

The proposed PLL described with Systemverilog and simulation result shows that the proposed PLL acquires to lock at 1 ~ 4.2GHz under 1μs. LC VCO for proposed PLL has been designed in 40nm CMOS technology, and simulation result shows that center frequency, tuning range, phase noise, and power of VCO are 28.2GHz, ±9.25%, -104.86dBc/Hz at 1MHz offset, 26.4mW at supply voltage of 1.1V.

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초 록

본 논문은 DDR5 Clock Buffer 를 위한, 넓은 범위에서 빠르게 락을 하는 LC PLL 에 대해서 설명한다. 넓은 범위의 입력 주파수에서 LC PLL 을 동작하기 위해, 제안한 PLL 은 28GHz 가 중심 주파수인 LC VCO 을 사용하여, 과도 상태에서 특정 입력 주파수에 알맞는 프로그램 가능한 divider 의 제수를 계산한다. 제수의 계산은 과도 상태에서 입력 클락의 주파수를 감지하는 정수 카운터와 소수 카운터를 통해 이루어진다. 제수의 계산 이후, 제안한 PLL 은 빠르게 락을 하기 위한 최적의 전류 값으로 3 차의 Charge pump PLL 로 동작한다.

제안한 PLL 은 systemverilog 로 기술되었고 시뮬레이션 결과 제안한 LC PLL 은 1 ~ 4.2GHz 의 입력주파수에서 동작하며, 1us 이내에서 성공적으로 락을 한다. 또한, LC-VCO 가 40nm CMOS 공정에서 설계되었고, 시뮬레이션 결과 VCO 의 튜닝 범위가 중심 주파수 28.2GHz 을 기준으로 ±9.25%이고, 중심 주파수와 1.1V 공급 전압에서 26.4mW 의 전력을 소모하고, phase noise 가 1MHz 오프셋에서 -104.86dBc/Hz 임을 확인할 수 있었다.

주요어 : PLL, LC VCO, 소수 카운터, 프로그램 가능한 divider, 클락 버퍼, DDR5, Systemverilog

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