Ph.D. Dissertation

A Low-Power Digital Capacitive MEMS Microphone Based on a Triple-Sampling Delta-Sigma ADC with Embedded Gain

3중 샘플링 방식 델타-시그마 ADC를 이용한 디지털 Capacitive MEMS 마이크로폰

by
Byunggyu Lee

August 2022

Department of Electrical and
Computer Engineering
College of Engineering
Seoul National University

A Low-Power Digital Capacitive MEMS Microphone Based on a Triple-Sampling Delta-Sigma ADC with Embedded Gain

이득이 내장된 3중 샘플링 방식 델타-시그마 ADC를 기반으로 하는 저전력 디지털 Capacitive MEMS 마이크로폰

지도교수 김 수 환

이 논문을 공학박사 학위논문으로 제출함

2022 년 8 월

서울대학교 대학원

전기정보공학부

이 병 규

이병규의 공학박사 학위논문을 인준함

2022년 8 월

위 원 장 : 정 덕 균 (印)
부위원장 : 김 수 환 (印)
위 원 : 김 재 하 (印)
위 원 : 최 우 석 (印)
위 원 : 채 주 형 (印)

ABSTRACT

A LOW-POWER DIGITAL CAPACITIVE MEMS MICROPHONE BASED ON A TRIPLE-SAMPLING DELTA-SIGMA ADC WITH EMBEDDED GAIN

BYUNGGYU LEE
DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

A triple-sampling ΔΣ ADC can replace the programmable-gain amplifier commonly used in the readout circuit for a digital capacitive MEMS microphone. The input voltage can then be multiplied by subtracting a further half-period delayed differential input and using the feedback capacitor of the DAC as a sampling capacitor. This triple-sampling technique results in a readout circuit with sensitivity and noise performance comparable to recent designs, but with a reduced power requirement. CMRR improvement is achieved by subtracting differential inputs and superior noise performance compare to conventional structure, as amplifier noise and DAC kT/C noise is not amplified by triple-sampling structure while the signal is increased by its gain. Triple-sampling also can be operated as a single-to-differential circuit. A MEMS microphone incorporating this readout circuit,

fabricated in a 0.18μm CMOS process, achieved an A-weighted SNR of 62.1 dBA at 94 dB SPL with 520 μA current consumption, to which triple-sampling was shown to contribute 4.5 dBA.

Keywords : A digital capacitive MEMS microphone, gain-embedded ADC, delta-sigma ADC, without PGA, read-out circuit, low-power circuits.

Student Number : 2017-30933

CONTENTS

LIST OF FIGURES

LIST OF TABLE

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

1.1.1 MEMS MICROPHONE TRENDS

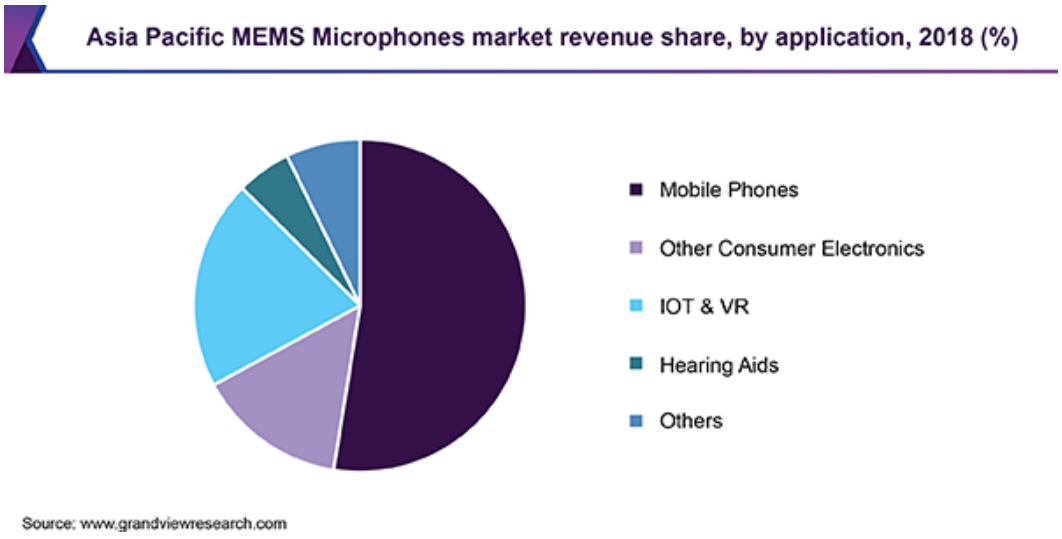


Figure 1.1.1.1 MEMS Microphones market revenue share

Microphones are ubiquitous in daily life such as smartphones and tablet PCs and are widely used in automobiles and medical devices. In Figure 1.1.1.1, more than 50% of the market revenue share is mobile devices and electronics and Internet of Things(IoT), Virtual Reality (VR) and hearing aids are also a part of it. More than 2 billion microphones are manufactured for various applications. Electret Condenser Microphones (ECMs) dominated the market share since 2005, but Micro Electromechanical System (MEMS) overtakes the market share and leads since 2016 according to Figure 1.1.1.2. A MEMS microphone is easier to integrate, more predictable, and smaller than ECM-type microphones [1.1.1], [1.1.2].

MEMS can be largely divided into capacitive type and piezoelectric type in terms of

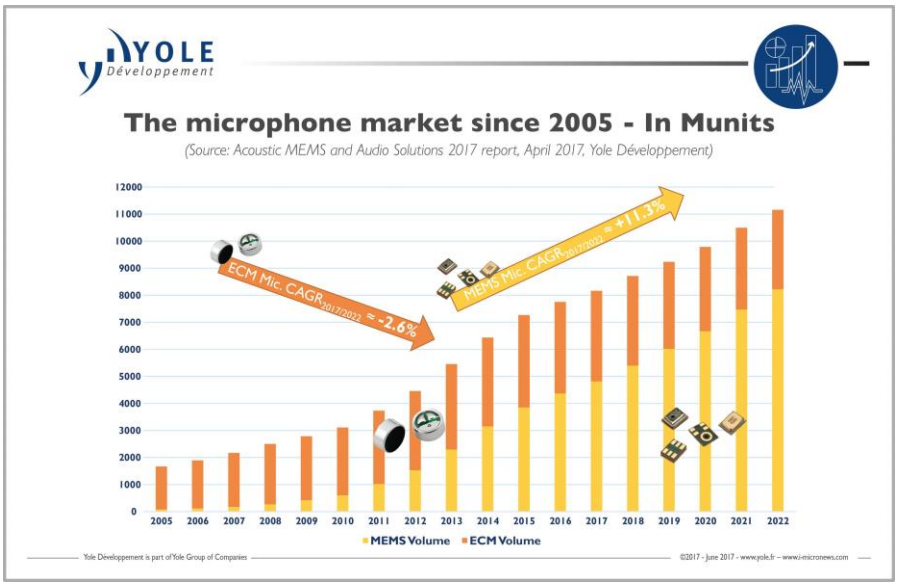


Figure 1.1.1.2 Market trends for ECM and MEMS microphone (Source : Yole Development)

operation method, and also divided into single-ended and differential type according to the type of output signal. First of all, the capacitive type is fixed with a back plate and a flexible diaphragm that fluctuates according to pressure, and this diaphragm is moved by sound pressure. When the sound pressure changes, a change in capacitance occurs between the diaphragm and the back plate, and an electrode attached to each is connected to a readout circuit and detects this change to detect an acoustic signal.

1.1.2 TYPE OF MEMS MICROPHONES

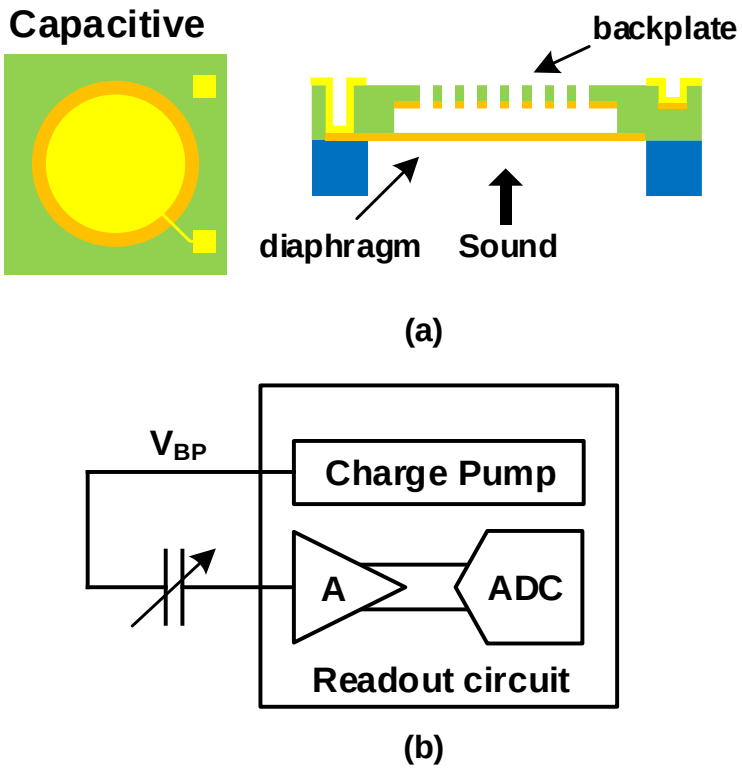


Figure 1.1.22.1. (a) Capacitive MEMS transducer structure (b) Block diagram for the connection between capacitive MEMS transducer and readout circuit.

A piezoelectric MEMS transducer consists of a moving plate made of piezoelectric material. The moving plate of the piezoelectric MEMS transducer is bent due to the incoming pressure. Mechanical stress is applied to a moving plate made of a piezoelectric material to generate an electric charge. Unlike capacitive MEMS transducers, piezoelectric MEMS transducers use the piezoelectric effect, so they are resistant to dust and liquids. It does not require high bias voltage unlike capacitive type MEMS transducer so the charge-

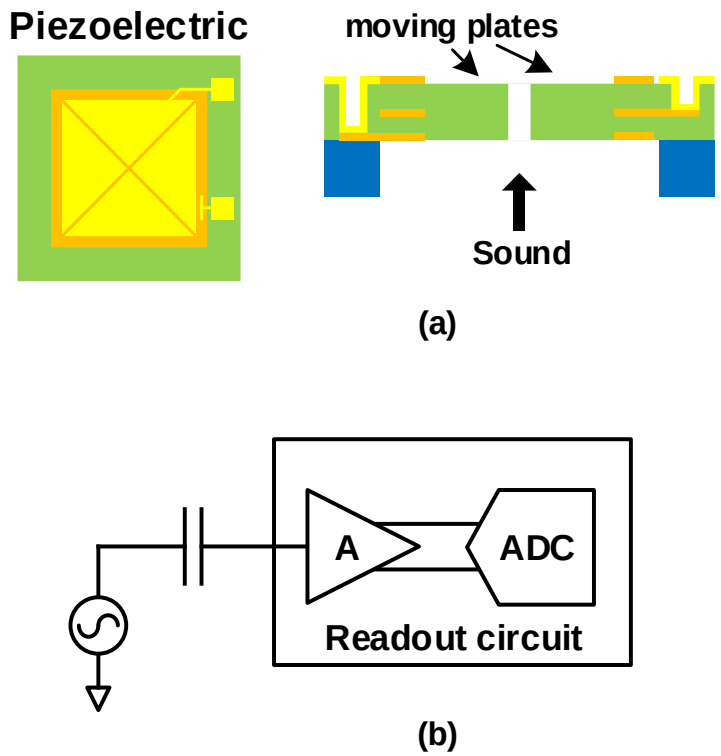


Figure 1.2.2.1 (a) Piezoelectric MEMS transducer structure (b) Block diagram for the connection between piezoelectric MEMS transducer and readout circuit.

pump is unnecessary. However, the many advantages of piezoelectric MEMS transducers over capacitive MEMS transducers, capacitive MEMS microphones are preferred over piezoelectric MEMS microphones due to their low noise performance, higher sensitivity, and flatter frequency response [1.1.3].

A MEMS microphone with a differential MEMS transducer, which offers a greater dynamic range by canceling out common-mode noise and even-order harmonic distortion. The differential type MEMS transducer offers both capacitive and piezoelectric MEMS transducers, but tends to be more expensive than a single-ended MEMS transducer because of their fabrication difficulty. [1.1.4]. Therefore, they are only used in products with the high-performance.

1.1.3 PREVIOUS WORKS

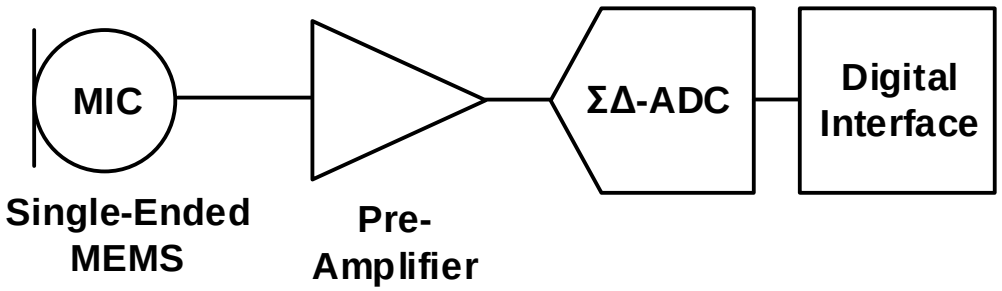


Figure 1.1.31 Conventional structure for digital MEMS microphone

Noise and sensitivity are huge challenges in MEMS microphone design and high sensitivity is achieved through the following four factors. Higher DC bias voltages, smaller parasitic capacitances, larger MEMS capacitance fluctuations, and pre-amplified gain are required for improved sensitivity. [1.1.5-1.1.7] However, increasing the MEMS DC bias voltage of the charge pump which drives the transducer decreases the distortion performance, and it is impossible to increase it indefinitely, while the MEMS transducer capacitance variance and the parasitic capacitance are beyond the control of the circuit designer of the readout integrated circuit(ROIC). As in Figure 1.1.3.1, introducing a pre-amplifier before the ADC is a simple way of increasing sensitivity but a pre-amplifier

requires additional power and noise budget [1.1.5]. A programmable gain embedded ΔΣ ADC can reduce the power drawn by the pre-amplifier and the amount of noise that it produces, but this type of ADC requires additional sampling capacitors and driving capabilities [1.1.8].

A MEMS microphone with a differential MEMS transducer introduces greater dynamic range and noise performance, but it is rather more expensive than a single-ended MEMS transducer and harder to fabricate [1.1.4].

Our design uses a triple-sampling ΔΣ ADC which is efficient in its requirement for capacitors and other components without changing any timing of the sampling and integrating phase. Also, in combination with existing methods, this triple-sampling ADC has an embedded gain of any rational numbers so that PGA is removable.

1.2 MEMS MICROPHONE BASIC TERMS

To explain the MEMS microphone, we must first understand the unit of sound pressure. The unit for expressing sound pressure is dBSPL (dB sound pressure level), and 94 dBSPL is equivalent to 1 Pa. In other words, Sound pressure level is a measurement of sound pressure that uses Pascals as its unit of measurement. Mics are rated by their sensitivity. This refers to the output voltage a microphone generates at a given sound pressure level (SPL). The standard "reference" SPL is a 1,000Hz tone at 94 dB-SPL at the mic capsule. Therefore, a microphone's sensitivity is expressed as the mic's output voltage when the mic capsule is presented with a 1,000Hz tone at 94 dB-SPL.

For analog microphones, the output signal is analog and therefore expressed in dBV. In the case of digital microphones, the analog signal is converted to digital because the ADC is built into the MIC and therefore expressed in dBFS (dB full scale). The maximum value that can be expressed in digital code corresponds to 0dBFS. dBFS is a relative unit that depends on the correlation between the analog voltage and the digital output code.

Sensitivity is defined as the magnitude of the output at 1Pa (94dBSPL). As explained in the previous paragraph, sensitivity is accordingly defined as dBV/Pa for analog MEMS

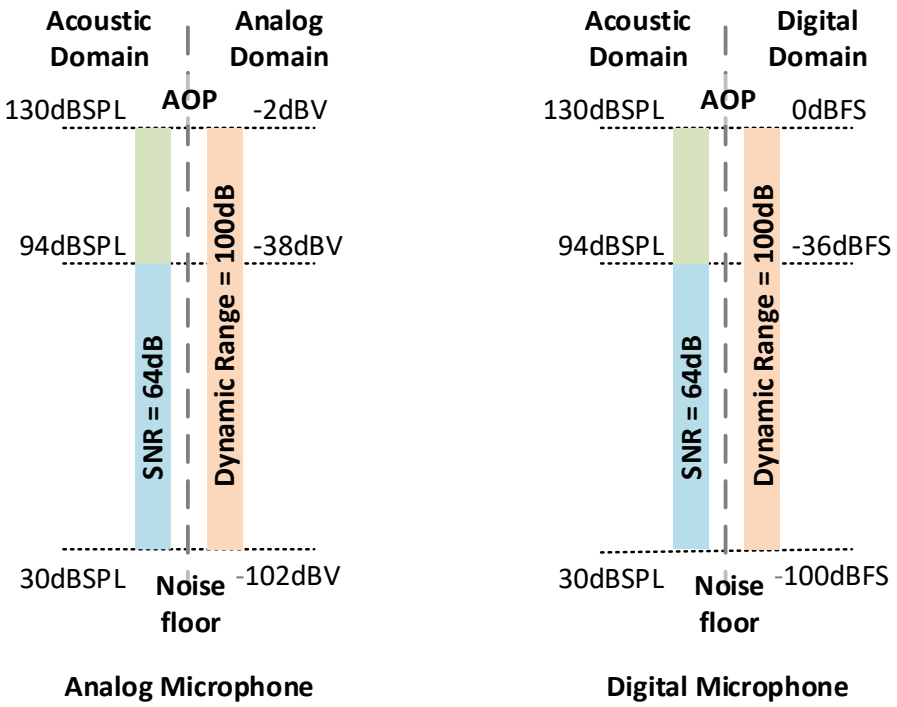


Figure 1.2.1. Example of analog and digital microphone specification.

and dBFS/Pa for digital MEMS. It is well represented in Figure 1.2.1. The noise floor is defined as the power of the output signal due to the noise of the microphone itself in the absence of an input signal. Normally, the noise floor of a mic applies an A-weighting filter that corresponds to the frequency response of the human ear, and the A-weighting filter has a magnitude of 0dB at several tens of kHz and has a minimum value at both ends of the audio bandwidth. The SNR of a microphone is defined as the sensitivity minus the noise floor, and in Figure 1.2.1, the SNR of the analog and digital microphones is 64dB. [1.2.1]

THD is defined as the sum of harmonic distortion compared to the output signal. This

means that the sum of 1% harmonic distortion equals 1% of the signal amplitude. Both the distortion characteristics of the ROIC itself and the distortion characteristics of the microphone have an effect, especially the microphone characteristic.

AOP represents the maximum sound pressure a microphone can record without distortion and defines the sound pressure level at which a microphone reaches 10% THD.

1.3 THESIS ORGANIZATION

This thesis is structured as follows. Chapter II presents overall system architecture. Chapter III introduces interface circuits and power management circuits. In Chapter IV we present the triple-sampling delta-sigma ADC and in Chapter V we present experimental results and we draw conclusions in Section VI.

CHAPTER 2

SYSTEM OVERVIEW

2.1 SYSTEM ARCHITECTURE

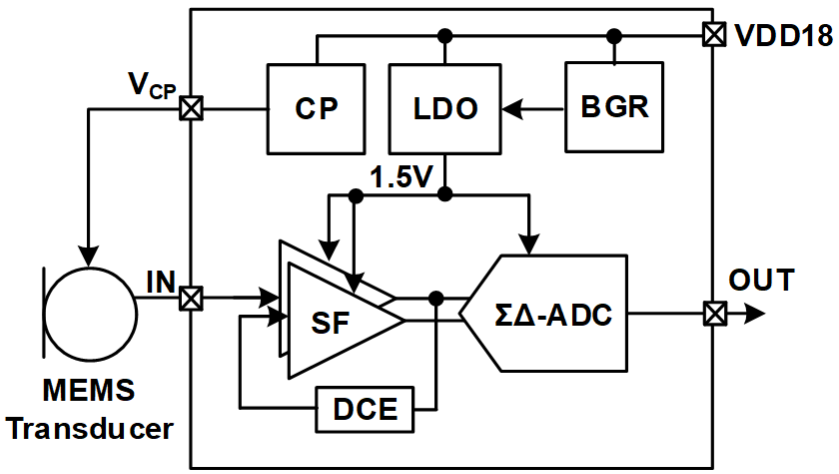


Figure 2.1 Structure of our MEMS microphone, showing the transducer and readout circuit

Figure 2.1 shows the structure of our MEMS microphone. It includes the microphone interface (pseudo-differential SFs) a ΔΣ ADC, low-dropout regulators (LDO), a bandgap reference (BGR), and a charge pump.

The signal transmitted from the MEMS transducer is buffered by the pseudo-differential source follower, converted from a single signal to a differential signal by the DC extractor, and transferred to the ADC [2.1.1]. The DC extractor (DCE) extracts the DC component from the output terminal of the SFs and feedbacks to the front-end of the SF, thereby making the input DC transmitted from the MEMS transducer and the DC part of the pseudo-differential SF the same. Our MEMS microphone used capacitive type MEMS transducer, which requires bias voltage is biased by charge-pump.

The delta-sigma ADC is optimal solution for audio application as it requires high resolution at the bandwidth of audible frequency [2.1.1]. A triple-sampling delta-sigma ADC converts analog signals from SF to digital signals. Our ADC has a 4^{th}-order cascaded integrator feedforward(CIFF) structure. The ADC has 13-level quantizers and an oversampling ratio of 64 to achieve target Signal-to-Quantization Noise Ratio (SQNR). The gain was obtained by triple-sampling 1^{st}-integrator by subtracting half-period delayed input and adding itself using DAC feedback capacitor. Also, triple-sampling integrator combined with the existing idea, the gain of ADC is adjustable from 1 to 4 in 0.5 increments, and the default setting is 4 according to dynamic range limitation. The slew-rate enhanced technique is also adopted in delta-sigma ADC.

The BGR produces a reference voltage independent of temperature. The LDO which adaptively changes pass transistor width size and quiescent current when output voltage and load current varies. It receives the reference voltage from the BGR and supplies it from 1.8V to 1.5V.

CHAPTER 3

INTERFACE CIRCUITS AND POWER MANAGEMENT CIRCUITS

3

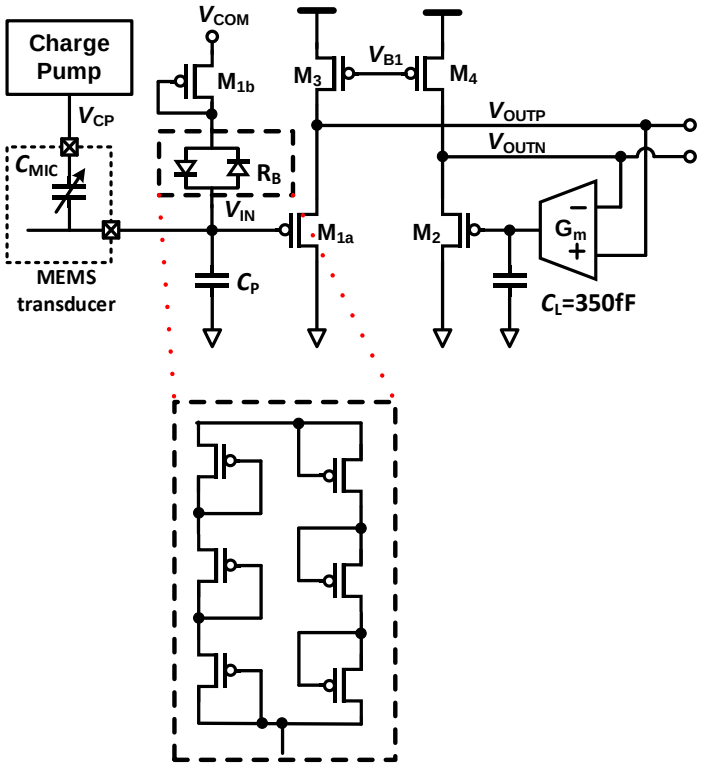


Figure 3.1.1 Pseudo-differential source follower schematic

3.1 PSEUDO-DIFFERENTIAL SOURCE FOLLOWER

Source followers are widely used as MEMS readout interfaces due to their high input impedance and driving capacity. Figure 3.1.1 shows the circuit diagram of the source follower (SF). The source follower buffers the output signal from the MEMS transducer and drives the input sampling capacitor stage of the ΔΣ ADC. It also applies a DC bias voltage to the signal transmitted from the MEMS transducer and shifts its level to the common-mode voltage. Source followers are widely used in MEMS transducer ROIC because of their high input impedance and low output impedance, together with a wide dynamic range and a high acoustic overload point (AOP). Since the DC component of the SF output voltage can be affected by the process variations, this voltage is compensated by the circuit shown in Figure 3.1.1. The compensation circuit modifies the common-mode voltage generated from the bandgap reference by supplying it with a bias current that is proportional to M_{1a} and M_{1b}. The input bias voltage is set by the back-to-back diodes R_b,

Figure 3.1.2 shows the schematic of the DC extractor. It is based on mirrored amplifier structure. The functionality of a DC extractor (DCE) is provided by a Gm-C filter which has a long output transistor to minimize its output capacitance. The ratio of M_{2a} and M_{3a}, M_{2b}, and M_{3b} is set to 10:1 and 21:1 respectively, thus the DCE does not affect the audio bandwidth and reduces the current consumption of DC extractor. In other words, by reducing the bias current of output of DC extractor, output resistance becomes very large, and thereby reduces the output required capacitance of DC extractor so that unity-gain

bandwidth of Gm-C filter is set to be less than audio bandwidth, which is 20Hz to 20kHz.

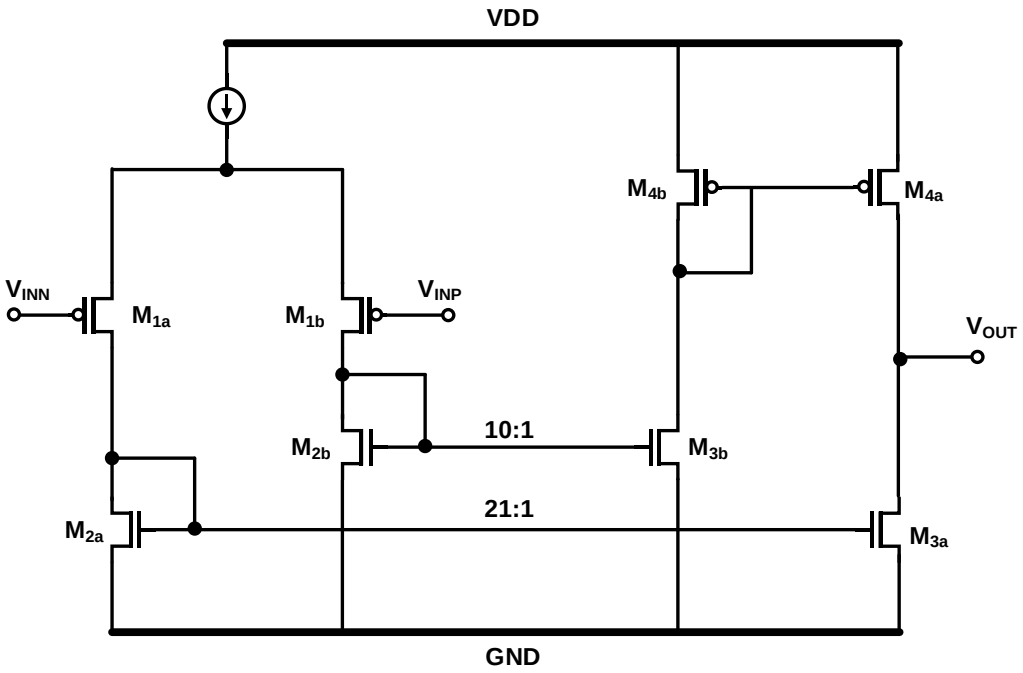


Figure 3.1.2 DCE schematic

3.2 CHARGE PUMP

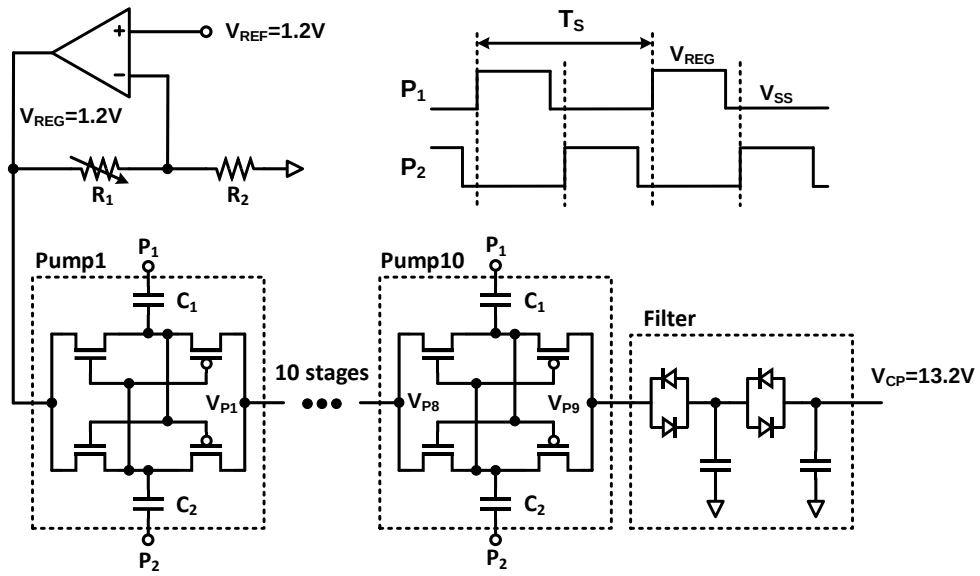


Figure 3.2.1 Schematic of charge pump.

The charge pump is a circuit for supplying high bias voltage to the capacitive MEMS transducer and is designed in a conventional structure. [3.2.1]. It is composed of a regulator 10 pump cell and RC filter as shown in Figure 3.2.1. The charge pump receives the reference voltage (1.2V) from the BGR and pumps it. This is done using a non-overlapping

clock. In P_1, the charge is stored in C_2, and the charge stored in C_1 is transferred to the output. In P_2, the charge is stored in C_1 and transferred by pumping the charge stored in C_2 to the output. Finally, at the end of the pump cell, the voltage is boosted as much as the reference voltage (1.2V) × the number of pump cells to output the final voltage. The low-pass filter consists of a passive RC filter, and frequencies above 20Hz must be filtered so as not to affect the audio bandwidth. However, in order to locate a large-size resistor to accomplish the above condition in the high voltage region, the resistor is configured in a back-to-back diode structure. The back-to-back diode structure occurs voltage to be degraded than we designed. Therefore, it is necessary to design a voltage higher than the actually desired voltage at the time of initial design. In the case of our charge pump, the actual goal was to output a voltage of 8 V to 11 V, but in simulation, it was designed to output a voltage of 13.2 V. The output of the charge pump is designed to be adjustable from 9 V to 13.2 V by adjusting V_{REG}, and it can be used to tune the appropriate charge pump voltage. ripple-removed DC voltage becomes the final output (V_{CP}). The output voltage of the charge pump is adjustable from 9 V to 13 V by controlling V_{REG} [1.2.1]. As shown in Figure 3.2.2, charge pump out voltage is smaller than 13.2V which is designed output voltage.

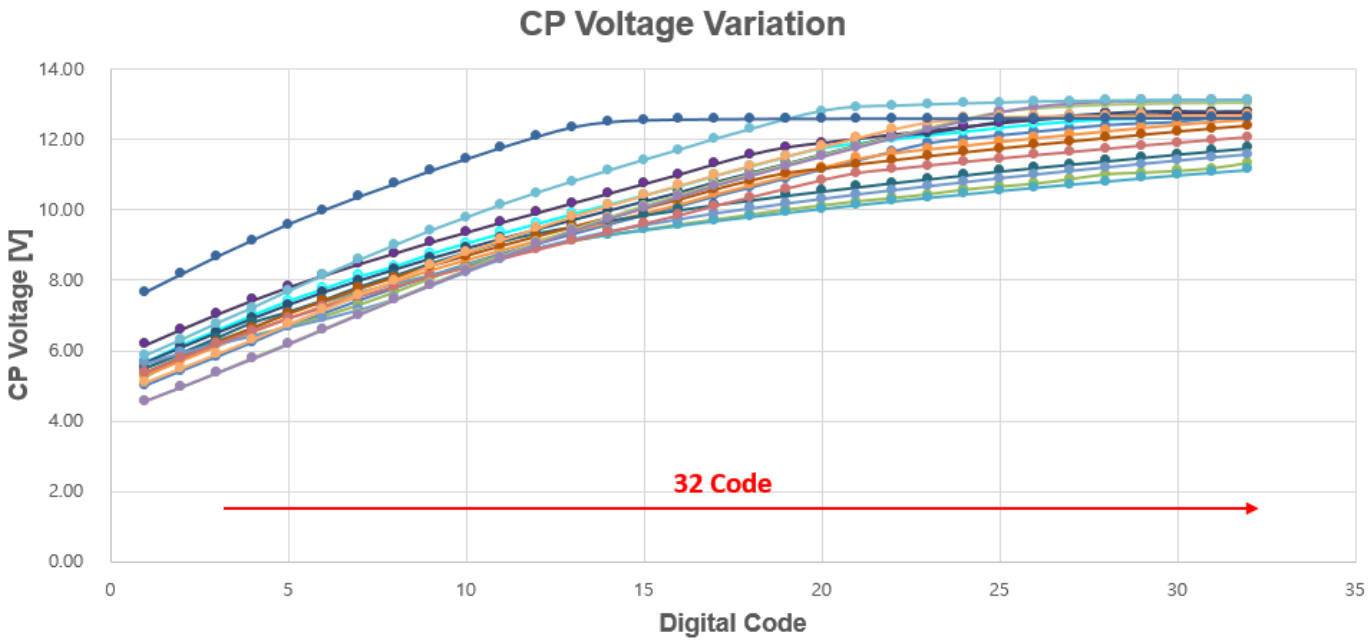


Figure 3.2.2 Measured output voltage of the charge pump on different samples.

3.3 LOW DROPOUT REGULATOR

3.3.1 DESIGN CONSIDERATION OF LOW DROPOUT REGULATOR

A typical LDO normally requires an external capacitor to have acceptable transient response, power supply noise rejection and stability of the LDO. The external capacitors

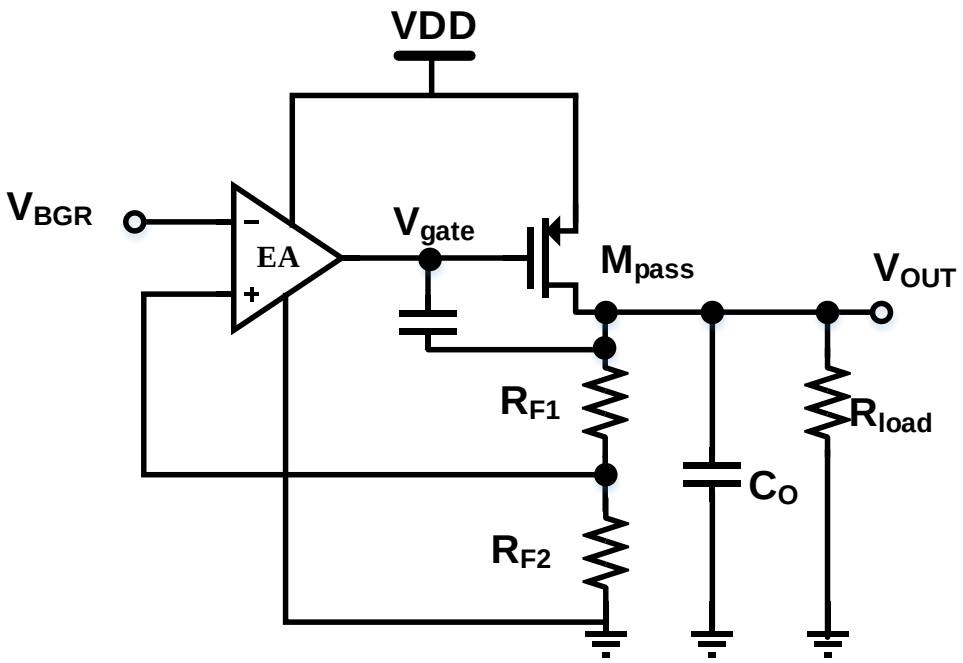


Figure 3.3.1.1 Conventional schematic of miller compensated LDO

occupy valuable board space and consumes pins in chips. Therefore, cap-less LDO is preferred over external cap type LDO as cap-less LDO does not use external capacitor. In

cap-less LDO, output capacitor which is less than few hundred pF is used for integration on chip. However, the conventional off-chip capacitor LDO depends heavily on the external capacitor for its stability and performance. Therefore, designing cap-less LDO requires stability, current and noise analysis.

It can be seen that there are two poles in the LDO circuit. At the output terminal of the error amplifier, the pole meets the gate capacitance of the pass transistor, and at the LDO output terminal, it is the pole formed by the parallel sum of the external capacitance and the pass transistor resistance and the resistance of the load.

In general, a transistor having a relatively large size is selected for passing a large amount of load current as the pass transistor, and accordingly, gate capacitance increases. A large value of the gain of the error amplifier is also selected to satisfy the target line voltage change rate/load current change rate, and accordingly, the output resistance of the error amplifier also increases. However, to attenuate output ripples, usually few hundreds of output capacitors is located at LDO output. Accordingly, the pole at the output stage of the error amplifier should be positioned sufficiently smaller than the unity gain frequency.

The pole of the LDO output stage is not a fixed value, but a pole that can be changed at any time by the load current, because the resistance of the pass transistor changes according to the load current. This is because, since the input voltage and output voltage are fixed, when the minimum load current flows, the resistance of the pass transistor increases and

the 2nd-pole becomes small. Therefore, when the minimum current that the LDO can drive flows through the load, it is located in the lowest frequency band. On the other hand, if the resistance of the output stage is changed, not only the 2nd-pole but also the loop gain will change, so this should be carefully considered.

In addition, when the output voltage is changed, the transconductance value of the pass transistor and the resistance value of the pass transistor are changed due to the change in the dropout voltage, so stability must be considered depending on the output voltage.

When the output voltage is minimum, the dropout voltage is maximum, and accordingly, the pass transistor resistance is increased and the 2nd-pole is decreased. As the transconductance value increases, the loop gain increases accordingly, thereby affecting the phase margin.

Since the gain of the error amplifier is large enough, the noise of the pass transistor is ignored. In order to minimize noise, a small feedback resistor should be used, but this means an increase in standby current, which means an increase in power consumption. Also, if the feedback resistance is not small enough, it will affect the 2nd-pole of the LDO output stage, so it should be set in consideration of this.

Our LDO feedback resistor that is about 500 times larger than the pass transistor resistance when the maximum driving current flows through the LDO is used. In addition, in order to reduce the flicker noise of the error amplifier, it is necessary to make the input

transistor of the error amplifier sufficiently large. Noise generated by the reference voltage amplifier can be partially offset by a low-frequency filter.

3.3.2 IMPLEMENTATION OF LOW DROPOUT REGULATOR

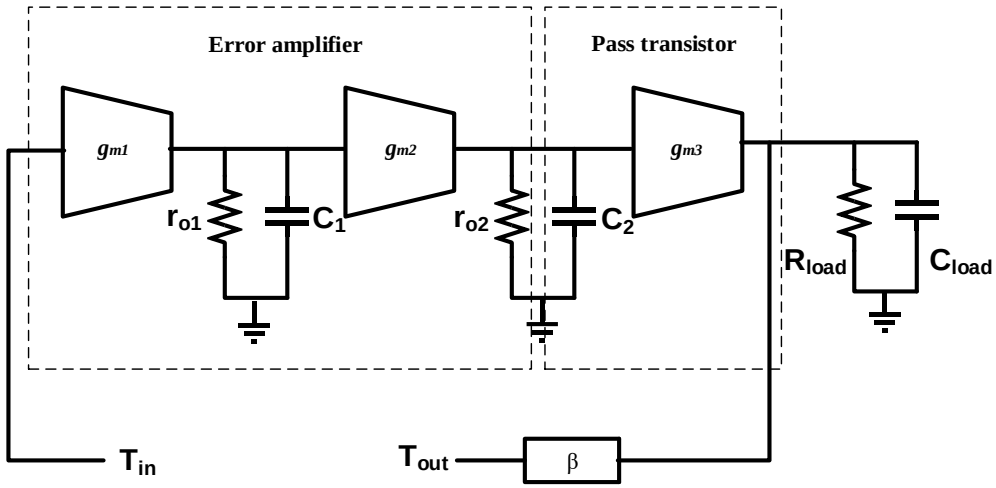


Figure 3.3.2.1 Small-signal model of LDO

The stability of the LDO loop can be analyzed by the following transfer function. Fig. 3.3.2 shows the small-signal model of LDO. Transfer function of LDO is expressed as

$$T_s = \frac{-\beta g_{m1} g_{m2} g_{mp} r_{o1} r_{o2} R_{load}}{(1+sC_{load}R_{load})(1+sC_1 r_{o1})(1+sC_2 r_{o2})} \quad (3.4.2.1)$$

where g_{m1}, g_{m2}, g_{mp} is the transconductance of error amplifier 1st, 2nd stage and pass transistor respectively, β is feedback factor consisting of the feedback resistor and C_{load}

and R_{load} are capacitor and resistor seen from output.

Since the pole generated at the output stage of the first stage of the error amplifier is negligible at a relatively high frequency, the LDO transfer function within the entire range of current that can be passed can be expressed as follows.

$$T_s = \frac{-g_{m1}g_{m2}g_{mp}r_{o1}r_{o2}R_{load}}{(1+sC_{load}R_{load})(1+sC_2r_{o2})} \quad (3.4.2.2)$$

Phase margin can be expressed as

$$\text{PM} \fallingdotseq 90 - \arctan\frac{w_u}{p_{2nd}} \quad (3.4.2.3)$$

Where w_u is unity gain frequency and $p_{2nd} = \frac{1}{R_{out}C_{load}}$

Phase margin from Equation (3.4.2.3) must greater than $30°$ at every corner cases.

However, Equation (3.4.2.3) is varies depends on load current and output voltage of LDO. Output voltage of LDO is controlled by feedback resistor, but if the output voltage is adjusted simply by changing the feedback resistance, the loop stability may be affected. This is because of a change in the transconductance of the pass transistor and a change in the resistance of the pass transistor according to a change in the dropout voltage. If the transconductance increases as the dropout voltage decreases, it is directly related to the

loop stability, and furthermore, the resistance of the pass transistor decreases as the LDO output voltage increases. Taking this into account, the position of the lowest 2nd-pole can be expressed as follows.

$$p_{2nd} = \frac{1}{(r_{ds}//R_{load})C_{\text{load}}} = \frac{1}{(\frac{V_{in}-V_{out}}{I_{load.min}}//\frac{V_{out}}{I_{load.min}})C_{\text{load}}} \quad (3.4.2.4)$$

Where $I_{load.min}$ is the minimum load current.

Therefore, it can be seen that appropriate size adjustment of the pass transistor to have an appropriate level of phase margin and current driving force is necessary for efficient power consumption. Also, load current affects the stability of the LDO by modifying r_{load} in Equation 3.4.2.2, it should be also considered in designing LDO. Introducing a quiescent current source at the output node is a solution for stability variance depending on load current. Then, output load resistance becomes

$$R'_{load} = R_{load}//R_{quiescent} \quad (3.4.2.5)$$

As a result, by adjusting $R_{quiescent}$ depends on load current, enough phase margin is achieved. In miller-compensated cap-less LDO, lowest load current causes worst stability, smaller enough $R_{quiescent}$ is required for stable operation. However, introducing a current source at an output stage of LDO requires static current consumption. Thus, adaptively

changes $R_{quiescent}$ is required for current efficiency.

Figure 3.3.3 shows the overall LDO circuit implementation including adaptively changes pass transistor width size and quiescent current source for current optimization and stable operation.

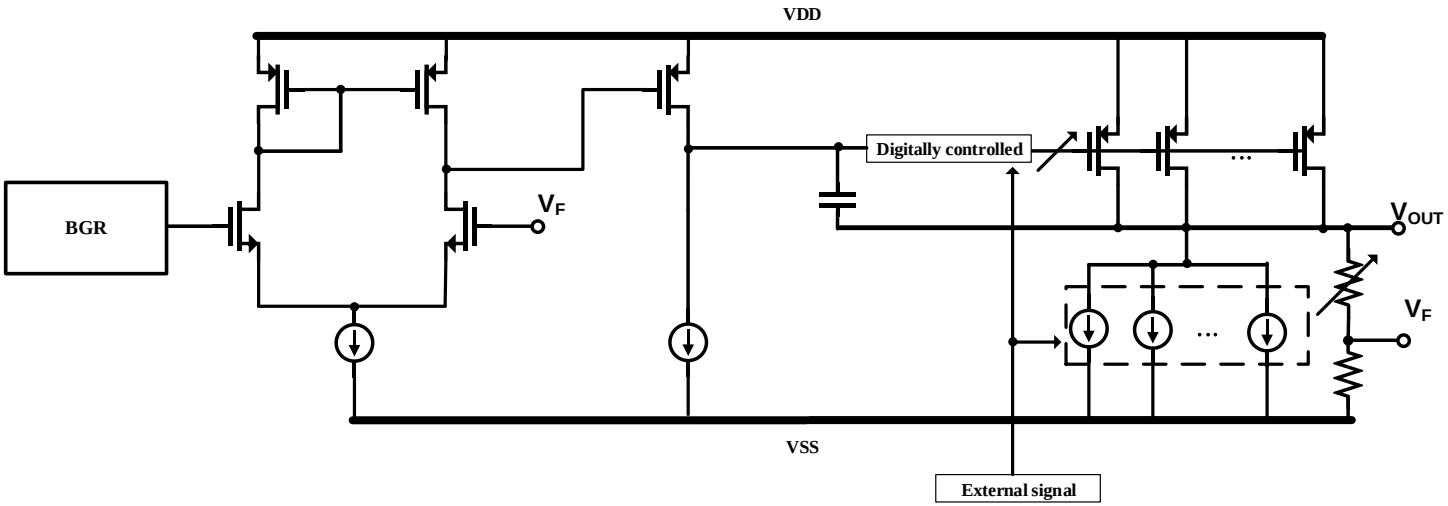


Figure 3.3.2.2 Overall LDO schematic

CHAPTER 4

TRIPLE-SAMPLING DELTA-SIGMA ADC

4.1 BASIC OF DELTA-SIGMA ADC

The delta-sigma ADC (ΣΔ ADC) offers high resolution and low noise by using noise shaping and oversampling making them a good ADC choice for many applications such as precision DC measurements, process control and especially in audio application. The ΣΔ ADC is composed of a delta-sigma modulator (ΣΔM) and a decimator as shown in Figure 4.1.1. A loop filter (H(z)), a quantizer (ADC), and a digital-to-analog converter (DAC) form a feedback loop. The main purpose of ΣΔM is to shape quantization noise. Figure 4.1.2 illustrates how the ΣΔ ADC operates in the frequency domain. The delta-sigma ADC, also called the oversampling ADC, samples faster than the Nyquist rate which is called oversampling. The half of the sampling frequency (F_S) is much higher than the signal bandwidth (F_B), and its ratio is defined as the oversampling ratio. Assume that quantization noise is white noise and is evenly distributed over all frequency bands. Oversampling evenly distributes quantization noise to the sampling frequency (F_S), reducing in-band quantization noise. The quantization noise of the signal band is shifted to the high frequency

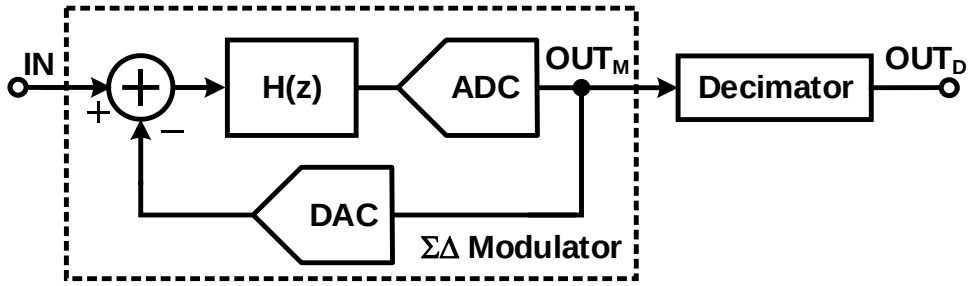


Figure 4.1.1 Block diagram of delta-sigma ADC.

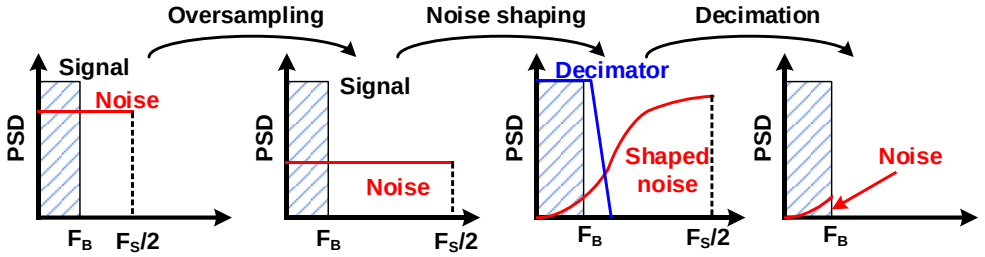


Figure 4.1.2 Operation of delta-sigma ADC in frequency domain.

region by noise shaping in ΣΔM. Only a few quantization noise remains in the signal band, and high resolution can be obtained. The high-frequency quantization noise is filtered out by a decimator which works as a low pass filter. The decimator also performs down-sampling to lower the data rate to the Nyquist rate.

We will now analyze operation of ΣΔ ADC through a quantitative approach. Figure 4.1.3 shows the ΣΔM as a linear model and quantization noise is modeled as E(z). The

transfer function from input and quantization noise to output is derived as follows.

$$Y(z) = V(z) + E(z) \tag{4.1.1}$$

$$V(z) = [U(z) + Y(z)]H(z) \tag{4.1.2}$$

$$Y(z) = \frac{H(z)}{1 + H(z)}U(z) + \frac{1}{1 + H(z)}E(z) \tag{4.1.3}$$

The transfer function from input to output is defined as signal transfer function (STF), and the transfer function from quantization noise to output is defined as noise transfer function (NTF). STF and NTF are expressed as follows.

$$STF(z) = \frac{H(z)}{1 + H(z)}, \qquad NTF(z) = \frac{1}{1 + H(z)}E(z) \tag{4.1.4}$$

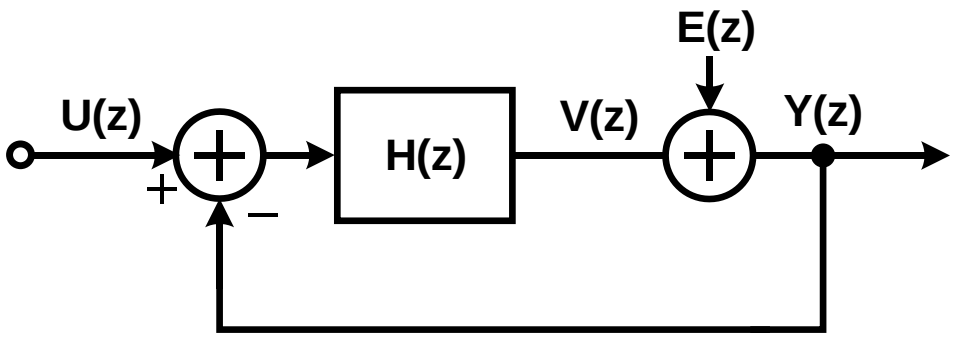


Figure 4.1.3. Linear model of delta-sigma modulator.

STF and NTF are determined by the transfer function H(z) of the loop filter. For proper operation of the ΣΔM, STF should be close to 1 and NTF close to 0 at low frequencies. Delaying or non-delaying integrator perfectly fits this conditions. Assume 1st-order DSM for simplicity and delaying integrator is used the derived NTF and STF a

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{4.1.5}$$

$$STF(z) = z^{-1}, \qquad NTF(z) = 1 - z^{-1} \tag{4.1.6}$$

At low frequencies (z=1), the magnitudes of STF and NTF are 1 and 0, respectively. The order of NTF follows the order of the loop filter H(z). That is, the effect of noise shaping increases as the higher order loop filter is used. Another factor that reduces quantization noise is the oversampling ratio (OSR). In Figure 4.1.2, as the OSR increases, the F_B moves toward the low frequency, which reduces the quantization noise. In addition, the quantizer noise itself can be reduced by using a high resolution quantizer. In summary, the factors affecting the signal-to-quantization noise ratio (SQNR) in ΣΔM are the order of the loop filter (L), OSR, and the number of quantizer resolution (N). The SQNR of ΣΔM can be derived as follows.

$$SQNR = 6.02 \cdot N + 1.76 + (2L + 1) \cdot 10 \cdot \log(OSR) \tag{4.1.7}$$

From Eq. (4.1.7), increasing L and OSR is more efficient than increasing N. However, a high OSR requires a high-speed clock, which increases the power consumption. Also, increasing L can make the modulator unstable. Therefore, the designer should find the optimal NFT by properly adjusting N, L, and OSR.

The in-band quantization noise power can be derived by using following equations.

$$S_e(f) = \frac{\Delta^2}{12 \cdot 2f_B \cdot OSR} = \frac{1\Delta^2}{12f_s} \tag{4.1.8}$$

$$z = e^{\frac{j2\pi f}{f_s}}. \tag{4.1.9}$$

$$|\mathrm{NTF}(z)|^2 = |1 - e^{-\frac{j2\pi f}{f_s}}|^2 = |2\sin(e^{-\frac{\pi f}{f_s}})|^2. \tag{4.1.10}$$

The in-band quantization noise-power is

$$\mathrm{P}\int_{-fB}^{fB} Se(f) \cdot |\mathrm{NTF}(z)|^2 d$$

$$= \frac{\Delta^2}{12}\frac{\pi^2}{3}\frac{8{f_B}^3}{{f_s}^3} = \frac{\Delta^2}{12}\frac{\pi^2}{3}\frac{1}{\mathrm{OSR}^3}. \tag{4.1.11}$$

.

(4.1.8) can be expanded for a L-th order modulator as follows

$$\mathrm{P}\int_{-fB}^{fB} Se(f)\cdot|\mathrm{NTF}(z)|^2 d$$

$$=\frac{\Delta^2}{12}\frac{\pi^{2L}}{2L+1}\frac{1}{\mathrm{OSR}^{2L+1}}. \quad (4.1.12)$$

Therefore**,** increasing order will be very effective for lowering quantization noise by trading-off stability and power consumption. Signal-to-quantization noise (SQNR) can be derived as

$$\mathrm{SQNR}=10\log(\frac{P_{signal}}{P_q})$$

$$=6.02\mathrm{N}+1.76-206.02\mathrm{N}+1.76-20\log\left(\frac{\pi^L}{\sqrt{2L+1}}\right)+(20L+10)\log(OSR) \quad (4.1.13)$$

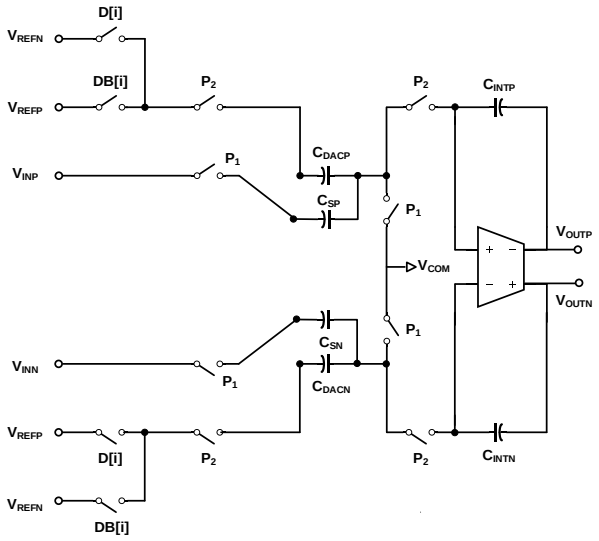
1.5-bit per octave can be increased if there is an increase in OSR.

4.2 IMPLEMENTATION OF TRIPLE-SAMPLING DELTA-SIGMA MODULATOR

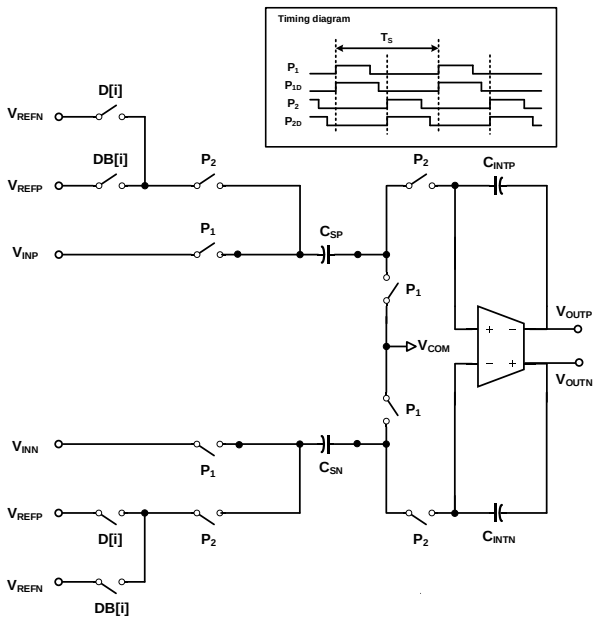
4.2.1 CONVENTIONAL 1ST INTEGRATOR STRUCTURE

Figure 4.2.1.1(a) and (b) show the conventional structure of a 1st integrator which are shared-capacitor DAC and a separate-capacitor DAC structure respectively. In this figure D[i] is one of the feedback signals from the DAC, V_{ref} is the reference voltage from the reference generator which is sampled to C_{DACP}, C_{DACN} at integrating phase P2. The differential input V_{INP} and V_{INN} are sampled by sampling capacitor C_{SP} and C_{SN} at sampling phase P1 respectively.

In the conventional method, the gain of a 1st integrator is unity, whether or not the capacitors are shared. The shared-capacitor method has an advantage in terms of kT/C thermal noise, but it limits the gain. In the separate-capacitor method, a gain can be applied by multiplying sampling capacitors C_{SP} and C_{SN} as shown in Figure 4.2.1.2 [4.2.2]. Separating the sampling capacitor and DAC feedback capacitors allows the signal transfer function(STF) to be changed without affecting the noise transfer function (NTF). Thus, the gain proportional to the multiplying factor can be achieved by introducing additional capacitors. However, assuming that the same capacitor is used in the shared-capacitor method, it is disadvantageous in terms of noise. Also, in the separate-capacitor structure, the sampling capacitor is not efficiently used at all in the integrating phase P2 as shown in Figure 4.2.1.2 as sampling capacitor is idle at P2 just resetting itself.



(a)



(b)

Figure 4.2.1.1(a) Conventional separate capacitor DAC structure and (b) shared capacitor DAC structure

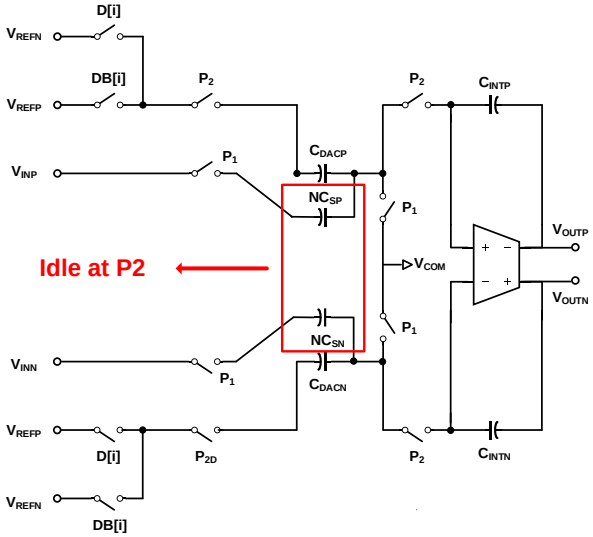


Figure 4.2.1.2. Conventional separate capacitor DAC structure with embedded gain

4.2.2 CROSS-SAMPLING 1ST INTEGRATOR

The proposed cross-sampling 1st integrator structure is shown in Figure 4.2.2.1. Through this circuit, the sampling capacitor is also used at P2. As a result, the voltage of the input signal is doubled by subtracting each complementary input from the corresponding signal. In other words, V_{INP} and V_{INN} are sampled in C_{SP} and C_{SN} at sampling phase P1 respectively, and then, V_{INP} and V_{INN} are also sampled in C_{SP} and C_{SN} at integrating phase P2 respectively. A sampling at P2 is subtracting from the value stored in the sampling capacitors. V_{OUTP} and V_{OUTN} are expressed as

$$\mathrm{V_{OUTP}} = \mathrm{a_1}(\mathrm{V_{INP}} - \mathrm{V_{DACP}} - \mathrm{V_{INN}}) \qquad (4.2.2.1)$$

$$\mathrm{V_{OUTN}} = \mathrm{a_1}(\mathrm{V_{INN}} - \mathrm{V_{DACN}} - \mathrm{V_{INN}}) \qquad (4.2.2.2)$$

where $\mathrm{a_1} = \frac{C_S}{C_{Int}}$, $\mathrm{V_{DAC}}$ DAC feedback voltage originated from BGR

Subtracting Equation 4.2.2.1 and 4.2.2.2 we obtain

$$\mathrm{V_{OUT.DIFF}} = \mathrm{a_1}(2\mathrm{V_{IN.DIFF}} - \mathrm{V_{DAC.DIFF}}) \qquad (4.2.2.2)$$

Since the signs of V_{INP} and V_{INN} are opposite, $2V_{INP}$ and $2V_{INN}$ are integrated through C_{SP} and C_{SN} respectively.

Also, the additional driving capability is unnecessary because it was made to use the sampling capacitor at P2. The common-mode rejection ratio (CMRR) of the proposed cross-sampling is improved by subtracting differential inputs in this way as we expected in differential circuit, reducing common-mode noise and even harmonic distortion. SNR performance can be improved by doubling the signal but the noise from DAC and amplifier are the same, without using additional sampling capacitors or timing.

Moreover, the cross-sampling structure can operate as a single-to-differential converter by adding a DC voltage to the V_{INN}. In this case, the gain is 1, or, strictly speaking, 2,

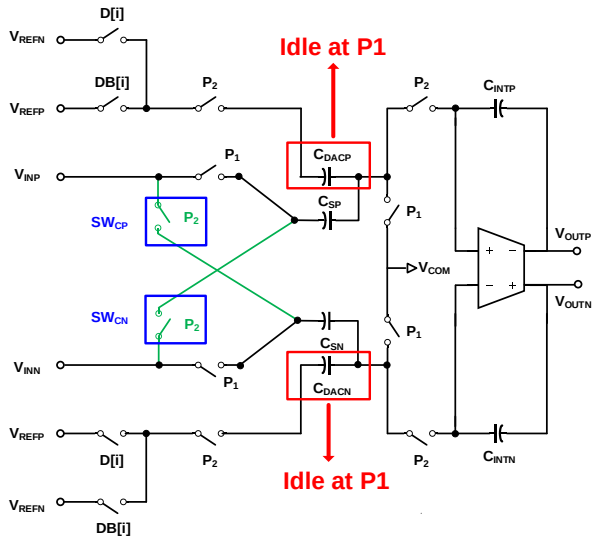


Figure 4.2.2.1. Cross-sampling structure 1st integrator

because of the differential input, but it can also obtain additional gain due to the method described later. However, the capacitor on the DAC side, which can be treated similarly, is idle during the sampling phase as shown in Figure 4.2.2.1.

4.2.3 TRIPLE-SAMPLING 1ST INTEGRATOR

By using the DAC feedback capacitor as the sampling capacitor in the sampling phase as shown in Figure 4.2.3.1, the effect of doubling the sampling cap can be achieved if we assume M=1. In other words, V_{INP} and V_{INN} are sampled to C_{DACP}, C_{DACN} at P1, $2V_{\mathrm{INP}}$, and $2V_{\mathrm{INN}}$ are integrated through C_{SP} and C_{SN} at P2 respectively as we already explained in Figure 4.2.2.1. V_{OUTP} and V_{OUTN} are expressed as

$$\mathrm{V_{OUTP}} = \mathrm{a_1}(2\mathrm{V_{INP}} - \mathrm{V_{DACP}} - \mathrm{V_{INN}}) \tag{4.2.3.1}$$

$$\mathrm{V_{OUTN}} = \mathrm{a_1}(2\mathrm{V_{INN}} - \mathrm{V_{DACN}} - \mathrm{V_{INN}}) \tag{4.2.3.2}$$

where $\mathrm{a_1} = \frac{C_s}{C_{Int}}$, $\mathrm{V_{DAC}}$ DAC feddback voltage originated from BGR

Subtracting Equation 4.2.3.1 and 4.2.3.2 we obtain

$$\mathrm{V_{OUT.DIFF}} = \mathrm{a_1}(3\mathrm{V_{IN.DIFF}} - \mathrm{V_{DAC.DIFF}}) \tag{4.2.3.2}$$

as a result, 3 times larger signal is sampled through this structure.

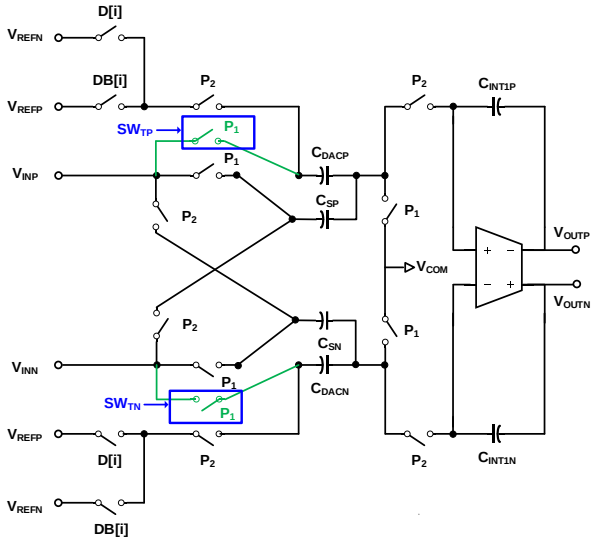


Figure 4.2.3.1 Triple-sampling structure 1st integrator

Figure 4.2.3.2 shows our final proposed 1st integrator circuit. Triple-sampling structure combined with Figure 4.2.1.2 we obtain triple-sampling 1st integrator with rational gain. From Figure 4.2.3.2 V_{OUTP} and V_{OUTN} are expressed as

$$\mathrm{V_{OUTP}} = \mathrm{a_1}(\mathrm{MV_{INP}} - \mathrm{V_{DACP}} - \mathrm{V_{INN}}) \tag{4.2.3.4}$$

$$\mathrm{V_{OUTN}} = \mathrm{a_1}(\mathrm{MV_{INN}} - \mathrm{V_{DACN}} - \mathrm{V_{INN}}) \tag{4.2.3.5}$$

where $\mathrm{a_1} = \frac{C_S}{C_{Int}}$, $\mathrm{V_{DAC}}$ DAC feddback voltage originated from BGR.

Subtracting Equation 4.2.3.4 and 4.2.3.5 we obtain

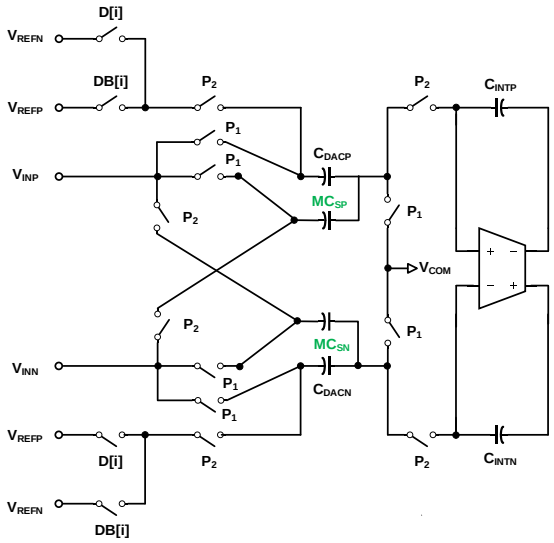


Figure 4.2.3.2 Triple-sampling structure with sampling capacitor multiplied by M

$$V_{OUT.DIFF} = a_1((2M+1)V_{IN.DIFF} - V_{DAC.DIFF}) \quad (4.2.3.6)$$

as a result, (2M+1) multiplied signal is achieved as shown in Equation 4.2.3.6

For convenience, as shown in Table 4.2.3.1, we will call the conventional separate-capacitor structure with a gain of 1 as case1, and the method in which the sampling capacitors and DAC capacitors are used in both sampling and integrating phases without modifying the sampling capacitor (M=1) with a gain of 3 as case3. If M is any rational value, non-integer gains can be achieved by changing the value of the sampling capacitor. In this case, V_{INP} and V_{INN} are sampled to C_{DACP}, C_{DACN} at P1, $2MV_{INP}$, and $2MV_{INN}$ are integrated through C_{SP} and C_{SN} at P2 respectively. As a result, a gain of

2M+1 can be achieved using the scheme shown in Figure 4.2.3.2 which is the case (2M+1).

However, in case (2M+1), more sampling capacitor is used in integrator compared to conventional separate capacitor DAC structure and shared capacitor DAC structure. This is not a fair comparison as kT/C thermal noise is dominated by sampling capacitor. Also, half-period delayed signal is not identical to its original input. Therefore, further analysis is required for triple-sampling 1st integrator structure. [4.2.3]

4.2.4 STF ANALYSIS OF TRIPLE-SAMPLING 1ST INTEGRATOR

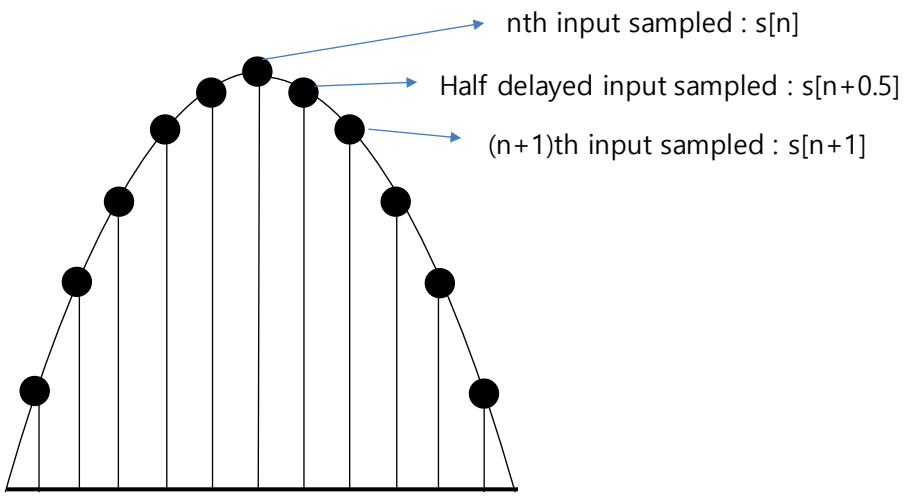


Figure 4.2.4.1 Difference of non-delayed input and half-delayed input

The triple-sampling 1st integrator increases gain, SNR. Further, it also operates as a single-to-differential circuit. However, as shown in Figure 4.2.4.1, when the cross-sampled input is sampled during the integration phase, it acquires a delay of half a period, which is expressed as $z^{-0.5}$ in Equation (4.3.4.1). Therefore, it cannot be said that the signal is the same as being multiplied by 2M. From a qualitative point of view, a half-period delayed signal can be considered negligible in an oversampling ADC, but a quantitative

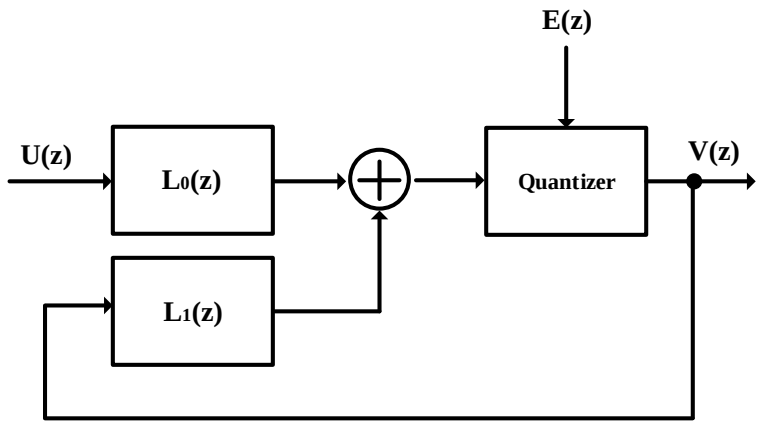


Figure 4.2.4.2 Block diagram of 1st-order delta-sigma modulator

analysis of the STF magnitude is additionally required.

Figure 4.3.4.1 is a block diagram of 1st-order DSM. The STF can be expressed as follows

$$\frac{L_0(z)}{1+L_1(z)} = (1+M)z^{-1} + Mz^{-0.5} \tag{4.3.4.1}$$

where $L_0(z) = \frac{z^{-1}(1+M+Mz^{0.5})}{1-z^{-1}}$, $L_1(z) = \frac{z^{-1}}{1-z^{-1}}$.

The NTF can be expressed as follows

$$\frac{1}{1+L_{1(z)}} = 1 - z^{-1}. \tag{4.3.4.2}$$

This expression is not affected by the gain, as the structure and timing of the DAC do not change. Therefore, we only need to consider the STF.

By applying an inverse z-transform to equation (4.3.4.1), we obtain

$$H_{\text{STF.2M+1}}(j\omega) = 2Me^{-\frac{3}{4}j\omega T}(\cos(\frac{wT}{4}))+e^{-j\omega T}. \quad (4.3.4.3)$$

Thus, the magnitude of the STF is

$$2M\left|\cos\left(\frac{\pi f}{2f_s}\right)\right| + 1 \quad (4.3.4.4)$$

Therefore, the signal will be most degraded when $f=f_{\text{in.max}}$ in Equation (4.3.4.4) which is expressed as

$$\min|H_{\text{STF.2M+1}}(j\omega)| = 2M\left|\cos\left(\frac{\pi f_{\text{in.max}}}{4OSRf_{\text{in.max}}}\right)\right| + 1 \quad (4.3.4.5)$$

where OSR is the oversampling ratio of ΔΣ ADC.

Assuming that $f_{\text{in.max}}$ is 20kHz, which is the fastest signal within the audio bandwidth, the signal magnitude, and signal loss, for oversampling ratio between 1 and 128 predicted by Equation (4.3.4.5) are given in Table 4.2.4.1. As OSR increases, the loss becomes smaller, as expected. An oversampling ratio of ΔΣ ADC is usually greater than 10, signal

degradation effects are negligible.

OSR	WORST SIGNAL MAGNITUDE	Worst Signal Loss
1	1.414214M+1	0.586M
4	1.961571M+1	3.84×10^{-2}M
16	1.997591M+1	2.41×10^{-3}M
64*	**1.999849M+1**	$\mathbf{1.51 \times 10^{-4}}$**M**
128	1.999962M+1	3.80×10^{-5}M

Table 4.2.4.1 The signal magnitude and worst signal loss for different oversampling ratio

4.2.5 THERMAL NOISE ANALYSIS OF TRIPLE-SAMPLING 1ST INTEGRATOR

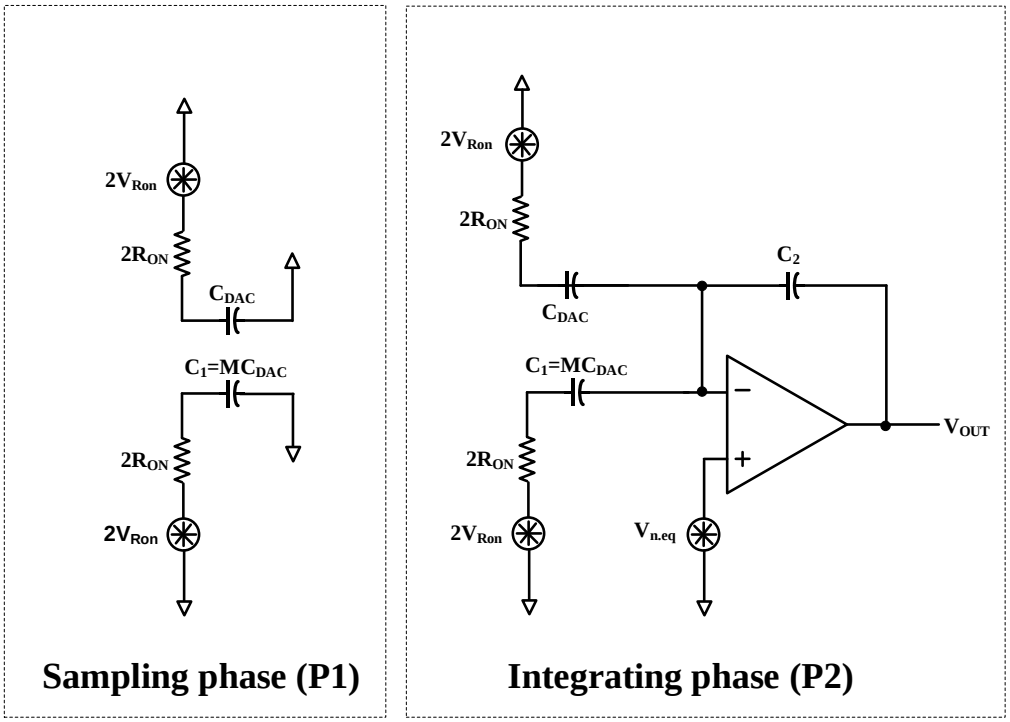


Figure 4.2.5.1 Detailed thermal noise of case(2M+1) 1st integrator

Figure 4.2.5.1 shows the thermal noise introduced by the triple-sampling integrator when the case (2M+1). For calculation simplicity, we assume the integrator is single-ended and the gain of the amplifier is large enough. Analyzing a 1st integrator's thermal noise is

acceptable because most of the noise produced by a high-order ΔΣ ADC comes from its 1st integrator. Then, output noise power during the sampling phase is expressed as

$$\overline{V_{\mathrm{p1}}^2} = \frac{MkT}{C_1}(1+M) \tag{4.3.5.1}$$

where $C_{\mathrm{DAC}} = C_2 = C_1/M$ and output noise power during the integrating phase is expressed as

$$\overline{V_{\mathrm{p2}}^2} = \frac{MkT}{C_1}\left(\frac{\frac{4}{3}n_{\mathrm{f}}(1+M)+2R_{\mathrm{ON}}g_{\mathrm{m}}(1+M)}{1+2R_{\mathrm{ON}}g_{\mathrm{m}}}\right) \tag{4.3.5.2}$$

where g_{m} is the transconductance of the amplifier and n_{f} is the noise factor of the amplifier.

Summing Equations (4.3.5.1) and (4.3.5.2), the total output noise power is expressed as

$$\overline{V_{\mathrm{total}}^2} = \overline{V_{\mathrm{p1}}^2} + \overline{V_{\mathrm{p2}}^2} = \frac{MkT}{C_1}\left(\frac{(\frac{4}{3}n_{\mathrm{f}}+1+2\mathrm{x})(1+M)}{1+x}\right) \tag{4.3.5.3}$$

where $x = 2R_{\mathrm{ON}}g_{\mathrm{m}}$.

The power of the signal is proportional to $(1+2M)^2$ and thus the SNR is expressed as follows

$$\mathrm{SNR}_{(2\mathrm{M}+1)} = \frac{\overline{V_{\mathrm{signal}}^2}}{\overline{V_{\mathrm{total}}^2}} = K_1\frac{C_1}{MkT}\frac{(1+x)(1+2M)^2}{(\frac{4}{3}n_{\mathrm{f}}+1+2\mathrm{x})(1+M)} \tag{4.3.5.4}$$

where K_1 is constant.

If a separate capacitor structure is being used, and the gain is 1, then the noise can be expressed as follows

$$\mathrm{SNR}_{\mathrm{sep}} = K_1 \frac{C_{1.\mathrm{sep}}}{2kT} \frac{1+x}{\frac{4}{3}n_{\mathrm{f}}+1+2\mathrm{x}}. \tag{4.3.5.5}$$

To compare the thermal noise, the size of the total capacitors C_{total} in each case is assumed to be the same. Thus,

$$C_1 = \frac{MC_{\mathrm{total}}}{(1+M)} \tag{4.3.5.6}$$

where $C_{\mathrm{total}} = C_1 + C_{\mathrm{DAC}} = (1 + 1/M)C_1$.

Using Equation (4.3.5.6), Equation (4.3.5.4) and Equation (4.3.5.5) are replaced to Equation (4.3.5.7) and Equation (4.3.5.8) respectively.

$$\mathrm{SNR}_{(2\mathrm{M}+1)} = K_1 \frac{C_{total}}{(1+M)kT} \left(\frac{(1+x)(1+2M)^2}{(\frac{4}{3}n_f+1+2\mathrm{x})(1+M)}\right) \tag{4.3.5.7}$$

$$\mathrm{SNR}_{sep} = K_1 \frac{C_{total}}{4kT} \left(\frac{1+x}{(\frac{4}{3}n_{\mathrm{f}}+1+2\mathrm{x})}\right) \tag{4.3.5.8}$$

To compare the SNRs of the two cases, dividing Equation (4.3.5.7) by Equation (4.3.5.8), we obtain

$$\frac{\mathrm{SNR}_{(2M+1)}}{\mathrm{SNR}_{\mathrm{sep}}} = \frac{4(1+2M)^2}{(1+M)^2} \tag{4.3.5.9}$$

The triple-sampling structure is SNR-wise superior to a separate capacitor structure. This is because only the signal magnitude is increased while the noise of the amplifier and the noise of the DAC remain the same.

If M=0, Equation (4.3.5.8) becomes

$$\mathrm{SNR}_1 = K_1 \frac{C_{\mathrm{total}}}{KT} \left(\frac{1+x}{\frac{4}{3}n_f+1+2x}\right). \tag{4.3.5.10}$$

Equation (4.3.5.10) is equation of SNR of shared-capacitor structure and it means that when M=0, the triple-sampling circuit becomes a shared-capacitor structure. This is because cross-sampling part is removed when M=0. From Equation (4.3.5.7), as M increases, the SNR increases. Therefore, maximum SNR is achieved when M goes to infinity. If M goes to infinity Equation (4.3.5.9) saturates to

$$\lim_{M\to\infty} \frac{\mathrm{SNR}_{(2M+1)}}{\mathrm{SNR}_{\mathrm{sep}}} = 16. \tag{4.3.5.11}$$

Practically, due to supply voltage and dynamic range limitation, the value of M is considered to lie between 1 and 4 depending on the application.

M	Signal Power $(1+2M)^2$	$SNR_{(2M+1)}/SNR_{sep}$
1	9 (9.54 dB)	9 (9.54 dB)
1.5*	16 (12.0 dB)	10.24 (10.10 dB)
2	25 (14.0 dB)	11.11 (10.46 dB)
10	441 (26.4 dB)	14.58 (11.63 dB)
100	40,401 (46.1 dB)	15.84 (12.00 dB)

Table 4.3.5.1 Signal power according to M and expected SNR improvement compared to separate cap DAC structure

Structure	Integrator Transfer function	NTF	STF		STF magnitude	
			Z form	S form(mag)	OSR=64	OSR=256
Conventional	$\frac{a_1 z^{-1}}{1-z^{-1}}$	$1-z^{-1}$	Z^{-1}	1	1	1
Case2'	$\frac{2a_1 z^{-1}}{1-z^{-1}}$	$1-z^{-1}$	$2Z^{-1}$	2	2	2
Case2	$\frac{a_1 z^{-1}(1+z^{\frac{1}{2}})}{1-z^{-1}}$	$1-z^{-1}$	$Z^{-1}+Z^{-\frac{1}{2}}$	$2\left\|cos\left(\frac{\pi}{4OSR}\right)\right\|$	1.9998	1.999991
Case3	$\frac{a_1 z^{-1}(2+1z^{\frac{1}{2}})}{1-z^{-1}}$	$1-z^{-1}$	$2Z^{-1}+Z^{-\frac{1}{2}}$	$1+2\left\|cos\left(\frac{\pi}{4OSR}\right)\right\|$	2.9998	2.999991
Case(2N+1)	$\frac{a_1 z^{-1}(1+N_1+N_2 z^{\frac{1}{2}})}{1-z^{-1}}$	$1-z^{-1}$	$(N+1)Z^{-1}+NZ^{-\frac{1}{2}}$	$1+2N\left\|cos\left(\frac{\pi}{4OSR}\right)\right\|$	1+1.9998N	1+1.999991N

Table 4.3.5.2 Summary of each case

4.3 CIRCUIT IMPLEMENTATION OF DELTA-SIGMA ADC

Figure 4.2.1 show the block diagram of delta-sigma ADC. The ΣΔ-ADC consists of a 13-level delta-sigma modulator and the output of the ΣΔ-ADC is transferred modulator. The ΣΔM is implemented as a switched-capacitor circuit. The ΣΔM has an oversampling ratio of 64, and a 13-level quantizer is used. The CIFF structure has the advantage of consuming less power than the cascade integrator feedback structure, where the voltage swing at each integrator output is relatively small than that of CIFB structure [4.2.1]. A data weighted averaging (DWA) circuit is adopted. It is commonly used to minimize the nonlinearity error from DAC mismatch. An oversampling ratio of 64 is chosen to fulfill the noise requirement in designing ADC.

Matlab simulations have been conducted to verify the NTF of the ΔΣ modulator. The signal-to-quantization noise ratio (SQNR) is 113 dB as shown in Fig. 4.2.2

In designing delta-sigma ADC three major sources of noise that have to be considered [4.2.2]. A kT/C noise which is purely determined by sampling capacitor and oversampling ratio, and thermal noise, which is dominated by transconductance (g_m) of input devices of the first integrator, must be well-balanced for optimal circuit design (quantization noise is negligible compare to other noise in oversampling ADCs). In other words, it is not suitable for circuit optimization to distribute too much noise distribution on one side of a noise source

at given current consumption. The thermal noise source does not decrease in proportion to the resource, and even if it succeeds in reducing one noise source, the kT/C noise is kept constant and the improvement effect becomes smaller. For example, sampling capacitor cannot become infinitely larger due to area limitations Also, usually, in the switched capacitor circuits require more g_m of input devices due to the slew rate than is required by the thermal noise target specification. Obviously, increasing the current consumption to ease the such slew-rate limitation can lead to such an imbalance in noise distribution. To solve this issue, dynamic settling-boost technique or circuit is presented [4.2.3-4.2.4], but these technique requires additional resources such as power or device area. To overcome slew-rate limitation, we introduce settling-enhancement technique to mitigate this issue with increasing negligible amount of current. The switch circuit located at the output of first integrator. It can be an alternative solution rather than increasing current consumption.

Both slew rate and noise have to be considered in determining the input g_m of the amplifier. In other words, a sufficient slew rate that guarantees adequate settling time within given sampling time is important, as well as thermal noise requirement. When the input signal increases, a large enough transconductance of input devices are needed to satisfy the target settling time. However, in a switched capacitor circuit, there are always glitches just before the integrator integrates the signal. This phenomenon extends the slewing region which influences the settling performance of switched capacitor circuits. Also, this phenomenon degrades the integrator's settling time performance as settling demand becomes wide. To mitigate this issue, a switch is added at the integrator's output between each output node as shown in Figure 4.2.3. The Figure 4.2.4. shows the timing diagram of

switch operation. As the integrator samples the signal at P_1 and integrates at P_2, the settling-enhancement switch is connected shortly at the starting point of the integrating phase(P_3). It is off after the settling period, so that the integrator can integrate without a glitch. By doing so, the effect of earning settling time is achieved. The advantage of using this technique is significantly increased as the signal becomes larger. Therefore, a relatively small amplifier g_m is required to meet the settling requirement. As first integrator consumes a large amount of overall ADC power consumption, low power is expected with this settling enhancement technique by not increasing the current consumption at first integrator to enhance the slew rate. This technique take effect when sampling capacitor is chosen to be small due to area efficiency. In other words, balanced noise distribution and high area efficiency can be achieved by using this technique. The PDM modulator a system for representing a sampled signal as a stream of single bits using delta sigma conversion is followed by ΣΔ-ADC

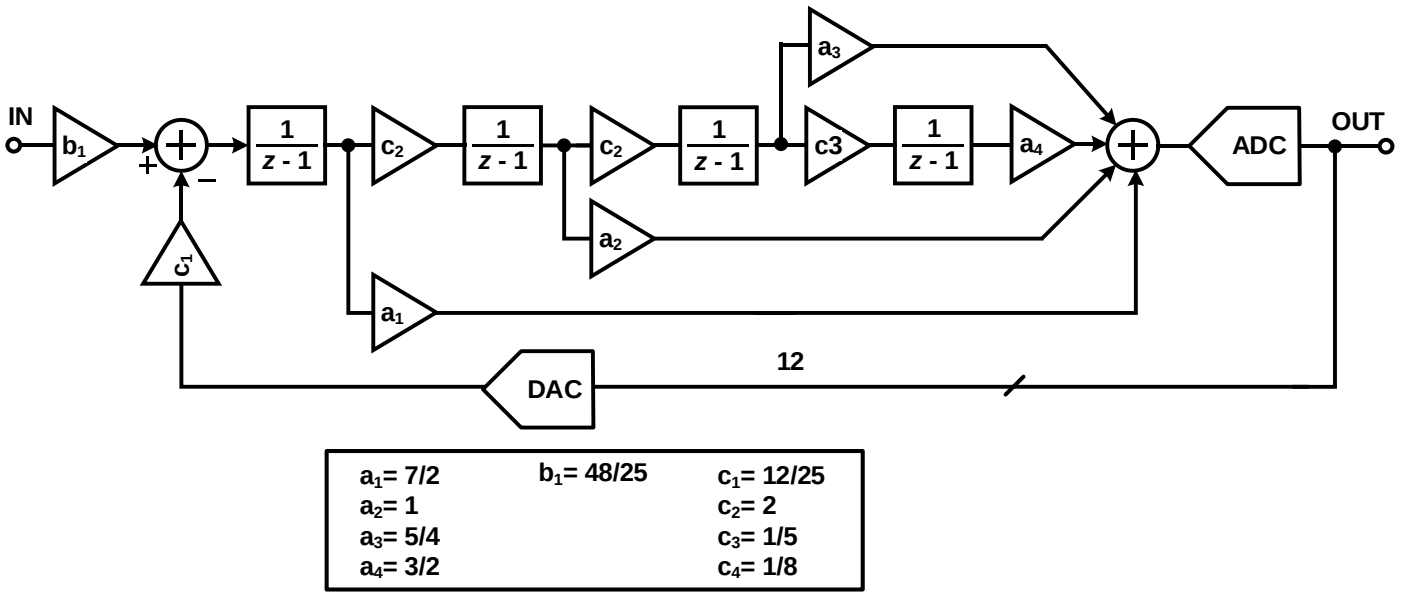


Figure 4.2.1 The block diagram of delta-sigma ADC

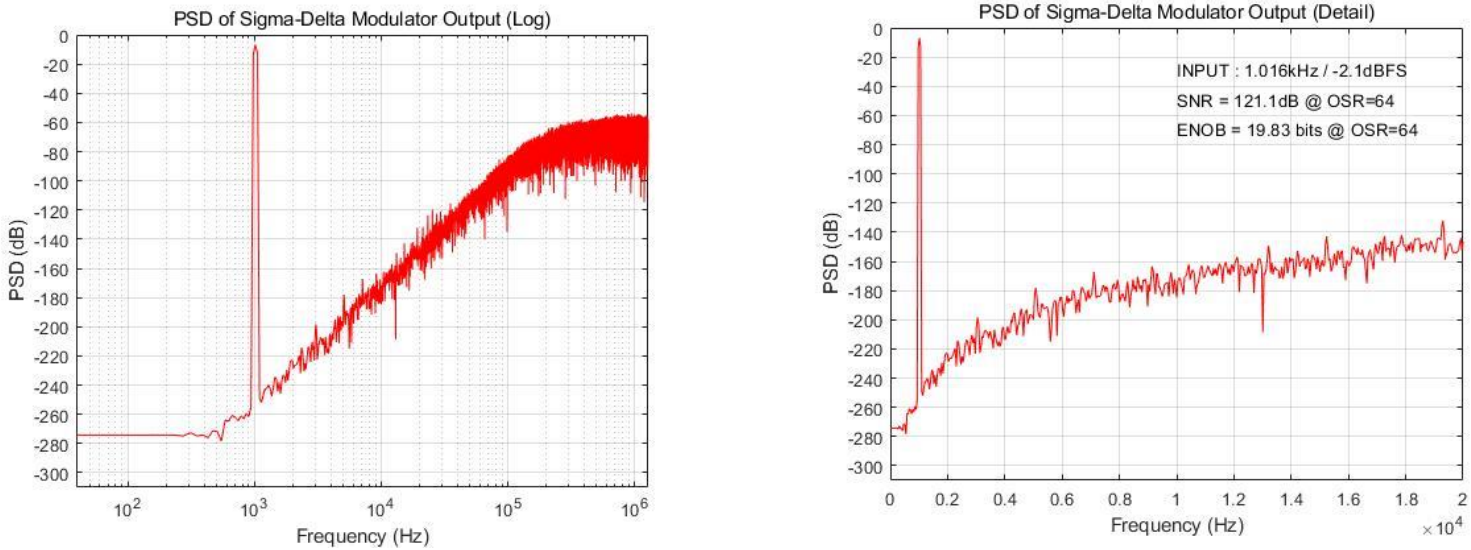


Figure 4.2.2 Matlab SQNR simulation of the designed NTF (The number of FFT points are 2^{16})

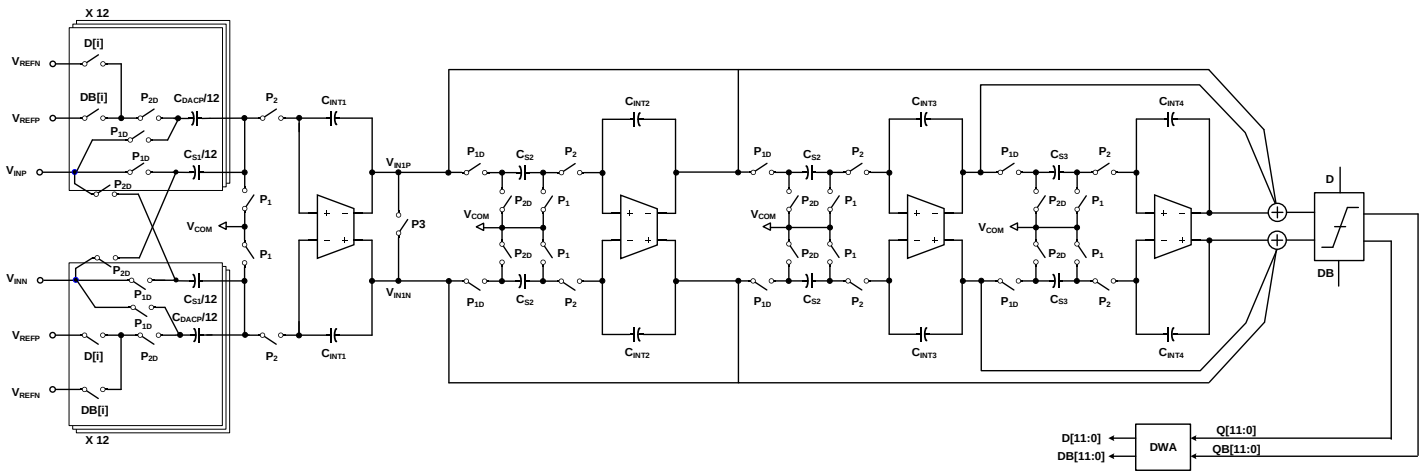


Figure 4.2.3 The schematic of delta-sigma modulator

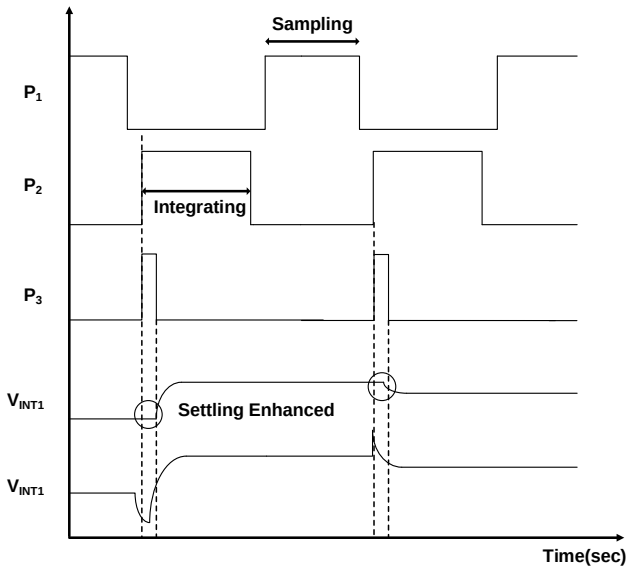


Figure 4.2.4 Timing diagram of delta-sigma ADC

CHAPTER 5

MEASUREMENT RESULTS

5.1 MEASUREMENT ENVIRONMENT

Our MEMS microphone readout circuit was fabricated in a 0.18 μm CMOS process and had an area of 0.98 mm^2. A microphone readout circuit and the measurement setup is

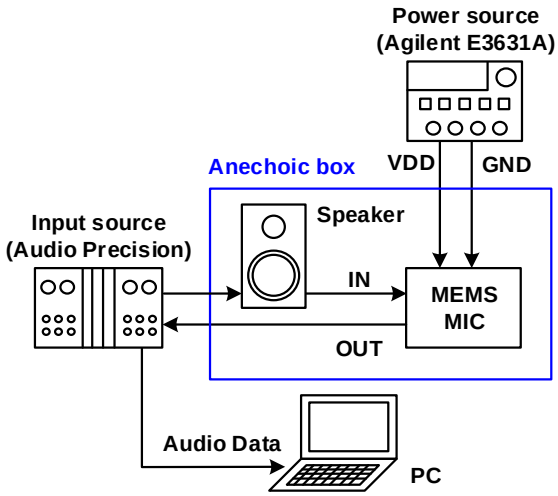


Figure 5.1.1 Measurement setup of MEMS microphone

shown in Figure 5.1.1. We set the distance between the speaker and our MEMS microphone through a reference microphone that consistently emits a 1kHz signal of 94dB SPL. Measurement were made using an Audio Precision AP2722 analyzer supplies a 1 kHz sine

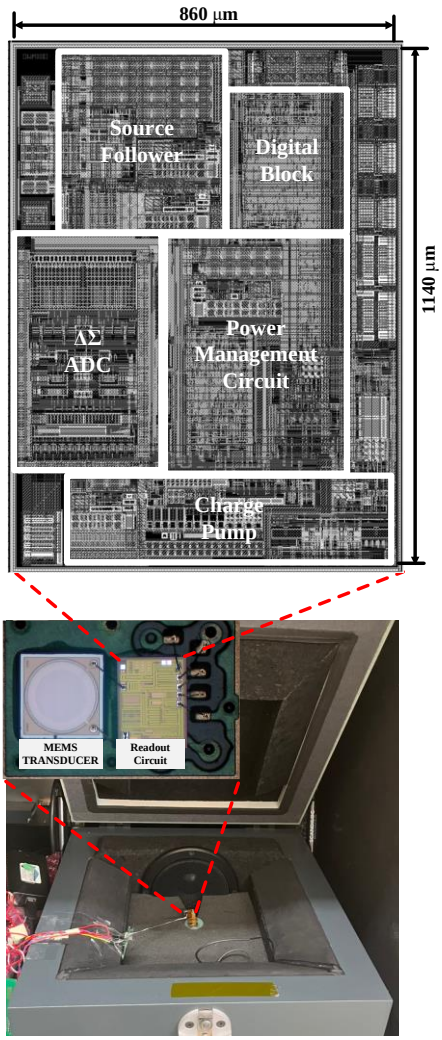


Figure 5.1.2 Microphotograph of the proposed MEMS microphone and measurement setup

wave to a speaker which produces a sound pressure of 1 Pa (or 94 dB SPL) at a microphone. The Microphotograph of the proposed MEMS microphone is shown in Figure 5.1.2.

5.2 MEASUREMENT RESULTS

The measured power spectral density of the output of the MEMS microphone with and without triple-sampling is shown in Figures 5.2.5(a) and (b) with the charge-pump voltage set to about 8 V. Without triple-sampling, the sensitivity of the MEMS microphone was -40.5 dBFS with an SNR of 57.6 dBA. With triple-sampling, the sensitivity was -28.4 dBFS with an SNR of 62.1 dBA. Sensitivity is exactly 12 dB different and this is because M=1.5 is used in the triple-sampling ADC. The thermal noise is increased, but the signal power increase is larger, resulting in an SNR improvement of 4.5 dB. The second-harmonic distortion is a characteristic of single-ended MEMS transducers. However, the increase in SNR of 4.5 dB has a difference from 10.91 dB in Table 4.3.5.1 which seems to be reasonable because the noise of the MEMS transducer itself and the noise of the source follower do not benefit from the triple-sampling structure

As shown in Figure 5.2.2, and assume flicker noise of ADC is negligible with A-weighting filter and since only ROIC SNR is measured to be 65.7dBA which means that noise from MEMS transducer itself is almost identical to ROIC noise. Also, noise of ADC with triple-sampling is designed to be almost same as that of source follower. Thus, the noise produced by the MEMS transducer, ADC with triple-sampling and SF can be calculated inversely

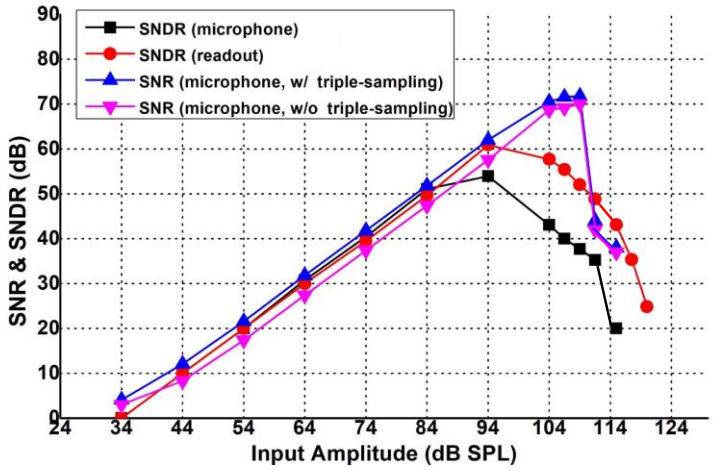


Figure 5.2.1 Measured A-weighted SNR and SNDR versus amplitude of the input

which is 64.6dBA, 68.7dBA and 68.7dBA respectively. From Table 4.3.5.1, SNR of ADC without triple-sampling becomes 58.6dBA. Therefore, we obtain 57.4dBA which is similar to our measured microphone SNR (without triple-sampling).

Figure. 5.2.1 shows how the A-weighted SNR and signal-to-noise-and-distortion ratio (SNDR) of the microphone and readout circuit with the amplitude of the input signal. The overall SNDR of a MEMS microphone is bounded by that of the MEMS transducer as described in Figure 5.2.1 [5.2.1]. The acoustic overload point, defined as the sound pressure level at which the total harmonic distortion exceeds 10 %, was found to be 115 dBSPL.

The measured output of the microphone versus gain with a fixed input (94 dBSPL) is shown in Figure. 5.2.3. As illustrated in Figure 5.2.3, the measured output is highly linear with a coefficient of determination of 0.9999.

Figure 5.2.4 shows the measured SNR of microphone versus M in triple-sampling.

When *M* is small, the effect of increasing the SNR due to triple-sampling is large, because as *M* is small, the total noise portion of the ADC increases.

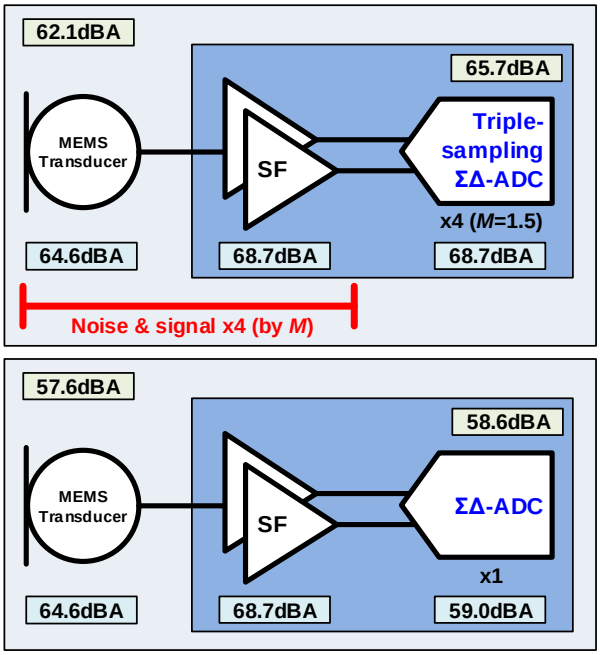


Figure 5.2.2 Verification of Equation based on a measurement results

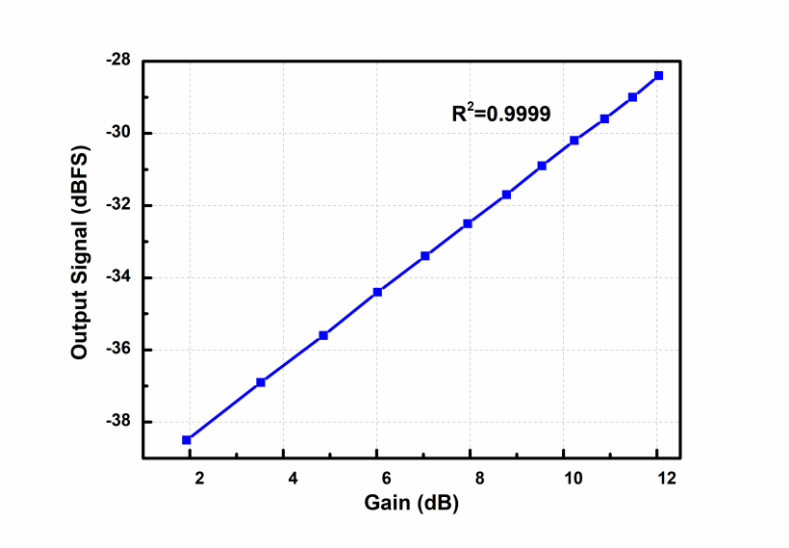


Figure 5.2.3 Measured MEMS microphone's output signal versus gain. (Changing M in triple-sampling)

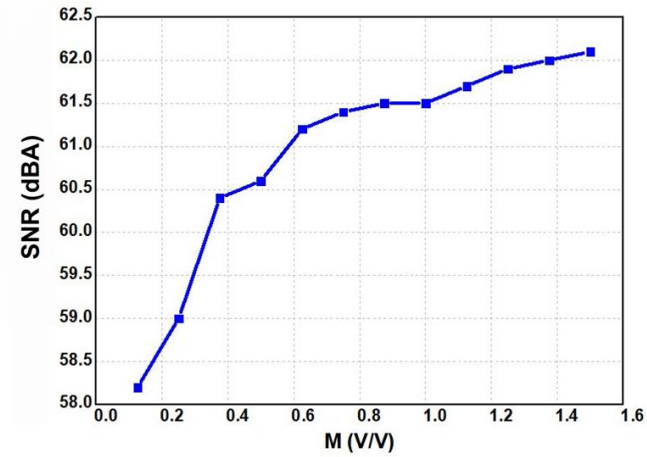


Figure 5.2.4 Measured SNR versus M in triple-sampling MEMS microphone

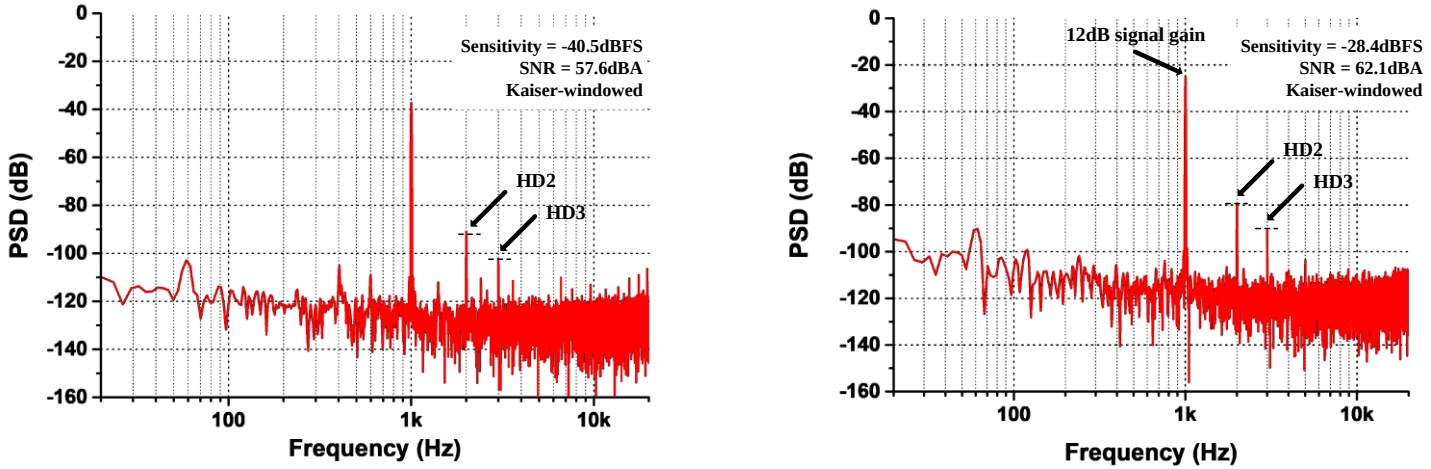


Figure 5.2.5 Measured power spectral density of the MEMS microphone (a) without using triple-sampling ADC (b) with triple-sampling ADC, for a 94dB SPL 1kHz sine wave input

5.3 PERFORMANCE SUMMARY

The current consumption drawn by the chip was 520 μA and the die size of our microphone is 0.98 mm^2. Table 5.3.1 summarizes the performance of our microphone and compares it with that of other recent designs. Power and area are reduced by removing the PGA and using triple-sampling ADC. Our microphone is designed by optimizing the power of ROIC according to the performance of MEMS itself and consumes the lowest current, among ROICs including MEMS. Also, our microphone has smallest area among ROICs including MEMS. The noise performance of our microphone is comparable to that of the other circuits in Table 5.3.1.

Parameter	**This work**	[4] ISSCC ‘17	[5] ICECS ‘13 *ROIC only	[9] TCAS-II ‘20	[10] SENSORS ‘18
MEMS microphone type	**Single-Ended**	Differential	Single-Ended	Single-Ended	Single-Ended
Technology [μm]	**0.18**	0.13	0.25	0.18	0.5
Supply voltage [V]	**1.8**	1.8	1.8	3.3	1.8
Sensitivity @ 94 dBSPL[dBFS]	**-28.4**	-46	-26	-37.2	-26
SNR @ 94 dBSPL [dBA] *microphone	**62.1**	67	-	62.8	63
SNR @ 94 dBSPL [dBA] *ROIC	**65.7**	-	63	65.8	-
AOP (10% THD) [dBSPL]	**115**	136	-	119.4	120 (1% THD)
Active current [mA]	**0.52**	1.2	0.47	2.75	0.72
Sampling rate (MHz)	**3.072**	3.072	2.4	12.288	-
Die size (mm^2)	**0.98**	1.17	0.72 *Active area	3.71	1.2 *Readout area

Table 5.3.1 Summary of the performance of our digital MEMS microphone, compared with that of other recent designs

CHAPTER 6

CONCLUSION

In this thesis, we have presented a digital capacitive MEMS microphone based on triple-sampling ADC rather than a PGA with slew-rate enhanced technique. This ADC introduces a half-period delay input and non-delayed input to one copy of the signal to increase the gain of the integrator but that has a negligible effect due to oversampling which is usually bigger than double digits. An additional driving capability is unnecessary because it was made to use the sampling capacitor at P2. The common-mode rejection ratio (CMRR) of the proposed cross-sampling is improved by subtracting differential inputs in this way as we expected in differential circuit, reducing common-mode noise and even harmonic distortion. Triple-sampling ADC also works as a single-to-differential circuit by simply adding DC input to differential input side. We also combine the idea with existing sampling capacitor multiplied structure and expand to rational embedded gain.

Noise performance of triple-sampling ADC is improved as amplifier noise and DAC kT/C noise does not affected by triple-sampling. Moreover, with embedded gain at delta-sigma ADC, PGA becomes removable thereby reduces noise and current consumption from PGA. Therefore, the SNR is improved by the increase in signal magnitude that results from

this design as well as the efficient use of the sampling capacitors and the DAC capacitors. The slew-rate enhanced technique is also adopted to reduce distortion.

Our readout circuit integrates a charge pump a pseudo-differential source follower and a power management circuit. Our microphone has an SNR of 62.1 dBA with triple-sampling ADC which has 4.5dB improvement compared to 57.6 dBA SNR without triple-sampling technique. It draws current consumption of 520 μA at 1.8 V with an AOP of 115 DBSPL. And had an area of 0.98 mm^2. The proposed readout circuit was fabricated in a 0.18 μm CMOS process.

BIBLIOGRAPHY

[1.1.1] S. A. Jawed, D. Cattin, M. Gottardi, N. Massari, A. Baschirotto and A. Simoni, "A 828μW 1.8V 80dB dynamic-range readout interface for a MEMS capacitive microphone," ESSCIRC 2008 - 34th European Solid-State Circuits Conference, 2008, pp. 442-445.

[1.1.2] J. Citakovic et al., "A compact CMOS MEMS microphone with 66dB SNR," 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, 2009, pp. 350-351,351a.

[1.1.3] R. J. Littrell, “High performance piezoelectric MEMS microphones,” Ph.D. dissertation, Univ. of Michigan, 2010.

[1.1.4] E. Bach et al., "9.5 A 1.8V true-differential 140dB SPL full-scale standard CMOS MEMS digital microphone exhibiting 67dB SNR," 2017 IEEE International Solid-State Circuits Conference (ISSCC), 2017, pp. 166-167.

[1.1.5] A. Barbieri and G. Nicollini, "A 470μA direct readout circuit for electret and MEMS digital microphones," 2013 IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS), 2013, pp. 341-344.

[1.1.6] I. Deligoz et al., "A MEMS-Based Power-Scalable Hearing Aid Analog Front End," in IEEE Transactions on Biomedical Circuits and Systems, vol. 5, no. 3, pp. 201-213, June 2011

[1.1.7] S. Wang et al., "A Power-Efficient Capacitive Read-Out Circuit With Parasitic-Cancellation for MEMS Cochlea Sensors," in IEEE Transactions on Biomedical

Circuits and Systems, vol. 10, no. 1, pp. 25-37, Feb. 2016

[1.1.8] J. Jun, C. Rhee, S. Kim and S. Kim, "An SC Interface with Programmable-Gain Embedded Delta-Sigma ADC for Monolithic Three-Axis 3-D Stacked Capacitive MEMS Accelerometer," in IEEE Sensors Journal, vol. 17, no. 17, pp. 5558-5568, 1 Sept.1, 2017.

[1.2.1] Y. Yang, “A Digital MEMS Microphone for Speech Recognition using a Sound Activity Detector.” Ph.D. dissertation, Seoul National University, 2020.

[2.1.1] Y. Yang, B. Lee, J. S. Cho, S. Kim and H. Lee, "A Digital Capacitive MEMS Microphone for Speech Recognition with Fast Wake-Up Feature Using a Sound Activity Detector," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 9, pp. 1509-1513, Sept. 2020.

[2.1.2] S. Pavan, N. Krishnapura, R. Pandarinathan, P. Sankar, “A Power Optimized Continuous-Time ΣΔ-ADC for Audio Applications.” IEEE J. of. Solid-State Circuits(JSSC), vol. 43, no 2, pp 351-360, Feb. 2008.

[2.1.3] Florin-Silviu Dumitrym, Serban Mihalache, Marius Enachescu, “OPAMP’s finite gain and slew rate impact on a 16-bit ΣΔ-ADC performance: A case study” International Semiconductor Conference (CAS) pp 161-164, Oct. 2017

[2.1.4] A. E. Stevens, G. A. Miller “A high-slew integrator for switched-capacitor circuits” IEEE J. of. Solid-State Circuits(JSSC), vol. 29, pp 1146-1149, Sep. 1994

[2.1.5] Mohammad H. Naderi, Suraj Prakash, Jose Silva-Martinez, “Operational Transconductance Amplifier With Class-B Slew-Rate Boosting for Fast High-Performance Switched-Capacitor Circuits” IEEE J. of. Solid-State Circuits(JSSC), Vol. 65, No. 11, Nov. 2018

[3.2.1] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," in *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374-378, June 1976

[4.2.1] Pin-Han. Su, Herming. Chiueh, “The Design of Low-Power CIFF Structure Second-Order Sigm-Delta Modulator” IEEE International Midwest symposium on circuits and systems(MWSCAS), pp. 377-380, no 9, Aug. 2009

[4.2.2] Schreier, Richard, and Gabor C. Temes. Understanding delta-sigma data converters. Vol. 74. Piscataway, NJ: IEEE press, 2005.

[4.2.3] B. Lee, J. Yang, J. s. Cho and S. Kim, "A Low-Power Digital Capacitive MEMS Microphone Based on a Triple-Sampling Delta-Sigma ADC with Embedded Gain," in *IEEE Access*, 2022

[5.2.1] G. Nicollini and D. Devecchi, "MEMS Capacitive Microphones: Acoustical, Electrical, and Hidden Thermal-Related Issues," in IEEE Sensors Journal, vol. 18, no. 13, pp. 5386-5394, 1 July 1, 2018.

한글초록

본 논문에서는 트리플 샘플링 적분기를 사용한 Capacitive 방식의 MEMS 마이크로폰이 제시되었다. 트리플 샘플링은 델타-시그마 방식의 아날로그-디지털 변환기의 첫 번째 적분기에 사용되었고 크게 두 가지의 동작으로 구분된다. 첫 번째로 적분기의 입력에서 반주기 지연 차동 입력을 빼서 신호 크기를 2배로 만들는 방식. 두 번째로 DAC의 피드백 커패시터를 샘플링 커패시터로 사용하여 입력 전압을 추가로 증가시키는 방식이다. 추가적으로 기존에서 샘플링 커패시터를 증가시켜 신호의 크기를 증폭시키는 방식과 결합하여 실수배의 이득을 얻을 수 있다. 또한 추가적인 커패시터, 타이밍, 전류 소모 없이 구조 변경만으로 이를 달성하였기 때문에 별다른 trade-off 없이 신호의 크기를 증폭시킬 수 있었다. 추가적으로 트리플 샘플링 방식의 적분기 신호 전달 함수 및 잡음 분석 또한 포함하였다.

우리의 readout 회로는 공급 전압이 1.8V인 0.18 μm CMOS 공정으로 구현하였고 single-ended capacitive MEMS 트랜스듀서를 사용하여 측정하였다. 전류 소모량은 520 μA 이다. 마이크로폰은 A-weighted 신호 대 잡음 비는 62.1 dBA, 음향 과부하 지점은 115 dB SPL을 달성하였고 칩의 die size는 0.98mm^2 이다.

주요어 : 디지털 capacitive MEMS 마이크로폰, readout 회로, 이득 내장된 아날로그 디지털 변환기, PGA 없는, 저전력회로

학 번 : 2017-30933