Wide-Band Compact 1.8 V-0.18 μm CMOS Analog Front-End for Impedance Spectroscopy

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***Abstract*—In this letter, a fully integrated configurable front-end for Impedance Spectroscopy (IS) is presented. The circuit includes fully differential in-phase and quadrature channels, using a transconductor (TC)-transimpedance (TI) approach. The input TC, shared for both channels, is based on a programmable degenerated differential pair to attain low-noise programmable-gain, while identical $TI_{I/Q}$ with embedded synchronous rectification provide both I,Q outputs, filtered through f_c adjustable G_m-C integrators. It exhibits a programmable gain ranging from 0 dB to 40 dB with 87 MHz bandwidth, amplitude and phase recovery errors below 1.9% and 2.5° respectively and an input referred noise floor of 16.7 nV/√Hz. The result is a high-performance very compact topology with a total power consumption of 292 μW at a 1.8 V power supply, thus constituting an appropriate solution for full on chip multichannel IS systems.**

***Index Terms*—Low-voltage low-power (LVLP), CMOS analog front-end, impedance spectroscopy (IS), synchronous demodulator, system on chip (SoC).**

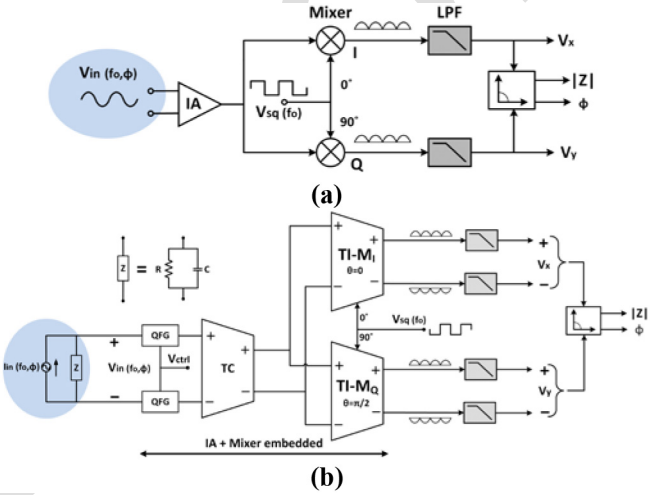

Fig. 1. Dual-phase analog front-end structure for IS: (a) classic structure; and (b) proposed structure.

I. Introduction

MANY emerging sensors, especially those based on bio and nano-materials, rely on Impedance Spectroscopy (IS), i.e., the sensor information is obtained from its impedance extraction over a specific frequency interval. However, despite its promising applications —from environmental monitoring to molecular/DNA/proteins diagnosis— the use in portable and wearable scenarios is hindered by the lack of suitable high performance low-voltage low-power (LVLP) on-chip electronic interfaces [1]–[7]: designs [1], [2] use discrete components; [3]–[5] present high power and area consumption; [1], [5], [6] are single-channel, not being capable of recovering the real and imaginary components of the impedance under test. In addition, the trend towards the integration of sensor arrays to permit multi-parameter sensor fusion imposes even more demanding design restrictions, with increasing operating frequencies to widen the application scenarios. Among the multichannel CMOS IS read-out approaches [8]–[10], the analog lock-in-based Frequency Response Analysis (FRA) technique seems an appropriate solution potentially featuring the required LVLP high frequency constraints. It is based on dual phase sensitive detection (PSD) to extract the response of low signal-to-noise ratio (SNR) sensor signals at a reference frequency f_0. Typically, as shown in Fig. 1a, the impedance sensor signal V_{in} (f_0, ϕ) is amplified (IA-instrumentation amplifier) and then multiplied by two mixers I, Q driven by quadrature square signals (f_0, $\theta = 0°$), (f_0, $\theta = 90°$). The resulting signals are low-pass filtered to extract the DC components V_x, V_y, proportional to the real and imaginary components, from which the signal magnitude $|Z|$ and phase ϕ can be recovered.

This letter presents the design of an analog dual-phase FRA-IS read-out recovering simultaneously both I and Q responses, while meeting the LVLP constraints with an ultra-compact topology and widening the state-of-art operating frequencies up to the 100 MHz range (molecular and cell range), contributing to the creation of the next generation of lab-on-chip devices.

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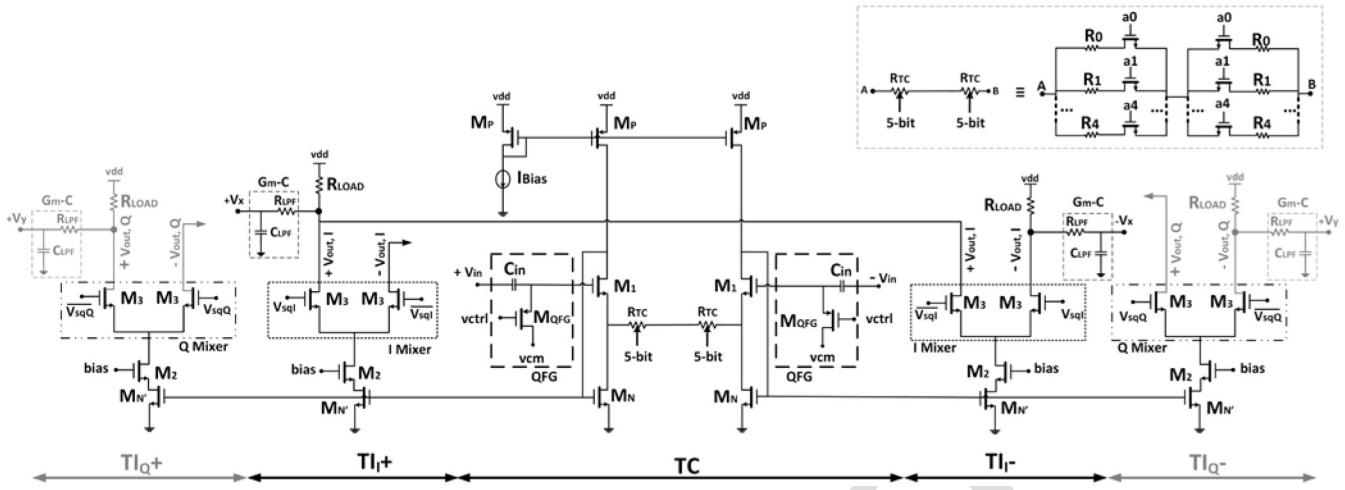

Fig. 2. Proposed fully configurable TC-TI-M structure with dual I/Q output. Schematic view.

II. Design

The block diagram of the proposed IS front-end is shown in Fig. 1b. Compared with previous structures, to enhance CMRR and reduce noise, a fully differential configuration is considered. It is based on an open-loop Transconductor-Transimpedance (TC-TI) approach [11], [12], with shared input TC and two identical I, Q quadrature TIs with embedded mixer (TI-$M_{I,Q}$). These strategies result in an enhanced bandwidth with better area and power efficiency. Both DC V_x and V_y I, Q outputs are simultaneously recovered after fully integrated LPFs, implemented using the G_m-C integrator reported in [13], optimized to work in this application.

Fig. 2 shows its schematic. The input signal is driven to the TC input stage through a Quasi Floating Gate (QFG) structure to allow direct sensor/front-end coupling, setting $V_{cm} = 0.9$ V and a high pass frequency $f_{c,H} = 1/2\pi R_{QFG} C_{in}$. The capacitance $C_{in} = 1$ pF (MIM) and R_{QFG} is a NMOS transistor, whose equivalent resistance can be modified through the gate voltage V_{ctrl}, adjusting $f_{c,H}$, in a 6.7 Hz-172 kHz range to filter low-frequency noise and undesired signal contributions, regulating the operating frequency range. The TC-stage (Fig. 2) is based on a NMOS-input Flipped Voltage Follower degenerated through a 5-bit array of symmetrical resistances R_{TC}, implemented with MOS-switches in series with POLY-resistances. The input differential voltage is buffered to R_{TC} and converted to current. The TC output currents are copied to I, Q TIs through the current mirrors M_N-$M_{N'}$, and converted back to voltage using POLY resistors $R_{LOAD} = 35$ kΩ, achieving overall programmable gains $G = R_{LOAD}/R_{TC}$ from 0 dB to 40 dB in 10 dB steps and 100 MHz bandwidth, allowing to fit different target applications.

The embedded-multiplication technique is based on [14]: taking the TI-M_I for the following explanation, in each $M_{N'}$-M_2 TI output current branch two M_3 split matched transistors are introduced, with their gates driven by complementary control signals (V_{sqI} and its inverse $\overline{V_{sqI}}$, f_0, in phase with the input signal) and connected to the R_{LOAD} outputs $V_{out,I}^{\pm}$. In this way, M_3 act as embedded mixers, providing an output $V_{out,I} = (V_{out,I}^{+} - V_{out,I}^{-})$ according to V_{sqI} and $\overline{V_{sqI}}$ variation and the I synchronously rectified signal is obtained. By replicating this TI structure, but with the quadrature control signals V_{sqQ} and $\overline{VsqQ}$ the dual-phase architecture with both I and Q outputs is achieved.

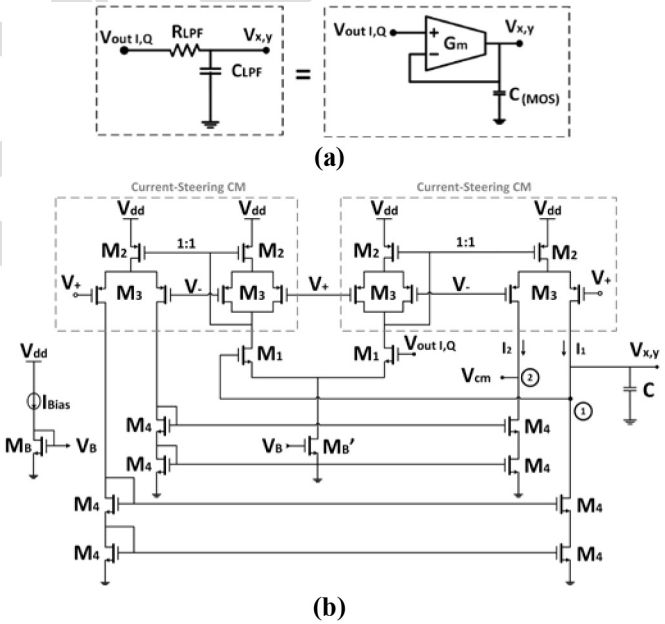

Fig. 3. G_m-C structure to filter the output signal: (a) Basic diagram; and (b) Schematic view [13].

The output G_m-C integrator is shown in Fig. 3. It is a differential-input single-output architecture in unity gain closed-loop feedback configuration.

The integrating C is a 50 pF MOS capacitor; the G_m is based on a classic mirrored OTA that keeps constant the V–I conversion gain (M_1, g_{m1}), while both G_m reduction and tuning are done in the output current transfer section, exploiting a M_2-M_3 cascode current mirror steering technique as the most suitable choice to effectively reduce the G_m, while preserving a good power-area-dynamic range trade-off. It presents a tuneable cut-off frequency f_c ranging from 66 mHz up to 2.5 kHz, with a power consumption of 5.4 μW, an area of 0.014 mm^2 and a DR > 70 dB.

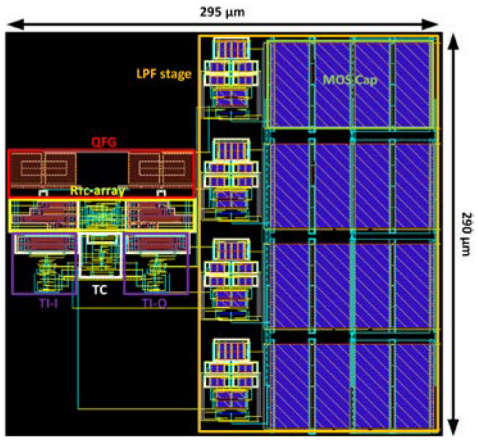

Fig. 4. Layout view of the proposed structure.

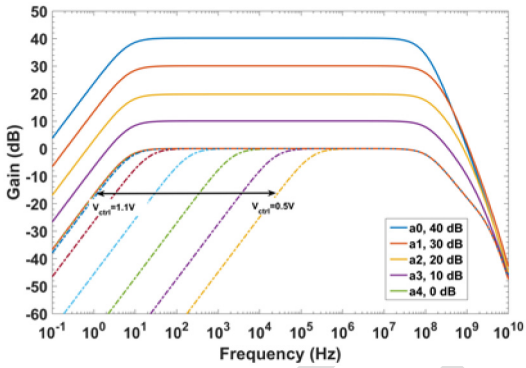

Fig. 5. 5-bit {a0-a4} programmable-gain, with High Pass Filtering control applied to minimum gain.

III. Performance

The proposed IS read-out has been designed in the 0.18 μm CMOS technology from UMC. The power supply is 1.8 V and a bias current I_{Bias} = 25 μA is set for the TC-TI-M structure (Fig. 3) and I_{Bias} = 0.5 μA for the G_m–C integrators (Fig. 3). It presents a total power consumption of 292 μW and an active area of 0.0569 mm^2 including the fully integrated G_m–Cs. The layout view of the proposed system is shown in Fig. 4.

Fig. 5 shows the 5-bit programmable gain post-layout frequency response, ranging from 0 dB to 40 dB. The bandwidth $f_{c,LP}$ is kept around 100 MHz (varies from 87 MHz at maximum gain, 123 MHz at 0 dB). For the minimum gain setup, the frequency response for variable V_{ctrl} is also shown: the high pass cutoff frequency $f_{c,HP}$ can be adjusted from 6.7 Hz (V_{ctrl} = 1.1 V) up to 172 kHz (V_{ctrl} = 0.5 V).

Fig. 6 shows the behaviour of the synchronously rectified dual-phase outputs for an input signal of 1 mV at a f_0 = 10 kHz and maximum gain, with V_{sqI} and V_{in} in phase. For this case, the theoretical $V_{x,theo} = (2/\pi)2V_{in}Gcos(\theta)$ = 127.3 mV, while after filtering V_{outI}, the recovered V_x is $V_{x,rec}$ = 125.8 mV, showing a relative error of 1.2 %.

Fig. 7a shows the simulated V_{out} DC I, V_x, and Fig. 7b the recovered input amplitude and its error, for an AC input voltage ranging from 100 nV to 5 mV at 0 dB, 20 dB and 40 dB gain configurations, f_0 = 10 kHz in-phase with V_{sqI} and with the LPF cutoff set to f_c = 10 Hz.

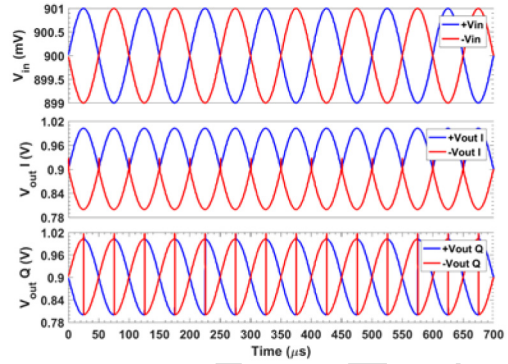

Fig. 6. Synchronously rectified $V_{out}I$ and $V_{out}Q$ outputs. Input signal: amplitude = 1 mV, f_o = 10 kHz in phase with $V_{sq}I$, gain = 40 dB.

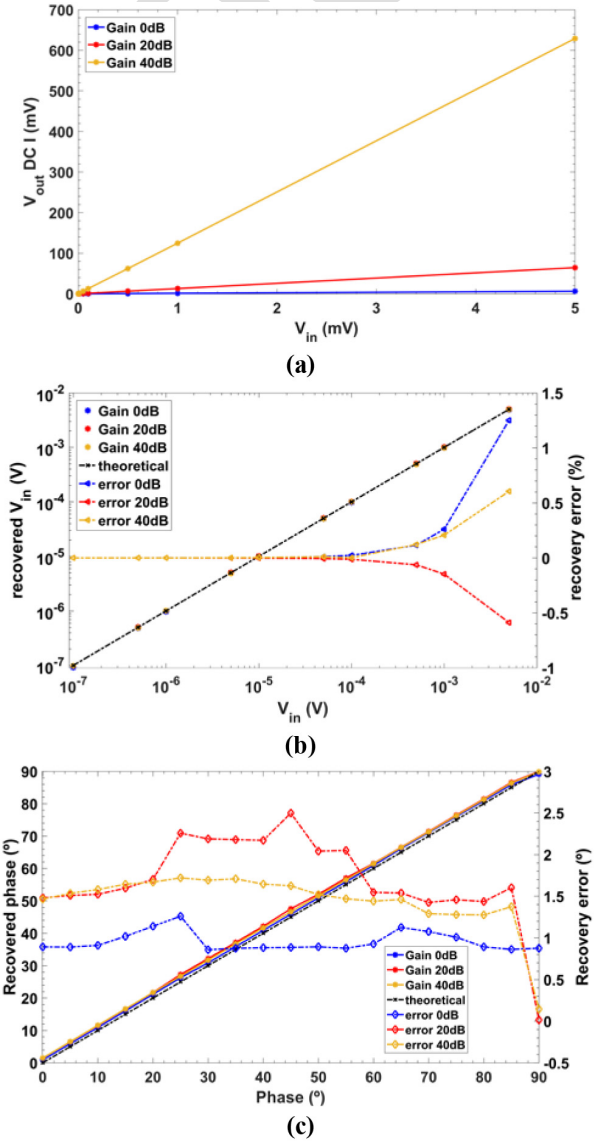

Fig. 7. Recovered performance at 0 dB, 20 dB and 40 dB gain: (a) DC output I (V_x) vs input signal amplitude from 100 nV to 5 mV; (b) recovered input signal amplitude and error (%); and (c) recovered phase and error (°) for a constant 1 mV input signal.

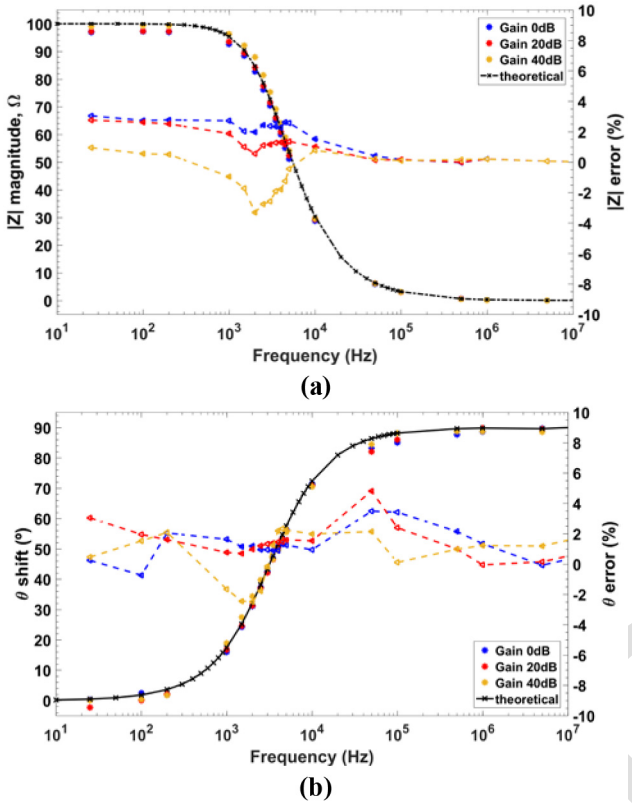

Fig. 8. Recovered Z magnitude and phase with their full-scale errors (w/o calibration): recovered vs theoretical for 0 dB, 20 dB and 40 dB gain (a) magnitude and (b) phase.

Fig. 7c shows the recovered phase and its error at a fixed 1 mV input amplitude, $f_0 = 10$ kHz, $f_c = 10$ Hz varying the input phase (ϕ) from 0° to 90°; note that phase offset calibration can be performed to optimize phase recovery.

To validate this proposal, a Z impedance composed of a resistor R = 100 Ω in parallel with a capacitor C = 500 nF as shown in Fig. 1b is used. Excited with an AC current, this generates the input voltage, V_{in}, driven through the QFG to the input pair of the TC-stage. The two resulting DC output voltages (V_x and V_y) at the branches Q and I are used to recover the phase shift and magnitude -or the real and imaginary components- of the impedance Z according to

$$|Z| = \frac{\pi}{2}\frac{1}{G}\sqrt{V_x^2 + V_y^2} \quad (1)$$

$$\theta = \text{atan}\left(V_y/V_x\right) \quad (2)$$

Fig. 8 shows, the recovered magnitude and phase for an AC input current of 100 μA_{pp} at 19 different frequencies over the 25 Hz-10 MHz range, operating at 0 dB, 20 dB and 40 dB and a $f_{c,HP} = 6.7$ Hz ($V_{ctrl} = 1.1$ V), which renders the worst case recovery errors. Fig. 8a shows the recovered magnitude compared to the theoretical value and Fig. 8b shows the recovered phase compared to its theoretical value. The full-scale Z magnitude (Fig. 8a) and phase (Fig. 8b) recovery errors are below 3.3 % and 4.8 % for all the frequency range and gain configurations.

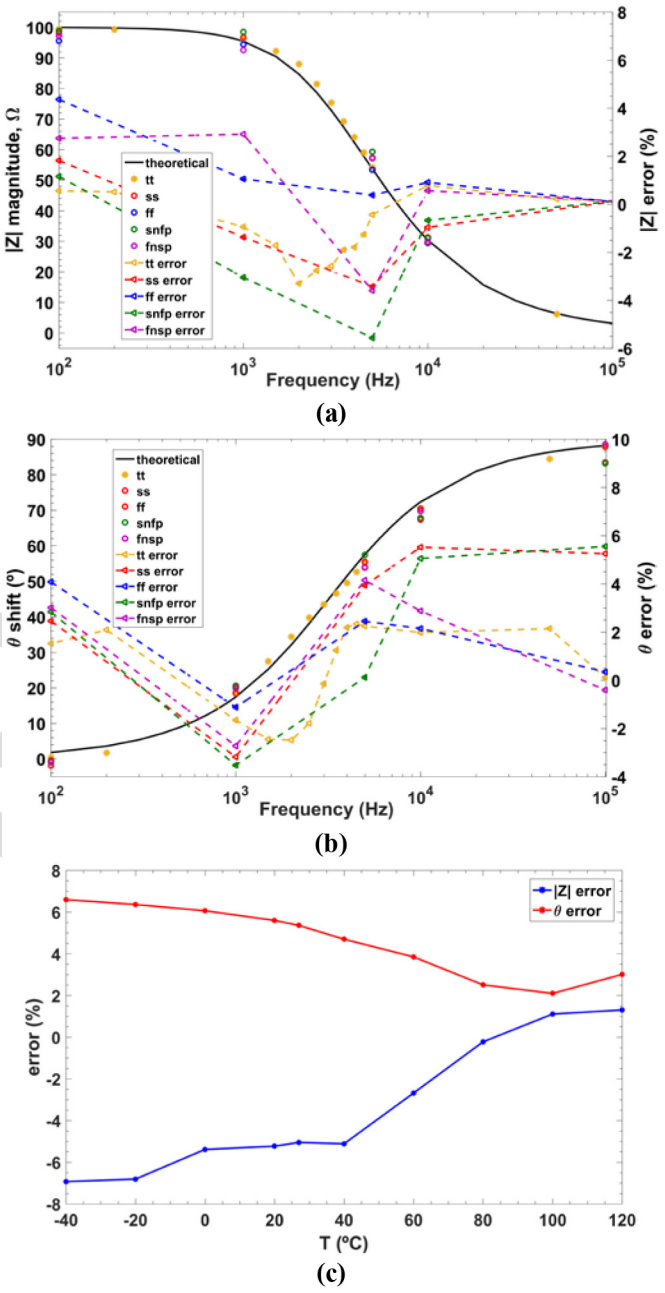

Fig. 9. Recovered Z magnitude and phase (w/o calibration), 40 dB gain: corner analysis (a) magnitude and (b) phase; and (c) temperature dependence at $f_{in} = 5$ kHz.

Fig. 9 shows the corner and temperature analysis at 40 dB gain, with their full-scale errors. Fig. 9a and Fig. 9b display the corners for the recovered Z magnitude and phase, showing recovery errors below 5.6% (magnitude) and 5.5% (phase). Fig. 9c presents the temperature dependence at f_{in} 5 kHz; recovery errors are below 7% for both magnitude and phase.

A comparison of the performance of the proposed structure with other previously reported works operating over 100 kHz is presented in Table I. The input-referred noise is given for both maximum and minimum gain in a frequency range from 6.7 Hz ($V_{ctrl} = 1.1$ V) up to 87 MHz (40 dB gain) or 123 MHz (0 dB gain).

TABLE I
COMPARISON WITH PREVIOUSLY REPORTED WORKS

Parameter	This work	[9]'13	[16]'13	[17]'15	[8]'16	[15]'20	[18]'20	[19]'21	[3]'21
Results	Sim	Exp	Sim	Exp	Sim	Sim	Exp	Sim	Exp
Mag&Phase recovery	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
LPF integrated	Yes, tuneable	Yes	N/A	No	Yes	Yes	Yes	Yes	N/A
CMOS (μm)	0.18	0.18	0.18	Arduino-based	0.18	0.18	0.18	0.18	0.065
Supply (V)	1.8	1.8	±0.9	N/A	1.8	1.8	1.8	1.8	1.8, 3.3
Power (W)	291.6μ	37m	28m	N/A	482μ	36.1μ	311.4μ	544μ	9.6m
Gain (dB)	0-40	N/A	N/A	N/A	39-59	0-20	N/A	7-48	24
Freq. range (Hz)	6.7–87M	15M-20M	100-580k[(b)]	0.01-100k	1.1M	0.1–1M	DC-100k	100-10M	1k-10M
Noise (nV/√Hz)	224.4-16.7	N/A	NA	N/A	N/A	189.6	80fA/√Hz @100Hz	N/A	14.2 @10-100k
Phase recov error	<2.5° / <1°[(a)]	N/A	<2.2°	<3°	N/A	<1.7°	<10%[(c)]	<1.8°[(c)]	≤4.32°
Amp recov error	<1.9%	N/A	<2.5%	<5%	<10%	N/A	<10%[(c)]	<1%[(c)]	N/A
Area (mm^2)	0.0569	5	0.4	N/A	0.03	N/A	0.208	1.95	16 (die, 8ch)
CMRR (dB)	164.4@100k	N/A	N/A	N/A	78@100kHz	55.3@N/A	N/A	N/A	N/A
FoM_1	0.477μ/0.191μ	N/A	42.5m	N/A	N/A	N/A	6.48m	190.9μ	8.3m[(d)]
FoM_2	0.362μ	N/A	48.3m	N/A	131.45μ	N/A	6.48m	106.1μ	N/A

N/A Not Available; [(a)] without/with phase offset calibration; [(b)] increased to 10 MHz for minimum gain; [(c)]Recovered Z error; [(d)]For an area of 2 mm^2/channel.

Two FoMs are proposed based on [15], to compare the behaviour of our structure with previously reported works.

$$FoM_1 = \frac{Power\ [\mu W] * area\left(mm^2\right) * Phase\ error[^\circ]}{Frequency\ range\ [Hz]} \quad (3)$$

$$FoM_2 = \frac{Power\ [\mu W] * area\left(mm^2\right) * Magnitude\ error[\%]}{Frequency\ range\ [Hz]} \quad (4)$$

The proposed TC-TI-$M_{I,Q}$ topology, with a common TC and the mixers embedded in the TI structures, results in a low area (0.0569 mm^2) and low power (291.6 μW) consumption solution, with the largest frequency range -close to 100 MHz- among the reviewed works in Table I and a tuneable gain range of 40 dB, while keeping both recovery errors within competitive values. Overall, it reports the best performance-consumption trade-off as shown by FoM_1 and FoM_2.

IV. CONCLUSION

A fully integrated reconfigurable dual-phase analog front-end for impedance spectroscopy has been presented, based on a fully differential approach. The proposed mixer-embedded structure results in a compact solution (0.0569 mm^2 area) with a wide bandwidth of 87 MHz, a programmable gain from 0 dB to 40 dB and a low power consumption of 291.6 μW, paving the way for full on chip multichannel wideband IS systems.

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