Novel Front-End Design with High-voltage Transceiver ASICs for Ultrasound Computed Tomography

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***Abstract*—3D Ultrasound Computed Tomography (USCT) is an imaging method for early breast cancer detection. The third generation 3D USCT device is developed at Karlsruhe Institute of Technology. The USCT III device has a hemispherical transducer distribution and emits and receives nearly spherical waves. This enables reflection and transmission imaging simultaneously and fully in 3D. The main challenges for the front-end design are to integrate a large number of transducers, to allow high voltage coded excitation, and to receive low amplitude signals with high quality. These challenges were solved using a smart sensor front-end design with a custom application specific integrated circuit (ASIC).**

***Index Terms*—front-end, smart sensor, ASIC**

I. Introduction

3D USCT is an upcoming method to detect the early breast cancer [1], [2]. Compared with other detection methods, diagnostic ultrasound is harmless to the human body. With the 3D transducer array, the system can obtain both transmission and reflection signals. Based on the data from these transducers, speed of sound, attenuation, and reflection of the measured object can be reconstructed [1], [3].

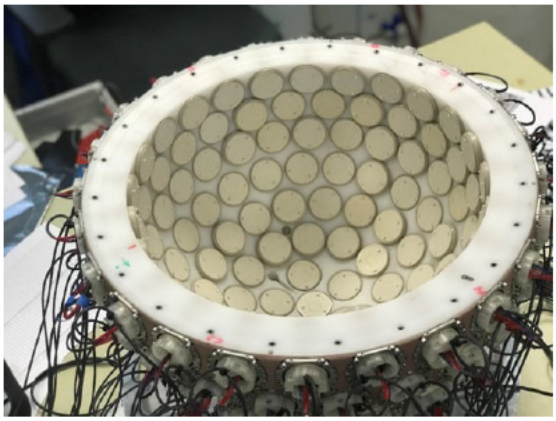

Fig. 1. Hemispherical 3D sensor array in USCT III device

Fig. 1 shows the 3D transducer array of the USCT III device, which consists of 2304 transducers grouped into 128 Transducer Array Systems (TAS). The transducers are pseudo-randomly distributed on the hemispherical holder [4]. They are working with linear frequency modulated ultrasound signals, which are set from 0.5 MHz to 4.5 MHz. However, the 3D transducer array sets challenges to the front-end design. To receive the signal less than uV, the transducers have to be as close as possible to the front-end electronics. In addition, a pulse compression method is used to improve signal penetration. Therefore, the front-end requires a large bandwidth and a high dynamic range.

II. System Architecture

To balance the large number of transducers and the transducers to front-end distance, the system was designed with a distributed architecture. As shown in Fig. 2, the TAS are divided into four clusters. Each cluster is responsible for 32 TAS, which consists of 18 channel transducers and one front-end board. The front-ends are interconnected with the two dimensional network. The first dimension is a digital communication bus, which is responsible for the front-end configuration and synchronization. The other dimension is the amplified analog signal, which will be digitalized by the external data acquisition system (DAQ).

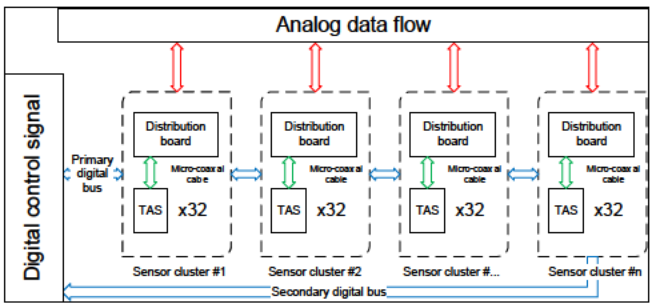

Fig. 2. System architecture

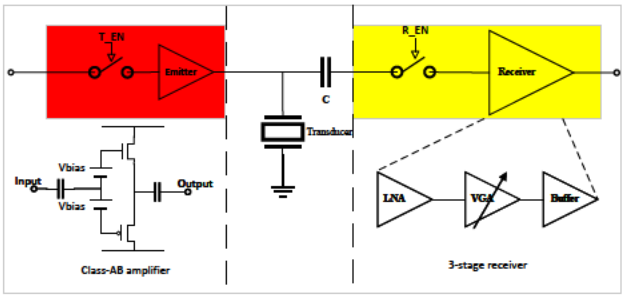

Fig. 3. Simplified single signal chain

To meet the needs of increasing transducers in the future, the system scalability is also considered in the system architecture. The system can support maximum 32 sensor clusters and up to 18,432 transducers.

III. Front-end Design

A. Analog Signal Chain

The analog signal chain of the front-end is based on a highly integrated, mixed-signal ASIC developed in commercial high-voltage Complementary Metal-Oxide Semiconductor (HV-CMOS) technology. Fig. 3 shows the simplified analog signal chain. It contains a class-AB amplifier as transmitter (TX), a 3-stage low-noise amplifier as receiver (RX) and a transmit/receive (T/R) switch.

The TX was developed as high voltage amplifier, which can amplify continuous, broadband coded excitation signals up to 120 V. The 3-stage RX amplifier has a large dynamic range to amplify low amplitude signal down to µV. The parallel RX channels are 6:1 multiplexed inside the front-end to reduce analog signal cables. The integrated ASIC allows a higher transducer density, high bandwidth, large signal dynamic range, and transducers to be transmitter (TX) and receiver (RX) at the same time.

As shown in Fig. 4 is the transceiver ASIC [5]. It is based on 350-nanometer HV-CMOS technology with a chip size of 3.3 x 4.1 mm^2. Linear high-voltage amplifiers are located at the bottom of the ASICs. In the middle is the 3-stage low-noise amplifier. At the top side, is the bias block digital to analog converter (DAC) to generate the reference voltage. The digital interface based on Serial Peripheral Interface (SPI) is used to configure the internal register for gain tuning, bias voltage adjustment, and channel selection. The average power consumption in working conditions of one ASIC is about 100 mW.

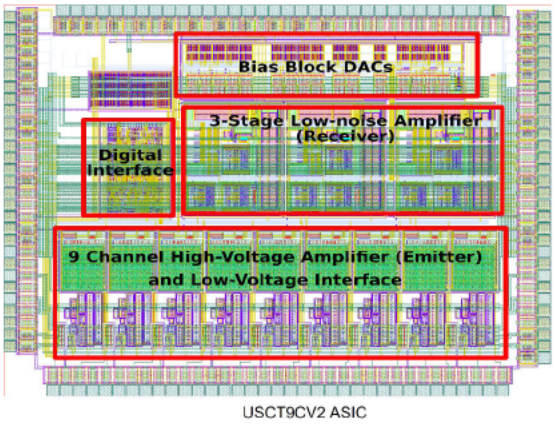

Fig. 4. ASIC layout

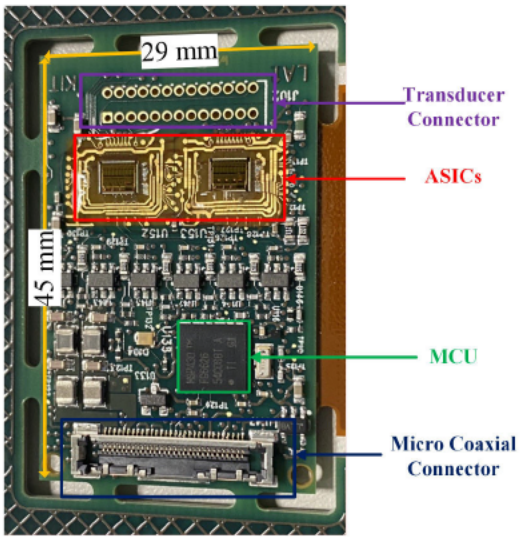

Fig. 5. Front-end layout

B. PCB Layout and Digital Interface

Fig. 5 shows the front-end layout. Each front-end consists of two ASICs. They are wedge-wedge bonded with 8-layer PCBs. 18 transducers are connected with a 2-row connector. The power, digital signal, and analog signal are transmitted by micro coaxial cables. In addition, one microcontroller (MCU) is implemented for digital communication, transducer temperature monitoring, and ASIC configuration.

The onboard MCU enables multiple front-ends to work simultaneously based on synchronization. Two different synchronization modes were implemented. The first mode is based on digital field bus communication. The front-ends are connected serially and the bus runs at 1 Mbit/s. The data acquisition system (DAQ) can configure the front-end via the digital bus for each measurement step.

Another method is a step/acknowledge. The 'step' signal is the trigger signal, which is generated by the DAQ system. All the front-ends are connected in parallel to the 'step' signal and can be triggered simultaneously. After that, the MCU will configure the ASIC with a pre-written configuration. The 'acknowledge' signal is generated by the front-end when the MCU completes the configuration.

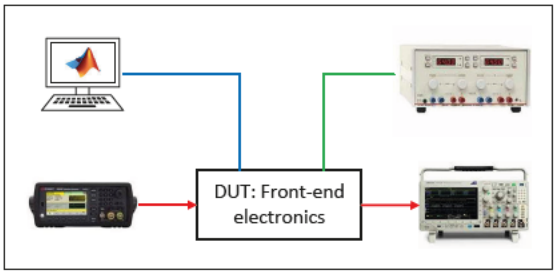

Fig. 6. Simplified test setup. DUT: Device Under Test

IV. Results

Two experiments were carried out to quantify the performance of the front-end. Firstly, characterization of the analog signals was conducted. The test environment is shown in Fig. 6. An arbitrary waveform generator generates a chirp signal (from 0.5 MHz to 7 MHz) and an oscilloscope measures the output of the front-end. A graphical user interface (GUI) developed based on MATLAB can be used to fully configure the front-end.

The second test was aimed to evaluate the digital synchronization. 128 front-ends were installed into the system. All front-ends were controlled by a data acquisition computer. One complete measurement was implemented to validate the synchronization mode.

A. Analog Characterization

We investigated gain, bandwidth, and signal-to-noise ratio (SNR) to characterize the new ASIC-based front-end design. In the TX measurement, a 1.8 V_{pp} chirp signal (0.5 MHz to 7 MHz) was amplified to 63 V_{pp}. The TX's spectrum diagram (Fig. 7) was based on 100 output channels of the transmitter amplifier, which conducts to 30.9 dB amplification of the TX amplifier. In addition, the TX amplifier can achieve 6.5 MHz bandwidth with 0.65 MHz deviation.

In the RX characterization (Fig. 8), a 2 mV_{pp} chirp signal (0.5 MHz to 7 MHz) was applied to the 3-stage RX amplifier. It

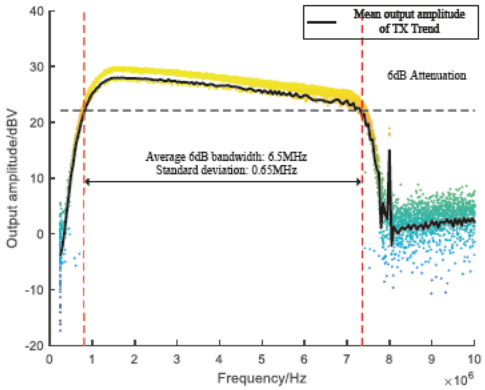

Fig. 7. Spectrum diagram of TX amplifier

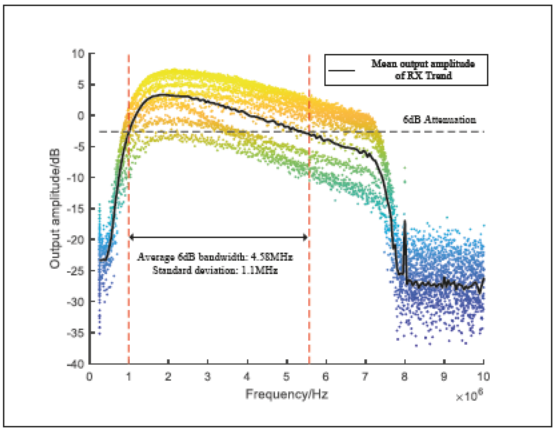

Fig. 8. Spectrum diagram of RX amplifier

shows 4.6 MHz bandwidth at 54 dB amplification. Compared to the diagram spectrum of TX, the RX amplifier shows large gain variation. In addition, the output SNR (37.6 dB on average with 2.7 dB standard deviation) of the RX amplifier is shown in Fig. 9.

B. Digital Synchronization

In this test, the entire transducer array with 128 front-ends was built up. The complete measurement was implemented on synchronization based on digital communication and step/acknowledge procedure. Table 1 lists the calculation of 2 synchronization modes. The step/acknowledge mode can reduce the overhead of each measurement step from 195.5 ms to 0.5 ms. In one complete measurement, the step/acknowledge procedure takes 55.3 s, which speeds up the measurement with a factor of 48.9.

Fig. 10 presents the 3D transducer array in one measurement step. TAS 21, transducer 12 was selected as an emitter. The other transducers were selected as receivers. The sound pressure of the transducers was normalized and color-coded

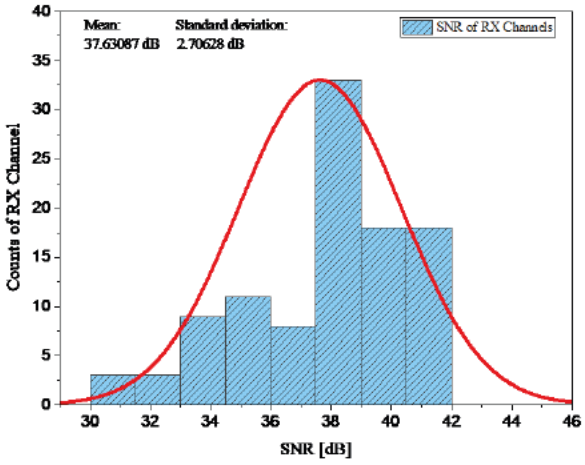

Fig. 9. SNR histogram of RX amplifiers

TABLE I
SYNCHRONIZATION MODE COMPARISON

	Digital Communication	**Step/Acknowledge**
Calculation formula for the time of one complete measurement	$(N_{dc} \times t_{dc} + t_{daq}) \times N_{step}$	$(t_{sa} + t_{daq}) \times N_{step}$
N_{dc} **(Communication times for one step)**	128	-
t_{dc} **(Configuration time for one front-end via digital communication)**	1.5 ms	-
t_{daq} **(Data acquisition time)**	3.5 ms	3.5 ms
t_{sa} **(Configuration time for one front-end via step/acknowledge)**	-	0.5 ms
N_{step} **(Steps for one complete measurement)**	13824	13824
Time of one complete measurement	2703 s	55.3 s

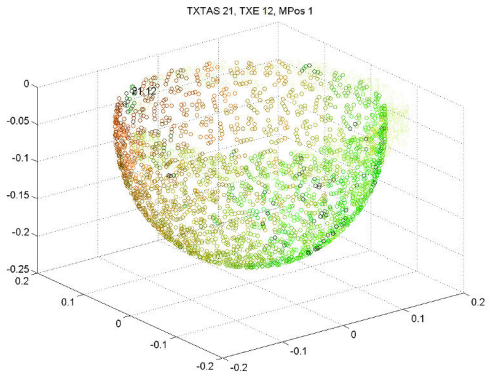

Fig. 10. Visualized 3D transducer array

(green (0) to red (1)). The attenuation of the sound pressure is also in line with the increment in propagation distance.

V. CONCLUSION AND DISCUSSION

We designed and tested the front-end for 3D ultrasound tomography. Due to the distributed structure, the front-end can be tightly coupled with the transducers. The ASIC enables our front-end to have large bandwidth, and to support coded excitation signal. In addition, the synchronization modes based on digital communication can manage thousands of transducers to work simultaneously.

In the future, we will optimize the digital communication to decrease the measurement time to arrive 10 seconds and also focus on a calibration method for the system channels, which are promising to decrease the gain variation for receiving amplifiers.

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