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The optimization of graphene field effect transistors (GFETs) for high frequency applications requires further understanding of the physical mechanisms concerning charge carrier transport at short channel lengths. Here, we study the charge carrier transport in GFETs with gate lengths ranging from 2 μm down to 0.2 μm by applying a quasi-ballistic transport model. It is found, that the carrier mobility, evaluated via the drain-source resistance model including geometrical magnetoresistance effect, is more than halved with decreasing the gate length in the studied range. This decrease in mobility is explained by the impact of ballistic charge carrier transport. The analysis allows for evaluation of the characteristic length, a parameter of the order of the mean free path, which is found to be in the range of 359-374 nm. The mobility term associated with scattering mechanisms is found to be up to 4456 cm^2/Vs. Transmission formalism treating the electrons as purely classical particles allows for the estimation of the probability of charge carrier transport without scattering events. It is shown, that at the gate length of 2 μm approximately 20 % of the charge carriers are moving without scattering, while at the gate length of 0.2 μm this number increases to above 60 %.

INTRODUCTION

The future progress in modern electronics partly relies on the development of novel materials with improved charge carrier transport properties, such as graphene.[1,2] The extremely high carrier mobility and saturation velocity in graphene could possibly enable much faster electronics compared to traditional semiconductors. Graphene has already demonstrated high potential as channel material in advanced graphene field-effect transistors (GFETs), specifically for high frequency applications.[3,4] However, full realization of the capabilities of the high-frequency GFETs requires better understanding of the charge carrier transport mechanisms, which will allow for optimization of device design and layout, as well as operational conditions. In the majority of the previous works, the high-frequency performance of GFETs was analyzed using the drift-diffusion theory of charge carrier transport assuming that the intrinsic transit (cutoff) frequency is limited by the saturation velocity (v_{sat}) as $f_{\mathrm{T}} = \frac{v_{\mathrm{sat}}}{2\pi L}$, where L is the gate length.[5–7] It was shown theoretically that, in the typical GFET structures, the saturation velocity is limited by the remote optical phonons of the adjacent dielectrics, *e.g.*, SiO_2 layer on surface of Si substrate, which phonon energy is significantly less than that of the longitudinal zone boundary phonons of intrinsic graphene (160 meV).[8,9] Therefore, for further increasing f_{T}, selecting the dielectric materials with higher phonon energies was suggested.[6,8] This approach was verified experimentally using encapsulation by hBN, Al_2O_3 buffer layer, or diamond substrate resulting in increased saturation velocity and transit frequency.[5,10,11] The approach apparently reaches its limit in the GFETs based on graphene encapsulated by diamond-like carbon (DLC) layers, since the surface phonon energy of DLC (165 meV) is slightly higher than that of graphene.[12] Thus, the remaining obvious way of further increasing f_{T} is continuing scaling down the gate length. However, the above analysis and conventional relationship between the f_{T} and L, *i.e.* derived using the drift-diffusion theory, might not be valid for GFETs with relatively short gate lengths due to contribution of the ballistic mode in the charge carrier transport.[13] In particular, in the purely ballistic mode, the saturation velocity in the above relationship should be replaced by a Fermi velocity or virtual source injection velocity.[13,14] For comparison, it was predicted, that in short channel (submicron) high-electron-mobility transistors, the effective, *i.e.*, measured, mobility must be much smaller than that in long channel devices, which was related to the ballistic transport.[15] There is relatively limited number of publications analyzing the ballistic charge carrier transport in GFETs. The reduction of the effective mobility in the GFETs with gate lengths shorter than 1-2 μm was reported in Refs.[14,16–18] In Refs.[14,17] the observed reduction of the mobility was associated with the quasi-ballistic transport and by using the concept of ballistic mobility,[15] the mean free path was found to be in the range of 175-400 nm. However, the reported data and analysis do not allow for conclusion to which extent the ballistic motion contributes to the total charge carrier transport in the GFETs. For comparison, in Ref.[19], electron mobility in quasi-ballistic Si metal–oxide–semiconductor field-effect transistors was analyzed using the concept of ballistic mobility and the transmission formalism, which allowed for evaluation of the transmission probability and estimation of fraction of the total number of ballistic electrons.[20]

In this work, we apply the concept of ballistic mobility and the transmission formalism to study the charge carrier transport in GFETs with different gate lengths in the range 0.2-2.0 μm. Comparative analysis of collision and ballistic mobility parameters allows us to clearly illustrate the transition of the charge carrier transport from the scattering regime through the quasi-ballistic to the purely ballistic regime.

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DEVICE FABRICATION AND MEASUREMENTS

The GFETs studied in this work have layout similar to those previously published,[21] *i.e.*, with dual-gate fingers centered between source and drain contacts separated by 100 nm long ungated regions. The layout and design are optimized for high-frequency performance of the GFETs taking into account the following considerations and conditions. As shown in introduction, the f_T, which is the device high-frequency figure of merit, is inversely proportional to the gate length, *i.e.*, charge carriers transit time. This relationship is a driving force of the scaling down, *i.e.*, implies that the L should be as short as possible. Analysis of extrinsic f_T indicates that, relatively large gate width and two gate fingers should be used to minimize the effects of the pad capacitances. Current optimal design and technology utilize the two gate fingers with total gate width of 30 μm. In the dc analysis of this work, only one gate finger is used. Analysis indicates also that the ungated regions should be as short as possible to minimize the effect of the total series resistance. With current technology the ungated regions of 100 nm are used, which is the lower limit defined by the e-beam lithography in this fabrication process flow. To minimize the resistance of the graphene-metal junctions, the overlapping of the drain and source electrodes with edges of the graphene in the channel direction is designed to be 10 μm, *i.e.* sufficiently larger than the transfer length, which is typically below 0.25 μm.[22] The top gate configuration of the GFETs is used with the aim to minimize the parasitic gate-source and gate-drain capacitances. In the current planar gate technology, a relatively thick gate electrode composed by 10 nm/300 nm Ti/Au layers is used to minimize the limiting effect of the gate resistance on the extrinsic maximum frequency of oscillations. In the optimized GFET design used in this work, the thickness of the SiO_2 layer on top of the Si substrate is increased up to 1 μm with the aim to reduce the parasitic pad capacitances. The above improvements in the design allowed for development and demonstrating GFETs with state-of-the-art high-frequency performance.[23] Fig. 1 (a) shows an optical microscope image of a fabricated device, where source, drain, and gate pads are indicated. Fig. 1 (b) shows a 3D schematic illustration of a cross-section of the gate region describing the material of the different layers. Several sets of GFETs with gate length ranging from 2 μm down to 0.2 μm and one finger gate width (W) of 15 μm were fabricated on a Si wafer.

The GFETs were fabricated using processing steps based on the previously developed technology optimized for improving high-frequency performance via preserving graphene intrinsic properties by encapsulation at initial stage of fabrication and reducing the contact resistance.[23,24] The very detailed recipe of the processing used in this work is given in Ref.[25] Fig. 2 shows main steps of the GFET fabrication summarized below. In the first step, graphene prepared by Graphenea using chemical vapor deposition (CVD) was transferred onto high resistivity silicon/silicon oxide (Si/SiO_2) substrate, with a SiO_2 thickness of 1 μm, using the Easy Transfer approach.[26] After the transfer, with the aim to remove water molecules absorbed on the surface and trapped at the interface,

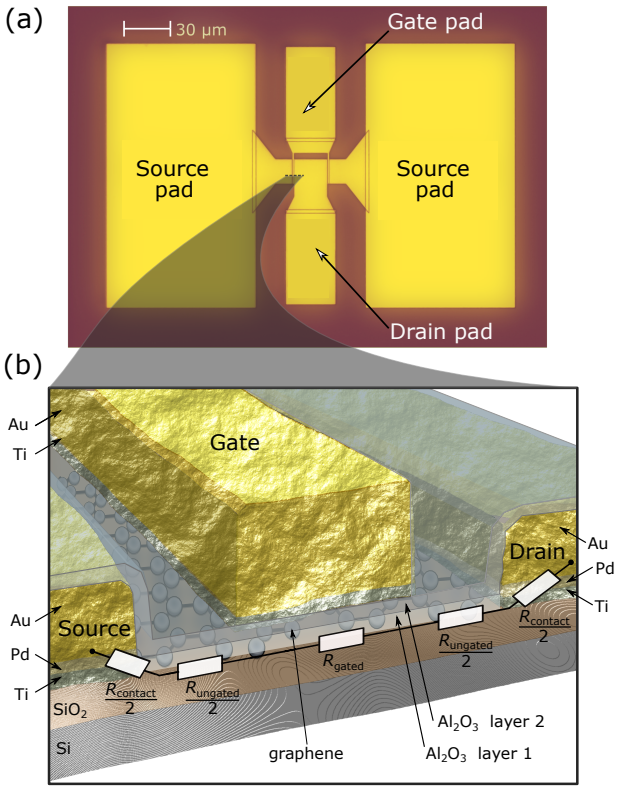

FIG. 1. (a) An optical microscope image of a fabricated device with the source, drain, and gate pads indicated. (b) A 3D schematic illustration of a cross-section area of a gate finger showing materials of different layers and total resistance equivalent circuit.

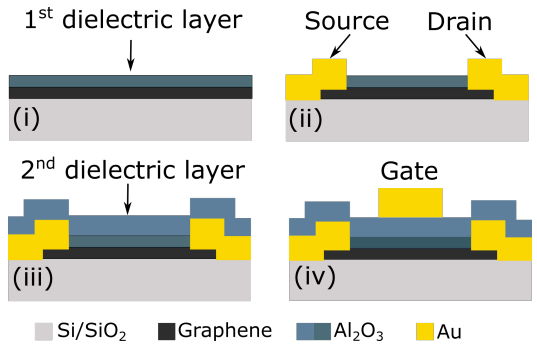

FIG. 2. Main steps of the GFET fabrication. (i) Formation of the 1st dielectric layer, (ii) patterning of the dielectric/graphene mesa and formation of the source and drain contacts, (iii) deposition of the 2nd dielectric layer, and (iv) formation of the gate electrodes and source, along with the drain contact pads. Labels S, D and G indicate source, drain and gate electrodes, respectively.

the graphene was dried on hotplate, first at low temperature of approx. 47°C until its color changed, then at higher temperature of 150-160°C to get rid of water bubbles. After that, the graphene was placed in vacuum chamber for 2-3 days with the aim to remove completely the residual water molecules. The transferred graphene film was covered by an approximately

8 nm thick Al_2O_3 layer obtained by six times repetitive deposition of 1 nm thick Al film and its subsequent oxidation on a hotplate at 160°C for 5 minutes. This layer constitutes the 1st layer of the gate dielectric, which encapsulates the graphene protecting it from contamination throughout the subsequent fabrication steps. In the following step the graphene/dielectric mesa and, subsequently, the openings in the Al_2O_3 layer for the drain/source contacts were patterned via e-beam lithography. The drain/source contacts were formed by deposition of 1 nm Ti/15 nm Pd/250 nm Au and the use of a standard lift-off process. After this, the approximately 14 nm thick 2nd gate dielectric layer of Al_2O_3 was formed by repeating ten times the process described above, which results in the total gate dielectric thickness (d_g) of approximately 22 nm. The 2nd dielectric layer covers the graphene edges exposed at the mesa sidewalls, which prevents short-circuiting by the overlapping gate fingers. As it can be seen from Fig. 2 (iv), the 2nd gate dielectric layer serves also as a passivation layer for the ungated regions, which prevents degradation of the corresponding part of the series resistance due to interaction with ambient, *e.g.*, absorbing water. Again, this improvement of the design and technology is experimentally verified by demonstrating GFETs with state-of-the-art high-frequency performance.[23] Finally, the gate electrodes and the contact pads were fabricated by e-beam lithography and deposition of 10 nm Ti/290 nm Au by e-beam evaporation followed by a standard lift-off process. Notice that before metal deposition in the openings of the source and drain contact areas, the 1st dielectric layer, which separates the graphene from the lithographic resist, is etched off by the buffered oxide etch (BOE) for metal/graphene ohmic contact formation. Apparently, this process allows for the effective removal of e-beam resist residues, providing a rather clean interface between the graphene and the metal and resulting in an extremely low specific-width contact resistivity of the graphene/metal junctions below 100 $\Omega \times \mu$m.[23,24] The specific-width contact resistivity have been evaluated via analysis of the GFET transfer characteristics and its low value confirmed by measurements using the multi-terminal transfer length method.[24,27] As it can be seen from Fig. 2, the graphene/metal contacts are made in the conventional top, or planar type, configuration. The measured specific-width contact resistivity is close to the theoretical limit of 88 $\Omega \times \mu$m for the planar contacts and comparable or even lower than that reported for the side, or edge type, contacts.[28,29] The effectiveness of removal of the e-beam resist residues in the source/drain contact openings have been confirmed by comparative study of the Raman spectra of the as-transferred graphene, graphene in the Al_2O_3 openings made by BOE and graphene in the e-beam resist openings made by a standard developer.[27] A feature of the GFET processing used in this work is formation of the Al_2O_3 gate dielectric by sequential deposition of 1 nm thick Al films followed by its oxidation on a hot plate at 160°C for 5 min. in ambient conditions, *i.e.*, ex-situ, without involving the atomic layer deposition (ALD). The high quality of the gate dielectric was confirmed by measurements of the permittivity using Corbino disc test structures similar to that reported in Ref.[30] The permittivity is found to be approximately 7.5, which is higher than approximately 6.5 typical for the 20 nm thick Al_2O_3 made by ALD.[31]

Fig. 1 (b) also shows the equivalent circuit of the total drain-source resistance (R_{total}). The R_{gated} and $\frac{1}{2} \times R_{ungated}$ are resistances of the gated and ungated regions of the channel, respectively. The $\frac{1}{2} \times R_{contact}$ is the contact resistance associated with a graphene-metal junction. The contact resistance also includes the probe and cable resistances (not shown in Fig. 1). The resistances of the ungated regions and contact resistances constitute the total series resistance as $R_{series} = R_{ungated} + R_{contact}$, and the total drain-source resistance can be expressed as $R_{total} = R_{series} + R_{gated}$. The transfer characteristics, *i.e.*, drain current (I_{DS}) versus gate voltage (V_{GS}), of the GFETs were measured in common source configuration at the drain voltage V_{DS} = -0.1 V using a Keysight B1500A parameter analyzer on a Cascade summit 12000 semi-automatic probe station. The drain-source resistance was calculated as $R_{total} = \frac{V_{DS}}{I_{DS}}$.

RESULTS AND DISCUSSION

Fig. 3 shows a typical dependence of the total drain-source resistance on the gate voltage of a GFET with the gate length of 1 μm. The mobility (μ_{eff}) in GFETs is usually extracted from the drain-source resistance model as

$$R_{total} = R_{series} + \frac{L}{W}\frac{1}{\mu_{eff} e}\frac{1}{\sqrt{n_0^2 + \left((V_{GS} - V_{Dir})\frac{C_g}{e}\right)^2}}, \quad (1)$$

where e is the elementary charge, n_0 is the residual concentration of the charge carriers, V_{Dir} is the Dirac voltage and C_g is the gate capacitance per unit area.[8,32] It can be shown that under the conditions used in our experiments, the graphene quantum capacitance can be ignored.[32] In the common approach the μ_{eff}, n_0 and R_{series} are used as fitting parameters with the μ_{eff} being of a target parameter, *i.e.*, main parameter to be found in this case. The C_g is usually associated with the capacitance of the gate oxide dielectric $C_{ox} = \frac{\varepsilon\varepsilon_0}{d_g}$, where the ε_0 is the vacuum permittivity and ε is the dielectric constant of the gate dielectric. We assume that, $\varepsilon \approx 7.5$, which gives $C_g = C_{ox} \approx 3.0 \times 10^{-3}$ F/m^2. Fig. 3 shows the fitting curve obtained using Eq. (1) with corresponding parameters presented in Table I in the row where mobility indicated as target parameter. It can be seen, that the very good fitting is obtained. The mobility is found to be 1777 cm^2/Vs. However, in our recent studies using the geometrical magnetoresistance (gMR) effect, we demonstrated that the mobility found assuming $C_g = C_{ox}$ can be significantly underestimated.[21] In particular, the average value of the gMR mobility of the same GFET, was found to be 3492 cm^2/Vs. We explained this by contribution of the interfacial capacitance, which significantly reduces the gate capacitance in comparison with that given by the oxide dielectric only. This agrees well with results of our previous studies using the delay time analysis and analysis of the capacitance-voltage dependencies in the GFETs.[33] Therefore, in this work the drain-source resistance model given by Eq. (1) is instead used to extract the gate capacitance with

the average mobility value found via the gMR effect, *i.e.*, 3492 cm^2/Vs. In this case, the gate capacitance per unit area is found to be 1.6×10^{-3} F/m^2, which is almost 2 times lower than the C_{ox}. Fig. 3 shows result of the fitting with the parameters given in Table I in the row where the C_g is indicated as target parameter. It can be seen, that almost identical fitting is obtained. Below, in the analysis of the charge carrier transport in GFETs applying a quasi-ballistic transport model, we use the mobility values found via fitting of the drain-source resistance model (Eq. (1)) with mobility as target parameter, for both values of the $C_g = 3.0\times10^{-3}$ F/m^2 and 1.6×10^{-3} F/m^2, for comparison.

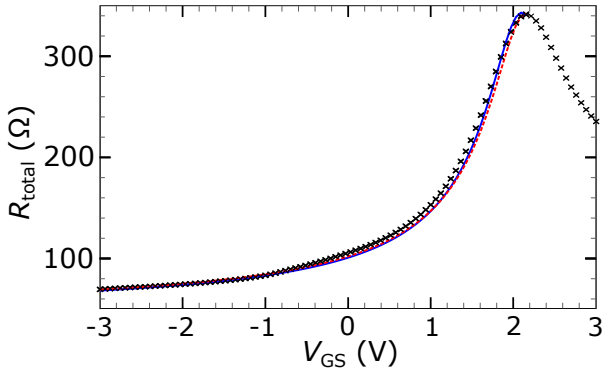

FIG. 3. Drain-source resistance (crosses) vs gate voltage of a GFET with the gate length of 1 μm obtained from measured transfer characteristic. The dashed line represents fitting by the drain-source resistance model, Eq. (1), in the common approach, *i.e.*, using the μ_{eff}, n_0 and R_{series} as fitting parameters with the μ_{eff} being of a target parameter and using $C_g = C_{ox} = 3.0\times10^{-3}$ F/m^2. The solid line represents fitting by the drain-source resistance model, Eq. (1), in the modified approach, *i.e.*, using the C_g, n_0 and R_{series} as fitting parameters with the C_g being of a target parameter and assuming μ_{eff} = 3492 cm^2/Vs found from the gMR effect.[21] The fitting parameters are presented in Table I.

TABLE I. Parameters used in the drain-source resistance model fitting in Fig. 3.

Target	μ_{eff} (cm^2/Vs)	R_{series} (Ω)	n_0 (10^{15} m^{-2})	C_g (10^{-3} F/m^2)
μ_{eff}	1777	45	10	3.0
C_g	3492	45	4.3	1.6

It was shown that in the quasi-ballistic regime, the measured, *i.e.*, effective, mobility can be expressed using Mathiessen's rule as[13,15,19,34]

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + \frac{1}{\mu_{ballistic}}, \tag{2}$$

where μ_0 is the mobility resulting from all scattering mechanisms, which would be measured in a long device under collision-dominated conditions, and termed as collision mobility in the analysis below. $\mu_{ballistic}$ is a length-dependent "ballistic" mobility. For a degenerate two-dimensional electron gas the ballistic mobility is given by[13]

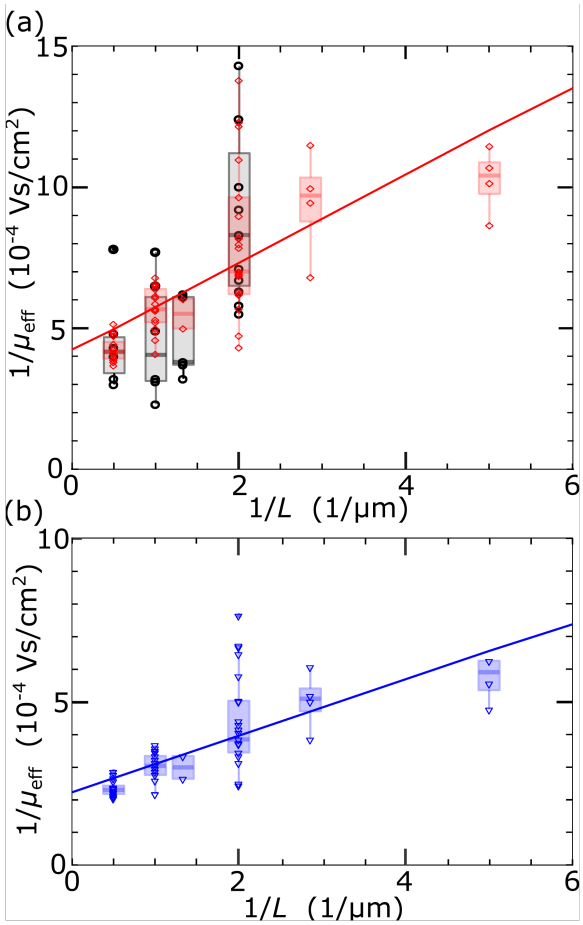

FIG. 4. Reciprocal of effective mobility vs reciprocal of gate length found using drain-source resistance model, Eq. (1), assuming $C_g = 3.0\times10^{-3}$ F/m^2 (a) and 1.6×10^{-3} F/m^2 (b) for sets of GFETs measured at each gate length. Shown in (a) are also data from Ref.[24] (circles), for comparison. The data are shown also in the box plot formats illustrating distributions. The straight lines are linear fits. The edges of the boxes indicate the 25th and 75th percentile values, while the short lines within the boxes indicate the median values.

$$\mu_{ballistic} = \frac{2qL}{\pi m v_F}, \tag{3}$$

where m is the effective mass and v_F is the Fermi velocity. The ballistic mobility parameter is not a real "physical" mobility, since the mobility concept relates to the collision-dominated regime.[15,34] The linear dependence of the $\mu_{ballistic}$ on L reflects the fact that the resistance of the purely ballistic device does not depend on the device length since there is no electric field in the channel, *i.e.*, gated and ungated regions and the applied voltage drops only in the graphene/metal contact areas where the scattering takes place.[13,19,20] Using Eq. (3), Eq. (2) can be rewritten as[14,19]

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + \frac{\lambda_B}{\mu_0}\frac{1}{L}, \tag{4}$$

where $\lambda_B = \frac{\mu_0 \pi m v_F}{2q}$ is the characteristic length of the order of

the mean free path.[14,19] Note, that this expression is obtained using Eq. (3) derived for a degenerate two-dimensional electron gas[13] and can be applied for graphene at the conditions of non-zero effective mass in doped graphene, *e.g.*, outside the Dirac point and at non-zero temperature.[35] The λ_B corresponds to the length on which the ballistic transport becomes significant, *e.g.* at $L = \lambda_B$ the effective mobility $\mu_{eff} = \frac{\mu_0}{2}$.[19] The λ_B is introduced in the works by Lundstrom *et al.* as the near-equilibrium mean-free-path for backscattering and the expression equivalent to Eq. (4) is derived.[34,36] It can be seen from Eq. (4) that a plot of $\frac{1}{\mu_{eff}}$ versus $\frac{1}{L}$ will be a straight line giving an interception with the y-axis at $\frac{1}{\mu_0}$ and having a slope of $\frac{\lambda_B}{\mu_0}$.[14]

Fig. 4 (a) and Fig. 4 (b) show plots of $\frac{1}{\mu_{eff}}$ versus $\frac{1}{L}$ for the GFETs in this work with mobilities found using the drain-source resistance model, Eq. (1), and assuming the $C_g = 3.0 \times 10^{-3}$ F/m^2 and 1.6×10^{-3} F/m^2, respectively. The data are shown also in the box plot formats illustrating the data distribution and allowing for statistical analysis. The edges of the boxes indicate the 25th and 75th percentile values, while the short lines within the boxes indicate the median values. According to our analysis, the error in evaluation of the λ_B is caused mainly by error in the straight-line fitting of the data in the $\frac{1}{\mu_{eff}}$ versus $\frac{1}{L}$ format made by a MATLAB code. Comparison with the best manual fit shows that the error in evaluation of the λ_B is less than 5 % in all cases. It can be seen from Fig. 4 that the 5 % error is significantly less than the dispersion of data due to surface distribution of the graphene properties, which, as shown below, is caused by Coulomb inhomogeneities and, hence, can be ignored. The values at $L = 0.5$ μm looks more scattered because the corresponding sample data set is intentionally larger. The reason is that the GFETs with this specific gate length were simultaneously used in more comprehensive studies for development of the integrated 10 GHz GFET amplifiers.[37] Fig. 4 (a) also shows the data from our previous work,[24] for comparison. The GFETs reported in Ref.[24] were fabricated by similar technology, using a different CVD graphene. The effective mobility values found in this work reveal comparable or even smaller distribution of the GFETs with similar gate lengths, compared to Ref.[24] The distribution of the mobility is usually explained by the spatially inhomogeneous screened Coulomb potential caused by charged defects and impurities.[38] The charged defects/impurities can be created during the GFET processing either in the graphene or adjacent dielectrics and usually associated with the water molecules trapped at the graphene/substrate interface or with the oxygen vacancies in the gate dielectric.[39–42] It was shown with terahertz time-domain spectroscopy that the mobility can be distributed in the range of approximately 600-1400 cm^2/Vs even in the bare CVD graphene.[43] For comparison, even in the GFETs based on the exfoliated graphene, *i.e.*, with potentially much cleaner graphene interfaces than that on the CVD graphene, the dispersion in the dependence of the measured mobility on the gate length with even relatively limited number of the experimental points can be up to 50 %.[17] One can expect that with a larger sample data set the dispersion will be correspondingly larger, *e.g.*, as it can be seen in Fig. 4 at $L = 0.5$ μm. According to the self-consistent theory, the mobility limited by Coulomb scattering depends only on the charged impurity concentration and the dielectric constant of the substrate.[38] The charged impurity concentration (n_{imp}) plainly defines the residual concentration of the charge carriers as $n_0 = 0.2 \times n_{imp}$ for graphene on SiO_2.[44–46] According to the theory, the product of the mobility and the residual carrier concentration is constant, and for graphene on the SiO_2 is $n_0 \times \mu_{eff} \approx 1.5 \times 10^{15}$ V^{-1}s^{-1}.[44–46] Fig. 5

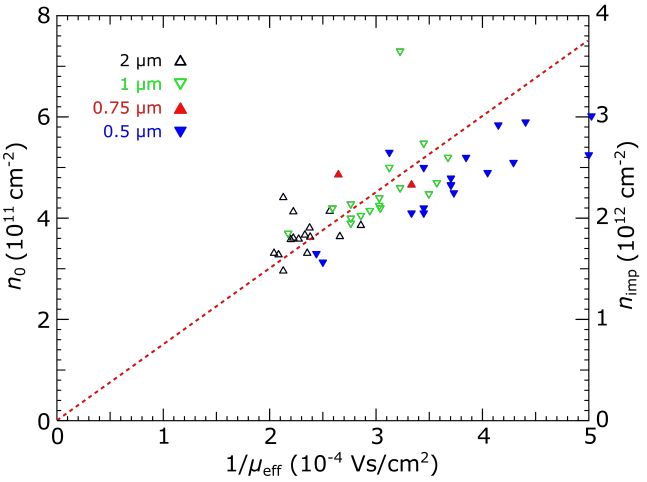

FIG. 5. Residual concentration of charge carriers (n_0) and concentration of charged impurities (n_{imp}) versus reciprocal of effective mobility, found using drain-source resistance model, Eq. (1), assuming $C_g = 1.6 \times 10^{-3}$ F/m^2, in the GFETs with gate lengths of 2 μm (△), 1 μm (▽), 0.75 μm (▲), and 0.5 μm (▼), located at different positions on the Si wafer. The line corresponds to the product $n_0 \times \mu_{eff} = 1.5 \times 10^{15}$ V^{-1}s^{-1}.

shows the n_0, found as fitting parameter in the drain-source resistance model, Eq. (1), assuming $Cg = 1.6 \times 10^{-3}$ F/m^2, and the n_{imp}, calculated using the above relationship, versus the $\frac{1}{\mu_{eff}}$ for the GFETs with different gate lengths located at different positions on the Si wafer. It can be seen, that the data can be fitted by the straight line corresponding to the product $n_0 \times \mu_{eff} \approx 1.5 \times 10^{15}$ V^{-1}s^{-1}, indicating that the Coulomb scattering dominates. The deviation from the straight line at the $\frac{1}{\mu_{eff}}$ above approximately 4×10^{-4} Vs/cm^2, *i.e.*, corresponding lower mobility values, can be explained by increasing contributions of the additional scattering mechanisms, *e.g.*, short range scattering associated with neutral defects and graphene ripples.[44] Alternatively, it can be explained by decreasing the μ_{eff} at shorter gate length due to increasing contribution of the quasi-ballistic transport, as shown below.

Fig. 4 clearly reveals a reduction of mobility with shorter gate length, which manifests the contribution of the ballistic motion to the charge carrier transport. The fact that the data from Ref.[24] show similar dependence on the gate length again supports results of this work. The straight lines in Fig. 4 are linear fits giving, in accordance with Eq. (4), $\mu_0 = 2389$ cm^2/Vs and 4456 cm^2/Vs, while $\lambda_B = 374$ nm and

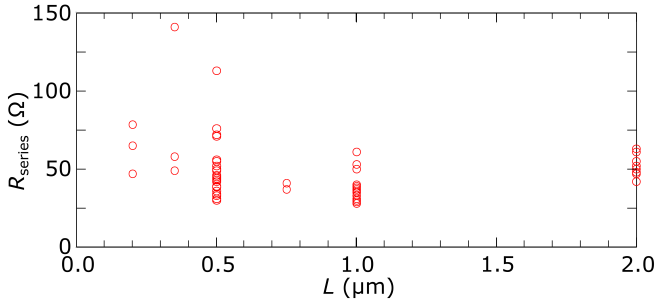

FIG. 6. Series resistance, found as fitting parameter of the drain-source resistance model assuming $C_g = 1.6 \times 10^{-3}$ F/m^2, versus gate length.

359 nm for $C_g = 3.0 \times 10^{-3}$ F/m^2 and 1.6×10^{-3} F/m^2, respectively. For comparison, the μ_0 and λ_B found using the ambipolar virtual source model and a similar analysis of the $\frac{1}{\mu_{eff}}$ versus $\frac{1}{L}$ characteristics using Eq. (4) are reported to be 2702 cm^2/Vs and 175 nm.[14] The larger values of the characteristic length found in our work can be explained by a higher quality of graphene, which should be associated with higher mobility. This indicates that the calculation of the mobility using the gate capacitance accounting for the interfacial states is more accurate, since it results in higher effective mobility. The values of the characteristic length found in this work agree well with that of 300 ± 100 nm reported in Ref.[17] In Ref.[17] the collision mobility evaluated via measurement of transconductance was found to be up to 3500 cm^2/Vs, which is also closer to that found in this work. The similarity of the values of the mobility and mean free path reported in Ref.[17] and those found in this work allows for conclusion that the methodology is reproducible and, hence, accurate enough.

Fig. 6 shows the R_{series}, found as the fitting parameter of the drain-source resistance model (Eq. (1)) with the $C_g = 1.6 \times 10^{-3}$ F/m^2, versus gate length. As it can be seen, the R_{series}, does not reveal any remarkable dependence on L in the studied range. This confirms, that the observed changes in R_{total} with the scaling down are governed mainly by the reduction of the μ_{eff} due to contribution of the quasi-ballistic charge carrier transport. In our previous works, we demonstrated correlations of both $R_{ungated}$ and $R_{contact}$ with the low-field mobility, associated with concentration of the charged impurities at the graphene interfaces and in the adjacent dielectrics.[24] Thus, the visible distributions of the R_{series} at certain gate lengths, again, can be explained by the spatially inhomogeneous screened Coulomb potential caused by charged defects and impurities.

Knowing the μ_0 allows for the calculation of all mobility terms in Eq. (2). Fig. 7 shows the mobilities plotted versus gate length. The μ_{eff} is calculated as a reciprocal of the linear fits in Fig. 4. This plot clearly illustrates the transition of the charge carrier transport from the scattering regime through the quasi-ballistic to the purely ballistic regime with a reduction of the gate length. It can be seen that the scattering regime fully dominates above $L \approx 4$ μm when the $\mu_{ballistic}$ is approximately 10 times larger than the μ_0. In the quasi-ballistic regime, which occurs when L is similar to λ_B (≈ 0.4 μm), $\mu_{ballistic}$ is of the same order as μ_0. The almost purely ballistic transport occurs below $L \approx 0.04$ μm when the $\mu_{ballistic}$ is approximately 10 times smaller than the μ_0. Transmission

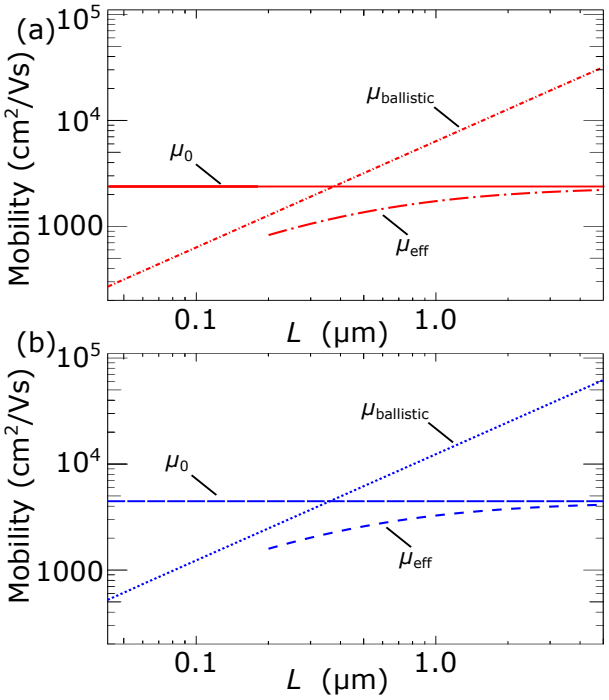

FIG. 7. Effective, collision and ballistic mobility vs gate length calculated using Eq. (2) and Eq. (4) assuming $C_g = 3.0 \times 10^{-3}$ F/m^2 (a) and 1.6×10^{-3} F/m^2 (b).

formalism treating the electrons as purely classical particles, *i.e.*, neglecting any quantum effects, gives the transmission probability through a conductor of length L by[20]

$$T = \frac{\lambda_B}{L + \lambda_B}. \tag{5}$$

A similar expression is derived in the Lundstrom-model for the backscattering coefficient.[36] In our case the T is equal to the probability that a charge carrier moves without scattering. In the purely ballistic regime $T = 1$, while in the quasi-ballistic regime T is smaller than 1, and much less than 1 for diffusive transport. Thus, the T can be considered as a measure of the ballisticity of a device.[19] Fig. 8 shows the transmission probability versus gate length calculated for our GFETs using Eq. (5), for both $C_g = 3.0 \times 10^{-3}$ F/m^2 and 1.6×10^{-3} F/m^2. The similarity of the T for both values of the C_g indicates relatively low sensitivity of the transmission probability calculated using Eq. (5) to the rather large uncertainty of the gate capacitance in the range studied in this work. One can explain it as follows. Combining Eqs. (4) and (1), at high enough V_{GS}, the transmission probability can be expresses as

$$T = 1 - \frac{\mu_{eff}}{\mu_0} = 1 - \frac{\frac{\partial I_{ds}^{eff}}{\partial V_{ds}}}{\frac{\partial I_{ds}^{0}}{\partial V_{ds}}} \frac{C_g^0}{C_g^{eff}} = 1 - \frac{g_{ds}^{eff}}{g_{ds}^{0}} \frac{C_g^0}{C_g^{eff}}, \tag{6}$$

where I^0_{ds}, g^0_{ds}, C^0_g and I^{eff}_{ds}, g^{eff}_{ds}, C^{eff}_g are the drain current, drain conductance and gate capacitance per unit area in a long device and in the quasi-ballistic regime, respectively; V_{ds} is the drain voltage dropped on the gated region. One can assume that the gate capacitance per unit area does not depend on the gate length, *i.e.*, $C^0_g = C^{eff}_g$ and, therefore,

$$T = 1 - \frac{g^{eff}_{ds}}{g^0_{ds}} \tag{7}$$

Thus, both T and, following Eq. (5), λ_B do not depend on the gate capacitance, *i.e.*, concentraton of the charge carriers, and are governed only by the response of the drain current to the variations of the drain field, *i.e.*, by contribution of the ballistic charge carriers. It can be seen from Fig. 8, that at $L = 2$ μm, approximately 20 % of the charge carriers are moving ballistically. At L = 0.2 μm this number increases to above 60 %. However, one should take into account that at such short gate lengths other mechanisms, like direct quantum tunnelling between source and drain, may contribute and govern the charge carrier transport.[19]

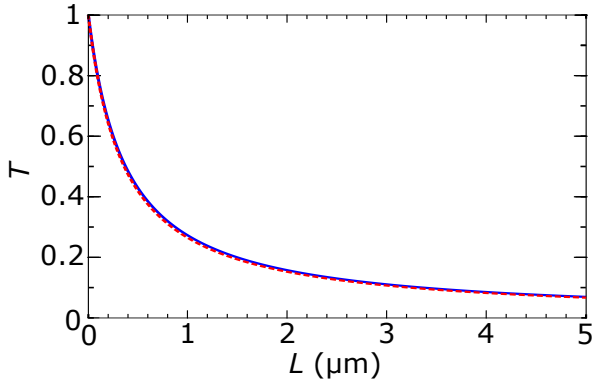

FIG. 8. Transmission probability vs gate length calculated using Eq. (5) assuming $C_g = 3.0 \times 10^{-3}$ F/m ^{2} (dashed line) and 1.6×10^{-3} F/m^2 (solid line).

CONCLUSION

In conclusion, we found that effective mobility in the GFETs is more than halved with decreasing the gate length from 2.0 μm down to 0.2 μm. The effective mobility was evaluated via the drain-source resistance model with gate capacitance corrected using the geometrical magnetoresistance effect. The observed reduction of the effective mobility is associated with contribution of the ballistic motion to the charge carrier transport. We applied the concept of the ballistic mobility and found the carrier mean free path to be in the range of 359-374 nm. Analysis indicated that the scattering regime fully dominates at gate lengths larger than 4 μm. At gate lengths similar to the mean free path, the quasi-ballistic regime occurs. The almost purely ballistic transport dominates at gate lengths below 0.04 μm. By applying transmission formalism, we evaluated the transmission probability, *i.e.*, probability of transport without collisions, and found that at the gate length of 2 μm approximately 20 % of the charge carriers are moving ballistically. At the gate length of 0.2 μm this number increases to above 60 %. The transmission probability was found to be relatively low sensitive to the variation of the gate capacitance studied in this work. Clarifying contribution of the ballistic motion to the charge carrier transport will allow for further development of GFETs, in particular, for advanced high-frequency applications.

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[1] A. K. Geim and K. S. Novoselov, "The rise of graphene," Nat. Mater. **6**, 183–191 (2007).
[2] A. Castro Neto, "The electronic properties of graphene," Reviews of Modern Physics **81**, 109–162 (2009).
[3] Y. Lin, "100-GHz transistors from wafer-scale epitaxial graphene," Science **327**, 662 (2010).
[4] F. Schwierz, "Graphene transistors," Nat. Nanotechnol. **5**, 487–496 (2010).
[5] M. A. Yamoah, W. Yang, E. Pop, and D. Goldhaber-Gordon, "High velocity saturation in graphene encapsulated by hexagonal boron nitride," ACS Nano **11**, 9914–9919 (2017).
[6] M. Bonmann, A. Vorobiev, M. A. Andersson, and J. Stake, "Charge carrier velocity in graphene field-effect transistors," Applied Physics Letters **111**, 233505 (2017), https://doi.org/10.1063/1.5003684.
[7] A. Vorobiev, M. Bonmann, M. Asad, X. Yang, J. Stake, L. Banszerus, C. Stampfer, M. Otto, and D. Neumaier, "Graphene field-effect transistors for millimeter wave amplifiers," in *2019 44th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)* (2019) pp. 1–2.
[8] I. Meric, M. Han, A. Young, and et al., "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," Nature Nanotech **3**, 654–659 (2008).
[9] V. E. Dorgan, M.-H. Bae, and E. Pop, "Mobility and saturation velocity in graphene on SiO_2," Applied Physics Letters **97**, 082112 (2010), https://doi.org/10.1063/1.3483130.
[10] M. Asad, K. O. Jeppson, A. Vorobiev, M. Bonmann, and J. Stake, "Enhanced High-Frequency Performance of Top-Gated Graphene FETs Due to Substrate- Induced Improvements in Charge Carrier Saturation Velocity," IEEE Transactions on Electron Devices **68**, 899–902 (2021).
[11] M. Asad, S. Majdi, A. Vorobiev, K. Jeppson, J. Isberg, and J. Stake, "Graphene FET on Diamond for High-Frequency Electronics," IEEE Electron Device Letters **43**, 300–303 (2022).
[12] Y. Wu, K. A. Jenkins, A. Valdes-Garcia, D. B. Farmer, Y. Zhu, A. A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia, P. Avouris, and Y.-M. Lin, "State-of-the-art graphene high-frequency electronics," Nano Letters **12**, 3062–3067 (2012), pMID: 22563820, https://doi.org/10.1021/nl300904k.
[13] M. Shur, "Ballistic transport and terahertz electronics," in *2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)* (2010) pp. 1–7.
[14] S. Rakheja, Y. Wu, H. Wang, T. Palacios, P. Avouris, and D. A. Antoniadis, "An ambipolar virtual-source-based charge-current compact model for nanoscale graphene transistors," IEEE Transactions on Nanotechnology **13**, 1005–1013 (2014).
[15] M. Shur, "Low Ballistic Mobility in Submicron HEMTs," IEEE Electron Dev Lett **23** (2002).

[16] I. Meric, "Channel Length Scaling in Graphene Field-Effect Transistors Studied with Pulsed Current-Voltage Measurements," Nano Letters **11**, 1093–1097 (2011).

[17] Z. Chen and J. Appenzeller, "Mobility extraction and quantum capacitance impact in high performance graphene field-effect transistor devices," in *2008 IEEE International Electron Devices Meeting* (2008) pp. 1–4.

[18] A. K. Upadhyay, A. K. Kushwaha, P. Rastogi, Y. S. Chauhan, and S. K. Vishvakarma, "Explicit model of channel charge, backscattering, and mobility for graphene fet in quasi-ballistic regime," IEEE Transactions on Electron Devices **65**, 5468–5474 (2018).

[19] J. Lusakowski, W. Knap, Y. Meziani, J.-P. Cesso, A. El Fatimy, R. Tauk, N. Dyakonova, G. Ghibaudo, F. Boeuf, and T. Skotnicki, "Electron mobility in quasi-ballistic Si MOSFETs," Solid-State Electronics **50**, 632–636 (2006), special Issue: Papers Selected from the 35th European Solid-State Device Research Conference - ESSDERC'05.

[20] S. Datta, *Electronic Transport in Mesoscopic Systems*, Cambridge Studies in Semiconductor Physics and Microelectronic Engineering (Cambridge University Press, 1995).

[21] I. Harrysson Rodrigues, A. Generalov, M. Soikkeli, A. Murros, S. Arpiainen, and A. Vorobiev, "Geometrical magnetoresistance effect and mobility in graphene field-effect transistors," Applied Physics Letters **121**, 013502 (2022), https://doi.org/10.1063/5.0088564.

[22] S. ang Peng, Z. Jin, P. Ma, D. yong Zhang, J. yuan Shi, J. bin Niu, X. yun Wang, S. qing Wang, M. Li, X. yu Liu, T. chun Ye, Y. hui Zhang, Z. ying Chen, and G. hui Yu, "The sheet resistance of graphene under contact and its effect on the derived specific contact resistivity," Carbon **82**, 500–505 (2015).

[23] M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier, and J. Stake, "Graphene field-effect transistors with high extrinsic f_T and $f_{\max}$," IEEE Electron Device Letters **40**, 131–134 (2019).

[24] M. Asad, M. Bonmann, X. Yang, A. Vorobiev, K. Jeppson, L. Banszerus, M. Otto, C. Stampfer, D. Neumaier, and J. Stake, "The dependence of the high-frequency performance of graphene field-effect transistors on channel transport properties," IEEE Journal of the Electron Devices Society **8**, 457–464 (2020).

[25] I. Harrysson Rodrigues, *Charge carrier transport in field-effect transistors with two-dimensional electron gas channels studied using geometrical magnetoresistance effect.*, Ph.D. thesis, series: 5194 (Chalmers University of Technology, 2022).

[26] "Graphenea," `https://www.graphenea.com` (2010).

[27] M. Asad, *Impact of adjacent dielectrics on the high-frequency performance of graphene field-effect transistors.*, Ph.D. thesis, series: 8754 (Chalmers University of Technology, 2021).

[28] F. Xia, V. Perebeinos, Y. Lin, Y. Wu, and P. Avouris, "The origins and limits of metal-graphene junction resistance," Nat Nanotechnol. **6**, 179–84 (2011).

[29] L. Wang, I. Meric, P. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L. Campos, D. Muller, J. Guo, P. Kim, J. Hone, K. Shepard, and C. Dean, "One-dimensional electrical contact to a two-dimensional material," Science , 614–7 ((2013)).

[30] X. Yang, M. Bonmann, A. Vorobiev, and J. Stake, "Characterization of Al_2O_3 gate dielectric for graphene electronics on flexible substrates," in *2016 Global Symposium on Millimeter Waves (GSMM) and ESA Workshop on Millimetre-Wave Technology and Applications* (2016) pp. 1–4.

[31] M. Groner, J. Elam, F. Fabreguette, and S. George, "Electrical characterization of thin Al_2O_3 films grown by atomic layer deposition on silicon and various metal substrates," Thin Solid Films **413**, 186–197 (2002).

[32] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric," Applied Physics Letters **94**, 062107 (2009), https://doi.org/10.1063/1.3077021.

[33] M. Bonmann, A. Vorobiev, J. Stake, and O. Engström, "Effect of oxide traps on channel transport characteristics in graphene field effect transistors," Journal of Vacuum Science Technology B **35**, 01A115 (2017), https://doi.org/10.1116/1.4973904.

[34] J. Wang and M. Lundstrom, "Ballistic transport in high electron mobility transistors," IEEE Transactions on Electron Devices **50**, 1604–1609 (2003).

[35] C. K. Ullal, J. Shi, and R. Sundararaman, "Electron mobility in graphene without invoking the Dirac equation," American Journal of Physics **87**, 291–295 (2019), https://doi.org/10.1119/1.5092453.

[36] M. Lundstrom, "On the mobility versus drain current relation for a nanoscale mosfet," IEEE Electron Device Letters **22**, 293–295 (2001).

[37] A. Hamed, M. Asad, M.-D. Wei, A. Vorobiev, J. Stake, and R. Negra, "Integrated 10-ghz graphene fet amplifier," IEEE Journal of Microwaves **1**, 821–826 (2021).

[38] S. Adam, E. H. Hwang, V. M. Galitski, and S. Das Sarma, "A self-consistent theory for graphene transport," Proceedings of the National Academy of Sciences **104**, 18392–18397 (2007), https://www.pnas.org/content/104/47/18392.full.pdf.

[39] S. Bidmeshkipour, A. Vorobiev, M. A. Andersson, A. Kompany, and J. Stake, "Effect of ferroelectric substrate on carrier mobility in graphene field-effect transistors," Applied Physics Letters **107**, 173106 (2015), https://doi.org/10.1063/1.4934696.

[40] Y. Zhang, V. Brar, C. Girit, and et al., "Origin of spatial charge inhomogeneity in graphene," Nature Phys , 722–726 (2009).

[41] "Adsorbates on graphene: Impurity states and electron scattering," Chemical Physics Letters **476**, 125–134 (2009).

[42] M. J. Hollander, M. LaBella, Z. R. Hughes, M. Zhu, K. A. Trumbull, R. Cavalero, D. W. Snyder, X. Wang, E. Hwang, S. Datta, and J. A. Robinson, "Enhanced transport and transistor performance with oxide seeded high-k gate dielectrics on wafer-scale epitaxial graphene," Nano Letters **11**, 3601–3607 (2011), pMID: 21805989, https://doi.org/10.1021/nl201358y.

[43] J. Buron, F. Pizzocchero, P. Jepsen, and et al., "Graphene mobility mapping." Sci Rep **5**, 12305 ((2015)).

[44] S. Adam, E. Hwang, and S. Das Sarma, "Scattering mechanisms and Boltzmann transport in graphene," Physica E: Low-dimensional Systems and Nanostructures **40**, 1022–1025 (2008).

[45] J. Chen, C. Jang, S. Adam, M. S. Fuhrer, E. D. Williams, and M. Ishigami, "Charged-impurity scattering in graphene," Nature Phys. **4**, 377–381 (2008).

[46] J. Chan, A. Venugopal, A. Pirkle, S. McDonnell, D. Hinojos, C. W. Magnuson, R. S. Ruoff, L. Colombo, R. M. Wallace, and E. M. Vogel, "Reducing extrinsic performance-limiting factors in graphene grown by chemical vapor deposition," ACS Nano **6**, 3224–3229 (2012), pMID: 22390298, https://doi.org/10.1021/nn300107f.