Monte Carlo Simulation of Flash Memory Elements' Electrophysical Parameters

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Abstract

Operation of modern flash memory elements is based on electron transport processes in the channel of silicon MOSFETs with floating gate. The aim of this work was calculation of electron mobility and study of the influence of phonon and ionized impurity scattering mechanisms on the mobility, as well as calculation of parasitic tunneling current and channel current in the conductive channel of flash memory element. Numerical simulation during the design stage of flash memory element allows working out guidelines for optimization of device parameters defining its performance and reliability.

In the work such electrophysical parameters, characterizing electron transport, as mobility and average electron energy, as well as tunneling current and current in the channel of the flash memory element are studied via the numerical simulation by means of Monte Carlo method. Influence of phonon and ionized impurity scattering processes on electron mobility in the channel has been analyzed. It is shown that in the vicinity of drain region a sufficient decrease of electron mobility defined by phonon scattering processes occurs and the growth of parasitic tunneling current is observed which have a negative influence on device characteristics.

The developed simulation program may be used in computer-aided design of flash memory elements for the purpose of their structure optimization and improvement of their electrical characteristics.

Keywords: flash memory, electron mobility, electron scattering, tunneling current, Monte Carlo method.

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Моделирование электрофизических параметров элементов флеш-памяти методом Монте-Карло

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В основе функционирования современных элементов флеш-памяти лежат процессы переноса электронов в проводящем канале кремниевых МОП-транзисторов с плавающим затвором. Целью данной работы являлось проведение вычислительного эксперимента по расчёту подвижности электронов и изучению влияния на подвижность фононного рассеяния и рассеяния на ионизированной примеси, а также расчёт паразитного туннельного тока и тока в проводящем канале элемента флеш-памяти. Проведение вычислительного эксперимента на этапе разработки и проектирования элементов флеш-памяти позволит выработать рекомендации для оптимизации параметров прибора, определяющих быстродействие и надёжность его работы.

Путем численного моделирования электронного переноса в элементе флеш-памяти методом Монте-Карло рассчитаны такие электрофизические параметры, характеризующие перенос, как подвижность, средняя энергия электронов, а также плотность туннельного тока и тока в канале прибора. Изучено влияние процессов рассеяния на фононах и ионизированной примеси на подвижность электронов в канале. Показано, что вблизи области стока происходит существенное снижение подвижности электронов, обусловленное процессами рассеяния на фононах, а также наблюдается рост паразитного туннельного тока, что приводит к ухудшению рабочих характеристик прибора.

Разработанная программа моделирования может быть использована при компьютерном проектировании элементов флеш-памяти с целью оптимизации их конструкции и улучшения электрических характеристик.

Ключевые слова: флеш-память, подвижность электронов, рассеяние электронов, туннельный ток, метод Монте-Карло.

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Introduction

In state-of-the-art integrated circuits short channel silicon MOSFETs with floating gate are widely used as the basis of flash memory elements. Modern trends in development of flash memory elements are directed to the miniaturization of their active regions (see, for example, [1, 2]). Further miniaturization of flash memory elements is restricted by growth of parasitic tunneling currents and decrease of performance in data reading mode. High density of parasitic tunneling currents can lead to distortion of data saved in the flash memory. The value of parasitic tunneling current is determined by design features of the MOSFET and conditions causing heating of electron gas in the conductive channel of the device [2–5]. Device performance is directly related to electron mobility in its active region. Electron mobility in the conductive channel of a MOSFET is defined by electron scattering processes. The main electron scattering mechanisms in short channel silicon MOSFETs are phonon scattering and ionized impurity scattering.

The aim of the work was to calculate of electron mobility and study the influence of phonon and ionized impurity scattering mechanisms on the mobility, as well as to calculate of parasitic tunneling current and channel current in the conductive channel of flash memory element.

Simulated device structure

In the Figure 1 schematic cross-section of the simulated silicon MOSFET with floating gate is represented [5, 6]. Dimensions of the regarded transistor are as follows: channel length L_{ch} = 0.2 nm, gate oxide thickness d_{ox} = 6 nm, tunnel oxide thickness d_{tun} = 2 nm, floating gate thickness d_{float} = 2 nm. Donor impurity concentration in the source and drain regions is $N_D = 10^{26}$ m^{-3}, acceptor impurity concentration in the substrate is $N_A = 10^{24}$ m^{-3}. The depth of the source and drain regions is d_j = 100 nm. The gate bias V_G and the drain bias V_D are supposed equal to 2 V which is a typical value for data reading mode.

Electron mobility and the influence of phonon and ionized impurity scattering mechanisms on the mobility in regarded flash memory element is studied by means of numerical Monte Carlo charge carrier transport simulation. The density of parasitic tunneling current jtun and the density of channel current jch are calculated too. Algorithms and self-consistent procedures may be found in [7].

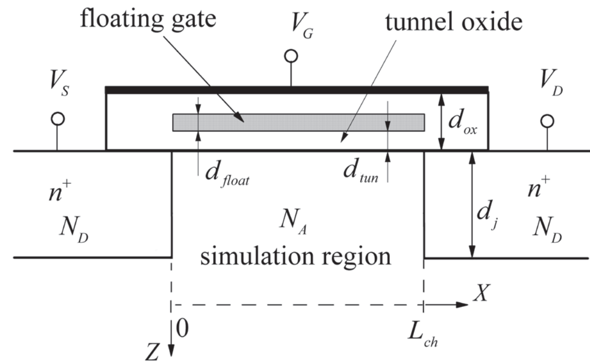

Figure 1 – Schematic cross-section of the flash memory element based on floating gate MOSFET

During the simulation the dependences of average values of electron concentration N_e, energy E_{av} and mobility μ on the position along the conduction channel (X-axis) and into the depth of the channel (Z-axis) are calculated. The self-consistent procedure implies that electron concentration $N_e(x, z)$ at every time step is used to solve Poisson equation and to calculate electric field strength in different points of the conduction channel, and also to calculate ionized impurity scattering rate. Acoustic and intervalley phonon as well as ionized impurity scattering processes are taken into account. Impact ionization process is also incorporated into the simulation algorithm according to Keldysh-type model discussed in [8]. However, calculations proof that its effect on transport properties is negligible for given transistor operation mode.

Acoustic phonon scattering rate is calculated according to the following expression [7, 9, 10]:

$$W_{ac} = \frac{D_{ac}^2 \sqrt{m_d^3} k_B T}{\pi \hbar^4 u_l^2 \rho} \sqrt{E(1+\alpha E)}(1+2\alpha E), \quad (1)$$

where D_{ac} is the deformation potential for scattering on acoustic phonons; m_d is electron density-of-states effective mass for corresponding valley; u_l is longitudinal sound velocity in silicon; ρ is silicon mass density; α is nonparabolicity coefficient.

Intervalley phonon scattering rate is defined as follows [7, 9, 10]:

$$W_{ij} = \frac{D_{ij}^2 \sqrt{m_d^3} Z_{ij}}{\sqrt{2}\pi\rho\hbar^3\omega_{ij}} \begin{pmatrix} N_{ij} \\ N_{ij}+1 \end{pmatrix} \times \sqrt{E \pm \hbar\omega_{ij} - \Delta E_{ij}} \left(1 + 2\alpha\left(E \pm \hbar\omega_{ij} - \Delta E_{ij}\right)\right), \quad (2)$$

where D_{ij} is the intervalley coupling constant; Z_{ij} is the number of possible final equivalent valleys for the transition; ω_{ij} is the phonon frequency and N_{ij} is the number of phonons according to the Bose–Einstein statistics; ΔE_{ij} is the energy difference between the energy minima of initial and final valleys.

Considering transitions between equivalent valleys in silicon for g-type scattering the values of parameters are $Z_{ij} = 1$, $\Delta E_{ij} = 0$, and phonon temperature is $T_{ij} = 537$ K. For f-type scattering $Z_{ij} = 4$, $\Delta E_{ij} = 0$, and phonon temperatures are $T_{ij} = 686$ K and $T_{ij} = 733$ K.

Ionized impurity scattering rate is defined according to Brooks–Herring model [7, 9, 10]:

$$\left[W_{\mathrm{I}}\right]_t = \frac{N_A^t \sqrt{2}\, e^4}{\left(\varepsilon_0 \varepsilon_{\mathrm{Si}}\right)^2 4\pi \sqrt{m_d}\, B_t^2} \frac{\sqrt{E_{\pm}}\left(1+2\alpha E\right)}{1+4\left(\dfrac{E_\alpha}{B_t}\right)}, \tag{3}$$

where N_A^t is acceptor doping density at t-th section of the channel; $E_\alpha = E(1+\alpha E)$; ε_0 is dielectric constant; $\varepsilon_{\mathrm{Si}}$ is silicon relative permittivity; $L_D^t = \sqrt{\dfrac{\varepsilon_{\mathrm{Si}} \varepsilon_0 E_{av}^t}{N_e^t e^2}}$ is Debye screening length for electrons with characteristic concentration N_e^t and average energy E_{av}^t, $B_t = \hbar^2 \big/ 2\left(L_D^t\right)^2 m_d$, $E_b^t = \sqrt[3]{0.75/\pi N_A^t}$.

Results of the simulation and their discussion

In the Figure 2 simulated dependence of the relation between parasitic tunneling current and drift current in the conductive channel versus the relative position along the device channel is presented. In the Figures 3 and 4 calculated electron average energy and average mobility along the device channel are shown.

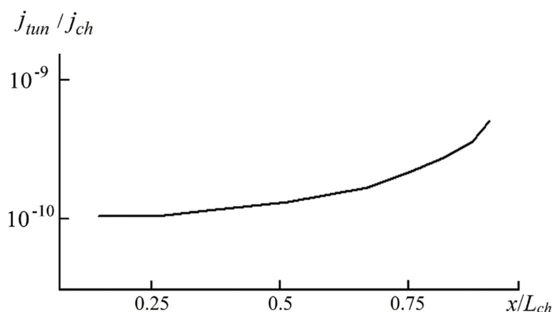

Figure 2 – Parasitic tunneling current to drift current ratio dependence versus relative position along the conductive channel

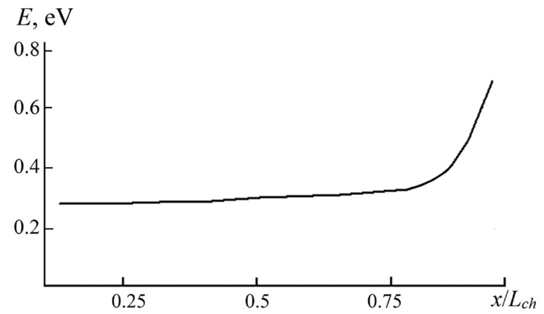

Figure 3 – Average electron energy dependence versus the relative position along the conductive channel of the flash memory element

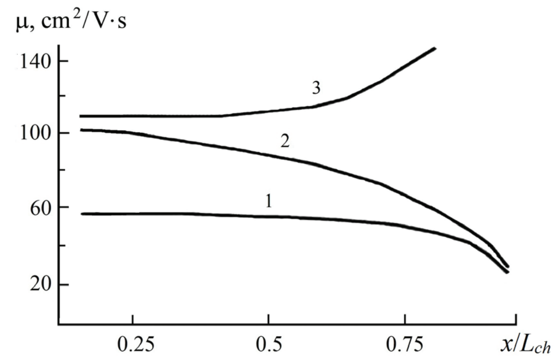

Figure 4 – Average electron mobility dependence on the relative position along the conductive channel: 1 – with account of both phonon and ionized impurity scattering; 2 – with account of only phonon scattering; 3 – with account of only ionized impurity scattering

Analysis of the dependences presented in the figures allow to conclude that in the part of the channel close to the drain region a sufficient growth of electron energy is observed. The latter leads to the growth of phonon scattering rates, which, in turn, causes a sufficient decrease of electron mobility. As well, the growth of parasitic tunneling current is observed. The phenomena are quite undesirable for normal operation of flash memory element.

The simulation results also show that the influence of every regarded scattering mechanism on electron mobility varies at different channel regions and is not uniform. As can be seen from the Figure 4, phonon scattering makes a decisive influence on the decrease of electron mobility in the part of the channel close to the drain region, while the influence of ionized impurity scattering is sufficiently reduced in this part of the channel. Such behavior is correlated to a rather steep increase of electron energy in this region.

To analyze variation of electron mobility along the device channel as well as into the depth of the

channel, in Figure 5 the spatial distribution of mobility is presented in the form of a two-dimensional dependence on x and z coordinates.

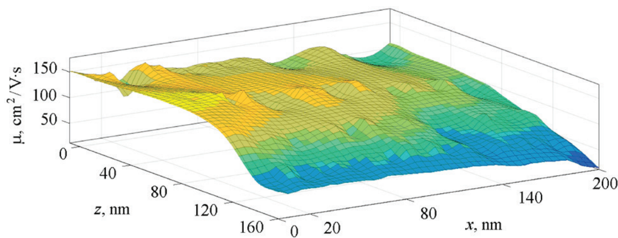

Figure 5 – Spatial distribution of electron mobility in the simulated flash memory element

As can be seen electron mobility decreases noticeably with the growth of coordinate value.

Conclusion

The dependences of parasitic tunneling current density, average electron energy and mobility versus the position along the channel of the flash memory element have been calculated for data reading mode. The calculation is made by means of Monte Carlo simulation of electron transport in the device.

It is shown that in the vicinity of drain region a sufficient decrease of electron mobility occurs. At the same time, the growth of parasitic tunneling current is observed, which can hinder the data reading process. Analysis of the influence of phonon and ionized impurity scattering processes on electron mobility in the channel of the device has revealed that both of these mechanisms make approximately equal effect on the mobility only in the origin of the channel. In the vicinity of the drain region phonon scattering processes have a determining influence on electron mobility and are responsible for significant decrease of its value and consequent lowering of the device performance.

The simulation program developed in this work may be used in computer-aided design of flash memory elements for the purpose of their structure optimization and improvement of their electrical characteristics.

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