VCO-based ADC with a simplified DAC for non-linearity correction

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The performance of open-loop analogue-to-digital converters (ADCs) implemented with voltage-controlled-oscillators (VCOs) is limited by VCO non-linearity and first-order noise shaping. The resolution limitation imposed by first-order noise shaping can be compensated by a ring oscillator VCO with many output phases. Linearity can also be improved by using a feedback loop around the VCO closed with a digital-to-analogue converter (DAC). However, a long ring oscillator may require a DAC with a prohibitive number of bits if feedback is used to compensate distortion. This letter proposes an ADC architecture based on the Leslie-Singh $\Delta\Sigma$ modulator that allows to implement a distortion correction loop around a VCO with a simplified DAC of few levels, yet keeping a large number of output quantisation levels to maintain resolution. The letter discusses the system level architecture and shows an implementation circuit example to verify the effective correction of distortion.

Introduction: Analogue-to-digital converters (ADCs) implemented with voltage-controlled-oscillators (VCOs) are an interesting choice to implement oversampled ADCs in low-voltage nanometre CMOS technologies. In addition of a mostly digital circuitry, VCO-ADCs constructed with ring oscillators may be designed with very low input-referred thermal noise [1] and flicker noise mitigation techniques [2]. Moreover, ring oscillators act simultaneously as a signal encoder and as an input preamplifier [3]. As a consequence, they are good candidates to replace switched-capacitor $\Delta\Sigma$ modulators with improved area and power. Although the peak signal-to-noise ratio (SNR) of a VCO-ADC can compete with that of switched-capacitor $\Delta\Sigma$ modulators, the signal-to-noise and distortion ratio (SNDR) performance is very limited in open-loop circuits due to ring oscillator non-linearity [1]. A possible way to overcome the SNDR limitation is to embed the VCO in a closed feedback loop [4]. This architecture does not provide any resolution enhancement compared to the open-loop architecture, but the presence of an extra digital-to-analogue converter (DAC) pays off when linearity and dynamic range are considered. Furthermore, restriction to first-order noise shaping implies the use of either a very high oversampling ratio or many bits in the VCO quantiser. This letter shows a simple VCO-ADC architecture that permits to implement a high resolution VCO quantiser with sufficient linearity using a feedback DAC with a reduced number of output levels. This architecture is based on the Leslie-Singh modulator [5], but modified to seize the inherent fine-coarse quantisation paths used in some VCO-ADCs [3, 6, 7].

Proposed architecture: First-order noise-shaped VCO-based ADCs can be built either with open-loop (Fig. 1a) or closed-loop (Fig. 1b) pseudo-differential configurations. In both cases, an ideal counter performs the integration of the VCO's phase by counting the edges of the output square wave $w_{p,n}(t)$ (single-phase). The counters are supposed to increase at most in $2^{(M\ \ 1)}$ counts in a single sampling period $T_s = 1/f_s$. Therefore signal $y[n]$ in Fig. 1 requires M bits to be represented. The main difference between Fig. 1a and Fig. 1b is how quantisation noise is spectrally shaped. While in Fig. 1a this is achieved by a digital differentiator after integration (counting), Fig. 1b uses a feedback loop around the VCO, as in a conventional continuous-time $\Delta\Sigma$ modulator.

If we assume that all VCOs in Fig. 1 perform a linear voltage-to-frequency conversion, both systems may be made equivalent in terms of quantisation noise at the output $y[n]$ [4]. However, when dealing with practical VCOs (as in the case of ring oscillators), the performance of both architectures strongly differs from each other due to the non-linearity of the VCO voltage-to-frequency relationship. The reason for this is the very different signal amplitudes that modulate the VCOs. The modulating signals of the VCOs in Fig. 1a correspond with the full scale value of the input signal $x(t)$, what results in a highly non-linear behaviour. On the contrary, in the feedback path of Fig. 1b, the feedback signal $y(t)$ will be approximately equal to $x(t)$, so that $u(t)$ becomes on the order of the quantisation error. This makes the VCOs work in a limited span of their voltage-to-frequency transfer function, reducing the influence of harmonic distortion. The main disadvantage of the structure of Fig. 1b is that, when the VCOs have many output phases, the feedback DAC might become large and complex.

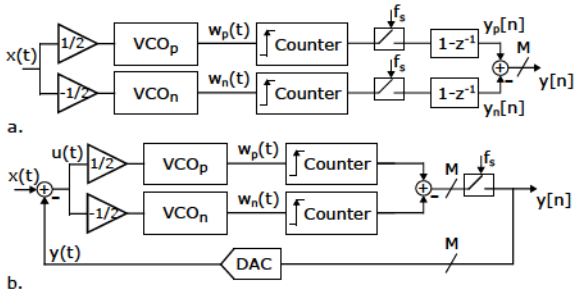

Fig. 1. VCO-based ADC configurations: a. open-loop, and b. closed-loop.

In this letter, we propose an intermediate solution between both architectures, solving the problem of the VCO non-linearity with a closed-loop configuration, but limiting the number of bits in the feedback path. According to [5], if proper digital filters are applied to reconstruct the output data, the resolution of a multi-bit quantiser in a $\Delta\Sigma$ modulator remains unchanged although the feedback path uses less quantisation levels. This idea can be extended to the implementation of a closed-loop VCO-based ADC with high resolution to improve linearity. The proposed solution, along with an equivalent discrete linear model (for simplicity, we use a single-ended version), are depicted in Fig. 2.

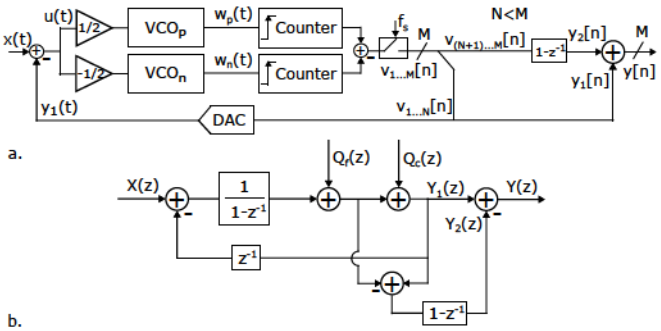

Fig. 2 *Proposed VCO-based solution: a. architecture, and b. equivalent single-ended discrete linear model.*

The architecture of Fig. 2a uses two ideal counters attached to two VCOs. The outputs of the two counters are sampled and subtracted generating a bipolar signal with discrete integer values $v[n]$. If the frequency difference of the VCOs is limited, the difference signal $v[n]$ can be represented using a finite number of bits M. However, in the feedback path, we only use the N first most-significant-bits (MSBs) $v_{1\ldots N}[n]$ such that $N < M$. This system can be modelled with two quantisation processes: a fine quantisation with M bits and a coarse quantisation with N bits. These two quantisation processes are represented in Fig. 2b as additive errors Q_f and Q_c respectively. In Fig. 2b we define signals Y_1 and Y_2 as follows:

$$Y_1(z) = \left(1 - z^{\ \ 1}\right)\left(Q_f(z) + Q_c(z)\right) + X(z), \tag{1}$$

$$Y_2(z) = \left(1 - z^{\ \ 1}\right) Q_c(z). \tag{2}$$

We may cancel error Q_c and obtain an output signal Y which is only affected by Q_f by means of a digital differentiator:

$$Y(z) = Y_1(z) - Y_2(z) = \left(1 - z^{\ \ 1}\right) Q_f(z) + X(z), \tag{3}$$

In Fig. 2a, we have represented signal $v[n]$ as a M-bit digital bus conveying data samples $v_{1..M}[n]$. This figure shows how with a simple bus splitting operation we can implement the fine-coarse quantisation and how to generate $y[n]$ with a digital differentiator and a bus merge operation.

System level simulations: Behavioural level simulations of Fig. 1 and Fig. 2 have been made to check the quantisation error cancellation of the model of Fig. 2b and its ability to compensate VCO non-linearity, which is the actual target of our new architecture. To model a real

VCO behaviour, a 11-phase VCO has been used with a pre-distortion function that mimics the 0.13 μm CMOS VCO described in [1]. The non-linear relationship between the modulation voltage and the oscillation frequency is represented by the coefficients of a 4$^{\text{th}}$-order polynomial approximation shown in Table 1. This approximation is valid for VCO input voltages within $\pm$500 mV. The sampling frequency is f_s = 4 MHz and the analogue bandwidth (ABW) is set to 20 kHz. The pulses generated at the 11-phase VCO are counted and added, producing a single output count signal equivalent to $v[n]$ in Fig. 2a, which would require M = 8 bits to be represented. Assuming the VCOs of Fig. 1 and Fig. 2 to have a linear voltage-to-frequency characteristic, the simulated SNDR is the same for Fig. 1a, Fig. 1b and Fig. 2a, and equals 98.5 dB for a - 6 dBFS 1 kHz sinusoidal input.

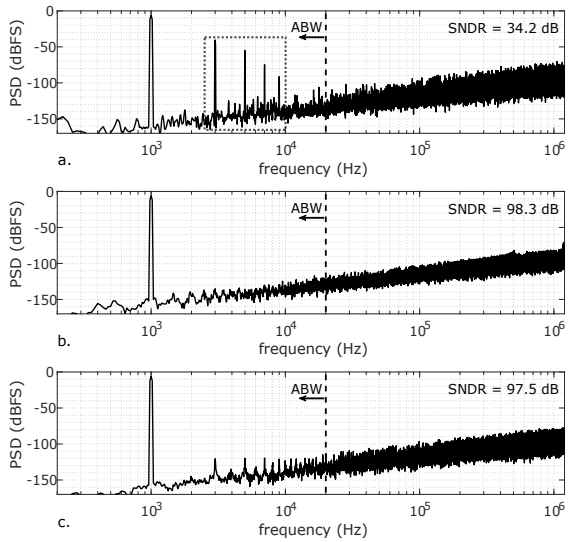

Fig. 3 *Behavioural simulations of: a. open-loop, b. closed-loop, and c. proposed configurations.*

The simulations have been replicated with the same parameters, but including the non-linear pre-distortion polynomial at the input of the VCOs as in a real implementation. The SNDR performance of the open-loop configuration is now limited to 34.2 dB by the distortion components shown in Fig. 3a in dotted lines. For the closed-loop configuration, the simulated spectrum of Fig. 3b shows that the influence of the non-linear characteristic of the VCOs is attenuated yielding a SNDR = 98.3 dB. The same occurs for the proposed architecture in Fig. 2a, but using N = 4 bits instead of M = 8 bits in the feedback path. According to Fig. 3c, the SNDR is improved from 34.2 dB in the open-loop architecture to 97.5 dB.

Practical implementation example: Fig. 4 shows a simplified schematic of a practical implementation example of the proposed architecture using the same 11-phase ring oscillator described before. It is based on a pseudo-differential coarse-fine quantisation architecture [3, 6, 7]. For each channel, the first phase of the VCO $w_1(t)$ is connected to a 3-bit pivotal counter [6] that performs the coarse quantisation. The difference between the positive and negative counters $y_1[n]$ is sampled and fed back to the VCOs input using a 4-bit DAC. The remaining 10 phases are sampled and decoded. The outputs of the decoder represent the differences between $y_1[n]$ and the outputs of a larger counter that would count all the edges present in w_1 to w_{11} in a sampling period T_s [3, 6, 7]. According to Fig. 2b, the difference of the pivotal counters is a 4-bit signal Y_1 and the signals coming from the rest of phases after the phase register, represent quantisation error Q_c, that would require also 4 bits to be represented. Therefore, we may obtain a finely quantised output signal Y with 8 bits of resolution by combining Y_1 and Y_2.

The schematic of Fig. 4 has been simulated including the polynomial approximation of the 0.13 μm CMOS ring oscillator presented in [1].

Table 1: Polynomial coefficients of a non-linear VCO.

$k_{VCO,0}$ [MHz]	$k_{VCO,1}$ [MHz/V]	$k_{VCO,2}$ [MHz/V^2]	$k_{VCO,3}$ [MHz/V^3]	$k_{VCO,4}$ [MHz/V^4]	$k_{VCO,5}$ [MHz/V^5]
15.16	29.33	-4.15	-0.82	14.40	-24.70

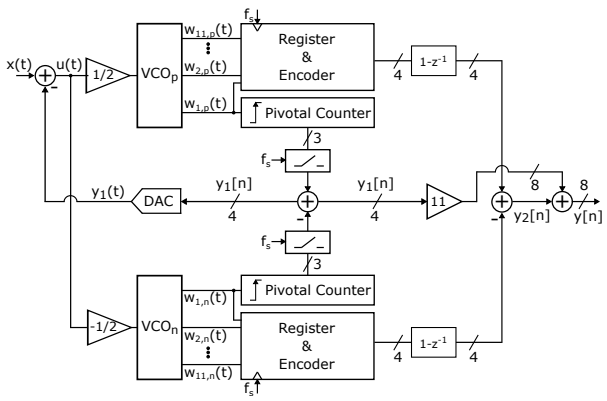

Fig. 4 *Practical implementation architecture of the proposed VCO-based ADC with a simplified DAC.*

Fig. 5 shows the output spectrum of the transient simulation applying the values of f_s and ABW mentioned above. For a - 6 dBFS 1 kHz sinusoidal input, the SNDR is 97.4 dB and the harmonic distortion components are almost indistinguishable from the quantisation noise floor. As can be observed, the non-linearity problem is solved by using a 4-bit DAC only but generating a 8-bit output.

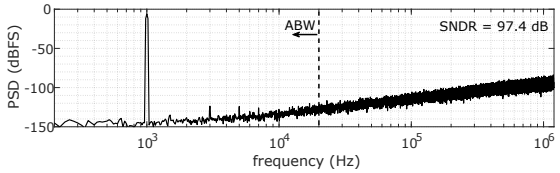

Fig. 5 *Circuit level simulation of the proposed practical implementation architecture.*

Conclusion: We have shown how a high resolution VCO-based ADC can be modified to benefit from dynamic range extension through feedback without requiring a highly complex DAC. This architecture is based on the Leslie-Singh modulator principle but with the added benefit of an easy quantiser scalability by use of digital counters in the VCO-ADC architectures. In particular, a VCO-ADC based in a ring oscillator connected to a pivotal counter and a phase register is well suited to this new architecture.

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