A VCO-based Sturdy MASH ADC architecture

E. Gutierrez, L. Hernandez and F. Cardes

This letter introduces a new multistage 1-1 $\Delta\Sigma$ ADC architecture implemented only with VCOs. A SMASH configuration is used to avoid the need of either calibration circuitry or noise cancellation filters. The digital nature of the VCO's output simplifies the implementation of the interconnection paths between stages, making unnecessary neither the use of multibit DACs nor analogue subtraction elements. The basic operation of the architecture is shown at system level and the sensitivity to VCO's frequency mismatch is analysed. The proposed architecture has been validated through behavioural simulations.

Introduction: The continuous development of deep-submicron CMOS design technologies supposes important challenges in the implementation of mixed signal circuits. On the one hand, analogue designs constantly get more complicated due to the decrease of the supply voltage and the low gain of narrow-length devices. On the other hand, digital designs benefit from the scaling process in terms of power consumption, speed and area [1]. Accordingly, conventional analogue-to-digital converters (ADCs) become difficult to implement. Time-encoding based ADCs are an interesting alternative to conventional ones. Voltage-controlled-oscillator based ADCs (VCO-ADCs) have specially enlisted the interest of the designer community, because they can be implemented mostly with digital circuitry and they work similar to noise-shaped $\Delta\Sigma$ modulators. One of the main drawbacks of VCO-ADCs is the restriction to first-order noise-shaping, which limits the converter resolution [2]. An increase of the noise-shaping order is usually accomplished by incorporating analogue integrators into a $\Delta\Sigma$ loop combined with VCO-based quantization [3]. However, the performance of these systems is restricted by the power consumption of the analogue integrators. Alternatively, continuous-time $\Delta\Sigma$ modulators implemented only with VCOs were proposed in [4, 5]. Fully VCO-based multistage noise shaping (MASH) architectures have also been described [6]. In particular, 1-1 MASH architectures implemented with VCOs described to date require analogue coupling of both the input signal and the quantization error. In addition, matching between the VCO gains and the corresponding noise-cancellation-filters (NCFs) is required to avoid noise leakage [7].

SMASH-$\Delta\Sigma$: A MASH-$\Delta\Sigma$ architecture without noise cancellation filters was proposed in [8], known as Sturdy-MASH architecture (SMASH). Absence of digital filters implies no matching requirements between analogue and digital circuitry. In addition, integrator requirements are alleviated thanks to a compensation loop in the first stage. Nevertheless, the SMASH architecture requires additional digital-to-analogue converters (DACs) in the feedback branches of the individual $\Delta\Sigma$ modulators. I

Fig. 1. Linear model of a discrete time 1-1 SMASH architecture

Fig.1 shows the linear model of a 1-1 SMASH-$\Delta\Sigma$ implemented in the discrete time domain. The expression for Y is:

$$Y = z^{-1} \cdot X + \left(1 - z^{-1}\right)^2 \cdot E_1 - \left(1 - z^{-1}\right)^2 \cdot E_2 \qquad (1)$$

Initially, as in a typical 1-1 MASH architecture, the input of the second stage is the quantization error from the first stage. However, the second stage output is subtracted from the first stage output and the result is applied to the input of the system to close the loop of the first stage. It can be observed in (1) that both E_1 and E_2 are second-order high-pass filtered.

Consequently, the need of digital filters is eliminated while shaping the quantization error of both stages [8].

VCO-based-SMASH: In this letter, the system modelling introduced in [9] is exploited to propose a novel 1-1 VCO-based-SMASH architecture. The proposed architecture combines the signals among the stages using only digital functions without requiring any linear analogue coupling circuit. The advantages of this new architecture are the disposal of the NCFs without requiring extra DACs or analogue subtraction nodes and the mostly-digital circuit, making this architecture adequate for low power and area implementations in current nanometer CMOS technologies.

Fig.2.a shows the typical model of a VCO-ADC, in which a VCO is assimilated to a phase integrator. This model is composed of a VCO followed by a sampler and a first differentiator in discrete time, where T_s is the sampling period and $f_s=1/T_s$. Nevertheless, the equivalence between a VCO and a pulse frequency modulator (PFM) will be considered here [9] in order to ease the description of the SMASH architecture. The general block diagram of a PFM is shown in Fig.2.b. A PFM can be considered as a VCO followed by an edge detector block $\delta(t)$, which generates Dirac Delta impulses when the phase of the oscillator equals multiples of π (the edges of signal w(t)). The delta stream p(t) is applied to a filter h(t) with square impulse response, which converts d(t) into a signal of fixed-length pulses y(t). The filter h(t) can be analysed as an integrator followed by a continuous time first difference. The spectrum of y(t) contains the signal x(t) at low frequencies and high frequency modulation components [9], similar to those observed in a frequency modulated signal. At the end, y[n] is identical in both Fig.2.a and Fig.2.b. In accordance with Fig.2.b, the VCO can be considered to work only as a signal coder, while noise shaping properties are defined solely by filter h(t). The quantization error in Fig.2.b. originates in the aliases of the high frequency modulation components of p(t), after being spectrally shaped by h(t). It can be considered a "time-error" after the integration, so it will be represent as the digital subtraction of the sampled u[n] and the unsampled u(t) signals resulting in a pulse width modulated (PWM) single-bit signal e(t).

Fig. 2 *VCO-ADC models; a. phase-integrator VCO model, b. PFM-based model*

The removal of digital filters in the SMASH architecture requires a feedback loop from the second stage output to the first stage input, typically added in front of the first integrator, as in Fig.1. Fig.3 shows the proposed VCO-based-SMASH architecture. In this block diagram, the first stage is viewed as a continuous-time first-order closed-loop $\Delta\Sigma$ modulator with an analogue integrator I_1. The input signal x(t) will be encoded into a PFM signal $p_1(t)$ using VCO_1. The feedback loop must be closed immediately before the $\Delta\Sigma$ integrator, at the point where signal $p_1(t)$ is applied. Note that the integration function in the loop of the first stage can be implemented as an up-down counter as long as its input p(t) is an impulse-like signal and y[n] is quantized and of discrete nature. Therefore, the integrator output u(t) will take integer values but will change asynchronously with respect to the sampling clock. Quantization noise e(t) will be attributed to the aliases generated at the sampler. Therefore, by properly manipulating the block diagram, the subtraction and integration will be made in the digital domain, avoiding the use of operational amplifiers or DACs.

A practical implementation of a 1-1 VCO-based-SMASH system is shown in Fig.4. A VCO integrator model suitable for closed loop $\Delta\Sigma$ modulators was introduced in [4], combining a VCO with a counter. A similar topology will be used in the first stage of the proposed
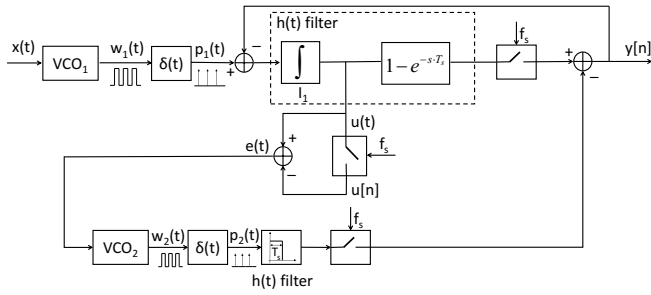
Fig. 3. Proposed VCO-based-SMASH

architecture, so the first VCO (VCO$_1$) is connected to an up-down counter. The count-up input of the counter is connected to VCO$_1$ and the count-down input is connected to the feedback path coming from the second stage. The second VCO (VCO$_2$) works similarly as a typical open loop VCO-ADC (Fig.2.a). All the subtraction operations are thus made in the digital domain and the output data are directly sampled from the first stage. Quantization error from the first stage is calculated as the difference of the actual up-down counter output and its sampled value. In the proposed system, this difference will take only two levels in spite that the counter output is multibit if we set the maximum oscillation frequency of VCO$_1$ below half the sampling rate, $f_{osc,1} \leq f_s/2$. Therefore, e(t) is a single-bit digital signal and VCO$_2$ can be implemented as a switched-ring oscillator (SRO) [10].
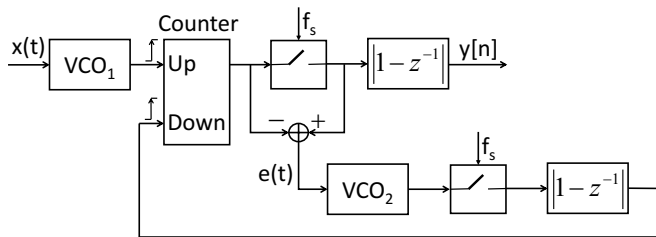
Fig. 4 *Practical implementation of a VCO-based-SMASH with an up-down triggered counter in the first stage*

Unlike SMASH-$\Delta\Sigma$ architectures implemented with discrete integrators, the quantization error cancellation in the VCO-based-SMASH architecture is completely independent with respect to the first-stage VCO gain. As can be seen in Fig.2.b, the first-stage VCO is not involved in the sigma-delta loop, that is closed afterwards, around the counter. This means no specific gain requirements in the first-stage VCO to achieve the desired noise shaping order in the architecture.

Simulation results: Behavioural level simulations of the system of Fig.4 have been made, obtaining the results shown in Fig.5. The instantaneous oscillation frequency of each VCO is defined by the rest oscillation frequency $f_{o,i}$ and an oscillation frequency gain $K_{VCO,i}$, both of them expressed Hz units. Input signal s(t) is considered dimensionless:

$$f_{osc,i} = f_{o,i} + K_{VCO,i} \cdot s(t) \quad s(t) \in [-1, 1] \quad (2)$$

In the simulations, $f_{o,i}$ and $K_{VCO,i}$ are normalized with respect to the sampling frequency f_s.
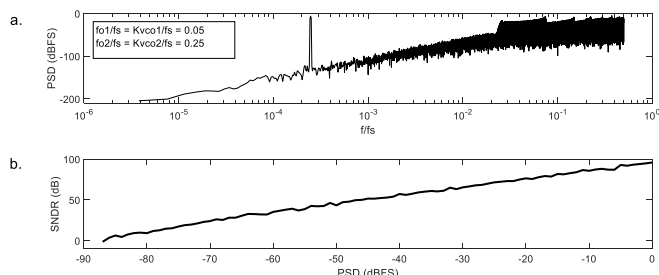
Fig. 5. Behavioural simulations; a. single-tone input, b. dynamic range

Fig.5.a shows the output spectrum for a single-tone input at -6dBFS, obtaining a signal-to-noise ratio (SNDR) equal to 86 dB with the oversampling ratio (OSR) equals 512. Fig.5.b depicts the dynamic range plot which reaches 88 dB. The oscillation frequency parameters are similar than in Fig.5.a.

As it was stated previously, the proposed architecture is insensitive to gain mismatches in VCO$_1$. Fig.6 shows two simulation examples in which $f_{o,1}$ (Fig.6.a) and $K_{VCO,1}$ (Fig.6.b) have been modified with respect to the values used in Fig.5.a. Although the SNDR is defined by the gain of the first oscillator (equivalent to changing the full scale in a conventional $\Delta\Sigma$ modulator), second order noise shaping is always observed.
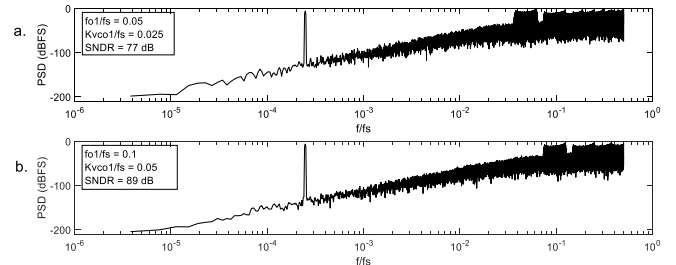
Fig. 6. VCO$_1$ mismatch simulations; a. $f_{o,1}$ mismatch, b. $K_{VCO,1}$ mismatch

Conclusion: The architecture of a 1-1 VCO-based-SMASH is proposed. The main novelty is the removal of the digital noise cancellation filters using VCOs and asynchronous digital blocks without any linear analogue circuitry. In addition, the proposed architecture is insensitive to the first stage VCO gain errors. The loop of the first stage is closed through an edge-triggered up-down counter in the digital domain and no direct coupling from the input signal is needed in the second stage. All these features may make the proposed architecture suitable for the design of mostly digital ADCs focused towards low power and low area systems.

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