Mixing Integrator for Compact Electrochemical Impedance Spectroscopy

Kerim Ture
Department of Electronic and Electrical Engineering
University College London
London, United Kingdom
k.ture@ucl.ac.uk

Sara S. Ghoreishizadeh
Department of Electronic and Electrical Engineering
University College London
London, United Kingdom
s.ghoreishizadeh@ucl.ac.uk

***Abstract*—With the rapid development in the miniaturization and monolithic integration of electrochemical sensors with integrated microchips on semiconductor technology, the power and area efficiency of the instrumentation circuits have become an emerging interest. Electrochemical Impedance Spectroscopy (EIS) is an analytical technique widely used in electrochemistry to investigate the properties of materials and electrode reactions. A conventional frequency-response analyzer (FRA) is a powerful EIS measurement instrument composed of amplification, mixing, and low-pass filtering blocks. This paper presents a resetting timing scheme in an integrating amplifier with capacitive feedback for combining three functions into one circuit. The proposed method benefits from lower power consumption and reduced silicon area occupation, as well as eases the design complexity. The theoretical principle of timing selection is expressed in mathematical equations and verified by the circuit simulations.**

***Index Terms*—electrochemical impedance spectroscopy, frequency response analyzer, mixer, integrator, capacitive feedback.**

I. Introduction

Over the past decades, new technological advancements have been embraced and played an essential role in reducing hospitalization rates by remote monitoring of patients and early detection of diseases. As our understanding of the underlying physical, chemical, and electrical principles, as well as used materials and manufacturing capabilities are extended, many new low-cost diagnostic techniques are still being developed. Electrochemical sensing procedures are concerned with the interrelation of electrical and chemical effects and are widely used methods for sensing applications [1]. For example, it is estimated that 1 in 11 adult populations in the world is living with diabetes, and electrochemical sensors are extensively adapted for frequent self-monitoring of glucose at home [2].

Electrochemical impedance spectroscopy (EIS) is one of the various electrochemical techniques providing information about charge transfer mechanisms and kinetics of electrochemical processes at an electrode as a function of frequency at a constant potential [3]. The main advantages of EIS are its label-free, non-invasive, and real-time detection capabilities [4]. Among the various EIS measurement techniques, the frequency-response analyzer (FRA) is a widely used method. Especially in monolithically integrated electrochemical sensors with instrumentation electronics fabricated in semiconductor technology, FRA becomes favorable due to its simplicity and small area requirements [5]. Miniaturization of the area and power consumption of FRA without compromising performance becomes essential in applications where a large number of electrodes are needed.

This paper discusses the drawbacks of the conventional FRA technique and presents a hardware-efficient method for EIS measurement. In the next section, the principle of hardware and power consumption reduction design is described. Section III validates the proposed approach with simulation results, followed by the conclusion and future work in Section IV.

This research was funded by the EPSRC [EP/T025638/1].

II. FRA Principle and Proposed Technique

A. Conventional FRA Operation

The FRA procedure is built upon the correlation between the analyzed signal and the reference signal. FRA sweeps over the whole frequency range of interest while processing the response of one frequency point at a time. The basic principle of the FRA technique for impedance measurement of an electrochemical cell is presented in the block diagram in Fig. 1(a). The amplifier, counter electrode (CE), and reference electrode (RE) connection create a basic potentiostat. The applied AC voltage at an ω frequency with a DC bias to the positive terminal of the amplifier creates the same voltage difference between the RE and working electrode (WE) by the current supplied by the CE. The DC component of the WE current (I_{WE}) can easily be calculated by taking a one-cycle averaging. Therefore, the paper focuses on the analysis and measurement of the AC response.

During the EIS measurement procedure, the applied AC signal is kept small in order not to affect the electrochemical activity. Thus, an amplification and current-to-voltage (I-V) conversion step is typically used before the mixing stage as shown in Fig. 1. The voltage after amplification and convertion can be expressed by $A\sin(\omega t + \phi)$, where A represents the amplitude and ϕ is the phase difference caused by the electrochemical impedance. The multiplication of the response voltage with in-phase and out-of-phase signals yields two equations to extract A and ϕ.

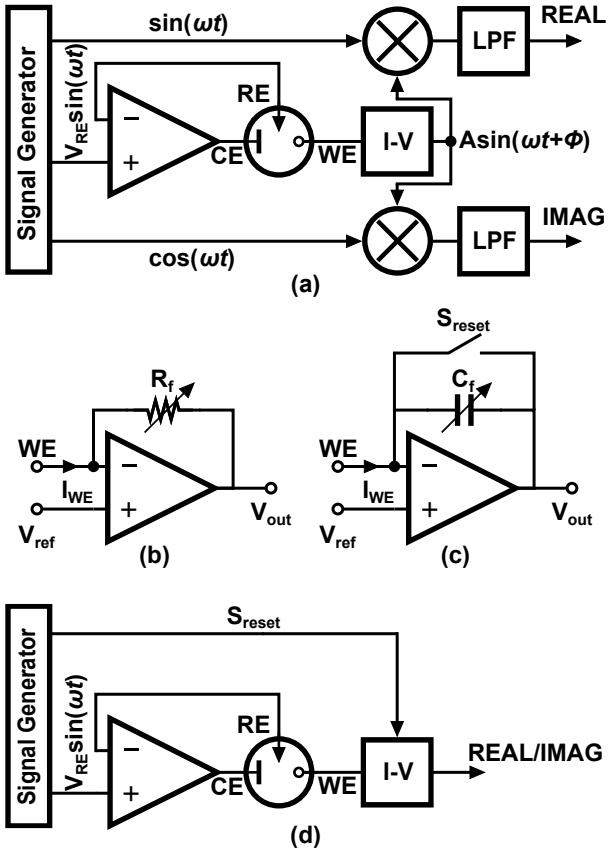

Fig. 1. (a) Conventional FRA block diagram. (b) Resistive feedback and (c) capacitive feedback current-to-voltage converters, (d) proposed FRA block diagram.

$$A\sin(\omega t+\phi)\sin(\omega t) = -\frac{A}{2}\left[\cos(2\omega t+\phi)-\cos(\phi)\right] \quad (1)$$

$$A\sin(\omega t+\phi)\cos(\omega t) = \frac{A}{2}\left[\sin(2\omega t+\phi)+\sin(\phi)\right] \quad (2)$$

Passing the multiplication results through a low-pass filter (LPF) with a cut-off frequency much smaller than 2ω yields real and imaginary parts of the response voltage.

$$\text{REAL} = \frac{A}{2}\cos(\phi) \quad (3)$$

$$\text{IMAG} = \frac{A}{2}\sin(\phi) \quad (4)$$

The sensor impedance can easily be calculated by using the applied AC voltage to the RE, and real and imaginary portions of the response current. As an alternative to the LPF, an averaging circuit with an integrator can be utilized to calculate the DC components of (1) and (2) [6].

Fig. 1(b) and (c) show the resistive and capacitive feedback topologies of the transimpedance amplifier (TIA) widely used for measuring WE current through amplification and I-V steps, respectively. To prevent the saturation of the amplifier for different current amplitudes in various frequencies, a variable resistor or capacitor is used in both approaches.

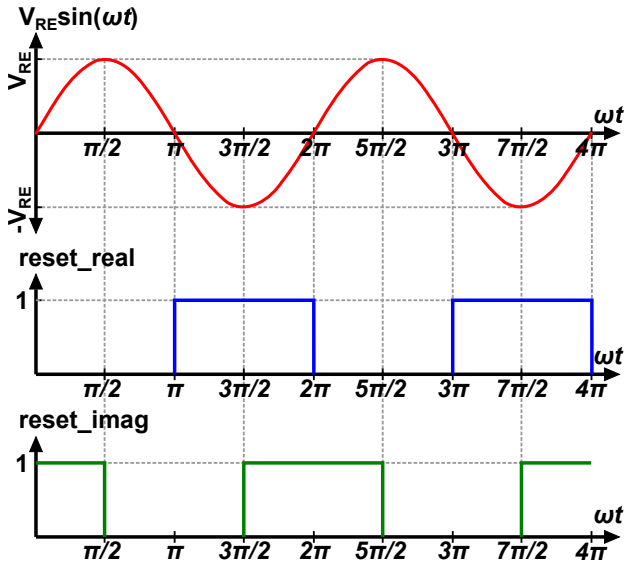

Fig. 2. Reset clock selections for simultaneous mixing and resetting functions in capacitive TIA.

The resistive feedback is the most typical interface with the provided linear relation between the voltage created between the terminal by the passing current. On the other hand, the capacitive feedback TIA generates an output voltage proportional to the current integration for a certain time duration and the capacitance value. Even though the capacitive feedback TIA is more complex in terms of operation, it has been theoretically and experimentally shown that the capacitive feedback has a lower noise level than the resistive feedback for the low current measurement systems [7]. Furthermore, we show here that with the careful selection of integration and resetting time of the integrator capacitor can eliminate the mixing and filtering operations, as the following subsection explains, and save power usage as well as silicon area occupation.

B. Proposed Reset Timing Scheme

A switch in series to a voltage input or parallel with a current input creates a mixing effect at the output of the TIA. We suggested a proper selection of the waveform of reset clock in the capacitive TIA, as in Fig. 1(d), serves as a mixer in addition to its resetting function. An example of the clock selections for measuring the real and imaginary portion of the WE current is presented in Fig. 2 as *reset_real* and *reset_imag*, respectively. In the case of applying the *reset_real* clock to the resetting switch, S_{reset}, the output voltage, V_{out_real}, can be expressed as follows

$$\begin{aligned} V_{out\_real} &= -\frac{1}{C_f}\int_0^{\pi/\omega} I_{WE}dt \\ &= -\frac{2A}{\omega C_f}\cos(\phi) \end{aligned} \quad (5)$$

where I_{WE} is assumed as $A\sin(\omega t+\phi)$. Similarly, when the *reset_imag* signal is selected as the resetting clock, V_{out_imag} can be calculated by the following equation.

$$V_{out\_imag} = -\frac{1}{C_f}\int_{\pi/2\omega}^{3\pi/2\omega} I_{WE}dt = \frac{2A}{\omega C_f}\sin(\phi) \quad (6)$$

The real and imaginary components of the I_{WE} can be calculated by sampling the V_{out} just before the reset clock arrives. In addition to eliminating the need for an additional mixer circuit in the conventional setup, the proposed technique does not require an LPF or averaging circuit. As through the correct timing of the resetting, all amplification, mixing, and averaging functions can be achieved. Another inherited advantage of this method is that the generation of *reset_real* and *reset_imag* clock does not need complex circuitries. A comparator circuit with $\sin(\omega t)$ or $\cos(\omega t)$ inputs can create the needed reset clocks. Alternatively, a divide-by-4 generator that accepts the 4ω reference clock as in [4] can be adopted.

The drawback of the mixing integrator approach is that the real and imaginary components of current through the working electrode requires to be measured in a time-interleaved manner. The driver of the S_{reset} switch needs to be adjusted separately for the real and imaginary part measurements. For example, once the real part measurement is completed with the *reset_real* timing scheme, S_{reset} should be driven by the *reset_imag* for the imaginary portion and vice versa. This situation extends the total EIS measurement duration, but does not alter the result. In the case of obtaining real and imaginary parts of the current simultaneously is necessary, additional capacitive TIA needs to be introduced. In such a scenario, the conventional technique is favorable since it allows using more than one mixer with a single amplifier.

III. Simulation Results

On-chip electrode arrays were designed and fabricated in different unit sizes and spacings. The aluminum base of the sensing electrodes was manufactured by utilizing the pad openings in a standard CMOS process without needing post-processing, and it was gold plated using the electroless deposition technique [8]. The circuit model depicted in Fig. 3 was measured with WE in the dimensions of 66 μm x 66 μm for the frequency range of 10 Hz to 10 kHz. The equivalent model between the RE and WE was characterized in a phosphate-buffered saline solution with an external platinum CE and Ag/AgCl RE.

In order to verify the analytical calculation in the previous section, a simulation testbench was created in 0.18 μm CMOS technology. The recycling folded cascode amplifier topology is selected for the capacitive feedback TIA architecture due to its higher gain, bandwidth, and slew rate performance for the same power and area usage in the conventional topology [9]. Additionally, a design technique based on the g_m/I_D characteristic is employed to provide a clear strategy for the optimum design [10]. The amplifier is designed to have a DC gain of

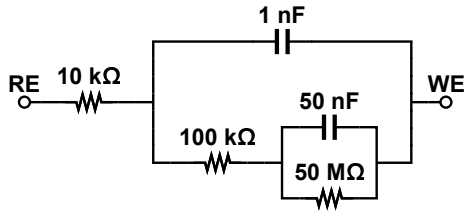

Fig. 3. The circuit model used to validate the proposed technique.

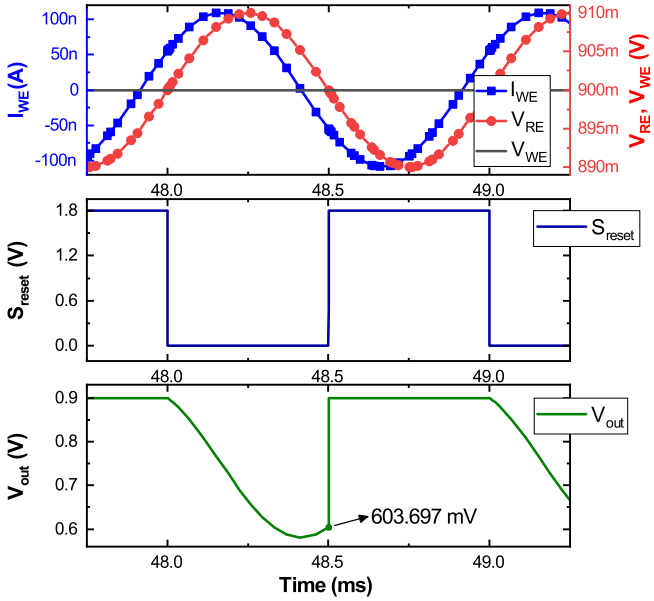

Fig. 4. I_{WE}, V_{RE}, V_{WE}, S_{reset} clock in $reset\_real$ timing scheme and V_{out}.

60 dB, unity-gain bandwidth of 3.9 MHz, and phase margin of 83 degrees for a 100 pF capacitive load while consuming 0.74 mW power from a 1.8 V supply.

As an example case, a sine wave at 1 kHz frequency and 10 mV amplitude is applied between the RE and WE. The simulation setup is completed with the 100 pF feedback capacitor and an NMOS transistor switch. The simulated waveforms for the I_{WE}, V_{RE}, V_{WE}, S_{reset} clock, and V_{out} are plotted in Fig. 4 when the $reset\_real$ clock timing is selected as the driver of the reset switch, S_{reset}. Equation (5) implies that the V_{out_real} is negative for the specified integrating time frame. However, the actual circuit implementation is limited by the supply voltage of 1.8 and the ground. Therefore, the mixing integrator's reference voltage, V_{ref}, is selected as 900 mV to achieve a V_{out} in the range operating voltage. In this scenario, the simulated V_{out_real} value just before the resetting phase becomes 603.697 mV. The $reset\_imag$ clock signal is selected as in (6) since there is no polarity problem. The simulated waveform for this selection is presented in Fig. 5 and V_{out_imag} value is found as 1.073 V.

The applied V_{ref} potential requires the simulated output voltages to be subtracted by 900 mV before further calculation. Using the (5) and (6), and converting the admittance to

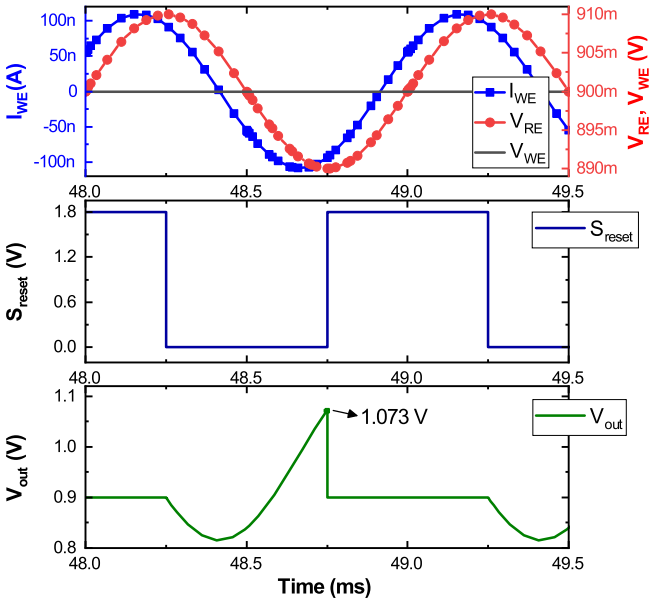

Fig. 5. I_{WE}, V_{RE}, V_{WE}, S_{reset} clock in $reset\_imag$ timing scheme and V_{out}.

TABLE I
ANALYTICAL AND SIMULATED PARAMETERS FOR THE CIRCUIT MODEL IN FIG. 3 AT 1 KHZ FREQUENCY

	Analytical	**Simulation**	**Error (%)**
$\mathbf{V_{out\_real}}$	600.517 mV	603.697 mV	0.53
$\mathbf{V_{out\_imag}}$	1073.063 mV	1073.187 mV	0.01
$\mathbf{Z_{re}}$	80.077 kΩ	79.680 kΩ	0.49
$\mathbf{Z_{im}}$	-46.814 kΩ	-46.040 kΩ	1.65

impedance, the real (Z_{re}) and imaginary (Z_{im}) parts of the electrochemical cell impedance can be calculated as 80.077 kΩ and -46.814 kΩ, respectively. Compared to the real and imaginary portion of the analytical impedance at 1 kHz, 79.680 kΩ and -46.040 kΩ, there is only a 0.49% error in the real part while a 1.65% error in the imaginary part calculation. Table I provides the summary for analytical and simulated values for the circuit model in Fig. 3 at 1 kHz frequency.

To validate the proposed technique for different operating frequency, the frequency of the applied sine wave is swept from 10 Hz to 10 kHz. Fig. 7 presents the analytical and simulated Nyquist plots for the validation of the proposed method: negative imaginary part of impedance, Z_{im}, as a function of the real part, Z_{re}, with frequency as a parameter. The simulations show a good agreement between the proposed method and the analytical solution. The error remains below 1.03% and 2.41% for real and imaginary part calculations, respectively.

IV. CONCLUSION

This paper introduces a new power and area efficient mixing integrator technique for FRA to be used in the EIS measurements. The careful selection of the reset clock of capacitive TIA eliminates the need for mixers and LPF in the conventional topology. Compared to the conventional FRA, the proposed method reduces power and silicon area usage as well as design complexity. The analytical expressions were derived to explain the operation principles, and simulations verified the approach for an example sensor model in the frequency range of 10 Hz and 10 kHz. The usage of the proposed technique can be extended to any other sensor model. The proposed circuit was sent for fabrication in 180nm CMOS together with an array of on-chip electrodes for fully integrated electrochemical sensing and EIS.

The future work includes conducting EIS experiments using on-chip and off-chip sensors to validate the proposed method in action.

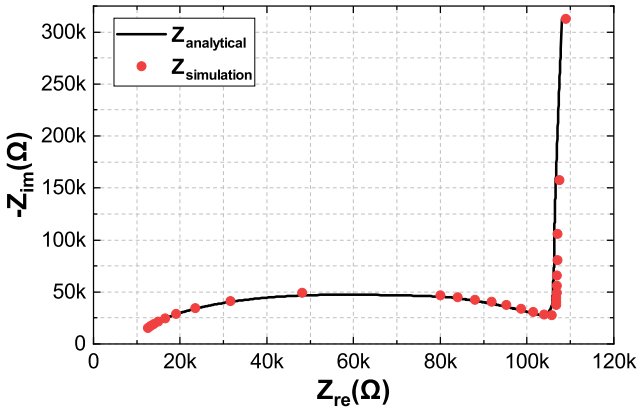

Fig. 6. The analytical (using Fig. 3) and simulated Nyquist plots for the validation of the proposed method.

REFERENCES

[1] A. J. Bard and L. R. Faulkner, *Electrochemical methods: fundamentals and applications*, 2nd ed. New York: Wiley, 2001.

[2] S. Ghoreishizadeh and S. Sharma, "Continuous Glucose Monitoring Sensors for Management of Diabetes: State-of-the-Art and Future Perspectives," in *Handbook of Biochips*, M. Sawan, Ed. New York, NY: Springer New York, 2021, pp. 1–17.

[3] A. Lasia, *Electrochemical Impedance Spectroscopy and its Applications*. New York, NY: Springer New York, 2014.

[4] A. Manickam, A. Chevalier, M. McDermott, A. D. Ellington, and A. Hassibi, "A CMOS Electrochemical Impedance Spectroscopy (EIS) Biosensor Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 6, pp. 379–390, Dec. 2010.

[5] D. Rairigh, A. Mason, and C. Yang, "Analysis of On-Chip Impedance Spectroscopy Methodologies for Sensor Arrays," *Sensor Letters*, vol. 4, no. 4, pp. 398–402, Dec. 2006.

[6] H. Jafari, L. Soleymani, and R. Genov, "16-Channel CMOS Impedance Spectroscopy DNA Analyzer With Dual-Slope Multiplying ADCs," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, no. 5, pp. 468–478, Oct. 2012.

[7] D. Kim, B. Goldstein, W. Tang, F. J. Sigworth, and E. Culurciello, "Noise Analysis and Performance Comparison of Low Current Measurement Systems for Biomedical Applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 1, pp. 52–62, Feb. 2013.

[8] A. A. Gill and S. S. Ghoreishizadeh, "Surface characterization techniques of gold coated micro-electrodes," in *BioMedEng22*, 2022.

[9] R. S. Assaad and J. Silva-Martinez, "The Recycling Folded Cascode: A General Enhancement of the Folded Cascode Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2535–2542, Sep. 2009.

[10] P. G. A. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*. Cambridge University Press, 2017, book Title: Systematic Design of Analog CMOS Circuits.