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Microstructural buffer effects in AlGaN/GaN high electron mobility transistors

Microstructural Buffer Effects in AlGaN/GaN High Electron Mobility Transistors

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Abstract

Efficient and reliable electronic devices beyond silicon technology are necessary to handle the ever-growing demand for electric power and advanced electronic technologies. Wide band gap semiconductors entailing high breakdown field characteristics are the ideal candidates to meet the demand for revolutionary power and communication electronics. Particularly gallium nitride (GaN) is a suitable material given its ability to form a 2D electron gas (2DEG) combined with the high electron mobility resulting in high device performance. Despite the great material properties and past research progress, many challenges remain for GaN technology, particularly when silicon substrates are used. The device buffer is one key component to ensure a high vertical breakdown voltage, however, it is prone to different liabilities compromising the device performance. Defects and impurities are inherently or deliberately incorporated during buffer growth defining the electronic properties during device operation. Understanding their behavior upon external stress imposed by the device operation or its environment is crucial to ensure stable and reliable device performance.

Dislocations are an inevitable consequence of GaN growth on silicon substrates given the different lattice properties. Threading dislocations have been found to act as localized vertical conductive paths jeopardizing the breakdown characteristics of the buffer. A novel measurement methodology combining Kelvin Probe Force Microscopy (KPFM) and substrate bias ramps was developed in order to probe the role of vertical leakage paths during off-state stress. KPFM measurements under high negative back bias show local drops in surface potential related to local 2DEG depletion regions at the location of conductive dislocations. A model is presented correlating the observed surface potential effect to large deformations of the off-state buffer potential around threading dislocations causing high localized electric field stress in the channel. The measurement suggests that breakdown is more of a localized phenomenon instead of a bulk buffer effect.

Dopants such as carbon are used to make the buffer more insulating. The doping profile with depth is specifically engineered to maintain ideal channel properties while ensuring good blocking and dynamic switching performance of the buffer. However, the resulting electronic band structure and charge concentrations are sensitive to illumination changing the charge distribution across the buffer. Absorption of ultraviolet (UV) light with an energy greater than the GaN band gap increases the channel conductivity which recovers only over long periods of time, known as persistent photoconductivity (PPC). The effect was measured and simulated for a wide range of device configurations. It is shown how light absorption and charge generation affect the electronic band diagram and charge distribution in the buffer. The magnitude of the effect is found to be directly related to the net doping density (difference of acceptor concentration and donor concentration), especially in the channel layer. This proposes that the UV-induced PPC effect can be used to determine the net doping density, a quantity that is extremely difficult to measure by any other method.

Dedication

To the future me.

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The thesis would have not been possible without the help and support of many people, both in the professional environment and in private life.

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AUTHOR'S DECLARATION

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

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CHAPTER 1

INTRODUCTION

One major challenge of the current day and age is the transition from fossil fuels to renewable energies as well as the sustainable and efficient use of our resources [1]. The ambition has encouraged vast developments of innovative ways to power vehicles using electric motors instead of traditional fossil fuel combustion engines [2]. Forecasts predict that by the year 2040, the global number of electric or hybrid vehicles will be on the order of 300 million [3–5]. Combined with further technological advancements such as autonomous driving and enhanced infotainment experience, highly efficient electronic devices will be in high demand in the mobility sector [6]. With the constant increase in technological improvements for society and the economy as well as growth in worldwide population, global electricity consumption is expected to increase by 50 % by 2050 [7]. Currently, an estimated 25 % of electricity is wasted due to inefficient power electronics and load technologies which shows the huge power-saving potential and necessity for highly efficient power electronics [8].

At the moment, the majority of power electronics is based on silicon, partially due to its availability and low cost. However, the field of silicon power electronics has seen a stagnation in performance improvements in the last years, ultimately owing to the limitations of silicon. Novel device structures such as superjunction configurations pushed the silicon technology beyond its restrictions related to its inherent material properties, however, there are also limits with new device concepts. Overcoming these limitations means exploring alternative semiconductors with a wider band gap that can enable high efficiencies as well as high power densities combined with low manufacturing costs [9]. Introducing gallium nitride (GaN) for power electronics is expected to revive Moore's law and has already achieved an increasing amount of commercialization [10]. Based on its wider band gap than silicon, a GaN device can withstand a breakdown field of $3.3\,\mathrm{MV\,cm^{-1}}$, which is ten times higher than silicon [11]. Therefore, GaN devices can operate

at much higher voltages using the same device dimensions. GaN also has an inherently high charge carrier mobility of up to $2000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ allowing high electron saturation velocities, low conduction losses as well as high switching speeds. Ultimately, those factors lead to higher switching frequencies without increased switching losses while enabling smaller sizes of passive electronic components [12]. On top, the improved efficiency simplifies thermal management. GaN devices are therefore not only the choice for high power and high voltage switching applications but they also enable compact circuit designs with higher power densities [13]. This makes GaN-based devices financially competitive to silicon within the power electronics market. Combined with the increased performance, GaN is expected to displace silicon in the multi-billion US-Dollar market of high voltage power converters [14].

To illustrate the potential of power savings, consider the example of data centers which are major energy consumers today. A typical data center does not even use half of the overall consumed power for the computation work which includes disk drives, memory, and microprocessors. The majority of power is lost in power conversion and distribution as well as facility cooling [15]. Several conversion steps are necessary to change from the high AC voltage supplied by the electric grid down to a few volts of DC power as required by digital processing chips. Conventional power supplies and conversions today have an overall system efficiency of about 73 % [16]. Using GaN technology with its high voltage capabilities instead of silicon-based converters leads to fewer required steps in this voltage down-conversion in addition to a higher efficiency at each step. That also improves thermal management by reducing the heat that needs to be removed using air conditioning. Every joule of heat to be removed requires roughly half a joule of electricity [17]. Thus, any efficiency-saving effect is cascaded to thermal management. Using GaN devices, the power conversion process for data centers can achieve efficiencies as high as 97 % [18, 19]. With data centers currently consuming about 3 % of all energy in Europe, a 20 percentage points more efficient power conversion process combined with improved thermal management could potentially save nearly 1 % of all electricity consumed in Europe [20]. The steady growth in number and size of data centers multiplies the entire savings effect [21].

Historically, it has already been a long journey of advancements for GaN High Electron Mobility Transistors (HEMT) to reach todays' level of commercialization. The early focus of research in the 1960s was on the pure material properties of GaN. First successful growth of GaN on a foreign substrate dates back to 1969 when Maruska *et al.* reported a large area single-crystalline GaN layer grown on a sapphire substrate [22]. As pristine GaN tends to have an n-type nature, researchers looked into suitable p-type dopants in order to create a p-n junction which is required for many electronic devices. Akasaki *et al.* demonstrated the first p-type GaN using magnesium as dopant in 1991 [23]. Nakamura *et al.* improved the electric conductivity by deploying high-temperature annealing in nitrogen atmosphere. [24]. Amano *et al.* improved the GaN material quality for GaN films grown on sapphire substrates by means of using an aluminium nitride (AlN) nucleation layer grown at low temperature [25]. Those advancements

massively contributed to the development of the blue light-emitting diode (LED) which makes it possible to build an LED with an overall white light spectrum. Consequently, in 2014, the Nobel committee awarded the Nobel prize in physics to the three leading scientists Isamu Akasaki, Hiroshi Amano, and Shuji Nakamura [26].

The first major discovery towards a functional transistor was the observation of a two-dimensional electron gas (2DEG) at an AlGaN/GaN heterojunction in 1992 [9]. Shortly afterwards in 1993, Khan *et al.* reported the first successful GaN HEMT grown on a sapphire substrate [27]. However, sapphire had a considerably large lattice mismatch leading to a high density of dislocations and consequently low GaN quality resulting in high leakage currents. In addition, sapphire has a relatively low thermal conductivity limiting high power applications due to heat management problems. The sapphire substrate was therefore replaced with silicon carbide (SiC) by Binari *et al.* in 1997. GaN-on-SiC has a less defective material quality with a dislocation density as low as $10^8\,\mathrm{cm}^{-2}$ and thus remains the choice for state-of-the-art high performance GaN-based devices up to today [28]. However, SiC substrates are very costly and limited to a small wafer area. This clearly hinders GaN for mass adoption competing with the cheap large-scale production of silicon-based (Si) devices. It took until the year of 2000 for the development of an affordable GaN-on-Si substrate technology. Silicon had the great advantage of having well-engineered and well-established processing facilities as well as the existing vast knowledge of its electronic properties and behavior [29]. However, implementing silicon as substrate material came at the cost of a large lattice mismatch and a different thermal expansion coefficient. The latter causes tensile stress resulting in significant wafer bow and cracks in the epitaxial layers which ultimately complicates GaN-on-Si wafer processing. This challenge was tackled by introducing graded AlGaN buffers or an AlN/GaN superlattice structure to reduce the tensile strain and wafer bow which improved the GaN film quality. Nevertheless, the typical dislocation density on the order of $10^9\,\mathrm{cm}^{-2}$ is still relatively high compared to GaN grown on SiC [30].

Along with improving the growth of the GaN, vast efforts went into the optimization of the device design. Owing to the spontaneous piezoelectric polarization, regular GaN HEMTs are normally-on devices operating in depletion mode. However, from a circuit design perspective, normally-off devices are favorable. On the one hand, this characteristic can be achieved with a small circuit combining a normally-on GaN device with a low voltage silicon MOSFET. On the other hand, a 'true' normally-off GaN HEMT requires a positive threshold voltage by itself. This can be accomplished via removal of the 2DEG underneath the gate by deposition of a p-type layer underneath the gate [31], by a tri-gate configuration [32], by implantation of negatively charged ions [33], or by a barrier recess [34]. Field plates create additional gate regions that help reshape the electric field and redistribute the potential drop across the entire gate-drain distance. That improves the breakdown characteristics by a multitude of up to five and is therefore important for high voltage power transistors [35].

The first time GaN HEMTs became commercially available was in 2004. The device was a depletion-mode radio frequency (RF) device. Ever since then, many companies started their development process and joined the competition [36]. Vast improvements have already made GaN HEMTs a bigger player in the high power and high frequency market. However, device reliability is still a big concern limiting broad market adoption. Material defects incorporated during wafer growth can become a center of degradation, especially under high voltage operation. While many of the surface-related effects have been tackled by optimized gate and field plate design as well as various passivation layer configurations, the GaN buffer still requires a lot of research attention. The main purpose of the GaN buffer is constraining the 2DEG at the AlGaN/GaN interface, suppressing high source-gate leakage under off-state conditions, and sustaining a high vertical breakdown field between channel and substrate. In order to achieve this goal, the buffer is typically extrinsically doped with iron or carbon which both introduce trap states with deep energy levels into the GaN band gap. Iron doping is usually the choice for RF applications. Doping densities on the order of 10^{18} cm^{-3} have shown to suppress buffer leakage under off-state conditions and reduce buffer-related current collapse (CC) [37]. For power applications, on the other hand, iron doping struggles to achieve sufficient off-state leakage suppression as well as a high breakdown voltage. Carbon doping is more suitable here as its acceptor trap energy level is much deeper in the band gap. Though, using carbon doping with typical densities around 10^{19} cm^{-3} comes with the tradeoff of inducing strong so-called dynamic R_{ON} [38]. Dynamic R_{ON} is associated with a significant increase in the on-resistance right after the device was held in off-state condition. During off-state, the transistor needs to block high voltages resulting in high electric fields which can cause electrons to get trapped around the channel. The recovery can happen on a broad range of time constants (milliseconds to thousands of seconds) which is not ideal for reliable device operation [39]. A similar problem with trapped charges and long recovery time constants of up to weeks is caused by the persistent photoconductivity effect upon UV light illumination. This effect prevents the same operation characteristics in different environments. Another key factor to achieve a high breakdown resilience is the thickness of the buffer. A highly resistive and thick buffer ensures high vertical breakdown fields. However, when grown on a silicon substrate, the thickness is limited to about 7 µm due to strain management in order to maintain good material quality [40, 41]. Nevertheless, lattice defects such as threading dislocations are inherently incorporated into the buffer during GaN growth on foreign materials. Dislocations can provide vertical leakage paths compromising the device breakdown capabilities [42]. All the effects mentioned above need further research to mitigate the consequences and advance the GaN HEMT performance.

This thesis will mainly focus on microstructural buffer effects induced by off-state stress or illumination. The following two chapters explain the necessary theoretical background and measurement techniques. The first research part of the thesis examines the effect of vertical conductive paths related to threading dislocations during off-state stress. For that study, a

new measurement methodology is developed by combining back bias ramps with Kelvin Probe Force Microscopy (KPFM). One chapter describes the technical development process and how hurdles were mitigated or overcome. Most problems stem from the fact that both techniques operate in different voltage regimes: back bias ramps in the hundreds of volts and KPFM in the millivolts. It also includes the first measurements with dislocation-related surface potential features induced by a large back bias. The subsequent chapter focuses on the physics of the observed effect. Simulations are used to help understand the influence of biased conductive paths in the buffer causing large buffer potential deformations around conductive paths which redirects the main electric field stress onto the channel. This effect has significant implications for device breakdown. As this is the first measurement of its kind to the author's knowledge, many repetition measurements on other samples of the same wafer are shown in the appendix to validate reproducibility of the data. The second part of the thesis investigates the UV-induced persistent photoconductivity effect. One chapter includes a study which focuses on buffer-related effects caused by UV light illumination. Photons are absorbed in the buffer influencing the electronic state of the buffer layers which in return changes the channel conductivity. Given the long time scale of days to weeks, this effect has implications for stable device performance under varying device environments. Simulations are used to correlate experimental results with material properties such as doping. As the effect depends highly on buffer doping, it can be leveraged to measure the net active doping density (difference of acceptor concentration and donor concentration) in the buffer, particularly in the channel region. This quantity is very difficult to determine by any other methods. For the investigated set of samples, the buffer-related effect was sufficient to explain the experimentally observed magnitude of the effect. The final chapter is building on the previous one using a different set of samples that reveal a significantly higher UV-induced increase in channel conductivity which cannot be purely achieved by the previously considered buffer effect. The hypothesis of an additional surface-related effect is explored. While this can be shown qualitatively, the high instability and poor reliability of the samples between repeated measurements prevented any quantitative analysis.

CHAPTER 2

THEORETICAL BACKGROUND

This chapter outlines the basic GaN material properties and growth processes. It also targets details related to AlGaN/GaN heterostructures and the GaN polarization effects which are the foundation of the AlGaN/GaN high electron mobility transistor (HEMT). It will also give an overview of device design, fabrication, and operation. Lastly, this chapter will cover key AlGaN/GaN HEMT reliability factors.

2.1 Gallium nitride

The research on GaN dates back to the 1960s with exploring different growth techniques and conducting first basic material analyses. First academic efforts using GaN to build functional devices such as a HEMT for power and high frequency applications started in the 1990s [43]. First commercial interest developed in the early 2000s and has gone a long way since [44].

2.1.1 Crystal structure and semiconductor properties

Gallium (Ga) nitride (N) is a group III-V semiconductor crystallizing in two structures: cubic zinc blende and wurtzite. The latter is thermodynamically more stable and is thus the preferred choice for electronic devices. Therefore, in this thesis, GaN refers to the wurtzite crystal structure, shown in fig. 2.1. The crystal structure is a hexagonal system with interpenetrating close-packed lattices with tetrahedrally arranged Ga atoms and N atoms as well as shifted by 5/8 along the c-axis. Each unit cell consists of two Ga atoms and two N atoms. It belongs to the space group C_{6v}^4 ($P6_3mc$) which means that the structure has no inversion symmetry in the c-plane. Combining the significant difference in electronegativity of Ga and N, this lack of inversion symmetry causes an intrinsic internal polarization effect and enhanced piezoelectric polarization when the crystal

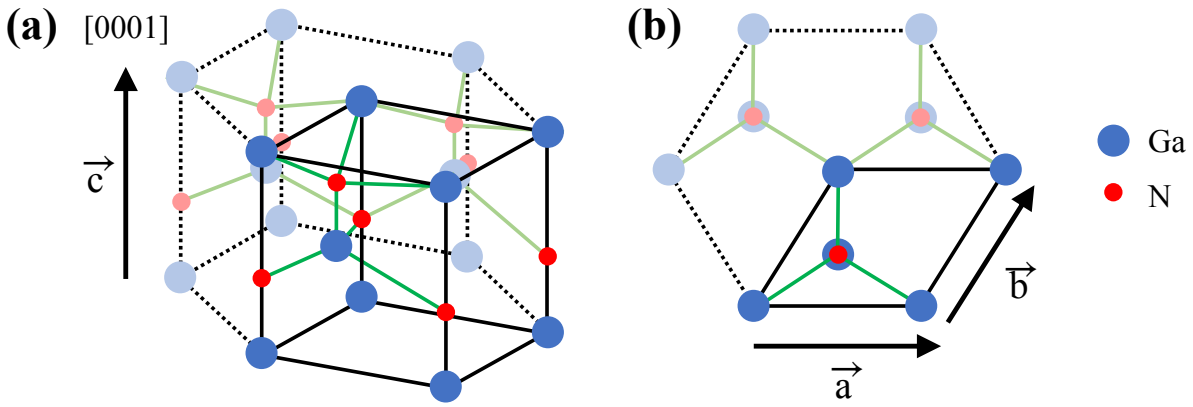

FIGURE 2.1. Wurtzite crystal structure of GaN. a) Primitive unit cell with positions of Ga and N atoms with the Ga-face at the bottom plane and the tetragonal bonding of one Ga atom to four N atoms in green. b) Plane view along the c-axis.

is exposed to compressive or tensile strain along the c-axis [45]. Another consequence is the two possible surfaces [0001] (Ga-face) and [000$\bar{1}$] (N-face) with different mobilities and surface chemistries. The Ga-face is more common for GaN HEMTs [46].

In order to evaluate certain crystal properties such as diffraction characteristics and electronic properties, the structure is first converted into the reciprocal space representing the momentum space. In the reciprocal space, the wurtzite crystal structure relates to a hexagonal prism as primitive unit cell and first Brillouin zone, also called Wigner–Seitz cell. The coordinate system in this momentum space is comprised of the wave vectors k_x, k_y, and k_z related to the Cartesian coordinate system [47]. The vector $\mathbf{k} = 0$ representing zero momentum sets the center of the Brillouin zone which is called Γ point. Similar to the crystal structure in the real space, there are several orientations of high symmetry in the Brillouin zone in the reciprocal space as shown in fig. 2.2a [48]. The electronic band structure in form of the energy–momentum relation can be computed using the periodic crystal potential $V(\mathbf{r})$ in the momentum space with vector $\mathbf{k}$ and the Schrödinger equation

$$\left(\frac{-\hbar^2}{2m^*}\nabla^2 + V(\mathbf{r})\right)\Psi(\mathbf{r},\mathbf{k}) = E(\mathbf{k})\,\Psi(\mathbf{r},\mathbf{k}) \tag{2.1}$$

with m^* being the carrier effective mass, Ψ as the wave function and E representing the carrier energy. Solving this equation in every momentum state constructs the electronic band diagram shown in fig. 2.2b. The minimum of the conduction band as well as the maximum of the valence band are located in the center of the band structure. Therefore, conduction in GaN mostly occurs at the Γ point where bands are the closest to the Fermi level. The curvature of a band inversely relates to the effective mass m^* of the respective carrier. In GaN, that reflects a higher effective mass for holes (m_h^*) than for electrons (m_e^*). Furthermore, the valence band at the Γ point consists of two bands with high and low curvature leading to light and heavy holes, respectively. Since the

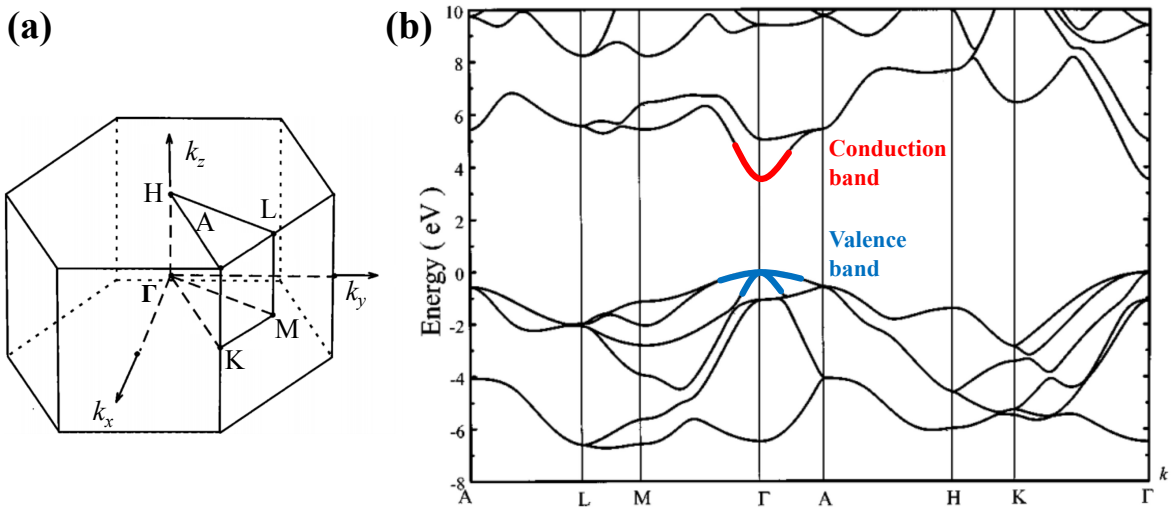

FIGURE 2.2. Wurtzite GaN band structure with a) the Brillouin zone highlighting labeled points of high symmetry as well as b) the band diagram and labeled valence band for heavy holes (milder curvature) and light holes (stronger curvature) plus conduction band for light electrons. Adapted from [49].

mobility on the other hand is inversely proportional to the carrier effective mass, the electrons have higher mobility than holes and are therefore the dominant charge carrier in GaN HEMTs. As the curvature of the conduction band differs for the Γ-A and Γ-M path, the effective mass of electrons is anisotropic with $m_e^{*\perp} = 0.18\,m_0$ and $m_e^{*\parallel} = 0.2\,m_0$ for the direction perpendicular and parallel to the c-axis, respectively [50]. The direct band gap makes GaN an excellent candidate for optoelectronic devices like solar cells and light-emitting diodes since photons do not carry momentum and can only induce direct band transitions. With the aid of a phonon, indirect band transitions are possible as well. Furthermore, the large GaN band gap of 3.4 eV means a high electric field is required for impact ionization as well as breakdown with further explanation in section 2.5. For a material with a direct band gap, the breakdown field increases with the band gap to the power of about 2.5 which makes GaN an ideal candidate for high power applications as shown in section 2.1.4 [51].

2.1.2 Polarization effect in nitride compounds

GaN belongs to the family of group III-V nitrides which form a crystal with polar characteristics given the different electronegativities of the atoms in each group. Particularly, nitrogen is the smallest and therefore most electronegative atom in group V. Nitride semiconductors occur in the wurtzite structure which has a high symmetry enabling spontaneous polarization (P_{SP}) [52]. The wurtzite crystal also has three non-vanishing independent piezoeletric tensor component enabling an overall strain-induced/piezoelectric polarization (P_{PZ}) [53]. Both types of polarization

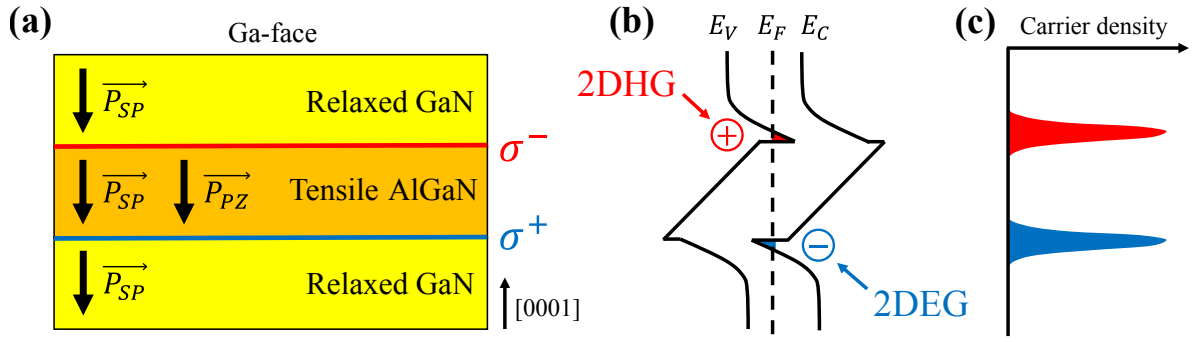

FIGURE 2.3. Heterojunction polarization with a) the GaN/AlGaN/GaN stack yielding interface charges, b) the consequential band diagram, and c) the resulting charge carrier accumulation.

are further explained below. With the absence of an external electric field, the total polarization P_{total} is therefore defined by

$$P_{total} = P_{SP} + P_{PZ} + P_{external} \tag{2.2}$$

with an external polarization $P_{external}$.

Spontaneous polarization: This effect relates to the equilibrium polarization without present strain and is mainly defined by the unit cell of the crystal. In the case of GaN, the anion–cation bond is along the c-axis. The strong electronegativity caused by the Coulomb potential of the N nucleus attracts the outer orbital electrons of the Ga atom which polarizes the connection. Combined with the absence of an inversion symmetry along the c-axis, this results in a macroscopic spontaneous polarization along the [0001] direction [54].

Piezoelectric polarization: GaN is typically grown on an underlying layer which inevitably introduces lattice mismatches and leads to stress incorporation within the materials. The resulting strain induces crystal distortions which lead to piezoelectric polarization. In the linear range, the piezoelectric polarization field can be expressed by

$$P_{PZ,\,i} = \sum_j e_{ij}\,\epsilon_j \tag{2.3}$$

with the piezoelectric constants e_{ij} and the crystal deformation ϵ_j. The equation shows that any crystal distortion along the c-axis can cause a change in macroscopic piezoelectric polarization [55].

2.1.3 Polarization in heterostructures

As discussed in the previous section, piezoelectric polarization is due to strain induced by lattice mismatches. Wurtzite AlN shows similar electronic band structure characteristics as GaN,

however, one key difference for AlN is the wider band gap of 6.1 eV. AlN also has a greater spontaneous polarization than GaN. The polarization field of AlGaN can be approximated as nonlinear interpolation between AlN and GaN. Growing a heterostructure as combination of GaN and AlGaN with sudden changes in Al content causes a spontaneous polarization discontinuity facilitated by induced piezoelectric polarization changes due to different lattice parameters. The discontinuity in the polarization field leads to an interface charge σ by accumulation of free charge carriers as shown in fig. 2.3. The polarity of the interface charge determines the formation of either a two-dimensional electron gas (2DEG) or a two-dimensional hole gas (2DHG). The change of polarization field across an interface between materials A and B defines the density of the sheet-like interface charge [56]

$$\sigma_{AB} = \left(P_{SP}^{A} + P_{PZ}^{A}\right) - \left(P_{SP}^{B} + P_{PZ}^{B}\right) . \tag{2.4}$$

In order to maintain charge balance across the structure, the electrons forming the 2DEG must cause a counterbalancing region with net positive charge balance. In AlGaN/GaN HEMTs, the origin of the electrons is attributed to surface donor states located at the AlGaN barrier surface with an energy level E_D [57]. For a Fermi level above E_D, the surface donor remains occupied as shown in fig. 2.4a. As soon as the Fermi level drops below E_D, the surface donor becomes ionized. The released electron transfers to empty conduction band states at the AlGaN/GaN interface creating the 2DEG as seen in fig. 2.4b. This mechanism also explains the necessity for a minimum barrier thickness to make surface state become unoccupied. For an $Al_{0.34}Ga_{0.66}N$ barrier, the minimum barrier thickness was determined to be about 3.5 nm as shown in fig. 2.4c [58]. Increasing the Al content increases the polarization field which in return lowers the minimum barrier thickness. However, there is a practical limit since an Al content too high causes poor material quality due to a higher lattice mismatch between channel and barrier leading to strain-induced crystal defects with cracks in extreme cases [59]. This can introduce deep-level defects at the barrier interface lowering the electron sheet mobility and ultimately deteriorating the device performance [60]. On the other hand, introducing a thin AlN spacer of a few nanometers at the AlGaN/GaN interface helps remove strain by allowing a smoother transition between both materials [61]. This interlayer has the additional advantage of reducing alloy disorder scattering leading to increased electron mobility along the channel [62].

2.1.4 GaN and other semiconductors for power applications

There are several considerations when choosing the semiconductor for a power transistor device. The ideal power transistor blocks any voltage in off-state and switches instantly to on-state without parasitic capacitive losses. Furthermore, it has an infinite off-resistance and zero on-resistance as well as no losses during switching between off-state and on-state. On top, it does not have reliability and degradation issues. In reality, power devices are not 100 % efficient and are mainly losing energy during switching by producing heat which needs to be drained away.

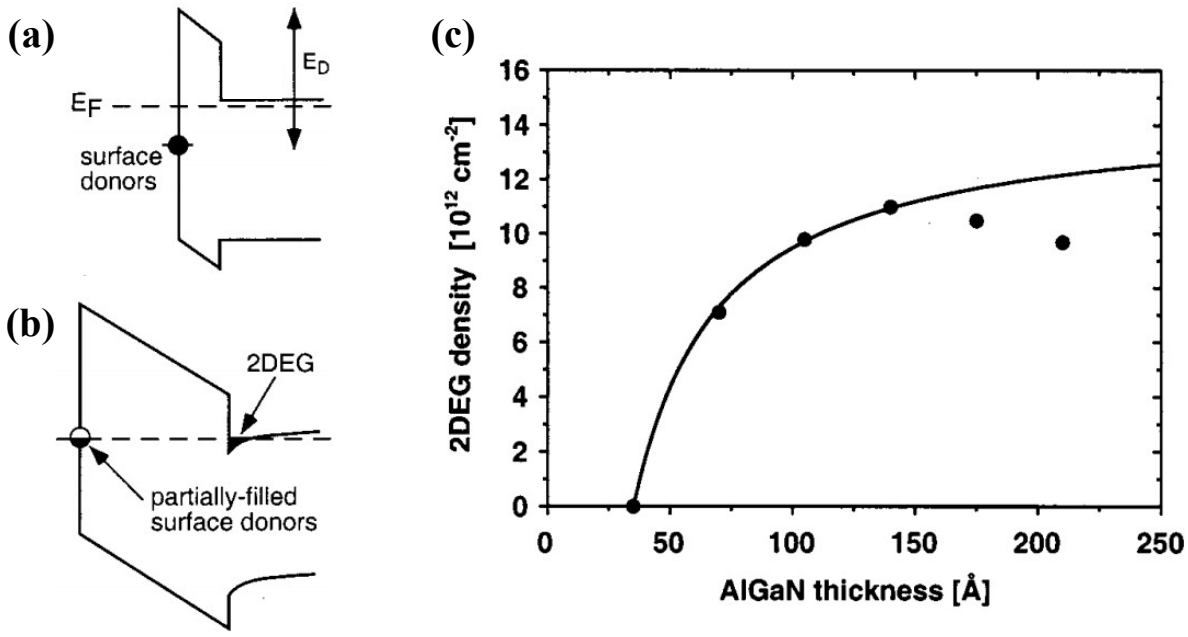

FIGURE 2.4. Formation of the 2DEG by ionization of surface donors with a) the energy level of the surface donor state at E_D, b) the ionization of the surface donors creating the 2DEG, and c) the 2DEG density as a function of barrier thickness of $Al_{0.34}Ga_{0.66}N$. The deviation above 140 Å was related to strain relaxation issues. Adapted from [58].

Aiming for the listed favorable characteristics, there are several semiconductors aside from GaN to choose from when configuring a power device. The Baliga figure of merit (BFOM) measures the suitability of a semiconductor for power switching application. It is defined by

$$\text{BFOM} = \epsilon \mu E_{BD}^3 \tag{2.5}$$

with the dielectric constant ϵ, charge carrier mobility μ and breakdown field E_{BD}. As evident in the equation, an increase in E_{BD} has the highest impact on the BFOM given the exponent of 3. For semiconductors with a direct band gap, E_{BD} itself is directly related to the band gap E_G by

$$E_{BD} = 1.7 \times 10^5 \, (E_G)^{2.5} \tag{2.6}$$

with an exponent of 2.5 highlighting the significance of the band gap on the BFOM with a compounded exponent of 7.5 [51].

Key parameters of popular materials for power applications are summarized in tab. 2.1 alongside the BFOM in comparison to Si. Given the wider band gap, especially 4H-SiC, GaN, and diamond have a breakdown field that is a multitude of the one of Si. A higher band gap means that much higher temperatures are required to thermally excite electrons from the valence band to the conduction band. Consequently, those materials can operate at a higher

TABLE 2.1. Intrinsic bulk properties of several semiconductors at 300 K considered for power applications [63–72].

	Band gap (eV)	Dielectric constant	Breakdown field ($MV\,cm^{-1}$)	Thermal conductivity ($W\,m^{-1}\,K^{-1}$)	Electron mobility ($cm^2\,V^{-1}\,s^{-1}$)	BFOM relative to Si
Si	1.12	11.8	0.3	148	1350	1
GaAs	1.42	13.1	0.4	56	8500	17
4H-SiC	3.26	10.0	2.0	280	720	134
GaN	3.44	9.5	3.3	160	370	294
β-Ga_2O_3	≈ 4.7	10	7 – 8	11 ([100])	200 – 300	1595 – 3571
C (diamond)	5.47	5.9	10	2000	4500	61728

temperature. 4H-SiC has the highest thermal conductivity among those three candidates which facilitates thermal management improving device reliability. Therefore, 4H-SiC is often used in high voltage applications where its disadvantage of a high gate drive voltage is manageable. On the other hand, GaN benefits from its polar crystal structure enabling the formation of a 2DEG which allows device designs using a 2DEG channel. This offers an increase in electron mobility from a bulk value of $370\,cm^2\,V^{-1}\,s^{-1}$ (with a donor density of $1.1 \times 10^{17}\,cm^{-3}$) [64] to as high as $2000\,cm^2\,V^{-1}\,s^{-1}$ [73]. This enables operation at higher frequencies and GaN is therefore often used in high frequency applications at medium voltage. Given its favorable BFOM, the semiconductor β-Ga_2O_3 has attracted a lot of attention in the scientific community lately. The advantage of the high breakdown field enabling ultra-high voltage applications comes at the costs of a low thermal conductivity. Diamond has the highest BFOM. However, diamond is yet rather unsuitable for widespread electronic devices due to the absence of an n-type dopant [74]. There have been efforts to build unipolar devices with the p-type dopant boron, however, the acceptor ionization energy was found to be as low as 0.37 eV which leads to a rather high series resistance paired with low mobility [70].

2.2 GaN epitaxy

It is generally possible to manufacture GaN substrates, however, the growth process is expensive and the wafer size is very limited which ultimately increases device fabrication costs [75]. From a commercialization perspective, GaN devices are therefore grown on foreign substrates. The difference in material properties such as lattice parameters triggers problems such as crystal defects which can be alleviated by introducing intermediary layers. Fig. 2.5 shows a typical GaN HEMT epitaxial structure. The first layer is a nucleation layer deposited onto the substrate. It is designed to aid the initial growth process by providing a nucleation site while simultaneously

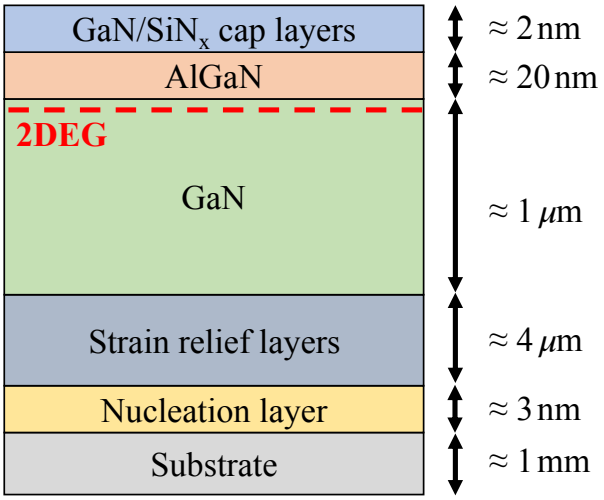

FIGURE 2.5. Typical GaN HEMT stack with typical thicknesses of the individual epitaxial layers.

protecting the substrate. For Si substrate, it is followed by the strain relief layers to overcome the lattice mismatch between the substrate and GaN. Subsequently, a GaN layer is deposited on top to ensure high vertical breakdown characteristics. The GaN layer and AlGaN barrier are creating the 2DEG functioning as device channel. The device is typically finished with a GaN cap to encapsulate the essential surface donor traps as well as a dielectric passivation layer of SiN_x to prevent oxidation. In the following, the various layers are individually discussed in more detail.

2.2.1 Substrate

There are several considerations to make when choosing a non-native substrate for GaN devices: substrate price, availability of large substrate sizes, integrability into device fabrication facilities, thermal conductivity, thermal expansion, and lattice mismatch. Especially thermal expansion is a key factor since most of the growth is performed at higher temperatures. Cooling down the wafer incorporates strain resulting in wafer bowing and cracking which in return makes subsequent device fabrication difficult. Tab. 2.2 summarizes the listed parameters for a set of the most suitable materials. Despite the low thermal conductivity and high lattice mismatch, Si has become a dominant substrate choice for power electronics, mainly driven by the low price and the availability of large area wafers. On top, Si processing and fabrication facilities are very well established which helps bring GaN to the market. The semi-insulating material SiC is a favorable choice based on the small lattice mismatch and higher thermal conductivity. Hence, state-of-the-art high performance devices are generally based on SiC where performance interest and thermal reliability outweighs the cost factor. It is therefore usually chosen for radio frequency (RF) devices as opposed to Si, also because the conductive Si substrate can couple to the channel

TABLE 2.2. Properties of several substrate candidates for GaN growth, at 300 K. From tab. 2.1 and [76, 77].

	Substrate price	Substrate size (mm)	Thermal conductivity ($W m^{-1} K^{-1}$)	Thermal expansion ($10^{-6} K^{-1}$)	Lattice mismatch with GaN (%)
GaN	very high	30	160	5.5	
Si	very low	300	148	2.6	17
SiC	high	150	280	4.5	4
Sapphire	medium	150	35	7.5	14
C (diamond)	very high	10	2000	1.0	89

leading to power losses [78]. The poor thermal conductivity of sapphire limits the maximum device output power and is therefore especially unsuitable for RF devices but rarely used in low power applications and LEDs [41, 79]. Diamond has a high thermal conductivity, however, the high lattice mismatch as well as the high substrate price and the small substrate size make broad commercialization difficult.

2.2.2 Nucleation layer and strain relief layer with formation of dislocations

If a semiconductor of different crystal parameters is grown onto a substrate with a larger lattice (fig. 2.6a), it will experience tensile stress (fig. 2.6b). The stress is relieved by creating a crystal distortion (fig. 2.6c). This dislocation typically propagates through the crystal structure. Two types of dislocations are depicted in fig. 2.6d and fig. 2.6e. Dislocations are characterized by the Burgers vector. It is determined by following an in-plane circuit around the dislocation. If the path is not returning to its origin, the path displacement is compensated by the Burgers vector. The magnitude and length of the Burgers vector relate to the type of dislocation and crystal distortion. For instance, fig. 2.6d and fig. 2.6e show an edge and a screw dislocation with Burgers vector of $1\vec{a}$ and $1\vec{c}$, respectively. Mixed-type dislocations are a combination of edge and screw dislocation. Fig. 2.7 shows transmission electron microscopy (TEM) cross-section images of different types of dislocations. The shown dislocations reach vertically through the crystal and are therefore often referred to as threading dislocations. The edge component of dislocations is usually harder to identify visually on the surface, however, when etched using a HCl vapor-phase treatment, it is easier to distinguish using the cross-sectional profile of the etched pit as seen in fig. 2.7a and fig. 2.7b [81]. Dislocations often reach from the substrate all the way to the surface but they can also terminate within the epitaxial layer, or potentially even start within it as observed in fig. 2.7c [82].

Threading dislocations have a significant impact on device reliability and performance. They are known to introduce band gap states which can trap and scatter electrons [83, 84]. Dislocations can also cause vertical leakage paths which, at a high density, cause reliability concerns and limit

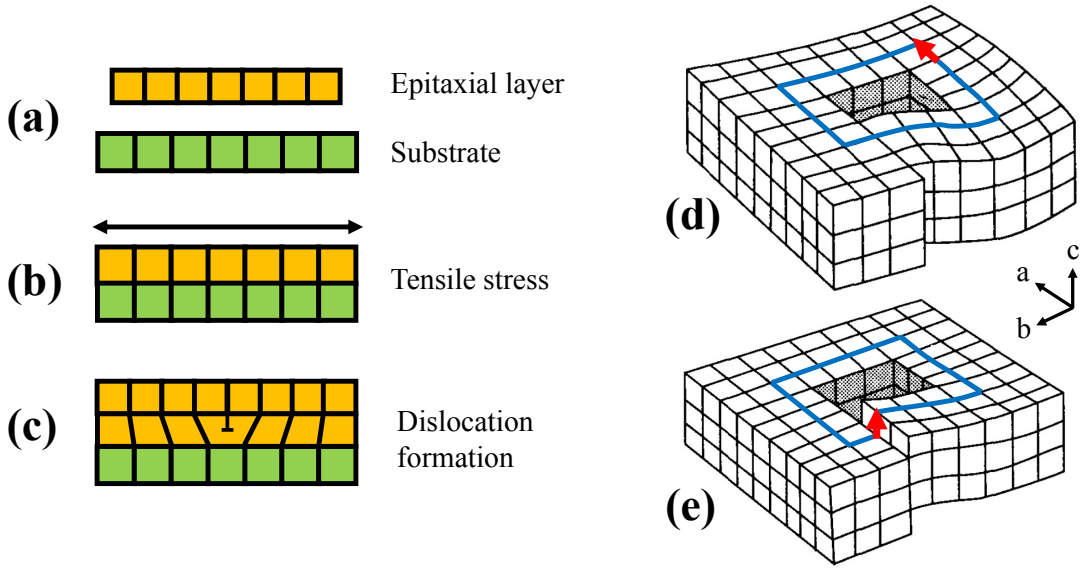

FIGURE 2.6. Illustration of a) the substrate and epitaxial layer of different lattice constant, b) the development of stress when the epitaxial layer is directly grown directly on top of the substrate, and c) the formation of a dislocation releasing the stress. The right side shows two different types of dislocation with d) an edge and e) a screw dislocation with the red Burgers vectors of $1\vec{a}$ and $1\vec{c}$, respectively. Adapted from [80].

vertical devices [85–87]. However, vertical leakage along threading dislocations can be beneficial to a certain degree in order to manage dynamic on-resistance in power devices following trapping under stressed conditions in off-state, particularly for a buffer with carbon doping [88, 89]. The ultimate consequence is a tradeoff between a low dislocation density to enable high breakdown characteristics paired with small high field leakage and sufficient leakage related to dislocations to ensure good dynamic device performance.

One key lever to manage the formation and density of dislocations in GaN HEMTs are the nucleation layer and the strain relief layers as shown in fig. 2.8. The primary purpose of the AlN nucleation layer is aiding the growth process by providing a nucleation site. The strain relief layers are meant to manage stress as well as the ultimate dislocation density caused by the lattice mismatch between the substrate and the overlaying GaN layer.

The research community spent big efforts on decreasing the density of dislocation in the attempt to reduce vertical leakage in GaN HEMTs, particularly for Si substrates [90–92]. There are several types of strain relief layer implementations. One way is a linearly or step-graded AlGaN composition layer which gradually decreases the Al content as the buffer is grown [41]. Another solution is a superlattice structure with either high Al-content AlGaN interlayers or AlN interlayers with a thickness of about 2 nm [93]. All techniques ultimately induce a strain gradient causing dislocations to bend away from the c-axis as the expitaxial growth progresses. This effect

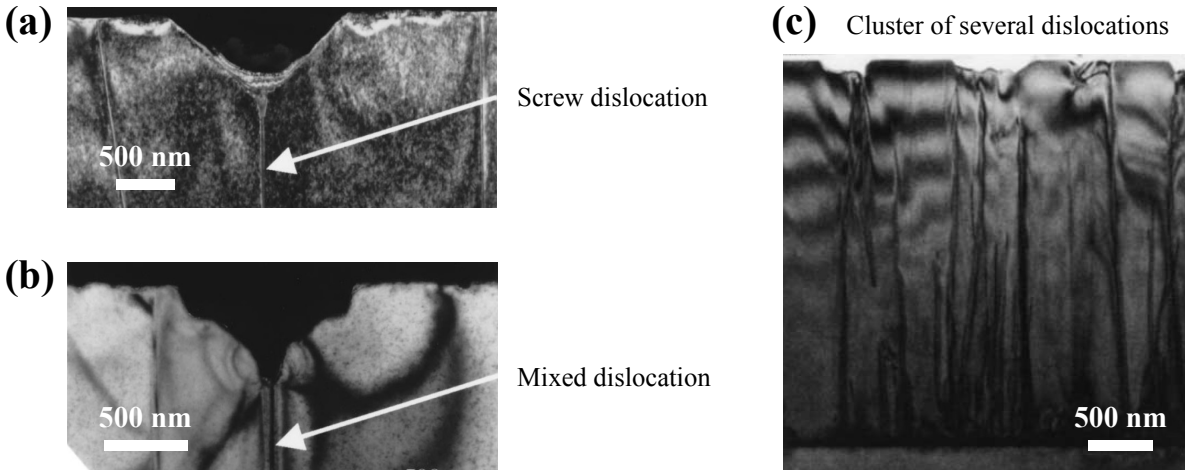

FIGURE 2.7. Cross-sectional TEM images of GaN dislocations from literature with a) an identified screw dislocation and b) an mixed (edge-screw) dislocation as well as c) a cluster of several dislocations. Images a & b adapted from [81] and image c adapted from [82].

increases the probability of dislocations to annihilate each other with opposite Burgers vectors or reach the outer edge of the wafer. Consequently, both effects lower the density of dislocations reaching the surface. Overall, the strain relief layers reduce the dislocation density by about a factor of ten down to the order of $10^9\,\mathrm{cm}^{-2}$ [81, 94–98]. Under high voltages in reverse bias condition, screw as well as mixed type (screw & edge) dislocations have shown to create leakage paths in Schottky diodes [99–101].

2.2.3 Buffer layer

Unintentionally doped GaN is typically slightly n-type. Defects like nitrogen vacancies and oxygen impurities act as donors giving nominally undoped GaN a resistivity on the order of $10^3\,\Omega\,\mathrm{cm}$ [102, 103]. If the region underneath the GaN channel is conductive, the device cannot properly pinch off which leads to high off-state leakage currents. Electrons are bypassing the gate by flowing through the buffer which is known as the punch-through effect and is further explained in section 2.5 [104]. The layer grown on top of the strain relief layers is therefore doped extrinsically with iron (Fe) or carbon (C) to pin the Fermi level deep in the GaN band gap as shown in fig. 2.9 in order to increase the buffer resistivity [37]. The dopants are added during the growth process. For instance, Fe can be introduced by including metalorganic precursors like $(\mathrm{Cp})_2\,\mathrm{Fe}$ or bis(cyclopentadienyl)iron into the metal organic chemical vapor deposition (MOCVD) process [105, 106]. The MOCVD growth involves organic carrier gases which always leads to the presence of C background doping. Increasing the C content requires amending the growth conditions such

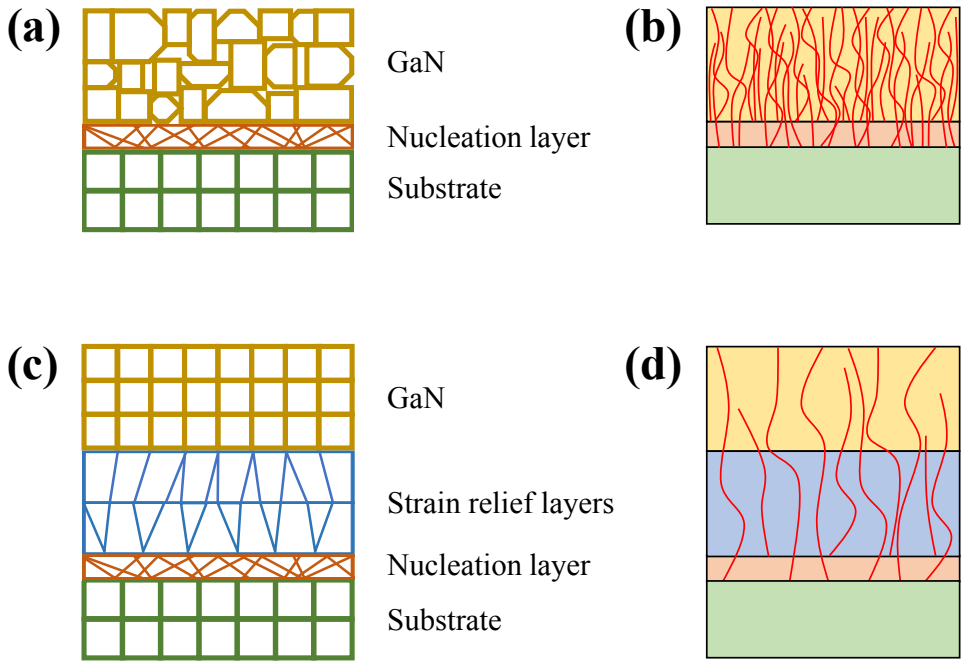

FIGURE 2.8. Illustration of the reduction in dislocation density using strain relief layers. a) The lattice mismatch between substrate and GaN creating b) a large number of crystal defects in form of dislocation. c) The utilization of strain relief layers countering the stress to help d) reduce the number of dislocations.

as temperature and pressure [107] or adding another C source like CBr_4 [38, 108]. The final concentration of dopants can be investigated by secondary ion mass spectroscopy (SIMS).

When Fe doping is used, the Fe atom occupies the N site giving rise to an acceptor state located $0.5-0.7\,\text{eV}$ below the conduction band as shown in fig. 2.10a [109–111]. The acceptor level pins the Fermi level in the upper half of the band gap making it weakly n-type and electrons the majority carrier [111]. Fe doping has the potential to increase the resistivity as high as $2\times10^9\,\Omega\,\text{cm}$ and is typically used for RF devices [112].

For power devices on the other hand, the requirements are different, especially the buffer needs to be more isolating to allow high breakdown voltages. For this case, C doping is the preferred choice allowing resistivities above $10^{13}\,\Omega\,\text{cm}$ [113]. The C dopant also acts as deep acceptor, however, the energy level is significantly lower in the GaN band gap, located at 0.9 eV above the valence band when C occupies the N site as shown in fig. 2.10b. This renders the buffer p-type and makes holes the majority carrier. When sitting on the Ga site, the C dopant introduces a shallow donor (fig. 2.10b) [114]. Beside the higher resistivity, C doping also increases the breakdown voltage through the reduced surface electric field (RESURF) effect, a phenomenon that is not available for Fe doping. In off-state at high drain bias, the p-type buffer ensures isolation of the C-doped region from the 2DEG through reverse-biasing of the p-n junction. The result is a negative ionized acceptor charge at the top of the carbon doped layer acting as back

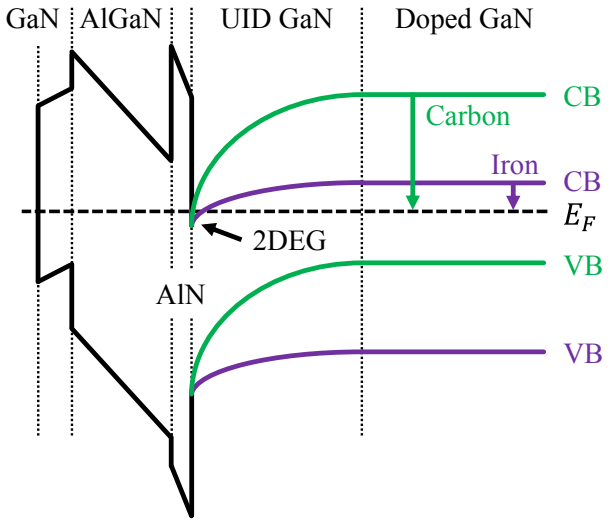

FIGURE 2.9. Schematic band diagram of an AlGaN/GaN HEMT showing the conduction band (CB) and valence band (VB) with C doping in green and Fe doping in purple. The diagram also includes an AlN interlayer between AlGaN barrier and the unintentionally doped (UID) GaN layer as well as a GaN cap on top of the AlGaN barrier.

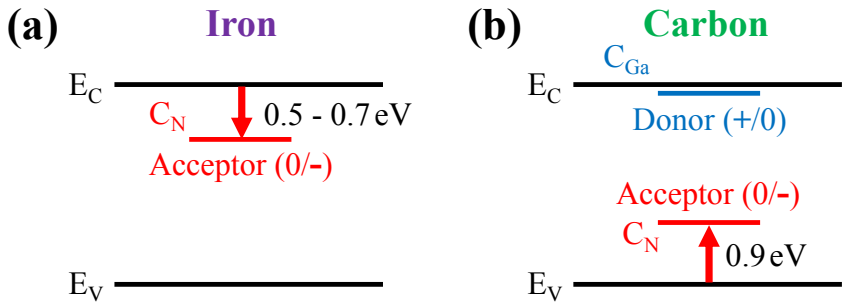

FIGURE 2.10. Band structure of a) iron-doped and b) carbon-doped GaN.

gate onto the 2DEG. This leads to an extension of the pinch-off region in the channel which reduces the electric field and facilitates higher lateral breakdown voltages. In the case of Fe doping, this effect is not possible due to the weak buffer n-type doping which eliminates the buffer isolation from the 2DEG. In this scenario, the buffer potential closely follows the 2DEG potential preventing the RESURF effect [88].

2.2.4 Barrier layer

The barrier is usually made of AlGaN which has a wider band gap than GaN. As described above in section 2.1.3, the AlGaN/GaN heterojunction causes the formation of the 2DEG which is vital to build transistors. The Al content is an important parameter as it influences the polarization effect and hence the electron concentration in the 2DEG. As the name implies, the purpose of the

AlGaN layer is also to represent a barrier for the gate to operate the device. Often, a $1-2\,\mathrm{nm}$ thick AlN layer is incorporated between the AlGaN barrier and the GaN channel as shown in fig. 2.9. The extra interlayer increases the 2DEG density by increased electron confinement as well as increases the electron mobility due to decreased alloy disorder scattering in the channel [115, 116].

2.2.5 Capping and passivation layer

The device stack is typically finished by depositing a thin GaN layer of $1-2\,\mathrm{nm}$ referred to as GaN cap followed by a device passivation layer. The layers are designed to reduce surface leakage and trapping. The GaN cap has a better surface quality than the AlGaN barrier leading to fewer deteriorating surface states and improved performance. However, the addition of another layer of GaN counters the polarization charge on top of the AlGaN barrier which reduces the 2DEG density [117]. The passivation layer usually consists of in-situ SiN_x and encapsulates the surface states. The passivation layer was also found to improve the surface quality yielding improved leakage properties [118]. Moreover, devices without passivation tend to have a pronounced virtual-gate effect. During high voltage application, electrons get trapped in surface states at the gate edge. This negative space charge acts on the 2DEG reducing its density and ultimately increasing the on-resistance. The passivation layer is meant to enclose and electrically deactivate these surface states [119].

The passivation layer is most commonly formed by three methods:

- Plasma-enhanced chemical vapor deposition (PECVD) at a temperature of about $300-400\,^{\circ}\mathrm{C}$, however, leading to the incorporation of a relatively high hydrogen content which facilitates diffusion of humidity [120]
- Epitaxial growth using low pressure chemical vapor deposition (LPCVD) at a temperature of $800\,^{\circ}\mathrm{C}$ yielding a passivation layer with a higher density and lower hydrogen contamination than PECVD resulting in a more thermally stable layer with lower electron trapping [121]
- Epitaxial growth using metal organic chemical vapor deposition (MOCVD) with the advantage of preventing contamination of the interface between the GaN cap and passivation [122]

2.3 High electron mobility transistor fabrication

After growing the layered epitaxial stack, the next processing step is building the actual functional device. Device fabrication involves the processes that create single devices on a wafer. A schematic of such a device is shown in fig. 2.11. This first step involves isolating individual devices from each other. In order to operate the device, two Ohmic contacts for source and drain as well as

a Schottky contact for the gate need to be created. To enhance device performance, field plates forming a metal–insulator–semiconductor (MIS) contact are deposited as well. The various steps and components are outlined below.

2.3.1 Device isolation

Isolating devices from each other means leaving areas with and without 2DEG. The two common techniques are mesa etching and ion implantation. The mesa etch process removes the upper layers of the stack beyond the channel which automatically removes the 2DEG. It is critical to create smooth sidewalls to avoid substantial sidewall leakage currents and not degrade the breakdown capabilities [123]. Ion implantation works via ion bombardment with different species (N^+, O^+, Fe^+, Ar^+, Zn^+, Mg^+) disordering the heterostructure in a line around the device [124]. Thereby, the 2DEG is locally disturbed and effectively cut which isolates the devices from each other. However, the ion bombardment impact can incur defects like lattice disorders, porosity, and erosion. Therefore, incident ion energies and doses need to be optimized to maintain good device reliability [125].

2.3.2 Contacts

The device needs to have electrical terminals to be operated. High performance source and drain contact have to be low-resistance ohmic contacts. On the contrary, the gate needs to be a rectifying non-ohmic contact. State-of-the-art devices typically also have field plates to optimize the electric field distribution across the device. The field plates are separated from the semiconductor by a dielectric and are thus metal–insulator–semiconductor (MIS) contacts. All these three types of contacts are shown in fig. 2.11 and described in further detail below.

Ohmic contact: The ohmic contact resistance has to be small to ensure a low on-resistance of the device. As visible in fig. 2.11b, there is no barrier between the metal work function and the semiconductor conduction band. The lower the contact resistance, the lower is the total on-resistance and the higher is the maximum source–drain current. For RF devices, a lower source–drain resistance leads to an increased transconductance allowing increased cut-off and maximum frequencies. Contacting the channel from the surface means penetrating the AlGaN barrier down to the 2DEG. For AlGaN/GaN devices, this process usually involves depositing a stack for the four metals titanium (Ti), aluminium (Al), nickel (Ni), and gold (Au) which are subsequently rapidly annealed at a high temperature of around 800 °C. This causes the metals to diffuse into the AlGaN and form a contact to the 2DEG [126]. Each metallization constituent has its own important role. Ti will react with N from the AlGaN and GaN forming the intermetallic alloy TiN which has a low work function aiding the contact to the 2DEG. The presence of Al will cause the formation of Al_3Ti which plays a similar role as TiN [127]. Both the formation of TiN and AlN also create N vacancies. Those defects act as n-type dopant enabling tunnelling

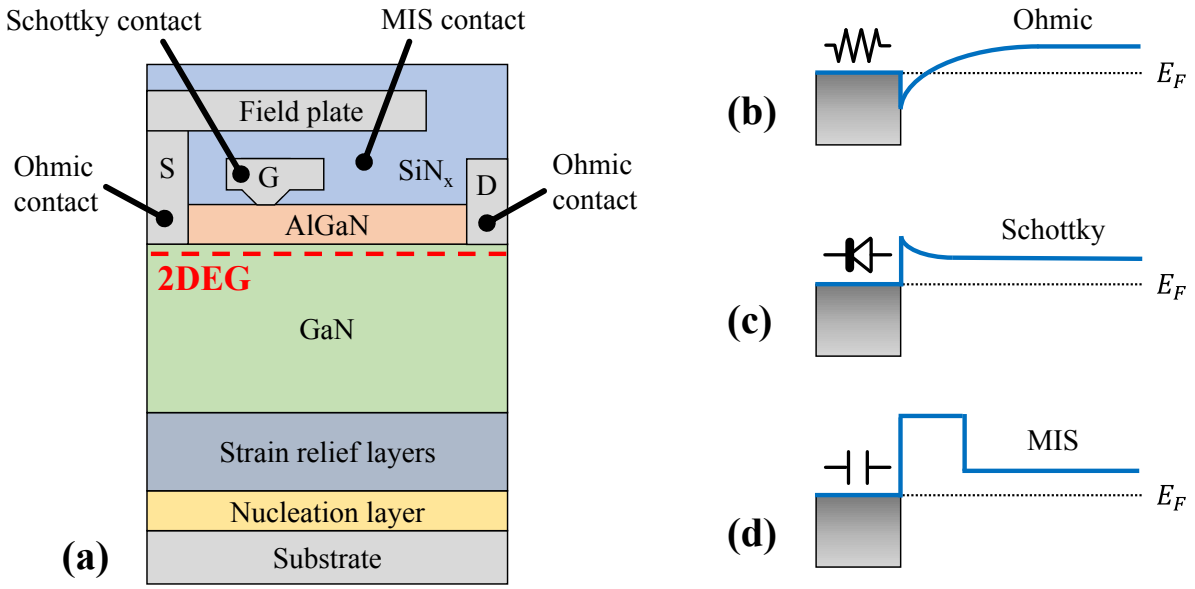

FIGURE 2.11. Illustration of a) the typical AlGaN/GaN HEMT device structure with source (S), gate (G), and drain (D) as well as the band diagram for three possible semiconductor contacts with b) an Ohmic contact, c) a Schottky contact, and d) a metal–insulator–semiconductor (MIS) contact.

across the barrier which aids the contact to the 2DEG [128]. Another purpose of Al is decreasing the aggressiveness of the Ti-GaN reaction to avoid voids underneath the TiN layer [129]. Ni is incorporated into the heterostructure to prevent the interflow between the Al and Au layer [130]. The formation of the Al-Au phase can lead to a rough surface morphology [131]. The metallization is topped by Au to prevent Ti and Al from oxidizing during the high temperature annealing step [132].

Schottky contact: The gate of the AlGaN/GaN HEMT controls the device and represents a Schottky contact. The key feature of the Schottky contacts is a non-zero barrier between the metal and the conduction band of the semiconductor as shown in fig. 2.11c. The Schottky contact largely behaves like a diode. Applying a negative bias to the gate causes the junction to be reverse-biased. Electrons need to be thermally excited in order to overcome the barrier and travel across the junction. If the barrier is thin enough, electrons can tunnel through the barrier. The resulting current is small and proportional to $\exp(-q\,\phi/k_\mathrm{B}T)$ with barrier height ϕ. However, if the applied bias is positive, the diode becomes forward-biased and the electrons can easily travel from the semiconductor conduction band to the metal. In forward bias direction and for voltages higher than $3k_\mathrm{B}T/q$ [133], the current is given by the equation

$$I = I_s \exp\left(\frac{q\,(V - I R_s)}{n k_\mathrm{B} T}\right) \tag{2.7}$$

with the ideality factor n, elementary charge q, serial resistance R_s, and the saturation current

$$I_s = A\,R\,T^2 \exp\left(\frac{-q\,\phi}{k_\mathrm{B}T}\right) \tag{2.8}$$

with device area A and Richardson constant R. The barrier height ϕ can be determined by

$$\phi = \frac{k_\mathrm{B}T}{q} \ln\left(\frac{A\,R\,T^2}{I_s}\right) \tag{2.9}$$

as extrapolation from the y-axis intercept of the IV characteristics [133]. For AlGaN/GaN HEMTs, it is typical to use a Ni/Au alloy as Schottky metal which has a barrier height of approximately 1 eV with respect to AlGaN [134–136]. Adding a thin $1-2$ nm AlN layer at the AlGaN/GaN interface increases the barrier height to about 0.65 eV [137]. A forward-biased metal/AlGaN/GaN system also has a barrier to overcome at the AlGaN/GaN junction. Therefore, this structure behaves similarly to a back-to-back diode. A large barrier is crucial to ensure small leakage currents and high breakdown voltages [138].

Metal–insulator–semiconductor contact: MIS contacts sit above the channel and are used for both building the gate (MISHEMT) and forming field plates. Given the high barrier height, a MIS contact dominantly behaves like a capacitor as seen in fig. 2.11d. The insulator functions as dielectric material and the charge storage is mediated via conduction through the dielectric. Field plates assist in lowering the off-state electric field in the channel by redistribution of the potential drop over ideally the entire gap from gate to drain. Without field plates, the 2DEG along the gap is biased at the drain voltage and therefore, the majority of the electric field peaks at the gate edge. Field plates are designed to deplete the 2DEG between gate and drain to increase the depletion distance and consequently reduce the peak electric field within it. Field plates are effectively acting as additional gated areas with increasing pinch-off voltage closer to the drain [139]. There are different variations of field plate configurations—connected to the source as shown in fig. 2.11a but also connected to the gate and drain—in order to shape the electric field at the contacts [140].

2.4 High electron mobility transistor operation

AlGaN/GaN HEMTs are designed for different operation purposes. One key factor is whether the HEMT is configured as normally-on and normally-off device. Depending on the device design, there are important aspects of the DC and switching performance which are outlined below.

2.4.1 Normally-on and normally-off operation

The GaN HEMT covered in the sections above describes a so-called normally-on device, also known as depletion mode (D-mode) device. A certain bias must be applied to the gate in order to

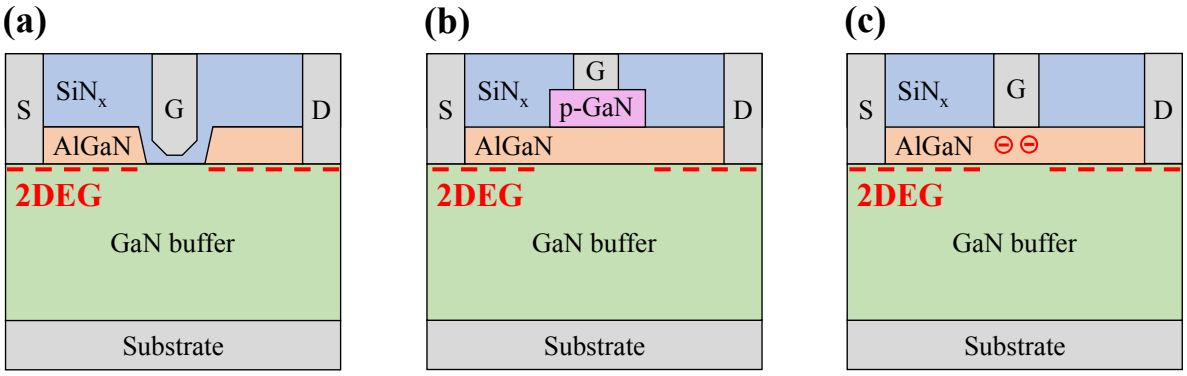

FIGURE 2.12. Schematic of an E-mode GaN HEMT using a) the gate recess method, b) by introducing an additional p-GaN layer at the gate, and c) via ion implantation into the barrier.

turn off the device. This is a severe complication for power applications. The lack of an inbuilt default mechanism to turn off the device can lead to serious damage of electric systems if the circuit malfunctions. To enable a fail-safe state, the device configuration must be converted to a normally-off device. This can be achieved by directly changing the HEMT design, otherwise known as enhancement mode (E-mode) device. Another method is combining the D-mode GaN HEMT with a normally-off low voltage Si MOSFET yielding a normally-off dual device cascode circuit.

2.4.1.1 E-mode GaN HEMT

There are several methods to amend the classic D-mode GaN HEMT design to feature E-mode switching behavior. They all have in common that they locally remove the 2DEG underneath the gate. The three most promising techniques are the gate recess process (fig. 2.12a), introduction of a p-GaN gate (fig. 2.12b), and ion implantation (fig. 2.12c).

Gate recess generally means thinning the AlGAN barrier until the threshold voltage turns positive. This occurs when the barrier is etched down to a few nanometers or removed completely as shown in fig. 2.12a. A thin layer of an insulator is necessary to block excessive gate leakage currents which turns the device into a MISHEMT. However, the dielectic material is close to the channel which makes it prone to electron trapping. This consequently increases the on-resistance [141].

Another E-mode configuration is the addition of a p-GaN layer between the AlGaN barrier and the gate metal as pictured in fig. 2.12b. The p-GaN layer will pull up the conduction band which in return depletes the 2DEG. P-type GaN can be achieved by magnesium (Mg) doping which creates a deep acceptor level about 200 meV above the valence band. The Mg doping level must be controlled accurately. An Mg concentration too high has shown to induce hole tunnelling at

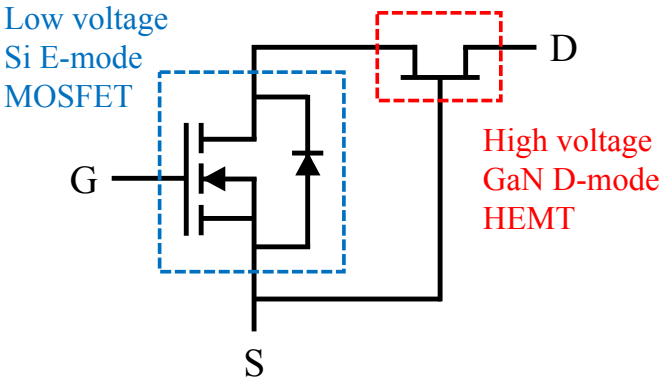

FIGURE 2.13. Electric circuit of a cascode configuration with a D-mode GaN HEMT and an E-mode Si MOSFET

the metal/p-GaN interface ultimately decreasing the threshold voltage again [142]. Another issue with Mg doping is that it easily reacts with H^+ leading to the formation of a Mg-H complex during the MOCVD process creating a passivation layer [143]. There is also a difficulty in removing the grown p-GaN layer locally where it is not needed. First the p-GaN layer is grown uniformly over the entire wafer and subsequently etched away everywhere but the gate access area. Damaging the AlGaN layer during that step can degrade the 2DEG carrier density and mobility [31].

Ion implantation incorporates F^- ions into the AlGaN barrier below the gate using a flourine plasma as shown in fig. 2.12c. The strong flourine electronegativity helps keeping the ions charged. The negative space charge will deplete the 2DEG locally underneath the gate which shifts the threshold voltage to positive values [144–146]. However, the fluorine treatment potentially damages the underlying GaN layers which reduces the 2DEG mobility. Thus, E-mode devices made by ion implantation typically have a lower mobility than the D-mode counterpart. The material destruction can partly be recovered by annealing the device at high temperatures [147].

2.4.1.2 Cascode

The cascode circuit combines the high voltage capability of a D-mode GaN HEMT with the normally-off properties of an E-mode Si MOSFET. Therefore, this configuration overall resembles a high voltage normally-off device. The circuit is pictured in fig. 2.13. At no voltage applied to terminal G, the E-mode Si MOSEFET is turned off with an increase in Si MOSFET drain–source voltage reverse biasing the D-mode GaN HEMT gate. The potential difference between gate and channel of the D-mode GaN HEMT pinches off the 2DEG. In this state, applying a positive voltage to the terminal D makes the voltage drop across the D-mode GaN HEMT. In on-state, when applying a positive voltage to G, the Si MOSFET is turned on. That electrically shorts the source and gate of the GaN HEMT. The cascode configuration is turned on and conducts [148, 149]. However, the higher voltage capabilities and higher switching efficiencies of the cascode configuration compared to only using a Si MOSEFT alone come at a cost. Adding another

device in series increases the overall on-resistance. Moreover, the dual device circuit entails parasitic inductances and capacitances which lower the high frequency abilities [150].

2.4.2 DC performance

The device current flows from source to drain passing underneath the gate. The channel current transporting electrons at an effective velocity v_{eff} is directly proportional to the device width equal to the gate width W_G. The drain current I_D can therefore be expressed as

$$I_D = q\, n\, v_{eff}\, W_G \tag{2.10}$$

with the elementary charge q and the 2DEG electron density n. The gate voltage V_{SG} defines the modulation of the current flowing between source and drain. Consequently, the drain current can be written as

$$I_D = q\, n_\sigma(x)\, \mu W_G \frac{\partial V_{SG}(x)}{\partial x} \tag{2.11}$$

with the two-dimensional sheet carrier density n_σ, the lateral gate voltage $V_{SG}(x)$ and the 2DEG electron mobility μ. Integrating this equation from the source edge ($x = 0$) to the drain edge ($x = L_G$) of the gate gives

$$I_D = \frac{\mu W_G\, \epsilon}{(d + \Delta d) L_G} \left[(V_{SG} - V_{th})\; V_{SD} - \frac{V_{SD}^2}{2} \right] \tag{2.12}$$

with the AlGAN Schottky barrier thickness d and permittivity ϵ as well as the source–drain voltage V_{SD}, the effective 2DEG distance from the heterojunction Δd and the threshold voltage V_{th}. The HEMT intrinsic pinch-off gain is analyzed by the transconductance

$$g_m = \frac{\partial I_D}{\partial V_{SG}} \tag{2.13}$$

which represents the gate effectiveness when modulating V_{SG} [133]. Fig. 2.14 shows an example of the I_D-V_{SG} switching characteristics and the I_D-V_{SD} output performance for a GaN HEMT with a positive V_{th}.

2.4.3 Switching performance

GaN HEMTs have two key applications: Power switches due to the high breakdown field and RF amplifiers owing to the high power density capabilities. Both applications involve different processes and have therefore different priorities.

For power switching, the device is required to block high voltages on the order of hundreds of volts when kept in off-state. The transition to on-state is preferably performed very quickly and results in a low on-resistance R_{ON}. As shown in fig. 2.15a, there are two switching paths. During hard switching, the device directly changes from low to high electric field whereas during soft switching, the trace passes through the origin point at $V_{SD} = 0\,\mathrm{V}$. Soft switching stresses the device a lot less with reduced trapping and degradation which extends the device lifetime [151].

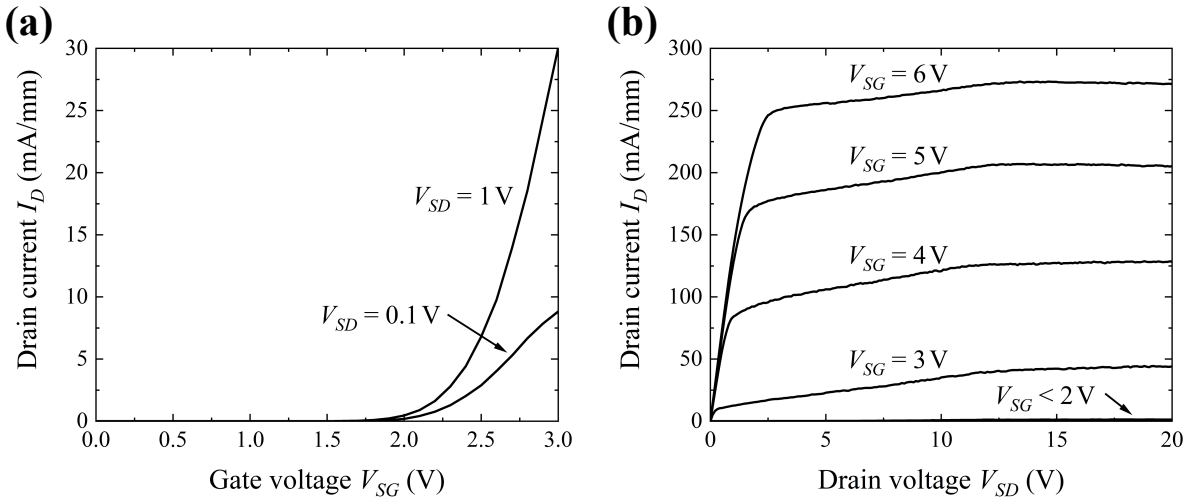

FIGURE 2.14. DC characteristics with a) the I_D-V_{SG} switching curve for two different V_{SD} and b) the I_D-V_{SD} output plot for several different V_{SG}.

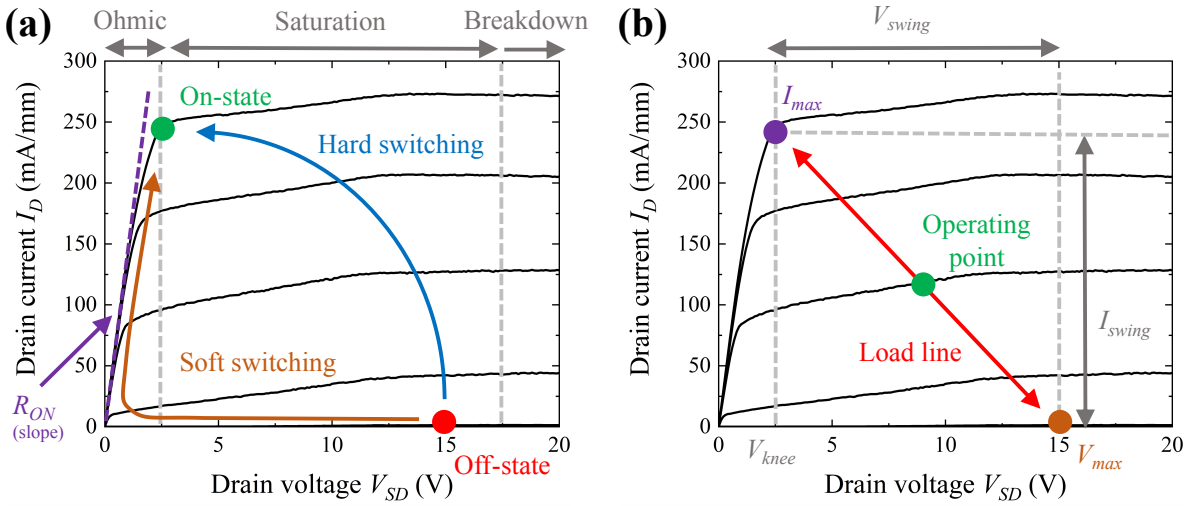

FIGURE 2.15. Illustration of a) the power switching process with hard and soft switching as well as b) RF switching with the load line going from V_{max} to I_{max}.

For RF switching, the 'knee' region is very important for stable device operation. The knee sits at the kink between the linear region and the saturation region (I_{max} at V_{knee} in fig.2.15b). As shown in fig. 2.15b, the device is operated around an operating point at a low bias along a dynamic load line which depends on the class of operation. In RF switching, the device typically remains at off-state drain biases below about 100 V. For this reason, RF devices do not require high breakdown abilities. However, a stable knee is very crucial, which in fact is jeopardized if the device is operated at high off-state fields leading to trapping and causing a knee dispersion. The

goal for RF amplifiers is to maximize V_{swing} and I_{swing} (fig. 2.15b). RF devices are thus optimized to have a low V_{knee} and high I_{max} which is, for instance, achieved by minimizing the device on-resistance [152].

2.4.4 Applications

There are several applications where GaN HEMTs can be used. A better understanding of types of circuits where GaN technology can be beneficial is important in order to optimize GaN device specifications. Two applications are introduced in the following: DC-DC power converters and DC-AC power inverters.

GaN power devices deployed for DC-DC power converters can work in two operational modes. This can either mean increasing the voltage while decreasing the current, also referred to as boost converter. For example, these so-called boost converters are needed in electric cars to achieve the high voltages driving the electric motor. They are also used in heaters and welders as well as distributed power architecture systems. On the contrary, so-called buck converters decrease the voltage while increasing the current upon conversion. They can play a key role in future data centers when stepping down the voltage from grid level on the order of hundreds of thousands of volts to data processor level on the order of volts. Other applications for buck converters are charging systems used in consumer electronics.

The second example for using GaN power devices is DC-AC inverters. Several power sources such as photovoltaic energy as well as power storage such as batteries output DC power. However, many applications such as electric motors require AC power. The electric grid operates on AC power as well. The conversion between DC power and AC power can be achieved by a DC-AC inverter.

DC-DC boost converter: The circuit of a basic DC-DC boost converter is shown in fig. 2.16a. A simple DC-DC converter will operate by switching on and off one power transistor with a duty cycle D. If the transistor is turned on, current flow through the inductor builds up a magnetic field which stores energy. If the transistor is turned off, the inductor polarity inverts which continues to drive the current. This adds a voltage in series to the input voltage V_{in} boosting the output voltage V_{out} applied to the load. The capacitor gets charged at this total voltage. When the transistor is turned on again, the capacitor maintains the load potential and the diode ensures the capacitor only discharges across the load. The conversion factor can be derived as

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \quad . \tag{2.14}$$

DC-DC buck converter: The circuit of a basic DC-DC buck converter is pictured in fig. 2.16b. The transistor, the inductor, and the diode are switched around compared to the boost converter but the same charging and discharging principles apply. When the transistor is turned on, the diode is blocking and current flows through the inductor and the load. Building up the magnetic

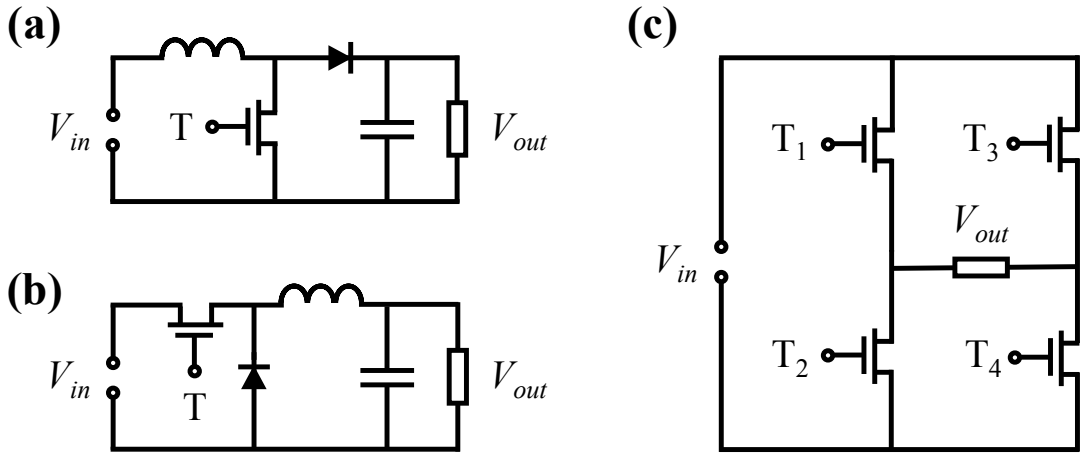

FIGURE 2.16. Simple circuit of a) the DC-DC boost converter making use of one transistor T, b) the DC-DC buck converter, and c) the DC-AC inverter.

field stores energy and creates a voltage opposing the input voltage. That reduces the output voltage V_{out} across the load compared to the input voltage V_{in}. At the same time the capacitor is charged. When the transistor is turned off, the diode is forward-biased and the collapsing magnetic field in the inductor continues to drive the current. The capacitor is discharging across the load adding to the current. The conversion factor can be derived as

$$V_{out} = V_{in}\, D \quad . \tag{2.15}$$

If $R\,C \gg D\,P$ with the cycle period P, the output voltage is nearly constant. However in reality, turning the transistor on and off for both boost and buck converter causes the output voltage to fluctuate. For practical application, those oscillations have to be filtered out compromising the conversion efficiency. The higher the switching frequency, the lower are the oscillations and the associated losses, and the smaller are the necessary inductance and capacitance to deliver the same output. Especially for the boost converter, when the transistor is turned off, the transistor needs to be able to block the boosted output voltage. When the transistor is turned on, the transistor is required to handle high current densities through the low resistance circuit. The switching process between both states incurs power losses when both high voltages and high currents are present. Therefore, GaN technology with its high frequency, high voltage-blocking and low resistance capabilities has clear advantages over Si MOSFETs [153].

DC-AC inverter: The circuit of a basic DC-AC power inverter is shown in fig. 2.16c. In this example, the circuit turns a DC input into an AC oscillation using four transistors. Turning on the transistors T_1 and T_4 causes an output voltage of V_{in}. Only turning on transistors T_1 and T_3 or T_2 and T_4 blocks the input voltage leading to a zero output voltage. Lastly, switching on only transistors T_2 and T_3 yields an output voltage of $-V_{in}$. Alternating between those three states approximates a sine wave output across the load. Having only three load voltage states causes

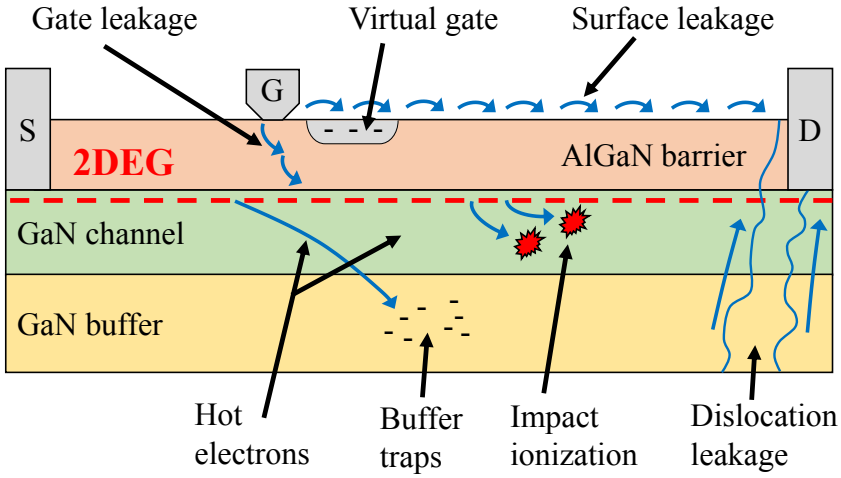

FIGURE 2.17. Schematic of all kinds of reliability and degradation mechanisms of AlGaN/GaN HEMTs.

higher square wave harmonics which need to be filtered out. Using a three-phase DC-AC inverter which can switch between six different load voltages can give a better approximation of the desired sine waveform. GaN HEMTs can allow DC-AC inverters to operate at higher frequencies and higher voltages while having low conduction losses [153].

2.5 High electron mobility transistor reliability

GaN HEMTs are promising devices for a wide range of applications. The ideal device would have an infinite off-state resistance and zero on-state resistance without any switching losses. Moreover, the transistor would be able to withstand high off-state electric fields without degradation. However, in reality that is not the case and there are many reliability problems that need to be understood and tackled. A variety of processes is shown in fig. 2.17 and explained in the following.

2.5.1 Leakage and breakdown phenomena

Leakage mechanisms occur in the off-state condition. They limit the voltage blocking capabilities and are a key driver for device breakdown. During off-state, a high voltage is applied to the drain generating a high field, laterally between gate and drain as well as vertically across the buffer. There are several lateral conduction mechanisms such as transport along the surface, gate leakage, as well as buffer punch-through. Vertical leakage can occur via conduction along dislocations.

Lateral surface leakage and gate leakage: Leakage through surface hopping along the passivation or across the AlGaN barrier happens at high electric fields. The conduction processes

through the insulator can be described by Folwer–Nordheim and Poole–Frenkel transport. The Folwer–Nordheim conduction mechanism represents a tunneling process through a field-reduced barrier. The Folwer–Nordheim current can be approximated by

$$J_{FN} = C_{FN} E_b^2 \exp\left(-\frac{8\pi\sqrt{2 m_e^* (q\,\Phi_b)^3}}{3\,q\,\hbar E_b}\right) \tag{2.16}$$

with constant C_{FN}, electric barrier field E_b, and barrier height Φ_b. Evidently, this mechanism has no temperature dependence. On the contrary, the Poole–Frenkel mechanism is a thermally excited electron hopping process via trap states within the band gap. The Poole–Frenkel current can be approximated by

$$J_{PF} = C_{PF} E_b \exp\left(-\frac{q\left(\Phi_t - \sqrt{\frac{q E_b}{\pi \epsilon}}\right)}{k_\mathrm{B} T}\right) \tag{2.17}$$

with constant C_{PF}, trap energy Φ_t with respect to the conduction band, and the semiconductor permittivity ϵ. This mechanism is temperature dependent. Consequently, this process is frozen at low temperatures and the overall conduction is dominated by the Folwer–Nordheim process. On the other hand, at higher temperatures the conduction is dominated by Poole–Frenkel current [154]. Modifications of the barrier and passivation layers can help improve leakage characteristics which can be investigated using step–stress measurements alongside electroluminescence measurements. Typical methods to tune the device reliability and control surface and gate leakage are a reduction of the Al content in the barrier to reduce strain and material cracking, optimized surface preparation and cleaning techniques to control surface pitting and oxidation, optimized gate metallization and the deposition parameters to align thermal mismatch and mitigate diffusion effects, improved thermal design aspects of the device to increase lifetime, among others [155].

Lateral buffer punch-through: At high off-state voltages, electrons can flow from the source through the buffer to the drain bypassing the depletion region underneath the gate. This effect is called punch-through. It can be suppressed by increasing the buffer resistivity using buffer dopants such as carbon. This also supports the 2DEG confinement which generally helps minimize lateral leakage through the buffer [104]. An alternative solution is the incorporation of wide band gap materials into the buffer layers as substitution of the traditional GaN buffer. A buffer with a linearly-graded AlGaN layer additionally helps with an increased electron confinement in the 2DEG. However, this solution compromises the device performance with a decrease in saturation current I_D. It also leads to an increase in threshold voltage V_{th} [156].

Vertical leakage: In off-state, the electric field spans vertically across the buffer as well. A drain voltage V_{SD} of hundreds of volts can cause an electric field high enough to trigger field-enhanced Poole–Frenkel current [157]. Electrons stored in ionized carbon acceptor traps are

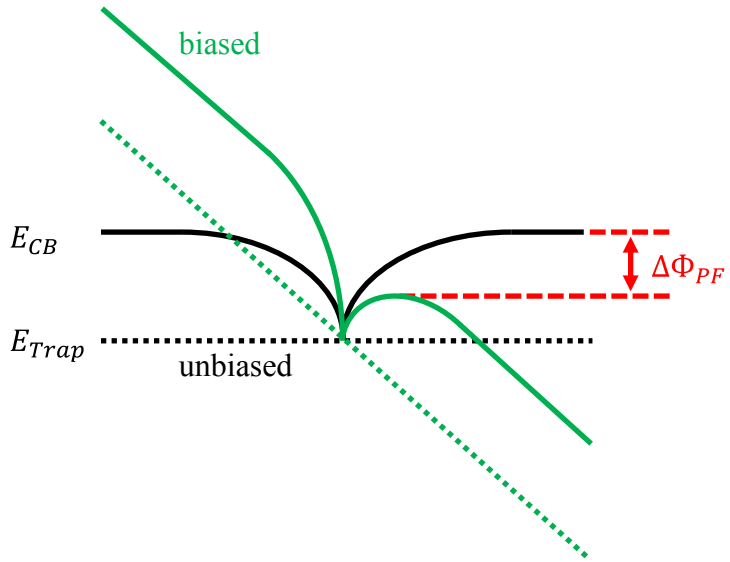

FIGURE 2.18. Band diagram with conduction band E_{CB} and trap state E_{Trap} leading to Poole–Frenkel emission at high field due to barrier lowering of $\Delta\Phi_{PF}$.

allowed to leak out of the traps by the barrier reduction as shown in fig. 2.18. Those additional electrons facilitate the creation of percolation paths between substrate and drain increasing the vertical leakage current overall and creating locations for breakdown [158]. Buffer defects such as threading dislocations through the insulating stack can also create vertical leakage paths that contribute to vertical breakdown. Especially dislocations with a screw component have shown to be electrically active [159]. The electrical behavior is modelled assuming that dislocations generate states within the band gap which allow variable-range hopping and trap-assisted tunneling [160]. The substrate resistivity plays an important role in vertical leakage and associated breakdown as well [161].

2.5.2 Trapping phenomena

Traps are related to imperfections in the crystal structure. They give rise to energy levels inside the semiconductor band gap. The type of trap and its energy level define the influence on the overall material behavior. So-called shallow traps have a state energy level that resides close to the respective band edge. With an energy difference of only a few millielectronvolts, charge carriers can easily be excited by the thermal energy of 26 meV at room temperature (300 K). On the other hand, deep defect states with energy levels further from the respective band cannot maintain a dynamic equilibrium with the conduction band and valence band during switching. Therefore, those states 'trap' charge carriers. There are two types of traps. Acceptors are neutral when empty, and negatively charged when ionized by occupation of an electron. Donors are positively charged when empty, and alternatively, neutral when ionized (fig. 2.10) [133].

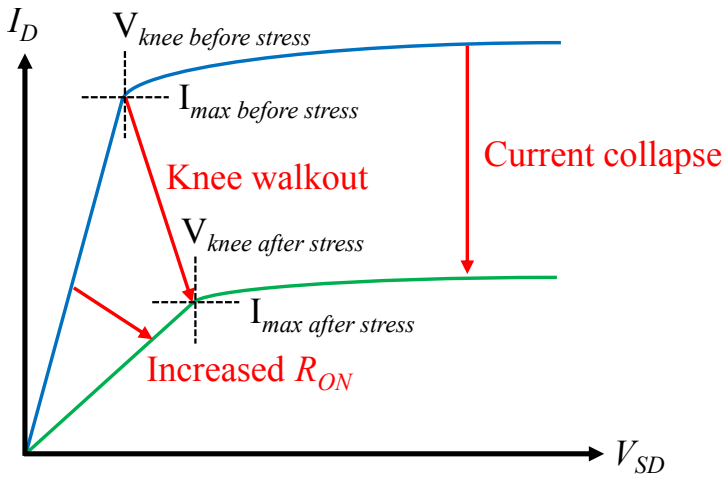

FIGURE 2.19. Schematic of the impact of off-state stress on the I_D-V_{SD} characteristic triggering an increase in on-resistance R_{ON}, a knee walkout, and current collapse.

2.5.2.1 Surface trapping

Surface traps are located at the top of the AlGaN barrier. At high electric fields, electrons can leak from the gate and travel across the surface. When the electric field is removed, the majority of trapped electrons relax back to their equilibrium. Trapped electrons at the gate edge can cause a so-called virtual gate. This negative space charge locally reduces the 2DEG carrier concentration and entails several other effects. One of them is gate lag which causes a delayed response of the channel current upon changing the gate potential. During off-state stress electrons get trapped. After switching to on-state, those defects detrap to their initial state. This process is thermally driven and therefore not instantaneous [162]. This effect is also related to current collapse and knee walkout referring to the DC-to-RF dispersion during switching. Trapped charges create a space charge repelling the 2DEG which obstructs the channel conduction. This can cause a dynamic change in device threshold voltage (knee walkout) and a decrease in saturation current (current collapse) as seen in fig. 2.19. Those effects reduce the output power compromising both RF and power device performance [163]. Proper surface passivation can mitigate the effect by decreasing the density of surface states [122, 164]. Adding field plates helps in reducing spots of high electric fields, primarily at the gate edge. A combination of source and gate field plates overhanging the channel redistribute the electric field along the gate–drain distance which prevents peaking of the electric field at the gate corner [165–168]. Reducing the electric field by means of field plates also helps diminish impact ionization in semi-on-state. This prevents accelerated device failure and increases the device lifetime. The electric field can also be reduced by increasing the gate–drain distance. Therefore, the gate is typically placed close to the source to provide a much longer gate–drain stretch over which the off-state potential is dropped [169].

2.5.2.2 Buffer trapping

Buffer trapping leading to current collapse or dynamic on-resistance R_{ON} poses a challenge for GaN power devices. Buffer traps are located below the device channel. At high off-state electric fields between gate and drain, electrons can get accelerated to energies greater than the band gap energy. This allows those hot electrons to travel to the buffer and get trapped in deep level defects with long time constants [170]. The trapped electrons in the buffer act as back-gate to the channel similar to the virtual gate at the surface. This causes a partial depletion of the 2DEG which reduces the channel conductivity similar to the surface-related current collapse [171]. Addressing undesired buffer trapping is difficult. Deep level defects are inevitably incorporated during the buffer growth process due to unintentional dopants. On top, the buffer is often intentionally doped to increase the resistivity. Thus, instead of reducing the trap density, the influence of traps is managed by allowing the electrons to neutralize much quicker. This can be achieved by decreasing the resistivity of the upper buffer layers. The resistivity gradient supports the injection of positive charge carriers into the buffer which facilitates buffer discharging [89]. Regaining a high electron concentration is important in the 2DEG in order to reduce conduction losses which, in return, is crucial for high performance devices.

Uren *et al.* developed a detailed model called 'leaky dielectric' to explain and manage dynamic R_{ON} based on the deep level dopant carbon (C) combined with the role of dislocation-induced leakage [89]. As shown above in section 2.2.3, C doping renders the GaN buffer p-type increasing the resistivity and making holes the majority carrier. This creates a reverse-biased p-n junction between 2DEG at the top of the unintentionally doped (UID) GaN layer and the isolated buffer which makes the buffer float electrically. Consequently, holes can flow laterally within the C-doped layer, albeit due to a low density of free holes leading to a large resistivity, the time scales are in the hundreds of seconds. As mentioned above, the C-doped layer acts as back-gate modifying the 2DEG conductivity. Changes in potential of the C-doped layer heavily impact dynamic R_{ON}. Vertical leakage along defects such as screw dislocations helps alleviate the problem of a floating buffer by allowing the C-doped layer to follow the potential of the 2DEG which prevents back-gating. With an applied high drain voltage in off-state, leakage within the epitaxial layers occurs leading to positive and negative charge accumulations based on the electrostatics as shown in fig. 2.20. Given the vertical field component, a negative charge gathers within the substrate underneath the drain. To match this charge, a positively charged region has to form further up in the buffer. Its location depends on the relative resistivities of the buffer layers but it would normally be located between the top of the strain relief layers and the drain contact itself. Assuming vertical leakage paths through the UID GaN layer, this region with positive charges will appear at the bottom interface of the C-doped layer. Considering the lateral field in the channel, a positive charge appears on the drain side of the capacitive region between source/gate and drain countered by a negative charge on the gate side. The origin of this positive charge will mostly be the exposing of the positive polarization charge at the bottom of the AlGaN/GaN

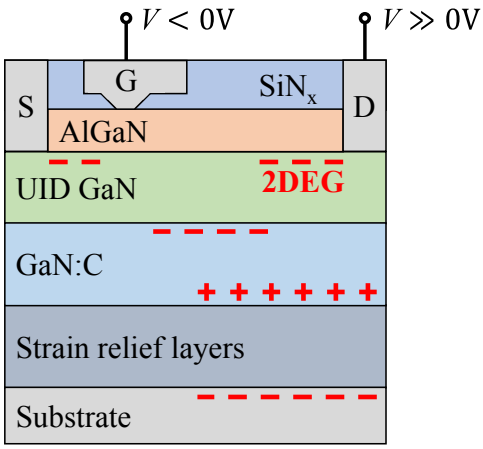

FIGURE 2.20. Schematic of charge accumulation under off-state across the buffer related to dynamic R_{ON} with applied drain bias.

interface by depleting the 2DEG. The negative countercharge is a combination between field plates and ionized acceptors in the GaN buffer. The latter is the one responsible for dynamic R_{ON}. All the mentioned charge regions are present during off-state but the proportion of trap-related charges in the GaN layer rather than at electrodes or the 2DEG defines the susceptibility of the device towards dynamic R_{ON}. The leakage and corresponding charge redistribution within the buffer can be analyzed using substrate ramp measurements as explained in section 3.4 [88, 89].

CHAPTER 3

CHARACTERIZATION TECHNIQUES

Investigating the physical and technical behavior of devices requires a deeper understanding of experimental techniques. This includes the electrical and material side. This chapter first introduces the basics of electrical instrumentation followed by basic DC measurements. It also covers the dynamic behavior by means of transient measurements as well as several scanning probe microscopy techniques.

3.1 Electrical measurement environment

The electrical data acquisition in this thesis was performed on unpackaged devices and directly measured on the devices on the wafer. The process involves different pieces of equipment which will be explained in the following.

3.1.1 Probe station

The probe station consists of several parts as seen in fig. 3.1. The wafer is placed onto a chuck made out of a conductive material such as aluminium, steel, or tungsten. During the measurement, the chuck is grounded, however, if required a substrate bias can be applied using a triaxial connector. There are also thermal chucks with heating and water cooling using a proportional–integral–derivative (PID) controller. Those allow the sample to be examined at a range of elevated temperatures up to 200 °C. The optical microscope sits above the chuck. It enables the operator to look at the sample at a magnification with a choice of different objectives. The device can be probed using manual micropositioners with independent x, y, and z movement. Depending on the test structure and measurement, there are two main probe species. A single connection can be established using probe needles. Standardized structure layouts with specific contact spacing

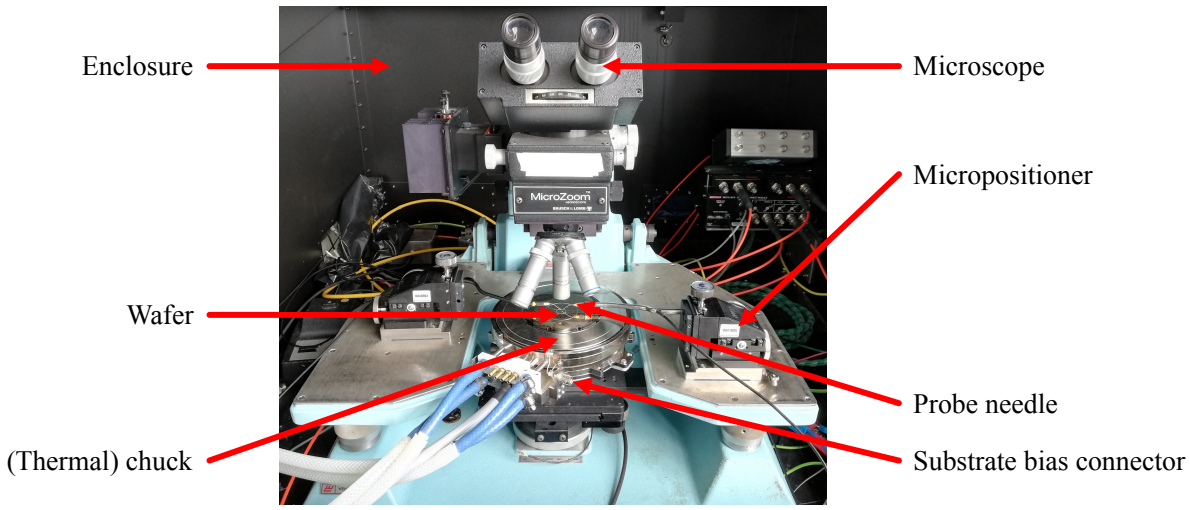

FIGURE 3.1. Probe station setup with placed sample wafer.

allow the usage of multiple-needle probes such as so-called ground–signal–ground (GSG) probes. The entire setup is enclosed in an interlocked and grounded enclosure for safety reasons. Another purpose of the enclosure is creating a dark measurement environment as every light exposure can manipulate the carrier density due to the generation of photoexcited charge carriers. The metallic enclose coating also functions as Faraday cage helping to prevent electromagnetic interference and noise.

3.1.2 Measuring instruments

Most measurements are performed using source measure units (SMU). Those measuring instruments are capable of sourcing a voltage or current while measuring the respective other quantity. Each SMU typically has a force and sense output which facilitates four-wire measurements. The SMU also has a high input resistance on the order of 100 TΩ to minimize circuit loading when measuring high impedance sources. The current sensitivity is usually as low as 10 pA.

In this work, the vast majority of electrical measurements have been carried out using three different SMU systems:

- Keithley 2636B: This instrument has two medium voltage SMUs with triaxial connectors sourcing voltages up to 200 V. In the presented work, it has been used to monitor the channel current during back bias ramp measurements as well as during UV illumination experiments.

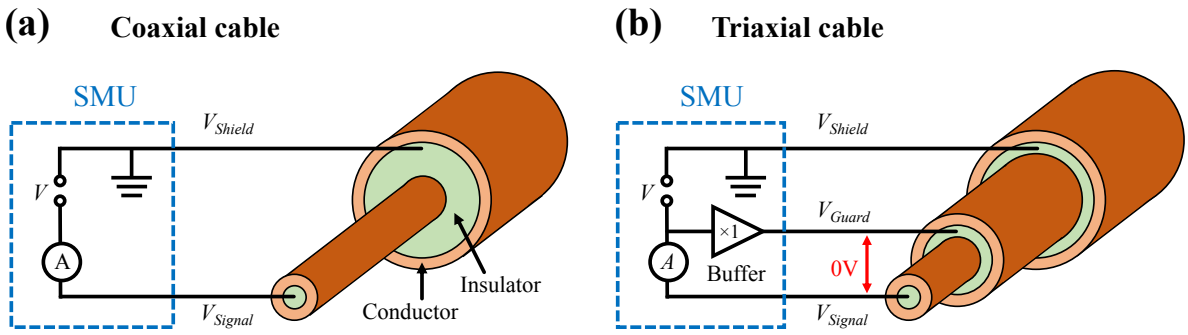

FIGURE 3.2. Cross-sectional view and basic circuit of a) the coaxial cable and b) the triaxial cable.

- Keithley 2657A: This instrument has one high voltage SMU with triaxial connectors sourcing voltages up to 3 kV. Here, it has been used to bias the substrate for back bias ramp measurements.
- Keithley 2410: This instrument has one high voltage SMU with banana connectors sourcing voltages up to 1100 V. As part of this thesis, it has been used to externally source the high substrate bias into the AFM instrument during back-biased KPFM measurements.

The instruments have been controlled using LabView or Test Script Builder (TSB).

3.1.3 Cabling

There are two main cable configurations used to contact the SMU to the device: coaxial and triaxial cables. The coaxial cable, as pictured in fig. 3.2a, has a grounded outer isolation which shields the cable core from external electromagnetic interference. Hence, coaxial cables are suitable for sensitive electrical measurements. However, when measuring low currents, the leakage through the dielectric can become significant compared to the current signal preventing precise current measurements. Introducing an additional conductor between core and shield, as shown in fig. 3.2b, referred to as guard, tackles that problem and creates a triaxial configuration. The guard is biased through a current buffer at the same voltage as the core. Consequently, there is no potential between guard and core. As there is no electric field, there cannot be any leakage current to and from the core. The leakage will still occur between guard and shield, however, the current is provided by the buffer which enables accurate measurements of low current signals.

3.2 DC measurements

DC measurements are useful for probing a variety of different device properties. This includes but is not limited to investigating the device pinch-off voltage, transconductance, maximum drain

current, and charge carrier mobility. DC measurements also allow testing of the contact and sheet resistance as well as various leakage mechanisms.

3.2.1 Current–voltage measurements

Current–voltage (*IV*) measurements are one of the basic characterization tools. Measuring the drain current while sweeping the gate voltage analyzes the device switching characteristics. Measuring the drain current versus drain voltage probes the output power capabilities. The current is typically normalized by the device width which gives the electric field dependent current density. The output and switching implications of these basic measurements have been discussed in section 2.4.2 and section 2.4.3, respectively.

The *IV* characteristics are also directly related to the device transport processes. Temperature dependent *IV* measurements allow analysis of any thermally activated transport mechanisms. Practically, that is performed by using a thermal chuck and setting the wafer temperature. Utilizing the Arrhenius formula

$$I = I_0 \, \exp\left(\frac{E_A}{k_\mathrm{B} T}\right), \tag{3.1}$$

a temperature dependent current can yield the activation energy E_A of the process. This energy often relates to the trap energy level causing leakage currents, however, changes in device temperature also simultaneously induce other effects such as a modification in electron mobility that need to be taken into account [172].

3.2.2 Contact resistance and sheet resistance measurements

An ungated device structure is shown in fig. 3.3a. The total source-to-drain resistance is comprised of a series of twice the contact resistance R_C plus the channel resistance $R_{Channel}$ which itself is related to the sheet resistance R_{Sheet}. The contact and sheet resistance is measured using the transmission line method (TLM) as pictured in fig. 3.3b. The TLM structure consists of a linear wafer strip with an isolated 2DEG underneath. The 2DEG is contacted with a series of ohmic contacts with increasing spacing. In this technique, the resistance of neighboring ohmic contacts gets measured separately. The individual resistances are plotted against the various channel lengths. Fitting a linear line, as shown in fig. 3.3c, gives the contact resistance R_C and sheet resistance R_{Sheet} according to

$$R(L) = \frac{R_{Sheet}}{W} \, L + 2R_C \tag{3.2}$$

with channel width W. The origin of the fit line is at the L-axis intercept equal to $-2L_T$ referring to the transfer length L_T. The conduction contribution from the ohmic contact to the channel is maximum at the channel edge of the contact exponentially decaying away from the edge. Therefore, the transfer length L_T represents the effective length of the ohmic contact.

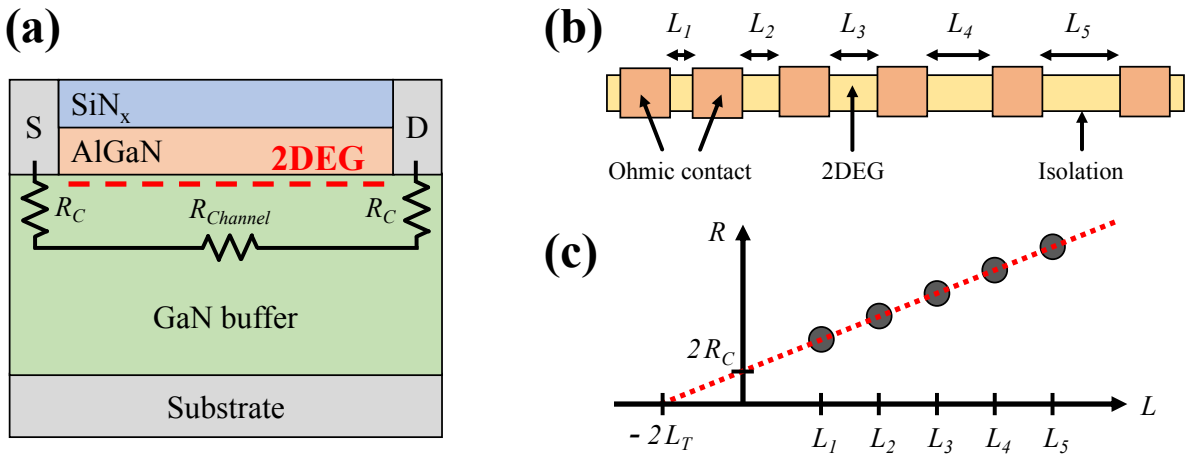

FIGURE 3.3. Illustration of sheet and contact resistance measurement with a) source-to-drain resistances, b) a schematical TLM structure, and c) the fit of resistances versus different channel lengths.

3.2.3 Persistent photoconductivity measurements using four-wire resistance measurements

The persistent photoconductivity (PPC) effect can be quantified by measuring the resistance of a TLM structure under the exposure of external influence compared to the state of a fully recovered or a pristine sample. In this thesis, the UV-induced PPC effect was investigated by quantifying the increase in channel conductivity with respect to the illumination of light with an energy greater than the GaN band gap. The channel conductivity was analyzed by measuring the channel resistance using a four-wire cabling setup in order to eliminate parasitic resistive influences of the cabling (fig. 3.4a).

To accurately quantify the magnitude of the UV-induced PPC effect, the sample should first be kept in darkness for a long time (e.g. one month) to allow full recovery from previous exposure to light. Similarly, these light sensitive measurements have to be undertaken in a fully darkened laboratory room. Firstly, as reference, the channel resistance is measured in dark conditions. Subsequently, the samples is illuminated with light for a certain time to allow the sample to stabilize under illuminated conditions. Typically, a few minutes are sufficient, after which the channel resistance is measured again under light illumination (fig. 3.4b). Finally, the magnitude of the PPC effect is calculated by the ratio of the two measurements.

3.2.4 Leakage measurements

The GaN HEMT consists of a complex stack of several layers. Therefore, there are various pathways for leakage currents. Using a specific leakage test structure as pictured in fig. 3.5a, different leakage mechanisms can be analyzed. The configuration consists of one ohmic contact

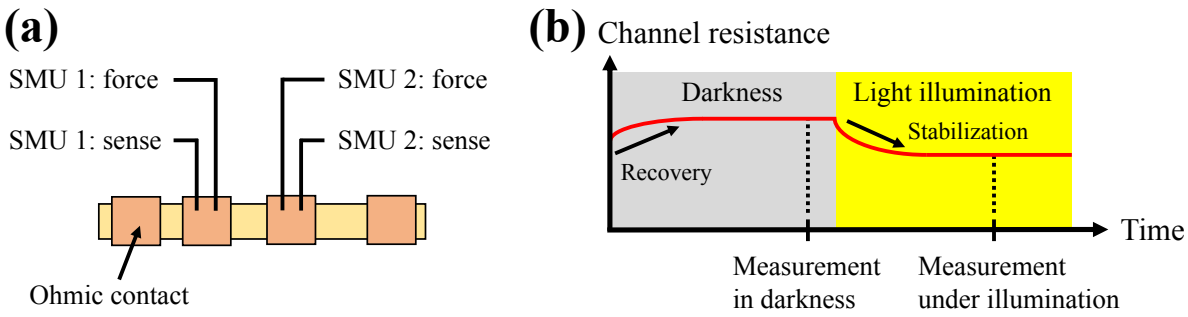

FIGURE 3.4. Schematic of a) the four wire probing configuration and b) the sequence of measurements using a TLM structure.

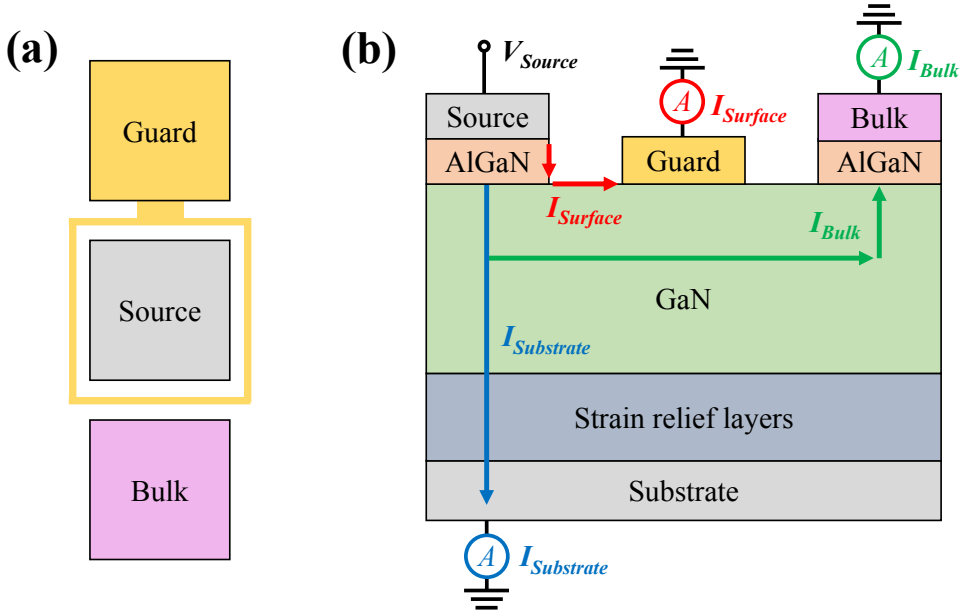

FIGURE 3.5. Leakage current analysis with a) the test structure and b) the different measurable leakage current contributions.

labeled 'source' which is used to bias the structure. It is surrounded by the 'guard' contact sitting on top of the GaN layer. The other ohmic contact labeled 'bulk' is electrically isolated from the source by a mesa etch. Using this structure, leakage mechanisms such as surface leakage, bulk leakage, and substrate leakage can be analyzed as seen in fig. 3.5b. The guard contact will pick up any surface leakage current, typically on the order of 10^{-10} A when applying several hundreds of volts to the source. Lateral leakage through the epitaxy is measured at the bulk contact, usually on the order of 10^{-9} A. The substrate contact collects vertical leakage through the entire stack which is normally on the order of 10^{-8} A.

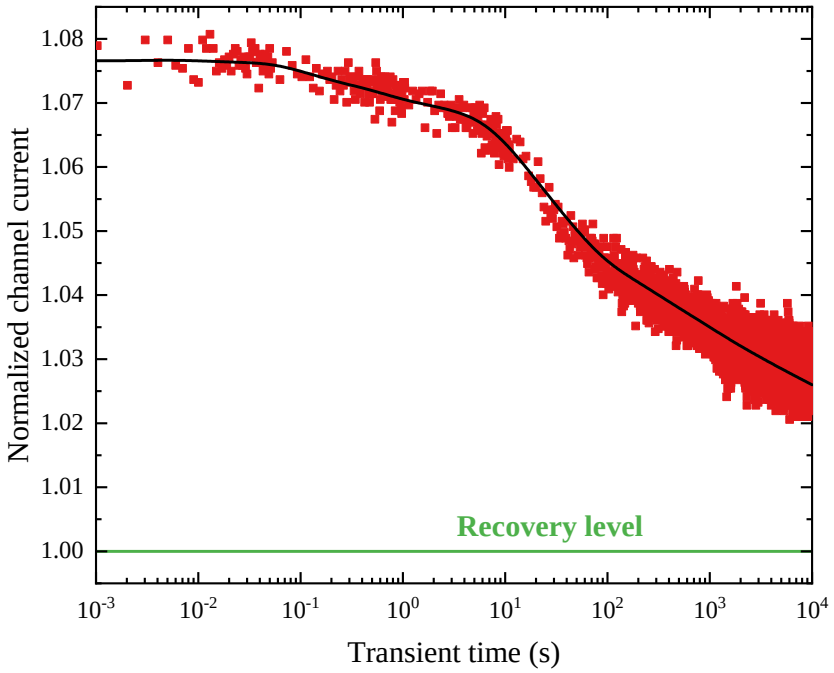

FIGURE 3.6. Example of a transient measurement with current recovery after UV illumination. The black line is a fit as guidance to the eye.

3.3 Transient measurements

While static measurements such as several DC techniques investigate certain HEMT operation conditions, they exclude any kinetics. Transient measurements can probe all kinds of process dynamics such as charge trapping and detrapping. There are different measurement setups targeting different involved processes, however, they all work with the same principle. The sample is stressed in a certain state for a given time. Then, the stress is abruptly released and, typically, a constant voltage is applied to the drain while continuously monitoring the channel current.

One example used in this thesis is a transient measurement investigating the recovery from UV illumination as pictured in fig. 3.6. Here, the sample was illuminated with UV light of 360 nm causing an increase in channel conductivity. Upon illumination stop, the current starts to relax towards the initial value measured in darkness. The transient shows several time constants on different orders of magnitude. Evidently, the channel conductivity does not fully recover to the initial level within the measured time.

Another, more typical measurement related to the HEMT operation is off-state stressing combined with on-state recovery transients. The involved trapping and detrapping time constants τ can be correlated to deep level trapping processes. Temperature dependent transient measurements probe the trap activation energy E_A. The transients are subsequently fitted with a stretched multiexponential function. The peaks of every respective differential are then plotted in an Arrhenius plot with $\ln(\tau T^2)$ vs. $1/k_B T$. Lastly, a linear fit through the data points yields

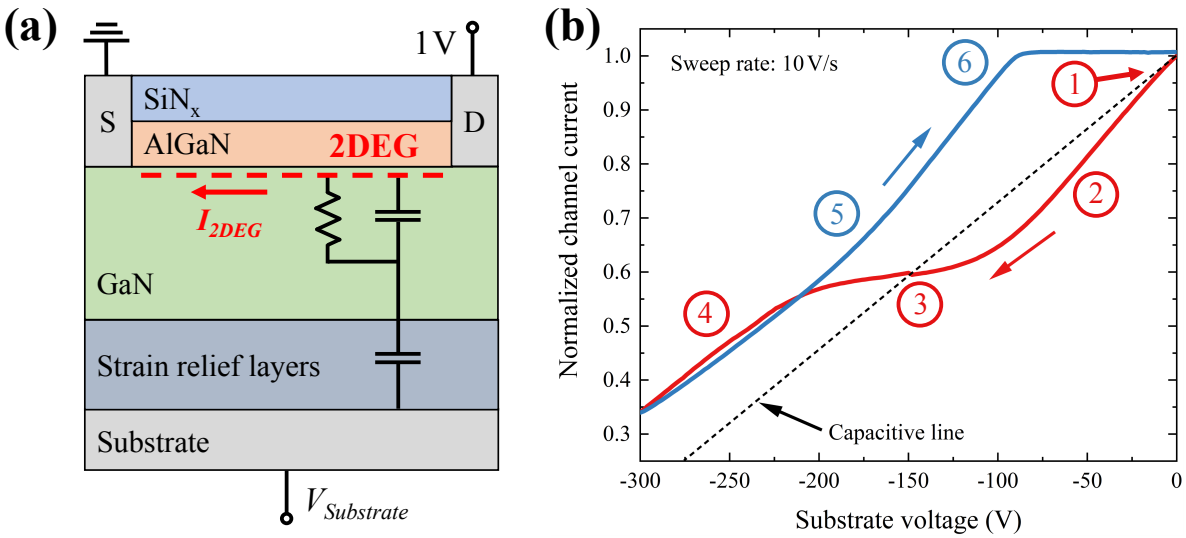

FIGURE 3.7. Back bias measurement technique with a) the electrical stack configuration and b) a typical back bias ramp with both downward (red) and return (blue) sweep.

the slope related to the trap activation energy E_A and the intercept related to the trap capture and release cross-section [173].

3.4 Back bias measurements

Substrate voltage ramp measurements are a powerful tool to examine crucial buffer characteristics as introduced in section 2.2. This technique uses the channel conductivity to sense various buffer effects by using the substrate as back-gate. A small voltage of typically 1 V is applied across a TLM structure which monitors the channel current while the substrate voltage is swept (fig. 3.7a). The magnitude of the channel current depends on the electron concentration in the 2DEG which in return is influenced by the buffer underneath. Applying a substrate voltage in a hysteresis fashion sweeping to high negative voltages and back to zero as shown in fig. 3.7b acts on the buffer which in return changes the 2DEG carrier concentration. Therefore, the channel current through the 2DEG acts as sensor for buffer effects induced by sweeping the substrate voltage. In region 1, at low negative voltages, the measured current follows a straight line of capacitive coupling where the epitaxial stack behaves insulating. In region 2, beyond a certain voltage threshold, the leakage current into the resistive GaN buffer exceeds the displacement current. This results in a charge redistribution which builds up a dipole from top to bottom. For this reason, the transconductance increases which causes the current to drop below the capacitive line. In region 3, the current reaches a plateau corresponding to positive charge storage at the heterojunction to the resistive buffer. This means that the resistivity of the channel has dropped below the resistivity of the buffer. This typically relates to occurring band-to-band leakage in the

channel layer facilitated by traps. Electrons from the buffer flow to the channel which leaves holes behind in the buffer. Those holes accumulate at the bottom interface diminishing the channel electric field which leads to the observed current saturation. In region 4, at higher negative back biases, leakage starts to occur throughout the stack exceeding the displacement current in all layers. Electron injection from the substrate adds to the vertical leakage. Applying a certain negative voltage high enough and beyond what is shown in the plot causes a full depletion of the 2DEG resulting in total cancellation of the channel current. This substrate voltage is typically referred to as back-gated pinch-off voltage. On the return sweep in region 5, the stored positive charge remains at the heterojunction and renders the stack insulting. In region 6, the stored positive charge reverses the electric field underneath the 2DEG. Electrons flow back into the stack neutralizing the positive charge in the buffer. The channel current reaches back to the initial level. This stack showed a clockwise loop with positive charge storage which is neutralized towards the end of the return sweep. On the contrary, a stack observing negative charge storage shows a counterclockwise loop. Its final current does typically not reach the initial channel current level but a value significantly below it [89].

3.5 Scanning probe microscopy

Beside analyzing the electrical performance of a fully processed GaN HEMT, there are many techniques that can give additional insights into the fundamental material properties. Scanning probe microscopy is beneficial to probe nanoscale features on the surface of a GaN epitaxy. In this regard, in this thesis, mainly atomic force microscopy and related techniques were used.

In the presented work, the used instrument was a Dimension Edge system from Bruker. Beside topography mapping using different scanning modes (contact mode, tapping mode, peak force tapping mode) with a height resolution of about 0.2 nm, the instrument is also capable of other related techniques such as surface potential scanning only using amplitude modulation as well as surface current mapping with different input gains. The internal system limit for the probe and chuck voltage is 10 V. The instrument was therefore externally upgraded using a Keithley 2410 with the ability to supply substrate voltages up to 1100 V as explained in chapter 4.

3.5.1 Atomic force microscopy

The primary aim of atomic force microscopy (AFM) is to map the surface topography using the interaction force between the probe and sample. The tip is typically shaped as pyramid or cone with an apex radius typically less than 10 nm which provides the nanoscale resolution. The tip is fabricated at the end of a cantilever with a resonant frequency on the order of $50 - 350$ kHz. Generally, the tip plus cantilever is referred to as probe. As shown in fig. 3.8a, the probe is connected to a piezoelectric actuator which makes the cantilever oscillate. This holder is connected to a piezoelectric scanner that performs x and y movements for mapping as well as

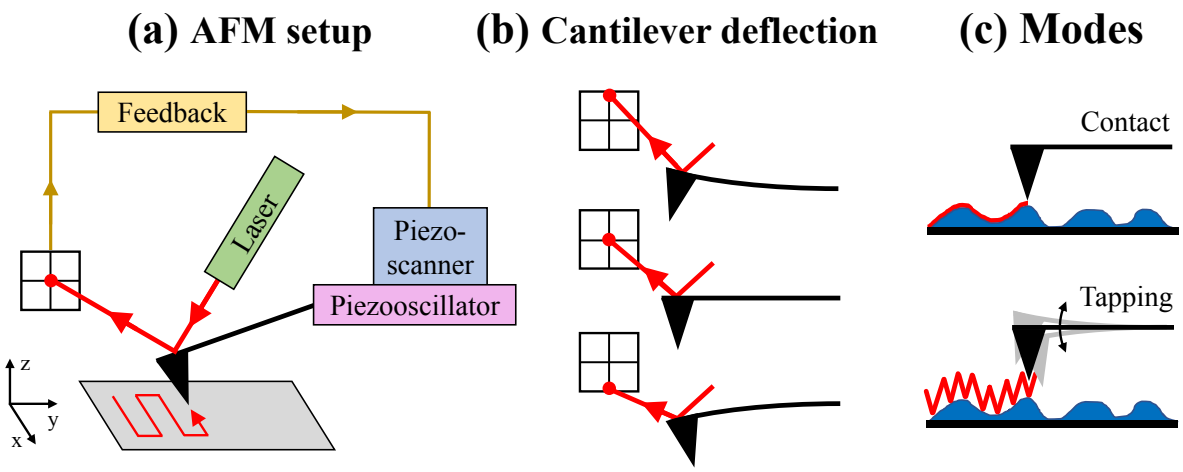

FIGURE 3.8. Principle of atomic force microscopy with a) the AFM setup, b) the cantilever deflection, and c) different scanning modes.

adjustments in height z based on the feedback loop response. The feedback input originates from the deflection signal of the laser beam reflection on the back of the cantilever. As seen in fig. 3.8b, the deflection signal depends on the cantilever bending. Using the signal of the four-quadrant sensitive detector, the feedback is designed to maintain a certain set deflection value owing to the repulsive or attracting forces between probe and sample by adjusting the probe–sample distance. The probe is moved line-by-line across the surface by the piezoscanner. Recording the z movement of the height adjustments, a 2D topography map can be measured. There are several different measurement modes and how the feedback is obtained. Contact and tapping mode are among the most widely used methods, illustrated in fig. 3.8c. They both work in the repulsive regime and maintain a set point for the deflection signal. In contact mode, the probe is in constant contact with the sample and moved along the surface. On the other hand, in tapping mode, the cantilever is stimulated to oscillate close to its resonant frequency. Consequently, the probe taps along the surface instead.

3.5.2 Electrostatic force microscopy

Electrostatic force microscopy (EFM) measures the electrostatic forces between sample and an electrically conductive probe. EFM is a two-pass measurement where the first pass measures the topography with an AFM line scan and the retrace scan performs the EFM line scan with a probe lifted by about $20-50\,\mathrm{nm}$. Thereby, in an alternating routine, both the topography and the electrostatics are mapped line-by-line. During the EFM line scan, the cantilever is driven near the resonant frequency ω_0 while applying a DC voltage V_{DC} to the probe with respect to the grounded sample. To ground the sample, the chuck is grounded, hence, it is important to establish a good electrical contact between chuck and sample. As simple approximation, probe

and sample can be modelled as parallel-plate capacitor storing an energy of

$$E = \frac{1}{2} C \, (\Delta V)^2 \tag{3.3}$$

with sample–probe capacitance C and voltage ΔV between both plates. This causes a force F between both plates which can be written in terms of sample–probe distance z as

$$F = -\frac{\mathrm{d}E}{\mathrm{d}z} = -\frac{1}{2} \frac{\mathrm{d}C}{\mathrm{d}z} \, \Delta V^2 \, . \tag{3.4}$$

The voltage ΔV is the difference between the applied probe voltage V_{DC} and the contact potential difference voltage V_{CPD} as well as any externally induced voltage $V_{induced}$, such as an additional bias of an operating device, and can be expressed by

$$\Delta V = V_{DC} - (V_{CPD} + V_{induced}) \, . \tag{3.5}$$

This changes the equation of the electrostatic force acting on the cantilever to

$$F = -\frac{1}{2} \frac{\mathrm{d}C}{\mathrm{d}z} \left[V_{DC} - (V_{CPD} + V_{induced}) \right]^2 \, . \tag{3.6}$$

The gradient of the electrostatic force F affects the oscillating behavior of the cantilever including the resonating frequency, amplitude, and phase. The EFM signal is generated by detecting the phase change between cantilever drive and cantilever response. It is sensitive to the force gradient

$$\frac{\mathrm{d}F}{\mathrm{d}z} = -\frac{1}{2} \frac{\mathrm{d}^2 C}{\mathrm{d}z^2} \left[V_{DC} - (V_{CPD} + V_{induced}) \right]^2 \tag{3.7}$$

which is dominated by the probe interaction with the sample. EFM is therefore only a qualitative measurement with an approximate spatial resolution of the apex diameter [174, 175].

3.5.3 Surface potential measurement principle

Advancing EFM, quantitative measurements of the surface potential are possible. This works by determining the value of the contact potential difference (CPD). Generally, the work function of sample and probe are different given the respective material as shown in fig. 3.9a. Electrically connecting both materials causes both Fermi energies to level out at the same energy. This induces a contact potential difference voltage V_{CPD} as illustrated in fig. 3.9b. This potential difference entails attractive or repulsive forces acting on the probe depending on the sign of V_{CPD}. Applying a probe voltage V_{DC} that is equal to V_{CPD} balances out the previous potential difference while eliminating the forces at the same time. Experimentally, this is achieved by sweeping V_{DC} while monitoring the cantilever response using one of the metrics, for example the phase difference, which allows the determination of V_{DC} at which the forces are nullified. This value of V_{DC} then equals V_{CPD} at the measured spot. To obtain the absolute value of the sample surface potential Φ_{Sample} instead of V_{CPD} which is only relative with respect to the probe, the

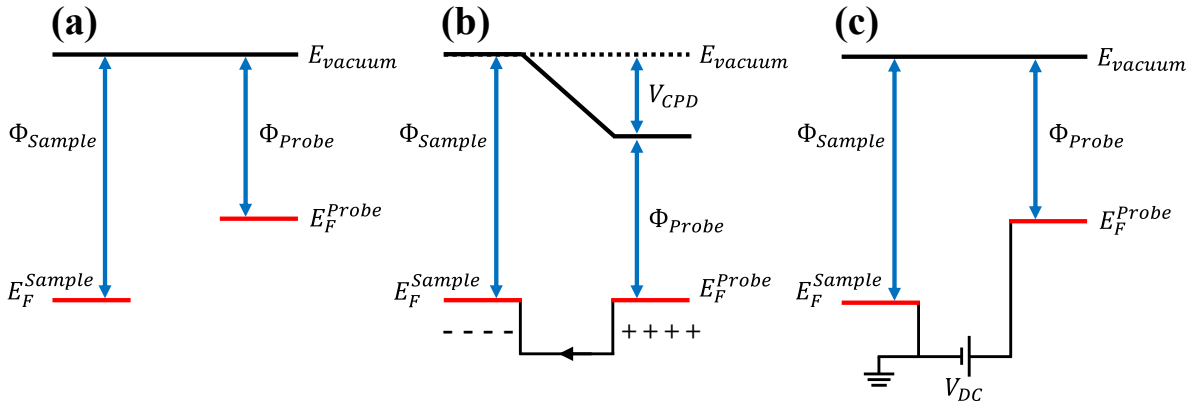

FIGURE 3.9. Schematic of the energy level configuration between sample and probe showing the Fermi level E_F with respect to the vacuum level E_{vacuum} when a) isolated, b) brought in contact, and c) compensated by an externally applied probe voltage.

work function of the probe (Φ_{Probe}) needs to be calibrated against a known reference material ($\Phi_{Reference}$) using

$$\Phi_{Probe} = \Phi_{Reference} - e\,V_{CPD}\ . \tag{3.8}$$

However, when qualitatively investigating features compared to the surrounding areas within one scan, the calibration is not required as it simply means a uniform value adjustment.

3.5.4 Kelvin probe force microscopy

Kelvin probe force microscopy (KPFM) exploits the previously introduced principle to determine V_{CPD} in a non-invasive manner. There are two different techniques that are used to generate the feedback signal: amplitude-modulated (AM) KPFM and frequency-modulated (FM) KPFM.

3.5.4.1 Amplitude-modulated KPFM

AM-KPFM can operate in both single-pass and dual-pass mode. In the single-pass mode, topography and V_{CPD} are typically recorded at the first and second cantilever resonant frequency as mechanical and electrical oscillation, respectively. On the contrary, in the dual-pass configuration, the cantilever resonates only at the first cantilever resonant frequency ω_0. In this case, the forward line scan is used to measure the topography using the cantilever resonant frequency mechanically while the probe is electrically grounded. On the reverse line scan, the probe is lifted by a constant sample–probe distance following the previously measured topography line and measuring V_{CPD} using the cantilever resonant frequency electrically as illustrated in fig. 3.10a. The dual-pass as opposed to single-pass has the advantage that there cannot be any mutual interference of signals since topography and V_{CPD} detection are fully separated. This usually

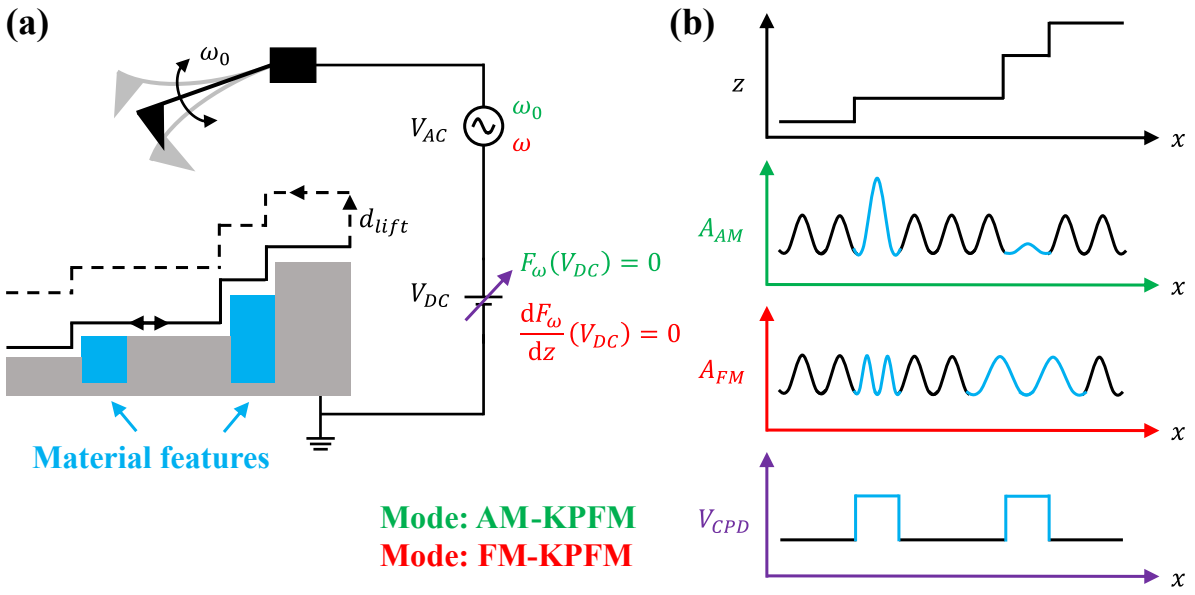

FIGURE 3.10. Principle of AM-KPFM in green and FM-KPFM in red with a) the setup and signal generation as well as b) the recorded signal topography height z, the measured KPFM amplitude for AM-KPFM, and FM-KPFM and lastly the processed V_{CPD} signal.

improves the signal-to-noise ratio of both topography and V_{CPD}. However, the constant electrical probe grounding and ungrounding can negatively influence the topography scan and generate erroneous features on the scan line edges.

The oscillating voltage

$$V_{AC} = V_{mod} \sin(\omega t) \tag{3.9}$$

applied to the cantilever creates an alternating force acting on the cantilever as seen in fig. 3.10b in green. The amplitude oscillation of V_{AC} creates an oscillating electric force

$$F_e = -\frac{1}{2}\frac{dC}{dz}\left[(V_{DC} - (V_{CPD} + V_{induced})) + V_{mod}\sin(\omega t)\right]^2 \tag{3.10}$$

with a DC term

$$F_{DC} = -\frac{1}{2}\frac{dC}{dz}\left[(V_{DC} - (V_{CPD} + V_{induced}))^2 + \frac{1}{2}V_{mod}^2\right], \tag{3.11}$$

with the first order component

$$F_\omega = -\frac{dC}{dz}\left[V_{DC} - (V_{CPD} + V_{induced})\right] V_{mod}\sin(\omega t), \tag{3.12}$$

and second order harmonic part

$$F_{2\omega} = \frac{1}{4}\frac{dC}{dz}V_{mod}^2\cos(2\omega t). \tag{3.13}$$

Using F_ω as feedback and minimizing its value by altering V_{DC} until F_ω is nullified allows measurements of V_{CPD} according to $V_{DC} = V_{CPD} + V_{induced}$. Therefore, AM-KPFM is sensitive to the force F_ω.

In AM-KPFM, the frequency ω of the oscillating bias V_{AC} is typically but not necessarily chosen to match a selected resonant frequency of the cantilever, for example $\omega = \omega_0$. This increases the sensitivity of F_ω and therefore the resolution of AM-KPFM measurements. A feedback loop by means of a lock-in amplifier operating at ω_0 uses the amplitude of the cantilever oscillation caused by F_ω and adjusts V_{DC} until the amplitude drops to zero. In this state, V_{DC} equals V_{CPD} assuming no other externally induced voltages ($V_{induced} = 0$) [176]. The signal processing is explained in more detail below in section 3.5.4.3.

The second order force component $F_{2\omega}$ determines the erroneous capacitive contribution. The cantilever beam is further away from the sample than the probe cone apex, however, it still has a significant contribution to the sample–cantilever capacitance given the large area. This has a strong parasitic influence on the AM-KPFM signal which worsens both the spatial and the V_{CPD} resolution, especially when the sample exhibits non-uniform electronic properties [177].

3.5.4.2 Frequency-modulated KPFM

FM-KPFM can be operated in both single-pass and lift-mode as well. Similar to AM-KPFM, FM-KPFM applies a voltage between probe and sample. This voltage is again a superposition of a DC voltage V_{DC} and an AC voltage V_{AC} with frequency ω. However, the principle in FM-KPFM is nullifying the component related to the electric force gradient instead of the electric force component itself. Hence, FM-KPFM is a technique that is sensitive to the force gradient

$$\frac{\mathrm{d}F_e}{\mathrm{d}z} = -\frac{1}{2}\frac{\mathrm{d}^2C}{\mathrm{d}z^2}\left[\big(V_{DC} - (V_{CPD} + V_{induced})\big) + V_{mod}\sin(\omega t)\right]^2 \tag{3.14}$$

and hence measuring the change of the mechanical resonant frequency.

In a similar fashion as for AM-KPFM, the equation can also be separated for FM-KPFM into the DC term

$$\frac{\mathrm{d}F_{DC}}{\mathrm{d}z} = -\frac{1}{2}\frac{\mathrm{d}^2C}{\mathrm{d}z^2}\left[\big(V_{DC} - (V_{CPD} + V_{induced})\big)^2 + \frac{1}{2}V_{mod}^2\right], \tag{3.15}$$

the first order component

$$\frac{\mathrm{d}F_\omega}{\mathrm{d}z} = -\frac{\mathrm{d}^2C}{\mathrm{d}z^2}\left[V_{DC} - (V_{CPD} + V_{induced})\right]V_{mod}\sin(\omega t), \tag{3.16}$$

and the second order term

$$\frac{\mathrm{d}F_{2\omega}}{\mathrm{d}z} = \frac{1}{4}\frac{\mathrm{d}^2C}{\mathrm{d}z^2}V_{mod}^2\cos(2\omega t). \tag{3.17}$$

Evidently, when V_{DC} is adjusted to exactly match V_{CPD} (assuming $V_{induced} = 0$), then the force gradient $\frac{\mathrm{d}F_\omega}{\mathrm{d}z}$ will decrease to zero. To detect the force gradient, the cantilever resonant frequency

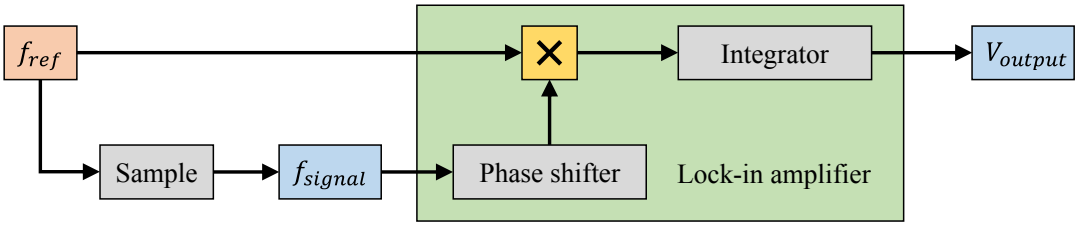

FIGURE 3.11. Working principle of a lock-in amplifier.

change is used. If a cantilever with spring constant k is oscillating in an external electric field, the effective spring constant k_{eff} is dependent on the electric force gradient by

$$k_{eff} = k - \frac{\mathrm{d}F_e}{\mathrm{d}z} \,. \tag{3.18}$$

The field gradient influences the fundamental cantilever resonant frequency

$$\omega_0 = \sqrt{\frac{k + k_{eff}}{m^*}} \tag{3.19}$$

with effective mass m^*. For small oscillations ($\mathrm{d}F_\omega/\mathrm{d}z \ll k$), the change in resonant frequency is

$$\Delta\omega \approx -\frac{\omega_0}{2k}\,\frac{\mathrm{d}F_\omega}{\mathrm{d}z} \,. \tag{3.20}$$

Consequently, an electrical oscillation applied to the probe modulates the electric force gradient which in return modulates the cantilever resonant frequency as pictured in fig. 3.10b in red. This means that applying an AC voltage V_{AC} oscillating at ω modulates both the first harmonic $\left(\frac{\mathrm{d}F_\omega}{\mathrm{d}z}\right)$ and the second harmonic $\left(\frac{\mathrm{d}F_{2\omega}}{\mathrm{d}z}\right)$ cantilever force gradient. Therefore, mechanically driving the cantilever at frequency ω_0 while electrically modulating the cantilever voltage at frequency ω results in four frequency side modes $\omega_0 \pm \omega$ and $\omega_0 \pm 2\omega$. The amplitude of both those frequency modes $\omega_0 \pm \omega$ is related to $\frac{\mathrm{d}F_\omega}{\mathrm{d}z}$. Hence, adjusting V_{DC} to null the amplitude of those two side frequencies can be used to measure V_{CPD} [176]. The signal processing in the feedback loop using a lock-in amplifier is further described below.

3.5.4.3 KPFM signal processing using lock-in amplifiers

As seen above, KPFM uses multiple frequencies simultaneously. To separate signals corresponding to different frequencies, lock-in amplifiers are essential. A lock-in amplifier is a phase-sensitive detector that can pick up a low intensity signal of known frequency from a very noisy signal that effectively consists of an entire spectrum of frequencies. Fig. 3.11 shows the working principle of a lock-in amplifier. A reference waveform f_{ref} at single frequency is used to stimulate a response from the sample. This happens simultaneously with other measurements using other frequencies, or no frequencies for static measurements equivalent to a continuous spectrum of frequencies. Hence, the recorded signal waveform f_{signal} is a superposition of all kinds of signals at different

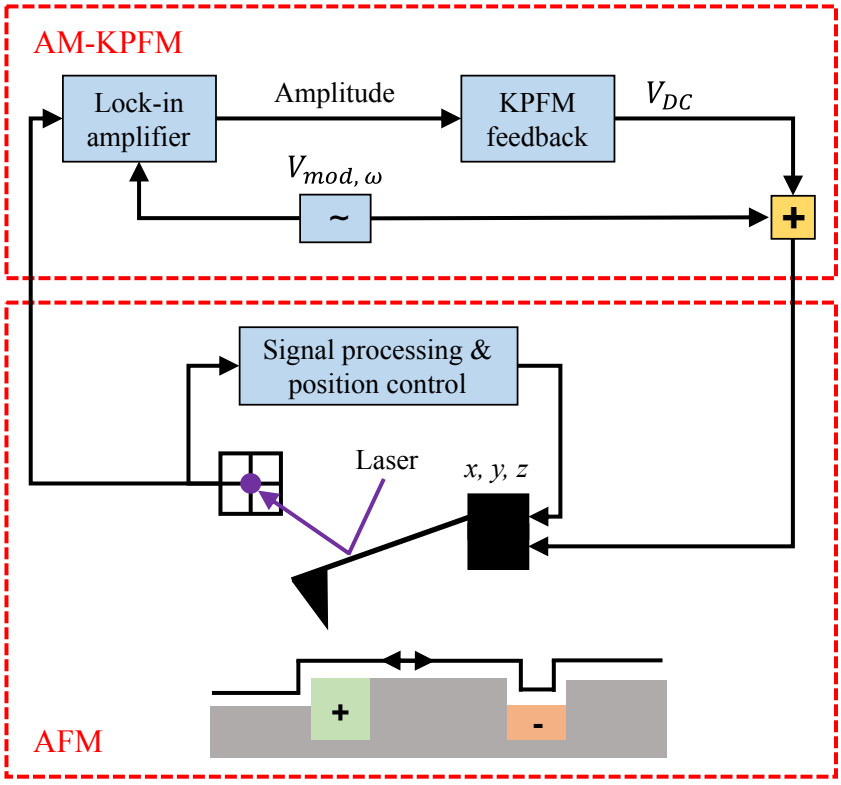

FIGURE 3.12. Schematic diagram of signal processing in AM-KPFM.

frequencies. Both waveforms f_{ref} and f_{signal} are fed to the lock-in amplifier where they get multiplied in the mixer. In case of a frequency match between both waveforms $(f_{ref} = f_{signal})$, the mixer outputs a DC voltage with a magnitude proportional to the amplitudes of the waveforms f_{ref} and f_{signal}. In all other cases $(f_{ref} \neq f_{signal})$, the mixer outputs voltage signals oscillating at the two frequencies $f_{ref} - f_{signal}$ and $f_{ref} + f_{signal}$. Integrating the mixer output with a long time constant suppresses the unwanted oscillating signals and their output is zero. Consequently, a lock-in amplifier can extract amplitude and phase of a signal at specific reference frequency f_{ref} among a noisy signal input f_{signal}.

AM-KPFM uses a single lock-in amplifier to detect the amplitude of the surface potential response of the cantilever deflection at V_{AC} frequency ω by setting the reference frequency f_{ref} of the lock-in to ω. Signals at other frequencies such as the DC component (eq. 3.11) and second harmonic component (eq. 3.13) are averaged to zero. The potential feedback loop adjusts V_{DC} until the amplitude of the lock-in output at ω is nullified according to eq. 3.12. Fig. 3.12 shows a diagram of the signal processing.

Proper AM-KPFM alignment requires adjustment of the phase shifter of the lock-in as seen in fig. 3.11. The relationship between the electric force F_ω and the total potential difference between probe and sample $(V = (V_{DC} - (V_{CPD} + V_{induced})) + V_{mod} \sin(\omega t))$ according to eq. 3.12 is not monotonic. F_ω has the same magnitude when V_{CPD} is positive or negative. When V is negative,

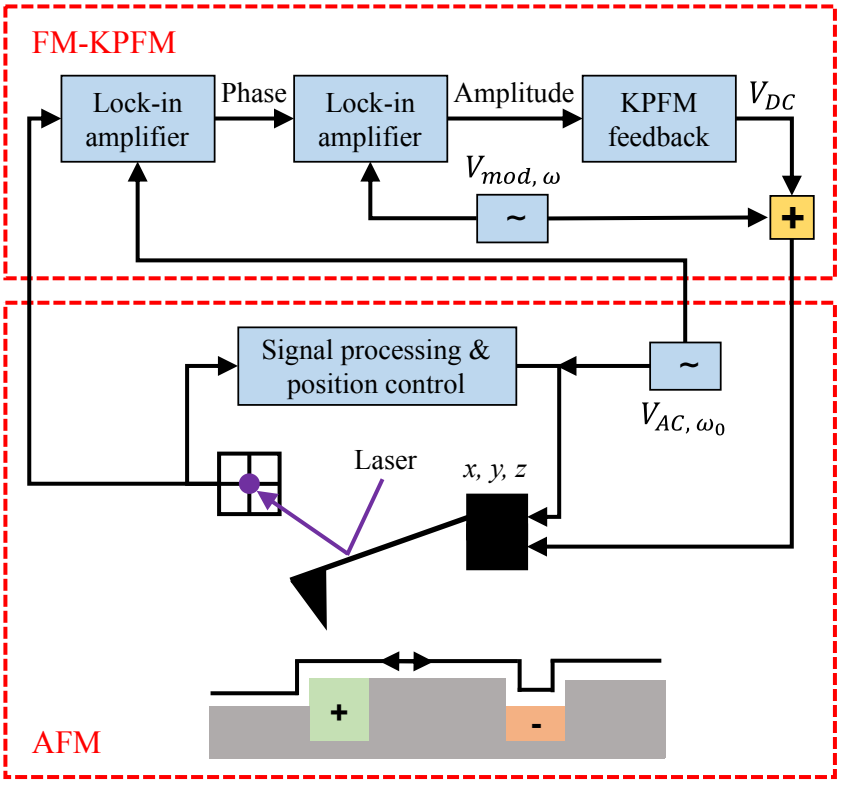

FIGURE 3.13. Schematic diagram of signal processing in FM-KPFM.

the electric force F_ω decreases with increasing V meaning F_ω is out of phase with V_{mod}. When V is positive, the electric force F_ω increases with increasing V meaning F_ω is in phase with V_{mod}. Therefore, it depends on whether the sample voltage is smaller or greater than the probe voltage resulting in a different phase between cantilever oscillation f_{signal} and the reference signal f_{ref}. For the lock-in to output the correct feedback direction, the lock-in phase has to be adjusted in the correct half range of the full lock-in phase range of $\pm 180°$.

FM-KPFM typically uses two cascaded lock-in amplifiers as shown in fig. 3.13. Combining eq. 3.20 with eq. 3.16, there is a frequency shift

$$\Delta\omega \approx -\frac{\omega_0}{2k}\frac{\mathrm{d}F_\omega}{\mathrm{d}z} = \frac{\omega_0}{2k}\frac{\mathrm{d}^2C}{\mathrm{d}z^2}\left[V_{DC} - (V_{CPD} + V_{induced})\right] V_{mod}\sin(\omega t) \tag{3.21}$$

due to the electrical force gradient $\mathrm{d}F_\omega/\mathrm{d}z$ that is varying with the AC voltage V_{AC} with frequency ω. The amplitude of the frequency modulation can be expressed as

$$\delta\omega = \frac{\omega_0}{2k}\frac{\mathrm{d}^2C}{\mathrm{d}z^2}\left[V_{DC} - (V_{CPD} + V_{induced})\right] V_{mod}\,. \tag{3.22}$$

Therefore, the cantilever deflection $x(t)$ with mechanical oscillation at cantilever resonant frequency ω_0 and electrical stimulation at frequency ω is

$$x(t) = A\sin\left\{\int_0^t \left[\omega_0 + \delta\omega\,\sin(\omega\tau)\right]\mathrm{d}\tau\right\} = A\sin\left[\omega_0 t - \frac{\delta\omega}{\omega}\cos(\omega t)\right] \tag{3.23}$$

with the cantilever amplitude A. For small electrically-induced cantilever deflections (i.e. $\delta\omega \ll \omega$), the cantilever motion $x(t)$ can be approximated as

$$x(t) = A\sin(\omega_0 t) - A\,\frac{\delta\omega}{\omega}\sin(\omega t)\cos(\omega_0 t) \tag{3.24}$$

with phase signal

$$\theta = \arctan\left[-\frac{\delta\omega}{\omega}\sin(\omega t)\right]. \tag{3.25}$$

The cantilever motion $x(t)$ can be transformed to

$$x(t) = A\sin(\omega_0 t) + \frac{A}{2}\,\frac{\delta\omega}{\omega}\sin\big[(\omega_0-\omega)\,t\big] - \frac{A}{2}\,\frac{\delta\omega}{\omega}\sin\big[(\omega_0+\omega)\,t\big]. \tag{3.26}$$

Thus, for small $\delta\omega \ll \omega$, the cantilever oscillates at the three frequencies ω_0 and $\omega_0 \pm \omega$. The amplitude of the side peaks at $\omega_0 \pm \omega$ is proportional to $\frac{\delta\omega}{\omega}$, however, the amplitude is difficult to detect directly with sensible resolution. Therefore, two cascaded lock-in amplifiers are used as shown in fig. 3.13. The cantilever deflection $x(t)$ is fed into the first lock-in amplifier with the lock-in reference frequency f_{ref} set to the cantilever resonant frequency ω_0. The lock-in phase output based on eq. 3.25 can be simplified to

$$\theta = -\frac{\delta\omega}{\omega}\sin(\omega t) \tag{3.27}$$

for small angles in case of $\delta\omega \ll \omega$. For further demodulation, the phase signal is fed to the second lock-in amplifier with the lock-in reference frequency f_{ref} set to the electric AC frequency ω. Consequently, the output voltage of the second lock-in amplifier is directly proportional to $\frac{\delta\omega}{\omega}$, the same proportionality as for the amplitude of the side peaks as seen in eq. 3.26. The output of the second lock-in amplifier is used as KPFM feedback to regulate V_{DC} in order to nullify $\frac{\delta\omega}{\omega}$ which in return determines V_{CPD} [176].

3.5.4.4 KPFM resolution and reliability

The resolution of AM-KPMF and FM-KPFM depends on various factors, however, the trend can be approximated using a highly simplified model where the tip of the AFM probe is modelled as sphere with radius R separated by a distance z from an infinite metal plate representing the sample surface (fig. 3.14). Assuming a potential difference ΔV between sphere and plate, the electrical force acting on both objects is

$$F(z) = -\pi\epsilon_0\left[\frac{R^2}{z(z+R)}\right]\Delta V^2 \tag{3.28}$$

with vacuum permittivity ϵ_0. The corresponding electrical force gradient is therefore given as

$$\frac{\mathrm{d}F}{\mathrm{d}z}(z) = \pi\epsilon_0\left[\frac{1}{z}+\frac{1}{z+R}\right]\left[\frac{R^2}{z(z+R)}\right]\Delta V^2\,. \tag{3.29}$$

The resolution of AM-KPFM is dependent on the electric force $F(z)$ whereas FM-KPFM is dependent on the electric force gradient $\frac{\mathrm{d}F}{\mathrm{d}z}(z)$. The equations clearly show that the force gradient

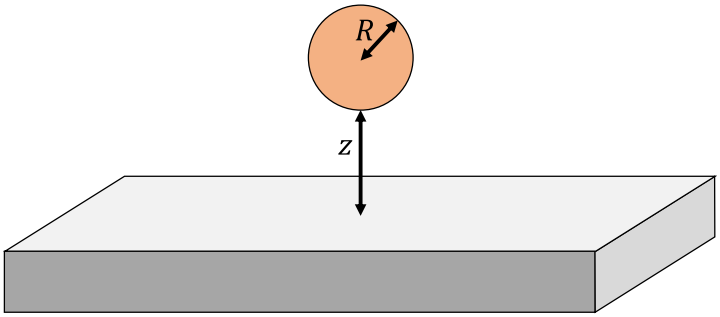

FIGURE 3.14. Simple model to examine KPFM resolution showing a sphere representing the probe tip with radius R in a height z above an infinite metal plate.

is much more localized due to the much steeper dependence on z. It has a stepper dependence in x and y direction as well which results in a better resolution for FM-KPFM over AM-KPFM [176].

Scientific studies examined the spatial resolution of KPFM and validated that FM-KPFM has a higher resolution than AM-KPFM [178–180]. It was found that for FM-KPFM, more than half the contribution originates from the front 0.3 % of the tip cone whereas for AM-KPFM, the contribution from the entire tip cone remains below 50 % [176]. Therefore, the measured V_{CPD} using AM-KPFM is in fact a weighted average over a larger sample area and the potential is distorted by capacitive coupling between the probe including the cantilever and different parts of the sample surface.

KPFM measurements are generally prone to reproducibility issues beside the usual problems arising from generic AFM and maybe electrochemically-induced reactions as well. The values of the KPFM signal are relative to the work function of the used probe which can vary significantly within one batch of probes [181]. Hence, the experiment depends on the material and coating of the probes making reproducing measurements harder. Another variable that influences KPFM measurements is the distance between probe and sample. This separation involves the fairly controllable lift height, however, it also includes the cantilever oscillation amplitude which highly depends on cantilever drive parameters as well as topography feedback loop settings resulting in a hardly unquantifiable sample–probe distance [176].

3.5.5 Conductive atomic force microscopy

Conductive AFM (CAFM) is another specialized AFM technique that measures electric bulk properties such as current conduction mechanisms or dielectric breakdown on a nanometer scale. It probes the topography using contact mode while simultaneously measuring the current through the sample at the touched spot as illustrated in fig. 3.15. A constant DC voltage is applied either to the chuck and hence the bottom of the sample or to the conductive probe. The resulting current can be as low as 1 pA which requires different degrees of current amplification depending

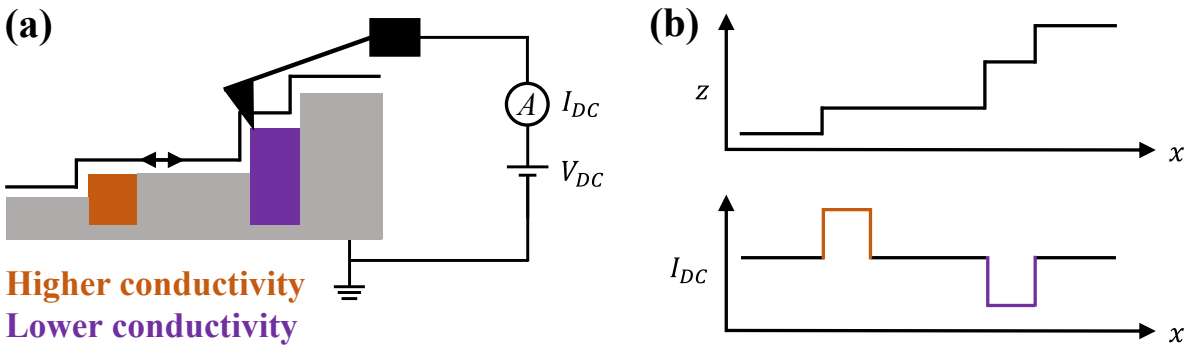

FIGURE 3.15. Principle of conductive AFM showing a) the measurement configuration in case the sample is grounded while the probe is biased and b) the recorded signals of topography and current.

on the current range. Areas of high conductivity become apparent by an increase in current whereas spots of low conductivity cause the opposite. As the probe is constantly in contact with the surface, usual conductive AFM probes utilizing a conductive probe coating wear off easily. Moreover, in order to establish and keep a good electrical contact between probe and sample, a sufficiently high contact force is necessary. Consequently, probes fully manufactured with a stiff and conductive bulk material such as boron doped diamond probes are more suitable than standard silicon probes only coated with a conductive material. A variation to the 2D mapping CAFM is utilizing CAFM locally on a particular spot of interest. Running an *IV* sweep on one point can give insights into the electrical characteristics of a certain feature of the sample as small as the tip diameter [182].

3.6 Simulation

Experiments have practical limits. Simulations on the other hand allow investigating unmeasurable and unintuitive processes on top of enabling understanding of internal device mechanisms. In this thesis, electrical simulations have been performed using the TCAD simulator ATLAS provided by Silvaco. The tool is specifically developed for electrical simulations on semiconductor devices. The basic principle of the simulator is based on solving the carrier transport and continuity equations in combination with the Poisson equation. This ultimately leads to the drift–diffusion equation

$$J_e = q\left(n_e \mu_e E + D_e \nabla n_e\right) \tag{3.30}$$

where J_e is the electron current density, q is the elementary charge, n_e is the electron concentration, μ_e is the electron mobility and D_e is the electron diffusion coefficient. This equation also holds true for holes with the respective parameter transformation. The electric fields experienced by electrons and holes can vary depending on the local curvature of the quasi-Fermi level [183].

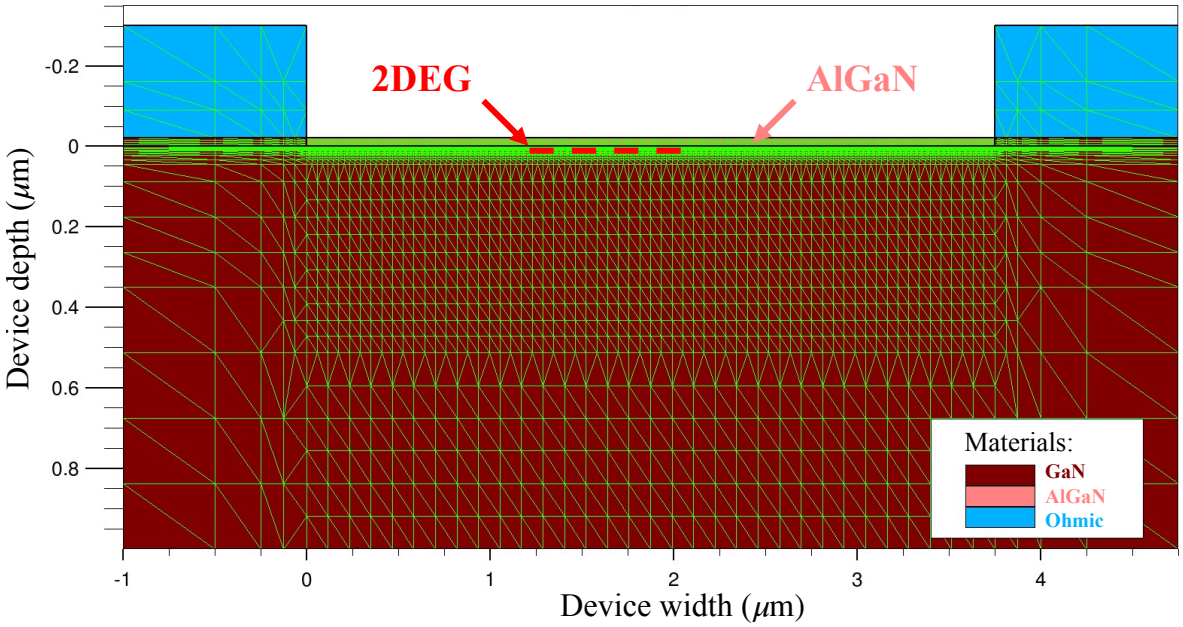

FIGURE 3.16. Simulation cross-section of a TLM structure overlaid with the mesh in green. In reality, the 2DEG spans all across the device underneath the AlGaN layer but the indication was shortened to show the denser mesh around the 2DEG.

The first step of the stimulation is configuring the device structure in a software called DevEdit. Typically, simulating a 2D cross-section of the device is sufficient for a regular GaN HEMT. However, for dislocation simulations or multichannel device simulations, a 3D configuration is necessary. For finite element computations, the device structure is overlaid with a triangular mesh. A typical cross-section of a TLM structure including the mesh is shown in fig. 3.16. In heterojunction areas with abrupt jumps of material properties or high electric fields, the mesh requires a higher density. Otherwise, the simulation may not converge and fail. That is particularly the case for the 2DEG as it is only a few nanometers thick. In the case of a TLM structure, the lateral node spacing is not as important given no high lateral electric fields. In general, an overall greater number of nodes is better, however, the more nodes, the longer is the simulation time.

The simulation with specific material parameters and measurement sequence is specified and run in a software called Deckbuild. The simulator has a comprehensive library of material properties which are automatically called when a device region is defined as a specific material. That includes parameters such as band gap and refractive indices as well as electron and hole mobility, affinity, and saturation velocity. However, those parameters can be overwritten with a user-defined value if necessary. For instance, the GaN bulk value of the electron mobility vastly underestimates the electron mobility present in the 2DEG. Dopants and traps can be added into the simulation as well. The key parameters of traps are energy level, density, capture cross-

section, as well as degeneracy. The simulation also requires setting which physical models should be enabled. That involves specifying charge carrier generation and recombination mechanisms as well as transport and scattering models. Those processes are calculated for each node of the mesh. The simulator also offers both static and transient simulations with varying ramp rates.

CHAPTER 4

BACK-BIASED KELVIN PROBE FORCE MICROSCOPY

One aim of this work was the development of a new measurement technique by combining the principle of back bias ramps as explained in section 3.4 with Kelvin probe force microscopy (KPFM) as introduced in section 3.5.4. This allows probing the effect of applying a high substrate voltage on the buffer potential and ultimately the surface potential. A key assumption in back bias measurements is the shielding properties of the 2DEG. Unless the 2DEG is fully depleted through a high negative back gate voltage, the entire back bias drops across the buffer between 2DEG and substrate while leaving the barrier and surface unaffected. This only holds true for areas of a continuous 2DEG whereas spots with defects can locally disturb the 2DEG. This is particularly the case for conductive threading dislocations which can penetrate deep into the epitaxy down to the substrate as shown in section 2.2.2 [184–187]. Therefore, applying a high negative back bias 'activates' spots of underlying conductive paths which affects the local surface potential mapping. On the other hand, areas between conductive dislocations with undisturbed 2DEG underneath do not change the surface potential upon applying any back bias.

This chapter focuses on the technical aspects of building and developing the measuring setup. It primarily discusses overcoming the hurdles that occur when trying to combine KPFM which operates in the millivolt range with substrate bias ramps that use hundreds of volts in close proximity to each other inside the AFM. The chapter first covers the measurement principle. The following part shows the result of the first primitive but successful measurement. The last sections discuss the optimizations of the identified remaining problems that arose from the initial measurements. Physical and GaN HEMT reliability implications are included in the subsequent chapter. The samples used in this study were fabricated by the Department of Electronic and Electrical Engineering at the University of Sheffield (UK).

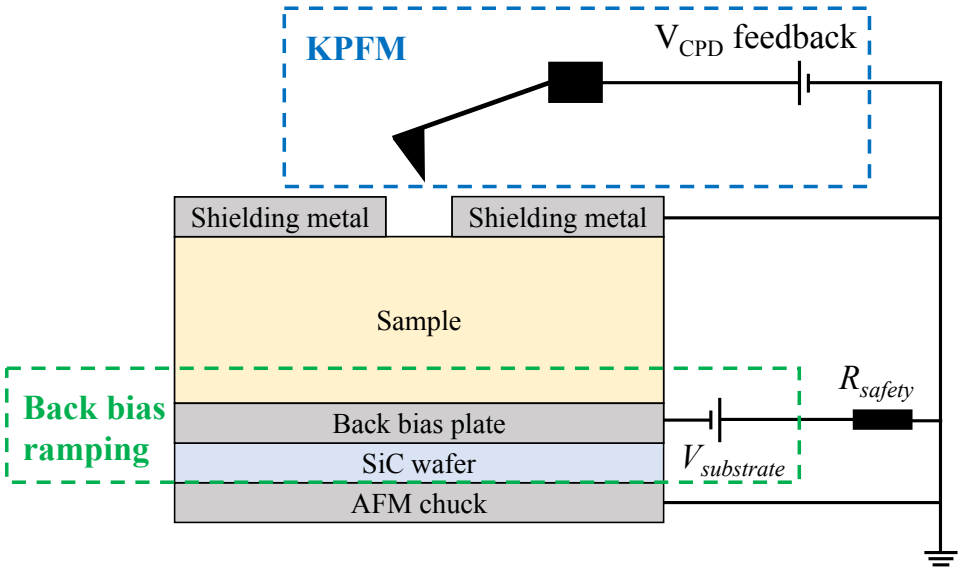

FIGURE 4.1. Principle and electric circuit of back-biased KPFM. The shielding metal is simultaneously the ohmic contact to ground the 2DEG.

4.1 Electrical implementation

For regular AFM measurements such as topography scans, the sample chuck is kept grounded. However, to facilitate electrical scanning probe measurements, AFM instruments usually allow the sample chuck to be biased. But AFM instruments can typically only bias the sample chuck up to ±10 V which is not enough to measure the back-gating characteristics over the entire voltage range of regular GaN buffers that are designed to withstand hundreds of volts. Therefore, this technique was implemented by modifying the KPFM configuration inside an AFM instrument. While in regular unbiased KPFM, the sample sits directly on the AFM chuck, here, the back bias setup with a separate bias plate was inserted between sample and AFM chuck, as shown in fig. 4.1 alongside the electric circuit. A back bias plate for back-gating the sample is separated from the grounded AFM chuck by an insulating SiC wafer to protect the AFM instrument. This configuration leads to two major problems: a) potential exposure of the expensive AFM system to high voltages and high currents in the event of a catastrophic sample breakdown and b) high erroneous fringing electric back bias fields. The former can be mitigated by inserting a high resistance in series with the back bias supply. The manufacturer of the AFM instrument advised limiting any currents to 1 µA to prevent damage to the system. This led to the choice of 1 GΩ for the safety resistance. The effect of the fringing fields can be addressed by shielding the KPFM detection system by measuring a large circular transfer length method (TLM) structure while grounding the large outer contact. Thereby, only the probe tip is exposed to the surface whereas the cantilever remains more protected. Hence, the test sample was processed with a mask having circular TLMs with an outer contact diameter of 1100 µm. An overall enclosure was constructed

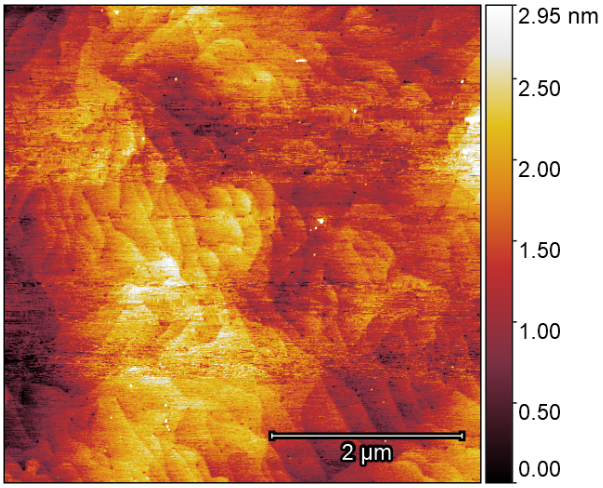

FIGURE 4.2. Topography image of the GaN surface in the scan area of the proof-of-concept back-biased KPFM measurement sequence. The quality is lower than usually shown in literature since the scan is not solely optimized to obtain clear topography features but to primarily yield good KPFM measurements.

around the AFM setup to prevent disturbance from external electric fields as well as for general safety purposes.

4.2 Primitive proof-of-concept measurement

The first successful measurement was achieved with a test sample that was grown using metal organic chemical vapor deposition (MOCVD) on a Si substrate. The buffer consisted of approximately 2.5 µm thick graded (Al,Ga)N buffer followed by 500 nm carbon doped GaN layer and a 250 nm thick unintentionally doped (UID) GaN channel. The AlGaN barrier with 25 % Al composition was 25 nm thick. The wafer had a 2 nm GaN cap. The sample was processed with Ti/Al/Ni/Au ohmic contacts alloyed at 800 °C in nitrogen ambient with Ti/Au top metal layer using circular TLM structures. The device was purposefully not passivated to keep the GaN surface exposed for KPFM measurements. Fig. 4.2 shows the topography of the GaN surface of the test sample. The topography features are less clear than commonly shown scans in literature since it is the corresponding topography scan for the back-biased KPFM measurement shown below in fig. 4.4 with compromised topography scan parameters. However, the atomic GaN steps and surface pits of threading dislocations (black spots at GaN step terminations) are still visible.

To prepare for the back-biased KPFM measurement, substrate ramp measurements were performed to determine the back-gated pinch-off characteristics. Exceeding the back-gated pinch-off voltage typically leads to rapidly increasing vertical buffer leakage which facilitates buffer breakdown and catastrophic sample short-circuiting. Therefore, knowledge of the back-gated pinch-off voltage is important to prevent sample breakdown which could lead to damaging the

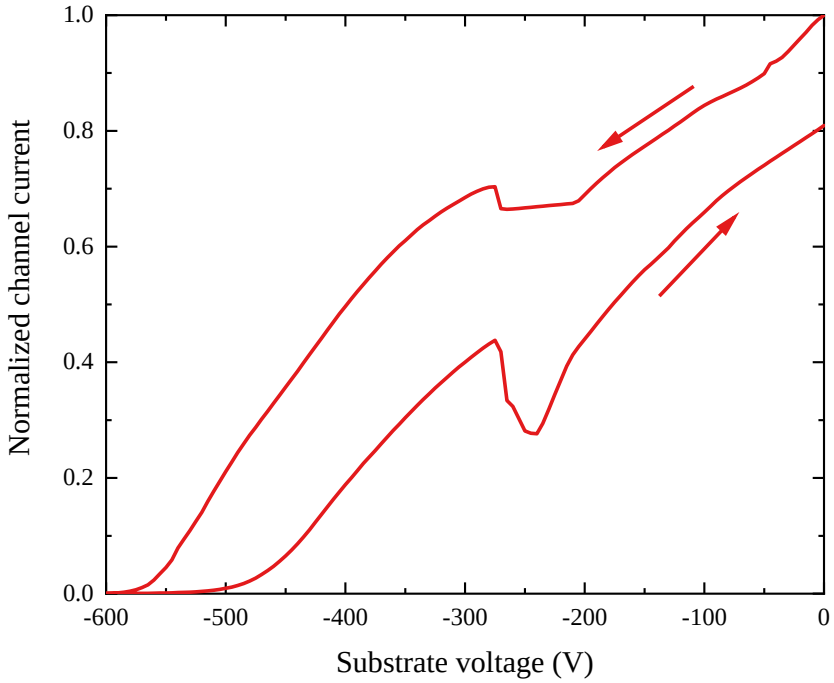

FIGURE 4.3. Substrate voltage ramp for the test sample used in the process of developing the back-biased KPFM setup. The ramp rate was $10\,\mathrm{V\,s^{-1}}$.

AFM instrument. During the gradual lowering of the substrate bias while measuring CPD maps, the sample has to remain at high substrate voltages and associated stresses for a long time. Approaching the back-gated pinch-off voltage leads to a depletion of the 2DEG (section 3.4). This eliminates the 2DEG as electrical screening sheet below the surface exposing the surface to the full effect of the high substrate voltage. Beyond this point, small substrate voltage steps cause large surface effects given the missing shielding in between. This results in a sharp decrease in surface potential for substrate voltages beyond the back-gated pinch-off voltage. Simultaneously, the noise of the KPFM measurement can be expected to increase substantially. Exposing the sample to voltages past its pinch-off severely risks device breakdown and consequent damage to the AFM instrument. Fig. 4.3 shows a back-gated pinch-off voltage of $-600\,\mathrm{V}$.

For the KPFM measurements, Pt-coated Sb-doped Si probes with a first harmonic resonant frequency of 70 kHz were used. Probes with other resonant frequencies were also tried but did not work well as shown in appendix A. This effect could be related to the different cantilever spring constants. A softer cantilever with a lower resonant frequency shows a higher sensitivity for weaker forces due to comparably larger induced oscillation amplitudes. There are multiple options for the setup of KPFM measurements as described above in section 3.5.4. For the available AFM system (Dimension Edge from Bruker), it was found that lift-mode with a lift height of 10 nm and a voltage V_{mod} of around 2 V yielded the best CPD signal resolution for this sample. The alternative KPFM configurations did not work well as shown in appendix A. The scan area was

chosen as $5\,\mu m \times 5\,\mu m$. Given reported densities for conductive dislocations of about $3-4\times10^{7}\,cm^{-2}$ [86, 97], the scan area is expected to contain at least a handful of conductive dislocations to become visible in the back-biased KPFM measurement. For each substrate bias step, the sample was allowed 5 min to reach equilibrium. The stabilization time has two particular reasons. The first consideration is the RC time constant of the circuit on the order of minutes. A large series resistance has the effect of increasing the time for the externally supplied substrate voltage to be dropped across the sample. The second point is allowing the charge redistribution and leakage in the epitaxial stack to stabilize according to the new bias stress conditions. The KPFM mapping resolution and scanning speed was a compromise between higher scanning resolution and shorter exposure time of the sample to high voltages. The total scan time for each bias step remained below 20 min.

Fig. 4.4 shows the sequence of CDP images for substrate voltage steps down to −700 V plus the reverse sequence followed by monitoring the recovery at no substrate bias for several hours. It can be observed that down to −200 V, the CPD signal remains homogeneous across the map. Starting at a back bias of −300 V, a dark feature appears in the top right corner. As the substrate voltage is swept down to −700 V, this feature becomes more pronounced while more smaller features appear at a back bias around −500 V. There are at least a handful of clear CPD features visible in the CPD images. Interestingly, the measurement noise did not increase substantially towards and past the pinch-off voltage of −600 V. Especially at −700 V, the 2DEG must have been fully depleted according to the back bias ramp (fig. 4.3), which is expected to expose the surface to drastic potential lowering as explained in section 3.4. When reversing the substrate voltage, the features gradually disappear again. The large feature in the top right corner remains visible at the end of the voltage sequence at no back bias. Therefore, the scanning was continued to monitor its evolution showing a gradual recovery on a time scale of hours. To analyze the measurement sequence further, the CPD values were extracted for three different locations as well as a reference spot, shown in fig. 4.5. The reference spot was chosen far away from any CPD feature. The CPD value for each spot was averaged over a radius of 100 nm. Interestingly, all spots exhibit a significantly increasing CPD for decreasing substrate voltage with a symmetric opposite trend on the reverse substrate bias sweep. Notably, that is also the case for the reference spot. Furthermore, after the sweep has returned to 0 V substrate bias again, the reference CPD value is lower than the initial value at the start of the sequence. That remains the case for subsequent measurements while slightly increasing over the following 10 h. Analyzing the three spots with respect to the reference shows the same effect as visually seen in the CPD images. The CPD value of spot 1 drops below the reference at a substrate voltage of −300 V remaining in that state until the end of the substrate voltage sweep, then slowly recovering over the course of 10 h with respect to the reference spot. The CPD value of spots 2 and 3 only drops below the reference for substrate voltages below −500 V.

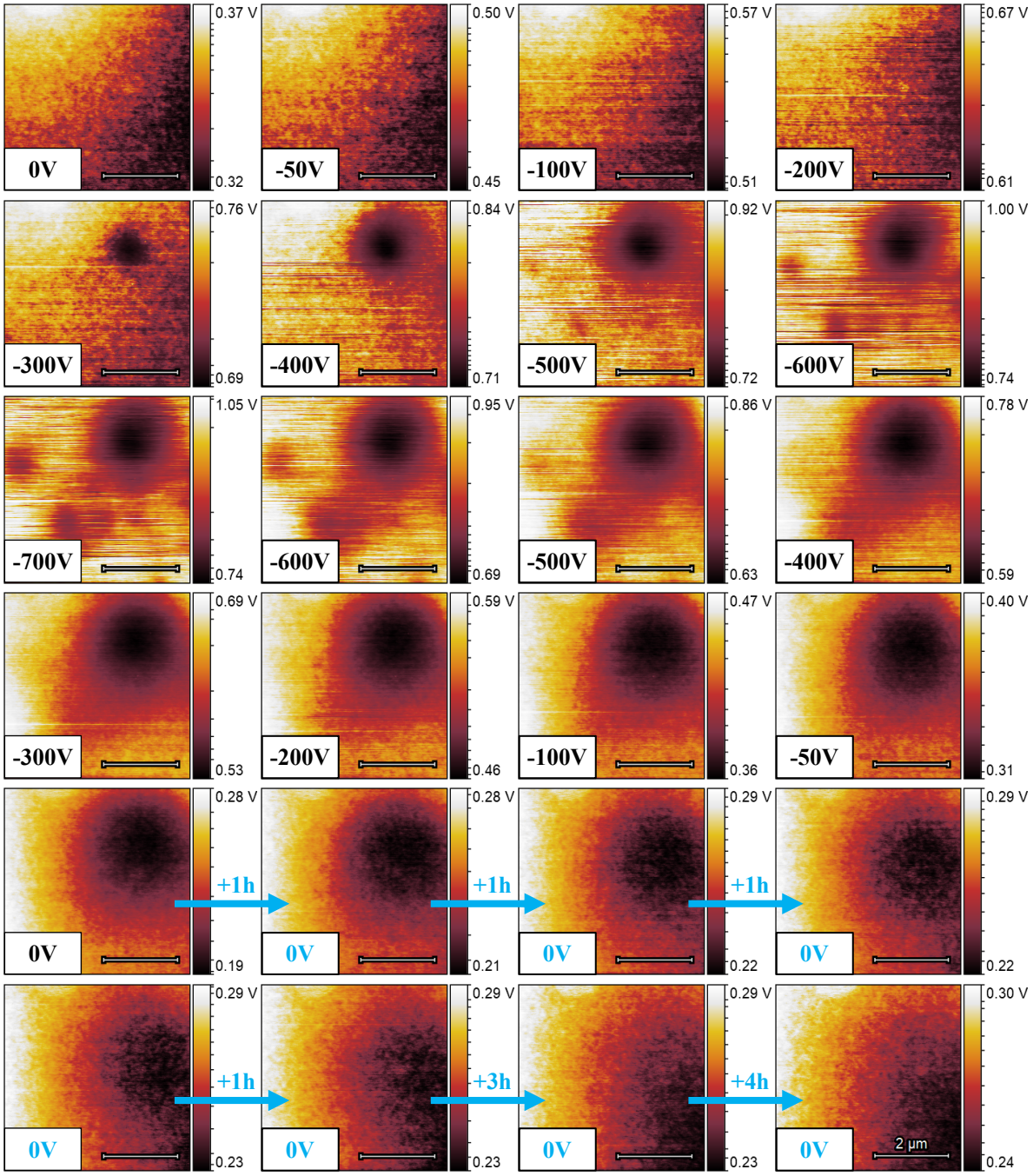

FIGURE 4.4. Sequence of CPD images while sweeping the substrate voltage downwards and in reverse. The time between CPD scans is about 0.4 h. After reaching no back bias again, a selection of pictures at certain time steps is shown. The scale bar is 2 µm.

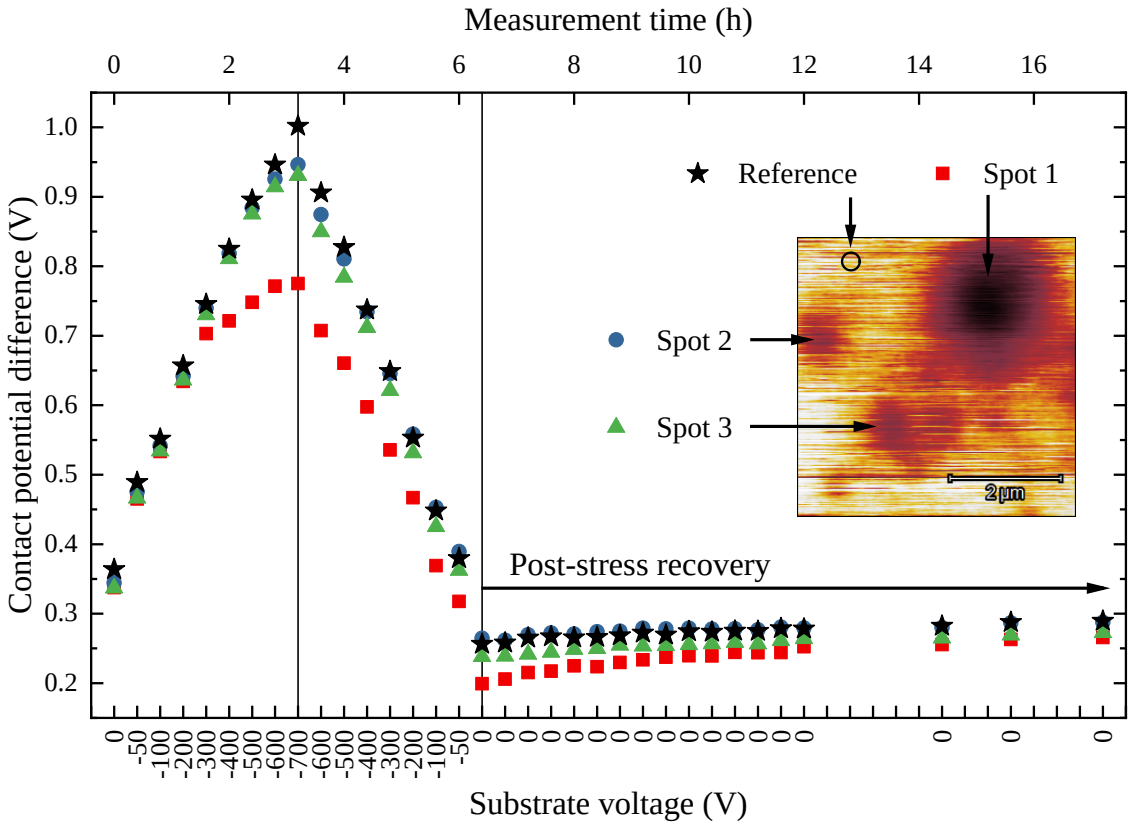

FIGURE 4.5. Spot analysis of the CPD signal for the back bias sweep used for troubleshooting in the process of developing the back-biased KPFM setup. The forward and return back bias sweep is followed by continuously monitoring the post-stress recovery for over 10 h. The inset shows the CPD image at a substrate voltage of −700 V with markers for the corresponding analyzed spots.

While the measurement was successful in resolving CPD features as the substrate voltage is lowered, it has revealed three major inconsistencies that need to be addressed:

- The change in reference signal is severe and significantly larger than the relative drops for the CPD features. This has been assigned to insufficient shielding of the KPFM detection system from fringing back bias fields.
- The noise of the CPD signal has not increased substantially towards and past the back-gated pinch-off voltage of the sample of −600 V. That condition seemingly made a KPFM measurement at a substrate voltage of −700 V possible. At this stage, the 2DEG should have been fully depleted making a KPFM measurement impossible.
- The CPD is increasing as the substrate voltage decreases. Validating the relation between surface potential and the output CPD value from the measuring system requires determination of the sign of the CPD in the used AFM instrument.

The analysis, mitigation, and optimization for the three points is explained in the following section. Other optimization attempts covering different KPFM measurement modes, different KPFM probes, and different measurement atmospheres are explained in appendix A. From all tested KPFM measurement modes, lift-mode with a low lift height yielded the best feature resolution. Regarding KPFM probes, the probes with a resonant frequency around 70 kHz worked the best. Equipping the AFM instrument with a nitrogen atmosphere did not change anything about the KPFM measurement.

4.3 Fringing field mitigation

The V_{CPD} feedback works by adjusting the voltage V_{DC} applied to the AFM probe on the order of millivolts. Consequently, fringing electric fields between biased substrate and KPFM system reaching around the sample and caused by the back bias on the order of hundreds of volts can severely disturb the KPFM feedback loop. Hence, to allow accurate and quantitative surface potential measurements, it is important to shield the cantilever from any erroneous fields as much as possible, particularly from the high voltage back bias.

Initially, a traditional circular TLM structure was deployed with an inner and outer ohmic contact diameter of 70 µm and 1100 µm, respectively, and a 10 µm gap in between both contacts (fig. 4.6a). This large structure with the largest outer contact was chosen to shield the KPFM system. Grounding the outer top metal, also connecting to the inner contact through the 2DEG, shields the cantilever from high voltage back bias fields. However, the CPD spot analysis (fig. 4.5) of the back-biased KPFM measurement sequence (fig. 4.4) still showed a significant shift in background potential when sweeping the substrate voltage. This influence prevents reliable quantitative back-biased KPFM measurements. To test the substrate bias dependent background CDP signal for this test structure, a systematic background scan was conducted. Fig. 4.7 shows the measurement of the background CPD signal when sweeping the substrate voltage for different locations on the TLM structure. The sequence of measurements starts at the center of the circular TLM structure gradually moving towards the outside while exposing more proportion of the cantilever to ungrounded surface. At the center of the TLM (sweep 1), the CPD voltage slightly decreases as the substrate voltage is lowered. The same trend is apparent when measuring in the TLM gap (sweep 2) which is in contrast to the previously shown back-biased KPFM measurement (fig. 4.5). One potential reason could be the different time scales of both measurements. The back-biased KPFM measurement allowed significantly longer stabilization times at high substrate voltages. The characteristics of decreasing background CPD signal remain when gradually moving the probe towards the TLM outside up to the point when the cantilever starts to get exposure to the TLM periphery (sweep 6). From this point, the trend is reversed with increasing CPD values for decreasing substrate voltage. The further out the probe is placed with respect to the TLM structure, the more extreme the background CPD potential shift becomes. Furthermore,

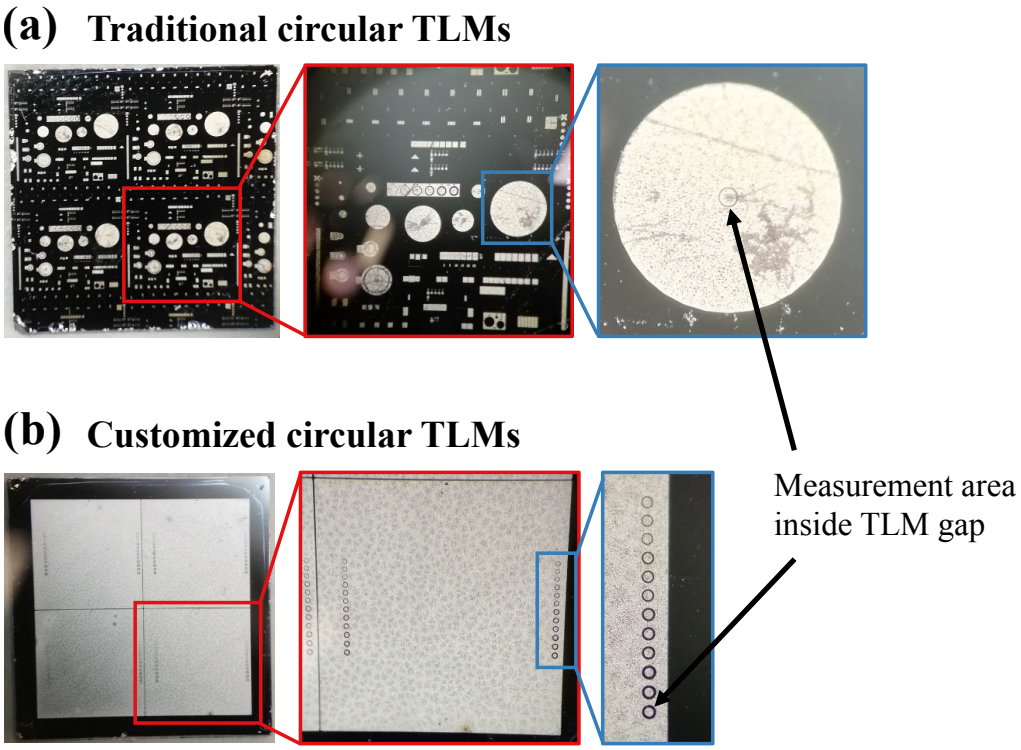

FIGURE 4.6. Optical images of a) the used traditional circular TLM structure and b) the customized TLM structure with more details in fig. 4.8.

many sweeps show a hysteresis trend with greater CPD value on the reverse sweep which is contrary to fig. 4.5. Using a single-pass KPFM instead of lift-mode KPFM made the trend of a highly substrate bias dependent background CPD signal even more severe.

Consequently, considering both this background measurement (fig. 4.7) and the actual back-biased KPFM measurement (fig. 4.5), there is no systematic trend and behavior of the CPD background. Nevertheless, the effect is severe in terms of order of magnitude, shows a hysteresis effect, and decreases or increases with lower substrate voltage. It was therefore concluded that the influence of the background has to be minimized further. To accomplish that, two factors were identified: optimizing the TLM structure and improving the back bias supply exposure which are both discussed in the following sections.

4.3.1 Device structure optimization

During the first successful back-biased KPFM measurement, it was seen that there is a substantial shift in background CPD signal when sweeping the substrate bias (fig. 4.5). Therefore, it is essential to optimize the test structure to increase the shielding properties and protected the KPFM detection system from fringing high voltage back bias fields. To ensure that, a special ohmic contact processing mask was developed to allow the deposition of shielding metal onto

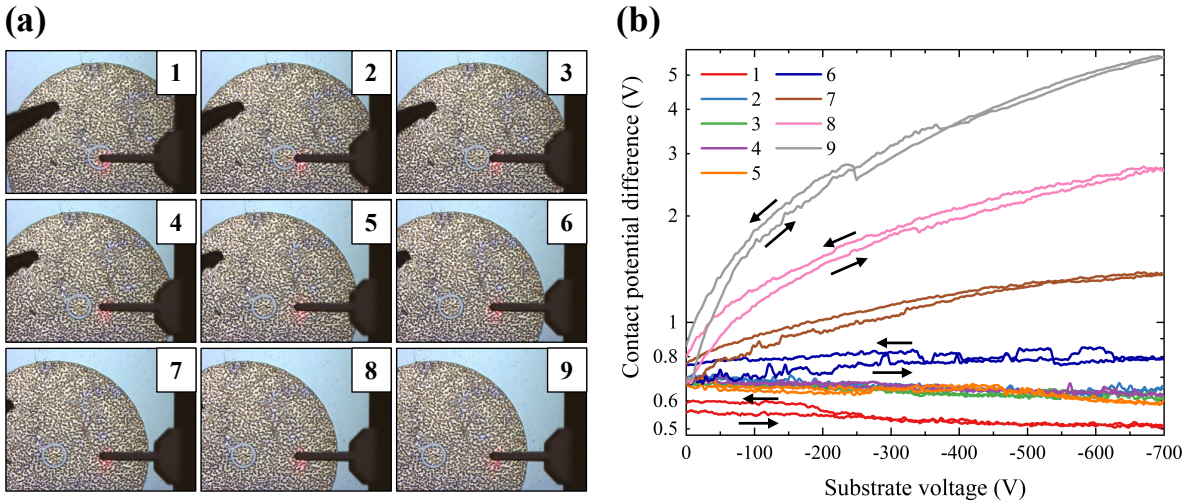

FIGURE 4.7. Background CPD signal test for different locations on test structure showing a) the measurement spot starting at the center of the TLM structure (image 1) gradually reaching the outside of the TLM structure (image 9) and b) a back bias sweep measuring the CPD for each location with a scan rate of $10\,\mathrm{V\,s^{-1}}$. The probe was engaged to the surface and stationary for each measurement. The black needle on the left side in image 1 is the probe which grounds the outer TLM contact.

the sample everywhere but in small gaps where the KPFM measurement can be performed. Simultaneously, the test structure needs to have a TLM configuration to allow back-bias ramp measurements to determine the back-gated pinch-off voltage as well as buffer leakage characteristics. The designed mask is illustrated in fig. 4.8, an optimal image of the processed sample is shown in fig. 4.6b in comparison to the previous sample mask using a circular TLM with an outer diameter of only 1100 µm. The sample consists of four large pixels that are separated by a mesa edge. In case that one pixel breaks down with a substrate-to-surface short, the sample still has other remaining pixels for experiments. The circular TLM structures share the outer contact to maximize the metallic area for grounding. The line of TLM structures is placed on the edge of the pixel to allow the AFM cantilever and KPFM detection system to come across the sample from the respective other side and sit above as much shielding metal as possible. The TLM gap size was varied to make the test structure more versatile, offer alternative gap sizes for back-biased KPFM measurements, and allow other systematic measurements.

4.3.2 Back bias supply optimization

Another method to reduce the apparent influence of the back bias field on the KPFM system observed in the first successful back-biased KPFM measurement (fig. 4.5) is shrinking the exposed biased parts. Therefore, the configuration was changed from the sample resting on large metal

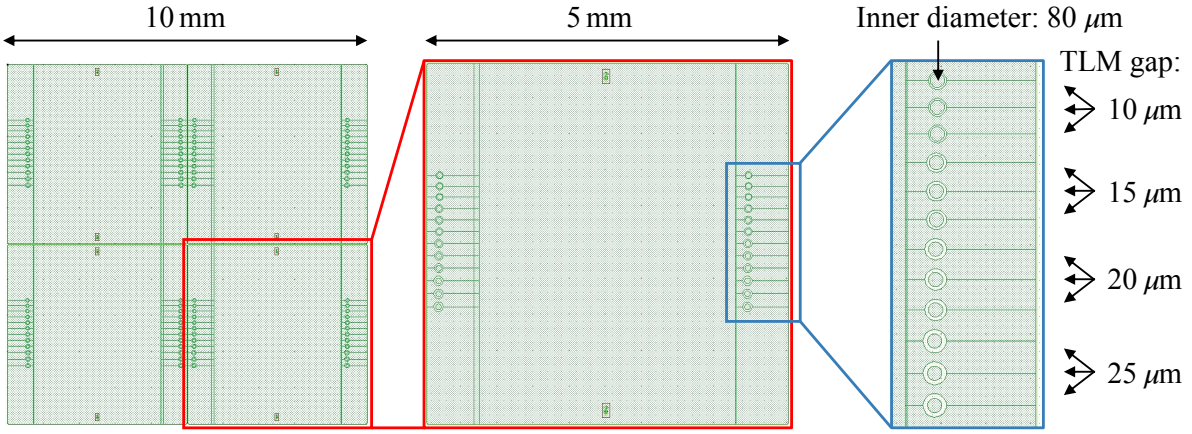

FIGURE 4.8. Customized circular TLM mask with four mesa edge-separated 5 mm × 5 mm squares and two lines of circular TLM structures, each consisting of triplets of circular TLMs with gap sizes of 10 µm (top), 15 µm, 20 µm, 25 µm (bottom) using an inner contact diameter of 80 µm.

plates multitudes wider in diameter than the sample width to the sample being directly electrically fixed to the insulation wafer. The back bias was directly provided to the sample substrate through a thin cable connecting from the side. This configuration reduces the biased area from a large metal plate to only the substrate area. This consequently reduces the exposed areas which create fringing fields. Fig. 4.9 shows an image of the setup. Thereby, the area of exposed back bias was decreased to a minimum reducing the electrical field exposure to the KPFM system. The image also schematically shows the placement of the KPFM probe reaching across the top metal that is grounded through the grounding probe coming from a shallow angle in order to leave space for the large KPFM probe holder.

4.4 Safety resistor and resistance calibration measurement

In the first back-biased KPFM measurement (fig. 4.4), the system seemed to cope with substrate voltages past the back-gated pinch-off voltage of the sample. However, at this point, the KPFM system should theoretically experience severe noise compromising any measurement. The reason for that is the safety series resistor which is needed to protect the AFM instrument from high currents caused by a catastrophic breakdown at high voltage. This resistor requires a resistance high enough to reduce the current below an acceptable limit in the event of a catastrophic sample short. Revisiting the substrate voltage ramp (fig. 4.3), it was found that the stack resistance of the sample varies depending on the substrate voltage due to a heavily substrate dependent vertical buffer leakage current. The vertical resistance of the sample is on the order of $1-10\,\mathrm{G\Omega}$. That range of stack resistance is in the same order of magnitude as the chosen safety resistor of $1\,\mathrm{G\Omega}$

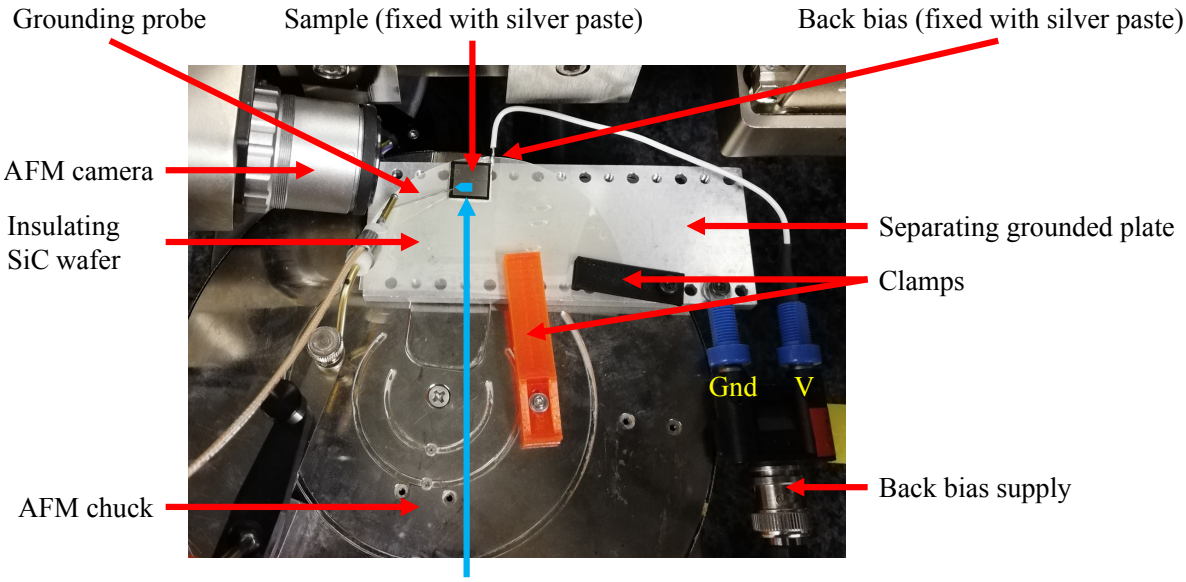

FIGURE 4.9. Optimized back bias supply setup for back-biased KPFM measurements. In this picture, the KPFM measurement system is removed from the AFM instrument but the KPFM probe is schematically shown at the measurement location.

that was inserted in series with the back bias supply to protect the AFM instrument. Evidently, a large proportion of the voltage applied to the substrate bias circuit is dropped across the safety resistance as opposed to the sample. Consequently, the resistance needs to be lowered compared to the vertical stack resistance to ensure the applied voltage drops across the sample instead of the safety resistor. However, this exposes the AFM instrument to higher risk. To optimize that tradeoff, it is necessary to measure the epitaxial stack resistance $R_{epitaxy}$ for each structure of the sample beforehand. The effectively applied back bias $V_{effective}$ can be calculated using

$$V_{effective} = \frac{V_{supplied}}{\frac{R_{safety}}{R_{epitaxy}} + 1} \tag{4.1}$$

with the supplied substrate voltage $V_{supplied}$ and safety resistance R_{safety}. Fig. 4.10 shows a measurement of the vertical epitaxial resistance and the effectively applied back bias for a set of series resistances. The higher the series resistance, the higher the deviation of the effectively applied back bias from the supplied back bias. This is particularly the case for high negative substrate voltages where the vertical epitaxial resistance is low. The setup was upgraded to include a switch to choose from a wide range of safety resistors ($10-100\,\mathrm{M\Omega}$ as shown in fig. 4.10) to adjust the back bias circuit in the optimal way for each sample. This ensures maximum protection of the AFM instrument while allowing the effectively applied back bias to reach voltages close to the sample pinch-off voltage.

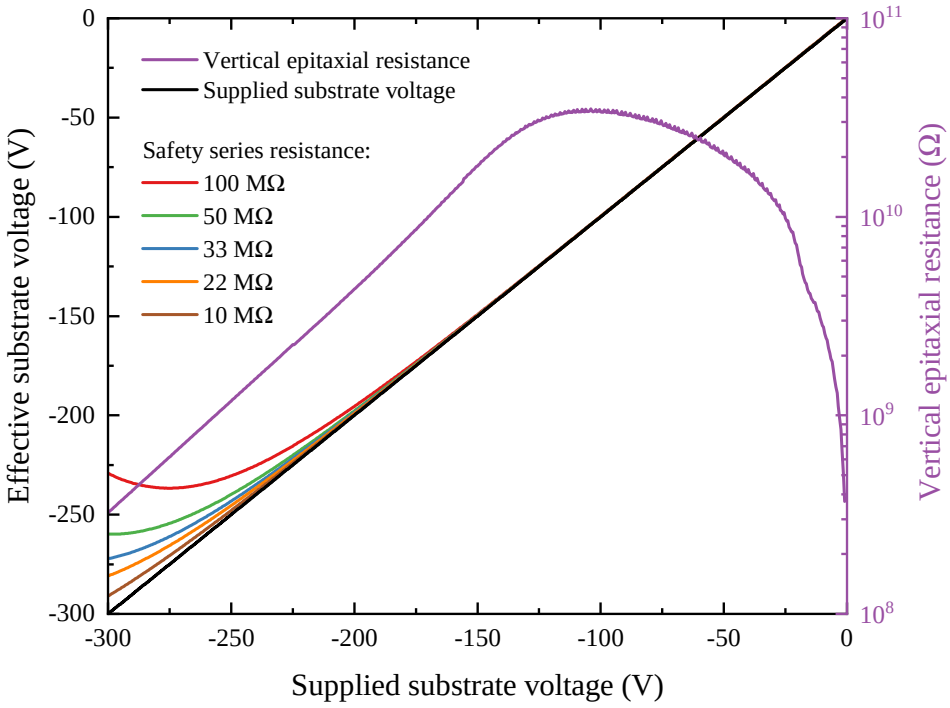

FIGURE 4.10. Calibration measurement and consideration of various safety resistors in series with the supplied substrate voltage.

4.5 CPD processing validation

The first back-biased KPFM measurement showed an increasing background CPD signal when lowering the substrate voltage. Therefore, to allow quantitative KPFM measurements, it is necessary to verify the polarity of the surface potential with respect to the CPD output signal of the AFM instrument. This evaluation was performed by scanning the CPD signal across two separated metal pads keeping one of them grounded and the other one biased at specific voltages. The ground was common with the AFM instrument. Fig. 4.11 shows the setup configuration as well as the measurement results. The plot shows the test result using the single-pass technique, however, the result was equivalent using lift-mode as cross-reference. The graphs show that the CPD is proportional to the applied bias on the metal pad. This confirms that the used AFM instrument outputs a CPD signal according to $V_{\mathrm{CPD}} = \left(\Phi_{\mathrm{sample}} - \Phi_{\mathrm{probe}}\right)/e$ where Φ and e are the work function and the elementary charge, respectively. This formula allows quantifying the surface potential from the measured CPD by measuring Φ_{probe} using a sample with a well-defined and known Φ_{sample} [177, 188, 189]. However, if scans are analyzed qualitatively or in comparison to one another, the conversion from CPD to surface potential is not necessary since surface potential and CPD are simply offset by a constant. In this case, only the sign between surface potential change and CPD change is relevant.

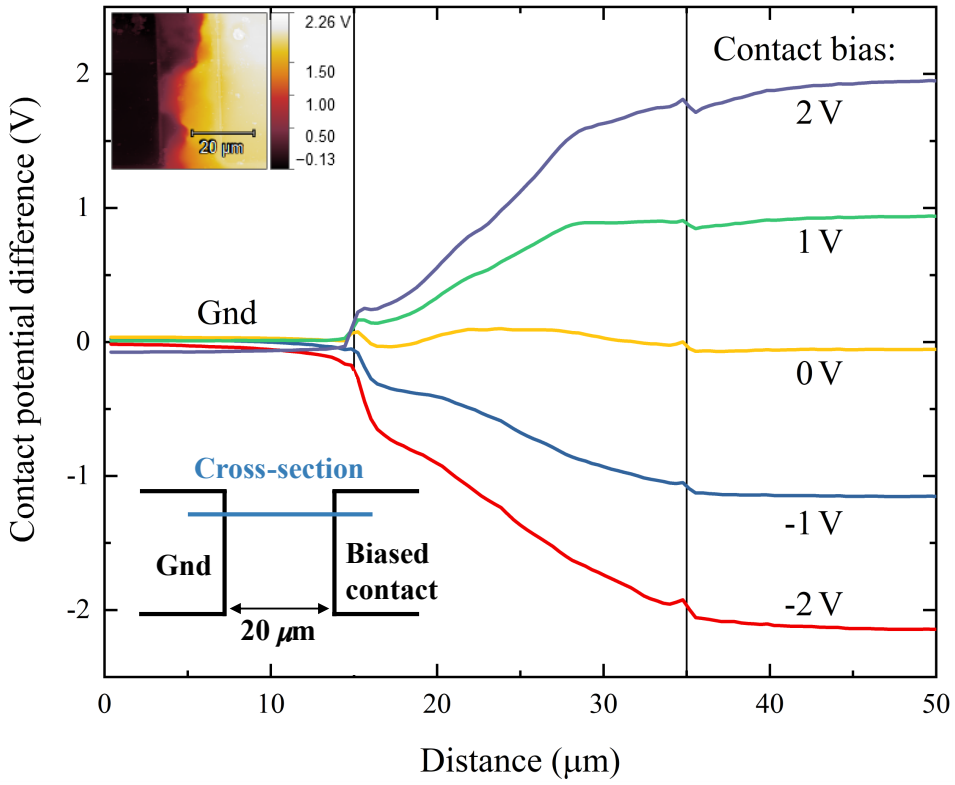

FIGURE 4.11. Polarity check of the CPD output using cross-sections from CPD measurements across a 20 μm junction with grounded and biased contact. The inset image shows the CPD scan for an applied bias of 2 V.

CHAPTER 5

VERTICAL ELECTRIC FIELD INHOMOGENEITIES ASSOCIATED WITH CONDUCTIVE DISLOCATIONS

A good understanding of dislocations as well as the associated electrical properties and leakage currents is important for device reliability. Breakdown is one of the key elements of GaN HEMT technology and its optimization. There are different suggested origins of device breakdown with many reports considering breakdown as a buffer bulk effect. However, another critical breakdown consideration is the role of conductive dislocations. This study uses the novel measurement technique introduced in the previous chapter 4 to show how conductive paths in the buffer can deform the electric field during substrate biasing, the equivalent of high drain bias stress in off-state. The approach combines two methodologies: KPFM and substrate voltage ramps. KPFM is a surface-sensitive technique that allows the mapping of the surface potential represented as contact potential difference (CPD) with respect to the probe work function [178]. Substrate bias ramps probe electrical buffer characteristics and yield information about vertical leakage and charge storage mechanisms in AlGaN/GaN HEMTs [89]. Combining both techniques allows imaging of the impact of the whole buffer leakage path on the 2DEG under operating conditions with sub-micrometer lateral resolution.

The samples used in this study were fabricated by the Department of Electronic and Electrical Engineering at the University of Sheffield (UK). Data shown in this section has been published in Applied Physics Letters [190]. Significant content has been reproduced from this publication.

5.1 Introduction

Despite vast efforts, GaN devices are still subject to inherent problems such as reversible and irreversible degradation processes, particularly when grown on Si leading to a high density of

defects which can create conductive paths as explained in section 2.2.2 [169, 191]. Reported densities of conductive dislocations, often correlated to device breakdown behavior, are in the range of $3-4\times10^{7}\,\mathrm{cm}^{-2}$ [85, 86, 97, 192, 193]. But correlating device leakage characteristics and breakdown values to the dislocation density is not that straightforward as bulk leakage also depends on other parameters such as carbon (C) doping. The density of conductive dislocations is typically measured by conductive AFM. However, conductive AFM measurements are often flawed since a leakage spot at the surface does not necessarily mean an underlying vertically conductive dislocation through the entire buffer because of the shunting effect of the 2DEG [194]. Furthermore, it is not understood how a single and potentially partially conductive dislocation of different current–voltage (*IV*) characteristics contributes to the overall breakdown of the device [195]. Consequently, neither measuring buffer leakage nor investigating dislocation density or conductivity of various types is sufficient to analyze and model device breakdown. Nonetheless, leakage along threading dislocations is also known to facilitate efficient discharging of the buffer following trapping under stressed conditions, especially when C-doped buffer layers are involved. The charge neutralization vastly benefits dynamic device performance following switching from off-state to on-state [89, 196–198]. Ultimately, there is a tradeoff between sufficient dislocation-originated leakage to achieve good dynamic device performance and a low density of conductive dislocations to ensure reduced high field leakage impacting breakdown [199].

5.2 Sample and measurement configuration

The sample wafer was grown using metal organic chemical vapor deposition (MOCVD) and consists of about 2.5 µm graded (Al,Ga)N buffer on a Si substrate, followed by 500 nm C-doped GaN, an unintentionally doped (UID) 250 nm thick GaN channel, a 25 nm thick AlGaN barrier with 25 % Al composition as well as a 2 nm GaN cap. The sample was processed with Ti/Al/Ni/Au ohmic contacts alloyed at 800 °C in a nitrogen atmosphere with Ti/Au top metal layer using circular transfer length method (TLM) structures with a shared outer ohmic contact. The TLM gap spacing used here was 20 µm. The channel resistance was around 600 Ω/sq. The circular TLMs allow measurement of the 2DEG conductivity as a function of negative substrate (back gate) bias, while the absence of passivation allows simultaneous access to the GaN surface. This allows KPFM measurements in the TLM gap, as well as visualization of atomic steps and surface dislocation pits using AFM (fig. 5.1). The area of the outer ohmic contact, electrically grounded, was deliberately as large as possible, extending to 5 mm × 5 mm to reduce KPFM noise as explained in section 4.3.1. The source contact was grounded in order to ground the 2DEG to replicate the vertical field conditions (magnitude and sign) that were used during substrate voltage sweeps. It also reproduces the regular positive drain bias conditions during operation mode.

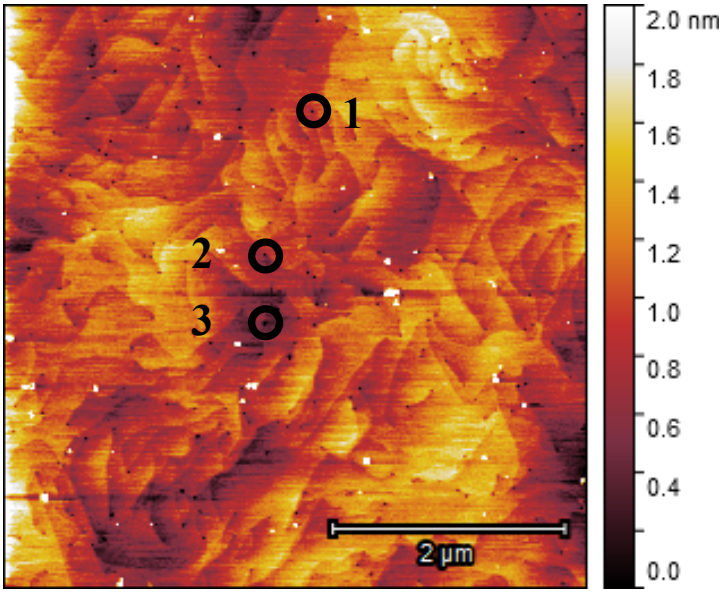

FIGURE 5.1. Post-processing AFM topography scan of the GaN surface. The marked dislocations are spots that are analyzed in terms of CPD values in fig. 5.3.

5.3 Substrate bias ramp

For the substrate ramps, the channel conductivity was measured by applying a small bias of 1 V between the two ohmic contacts on the top of the AlGaN/GaN-on-Si stack while a bidirectional negative voltage sweep was applied to the Si substrate (fig. 5.2a). The 2DEG concentration determines the channel conductivity and can therefore be used as a sensor of the electric field directly underneath the 2DEG. Different buffer transport mechanisms are probed depending on the maximum sweep voltage and resulting current hysteresis loop. If the buffer behaves as an insulator and the leakage in the entire buffer is smaller than the displacement current, the channel is capacitively coupled to the substrate. The result is a linear relation between normalized channel current and substrate voltage. This typically remains the case for small substrate voltages. However, when the back bias is further increased, charge redistribution within the buffer occurs. Depending on which layer starts to conduct, charge can either be redistributed within that layer to form a dipole, or alternatively, charge can flow from the contacts. Either case causes charge accumulation in depletion regions or at blocking interfaces [89]. This charging behavior leads to a deviation from pure capacitive behavior and its linear relationship. Fig. 5.2a shows a rather typical substrate ramp characteristic for a good quality epitaxy. Positive charge storage occurs when sweeping to −100 V that gets neutralized again on the return sweep when reaching 0 V. When sweeping to −300 V, a deviation occurs in the opposite direction correlated to small negative charge storage that remains present when the bias is removed [200].

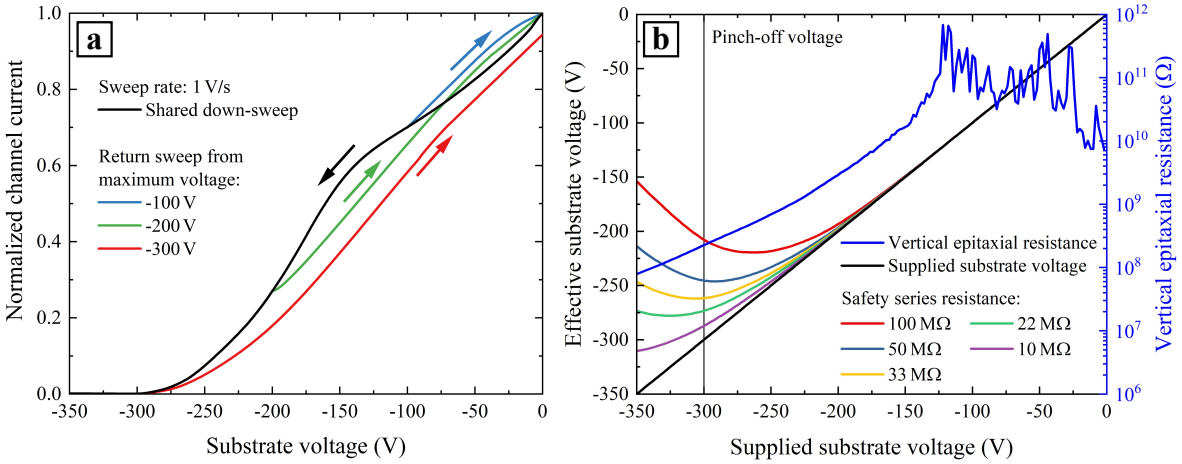

FIGURE 5.2. a) Substrate ramp of the investigated sample with a shared downward sweep and return sweeps from different maximum voltages. The sweep rate was $1\,\mathrm{V\,s^{-1}}$. b) Vertical epitaxial resistance and the corresponding effective substrate voltage based on different safety resistors placed in series with the substrate voltage supply.

The substrate voltage sweep simultaneously measures the substrate current representing the vertical epitaxial leakage current. That defines the stack resistance in relation to the safety resistor that is needed for back-biased KPFM measurements as shown in fig. 5.2b. The vertical epitaxial resistance is above the detection limit of about $10^5\,\mathrm{M\Omega}$ until a back bias of $-125\,\mathrm{V}$. When decreasing the substrate voltage more, the stack resistance decreases exponentially to about $100\,\mathrm{M\Omega}$ at $-350\,\mathrm{V}$. Based on that dynamic resistance change, the effective substrate voltage for the back-biased KPFM measurement with the safety resistance in series can be calculated. Fig. 5.2b shows the effective substrate voltage for a set of available safety resistors ranging from $10\,\mathrm{M\Omega}$ to $100\,\mathrm{M\Omega}$. The necessity for a safety resistor is explained in section 4.4. For a small safety resistance and at substrate voltages close to back-gated pinch-off, the vast majority of the supplied substrate voltage is dropped across the sample. This makes the effective substrate voltage closely follow the supplied substrate voltage. For larger and larger safety resistances, a greater and greater portion of supplied substrate voltage is dropped across the resistor instead of the sample. This leads to the effective substrate voltage deviating more and more from the supplied substrate voltage. While this is disadvantageous in terms of effective substrate voltage, it is beneficial to protect the AFM instrument in case of a catastrophic sample breakdown and short-circuit. As a compromise, for this sample, a safety resistance of $33\,\mathrm{M\Omega}$ was chosen for the back-biased KPFM measurements.

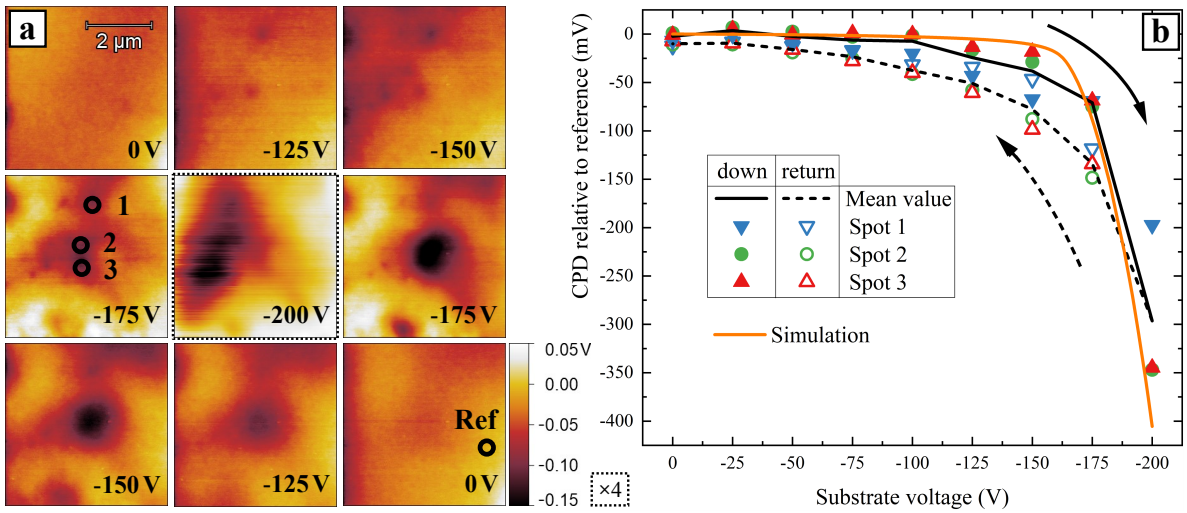

FIGURE 5.3. a) Selection of contact potential difference (CPD) scans with substrate voltages down to −200 V and the return sequence to no substrate bias in voltage steps of 25 V from top left to bottom right. Note the quadruple scale at −200 V. The reference spot was placed far away from apparent CPD features. b) Quantitative analysis of spots 1, 2, and 3 relative to the reference values for each scan for the downward and return sweep of substrate voltage as well as the simulated sweep. Values of CPD for the analyzed spots were averaged over a radius of 100 nm.

5.4 Back-biased KPFM measurements

KPFM scanning was performed in the dual-pass (lift-mode) amplitude-modulated (AM) KPFM mode combined with tapping mode topography scanning [188, 201, 202]. The lift height for the reverse scan was 20 nm. Fig. 5.3a shows a sequence from CPD measurements taken in substrate voltage increments of 25 V down to −200 V. The measurement was analyzed in terms of CPD relative to the work function of the KPFM probe instead of converting to the actual surface potential by not determining the work function of the probe. The background signal could not be fully eliminated preventing quantitative analyses. The analysis here is therefore done relative to a reference spot instead. This analysis still accurately represents the surface potential since the values of surface potential are just offset by the probe work function which remained the same throughout the sequence of measurements. For each voltage step, the sample was given 2 min to stabilize at the new bias conditions before measuring the CPD. Down to a substrate bias of −100 V, the CPD was rather uniform with no obvious features. Beyond this voltage, spots appeared with lower CPD becoming more pronounced and increasing in size, with more spots appearing the more negative the voltage. Approaching a substrate voltage of −200 V equal to two-thirds of the pinch-off voltage (fig. 5.2a), the spots increased to a size of up to 1 µm in diameter. At a substrate voltage of −200 V, the signal-to-noise ratio for the CDP signal increased

substantially. The maximum sweep voltage was also limited by the large series resistor (33 MΩ) in the back bias supply required to prevent damage to the KPFM instrument in the event of sample breakdown. When stepping the substrate bias back towards 0 V, the trend was reversed showing some latency. The features gradually disappeared, however, a center spot—likely a superposition of several CDP features—remained weakly present at 0 V (fig. 5.3a). In fig. 5.3b, the CPD is analyzed for the three marked spots in fig. 5.1 and fig. 5.3a. The potential is referenced to a spot far away from any dislocation feature to account for a potential drift associated with fringing fields coupling the substrate voltage to the AFM scanning unit. Aligned with the CPD images, the CPD spot analysis is initially substrate bias independent, but beyond a substrate bias of −100 V, the CPD starts to decrease gradually followed by a rapid drop at −200 V. The reverse line validates the observed latency with lower CPD compared to the downward sweep for any substrate voltage indicating a hysteresis behavior for the back-biased KPFM measurement similar to regular substrate bias ramps in fig. 5.2a.

This back-biased KPFM measurement is reproducible as well. Several other sister samples from the same wafer were fabricated alongside the main sample investigated here. All samples showed the observed effect to a certain degree at different sample locations, however, sometimes not as clear as in fig. 5.3. Several of those sequences of similar back-biased KPFM measurements are shown in the appendix B.

5.5 Conductive AFM measurements

Conductive AFM, as explained in section 3.5.5, was measured with a grounded probe and a substrate voltage down to −200 V using highly doped diamond probes (Nanosensors CDT-NCHR) with a high spring constant to ensure high contact force and thus good electrical contact between probe and sample. Fig. 5.4 shows conductive AFM measurements at different substrate voltages under the same conditions that were used for the CPD measurements with a grounded 2DEG and the large series safety resistor present. A bias applied to the substrate does not reveal any leakage paths reaching the surface for both small (fig. 5.4a) and large (fig. 5.4b) substrate voltages. This result was quite unexpected compared to published literature [85, 86, 97, 192, 193]. Therefore, to validate the conductive AFM result, the sample was sent to an expert in the field and the author of several publications showing such distinctive conductive AFM measurements [159, 192, 194, 195]. Fig. 5.4c shows this external comparison measurement taken under the same conditions using the same kind of conductive AFM probes. Also, this measurement does not reveal any pronounced leakage spots similar to fig. 5.4b. Therefore, this cross-reference measurement validates the unexpected results of no apparent leakage spots reaching the surface.

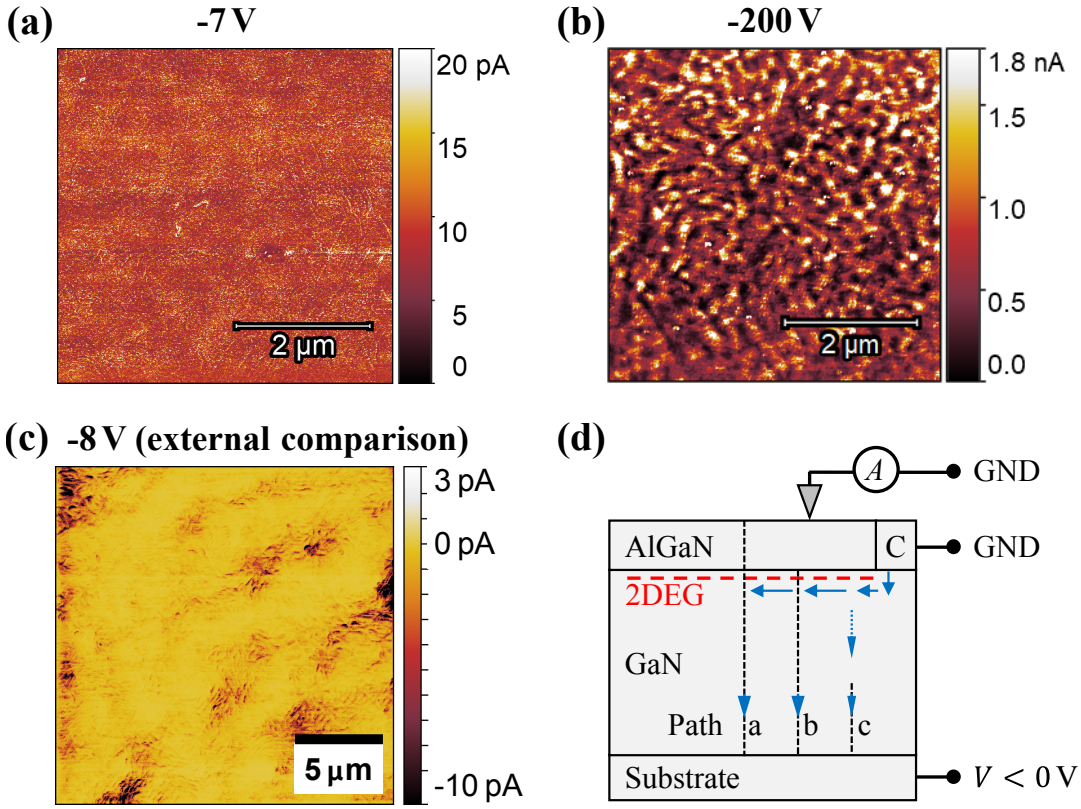

FIGURE 5.4. Conductive AFM images with a) the small substrate voltage of −7 V and b) a high substrate voltage of −200 V. c) Conductive AFM image of the same sample measured externally under similar conditions by the author of [159, 192, 194, 195] using a substrate voltage of −8 V. d) Schematic of the conductive AFM measurement with different types of leakage paths.

5.6 Experimental and model discussion

All CPD spots that appear for high negative substrate voltages (fig. 5.3a) can clearly be correlated to the location of a screw dislocation in the topography image (fig. 5.1). Threading edge dislocations typically form small depressions whereas threading screw dislocations lead to larger depressions [96]. The density of the observed features showing a significantly lower surface potential (fig. 5.3a) is about $4 \times 10^7\,\mathrm{cm}^{-2}$ which is consistent with reported densities of $3-4 \times 10^7\,\mathrm{cm}^{-2}$ for conductive dislocations [85, 86, 97, 192–195]. Interestingly, the conductive AFM measurements under the same conditions as the CPD measurements, particularly having the 2DEG grounded (fig. 5.4a and fig. 5.4b), did not show apparent leakage paths reaching the surface while applying up to −200 V to the substrate. Instead, the conductive AFM image shows certain patterns that are potentially correlated to the topography and caused by smaller and larger contact area between probe and surface, especially at large back bias. The conductive AFM result was quite unexpected since previous publications of conductive AFM using lower biases revealed local leakage spots

reaching the surface with currents that are orders of magnitude greater than the background current [86, 97, 159, 192–195, 203–206]. However, those studies were likely all conducted with a floating 2DEG. Many reports do not explicitly specify but the publications do not contain device measurements which would require wafer processing and contact fabrication. It can therefore be assumed that the focus of those studies was purely on material properties such as leakage path density and IV characteristics using unprocessed as-grown GaN wafers without a grounded 2DEG. Therefore, for the measurements in those publications, the full applied voltage is allowed to drop across the top barrier layer. The conductive AFM measurement reported here suggests that the presence of the grounded 2DEG clamps the dislocation potential and connects any electrically conductive dislocations in the buffer to ground, similar to the suggestion in some previous reports [192, 194]. This situation is schematically shown in fig. 5.4d highlighting the possible leakage paths. The latency between down-sweep and return-sweep observed in fig. 5.3b indicates a charging effect associated with the threading screw dislocation. This effect may represent a previously unreported localized mechanism for dynamic on-resistance R_{ON}.

The observed change in CPD in the 2DEG can be explained using a model that considers the electrostatics as schematically shown in fig. 5.5. At a location of pristine GaN buffer far away from the dislocation, the potential is dropped linearly and vertically between substrate and 2DEG along R_{Buffer} establishing an electric field E_{Buffer} in an ideal case where charge trapping or accumulation is excluded. On the contrary, with a conductive path along the core of the dislocation to the 2DEG, the potential distribution is strongly dependent on the specific conduction characteristics of the dislocation. A smaller resistivity along the dislocation ($R_{Conductive\ path} < R_{Buffer}$) extending partway through the buffer results in a more negative potential at the top of the conductive path relative to the surrounding buffer. Consequently, the conductive dislocation has effectively electrically 'thinned' the buffer at the location of the conductive path. The electrical thinning causes a more concentrated electric field ($E_{Above\ conductive\ path} > E_{Buffer}$) from the top of the conductive path across the gap (R_{Gap}) to the 2DEG leading to a localized depletion in the 2DEG region ($R_{Depletion}$). The local 2DEG depletion causes a reduced potential at the surface across the barrier ($R_{Barrier}$) at the location of the conductive path ($V_{Above\ conductive\ path} < V_{Above\ buffer}$) which was observed in the back-biased KPFM measurements. It is a reasonable assumption that this effect remains even when the conductive dislocation ends deep in the buffer for a sufficiently conductive dislocation. Moreover, it can be expected that the magnitude of the effect is directly proportional to the conductivity of the path, i.e. inversely proportional to the path resistivity ($\propto R^{-1}_{Conductive\ path}$), and inversely proportional to the depth where the conductive path ends beneath the 2DEG ($\propto d^{-1}$). Previous reports showed that the conductivity of dislocations can be modified by wafer processing [207]. Furthermore, it has also been observed that processing can change the conductivity partway through the buffer, although in that case, it was a conductivity increase in the upper part of the stack [208]. The mechanism is speculative but may be associated with decoration or the removal of decoration of the dislocation core with contaminants such as

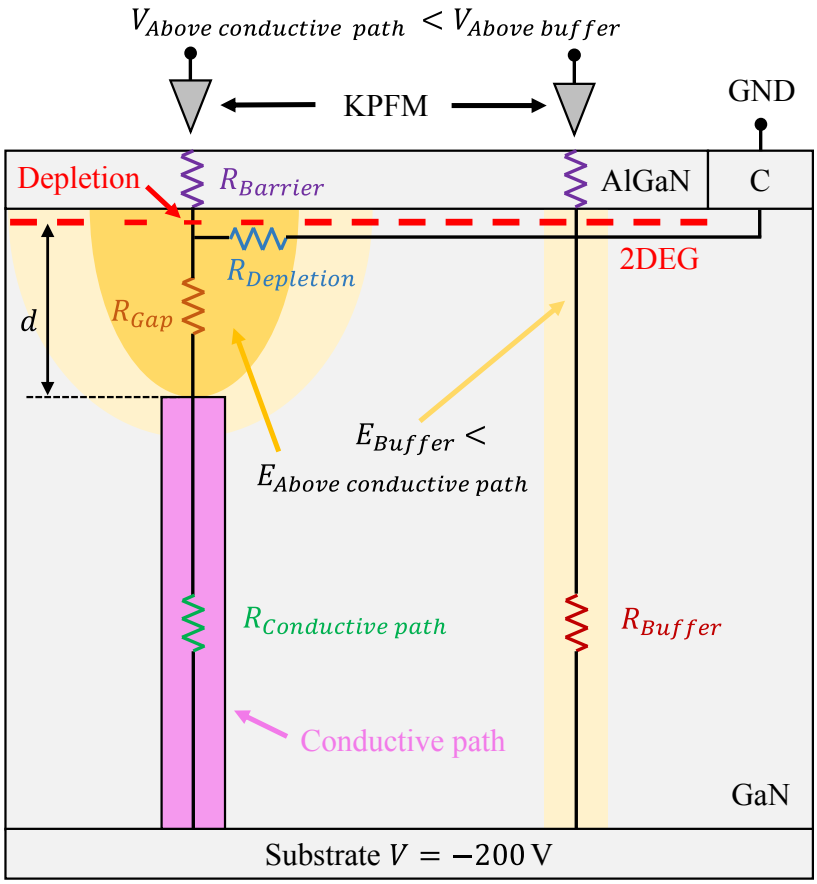

FIGURE 5.5. Schematic of the electrostatics around a conductive path as opposed to a pristine buffer with KPFM measurement on the surface and higher electric field in the gap between conductive path and 2DEG.

hydrogen that happened during processing. While the proposed model explains the observed data from the back-biased KPFM measurement, further validation is required to show the origin of the effect. That also includes the consideration of alternative explanations.

The observed CPD features under high back bias conditions leading to deformation at off-state stress have implications for vertical leakage and device breakdown. The higher the conductivity of the lower part of the dislocation, the greater is the electric field below the 2DEG around the dislocation core. The measurements also suggest that breakdown can potentially be a highly localized phenomenon that is driven by a non-uniform potential distribution through the buffer. The extent of the effect becomes particularly apparent from the large local depletion regions in the 2DEG, indicated by surface potential features with a diameter in the micrometer range (fig. 5.3a). The indicated local potential deformation increases the electric field in the top GaN buffer layers, especially the channel, compared to the bulk of the buffer. Instead of dropping the voltage uniformly across the buffer from substrate to 2DEG, the channel gets locally exposed to a higher level of stress. Therefore, vertical leakage and device breakdown can not simply be

modelled as a bulk effect of the epitaxy but may well be caused by a small number of highly enough conductive dislocations. The back-biased KPFM measurement in fig. 5.3a particularly suggests that threading dislocations where the conductivity does not fully extend from the buffer to the surface still cause substantial potential deformations at off-state stress. This kind of dislocation and its breakdown behavior has not been directly observed before and has only been derived from indirect capacitance measurements [208]. Consequently, dislocation-induced breakdown may well be more complicated than only considering apparent and conventionally measurable conductive dislocations.

5.7 Simulations

The observed CPD effect was simulated using the drift–diffusion TCAD tool Silvaco ATLAS. The structure is based on the known dimensions for channel and total device thicknesses. The GaN cap has been neglected since its purpose is optimizing dynamic HEMT performance which is not applicable in this measurement [209]. The energy levels for shallow donors and carbon (C) occupying the N site (C_N) were chosen as 0.03 eV below the conduction band and 0.9 eV above the valence band, respectively [114, 210], as explained in section 2.2.3. The buffer was simplified as one single layer of C-doped GaN with compensating donor and C_N acceptor densities of $5 \times 10^{18}\,\mathrm{cm}^{-3}$ and $1 \times 10^{19}\,\mathrm{cm}^{-3}$, respectively. The channel was doped with $1 \times 10^{16}\,\mathrm{cm}^{-3}$ of donors and $2 \times 10^{16}\,\mathrm{cm}^{-3}$ of C_N acceptors. As shown in fig. 5.6, the situation has been modelled using a cylindrical symmetry surrounding the conductive dislocation. The conductive path was located at the edge of the 2D simulation structure mimicking the radial confinement. The AFM probe was placed as a floating contact 20 nm above the 25 nm thick AlGaN barrier with the gap filled by air. The ohmic contact to the 2DEG was placed 20 µm away from the AFM probe.

Modelling the dislocation conductivity is challenging because different conduction properties have been experimentally observed. Previous experimental reports measured *IV* curves of conductive dislocations showing super-exponentially increasing current along the dislocation when exceeding a few volts applied as forward bias [99] or reverse bias [86], however, the onset voltage showed a large variation between the samples. The conduction mechanism along dislocations is likely one-dimensional nearest neighbor hopping conduction, however, this is difficult to reproduce in the simulator [200]. There is a lot of speculation about dislocation-related trap states with some experimental reports attributing the conductivity to donors [211, 212], with trap levels ranging around 1 eV below the conduction band [213–217]. Others assigned it to acceptor states, with a wide energy range of $0.9 - 1.6$ eV above the valence band [86, 218]. For simulations, it has been previously shown that using localized acceptor traps can sufficiently approximate the measured electrical properties of dislocations [216, 219]. Here, an approach with p-type doping for the dislocation was used where deep acceptors were placed 0.6 eV above the valence band corresponding to the maximum hopping energy on a 1D hopping path to approximate the dislocation

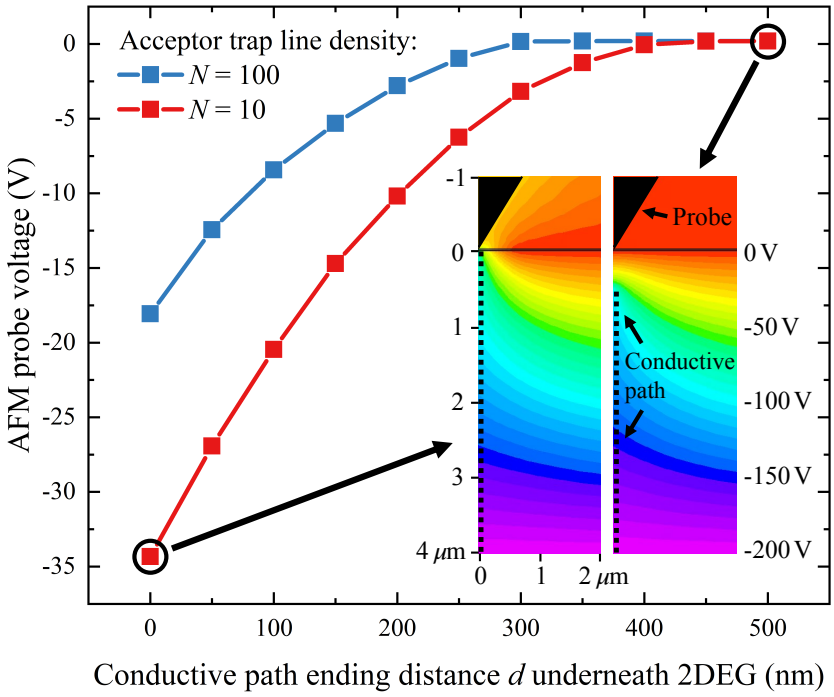

FIGURE 5.6. Simulated AFM probe voltage for partially extending conductive paths ending distance d beneath the 2DEG for different conductivities represented as acceptor trap line density (continuous density as if every N^{th} atom along dislocation was a trap) at a substrate voltage of −200 V. The inset shows a cross-sectional view of the simulated potential for two conductive path lengths (left: full vertical extension; right: conductive path ending $d = 500$ nm underneath the 2DEG).

conductivity by using band edge hole conduction. The acceptor traps were 50 % compensated by shallow donors placed 0.2 eV below the conduction band which makes the dislocation core p-type. The doping polarity was found to have an important effect which is more discussed below. The trap concentration for the conductive path was implemented with a parameter relative to the atomic lattice density. The conductivity parameter N represents a path where every N^{th} atom along the conductive path is a trap, but of course, the simulator interprets the dislocation trap concentration as a continuous and homogeneous trap density.

Typical device simulations consider a 2D device cross-section that extends infinitely in perpendicular direction. Therefore, including a conductive vertical line in a regular 2D simulation would actually represent a 'dislocation sheet' instead of a dislocation line path with its radial confinement. Due to the cylindrical symmetry of the problem, the simulations were first attempted using radial 3D simulations with the vertical leakage path at the center, however, this configuration prevented the simulator from converging when sweeping the substrate voltage. Likewise, the simulator failed when using a 3D cuboid structure with a cuboid-shaped leakage path surrounded by a cuboid-shaped buffer. As 3D simulations seemed impossible, the structure was compromised

using a 2D simulation placing the leakage path at one edge of the cross-sectional view to represent the cylindrical symmetry, as shown in fig. 5.6. The conductive path was modelled as vertical doped region with a radius of 2 nm at the origin directly below the AFM probe. To account for the cylindrical representation in an orthogonal computation, the trap concentration was adjusted by a factor of $\frac{\pi}{4}$.

Given the dynamic nature of the back-biased KPFM measurement gradually stepping the substrate voltage down about every 25 min (stabilizing time plus measurement time), the simulation was set up in a dynamic manner as well. However, simulating the experiment time scale of about 8 h total covering the entire downward and return sweep was practically impossible as the simulator required small time steps to ensure convergence. For practical reasons, the simulation focused on the down-sweep using a substrate voltage ramp rate of $10\,\mathrm{V\,s^{-1}}$.

The simulated model results in a depletion region around the dislocation core which extends into the 2DEG. This is an ideal reverse-biased junction which can result in a significant proportion of the applied bias being dropped across the junction from the 2DEG to the dislocation top. Here, two of many possibilities for the electrical behavior of the structure are investigated. Particularly, the impact of varying dislocation conductivity and the possibility of suppression of conduction in the upper part of the epitaxy on the AFM probe potential is considered. Fig. 5.6 shows the simulation of the AFM probe voltage depending how far the conductive path extends within the buffer from substrate towards surface ending distance d below the 2DEG. This is undertaken for different line charge densities within the dislocations, representing each N^{th} atom along the conductive path being an acceptor trap, at a substrate voltage of $-200\,\mathrm{V}$. The data shows that the AFM probe voltage drops significantly, even when the conductive path stops within the buffer. The closer the conductive path reaches the 2DEG, the more pronounced is the observed effect. The dislocation hopping site density also plays an important role in the magnitude of the effect. Increasing N, which reduces the dislocation doping and conductivity, leads to a smaller surface potential disturbance. The inset of fig. 5.6 shows two cross-sectional views of the potential around the conductive path. Far away from the dislocation, the potential is dropped linearly and vertically between 2DEG and substrate. However, in and around the dislocation core as well as the 2DEG, the distribution of potential is strongly dependent on the specific characteristics of the conductive dislocation. This leads to a reduced potential at the surface at the dislocation and to a local depletion of the 2DEG around the dislocation core. This effect persists even when the conductive path ends hundreds of nanometers underneath the 2DEG.

When fitting the simulation and experiment, the two parameters N and d can be tuned. Fig. 5.7 shows the simulation of the AFM probe voltage for a substrate ramp when changing those two parameters. For a fixed d, increasing N lowers the magnitude of the AFM probe voltage drop with decreasing substrate voltage (fig. 5.7a). Therefore, the magnitude of the voltage drop depends on the dislocation doping and therefore conductivity. The higher the density of hopping sites (lower N), the higher is the disturbance in the potential field and the higher is

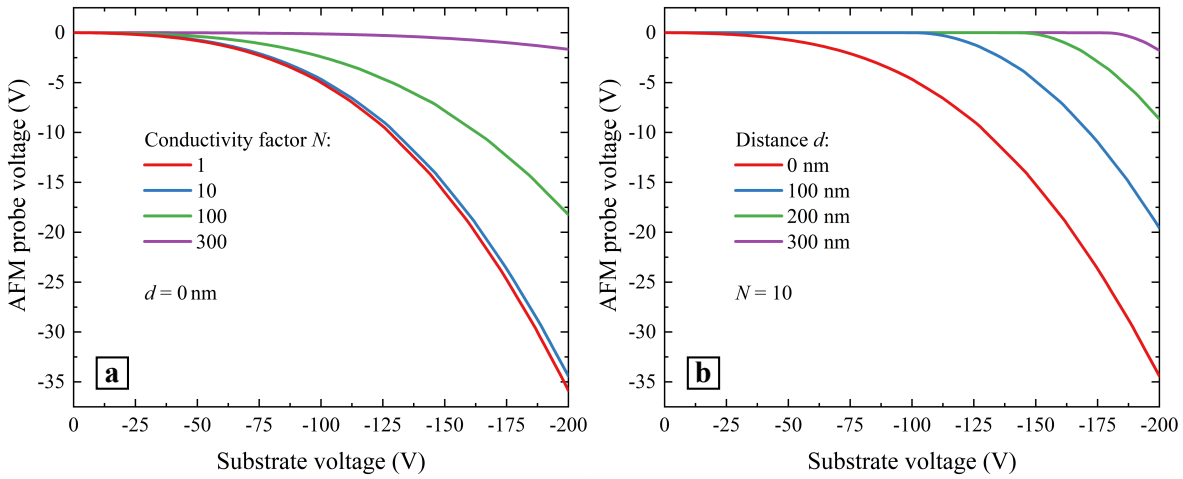

FIGURE 5.7. Simulated AFM probe voltage for substrate voltage ramps for a) different conductivities represented as acceptor trap line density (continuous density as if every N^{th} atom along dislocation was a trap) and b) with partially extending conductive paths ending distance d beneath the 2DEG.

the drop in surface potential. For a fixed N, increasing d shifts the onset of the AFM probe voltage drop to lower substrate voltages while simultaneously lowering the magnitude of the effect (fig. 5.7b). For the measured back-biased KPFM sequence a good fit was achieved for a dislocation conductivity factor $N = 300$ and the dislocation ending $d = 50\,\text{nm}$ underneath the 2DEG. The AFM probe response upon sweeping the substrate voltage to negative biases with those parameters is included in fig. 5.3b. Similar to the experiment, the simulated AFM probe voltage remains unaffected for low substrate voltages when the 2DEG is still present at the dislocation location. It requires a higher negative substrate voltage to start depleting the 2DEG leading to the drop in surface potential sensed by the AFM probe. At high negative substrate voltage, the AFM probe voltage in the simulation starts to drop sharply, resembling the drop observed in the experimental data (fig. 5.3b).

While the simulation model qualitatively shows the surface potential drop observed in the back-biased KPFM measurement, it has to be considered a rough approximation. The main reason is the lower acceptor trap level inside the dislocation core compared to the buffer in combination with the p-type dislocation doping. This, by default, generates a depletion region around the dislocation core from substrate to 2DEG. The magnitude and spacial extension are small enough to not be detectable by the AFM probe across the barrier and gap at this stage with no back bias applied. However, this effectively manifests a 2DEG depletion region as well as buffer potential deformation around the dislocation into the default bias conditions at 0 V substrate voltage. When sweeping the substrate bias to lower voltages, this 2DEG depletion region widens alongside the more pronounced buffer potential deformation creating the observed

effect. However, this means that the final simulation result has effectively been triggered by the choice of the initial parameters. To tackle the inconsistency, it was attempted to invert the dislocation doping ensuring an n-type dislocation core, however, potential continuity issues in the simulations prevented this. It was impossible to make the simulator electrically connect the dislocation to the substrate in order to bias the bottom of the dislocation at the substrate voltage. Instead, the simulator always formed a depletion region between substrate and dislocation creating a large potential discontinuity which made accurate dislocation biasing impossible, irrespective of the simulation setup. Nevertheless, despite the inconsistency in the particular initial choice of doping using a p-type dislocation, the simulation validated the widening of the 2DEG depletion region for lower substrate voltages indicating a greater buffer potential deformation around the dislocation core. It also confirmed the trend of a lower surface potential above the conductive dislocation, the higher the dislocation conductivity and the further the conductive path extends through the buffer.

5.8 Conclusion

The measurements and experimental discussion demonstrated the complexity of dislocation-induced breakdown. The back-biased KPFM measurements show inhomogeneities of the 2DEG at negative substrate voltages that are comparable to high off-state device stress. At low and moderate substrate bias, there are no apparent features in the surface potential scan. However, beyond a certain threshold, localized drops in surface potential start to appear. The more negative the substrate voltage, the more surface potential features appear reaching up to 1 µm in diameter indicating local areas of depletion regions in the 2DEG. This effect relates to a significant potential deformation and a highly non-uniform electric field distribution through the buffer which stresses the upper GaN layers, especially the channel, instead of the buffer. The measurement suggests that breakdown is not a bulk effect but can be a highly localized phenomenon. The measurement can be explained considering threading dislocations that are only partway conductive through the epitaxial stack. The simulations qualitatively showed the buffer potential deformation around the dislocation core. The simulation also validated the trend of a more pronounced effect, the closer the conductive path reaches the 2DEG, and the higher the dislocation conductivity.

CHAPTER 6

DOPING MEASUREMENT VIA UV-INDUCED PERSISTENT INCREASE IN CHANNEL CONDUCTIVITY

For stable device operation, it is crucial to have a clear knowledge of how the device acts in different environments. GaN HEMTs often demonstrate an UV-induced increase in channel conductivity known as persistent photoconductivity (PPC). The PPC effect is generic and exists for a wide range of HEMT configurations irrespective of the nominal buffer doping type and magnitude or the substrate material. Fig. 6.1 shows a histogram of the measured magnitude of the PPC effect for 24 wafers covering the entire range of RF and power device GaN HEMT structures. The PPC effect was measured on unprocessed wafers using a resistivity meter based on non-contact eddy-currents in an industrial context following UV exposure from either conventional fluorescent tube light or background daylight. Evidently, there is no 'typical' value for the PPC effect with magnitudes ranging from as low as 1 % all the way to values as high as 13 %. Given the widespread magnitude of the UV-induced PPC effect, a clear understanding of the effect is necessary.

The chapter presents a detailed model for the transport of photogenerated charges in GaN HEMTs, and their effect on the electronic band bending. It is demonstrated that absorption of UV light in the bulk and band bending is sufficient to explain the magnitude of PPC increase in channel conductivity for the investigated samples. This magnitude is found to be directly related to the net doping density directly below the 2D electron gas (2DEG) meaning that the PPC effect can be used to determine the difference in buffer concentration between acceptors and donors. This parameter is very difficult to measure by any other technique to date since dopants are deep and they result in a semi-insulating material below the 2DEG. Hence, conventional capacitance–voltage profiling cannot normally access the doping density. Moreover, the density of intrinsic donors and the site location of extrinsic dopants like carbon (C) is challenging to

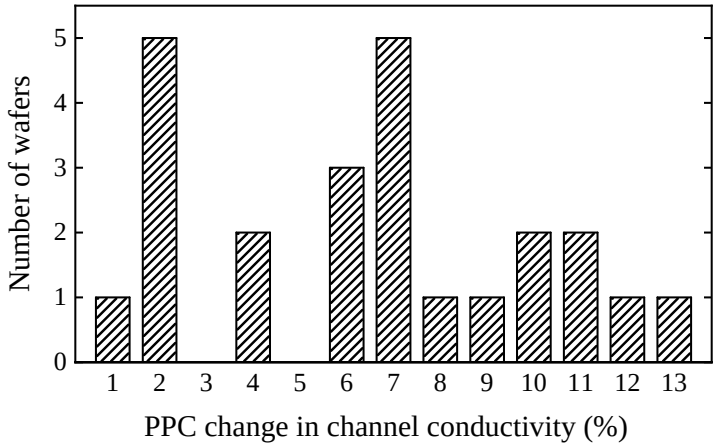

FIGURE 6.1. Histogram of the UV-induced PPC effect for a large set of various samples with both carbon doped and iron doped buffers grown on both Si and SiC substrates. Note the wide spread of the PPC magnitude. Data provided by IQE PLC.

determine by techniques such as secondary ion mass spectrometry (SIMS). These can only provide the density of certain atoms but it cannot yield any site information. Detailed knowledge of the net doping density is important for device engineering as it influences the density of free carriers and hence the bulk GaN resistivity and the leakage behavior of devices [89, 104, 208]. It also affects the two-dimensional potential distribution in the device which ultimately defines the peak magnitude in electric field [220].

The samples used in this study were provided by the IQE PLC. Data shown in this section has been published in Applied Physics Letters [221]. Significant content has been reproduced from this publication.

6.1 Introduction

GaN HEMTs have the advantage of a high breakdown voltage and a high electron mobility [196]. Nevertheless, devices still possess reversible and irreversible degradation processes that require further analysis to be fully understood [84]. Several research groups reported that UV light illumination of AlGaN/GaN HEMTs affects the carrier trapping during pulsed operation [222] as well as initiates low-frequency drain current noise [223]. Besides, UV light substantially increases the channel conductivity indicated by an increased drain current known as persistent photoconductivity (PPC) [224]. The magnitude of the PPC effect increases logarithmically with optical power densities around $10^{-4}\,\mathrm{W\,cm^{-2}}$ with a subsequent tendency to saturate at higher illumination densities [224]. This effect predominantly occurs for photon energies greater than the GaN band gap [224–227]. The PPC effect has been studied before. Various reports analyzed the PPC effect qualitatively and explained it by considering dopants or traps that capture and release charge carriers in the GaN buffer and/or the AlGaN barrier under UV light exposure

[224–226, 228–231]. Other reports suggested the hypothesis of an UV-induced change in the charge status of surface states [228–230]. Heating the sample reduces the PPC effect due to the acceleration of carrier capture and release rates [232, 233]. The PPC effect is a generic phenomenon that exists for many different sample configurations. It also appears with a wide range of observed magnitudes (fig. 6.1). However, the PPC effect magnitude has not been explained quantitatively. Moreover, it has also not been exploited to date to determine critical material or device parameters.

6.2 Sample configuration

The studied sample set consisted of four GaN wafers covering a range of typically used epitaxial variants. The samples were grown using metal organic chemical vapor deposition (MOCVD). Wafers A and B had an iron (Fe) doped GaN buffer and were grown on insulating SiC substrates. Wafers C and D had a C-doped GaN buffer and were grown on p-type Si substrates. All samples had a top AlGaN barrier generating a 2DEG. The Si substrates were electrically isolated from the bulk GaN by the AlN nucleation layer followed by AlGaN strain relief layers. Transfer length method (TLM) structures with 20 µm gap were fabricated by mesa etching and using Au-based ohmic contacts. The key parameter which differentiates the set of wafers is the C doping distribution, incorporated either purposefully or as an unintentional but inevitable consequence of MOCVD growth. Wafers A and B incorporated the same Fe doping profile in the buffer and had a similar 200 nm thick unintentionally doped (UID) GaN region below the 2DEG with C density of $5 \times 10^{16}\,\mathrm{cm}^{-2}$. But both wafers had different background C density in the bulk of the GaN of $3 \times 10^{17}\,\mathrm{cm}^{-2}$ and $2 \times 10^{16}\,\mathrm{cm}^{-2}$, respectively [210]. Wafers C and D had a 300 nm and a 390 nm thick UID GaN layer, respectively, with a C density of $3 \times 10^{16}\,\mathrm{cm}^{-2}$. Both wafers had a buffer C doping of about $1 \times 10^{19}\,\mathrm{cm}^{-2}$.

6.3 Measured PPC effect magnitude and recovery

The wafers were illuminated with UV light with a wavelength of 360 nm (3.44 eV) with a photon energy greater than the GaN band gap. The light source was a xenon light source (Spectral Products ASB-XE-175) combined with a monochromator (Spectral Products CM110). The illumination power was $10^{-4}\,\mathrm{W\,cm}^{-2}$ which resembles a typical intensity for laboratory lighting around 360 nm making this effect relevant to many measuring environments. The samples were kept in the dark for 30 d before the device measurement. The PPC effect upon UV illumination typically occurs quite rapidly in a matter of seconds, however, to ensure equilibrium, the samples were kept exposed to UV light for 5 min. The channel conductivity was measured using a four-wire resistance configuration as explained in section 3.2.3 and a 20 µm TLM structure. All wafers showed an increase in channel conductivity covering a range from 5.9 % (wafer B) to 7.5 % (wafer A), shown in table 6.1. The transient recovery in darkness following UV exposure was measured

TABLE 6.1. Measured and simulated increase in channel conductivity induced by UV light with a wavelength of 360 nm and illumination power of $10^{-4}\,\mathrm{W\,cm^{-2}}$.

	Wafer A	**Wafer B (p-type)**[a]	**Wafer B (n-type)**[a]	**Wafer C**	**Wafer D**
Measurement	$(7.5 \pm 1.8)\,\%$	$(5.9 \pm 1.5)\,\%$		$(7.1 \pm 0.6)\,\%$	$(6.5 \pm 0.9)\,\%$
Simulation	8.0 %	6.5 %	1.7 %	6.8 %	6.7 %

[a] Buffer C doping for simulation

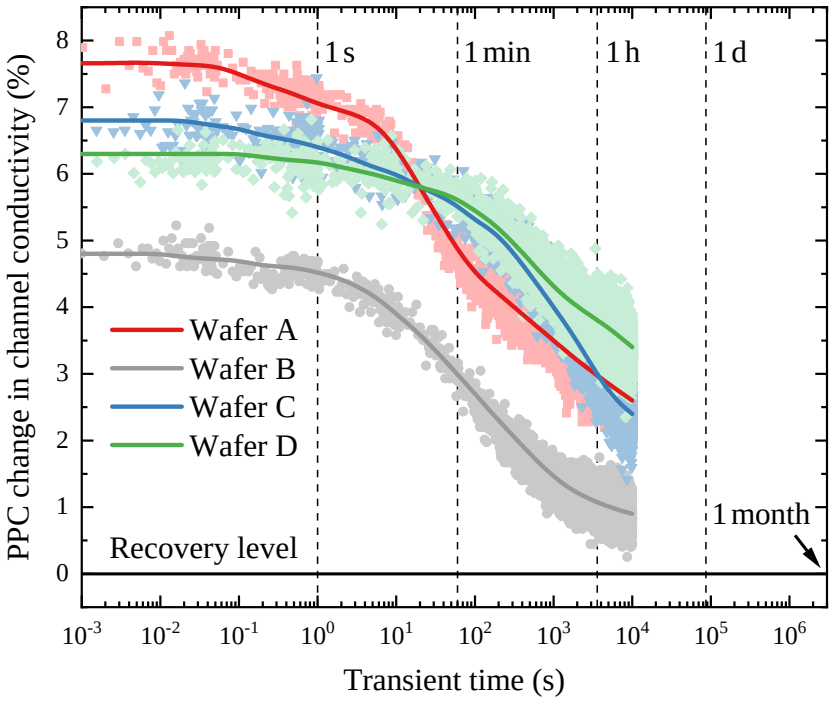

FIGURE 6.2. Time transient of the change of channel conductivity following UV illumination normalized with the conductivity measured in dark. The solid lines are trend line fits as guidance to the eye.

as explained in section 3.3 and is shown in fig. 6.2. The channel conductivity was normalized to the initial measured value in darkness. All recovery transients share a common trend. As temporal response, the conductivity exhibits a small decline over a period of seconds followed by a steeper decrease over subsequent minutes (wafers A and B) or hours (wafers C and D). No full recovery was achieved within the measurement time frame. As hinted by the measured transients (fig. 6.2), full recovery may take up to one month indicating a further slow time constant.

TABLE 6.2. Doping profiles used in the simulation for the studied wafers with acceptors (N_A) and donors (N_D) in units of cm^{-2}. The profiles for wafers A and B are based on the SIMS profile for C and Fe in a publication [210], with two options for the compensation ratio for wafer B. The doping profiles for wafers C and D are based on SIMS measurements.

		Wafer A	**Wafer B (p-type)**	**Wafer B (n-type)**	**Wafer C**	**Wafer D**
UID GaN	$N_A - N_D$ (C donors plus intrinsic donors)	3×10^{16}			2×10^{16}	
	Thickness	200 nm			300 nm	390 nm
Buffer	$N_A - N_D$ (C)	10^{17}	10^{16}	-10^{16}	8×10^{18}	
	Compensation ratio N_D/N_A (C)	0.5	0.33	1.67	0.5	
N_A (Fe)		10^{15} at 2DEG exponentially increasing with depth to 3×10^{18} at 1.1 µm			none	
Substrate		Insulating SiC			p-type Si	

6.4 Simulation configuration

The PPC effect was simulated in 2D with Silvaco ATLAS drift–diffusion software to understand the increase in channel conductivity induced by illuminating the GaN HEMTs with UV light. The simulation used TLM structure with a 3 µm gap and uniform UV illumination from the top. An optical absorption coefficient for GaN of 9×10^4 cm^{-1} was used [234]. The doping profiles for acceptors (N_A) and donors (N_D) for the simulation were consistent with the measured SIMS profiles. All essential simulation configuration parameters are shown in table 6.2. The Fe acceptor level was chosen as 0.7 eV below the conduction band. The energy level for the C acceptor and C donor (including intrinsic donors) level corresponding to C occupying the N and Ga site, respectively, were considered as 0.9 eV above the valence band and 0.03 eV below the conduction band, respectively [114], as explained in section 2.2.3. The bulk GaN of wafers A, C, and D can be assumed p-type given the high C concentration in the buffer. The Fermi level in the buffer can be expected to be pinned close to the C_N acceptor level. On the other hand, the bulk C doping of wafer B was so low that it is possible that there were sufficient intrinsic or extrinsic (C_{Ga}) donors to overcompensate the C_N acceptors. This scenario leads to rendering the buffer of wafer B n-type. Therefore, all buffers were assumed to be p-type, however, for wafer B, two different compensation ratios N_D/N_A were considered, representing a p-type and an n-type buffer. To facilitate hole leakage from the 2DEG through the UID GaN layer to the buffer, leakage

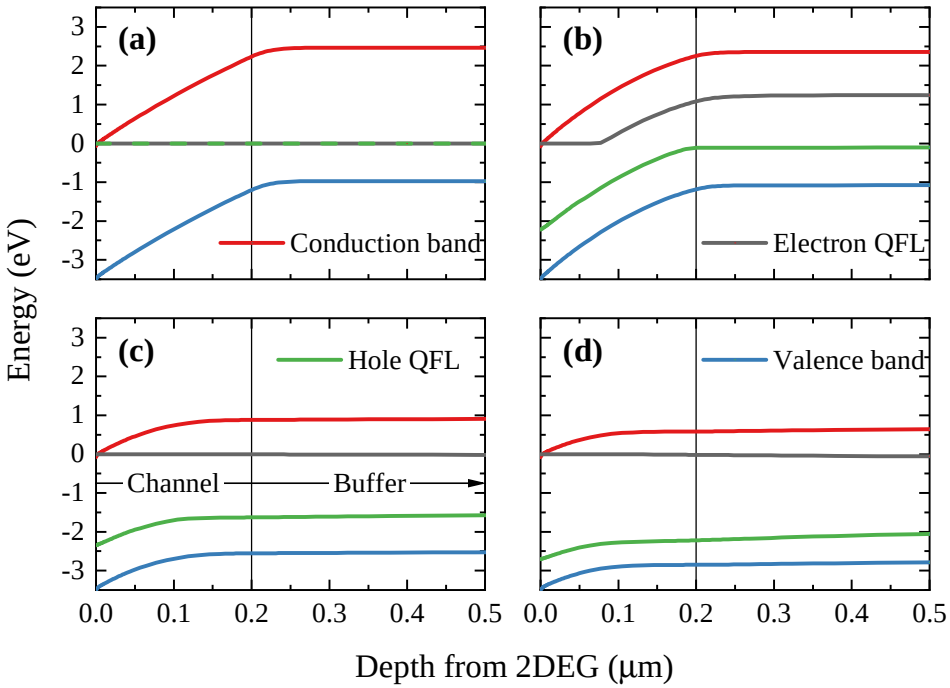

FIGURE 6.3. Cross-section of the band diagram of wafer A with conduction band and valence band as well as electron and hole quasi-Fermi level (QFL) for a) the initial solution in darkness, b) $10^{-12}\,\mathrm{W\,cm^{-2}}$, c) $10^{-10}\,\mathrm{W\,cm^{-2}}$, and d) $10^{-4}\,\mathrm{W\,cm^{-2}}$ of static UV illumination.

paths were simulated using heavily p-doped vertical lines below the 1 µm wide contacts on either outer edge of the TLM structure terminating at the C-doped region. This approach considers reverse bias leakage along threading dislocations by means of a trap-assisted band-to-band hopping process [216, 235]. Substrate voltage sweeps demonstrated that this leakage path can already occur at very low fields [200]. To improve convergence of the simulator, no doping was incorporated for 5 nm below the AlGaN/GaN interface. In the simulation, the magnitude of the UV-induced PPC effect was measured by applying 10 mV across the TLM gap and monitoring the current.

6.5 Model and PPC effect magnitude

The UV-induced response can be explained by considering the band diagram and charge carrier concentrations. Here, the wafer A doping profile was used as an example shown in fig. 6.3 and fig. 6.4. Initially in darkness, the Fermi level is pinned by the lowest partially occupied acceptor level in the band gap. In this case, it is the C_N level 0.9 eV above the valence band which bends the bands up towards the buffer (fig. 6.3a). The initial buffer hole concentration is defined by the

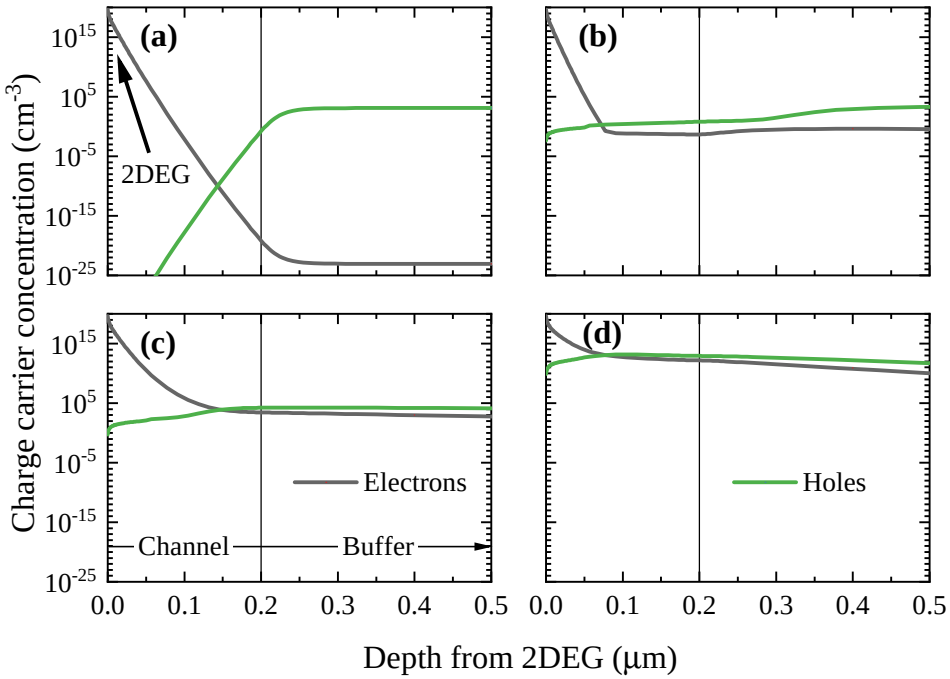

FIGURE 6.4. Cross-section of the charge carrier concentration in wafer A for a) the initial solution in darkness, b) $10^{-12}\,\mathrm{W\,cm^{-2}}$, c) $10^{-10}\,\mathrm{W\,cm^{-2}}$, and d) $10^{-4}\,\mathrm{W\,cm^{-2}}$ of static UV illumination.

compensation ratio, more specifically by N_D/N_A at the Fermi level pinning acceptor level [236]. On the other hand, the initial electron density in the buffer is insignificant (fig. 6.4a).

When the device structure is illuminated with UV light with a photon energy greater than the GaN band gap but below the AlGaN band gap, photons are being absorbed in the GaN buffer creating electron–hole pairs. The charge generation causes a split in Fermi level to separate quasi-Fermi levels (QFL) for electrons and holes. Increasing the illumination power raises the electron concentration in the buffer (fig. 6.4b). Consequently, the electron QFL moves closer to the conduction band (fig. 6.3b). At this stage, the hole concentration in the buffer remains largely unaffected. The PPC effect induces an inbuilt potential that drives the photogenerated holes via a band-to-band leakage process, primarily provided by dislocations, to the 2DEG or the contacts. The hole QFL remains fixed at zero energy due to this leakage path of the buffer to the contacts.

The total leakage path resistivity is comprised of lateral leakage within the GaN layer to the dislocation followed by vertical leakage along the dislocation to the contact. Increasing the illumination power more and more increases the generation of electron and holes in the buffer. At a certain illumination power, the generation of holes exceeds the leakage capabilities of the total leakage path from buffer to contact. The rate of photogenerated holes is higher than the buffer hole discharge rate by the leakage paths leading to an accumulation of holes in the buffer. At this stage, all bands bend down resulting in a near-flat electron QFL again (fig. 6.3c) and an increase

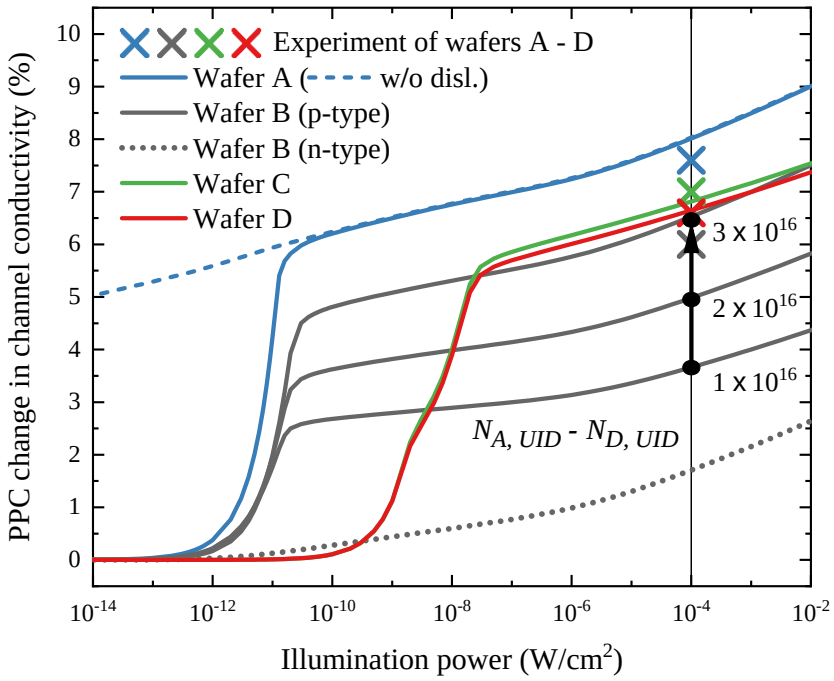

FIGURE 6.5. Simulated static normalized 2DEG conductivity for increasing UV illumination power. The buffer doping is p-type except for Wafer B showing the n-type case (dotted) as well. The dashed line for wafer A represents the case without p++ shorting dislocations to the buffer below the contacts. The arrow represents increasing $N_{A,\,UID} - N_{D,\,UID}$ for wafer B (p-type) in units of cm^{-2}. The vertical line symbolizes the experimentally used illumination power of $10^{-4}\,\mathrm{W\,cm}^{-2}$.

in channel conductivity occurs. The electron buffer concentration has become comparable to the initially set hole concentration in the buffer (fig. 6.4c). During this process, the electron QFL went from being initially pinned in the lower half of the band gap (fig. 6.3a) to being shifted to the upper half (fig. 6.3c). From this stage, increasing the illumination power even more leads to an increase of both concentrations for electrons and holes (fig. 6.4d). This development pushes the electronic bands closer to a flat band configuration (fig. 6.3d) while simultaneously increasing the electron concentration in the 2DEG.

Fig. 6.5 shows the PPC effect magnitude for the simulations as a function of illumination power. There is no effect with increasing illumination power until about 10^{-12} to $10^{-10}\,\mathrm{W\,cm}^{-2}$. For higher illumination intensities, the PPC response increases by a steep increase followed by a gradual logarithmic increase. As shown in table 6.1, there is good agreement between the experimental results and the simulated values for the PPC effect at $10^{-4}\,\mathrm{W\,cm}^{-2}$ using the simulation parameters (table 6.2). Simulation and experiment only achieve a good fit for one specific value of $N_A - N_D$. As illustrated for Wafer B in fig. 6.5, there is also a high sensitivity of the PPC effect for small changes in $N_{A,\,UID} - N_{D,\,UID}$ in the UID GaN layer. The simulation for Wafer B particularly shows that it has a p-type buffer given the underestimation of the simulated

increase in channel conductivity compared to the experimental result for an n-type buffer. This also demonstrates that the PPC effect is stronger for p-type buffers. As a final consequence, the net doping concentration $N_A - N_D$ can be determined by measuring the UV-induced change in channel conductivity and using simulations to correlate experimental value with simulation input parameters.

The TCAD model demonstrates the difference in magnitude of the PPC effect from wafer to wafer and its high sensitivity on the net deep-level doping density $N_A - N_D$. To phenomenologically understand the high dependency of the PPC effect on $N_A - N_D$, the system can be considered as a parallel-plate capacitor established by the depletion region with the 2DEG as one plate and the buffer as opposite plate. The parallel-plate capacitor charge Q is given by

$$Q = C\,V = \frac{\epsilon\,A}{d}\,V \tag{6.1}$$

with capacitance C, dielectric permittivity ϵ, capacitor plate area A and separation d, as well as capacitor voltage V. Considering the equation, the 2DEG concentration (i.e. capacitor charge) can be increased in two ways: increasing the capacitance by reducing the plate separation via an increase in net doping $N_A - N_D$, or increasing the capacitor voltage by a higher change in band bending. Initially without UV exposure, the Fermi level is pinned at the same C_N acceptor energy level for all wafers, thus, at roughly flat bands at $10^{-4}\,\mathrm{W\,cm^{-2}}$ of UV illumination, the change of band bending is the same. Using the capacitor analogy, the same degree of band bending relates to an equal capacitor voltage for all samples. Hence, only the channel–buffer capacitance, particularly the depletion region width, defines the magnitude of the effect. The depletion width underneath the 2DEG is determined by the concentration difference between acceptors and donors ($N_{A,\,UID} - N_{D,\,UID}$) in the UID GaN layer. Potentially, the concentration difference between buffer acceptors and donors ($N_{A,\,Buffer} - N_{D,\,Buffer}$) can also play a role for wider depletion regions that do not end within the UID GaN. For wafers A and B, the UID GaN layer is narrow and was therefore fully depleted. Therefore, $N_{A,\,Buffer} - N_{D,\,Buffer}$ defines how far the depletion region reaches into the buffer. The greater $N_{A,\,Buffer} - N_{D,\,Buffer}$ for wafer A relates to a narrower depletion region, in return leading to a greater channel–buffer capacitance. As a consequence, the PPC effect for wafer A is greater than for wafer B. For larger UID GaN widths, as it is the case for wafers C and D, the depletion region is expected to end within the UID GaN layer. Therefore, the thickness of UID GaN layer is not relevant in defining the depletion region width and ultimately the magnitude of the PPC effect. This can be experimentally observed for wafers C and D as their PPC effect magnitudes only differ marginally despite the different UID layer thicknesses. Nevertheless, the small difference still means that the depletion region in wafer D extends less within the UID GaN layer width than in wafer C.

Threading dislocations and the leakage paths associated with them are important for the UV-induced PPC effect. The role was investigated in the simulation by disabling the dislocations, as shown for wafer A in fig. 6.5. In this case, the steep increase in channel current around about 10^{-12} to $10^{-10}\,\mathrm{W\,cm^{-2}}$ is eliminated. Instead, the channel current gradually increases starting

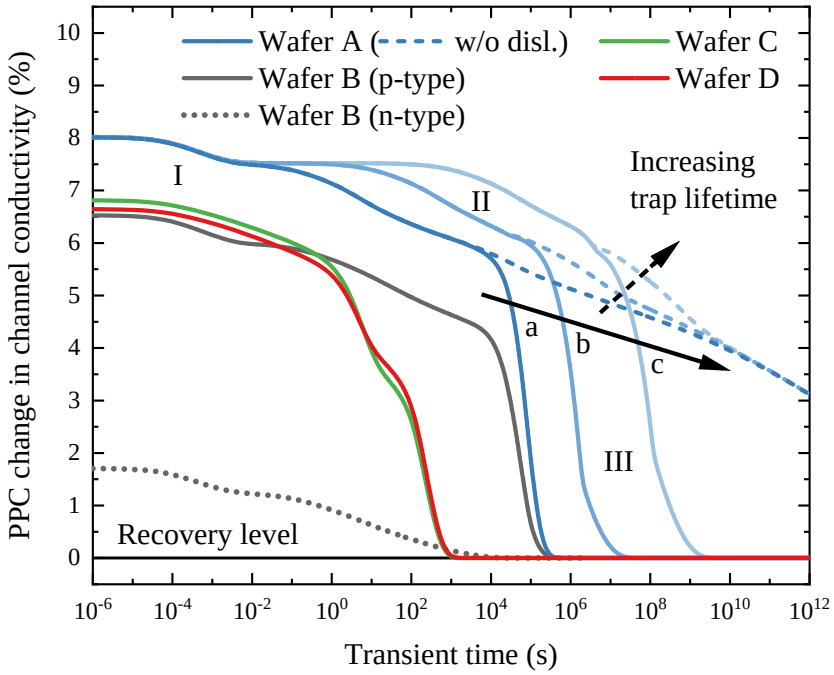

FIGURE 6.6. Simulated transient recovery following UV illumination normalized by the initial channel current in darkness, for wafer A, B, C, and D. Dashed lines represent the recovery without dislocation-related p++ shorting leakage paths to the buffer underneath the contacts for wafer A. It also demonstrates several different transients for wafer A with increasing trap lifetime realized by consecutively decreasing the trap capture cross-section for each step by two orders of magnitude (a: $10^{-15}\,\mathrm{cm}^2$, b: $10^{-17}\,\mathrm{cm}^2$, c: $10^{-19}\,\mathrm{cm}^2$). Three key processes labelled I, II, and III can be identified.

at a low illumination power of $\ll 10^{-20}\,\mathrm{W\,cm}^{-2}$ until it merges with the graph with enabled dislocations leakage paths. Hence, the absence of a hole leakage path from the buffer to the contacts results in a logarithmic dependence of band bending on illumination power. In this case, the hole QFL in the buffer does not remain pinned to the ground level as in fig. 6.3b. Instead, the electron QFL stays pinned to the ground level for the entire illumination power sweep causing a gradual band bending process.

6.6 Simulated transient recovery

To gain insight into the experimentally observed logarithmic recovery of the PPC effect demonstrated in fig. 6.2, the transient recoveries were simulated and are shown in fig. 6.6. The transients exhibit multiple time constants. Similar to the experimental result, an initial slight decline (I) is followed by a gradual decrease (II) and ultimately a drop (III) as a function of time. At the beginning of the transient, the structure has a higher buffer electron (n_e) and hole (n_h) concentration

(fig. 6.4d) than the initial buffer hole concentration $n_h^{initial}$ in darkness (fig. 6.4a). Consequently, the electron–hole recombination rate can be expected to be proportional to both buffer n_e and n_h ($\mathrm{d}n_e/\mathrm{d}t \propto n_e\, n_h \approx n_e^2$) until n_h has decreased to the level of $n_h^{initial}$ according to Shockley–Read–Hall recombination statistics [237, 238]. Based on this assumption, n_e decays by a multiplicative inverse function ($n_e \propto t^{-1}$). This process is related to the first small decrease occurring on a milliseconds timescale (I in fig. 6.6). This is consistent with the observed rapid fall in the first few seconds of the experimental transient in fig. 6.2. This recombination process can only be expected if the structure has been illuminated with a high enough UV power to increase the buffer n_e above $n_h^{initial}$. The longer period recovery in form of a gradual decline (II in fig. 6.6) is dependent on the recombination process as well. Here, two different paths are simulated for wafer A: electron–hole recombination and leakage along dislocations. In the absence of dislocations, it can be observed that the timescale shift in logarithmic recovery is dependent on trap lifetime (a, b, and c in fig. 6.6) leading to a long gradual decline on the order of minutes to hours (II in fig. 6.6). In the presence of dislocations, i.e. when there is a leakage path from the 2DEG to the buffer, holes flow out of the buffer through the dislocations to the contacts. The current is related to an *RC* effect discharging the channel–buffer capacitor. The rate of the process can be expected to be proportional to n_e ($\mathrm{d}n_e/\mathrm{d}t \propto n_e$) which leads to an exponential decay ($n_e \propto \exp[-\mathrm{const}\ t]$) as seen in the simulation (III in fig. 6.6). Both mechanisms could contribute to the experimentally observed drop in PPC over a few minutes to hours followed by the very slow recovery (fig. 6.2). However, as evident by the comparison of experimental and simulated recovery for wafers C and D, the model has limitations to capture all processes that occur in a device.

6.7 Conclusions

The UV-induced increase and transient recovery of the channel conductivity were measured and simulated for a set of different samples, however, industrial data on a larger sample set illustrates that the PPC effect occurs on a wide range of different sample configurations showing a wide range of measured magnitudes of the PPC effect. For the studied samples, the PPC effect can be fully attributed to a shift in the electronic band diagram and capacitive coupling of the 2DEG and buffer represented by the depletion charge without consideration of a change in surface charge. The transient recovery shows long time constants, experimentally pointing towards one month until full recovery, which can be explained by a combination of direct electron–hole recombination and dislocation-assisted leakage. The greater the difference between acceptor and donor density, i.e. the net doping density $N_A - N_D$, the greater is the PPC magnitude. The magnitude of the effect is very sensitive to small changes in $N_A - N_D$, especially in the UID GaN region ($N_{A,\,UID} - N_{D,\,UID}$). Ultimately, this means that the UV-induced PPC effect can be used to probe the net deep-level doping density $N_A - N_D$.

CHAPTER 7

SURFACE-RELATED PERSISTENT PHOTOCONDUCTIVITY BY UV LIGHT ILLUMINATION

As the previous chapter 6 showed for the investigated samples, the persistent photoconductivity (PPC) effect induced by UV light illumination can be fully explained by considering the shift in the electronic band structure in the buffer. However, many previous publications speculate about a surface contribution to the PPC via different processes. Device passivation may play an important role in the UV-induced PPC effect as well.

For this chapter, a specific set of samples with different channel C doping levels, channel thicknesses, and sample passivation was fabricated. The samples were provided by IQE PLC. Comparing the experimental PPC effect magnitude to the simulated expected magnitude based on the buffer-induced PPC effect aims to separate off the surface-related PPC effect.

7.1 Introduction

Illuminating AlGaN/GaN HEMTs with light causes different effects with various device performance implications. Light illumination with absorption in the bulk with different wavelengths can accelerate the recovery from current collapse [239]. Continuous optical pumping of deep traps during device operation can minimize influences of dynamic on-resistance and allows better power HEMT performance [240]. Blue light radiation can also mitigate the kink effect in the DC characteristics due to facilitated trapping and detrapping phenomena [231]. Illuminating with wavelengths greater than the GaN band gap allows for direct absorption triggering other effects. UV light can increase the channel current noise level [223]. UV illumination also increases the channel conductivity [224]. For photon energies not allowing absorption in the AlGaN barrier, absorption in the buffer and field-induced charge separation with electrons drifting to the 2DEG

TABLE 7.1. Sample configuration with the key parameters of C doping and layer thicknesses. Doping concentrations were measured using SIMS. Doping is given in units of cm^{-3}, thicknesses are given in units of nm.

	Sample 1	**Sample 2**	**Sample 3**	**Sample 4**	**Sample 5**
UID C doping	$\mathbf{7 \times 10^{15}}$	$\mathbf{2 \times 10^{16}}$	$\mathbf{4 \times 10^{16}}$	6×10^{16}	7×10^{15}
UID thickness	200	200	200	200	**400**
Buffer C doping	3×10^{18}	3×10^{18}	3×10^{18}	3×10^{18}	2.5×10^{18}
Buffer thickness	400	400	400	400	200
Passivation	no	no	no	**yes**	no

has been considered qualitatively [226, 228, 230]. In fact, for some samples, absorption and charge accumulation in the buffer can fully quantitatively explain the PPC effect [221]. As shown in chapter 6, charge carrier generation in the buffer causes bending of the electronic bands leading to an increase in electron concentration in the 2DEG due to capacitive coupling across the doping-related depletion region between channel and buffer. Other studies consider surface states with changing charge status [224, 228–230]. Passivation can alter the magnitude of the PPC effect as it reduces the surface trap density [241]. However, the interplay and ratio between buffer-related and surface-related effects have not been investigated in detail yet.

7.2 Sample configuration

The samples for this study were specifically designed to probe three different dimensions of the UV-induced PPC effect: Net doping density $N_A - N_D$ (difference between acceptor concentration N_A and donor concentration N_D), unintentionally doped (UID) layer thickness, and passivation. While the first two factors were key learnings from the study in chapter 6, the last factor covering the effect of device encapsulation aims to probe potential surface-related effects due to surface instabilities of the dielectric. Table 7.1 shows the sample configurations with samples 1 to 3 increasing in carbon (C) doping in the UID layer in order to probe $N_A - N_D$. As sample 3 was expected to yield the greatest PPC magnitude, this sample configuration was chosen to study the impact of surface passivation. However, the corresponding passivated sample 4 exhibited a somewhat higher C doping than targeted during growth. To probe the UID layer thickness dependence, the doping configuration of sample 1 was chosen since the lowest UID C doping relates to the widest extension of the depletion region. The corresponding sample 5 has a doubled UID layer thickness. The substrate was Si followed by an AlGaN-based strain relief layer and the GaN buffer, grown using metal organic chemical vapor deposition (MOCVD). The AlGaN barrier had a 25 % Al content and a thickness of 20nm. Transfer length method (TLM) structures with

20 µm gap were fabricated using Au-based ohmic contacts and mesa isolation. Two batches of samples were fabricated consecutively.

7.3 Simulated expected UV-induced PPC effect magnitude

Similar to the previous report [221], the expected UV-induced buffer-related PPC effect was simulated in 2D using Silvaco ATLAS drift–diffusion software as explained in section 6.4. The simulation used a TLM structure with a 3 µm gap and uniform UV illumination from the top. The GaN absorption coefficient was chosen as $9 \times 10^4\,\mathrm{cm}^{-1}$ [234]. Doping profiles measured with SIMS were taken into account (table 7.1). In the buffer, a compensation ratio N_D/N_A between donors N_D and acceptors N_A of 0.5 was chosen with the sum of N_D and N_A equal to the total C doping concentration. The C acceptor and C donor (including intrinsic donors) level was chosen as 0.9 eV above the valence band and 0.03 eV below the conduction band, respectively [114], as explained in section 2.2.3. To tackle convergence issues of the simulator, no C doping was incorporated for 5 nm beneath the AlGaN/GaN interface. The impact of UV illumination was probed in the simulation by applying 10 mV across the TLM structure and monitoring the current while sweeping the illumination power from zero to $10^{-4}\,\mathrm{W\,cm}^{-2}$.

The crucial unknown factor is the ratio of N_A and N_D (including intrinsic N_D) in the UID layer given the total magnitude of C doping. Therefore, for every sample, N_D in the channel was varied up to N_A chosen at the level of the measured C doping level, which effectively changes $N_A - N_D$. Fig. 7.1 shows the corresponding expected magnitude of the PPC effect. Sample 1 shows nearly no dependency on UID N_D. The UID C doping is so low that the depletion region width is predominantly defined by the UID layer thickness which, in this case, mainly influences the magnitude of the PPC effect. Increasing the UID C doping as in the case for samples 2 and 3 increases the UID N_D dependency. When $N_D = N_A$—rightmost respective data point for samples 1 to 3 in fig. 7.1—which effectively eliminates any influence of doping on the depletion region width, the simulated PPC effect shows nearly the same magnitude for sample 1 to 3 due to the equal UID thickness. Sample 4 exhibits yet another increase in channel conductivity and high dependency upon UID N_D given the higher UID C doping. The passivation of sample 4 was not considered in the simulation. Sample 5 has the lowest expected UV-induced PPC effect based on the wider UID layer.

7.4 Measured UV-induced PPC effect for the first sample batch

The first batch of samples contained normal TLM structure as required for the measurement of the UV-induced PPC effect. To ensure sample versatility, additional fabrication steps were used to also manufacture functional HEMT devices with gate contacts. The magnitude of the effect was measured using UV illumination of 360 nm equivalent to a photon energy greater than the GaN band gap. The illumination power was $10^{-4}\,\mathrm{W\,cm}^{-2}$. The samples were kept in darkness for one

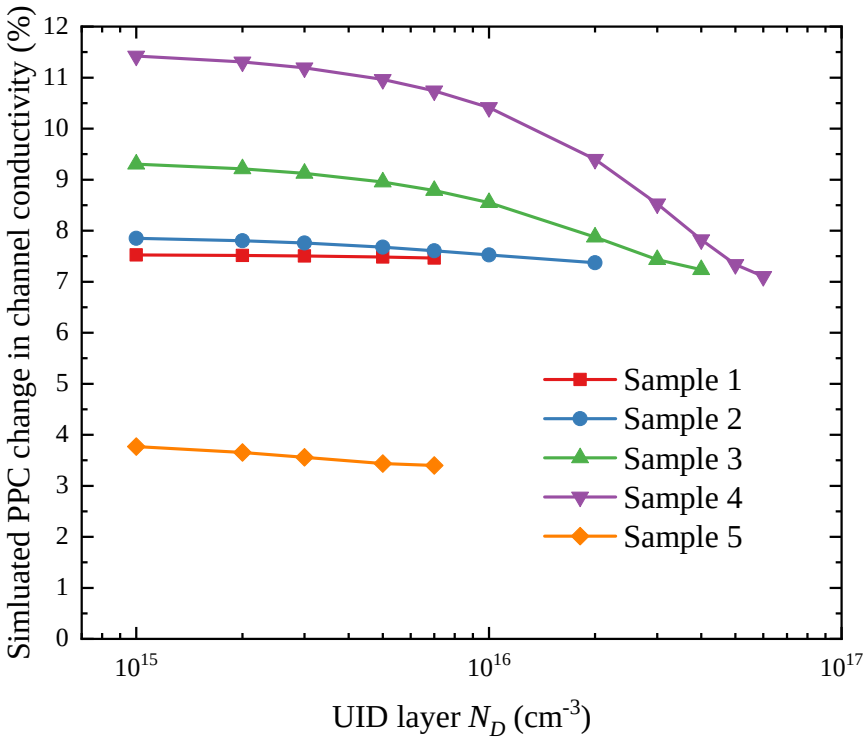

FIGURE 7.1. Simulated PPC effect magnitude for a varying UID layer N_D up to the measured channel C doping taken as channel N_A for an illumination power of $10^{-4}\,\mathrm{W\,cm^{-2}}$.

month before the initial measurement and for weeks between follow-up measurements. After the channel conductivity was measured in dark conditions for all investigated 20 µm TLM structures, the sample was illuminated with UV light for 120 s before every individual cell measurement under illuminated condition. Fig. 7.2 shows the PPC effect magnitude measurements as scatter plot and mean value alongside the expected values based on the simulations. In the initial measurement, all samples show a significantly higher PPC magnitude than simulated, however, the trend in the experiment follows the simulated trend between samples. The PPC magnitude gradually increases from sample 1 to sample 4 while sample 5 exhibits the lowest effect magnitude overall. The scatter plot highlights the widespread range for each sample showing cells with up to twice the value compared to sister cells on the same sample. Given the significant difference between experiment and simulation, the measurement was repeated after 19 d in darkness allowing for sample recovery. The repeat measurement showed an increase in PPC effect magnitude compared to the initial measurement with yet an increased variance of results for each sample. Given this observation, the measurement was repeated another two times, however, for these iterations the functionality and calibration of the setup were verified by measuring an old sample from another study as reference considering the difference in the measurement, to exclude any issues with the equipment as a reason for observed inconsistencies. Those two reference measurements using the

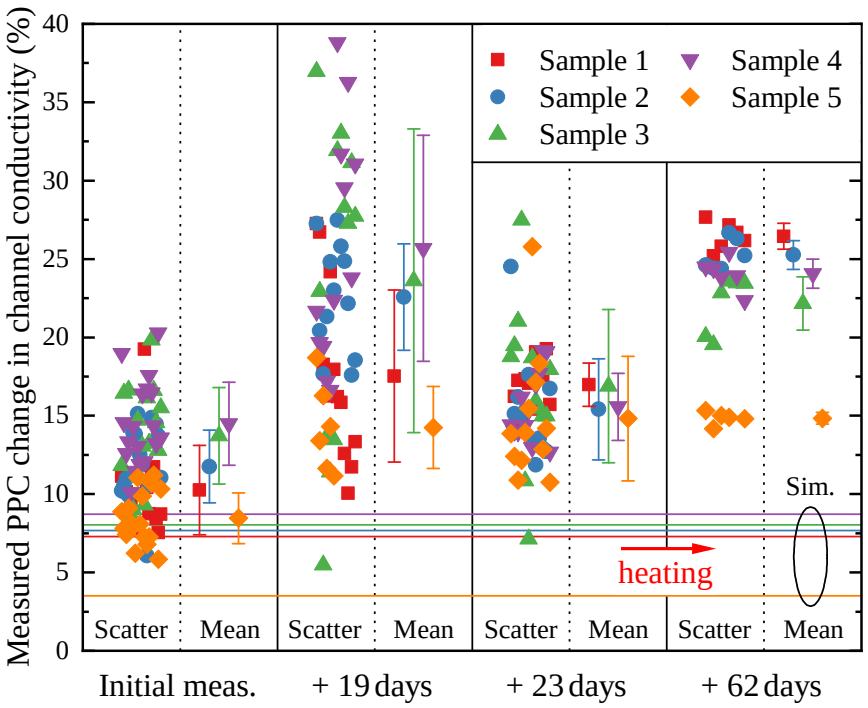

FIGURE 7.2. Measured PPC effect magnitude of the first sample batch from four different measurement dates with the respective data shown as scatter plot and mean value. The horizontal lines represent the simulation values for a respective channel compensation ratio N_D/N_A of 0.5. Time differences are relative to the respective previous measurement. Samples were stored in darkness between measurements.

old reference sample yielded an average UV-induced channel conductivity increase of 10.6 % and 12.9 %, respectively, which was aligned with a previous measurement yielding 11.7 %. This old measurement was initially intended to be part of the study in chapter 6 but was later excluded. The consistency in reference measurements illustrates the reliability of the experimental setup and any prior inconsistencies between measurements are therefore related to the samples. As the third measurement on the most recent series of samples gave yet another different result for the PPC magnitude as shown in fig. 7.2, the samples were heated at 150 °C for 1 h to accelerate any recovery of trap occupation before attempting a new measurement. The final iteration of measurement after the heating stage now showed rather consistent results for each sample, however, the values shown in fig. 7.2 are still higher than anticipated from the simulation in fig. 7.1. At this stage, it was concluded that the samples are unstable between measurements but still consistently show a persistent disagreement between simulation and experiment. This conclusion was supported by analyzing the raw measurement values for the channel conductivity under dark conditions and under UV illumination shown in fig. 7.3. Assuming insufficient recovery time between measurement iterations and traps not reaching full equilibrium, the resistance under UV illumination is expected to not change under equal illumination intensities quickly

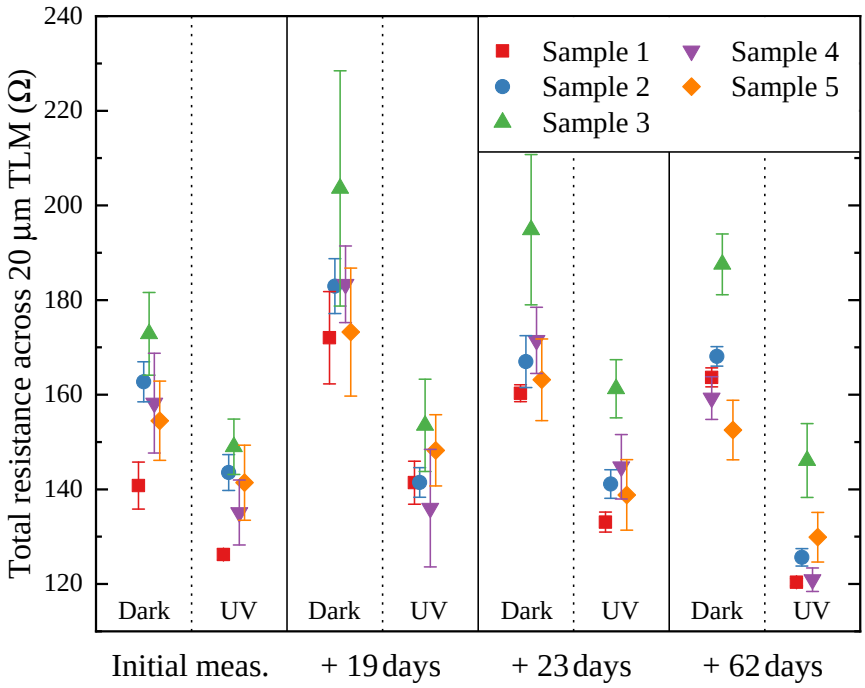

FIGURE 7.3. Total resistance under dark condition and UV illumination across the measured TLM structure with a 20 µm gap for the first sample batch. Time differences are relative to the respective previous measurement. Samples were stored in darkness between measurements.

replenishing the illuminated equilibrium condition. Only the channel conductivity in darkness should be influenced with a lower resistance given the light history. However, the first repeat measurement after 19 d shows a higher channel resistance in darkness for all samples indicating a fundamental sample instability. The resistances under UV illumination are not stable between measurements supporting the instability assessment making the set of samples unsuitable for further analyses.

7.5 Measured UV-induced PPC effect for the second sample batch

As a consequence of the previous unstable set of samples, another batch of samples was manufactured with sister pieces of the same original wafers. However, this time the last processing step fabricating gate contacts for functional HEMTs was eliminated based on the speculation that it influences the surface states that potentially play a role in the UV-induced increase in channel conductivity. The reference measurements on an old reference sample verifying proper setup alignment (details explained in section 7.4) yielded an average UV-induced channel conductivity increase of 9.5 % and 10.9 %, respectively. The second measurement showed good agreement with

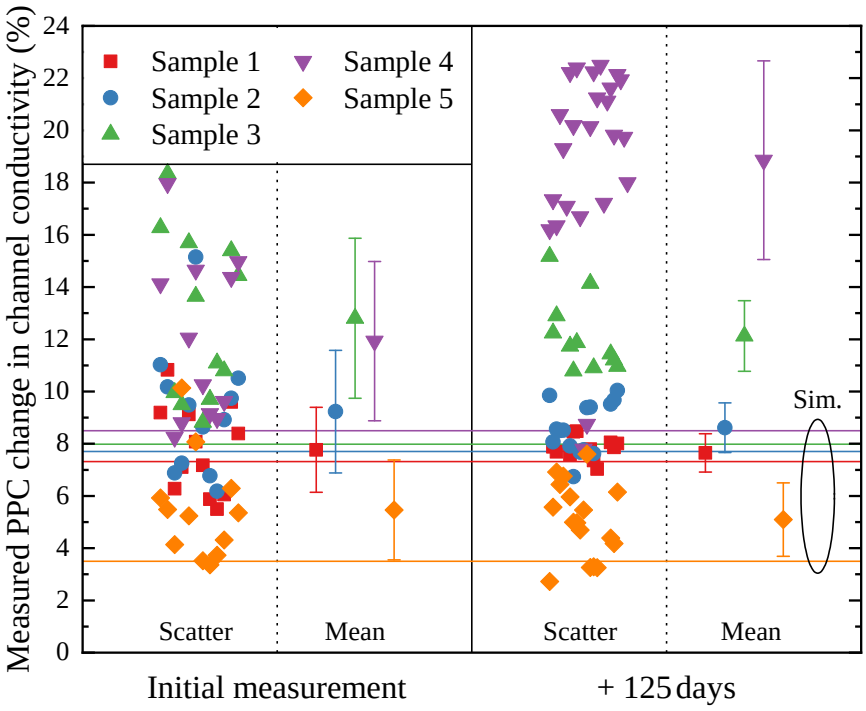

FIGURE 7.4. Measured PPC effect magnitude of the second sample batch from two different measurement dates with the respective data shown as scatter plot and mean value. Horizontal lines represent the simulation values for a respective channel compensation ratio N_D/N_A of 0.5. Time differences are relative to the respective previous measurement. Samples were stored in darkness between measurements.

the old reference value of 11.7 % and is therefore the focus of the subsequent analysis. Fig. 7.4 shows the PPC effect magnitude measurements as scatter plot and mean value for the second batch of samples. Given the experience with the previous batch, firstly the stability was examined by repeating the PPC effect magnitude measurement after the initial measurement and sufficient recovery time in darkness. All samples except sample 4 showed better repeatability between measurements compared to the first sample batch in fig. 7.2. This supports the speculation that the final processing steps to generate full transistors may have modified the surface of the wafers.

The experimental PPC values are higher than the respective simulated magnitude for all samples similar to the first sample batch. The simulation considers a buffer-related effect increasing the 2DEG concentration. The UV light absorption in the buffer causes charge accumulation in the buffer leading to a flattening of the electronic band diagram resulting in an increase in electron concentration in the 2DEG [221]. As the simulated effect magnitude may underestimate the experimentally observed magnitude, the considered buffer effect is not sufficient to fully explain the UV-induced PPC effect for those investigated samples. Even decreasing N_D in the channel having channel C doping heavily dominated by N_A does not bridge the gap (fig. 7.1). Table 7.2 shows the absolute and relative difference between experiment and simulation. The observed

TABLE 7.2. Comparison of simulated (channel N_D/N_A of 0.5) and measured PPC effect magnitudes with the absolute difference in units of percentage points (pp) and relative difference.

Sample	Simulation	Experiment	Absolute difference	Relative difference
1	7.5 %	(7.9 ± 0.4) %	+0.4 pp	+5 %
2	7.7 %	(8.6 ± 1.0) %	+0.9 pp	+12 %
3	8.0 %	(12.1 ± 1.4) %	+4.1 pp	+51 %
4	8.6 %	(18.9 ± 3.8) %	+10.3 pp	+220 %
5	3.6 %	(5.1 ± 1.4) %	+1.5 pp	+42 %

magnitude of the difference and related change in 2DEG density requires a positive charge in close proximity to the 2DEG. One potential reason for the disagreement can be an additional surface effect as considered in previous reports [224, 225, 228] which so far are neglected in the used PPC model. Using the analogy of a capacitor between surface and 2DEG, a surface potential change correlates to a capacitor voltage change leading to a capacitor charge change. Hence, an increase in surface potential causes an increase in the 2DEG electron concentration from the initial level $n_{2DEG}^{initial}$ according to

$$PPC\,[\%] = \frac{n_{2DEG}^{initial} + n_{Buffer\text{-}related\ \Delta V} + n_{Surface\text{-}related\ \Delta V}}{n_{2DEG}^{initial}} \,. \tag{7.1}$$

Using the capacitance formula of a parallel-plate capacitor

$$V = \frac{d}{\epsilon}\frac{Q}{A} \tag{7.2}$$

with plate voltage V, plate separation d, permittivity ϵ, plate charge Q, and plate area A, the required change in surface potential can be estimated by

$$\Delta V = \frac{e\,d}{\epsilon_0\,\epsilon_r}\,\Delta n_{2DEG} \,. \tag{7.3}$$

with elementary charge e, vacuum permittivity ϵ_0, and relative permittivity ϵ_r of the material. Using the absolute change in 2DEG concentration

$$\Delta n_{2DEG} = PPC\,[\%]\ n_{2DEG}^{initial} \,, \tag{7.4}$$

the required surface potential change based on the surface-related component $PPC_{Surface}\,[\%]$ can be calculated using

$$\Delta V_{Surface} = \frac{e\,d_{AlGaN}\,n_{2DEG}^{initial}}{\epsilon_0\,\epsilon_{AlGaN}}\,PPC_{Surface}\,[\%] \,. \tag{7.5}$$

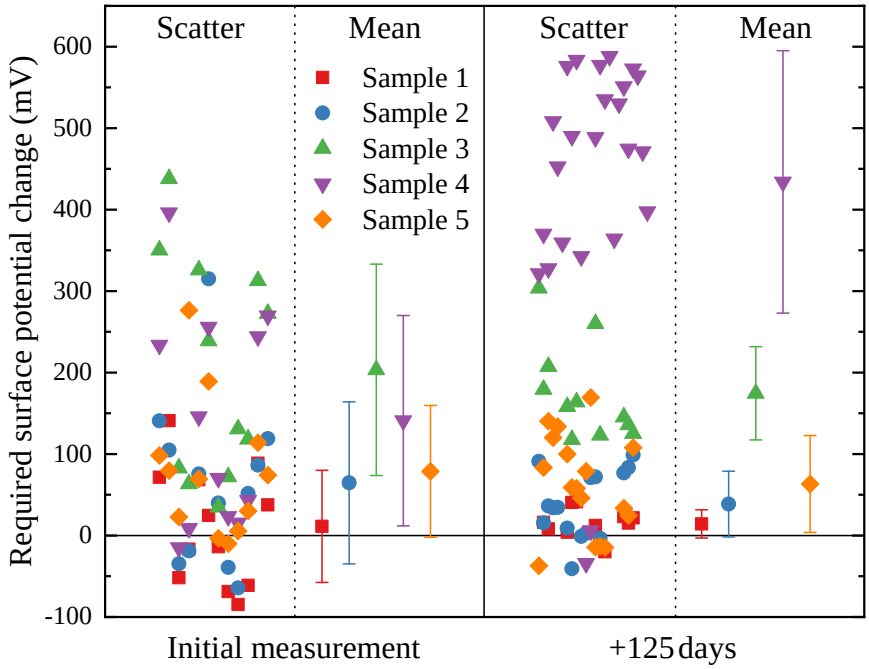

FIGURE 7.5. Calculated change in surface potential associated with the surface-related PPC effect component shown as scatter plot and mean values for initial and repeat measurement for the second sample batch. Time differences are relative to the respective previous measurement. Samples were stored in darkness between measurements.

Building on the hypothesis that the PPC difference between experiment and simulation is related to a surface effect ($PPC_{Surface} = PPC_{Experiment} - PPC_{Buffer}$), the required change in surface potential can be estimated for the samples as shown in fig. 7.5 using

$$\Delta V_{Surface} = \frac{e\, d_{AlGaN}\, n_{2DEG}^{initial}}{\epsilon_0\, \epsilon_{AlGaN}} \left(PPC_{Experiment}\,[\%] - PPC_{Buffer}\,[\%]\right) \tag{7.6}$$

with $d_{AlGaN} = 20\,\text{nm}$, $n_{2DEG}^{initial} = 10^{13}\,\text{cm}^{-2}$ [242, 243], and $\epsilon_{Al_{0.25}GaN_{0.75}} = 9.4$ [244]. As the absolute difference between experiment and simulation heavily varies between samples (table 7.2), the corresponding calculated shift in surface potential severely differs for all samples. The repeat measurement (+125 days) will be considered here given the more accurate setup calibration for PPC measurements shown by the reference measurements. Similar to the PPC plot (fig. 7.4), the scatter plot in fig. 7.5 highlights the wide range of surface potential values. Particularly, for most samples, there are a few measured cells with opposite (negative) surface potential change given a lower experimental than simulated PPC magnitude. The mean value for each sample is also shown in table 7.3. The differences between samples are significant. Samples 1, 2, and 5 require a surface potential shift on the order of tens of millivolts whereas samples 3 and 4 are on the order of hundreds of millivolts. Particularly, the passivated sample 4 requires the highest change

TABLE 7.3. Calculated required shift in surface potential based on the PPC measurement as well as the measured shift in surface potential 120 s after UV light exposure using KPFM for the second sample batch.

Sample	Surface potential change based on the second PPC measurement	First KPFM measurement	Second KPFM measurement
1	(14 ± 17) mV	280 mV	190 mV
2	(39 ± 40) mV	330 mV	300 mV
3	(175 ± 57) mV	460 mV	430 mV
4	(434 ± 161) mV	80 mV	40 mV
5	(63 ± 60) mV	20 mV	60 mV

in surface potential whereas studies have shown that passivation rather causes the opposite by mitigating the surface effect [241].

In order to follow the hypothesis of an additional surface-related PPC effect, it was attempted to measure the shift in surface potential for each sample using Kelvin Probe Force Microscopy (KPFM). The shift in surface potential was examined by point KPFM measurements using a TiPt-coated AFM probe with a resonant frequency of 70 kHz in a single-pass KPFM configuration operating at the second harmonic of the probe and an oscillating voltage V_{mod} of 5 V. The CPD signal was constantly monitored for 20 min while the UV illumination with a wavelength of 360 nm and a power of about $10^{-4}\,\mathrm{W\,cm^{-2}}$ was turned on for the first 10 min capturing the UV effect and subsequent recovery. Fig. 7.6a shows the KPFM transient measurements. All samples show a rapid increase in surface potential upon UV light illumination. Subsequently, samples 1, 2, and 3 continue to gradually increase to further positive surface potential shifts while samples 4 and 5 unexpectedly reverse after a few seconds, even drifting to negative voltages at 10 min of UV exposure. Despite the unexpected result, the transients can be reproduced as observed in the repeat measurement in fig. 7.6b after allowing sufficient recovery time in darkness of two weeks. A reference measurement on a pure Si substrate was measured to probe any light-induced voltage effects interfering with KPFM detection system but no apparent effect can be observed. Previous reports on GaN HEMT structures observed similar behavior for the surface potential upon UV light illumination [245, 246]. It is speculated that a sharp surface potential increase due to hole accumulation at the surface is followed by saturation at positive voltages for the Ga-polar GaN face and a trend reversing saturating at negative voltages for the N-polar GaN face due to elevated photoinduced oxygen chemisorption [247, 248]. Other publications observed similar characteristics with a surface potential increase for n-GaN and surface potential decrease for p-GaN, due to separation of the photogenerated charges caused by the electronic bands [249].

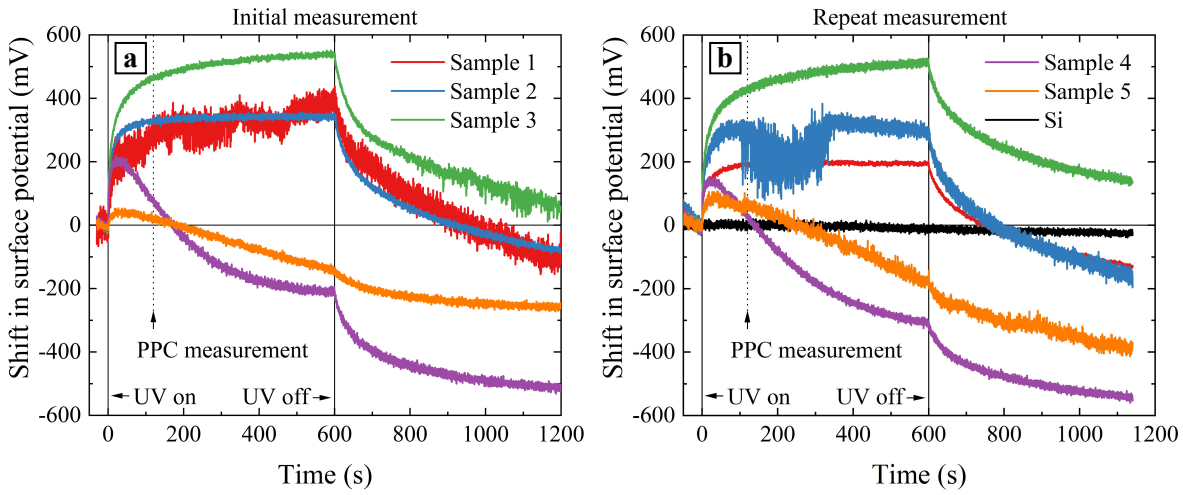

FIGURE 7.6. Surface potential shift transients as KPFM point measurements for one representative cell of each sample (individual cell PPC equivalent to mean sample PPC) of the second sample batch: a) initial measurement and b) repeat measurement after sufficient recovery in darkness of two weeks. Transients were offset by the initial KPFM value to focus on relative change. The repeat measurement included a reference measurement on a pure Si wafer. The vertical dashed line at 120 s represents the duration waited for stabilizing purposes during PPC magnitude measurements.

Although those studies were conducted on pure GaN epitaxies, the same effect may apply to the AlGaN/GaN structures examined here as well.

Initially, the magnitude of the PPC effect was measured after allowing the samples for 120 s to reach equilibrium. While this seems reasonably sufficient for samples 1, 2, and 3 given the KPFM measurements, samples 4 and 5 had already reversed the surface potential shift trending to negative values. However, after 120 s of UV light exposure, the surface potential change is still positive in accordance with the PPC measurements. The voltage values at this point are given in table 7.3 in comparison to the calculated required surface potential shift based on the PPC measurements. Qualitatively, for samples 1, 2, and 3, the trend is aligned between KPFM measurement and PPC measurement. Samples 4 and 5 are difficult to compare given the apparent different dynamics. As all samples except sample 4 are unpassivated, the surface potential can also be influenced by various chemical or electrochemical reactions. Clearly, surface effects can impact the measurements, and this needs to be built into a future extension of the PPC model developed here to accurately extract insights and quantities from the PPC measurements.

7.6 Conclusions

The UV-induced PPC effect was studied using a set of five samples with different UID C doping, layer thicknesses, and sample passivation. The first batch of samples turned out to be unstable yielding a different result every repeating measurement. The proper operation of the setup was verified by measurements using a reference sample. Examination of the raw channel conductivity values in darkness and under UV illumination showed that the reason cannot be insufficient recovery time between measurements. Nevertheless, all measurements showed a higher UV-induced PPC effect than simulated for all samples. The replacement batch of samples proved to be more stable except for the passivated sample, counterintuitively. Again, all samples revealed a PPC effect magnitude higher than the respective simulated magnitudes indicating an additional effect on top of the considered buffer-related electronic band bending. The possibility of an additional surface-related effect is explored. Using the analogy of a parallel–plate capacitor, an increase in potential on the surface leads to an increased electron concentration in the 2DEG. However, the equivalent shift in surface potential is inconsistent between samples. The surface potential shift was measured using KPFM transient measurement under UV light exposure. Again, the samples showed an inconsistent transient behavior, however, the difference in magnitude after 120 s of UV illumination qualitatively represents the calculated required positive shift in surface potential based on the PPC magnitude measurements. Overall, for the investigated samples here, the UV-induced PPC effect is likely a combination of a buffer effect flattening the electronic band structure as well as a surface effect changing the occupation of surface charge states. Unfortunately, the inconsistencies between samples and measurements prevent further structured analyses.

CHAPTER 8

CONCLUSIONS

With its many advantages over competing electronic components, the GaN HEMT technology can revolutionize the power electronics and radio frequency industry. The high breakdown field and high electron mobility allow for highly efficient devices facilitating the transition to more sustainable technologies such as electric vehicles. It reduces weight and size of equivalent electric circuits yielding a higher power density. However, many technical challenges such as buffer optimization to facilitate high voltage breakdown fields remain to be addressed before GaN technology can be widely used in application. The buffer and its behavior is also the center of this thesis. It primarily focuses on the effect of different external stresses on the buffer as found during operation in different environments.

GaN growth on foreign substrates such as silicon inevitably leads to the incorporation of defects such as threading dislocations. These dislocations are known to act as vertical conductive paths that can reach from the substrate all the way to the surface. The associated leakage has various implications and is expected to heavily affect the breakdown characteristics. Often, buffer leakage is measured as a bulk current and therefore understandably considered a bulk effect without correlation to individual contributions of different dislocations. However, a device can be expected to break down at the weakest point related to individual dislocations. Hence, dislocation-related leakage has to be measured at the location of the defect which is typically done using conductive AFM and potentially measuring the current–voltage characteristics of that spot. However, the major drawback of those conductive AFM measurements is the fact that it is a surface-sensitive technique that does not yield information about length, direction, and type of the leakage path. On top, the shunting effect of the 2DEG can obscure conductive AFM measurements as it can electrically connect vertical leakage paths horizontally causing conductive AFM to be sensitive to leakage through the AlGaN barrier instead of the buffer.

Furthermore, there is no information about threading dislocations that create a leakage path that is only partway conductive. All in all, there is limited information how dislocation-induced leakage paths are locally acting under real device operation conditions with off-state stress.

As part of the work, a new measurement methodology was developed to assess the influence of vertical leakage paths under off-state stress conditions. The technique combines surface-sensitive KPFM measurements with substrate bias ramping. Thereby, the buffer and its different kinds of threading dislocations causing vertical leakage paths to become 'visible'. The large negative substrate voltage biases the conductive paths on the bottom which in return causes potential deformations through the buffer to the 2DEG that are probed by KPFM on the surface. Building such a back-biased KPFM setup comes with many challenges. One key hurdle is the attempt to measure surface potential changes in the range of millivolts while applying hundreds of volts to the back of the sample. Fringing fields can disturb the KPFM detection system and can make surface potential measurements impossible. That is particularly the case for amplitude-modulated KPFM where the sensitivity is not very localized around the tip of the AFM probe. This problem was tackled by designing a specific device processing mask that leaves the majority of the surface as metallic contact while only having a few narrow gaps which allow access to the GaN surface. The metal surface was grounded which shields the cantilever and KPFM system from any back bias field. Another step of improvement was achieved by optimizing the substrate bias supply and reduce it in size lowering the openly exposed biased areas. Another consideration is the electrical protection of the expensive AFM instrument itself. AFM instruments are not regularly designed to handle hundreds of volts around the sample chuck and the KPFM system, typically internally providing a chuck voltage of only up to $\pm 10\,\mathrm{V}$. Limiting the peak current in the event of a catastrophic device breakdown is vital to protect the AFM instrument. This was achieved by inserting a highly resistive safety resistor in series with the back bias supply. However, that safety solution implicates other challenges. A very high resistance can extend the RC time of the substrate voltage supply to unpractical timescales. A resistance too high and close to the vertical resistance of the sample also leads to a reduction of the effectively applied substrate voltage at the sample as a substantial proportion of the supplied back bias is dropped across the safety resistor instead. A resistance too low imposes safety risks. A compromise has to be made for every device based on the substrate ramp measurement and the corresponding vertical leakage characteristics.

Measurement of the surface potential while applying a substrate voltage demonstrated the complexity of breakdown associated with dislocations. At zero to moderate levels of negative substrate voltage, there are no apparent surface potential features. However, at a negative back bias comparable to off-state device stress, certain spots related to vertical conductive paths show a reduced surface potential compared to the surrounding areas. The spot size and the magnitude of the potential drop both increase with higher negative substrate voltages. At a substrate voltage of two thirds of the back-gated pinch-off voltage, the spots reach up to $1\,\mu\mathrm{m}$

in diameter. Stepping back the substrate voltage shows a degree of irreversibility of the effect. Looping the substrate voltage down and back to no back bias reveals a hysteresis effect of the surface potential features, occasionally with surface potential features remaining for a long time of several hours after returning to zero back bias again. This event potentially indicates a previously unconsidered effect of dynamic on-resistance. The drop in surface potential indicates an inhomogeneity of the 2DEG with significant associated potential deformations throughout the buffer. Simulations demonstrate that a conductive path of any length is locally electrically thinning the buffer causing a potential deformation around the core of the leakage path. The magnitude of the effect is proportional to the conductivity of the conductive path. This effect also occurs for conductive paths that only extend partway through the buffer, however, the closer the conductive path reaches the 2DEG, the more severe are the implications. The deformations of the vertical buffer field under off-state bias conditions correlate to a highly non-uniform electric field stressing the upper GaN layers, particularly the channel, instead of the buffer which is designed and expected to actually handle the stress. This location of elevated stress is very prone to induce device breakdown suggesting that breakdown in general is rather a highly localized phenomenon driven by weak locations in the vicinity of highly conductive vertical path associated with threading dislocations rather than a bulk effect.

Illuminating a GaN device with light imposes another type of stress onto the buffer. Especially wavelengths with an energy greater than the GaN band gap allow for absorption and charge carrier generation within the GaN layers. In that case, ultimately, the 2DEG concentration is increased due to the UV illumination leading to an increase in channel conductivity that lasts for a long time up to one month, known as persistent photoconductivity (PPC). The effect is shown to yield different levels of magnitude in channel conductivity change and it exists for a wide range of device configurations irrespective of buffer doping type and level as well as substrate material. The light exposure necessary to trigger a significant impact of the effect is equivalent to the conditions in many laboratories. Measurements and simulations demonstrate that the effect can be attributed to charge generation in the buffer changing the buffer charge concentrations. This causes a change in the electronic band diagram alongside capacitive coupling between 2DEG and buffer. The magnitude of the effect is closely linked to the difference between acceptor density (N_A) and donor density (N_D) in the buffer, i.e. the net doping density $N_A - N_D$, which in return defines the depletion region width. The greater $N_A - N_D$, particularly in the unintentionally doped (UID) region ($N_{A,\,UID} - N_{D,\,UID}$), the larger is the magnitude of the effect. Consequently, it was discovered as part of this work that the effect magnitude can be used as a technique to determine the net deep-level doping density $N_A - N_D$ which ultimately defines the buffer dynamics during device switching and the buffer insulation properties. This essential quantity is extremely difficult to determine by any other method. Full recovery from UV exposure and full elimination of the effect can take up to one month. The transient recovery and its timescale components can be explained using a combination of direct electron–hole recombination dynamics

and dislocation-assisted leakage currents. Another set of samples revealed a significantly higher persistent photoconductivity effect than predicted by the buffer-related change in electronic bands, independent from adjustments of $N_A - N_D$. However, those samples showed pronounced instability and reliability issues complicating a systematic analysis of potential additional surface-related contributions to the persistent photoconductivity effect.

Future work based on back-biased KPFM could further investigate the observed contribution of partially conductive dislocations. Simulating the effect of these dislocations on a quantitative level might yield insights into the overall extent and which part of the buffer to focus on for reliability concerns. It could also be useful to understand the observed dynamic hysteresis behavior after returning to no back bias again with recovery requiring many more hours. This could potentially be another effect of dynamic on-resistance. Another possibility for future work is studying the difference between sets of samples using different buffer designs with different dislocation densities and potentially varying dislocation type ratios. The technique itself could have more application beyond the GaN HEMT space where the surface potential is expected to change based on applying hundreds of volts to the back of the sample.

Future studies regarding the UV-induced PPC effect could center around analyzing the barrier and surface contribution in comparison to the buffer contribution on a quantitative level. These studies could also focus on the role of the passivation layer. Given the different timescales involved—a rapid initiation of the effect in matters of seconds as well as recovery times from UV exposure up to one month—the dynamics of the effect could help further understand the involved processes.

APPENDIX A

ADDITIONAL DATA FROM OPTIMIZING THE BACK-BIASED KPFM SETUP

In order to develop the experimental setup and optimize it, many different measuring modes, AFM probes, and measurement configurations were tested. This appendix shows related data alongside the discussion why those options were not as ideal or did not work at all.

A.1 Different KPFM measurement modes

As discussed above in chapter 4, there are several options how to measure KPFM. Regarding topography scanning, the available AFM instrument (Bruker Dimension Edge) did not offer peak-force tapping in combination with KPFM but only regular tapping mode. In terms of KPFM measurement modes, the available AFM instrument did not allow FM-KPFM but only AM-KPFM. Regarding the KPFM measuring configuration, there are two different modes: lift mode with KPFM operating at probe resonant frequency f_0 and single pass (dual frequency) mode with KPFM using the second harmonic frequency f_1 of the probe at typically $f_1/f_0 \approx 6.2$ [250, 251]. Operating the single pass mode with two resonant frequencies risks cross-talk between topography and KPFM scanning. Therefore, for single pass, it is also suggested to try a low non-resonant frequency for KPFM [252].

All three modes were tested to identify which mode works best in the available AFM instrument. For lift mode, different lift heights were tried since it has a crucial influence on the potential contrast [253]. As the GaN samples do not show clear surface potential features unless a high back bias is applied, this test was performed on highly oriented pyrolytic graphite (HOPG) flakes on Si. Fig. A.1 shows the CPD scans for each KPFM mode. The topography images shows HOPG flakes on the left and lower right part of the scan area. Both single pass CPD images,

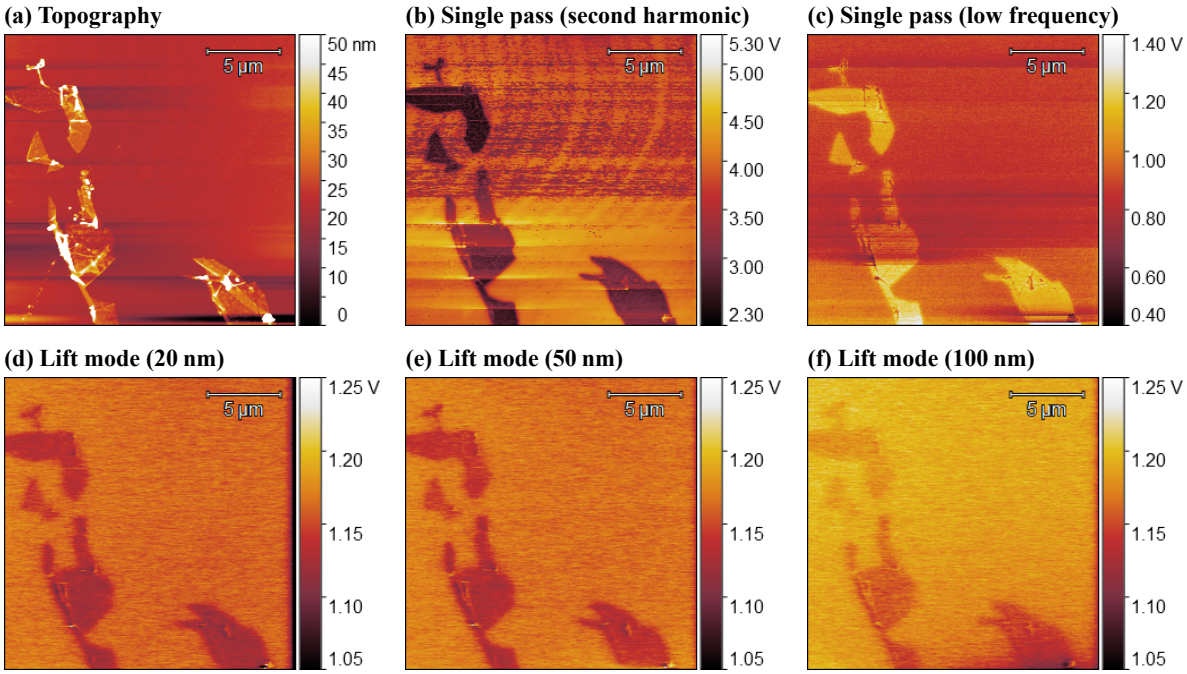

FIGURE A.1. Test of different KPFM modes on HOPG flakes on Si with a) topography, b) CPD image by single pass mode using the second harmonic frequency, c) CPD image by single pass using a low non-resonant frequency of 20 kHz, and the CPD image by lift mode with the different lift heights of d) 20 nm, e) 50 nm, and f) 100 nm.

particularly the single pass at the second harmonic frequency, are significantly noisier than lift mode. Moreover, the CPD values for single pass differ in terms of magnitude and range compared to lift mode. However, when analyzing CPD scans qualitatively, the exact CPD magnitude is not relevant and single pass can still give valuable measurements if lift mode does not work due to other artifacts such as edge effects caused by probe lifting and lowering as well as by probe grounding for every topography scan. For lift mode, the scans with the lower lift height resulted in better feature resolution. It was therefore concluded, that for the available AFM instrument, lift mode with a smaller lift height is the preferred method over the single pass technique with its disadvantages that are probably caused by potential cross-talk between topography and KPFM measurement [180].

A.2 Different KPFM probes

During the study, three different kinds of conductive AFM probes were considered to investigate whether one kind of probe would work better: Bruker SCM-PIT-V2 (75 kHz), NuNano Scout 70 (70 kHz) and NuNano Scout 350 (350 kHz). Initial testing showed that there was no clear

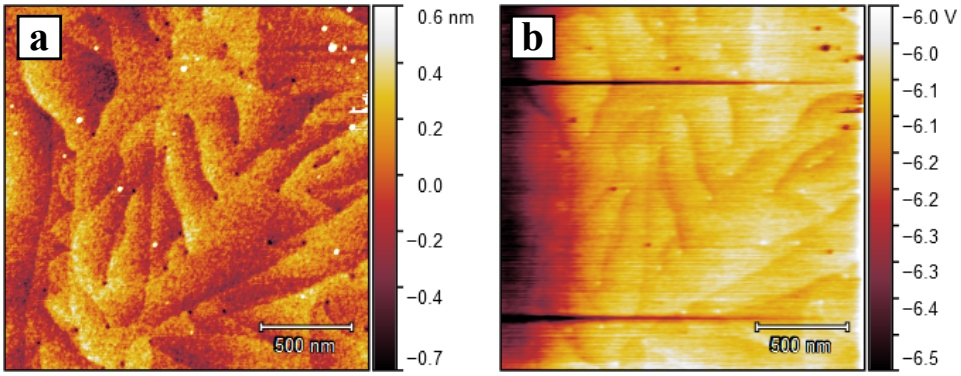

FIGURE A.2. Surface potential measurement using high frequency KPFM probes (350 kHz) with a) the topography scan and b) the corresponding CPD image.

topography resolution difference between the Bruker and NuNano probes despite the stated tip radius difference of 25 nm and 5 nm, respectively. Hence, all data shown in the thesis were measured with NuNano probes due to economic factors. Several published reports suggest that high spring constant and high frequency KPFM probes have excellent measuring performance [188]. Therefore, a set of probes with a frequency of 350 kHz instead of 70 kHz was compared. Fig. A.2 shows one surface potential measurement under no back bias using lift mode with a lift height of 10 nm. While the topography performance was satisfactory showing the typical atomic GaN steps as well as the dislocation pits on the surface, the CPD scan seemed off. Firstly, the general magnitude of the CPD values seemed too low. This effect could be related to the higher cantilever spring constants. For comparison, a softer cantilever with a lower resonant frequency shows a higher sensitivity for weaker forces due to the comparably larger induced oscillation amplitudes. Secondly, the probes showed pronounced edge effects when lowering the probe on the left side (potential dip) and raising the probe on the right side (potential spike). Thirdly, CPD scan showed features heavily correlated with the topography scan. It was therefore concluded that these KPFM probes do not work as well as the low frequency counterparts.

A.3 Different setup atmosphere

In an attempt to tackle background effects and improve the CPD signal quality, a different measuring atmosphere was tested. Often, KPFM measurements are performed in a dry nitrogen atmosphere to have inert conditions and minimize atmospheric interference [254, 255]. Especially humidity can have an erroneous influence on the KFPM measurement [256, 257]. While the available AFM instrument did neither have its own atmospheric enclosure nor it was placed in a glovebox, an initial test was performed by providing a constant nitrogen flow into the air turbulence prevention hood sitting above the AFM instrument. The humidity level was simultaneously monitored using a humidity sensor (Honeywell HIH-4000-003). As reference, first

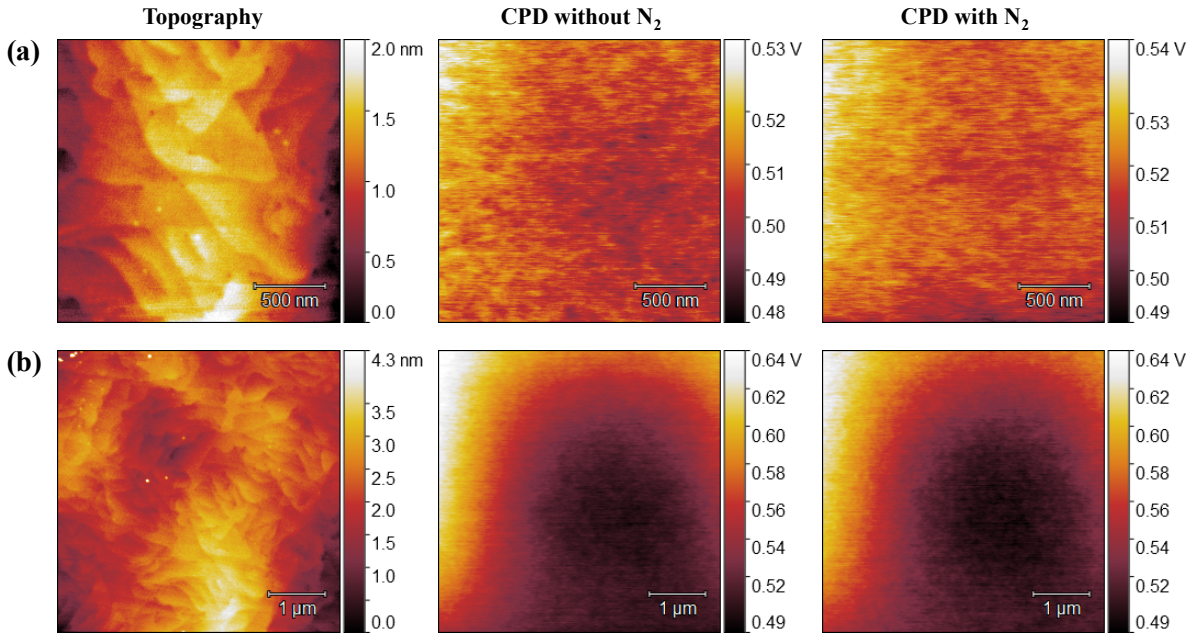

FIGURE A.3. Surface potential measurement with and without a nitrogen atmosphere for a) a smaller and b) a larger scanning area.

a measurement under ambient conditions was performed. Then the AFM hood was flooded with nitrogen until the humidity level had dropped way below 10 % followed by the measurement under near-inert conditions. Fig. A.3 shows the sequence of measurements for two differently sized scans. The KPFM measurements used single pass mode with the KPFM detection operating at the second harmonic frequency. Both measurements do not show any significant change and improvement in KPFM feature resolution, taking the surface dirt as reference. It was therefore concluded that equipping the AFM system with a dry nitrogen atmosphere was not beneficial to the back-biased KPFM measurements on GaN.

APPENDIX B

ADDITIONAL BACK-BIASED KPFM MEASUREMENTS

There were many attempts at back-biased KPFM that show CPD features correlated to conductive dislocations at negative substrate voltages. The quality of those scans was simply not as good, however, they validate that the observed result is reproducible. All measurements were taken on samples from the same wafer as discussed in chapter 5. The scans were acquired at different locations on the samples using both lift mode and single pass mode. However, for all these measurements, the initial high safety resistor of 1 GΩ was still in place lowering the effectively applied substrate voltage in comparison to the supplied substrate bias.

Fig. B.1 shows a lift mode back-biased KPFM measurement sequence where several CPD features appear at a substrate voltage of −400 V in the upper left corner. Similar to the shown data in the main chapter, the features become more pronounced while more features appear as the substrate voltage is stepped down to −600 V. On the reverse stepping, the spots disappear again beyond −400 V. Fig. B.2 shows another lift mode measurement sequence with similar behavior, however, CPD features already appear at −200 V in the upper half and disappear more gradually on the reverse sequence, even slightly remaining when no back bias is reached again. Fig. B.3 shows a single pass back-biased KPFM measurement sequence that was performed on the same area following the lift mode measurement in fig. B.2. Therefore, the initial scan shows the same mild CPD features from the end of the previous measurement sequence. Stepping the substrate voltage down, the lift mode measurement from earlier is essentially reproduced. While the feature resolution is reduced, the scans generally appear more stable. Fig. B.4 shows another single pass measurement sequence with only one CPD feature appearing on the center left edge at a substrate voltage around −500 V. But the spot remains visible until −100 V on the return stepping. Fig. B.5 shows a small area single pass measurement with one CPD feature occurring in the upper right corner at a substrate voltage around −500 V and arguably another spot appearing in the lower center at −650 V.

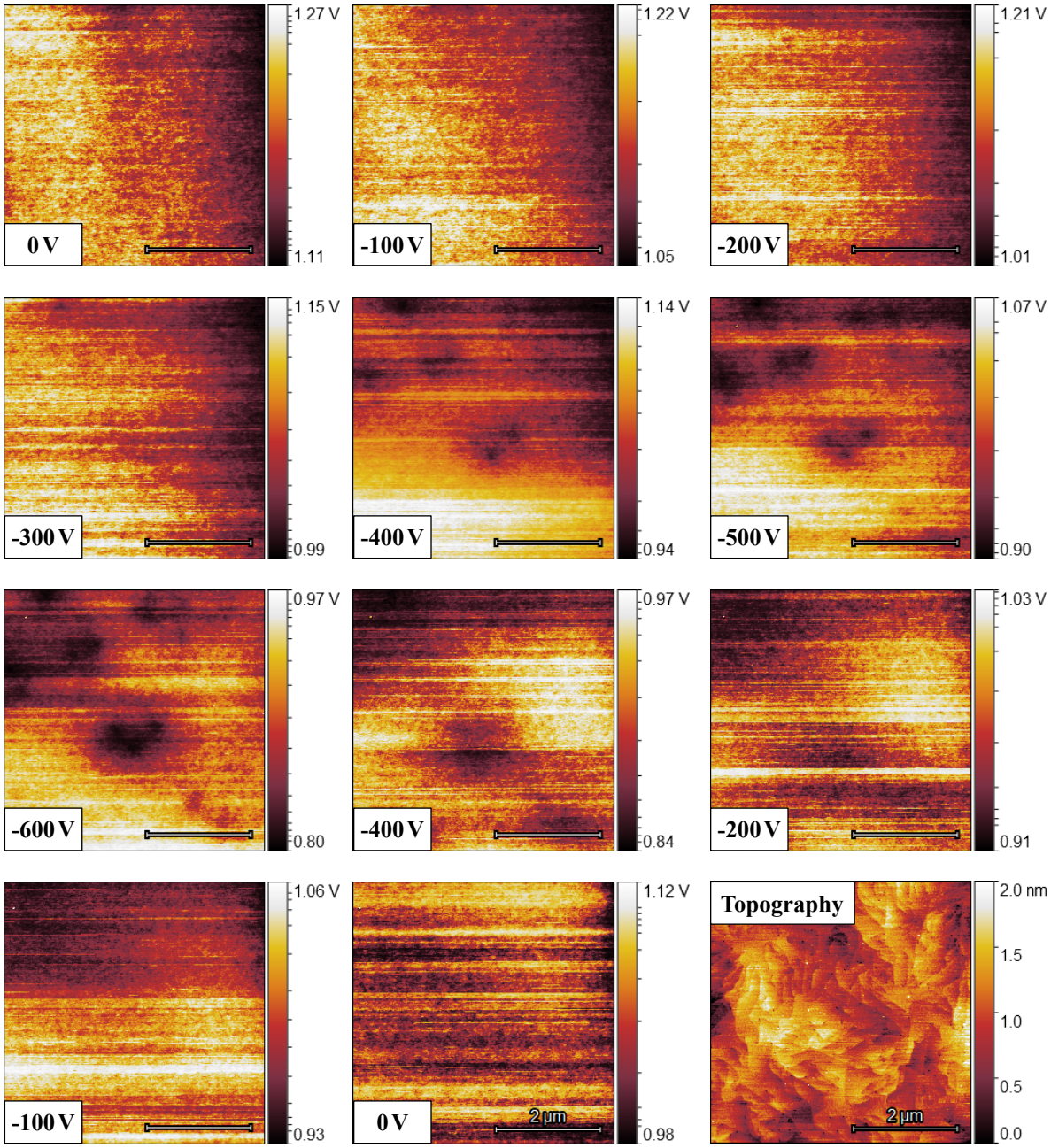

FIGURE B.1. Sequence of CPD images for varying substrate voltage from 0 V down to −600 V and back to no substrate bias measured in lift mode with a lift height of 10 nm. The scale bar is 2 µm.

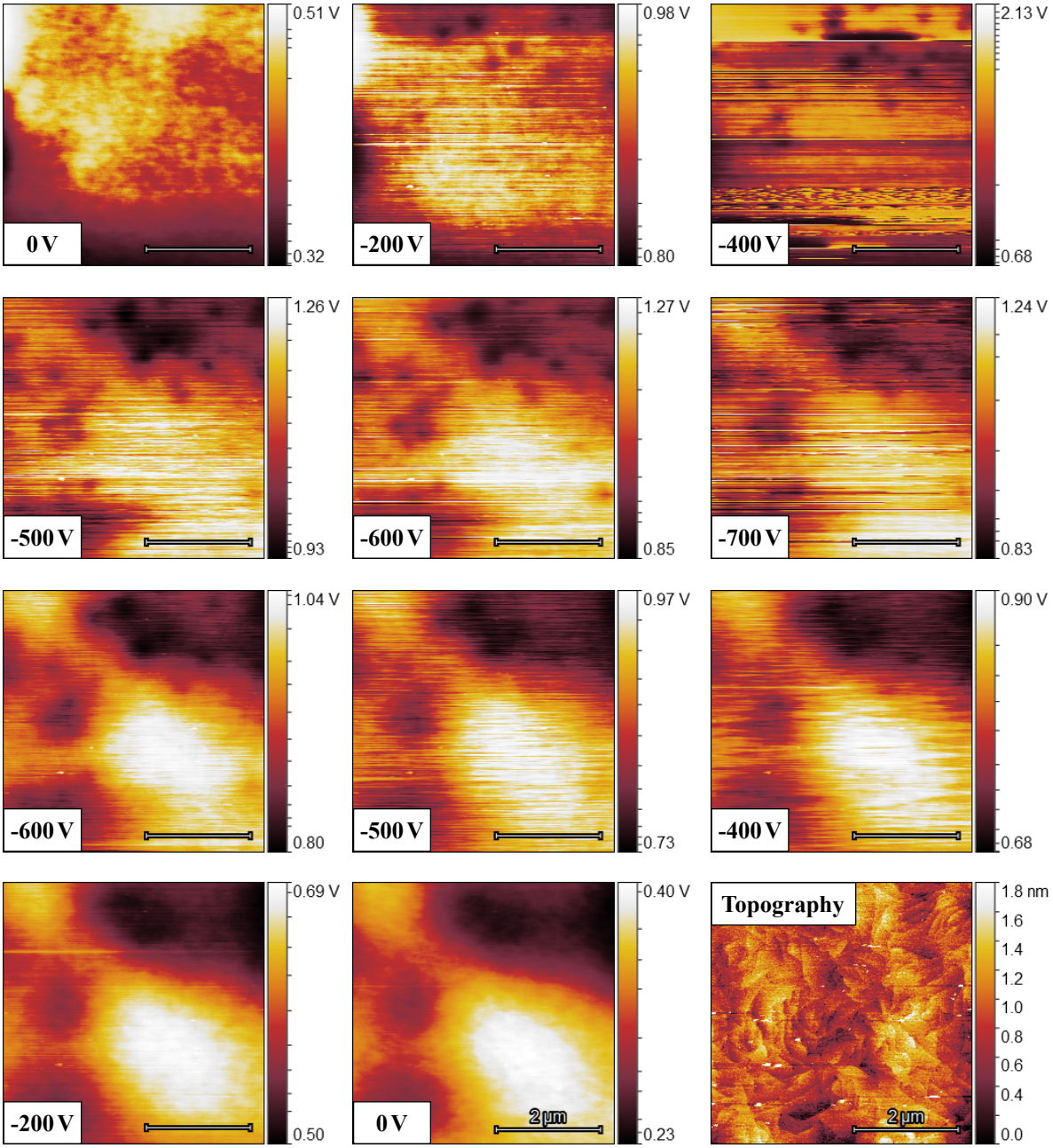

FIGURE B.2. Sequence of CPD images for varying substrate voltage from 0 V down to −700 V and back to no substrate bias measured in lift mode with a lift height of 10 nm. The scale bar is 2 µm.

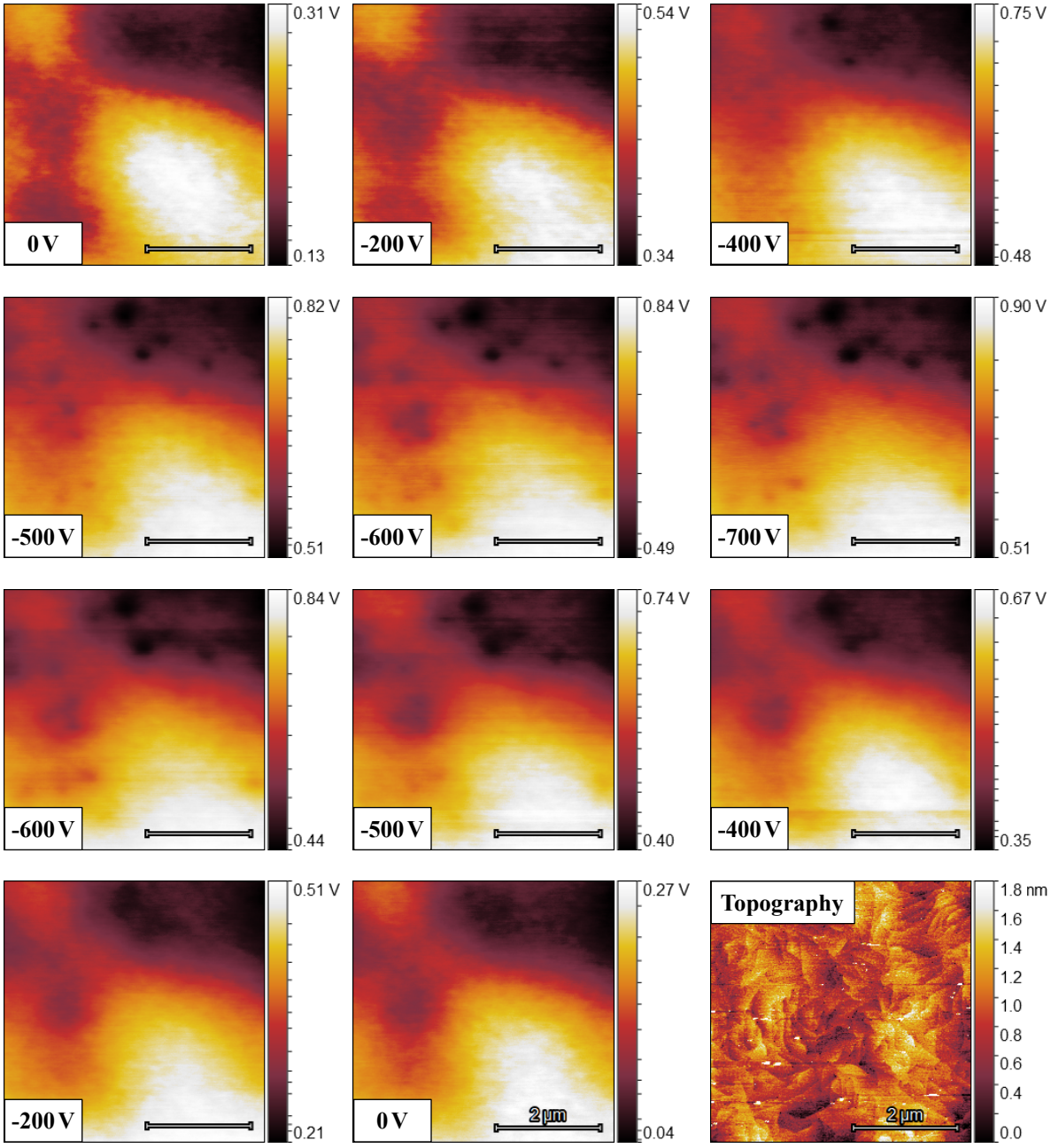

FIGURE B.3. Sequence of CPD images for varying substrate voltage from 0 V down to −700 V and back to no substrate bias measured in single pass mode on the same area right after the previous lift mode measurement in fig. B.2. The scale bar is 2 µm.

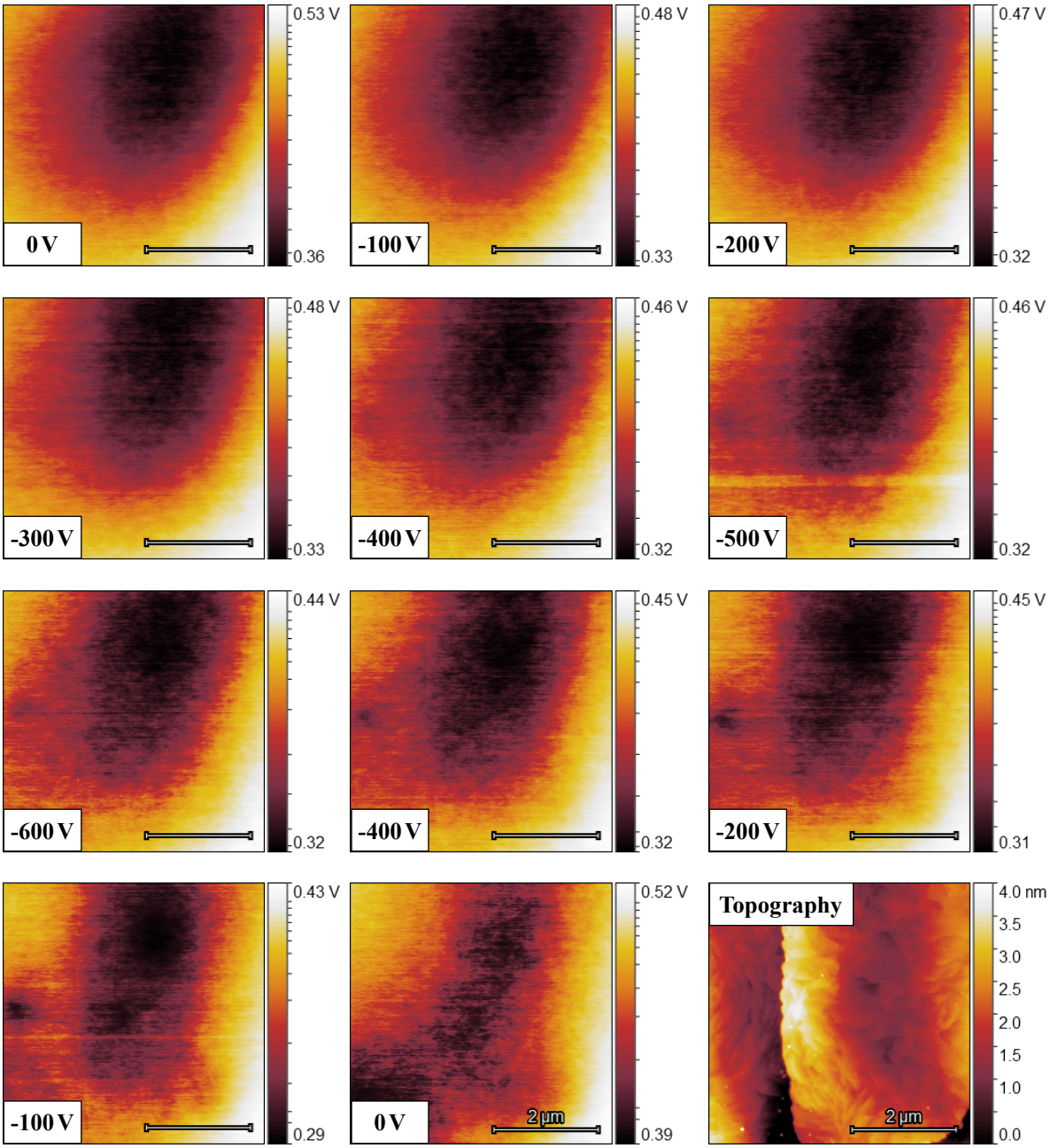

FIGURE B.4. Sequence of CPD images for varying substrate voltage from 0 V down to −600 V and back to no substrate bias measured in single pass mode. The scale bar is 2 µm.

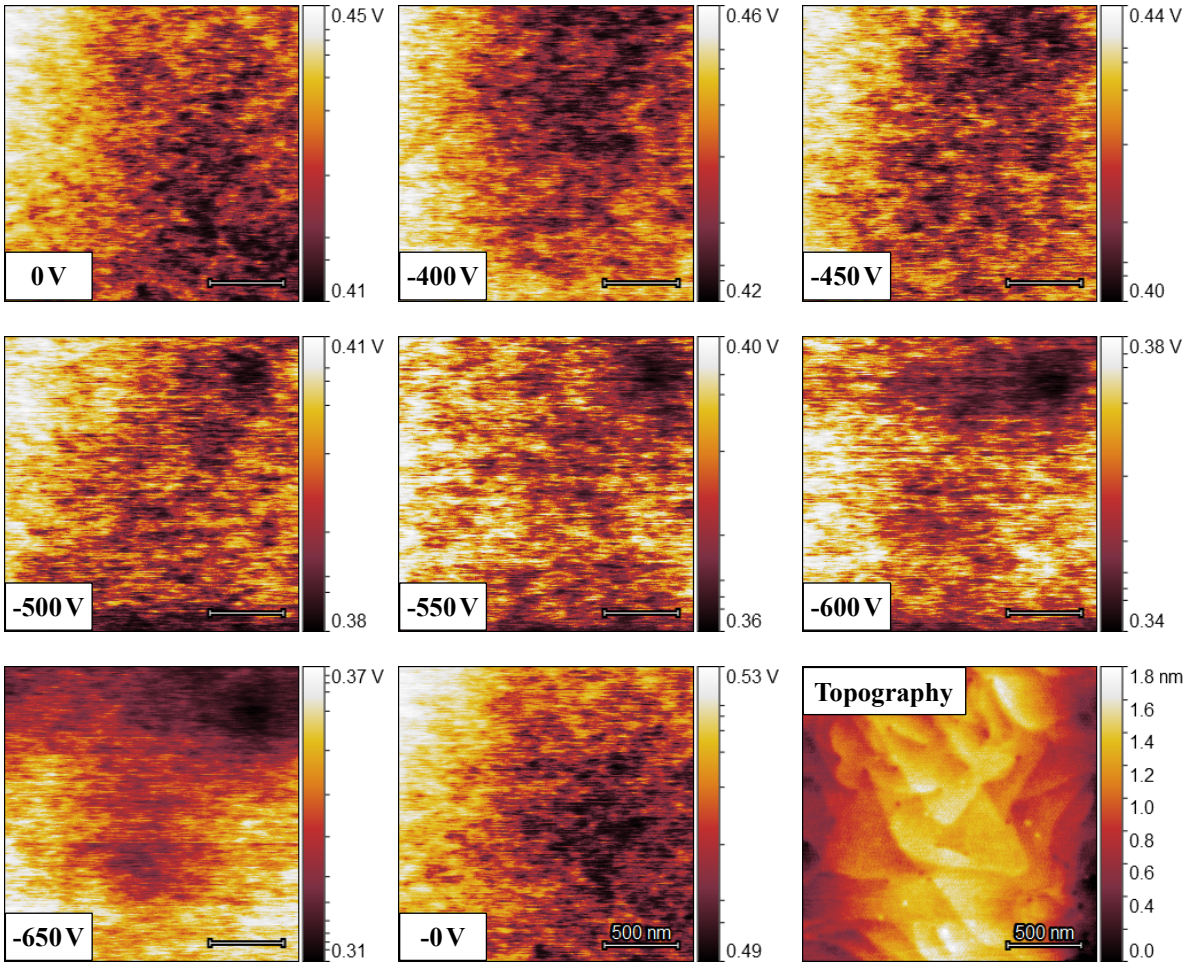

FIGURE B.5. Sequence of CPD images for varying substrate voltage from 0 V down to −650 V plus one scan again at 0 V back bias measured in single pass mode. The scale bar is 500 nm.

APPENDIX C

SUPPLEMENTARY MEASUREMENTS FOR BUFFER-RELATED UV-INDUCED PPC

The chapter 6 focuses on the PPC effect under UV illumination, however, there are more dimensions under which the PPC effect can be explored. The used light source and light setup did not allow for accurate attenuation of the illumination power. This prevents probing the magnitude of the UV-induced PPC effect upon changes in illumination power for the investigated samples. Previous reports showed that the magnitude typically increases logarithmically around $10^{-4}\,\mathrm{W\,cm^{-2}}$ with a subsequent tendency to saturate at higher illumination densities [224].

However, the setup allowed a wavelength dependent measurement. The wavelength dependent power calibration of the light source is shown in fig. C.1. The optical density is around $10^{-4}\,\mathrm{W\,cm^{-2}}$ for wavelengths in the range $300-550\,\mathrm{nm}$. At lower wavelengths, the illumination power drops quickly reaching effectively no light output at 200 nm, however, this can also be partly due to the low responsitivity of the Si photodiode used to measure the illumination power.

The wavelength dependent PPC effect was exemplarily measured for sample A after recovery in darkness for one month. The measurement starts at high wavelengths stepping down into the UV light regime and is shown in fig. C.2. The channel current increases when the wavelength crosses the wavelength equivalent to the energy of the GaN band gap. Particularly, it is not further affected when the wavelength crosses the wavelength with an energy equivalent to the AlGaN band gap. This measurement validates that the key contribution for the UV-induced PPC effect in the presented samples originates from absorption in the GaN buffer, aligned with previous reports [224–227].

The UV-induced PPC effect occurs on a rapid time scale, however, it is important to measure the channel conductivity under UV light illumination conditions once the sample has reached

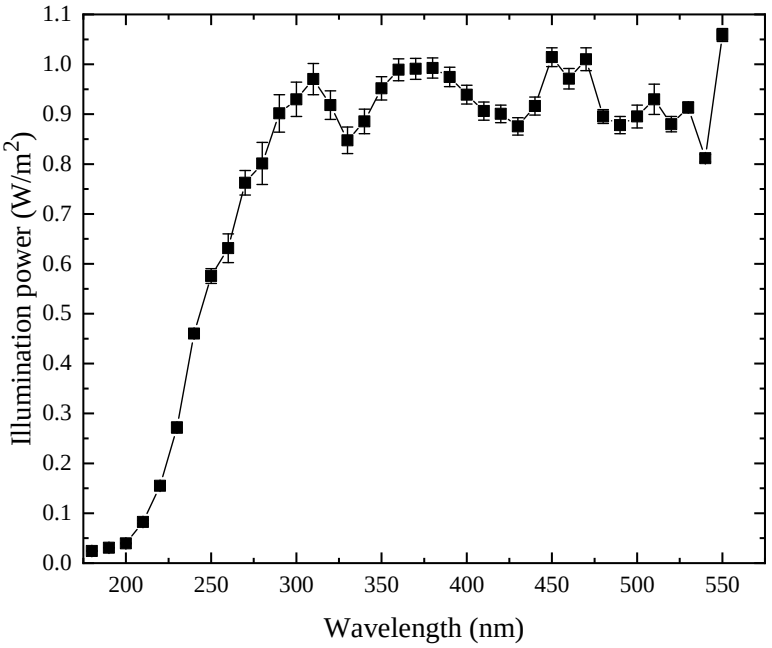

FIGURE C.1. Wavelength dependent illumination power measurement of the used light source combined with the monochromator in a distance of about 2 cm from the outlet of the optical fiber measured using a Si photodiode.

equilibrium. For the measurements presented in the thesis, this stabilization time was chosen to be 2 min long. This duration was primarily based on a calibration measurement monitoring the channel current after the sample has been exposed to UV light, shown in fig. C.3 for wafer A. The vast majority of the channel conductivity increase occurs within seconds reaching a plateau after the first minute of illumination.

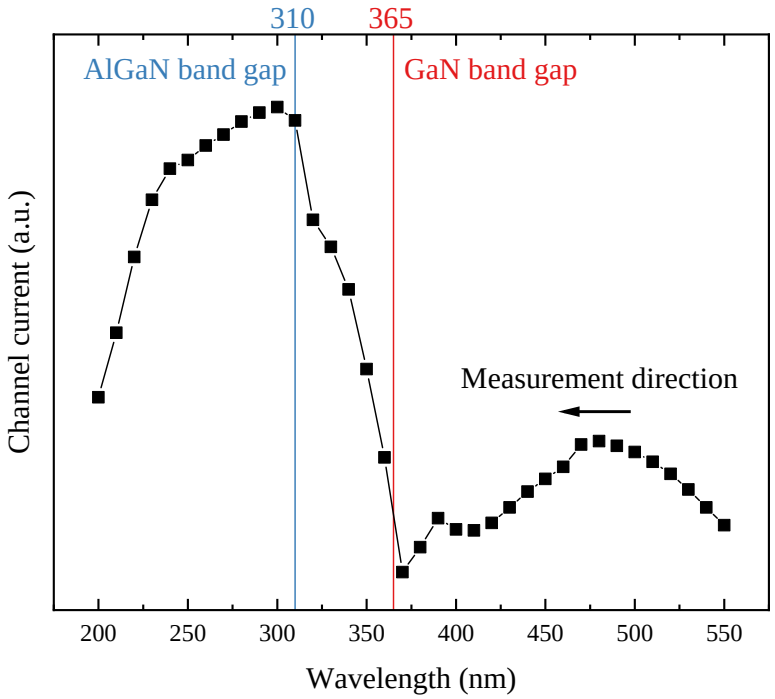

FIGURE C.2. Wavelength dependent channel current for wafer A measuring across a TLM structure with illumination starting from long wavelengths stepping down into the UV light range. The AlGaN band gap line is drawn for a 25 % Al mole fraction [258–261].

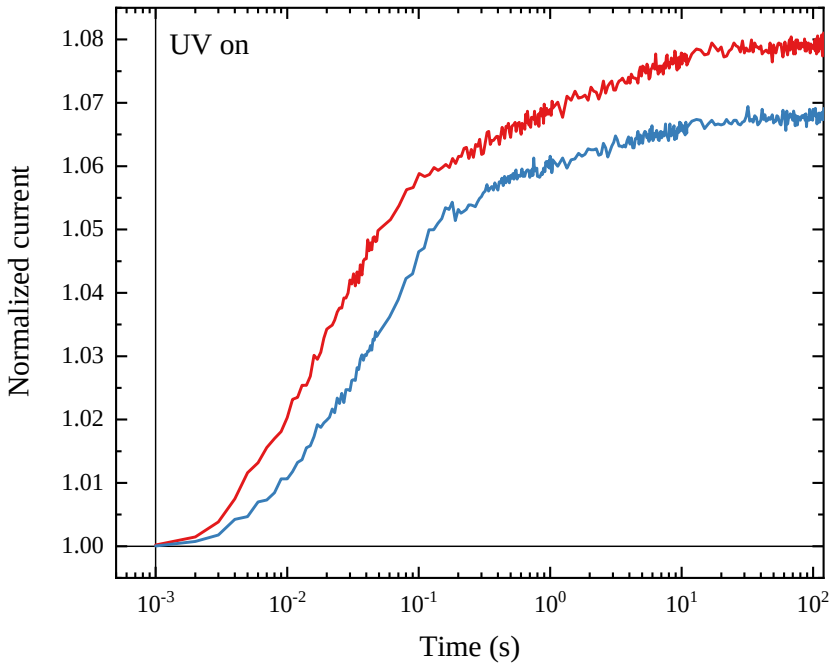

FIGURE C.3. Channel current transient following UV light illumination of 360 nm for two different TLM structures on wafer A.

APPENDIX D

SUPPLEMENTARY MEASUREMENTS FOR SURFACE-RELATED UV-INDUCED PPC

The chapter 7 showed a large discrepancy between experimental PPC effect magnitude and simulated expected buffer-related PPC effect magnitude. The PPC effect magnitude measurement was conducted as dark and UV resistance measurement of the total resistance of a 20 µm gap TLM structure. However, this measurement has a comparably small error ($\leq 10\,\%$) by incorporating the contact resistivity and not only considering the pure sheet resistivity. This leads to an underestimation of the measured UV-induced increase in channel conductivity which means that the true PPC magnitude values would actually be higher rather than lower. Therefore, accounting for the contact resistivity cannot compensate the gap between experiment and simulation. However, measuring the contact resistance might indicate large differences between samples which may account for the inconsistent differences between experiment and simulation.

Fig. D.1 show the sheet and contact resistivity measurements for the first and second sample batch. Most notably, the sheet resistivity measurement conducted by the wafer manufacturer are significantly lower, however, the wafer manufacturer used a different measurement setup. They used a non-contact eddy current-based measuring instrument on the unprocessed wafers. The contact resistivity for the first sample batch varies quite significantly between samples but this batch proved to be unreliable in general. The contact resistivity of the second sample batch showed a smaller spread between samples. Sample 1 and 3 exhibit the highest values which are in contrast to the PPC measurements because those two samples show the smallest and largest difference between experiment and simulation, respectively. A larger difference between experiment and simulation could be balanced by a smaller contact resistance leading to a smaller underestimation of the experimental value, but not vice versa which is the case here.

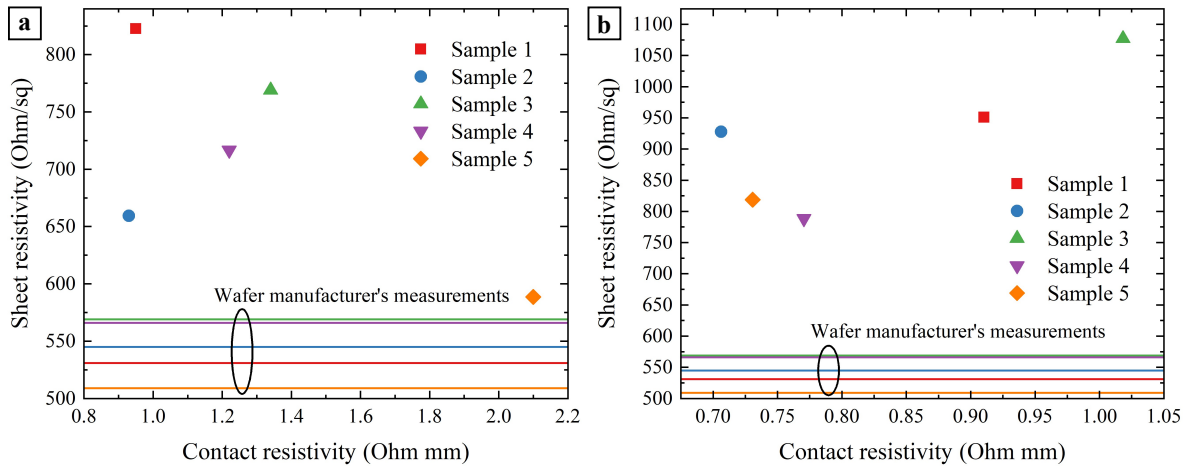

FIGURE D.1. Sheet and contact resistivity measurements of a) the first sample batch and b) the second sample batch using the entire set of different gap sizes of the TLM structure in comparison with the measurement from the wafer manufacturer using a non-contact eddy current-based method.

The KPFM measurements showed inconsistent surface potential changes between samples compared to the prediction by the PPC measurements. Fig. D.2 shows optical images of the measured TLM gaps. All samples exhibit different visual surface morphologies potentially indicating (electro-) chemical reactions which can influence KPFM measurements. Only sample 4 appears with a uniform surface, however, it is the only sample with a passivation layer on top of the AlGaN/GaN stack.

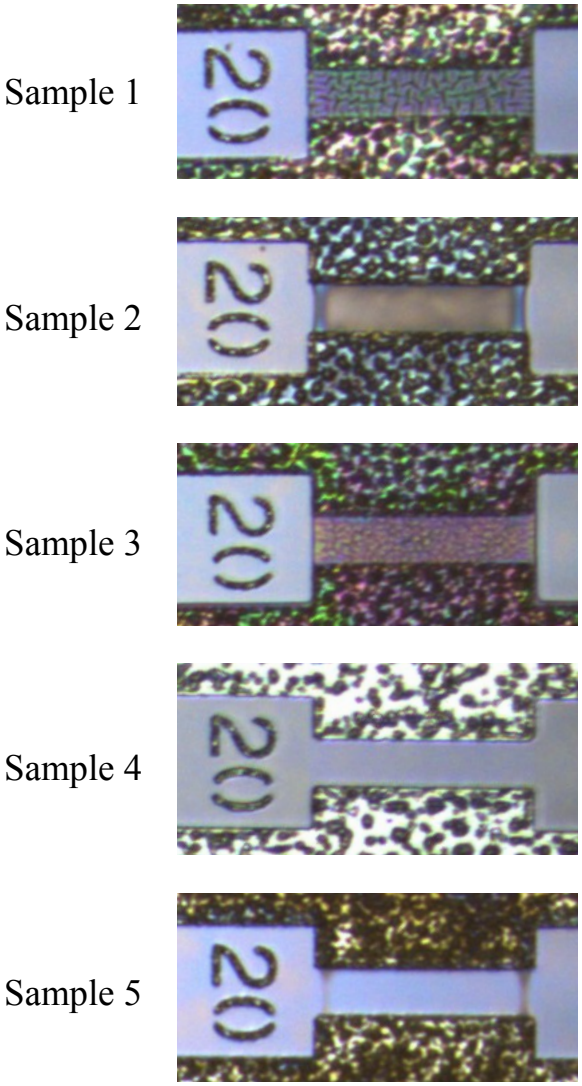

FIGURE D.2. Optical image of the measured 20 µm TLM gap during KPFM measurements of the second sample batch. Only sample 4 has a passivation layer on top of the GaN epitaxial stack.

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