BROADBAND HIGH GAIN MM-WAVE CMOS AMPLIFIER WITH COMPLEX DEVICE NEUTRALIZATION FOR 5G COMMUNICATION SYSTEM

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BROADBAND HIGH GAIN MM-WAVE CMOS AMPLIFIER WITH COMPLEX DEVICE NEUTRALIZATION FOR 5G COMMUNICATION SYSTEM

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In the Name of Allah, the Most Merciful, the Most Beneficent. Prayers and peace be upon our Prophet, Muhammad, his family, and all of his companions

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LIST OF SYMBOLS AND ABBREVIATIONS

CL	Couple Line
DUT	Device Under Test
Fmax	Maximum Operating Frequency
Ft	Transient Frequency
Gma	Maximum Available Gain
Gmax	Maximum Achievable Gain
Gms	Maximum Stable Gain
LLR	Linear, Lossless, Reciprocal
LNA	Low Noise Amplifier
MAG	Maximum Available Gain
MSG	Maximum Stable Gain
PA	Power Amplifier
RX	Receiver
TX	Transmitter
U	Unilateral Power Gain

SUMMARY

Presently, the major challenge at the device level is the lack of sufficient device power gain of commercial IC technologies at THz. In this dissertation, we will address this device-level challenge. We first characterize their THz behaviors/modelling. Then, novel circuits-aware device core designs and optimizations to boost the device-level "gain-bandwidth product" at THz are presented.

This dissertation presents a wideband power amplifier at THz frequency range. The proposed power amplifier covers the frequency range from 100 to 125 GHz, supporting the operation in the low band of the D-band.

Moreover, a novel embedding network, called a complex neutralization scheme, is presented to boost the power gain of the device for near-fmax operation. Furthermore, an in-house automation program is presented for optimum selection of the complex neutralization embedding network. The goal of this program is to maximize device Gain-BW for the available technology at target operating frequencies.

Furthermore, the proposed power amplifier is cascaded to increase the output power along with high gain. The presented work contains 3-stage complex neutralized differential blocks with output power combiner. The matching stages are optimized for low loss and wideband operation.

The proposed power amplifier is taped-out using GlobalFoundries 45nm FD-SOI CMOS process. The electromagnetic simulations for the proposed power amplifier, which is biased in class AB, demonstrate a small signal gain of 19dB at 115 GHz with k factor

more than 17. Moreover, the large signal simulations show a peak power added efficiency of 14% with a saturated output power of 12.6dBm. The proposed system has a total active area of $0.23mm^2$.

CHAPTER 1. INTRODUCTION

Recently, circuit design at THz frequencies is gaining a big momentum as it is considered a key enabler for six generation (6G) wireless communications systems. Moreover, at these frequencies, the communication system has the advantage of low latency, higher capacity, and much higher data speed [1]. This is achieved by the available wide bandwidth that can be utilized for the higher-order spectrum modulation.

The conventional receiver (RX) and the Transmitter (TX) architectures within the wireless communications system are shown pagein Figure 1. As illustrated, at the TX, the signal needs to be amplified through the power amplifier (PA). While, at the RX, the signal needs to be amplified using a low noise amplifier (LNA). This is to compensate for the larger path loss present at these frequencies and ensure sufficient link budget within the communication chain.

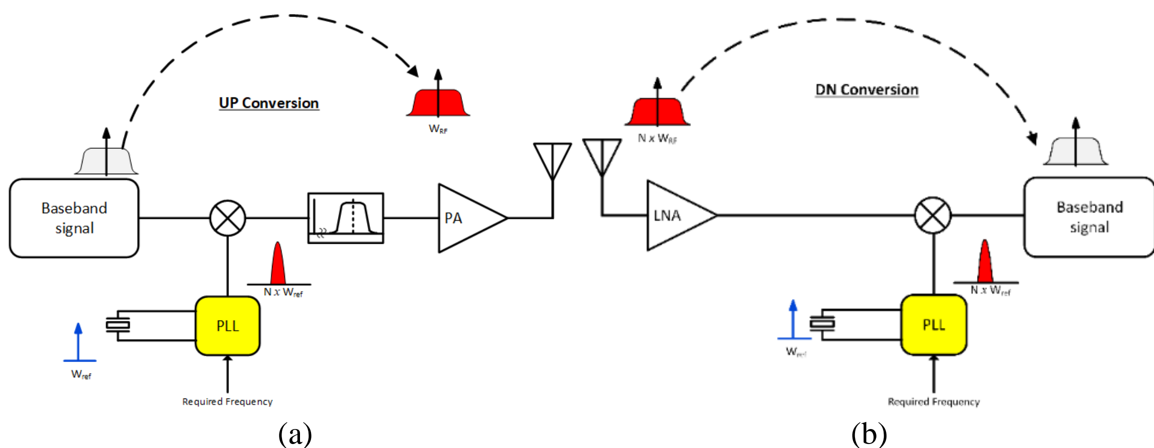


Figure 1: Simple architecture of (a) RF Transmitter (b) RF Receiver for wireless communication system [2].

However, at the THz frequencies, radio frequency (RF) frontend circuitry design has unique challenges for achieving high gain, wide bandwidth, while achieving high efficiency [2].

Signal amplification at submillimeter-wave and THz frequencies is one of the most challenging design aspects in transceiver design because these frequencies are close to $fmax$ of the transistor device which reduces the available gain from the active design. Also, the matching network losses at the input and the output increase as a function of frequency, reducing the verall amplifier gain even further.

To solve this issue, different design methodologies are taken to unilateralize the active transistor, to improve the stability and to increase the power gain [3-4]. However, the unilateralized device performance degrades near fmax of the device. To, handle the problem of power gain at $fmax$, some designs use appropriate embedding networks to boost the gain [5]. Also, to address the wide band operation, a complex neutralization capacitor is used to cancel out the cgd capacitance and achieve wideband operation [6].

In fact, transistor devices are the elemental blocks for circuits and systems. This is particularly critical at THz, as devices exhibit limited cutoff frequencies ($fmax/ft$), low power gain, and vulnerability to parasitics, rendering most THz circuits device limited. Figure 2 summarizes PAs above 100GHz. As depicted, a degradation trend of output power vs. frequency that follows the device Johnson's limit.

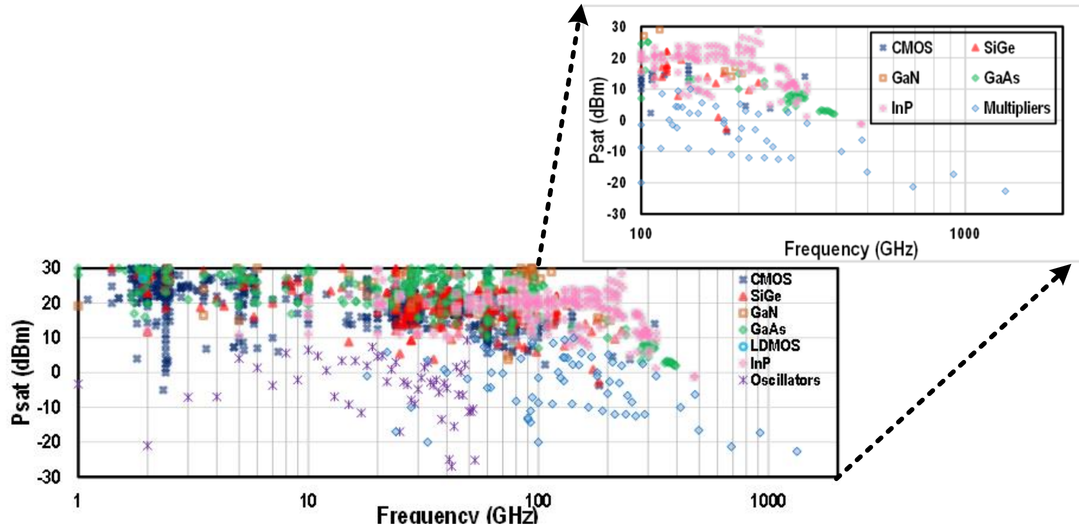


Figure 2: Recently Reported power amplifiers (PAs) output power vs. frequency for different technologies [7].

Accordingly, given the requirements and challenges for designing power amplifiers at the THz bands (0.1-10THz), we propose an ultra-wideband power amplifier with a power gain higher than the unilateral gain of the device. Also, a systematic design approach is presented to choose the optimum embedding network values for the targeted frequency band.

This dissertation is organized as follows: CHAPTER 2 discusses the proposed technique and its design approach. CHAPTER 3 presents the system level simulations. Finally, chapter 4 concludes the work.

CHAPTER 2. PROPOSED BROADBAND HIGH GAIN AMPLIFIER

One of the most challenging design aspects in any transceiver design is signal amplification as it improves the signal-to-noise ratio and data rate as well as the transceiver range. However, signal amplification at mm-Wave and THz frequencies, is challenging. Since these frequencies are very close to the device $fmax$, where the available gain from the active device is low. In addition, there are high losses of input and output matching networks. Consequently, at these frequencies, intelligent techniques need to be introduced to enhance the device power.

2.1 Gain Boosting Techniques

In this section, different gain boosting techniques are presented and compared to one another.

2.1.1 Power Gain Definitions

This section will review several power gain definitions for a general two-port network, as shown in Figure 3. First, the maximum available gain G_{ma}, otherwise known as MAG, is the ratio of available power at the load to the available at the source [3]:

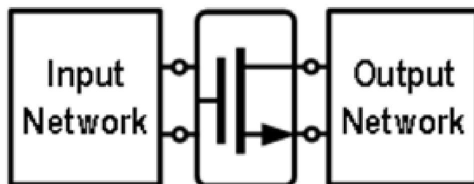


Figure 3. A general two-port network with input and output outmatching network.

$$G_{ma} = \frac{|Y_{21}|}{|Y_{12}|}\left(K - \sqrt{K^2 - 1}\right) \tag{2.1}$$

where K refers to the Rollet's stability factor $K \ that \ can \ be \ defined \ as$[8]:

$$K = \frac{2\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|} \tag{2.2}$$

where Y_{21}, Y_{21} are the Y parameters of the 2-port network.

In fact, G_{ma} is the power gain of the two-port network when both the input and output ports are conjugately matched. From (2.1), G_{ma} is undefined when $K < 1$. This is because bi-conjugate matching only exists when the two-port network is unconditionally stable ($K \geq 1$). When the network is not unconditionally stable, a useful power gain definition is the maximum stable gain G_{ms}[9], sometimes called MSG, which is simply the maximum transducer gain in (2.1) with $K = 1$:

$$G_{ms} = \frac{|Y_{21}|}{|Y_{12}|} = A \tag{2.3}$$

Another useful characterization for any two-port network is Mason's invariant U [10]:

$$U = \frac{|Y_{21} - Y_{12}|^2}{4[\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{12})\text{Re}(Y_{21})]} \tag{2.4}$$

where U reflects a device's intrinsic property that will not be altered under any linear, lossless, reciprocal (LLR) embedding network. It turns out that U is equivalent to the power

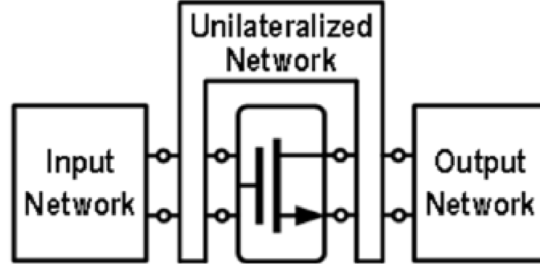


Figure 4: A general two-port network being unilateralized by a linear, lossless, reciprocal (LLR) embedding network. The power gain in this case is equal to Mason's invariant U.

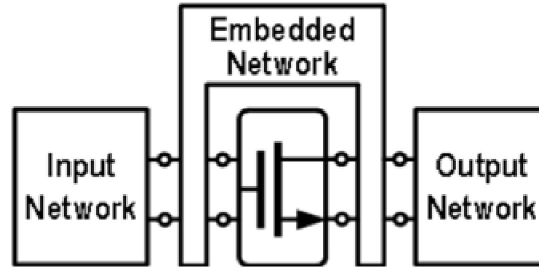


Figure 5: General two-port network with an LLR embedding network. The maximum $\boldsymbol{G_{ma}}$ across all embedding network choices is defined as $\boldsymbol{G_{max}}$

gain when the two-port is unilateralized with an LLR network, as shown in Figure 4.

Furthermore, the maximum achievable gain of the device G_{max}, is defined as the maximum of maximum available gain across all LLR embedding networks. It is the highest power gain that can be achieved by the active two-port network under proper choice of LLR embedding network and biconjugate matching of input and output Figure 5.

$$G_{max} = (2U - 1) + 2\sqrt{U(U - 1)} \approx 4U \tag{2.5}$$

2.1.2 Device Power Gain Simulations

Figure 6 shows the maximum available power gain simulation of a single NMOS transistor device in GlobalFoundries 45nm SOI process. The stability K-factor is also

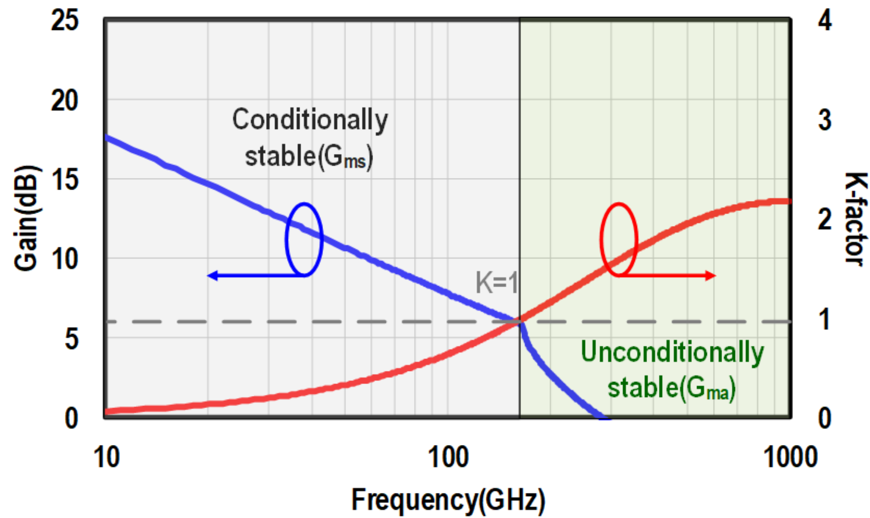


Figure 6: Maximum available power gain of NFET in GlobalFoundries 45nm CMOS SOI process.

overlayed with the power gain, G_{ms} , plot. As depicted, the device becomes unconditionally stable after around 200GHz. Thus, embedding network is required to stabilize device for power generation below 200GHz. It should be noted that, at mm-Wave frequencies and above, the layout of the device should be extracted to capture the parasitics of the internal gate, source, and drain connections.

Figure 7 shows the maximum available power gain of the same device with its unilaterized power gain, U, and its maximum achievable gain, G_{max}. Consistent with theory, the maximum achievable gain is around 6dB higher than U. At low frequencies, U is significantly higher than the intrinsic device. One thing worth noting is that as the device operates in the near-fmax region, U is no longer higher than the intrinsic gain of the device. Consequently, embedding a unilateralization network to boost power gain is no longer useful at very high frequencies (near fmax). It's worth noting that, both U and G_{max} curves intersect with the G_{ma}/G_{ms} curve at the point of 0dB gain, which is the *fmax* of the

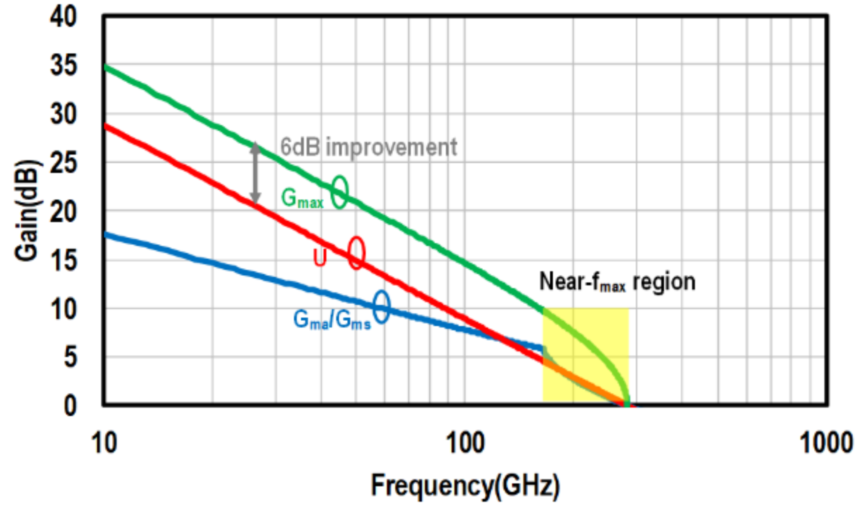


Figure 7: Gain simulations of NFET in GlobalFoundries 45nm CMOS SOI process.

transistor as indicated in in Figure 7.

2.1.3 General Solution to reach G_{max}

It can be shown that the maximum available power gain of a two-port network (device) can be written as a function of its U and A as [3]:

$$\frac{U}{G_{ma}} = \left(\mathrm{Re}\left(\frac{U}{A}\right) - \frac{U}{G_{ma}}\right)^2 + \left(\mathrm{Im}\left(\frac{U}{A}\right)\right)^2 \tag{2.6}$$

Since U is a constant, the goal is to modify A to reach the maximum achievable gain in use of embedding network to the two-port. If we take the real and imaginary part of U/A as the x and y axis respectively, equation (2.6) describes a group of equal-gain circles centered at $(U/G_{ma}\ , 0)$, each with radius $\sqrt{U/G_{ma}}$. This is shown in Figure 8.

Imposing the restriction that the device must be unconditionally stable gives the

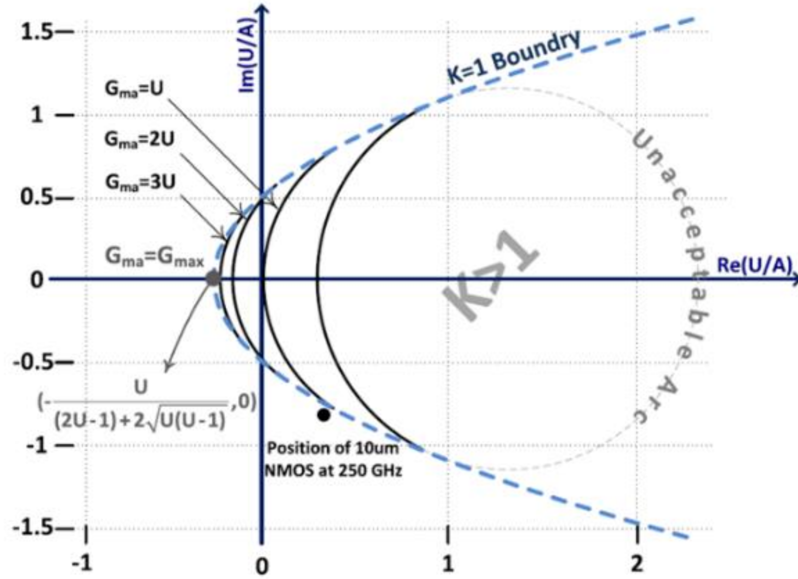


Figure 8: Gain plane definitions with equal-gain circles [3].

following boundary equation when $K = 1$ (assume $|A| \gg 1$):

$$\frac{1}{4} + \mathrm{Re}\left(\frac{U}{A}\right) = \left(\mathrm{Im}\left(\frac{U}{A}\right)\right)^2 \tag{2.7}$$

Equation (2.7) is a horizontal parabola with the inside and outside regions corresponding to $K > 1$ and $K < 1$ respectively. Figure 8 also shows this $K = 1$ boundary. As G_{ma} increases, the equal-gain arcs move to the left in the gain plane, and finally converges into a single point at $\left(-\frac{U}{(2U-1)+2\sqrt{U(U-1)}}, 0\right)$. This point corresponds to the maximum achievable gain where $|A| = G_{max}$ and $\angle A = 180°$.

As mentioned above, the embedding network will change A of the whole two-port structure, such that G_{ma} can approach G_{max}. In the gain plane, this embedding corresponds to a movement in the gain plane.

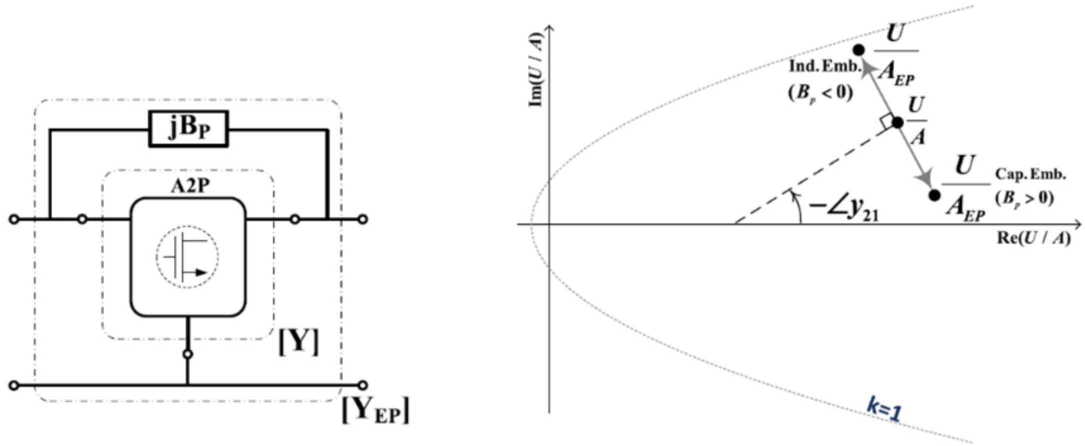


Figure 9: Gain plane movement by a parallel reactive embedding element [3]. For capacitive element, the relative movement is to the lower-right. For inductive element, the relative movement is to upper left.

In order to reach G_{max} the proper embedding network should be selected. For instance, as shown in Figure 9, the movement in gain plane utilizing parallel reactive element embedding. Therefore, with proper choice of the embedding network, the G_{ma} of the intrinsic device can be boosted to G_{max} by a series of movements in the gain plane.

In the following section of the thesis, we experimented with several embedding networks in simulation and proposed a wideband gain boosting technique using ideal LLR embedding network. We chose the thin-oxide NFET device in GlobalFoundries 45nm CMOS SOI process as the device under test. The transistor has width of 30μm and length of 40nm. Widely used in CMOS power amplifier cells, the device is in common-source configuration as shown in Figure 10 (a), while the corresponding layout of the device is presented in Figure 10 (b).

Moreover, Figure 10 (c) shows the maximum available power gain simulation of the device using the provided schematic model and the layout-extracted model respectively

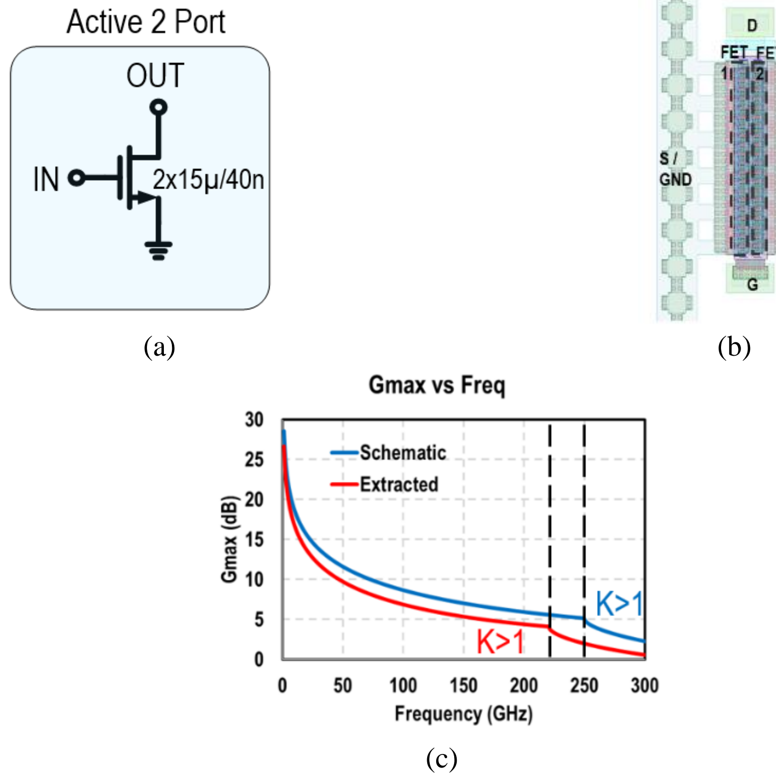


Figure 10: Active two port transistor (a) Schematic view (b) Layout view (c) Device Power Gain simulations in GlobalFoundries 45nm CMOS SOI process for schematic and extracted view.

As indicated, the extracted device has lower gain and becomes unconditionally stable at a lower frequency than the schematic model. That is due to the additional parasitics from the layout. Therefore, for a fair comparison between different embedding networks, the extracted device was used in simulation for more accurate modelling of device parasitics.

Also, to adhere to common terminologies, we use G_{max} to represent the maximum available power gain instead of maximum achievable gain discussed in the previous section. Alternatively, the maximum achievable gain will be represented by the $4U$ approximation and explicitly stated.

(a) Single inductor element-based embedding

One common embedding element is an inductor placed across the gate and drain of the inductor, as shown in Figure 11 (a). This will resonate out the parasitic capacitance, C_{gd}, of the device and boost the gain.

Figure 11 (b) shows the schematic of the simulation setup. As indicated, large inductors and capacitors are used as DC feed and DC block respectively. The DC block capacitor between the gate and drain is impractical for implementation. Therefore, in actual

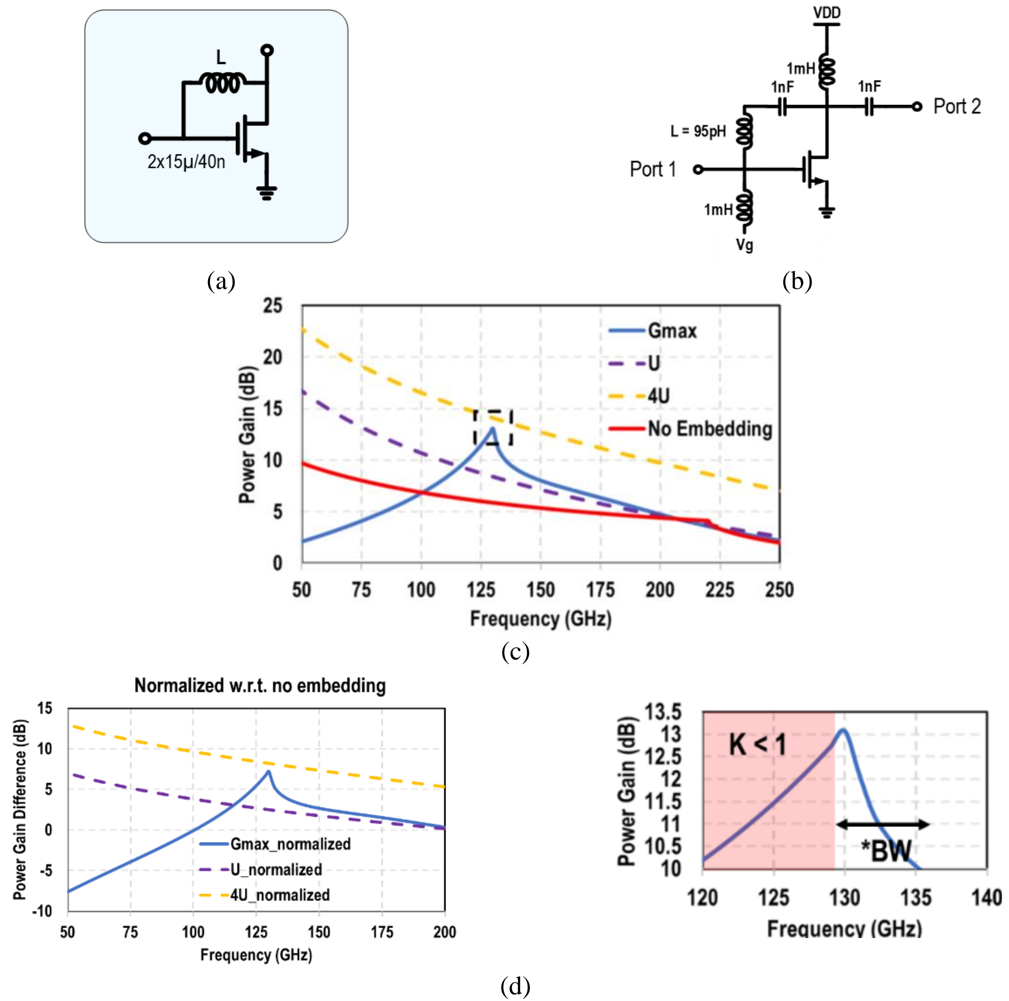


Figure 11: Single ended inductor embedding (a) Conceptual block diagram (b) Schematic view (c) Device Power Gain simulations (d) Normalized device power gain simulations w.r.t no embedding

amplifier implementation of this inductor embedding, the device needs to be biased in diode-connected fashion, which reduces the design degree of freedoms. Figure 11 (c) shows the power gain of this embedding network. As illustrated, the gain is boosted to near $4U$ at around 127GHz. However, after this frequency, the gain drops sharply. The inset in Figure 11 (c) shows the zoomed in view of the gain peak. If unconditional stability is taken into consideration, this embedding network choice exhibits a 3dB stable bandwidth of 6 GHz, as depicted in Figure 11 (d). Also, Figure 11 (d) plots the relative gain with respect to the intrinsic device gain.

Figure 12 shows the gain plane trajectory across frequency for the single inductor embedding technique. The data points of the intrinsic device are also included for reference. As frequency increases, the device moves further inward towards the stable region, which is consistent with the decreasing gain behavior. Ideally, gain trajectory for the embedded device should all land on the $4U$ target points. However, if the trajectory can follow the same high equal-gain arcs, desirable wideband gain boosting can be achieved.

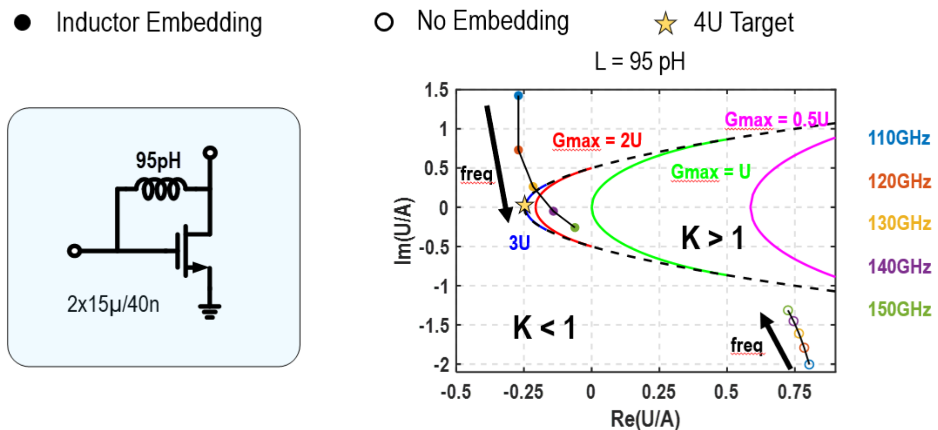


Figure 12: Single-ended one inductor embedding Gain Plane

(b) Three-inductor-elements based embedding

The second embedding network is the extension of the first technique, where two additional inductors are added to the drain and gate (Fig. 12 (a)). The simulated power gain is shown in Fig. 12 (b). The result is similar to that of the single inductor element embedding. As shown in the inset of Fig. 12 (b), the gain peaks to a point near the

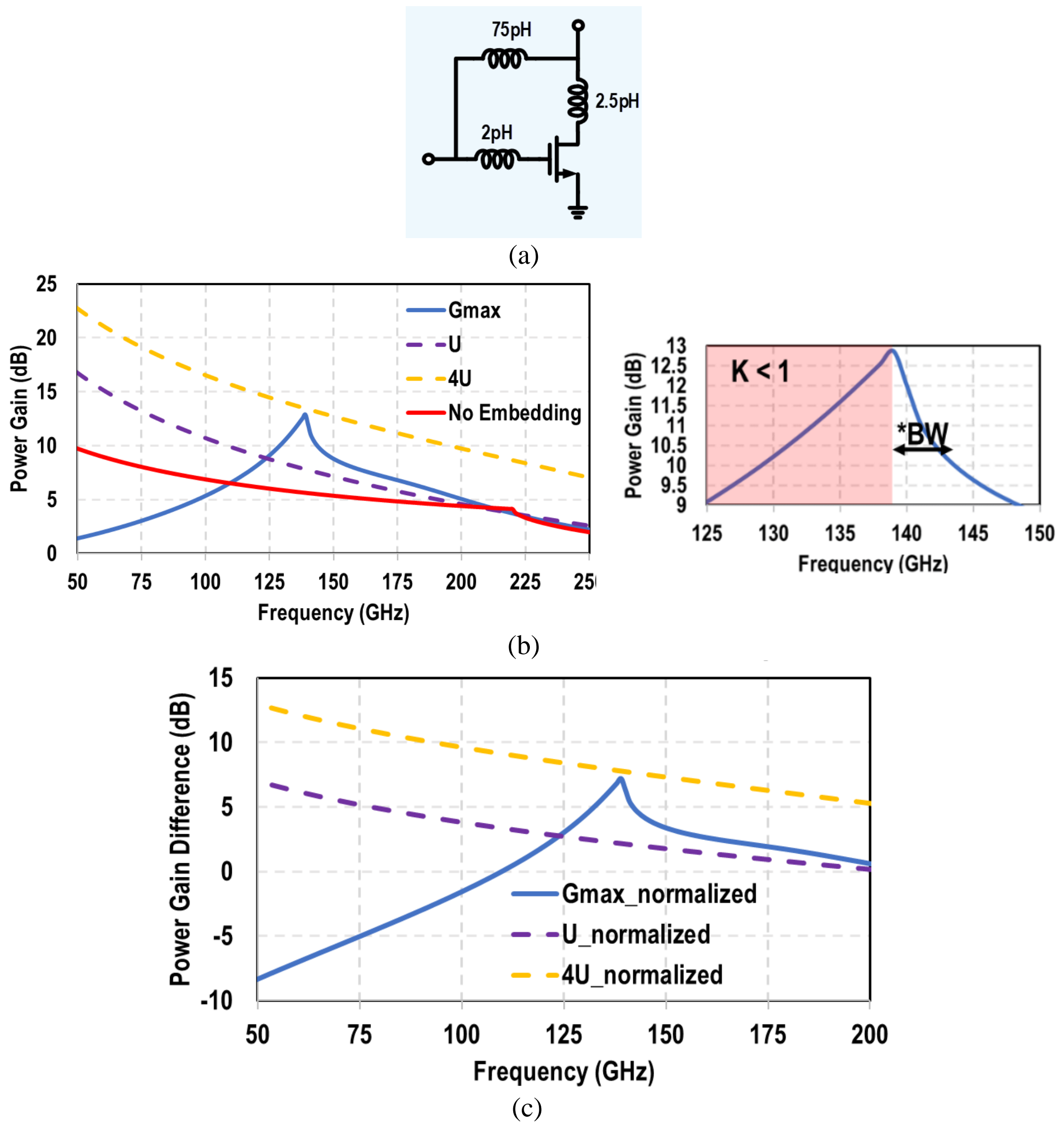


Figure 13: Single-ended 3-element inductor (a) schematic view (b) Device power gain simulations (c) Normalized device power gain simulations w.r.t no embedding

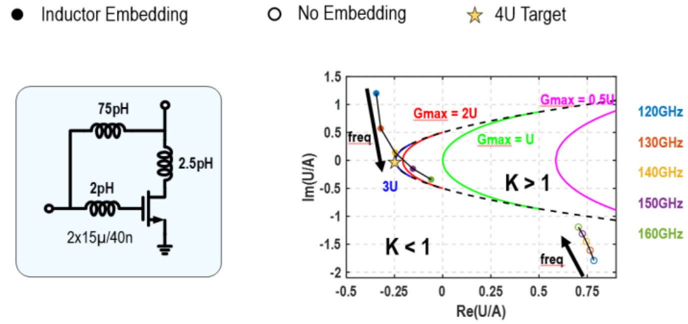


Figure 14: Single-ended 3-element inductor embedding Gain Plane

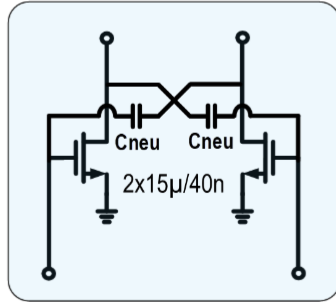
maximum achievable value and then sharply drops. The 3dB stable bandwidth is around 5 GHz in this case.

Figure 14 shows the gain plane trajectory of this embedding network. Same as the single inductor embedding, the two-port quickly moves inward to the right, which accounts for the narrowband simulated power gain.

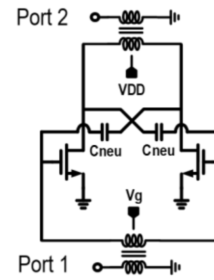
(c) Differential capacitor neutralization

The most common embedding technique used in differential PAs is capacitive neutralization, shown in Figure 15 (a). This technique can provide wideband cancellation of transistor parasitic C_{gd} because of the 180° phase shift between the two branches. Figure 15 (b) shows the simulation setup where ideal baluns are used to convert differential to single-ended two-port.

The gate and drain DC biases are fed through the center tap of the baluns. Accordingly, the limitation of the same bias for both the drain and the source of the single inductor element-based embedding is avoided.



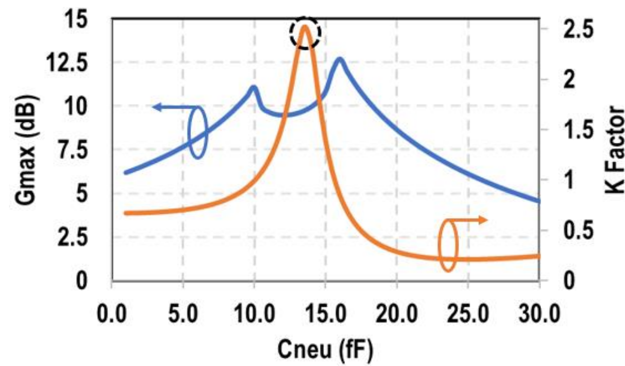
(a)



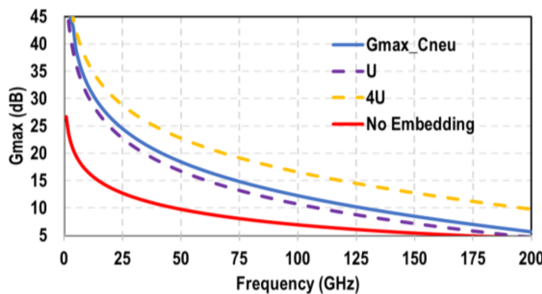
(b)

Figure 15: (a) Ideal Capacitor Neutralization (b) Introduce biasing to the ideal capacitor neutralization

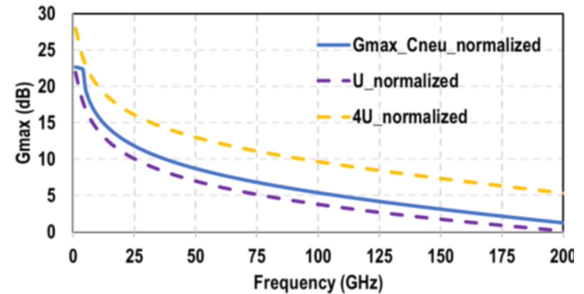
Figure 16 (a) shows the design choice of the neutralization capacitor for the chosen DUT. The 13.5fF capacitance is chosen at the valley of the volcano-shaped maximum available gain to ensure stability. Figure 16 (b) shows the simulated power gain.



(a)



(b)



(c)

Figure 16: Differential capacitor neutralization (a) Choice of capacitance value (b) Device power gain simulations (c) Normalized device power gain simulations w.r.t no embedding

As indicated, the cancellation of C_{gd} eliminates most of the feedback from the drain to the gate. Thus, the capacitor neutralization is essentially a unilateralization network. Accordingly, the simulated G_{max} is approximately U.

As depicted in Figure 16 (c), the differential capacitor neutralization device gain is large compared to the intrinsic device gain. Despite the capacitor neutralization device broadband characteristics, it cannot provide significant gain boosting at high frequencies as mentioned before.

Figure 17 shows the gain plane trajectory across frequency for differential capacitor neutralization, which verifies its broadband feature of capacitor neutralization as overall network hardly shifts across frequency.

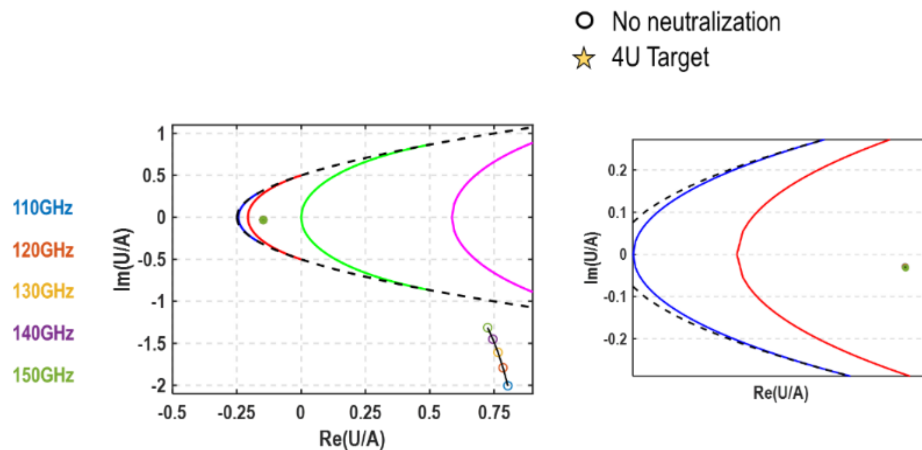


Figure 17: Differential capacitor neutralization gain plane trajectory. The inset shows the zoomed-in view of the box area.

2.1.4 Proposed Complex Neutralization Network

As mentioned above, single-ended inductive embedding can boost the gain up to $4U$, but suffers from narrow bandwidth. On the other hand, the capacitor neutralization device is broadband. However, using differential capacitor neutralization alone will provide a limited gain at high frequencies. Moreover, this broadband neutralization is not practical at high mmWave frequencies (D band and beyond) due to routing parasitics.

Therefore, to combine the advantage of both techniques, we propose the following differential complex neutralization network shown in Figure 18. Essentially, we leverage the routing parasitics together with the neutralization capacitor to provide wideband gain boosting. The gate and drain inductors L_g and L_d are lumped models for the parasitic inductances of the routing. Our proposed technique can also offer flexible design choices which will be illustrated in detail later.

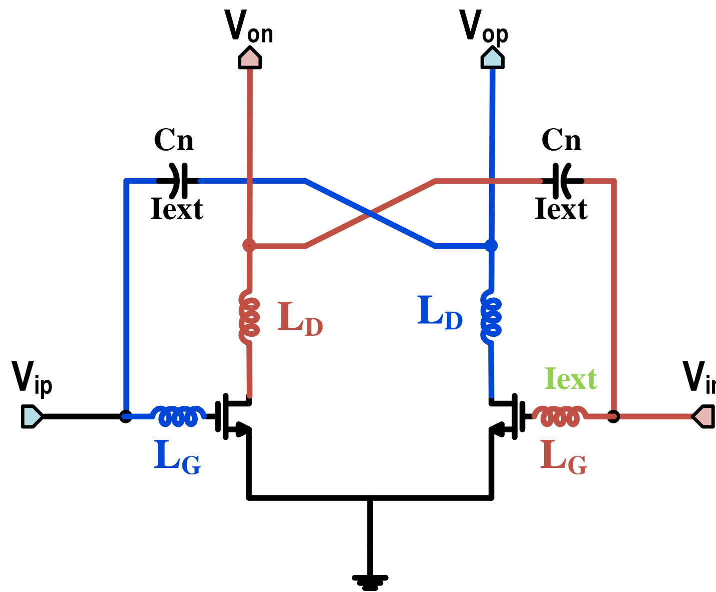
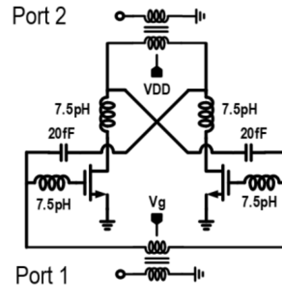
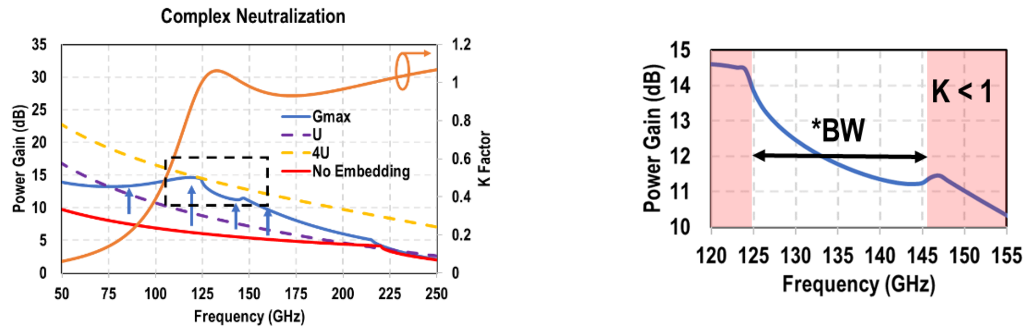


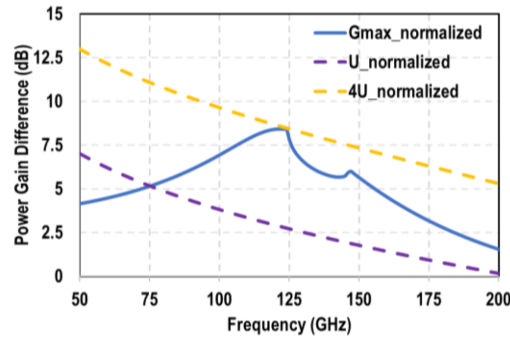
Figure 18: Proposed differential complex neutralization network, using CMOS device as an example. The finite quality factors of passive elements are modelled.



(a)



(b)

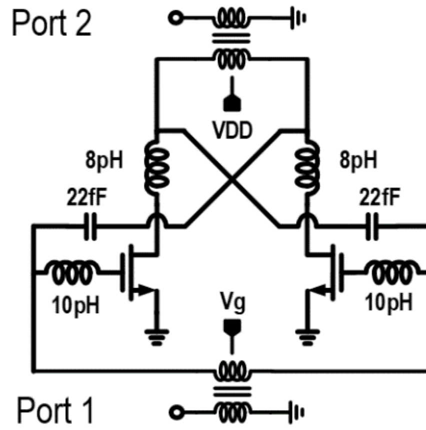


(c)

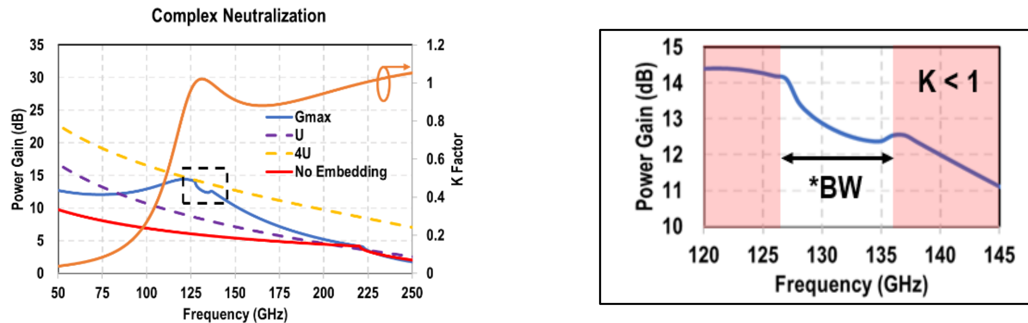
Figure 19: Differential complex neutralization network design example #1. (a) schematic view (b) Device power gain simulations (c) Normalized device power gain simulations w.r.t no embedding

Figure 19 (a) shows the schematic of the first design example of complex neutralization ideal network, with the simulated power gain shown in Figure 19 (b). The G_{max} of the proposed network can reach near *4U* values at two frequencies, thus providing a wideband gain enhancement. As shown in the inset of Figure 19 (b), the 3dB stable bandwidth is around 21GHz.

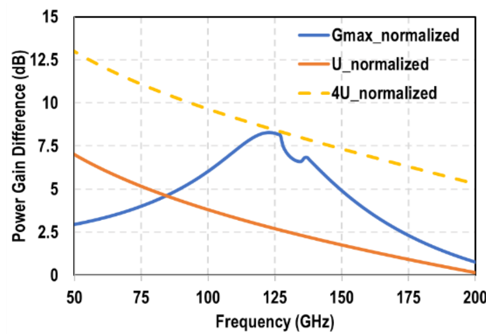
Figure 20 (a) shows the second design example. As depicted, it has narrower bandwidth, but with higher overall gain within the bandwidth compared to the first design example (Figure 20 (b) and (c)).



(a)



(b)



(c)

Figure 20: Differential complex neutralization network design example #2. (a) schematic view (b) Device power gain simulations (c) Normalized device power gain simulations w.r.t no embedding

2.2 System Design Methodology

The last section illustrated the flexibility of the proposed complex neutralization amplifier. However, it raised a question about the choices of the embedding network at the target frequency band. Moreover, the non-idealities of the embedding network, including the quality factor, self-resonance, and mutual inductance, should be taken into consideration

Furthermore, accurate device modelling above 150GHz is typically not provided by foundries, which complicates the THz electronics research. Accordingly, parasitics-aware models for the transistor should be also used to support THz circuit design.

Ultimately, we propose a new differential complex neutralization network to attain a radical wideband device gain boosting. Essentially, we leverage and engineer the routing inductive parasitics L_g, L_d, and L_c with the feedback capacitors C_{neut} to form a high-order neutralization network and enable wideband gain boosting. It is worth noting that device gate/base and drain/collector now can be independently biased for optimum device operation. In the following subsection, the analysis of the proposed circuit is developed.

2.2.1 Theoretical Analysis

The proposed complex neutralization amplifier mainly consists of an NFET device in a common source configuration, gate inductance, drain inductance, and a neutralized capacitor. In order to describe this system with equations, for the optimization task, the differential amplifier should be represented using a half circuit model. Knowing the basics of the differential amplifier [2], the half circuit model can be developed for the proposed

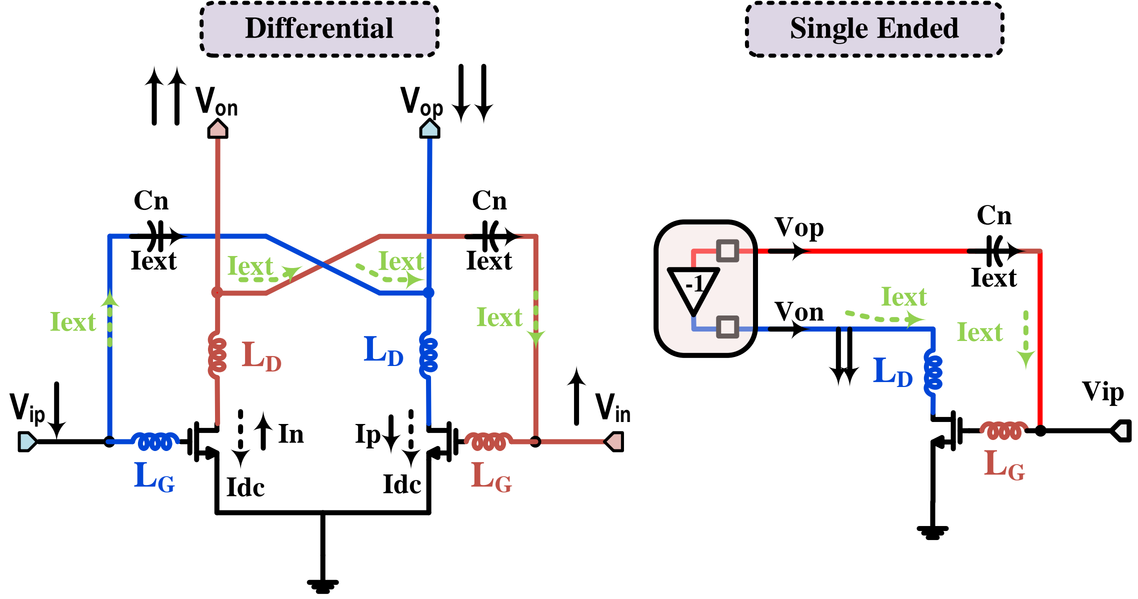


Figure 21: Conversion of the Proposed differential complex neutralization network to half circuit model.

complex neutralization scheme, as shown in Figure 21. As indicated, the half circuit model contains a negative gain in the feedback, to mimic the 180-phase difference between the Vop, and Von. This will change the behavior of the capacitor similar to the conventional capacitor neutralization.

Figure 22 shows the equivalent Y parameters of the half circuit model of the proposed complex neutralization amplifier. As depicted, the position of the gain (negative one) does not affect the Y parameters. Moreover, the device is represented with its Y-parameters. Similar, the embedding network is modelled with the corresponding Y parameters.

The equivalent Y parameters of the whole system are as follows:

$$Y_{11} = \left[\frac{y_{11_m} y_{22_m} y_{11_{z1}} - y_{12_m} y_{21_m} y_{11_{z1}} + y_{22_m} y_{22_{z1}} y_{11_{z1}} - y_{22_m} y_{21_{z1}} y_{12_{z1}}}{(y_{22_m} + y_{11_{z2}})(y_{11_m} + y_{22_{z1}}) - (y_{12_m} y_{21_m})} \dots \right. \\ \left. + \frac{y_{11_m} y_{11_{z1}} y_{11_{z2}} + y_{11_{z1}} y_{22_{z1}} y_{11_{z2}} - y_{11_{z2}} y_{12_{z1}} y_{21_{z1}}}{(y_{22_m} + y_{11_{z2}})(y_{11_m} + y_{22_{z1}}) - (y_{12_m} y_{21_m})}\right] + y_{11_{z3}} \quad (2.8)$$

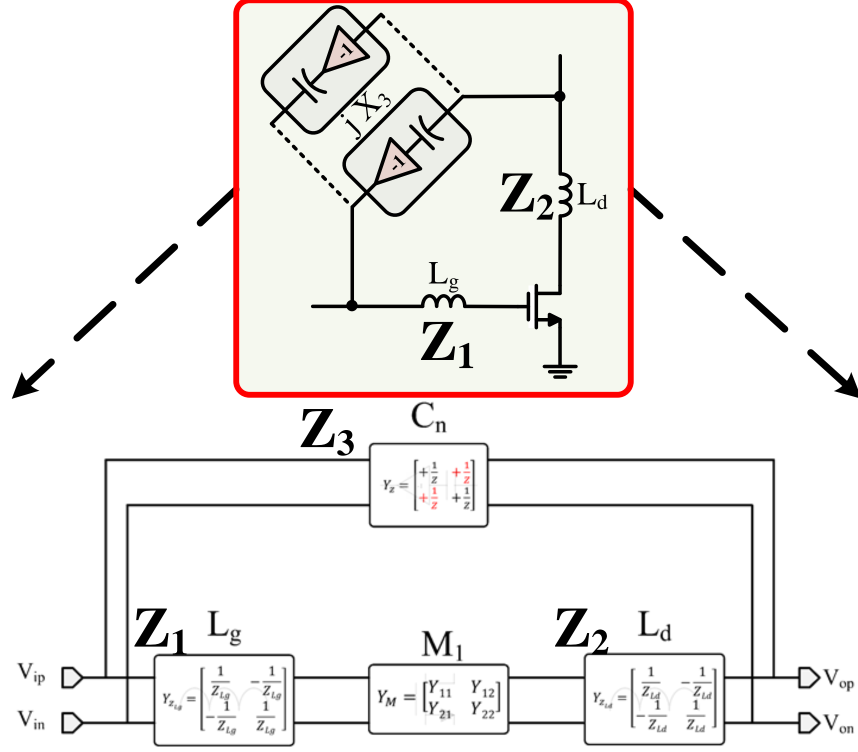


Figure 22: The developed Y parameters of the half circuit model of the proposed complex neutralization circuit.

$$Y_{22} = \left[\frac{y_{11_m}\, y_{22_m}\, y_{22_{z2}} - y_{12_m}\, y_{21_m}\, y_{22_{z2}} + y_{22_m}\, y_{22_{z1}}\, y_{22_{z2}} - y_{11_m}\, y_{21_{z2}}\, y_{12_{z2}}}{(y_{22_m} + y_{11_{z2}})(y_{11_m} + y_{22_{z1}}) - (y_{12_m}\, y_{21_m})} \cdots \right.$$
$$\left. + \frac{y_{11_m}\, y_{11_{z2}}\, y_{22_{z2}} + y_{11_{z2}}\, y_{22_{z1}}\, y_{22_{z2}} - y_{22_{z1}}\, y_{12_{z2}}\, y_{21_{z2}}}{(y_{22_m} + y_{11_{z2}})(y_{11_m} + y_{22_{z1}}) - (y_{12_m}\, y_{21_m})}\right] + y_{22_{z3}} \tag{2.9}$$

$$Y_{21} = \left[\frac{y_{21_m}\, y_{21_{z_1}}\, y_{21_{z2}}}{(y_{22_m} + y_{11_{z2}})(y_{11_m} + y_{22_{z1}}) - (y_{12_m}\, y_{21_m})}\right] + y_{21_{z3}} \tag{2.10}$$

$$Y_{12} = \left[\frac{y_{12_m}\, y_{12_{z_1}}\, y_{12_{z2}}}{(y_{22_m} + y_{11_{z2}})(y_{11_m} + y_{22_{z1}}) - (y_{12_m}\, y_{21_m})}\right] + y_{12_{z3}} \tag{2.11}$$

Then, the system can be presented as a 2-port network. Consequently, we can define the different power gain equations described in (2.1)-(2.5) using these Y parameters. Now, we have equations that describes the gain of the whole system based on the embedding network.

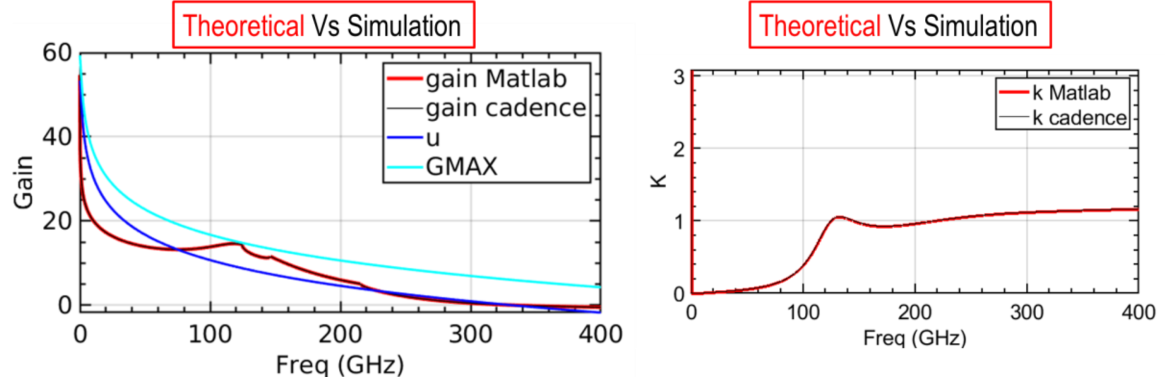


Figure 23: Device power gain simulations for design example #1 using the equations (red) and CADENCE (black).

As a proof of concept, these equations are used in MATLAB to describe the system for the design example #1, presented in section 2.1.4,18 and compare the results with the previous simulation results from CADENCE, as shown in Figure 23. As depicted, the theoretical equation results perfectly match CADENCE simulation results.

Given the above, we have equations that fully describe the proposed complex neutralization amplifier. For further understanding of the effect of each element in the embedding network, a one-by-one parametric sweep of each element of the embedding network is simulated while maintaining the other two elements fixed.

Figure 24 shows the gain plane trajectory of this design, together with a parametric sweep of Cneu of the embedding elements while maintaining the other two fixed at different frequency values. As depicted, the trajectory with the frequency for all the curves crosses first the $K = 1$ boundary, then closely follows one of the gain circles until moving out of the $K = 1$ boundary. Sweeping the gate inductance, L_g, and drain inductance, L_d, is shown in Figure 25 and Figure 26 respectively. As indicated, increasing L_g, and decreasing L_d push the G_{max} to the target, 4U. While the neutralization capacitor has a sweet point to

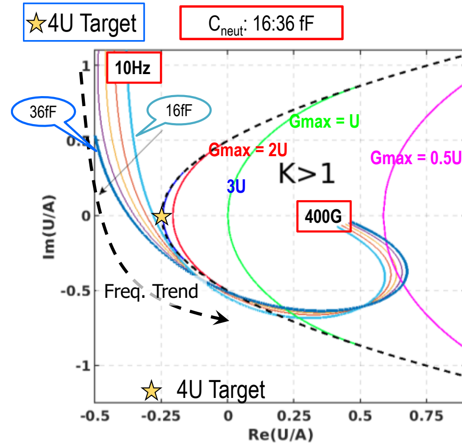


Figure 24: Differential complex neutralization network design example #1 gain plane trajectory, while sweeping Cneu with fixed gate and drain inductance, while sweeps frequency.

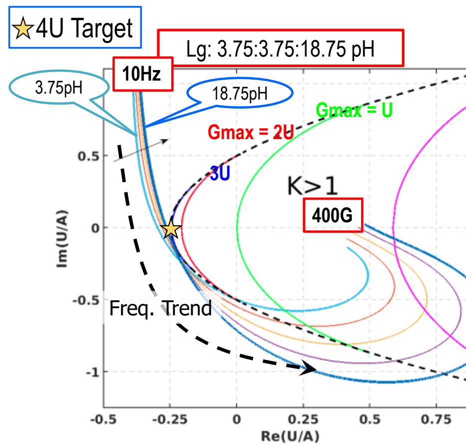


Figure 25: Differential complex neutralization network design example #1 gain plane trajectory, while sweeping Lg with fixed Ld and Cneu.

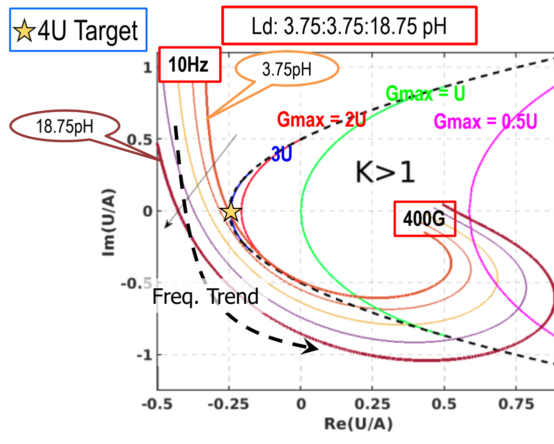


Figure 26: Differential complex neutralization network design example #1 gain plane trajectory, while sweeping Ld with fixed Lg and Cneu.

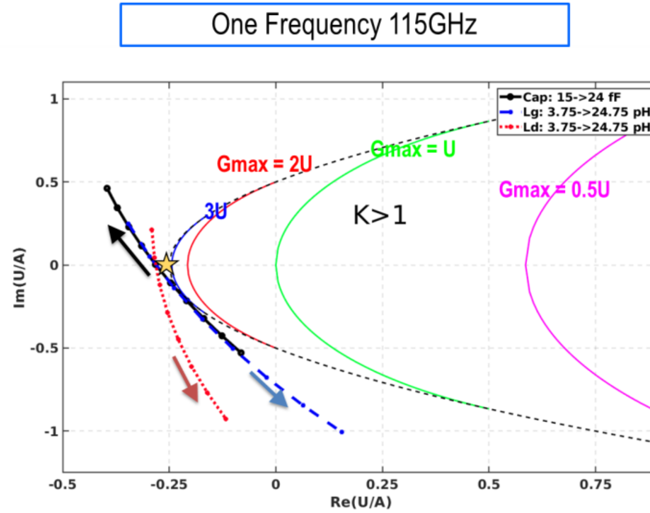


Figure 27: Differential complex neutralization network design example #1 gain plane trajectory for all the embedding networks, at a frequency of 115GHz.

approach the target gain.

Moreover, the gain plane trajectory for all the embedding networks, at one frequency of 115GHz is shown in Figure 27.

2.2.2 Optimum Embedding Network design

As shown previously, there are multiple solutions to reach the target, 4U. Therefore, we need to differentiate between these solutions and choose the optimum one in terms of optimization goals. Also, as mentioned before, the choices of the embedding network parameters should be automated in a systematic way to reduce the trials.

First, a design automation program is used to collect all the possible solutions for the target operating frequencies, which is selected by the end user, as shown in Figure 28.

Furthermore, a new device-level 3dB BW can be defined as the BW, over which the device gain exceeds *2U*, i.e., 3dB drop from the theoretically maximum device gain of *4U*. A device Gain-BW product can be formulated as the device power gain integrated over

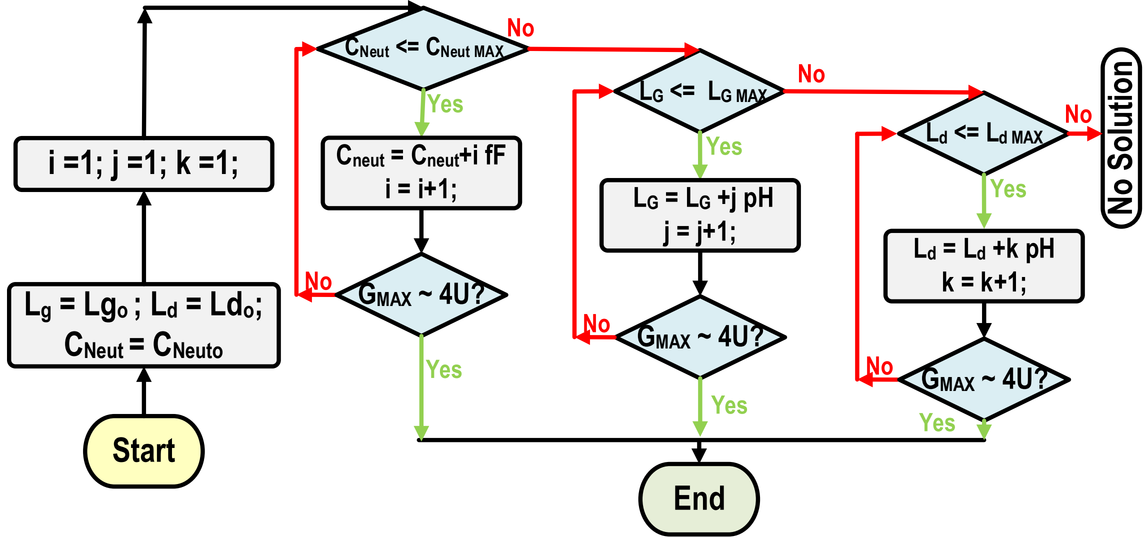


Figure 28: Program for collecting all possible solutions for the proposed complex neutralization network at the target operating frequencies.

this 3dB BW. This device Gain-BW can be used as the optimization goal for the gain boosting techniques.

Consequently, an in-house design automation program, Appendix A, has been developed to maximize the device Gain-BW using complex neutralization for given device technologies and target operating frequencies, as shown in Figure 29. This program will be used in the project to optimize devices with complex neutralization to achieve maximum Gain-BW based on the previous definition.

The proposed program is used to achieve the maximum Gain-BW under the same bias conditions of design example #1, which was presented in 2.1.4. The comparison is shown in Figure 30. As illustrated, at the same frequency, both G_{max} curves provide almost the same peak gain. However, the second curve provides around 25% higher bandwidth. Moreover, the second curve provides the optimum Gain-BW, under the new definition.

Figure 29: In-house program for optimum complex neutralization network design to maximize device Gain-BW for given technologies at target operating frequencies. The passive elements quality factors are included in the optimization.

➢ Design Example #1

Parameter	Value
Lg	7.5pH
Ld	7.5pH
Cn	20fF

➢ Best BW: 2U Crossing

Parameter	Value
Lg	5.25pH
Ld	7.25pH
Cn	18.5 fF

Figure 30: Comparison between the power gain for the design example #1 and the chosen embedding network from the in-house optimization program.

It's worth mentioning that, in order to make the program more reliable, the quality factors of the embedding network should be included in the program. Meanwhile, at the THz frequencies, the metal traces that connect the capacitor with the drain and the gate of the NFET device should be modelled. Based on the frequency of operation, these traces can be modelled as inductors or transmission line. The proposed schematic with these updates is shown in Figure 31.

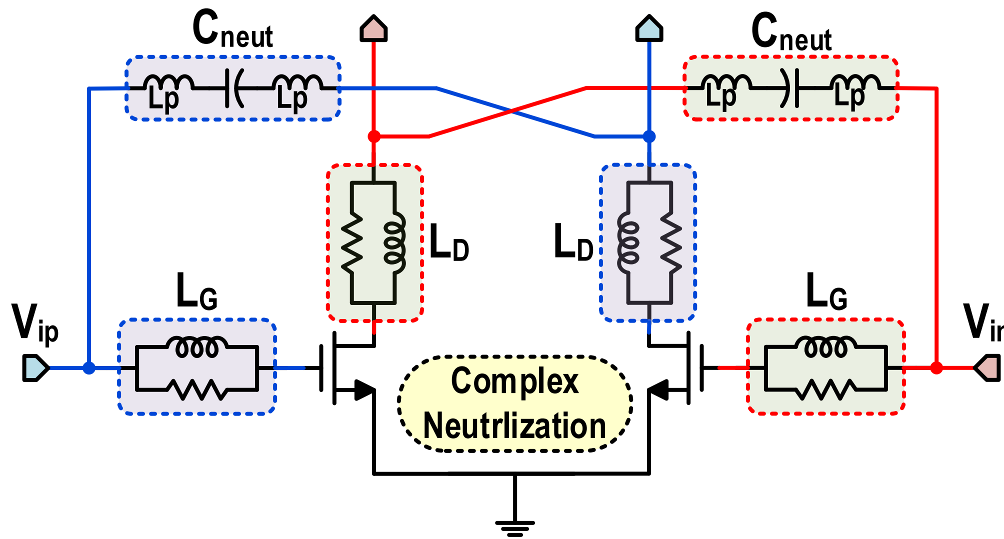


Figure 31: The proposed differential complex neutralization network, with the finite quality factors of passive elements are modelled.

CHAPTER 3. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

A prototype of the designed complex neutralization amplifier has been taped out in GlobalFoundries 45nm RF-CMOS SOI process. In this chapter, the supported simulations for the proposed amplifier are presented.

First, the transistor is RC extracted using the CALIBRE tool. Then, the embedding network, including both the inductors and the neutralization capacitors, are modelled using an electromagnetic simulator. Furthermore, the unit cell for the proposed amplifier is tested for gain and stability. The matching network is simulated and modelled using electromagnetic simulator. Eventually, the cascaded proposed is evaluated using both small and large signal and the performance summary are reported.

3.1 Physical Implementation for the Proposed Amplifier

The physical implementation for the proposed complex neutralization amplifier is shown in Figure 32. As depicted, the drain inductance is implemented using only routing. Moreover, for the gate inductance, it is implemented using one turn of a metal trace. The total area for the unit cell is $43x70\ um^2$.

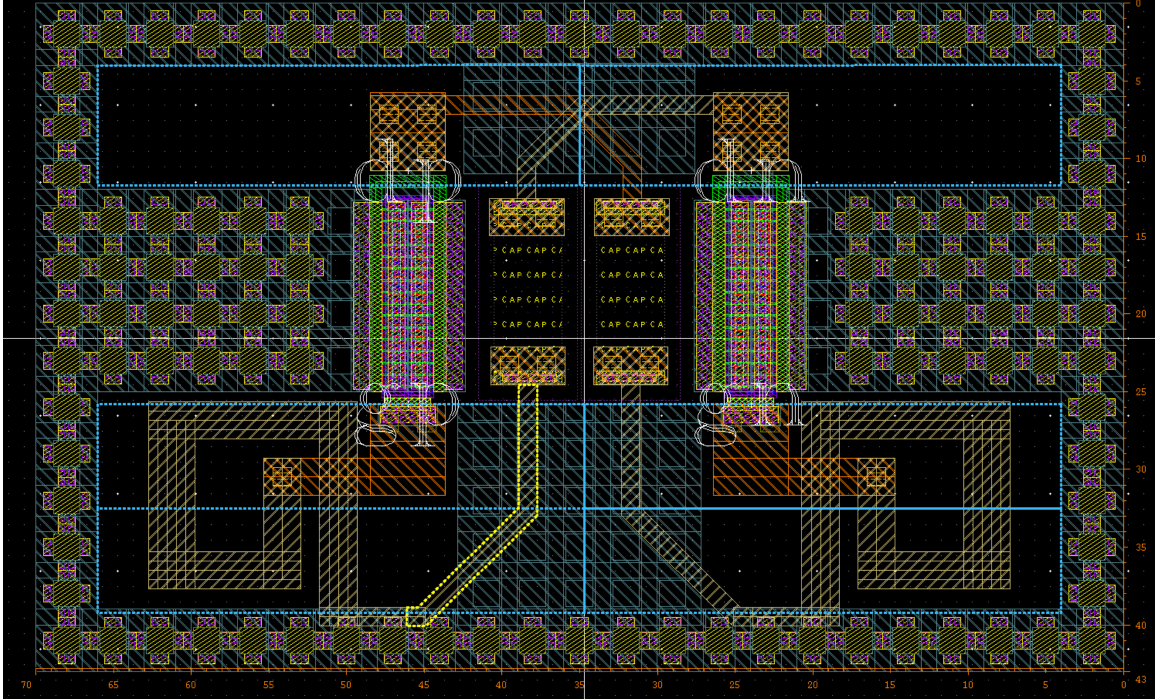


Figure 32: The physical implementation of the proposed complex neutralization amplifier.

The schematic presented in Figure 32 was simulated using Electromagnetic simulators and the S-parameters are extracted. The model of the proposed complex neutralization contains the CALIBRE view for the transistors and S-parameters for the passives.

Moreover, SP analysis is used to evaluate the small signal gain for the proposed amplifier. The power gain simulations for the previous model are shown in Figure 33. As illustrated, the gain of the transistor, G_{max}, is boosted to reach its maximum nears to *4U* near to the frequency of 50GHz and 105GHz. Furthermore, according to our proposed definition for the bandwidth, the bandwidth is around 110GHz, as the G_{max} exceeds the power gain of $2U$ from 30GHz to 140GHz.

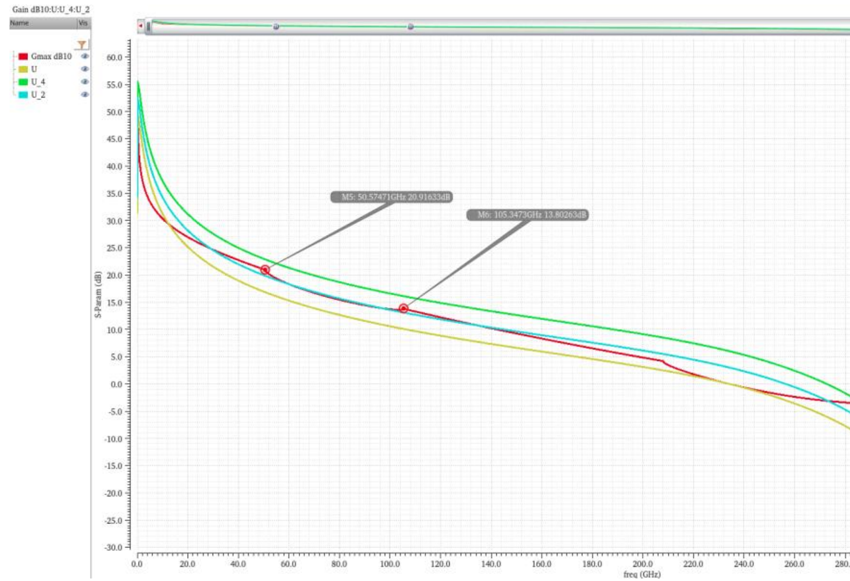


Figure 33: Device Power Gain Electromagnetic simulation results.

3.2 System Integration

The Proposed complex neutralization power amplifier is used within a three-stage PA chain with an output power combiner, as shown in Figure 34. As illustrated, the system consists of an input matching stage, an inner-stage matching, and an output matching network.

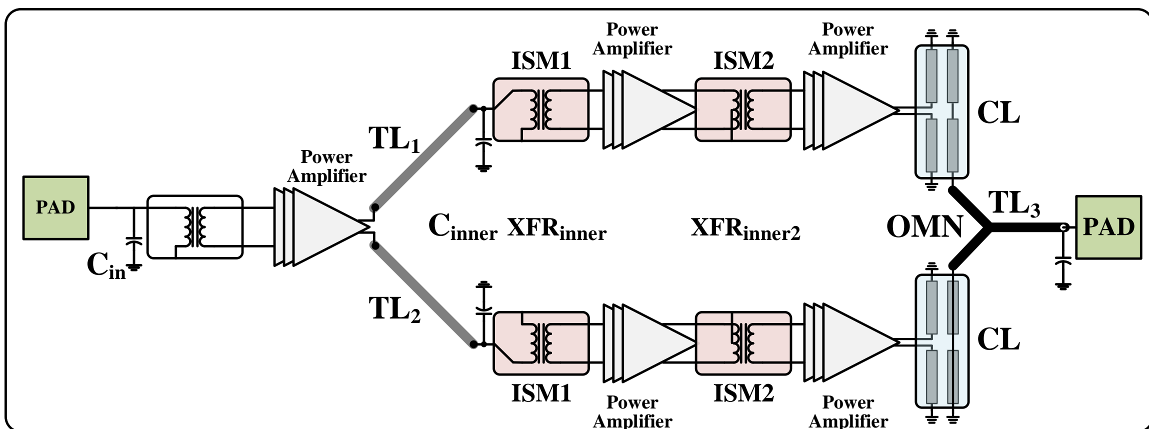


Figure 34: System Integration for the proposed complex neutralization amplifier.

3.2.1 Matching

(a) Input Matching Network

The input matching of the proposed system consists of a transformer with a capacitor at the input, as shown in Figure 35. As depicted, the ground signal ground (GSG) probe is simulated with the input matching to include its parasitics. The proposed input matching is simulated using an electromagnetic simulator and modelled with its S-parameters. The main purpose of the input matching is to match the PA to a 50-ohm input while transforming the single input to a differential input for the proposed stage.

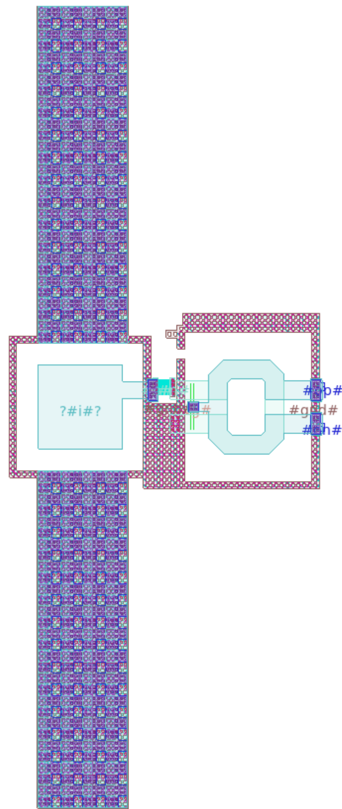


Figure 35: The GDS view using EMX for the proposed input matching network.

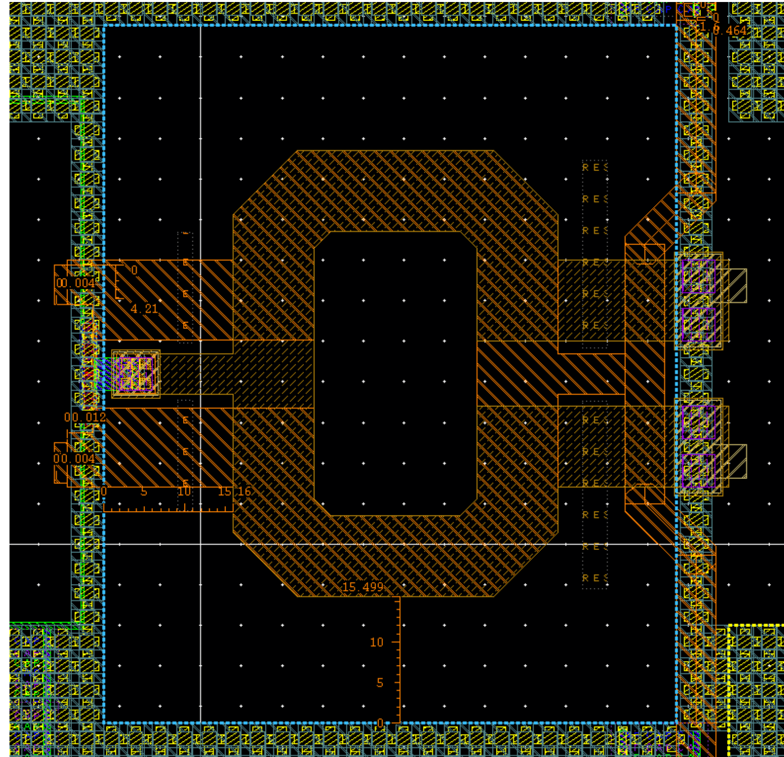


Figure 36: The physical implementation for the proposed inner stage matching network.

(b) Interstage Matching Network

The interstage matching network is used to match between the main PA and the driver and between the driver and the predriver. The physical implementation of the inner stage is shown in Figure 36.

(c) Output Matching Network

The output matching network consists of two pairs of Couple-lines, and a power combiner, as shown in Figure 37. Moreover, each coupled line pair will transform the 50 ohms output to the optimum load impedance for the power amplifier. Furthermore, the couple line stage will absorb the output capacitance of the power amplifier, while acting as a balun that transforms the differential signal

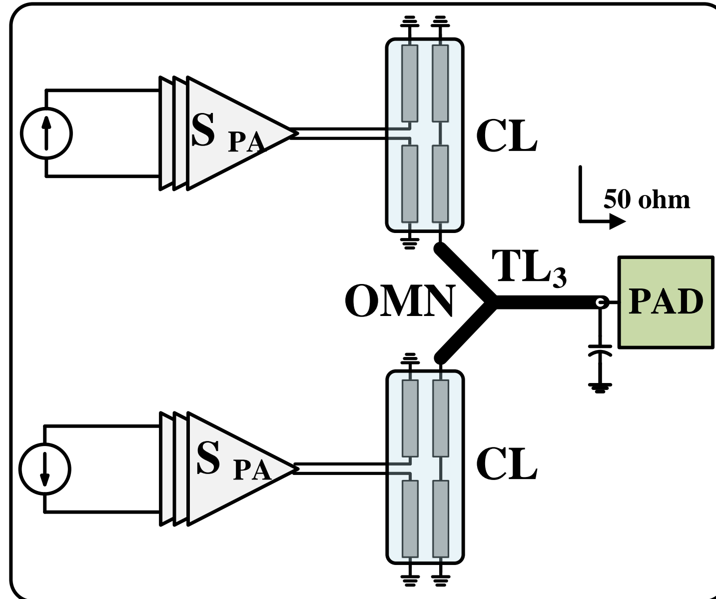


Figure 37: The output matching network with output power combiner.

from the power amplifier to a single-ended output.

The physical implementation of the coupled line balun is shown in Figure 38 while the power combining output matching network implementation is shown in Figure 39.

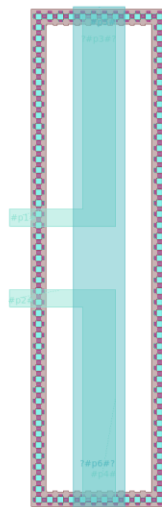


Figure 38: The GDS view using EMX for the proposed output matching for the power amplifier using a couple line.

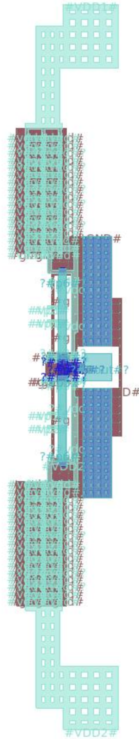


Figure 39: The full GDS view using EMX for the proposed output matching network with the output power combiner using a couple line.

The output matching network loss is shown in Figure 40. As indicated, the loss at the target frequency is less than 0.85dB. Also, the output matching loss is less than 1.5dB from 80-140GHz.

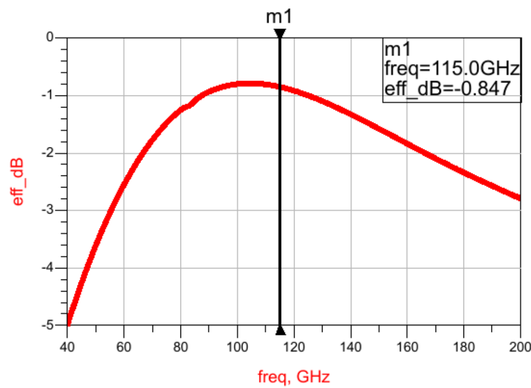


Figure 40: The passive efficiency for the output matching network.

3.3 Performance Summary

The physical implementation for the proposed system is shown in Figure 41. As indicated, the system occupies a total area of $635x1360\ um^2$, while the active core area is around $0.23mm^2$.

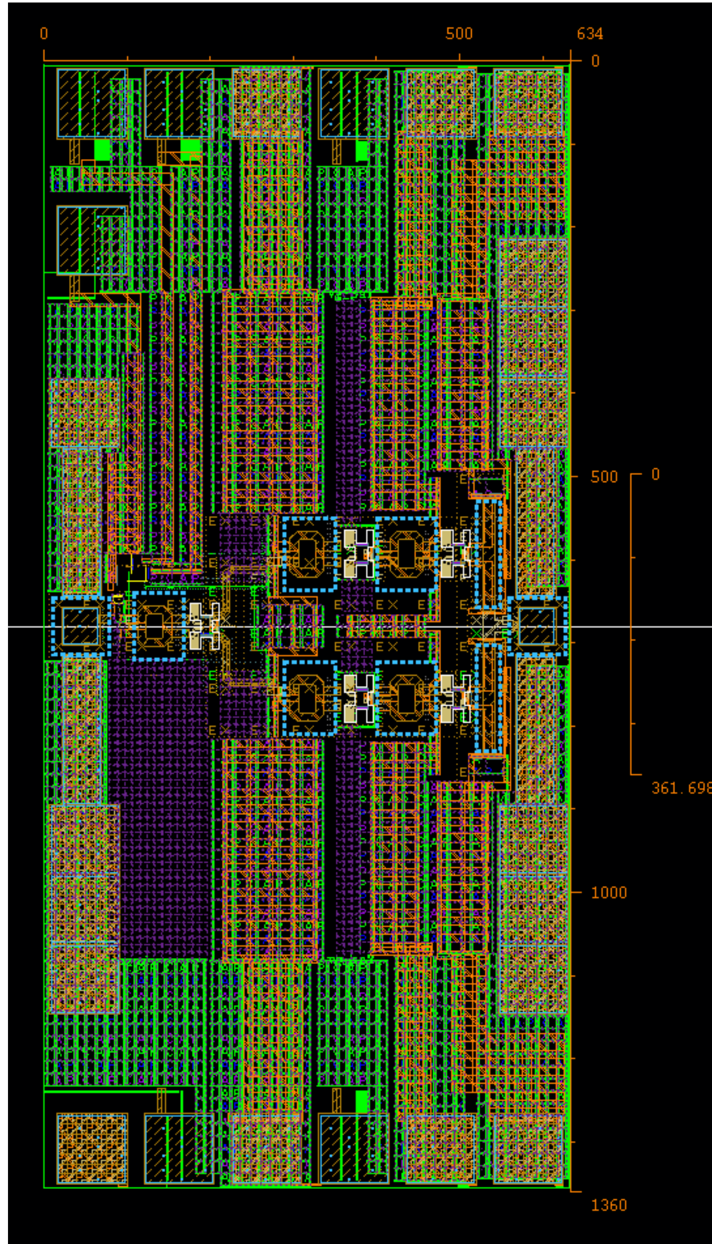


Figure 41: The physical implementation of the proposed system using the complex neutralization amplifier.

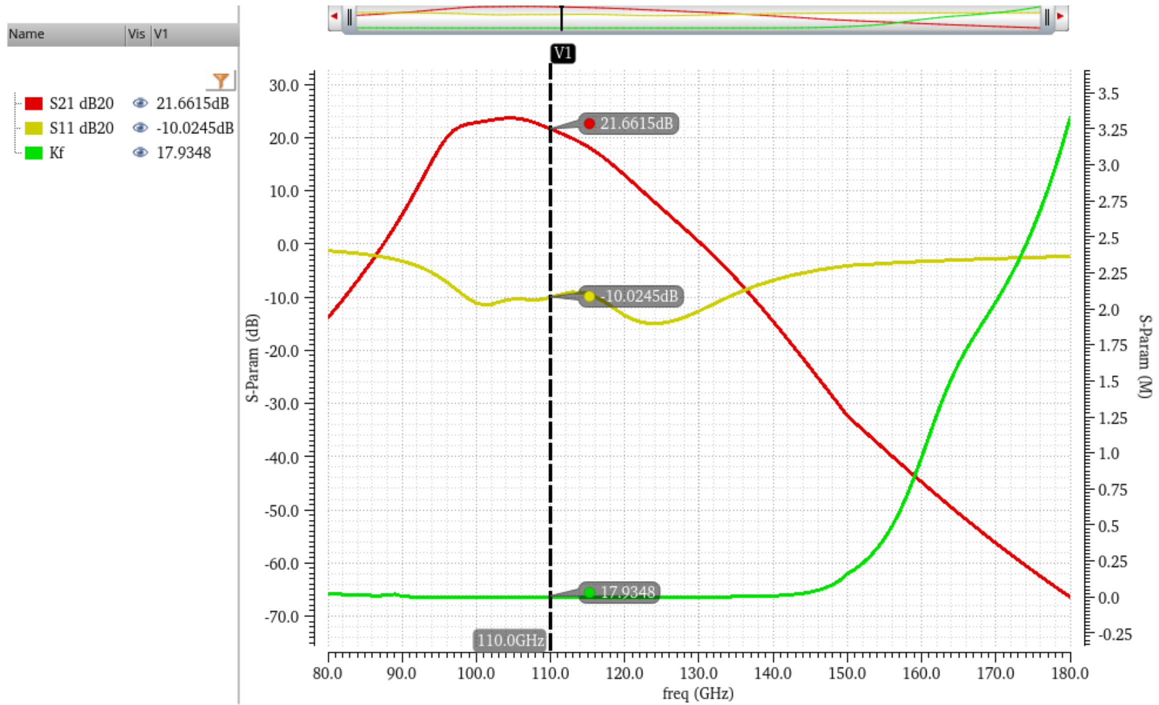


Figure 42: The small signal simulations for the proposed complex neutralization amplifier.

The small signal performance for the proposed system is shown in Figure 42. As depicted, the peak small signal gain is around 21.6dB at 115GHz.

The input matching return loss is less than -10dB from 100GHz to 140GHz. Also, the stability factor k is more than 1 across the design's entire frequency range.

On the other hand, the large signal performance is shown in Figure 43. As indicated, the achieved power gain is around 19dB, while the peak power added efficiency (PAE) is 14.25%. The saturated output power is around 12dBm.

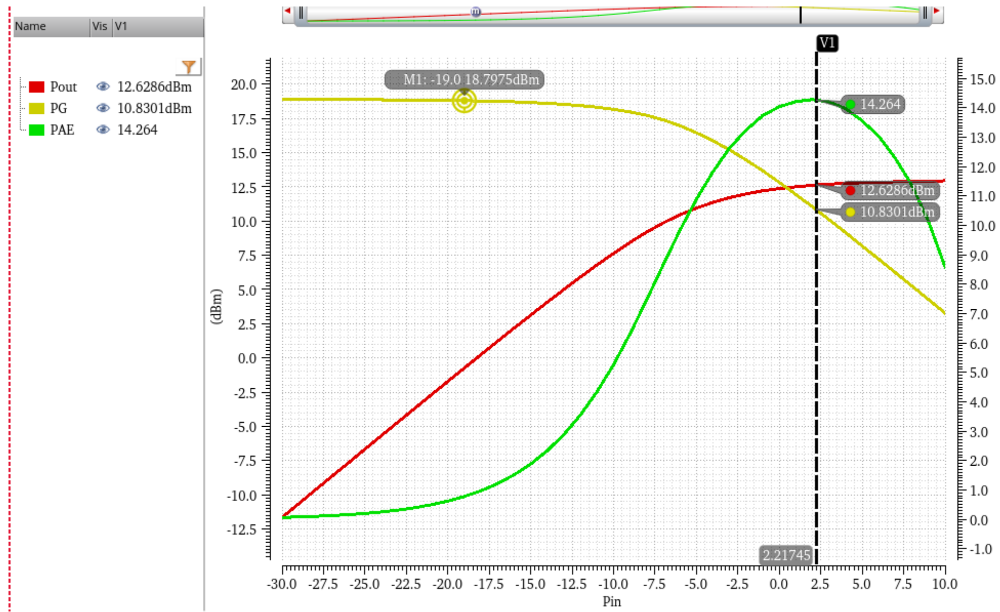


Figure 43: The large signal simulations for the proposed complex neutralization amplifier.

The summary of the performance summary with a comparison table with the state-of-artwork is shown in **Error! Not a valid bookmark self-reference.**.

Table I: The Proposed PA Performance Summary

	[11]	[12]	[13]	[14]	[15]	[16]	This Work
Technology	45nm CMOS	16nm FinFET	250nm InP	90nm CMOS	90nm CMOS	65nm CMOS	45nm CMOS
VDD (V)	1	0.8	N/A	1	2.5	1.1	1
Number of stages	8	4	1	3	3	3	3
Gain	22.2	19	6.5	9.34	17.4	8	19
Psat(dBm)	16	13.1	19-20.1	N/A	4	6	12.6
P-1dB(dBm)	12.5	7.1	N/A	N/A	2	1.5	11
Pdc (mW)	305	162	N/A	22	54	25.5	115
Freq. (GHz)	140	135	110-150	103.8	91	15	115
Peak PAE %	12.5	11	34	N/A	N/A	N/A	14.25
Area (mm^2)	0.43	0.062	N/A	0.256	N/A	0.16	0.24

CHAPTER 4. CONCLUSION AND FUTURE WORK

Although various advanced IC technologies can attain THz or sub-THz operations, including bulk CMOS, CMOS SOI, SiGe HBT and GaN, most of the implemented designs cannot achieve high gain and typically cover at-best up-to U at 100-150GHz (near to fmax of the device).

In addition, most advanced commercial IC devices still have limited cutoff frequencies compared to the THz spectrum, while scaling starts to see diminishing improvements due to increasing device/routing parasitics and base/gate resistance. Thus, operating frequencies at THz are often close to the devices' $(fmax/ft)$ limit, resulting in limited device power gains. However, existing device gain-boosting methods are either narrow-band (the embedding technique or are very sensitive to routing parasitics at THz. Therefore, the proposed complex device neutralization fundamentally maximize the device-level "gain-bandwidth product" at the target THz operating frequency.

Furthermore, native devices experience severely degraded power gain when operating close to the device f_{max} frequency. Moreover, with high passive losses of input/output matching networks, amplifiers with close-to-f_{max} operations typically exhibit very poor gain, which in turn degrades the energy efficiency and output power. To increase the gain, multiple stages in cascade are required, which increases the area and DC power overhead. Therefore, enhancing the device power gain at close-to-f_{max} frequencies has become a critical task.

Traditional capacitive neutralization enhances device gain to its unilateral gain *U* over a large bandwidth (BW) but the inductive routing parasitics will drastically degrade its performance at THz. Single-ended inductive embedding can boost the device gain up-to a remarkable value of *4U*. But it achieves so only at one single frequency. It also enforces the same DC biasing voltage at device gate/base and drain/collector, yielding low energy efficiency and poor biasing adjustability.

In this work we propose a new differential complex neutralization network which is implemented to attain a radical wideband device gain boosting. Essentially, we leverage and engineer the routing inductive parasitics L_g, L_d, and L_c with the feedback capacitors C_{neut} to form a high-order neutralization network and enable wideband gain boosting. Note that the device gate/base and drain/collector now can be independently biased for optimum device operation.

In order to understand different device characteristics, summarize their parasitic behaviors, and optimize their performance, a native gain simulation vs. frequency for several silicon/III-V devices are done as shown in Figure 28. As depicted, the InP shows a promising performance for the THz frequency. Also, the IHP SiGe shows a superior fmax performance compared to the CMOS SOI devices.

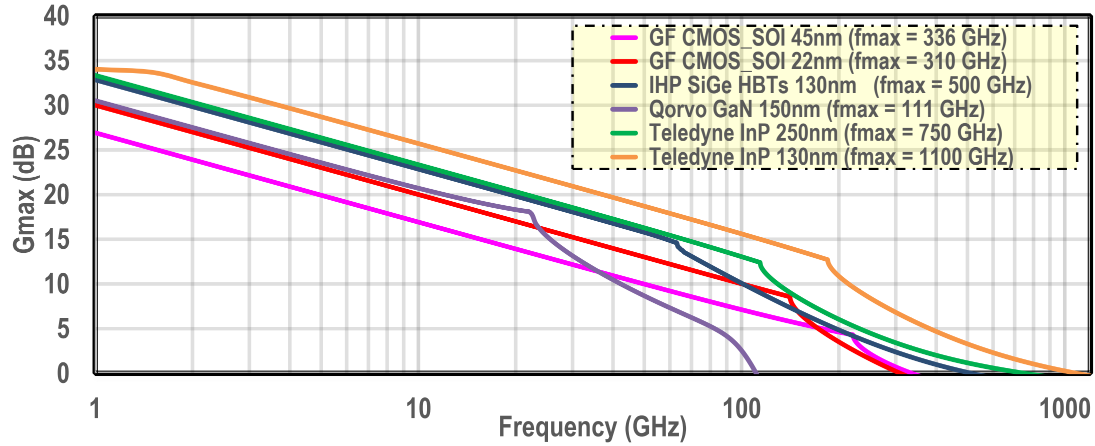


Figure 44: Simulated device power gain vs. frequency and fmax of different commercial IC processes.

In this dissertation, we investigated different embedding networks for gain boosting in high mmWave frequencies using a common-source NMOS transistor in GlobalFoundries 45nm CMOS SOI as a starting point. Fig. 21 shows the summary of the power gain of the overall two-port network across different embedding networks. The proposed complex neutralization technique provides much wider bandwidth with considerable gain enhancement that is more than unilateralizing the device by capacitor neutralization. Moreover, it does not suffer from the same gate and drain DC biasing issue faced by single-ended embedding with inductors.

To validate the feasibility of the proposed complex neutralization embedding network, the proposed complex neutralization is applied on the Globalfoundries 45nm CMOS SOI within a three-stage embedded differential amplifier. The system shows a power gain of 19dB at 115GHz with a total PAE of 14% while achieving a saturation power of 12.5 dBm.

APPENDIX A

MATLAB

```
function [cz, cp, rz] = PLL_LP(Icp, CSRO_snstvt, fout, fref, bandwidth, pm)
%==========================================================================
% Type II Charge pump based Phased Locked Loop PLL %
%==========================================================================
clc
clear all
close all
% % read Y Parameters

% the boundary for the embedding network
qg = 15; % the quality factor of the gate inductance
qd = 15; % the quality factor of the drain inductance
lg = (0:0.1:3 )*1e-12 ; % the gate inductance range
ld =  (0:0.1:5 )*1e-12 ; % thedrain inductance  range
cneut = (1:0.5:50) *1e-15 ; % the cap neutrlizaation range
lparasitic = 0.5e-12; % the seriwes inductance with the cap neutrlizaation due to the connection
L_parastc_q = 15;
L_parastc_q_en= 1;
% choose frequency 1 position
freq_pnt1 = 1800;

% define initial values for the embedding nw
l1 = lg(1) ;
l2 = ld(1) ;
c3 = cneut(1) ;

l1_max = 0 ;
l2_max = 0;
c3_max = 0;

i_l1 =1; % index for the Lg
i_l2 =1; % index for the Ld
i_c3 =1; % index for the Cneut

i_max =0;  % index for the maximum gain

approx_f1 = 0.66;  % percentage of the gmax

% reading the y paramaters of the transistor at frequency position 1
freq_pnt= freq_pnt1;


for i_read_yp=1
% % READ Y PARAMETERS
sobj = yparameters('/home/gems6/meleraky/EMX/INP/250nm_tr_0p805vbe_fmax_750Gfmax.s2p');


% choose the specified frequency
frequency = sobj.Frequencies;
freq = frequency(freq_pnt);
w = 2*22/7*freq;
y11m = rfparam(sobj,1,1) ; y11m = y11m(freq_pnt) ;
y12m = rfparam(sobj,1,2) ; y12m = y12m(freq_pnt) ;
y21m = rfparam(sobj,2,1) ; y21m = y21m(freq_pnt) ;
y22m = rfparam(sobj,2,2) ; y22m = y22m(freq_pnt) ;


end

while 1 % searching for the first frequency

for i_l1 =1:length(lg)
    l1 = lg(i_l1);
    x1  =  w .* l1 ;
    x2 = w .* l2 ;
    x3 = -1./(w .* c3) ;

%     adding Quality factor for inductance
rlx1= qg.*2.*22./7.*freq.*l1 ; % parallel resistance
rlx2= qd.*2.*22./7.*freq.*l2 ; % parallel resistance
rlx3= 2.*22./7.*freq.*lparasitic./L_parastc_q ; % series resistance
rlx4= 2.*22./7.*freq.*lparasitic./L_parastc_q ; % series resistance
    y12z1 = -1/1i./x1-1/rlx1;
    y12z2 = -1/1i./x2-1/rlx2;

    y21z1 = -1/1i./x1-1/rlx1;
    y21z2 = -1/1i./x2-1/rlx2;

    y11z1 =  1/1i./x1+1/rlx1;
```

```
    y22z1 =  1/1i./x1+1/rlx1;

    y11z2 =  1/1i./x2+1/rlx2;
    y22z2 =  1/1i./x2+1/rlx2;

    % add  parasitics to the comlex neutrlization traces
    y11z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));
    y12z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));
    y21z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));
    y22z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));



    y11 =  (y11m./y21m + (y11m.*y22m - y12m.*y21m)./(y21m.*y11z2))./((y22m./y21m + (y11m.*y22m -
y12m.*y21m)./(y21m.*y11z1))./y11z2 + 1./y21m + y11m./(y21m.*y11z1))+y11z3;
    y22 = (y22m./y21m + (y11m.*y22m - y12m.*y21m)./(y21m.*y11z1))./((y22m./y21m + (y11m.*y22m -
y12m.*y21m)./(y21m.*y11z1))./y11z2 + 1./y21m + y11m./(y21m.*y11z1))+y22z3;
    y12 = ((y12m.*y12z1.*y12z2)./((y11m+y22z1).*(y22m+y11z2)-y12m.*y21m))+y12z3;
    y21 = ((y21m.*y21z1.*y21z2)./((y11m+y22z1).*(y22m+y11z2)-y12m.*y21m))+y21z3;


A(i_l1) = y21 ./ y12 ;
gms(i_l1)= abs(y21 ./ y12) ;
k(i_l1) = (2*real(y11).*real(y22)-real(y12.*y21))./abs(y12.*y21);
    if k(i_l1)>=1
        k_max = 1;
    else
        k_max =0 ;
    end
gma(i_l1)= gms(i_l1).*(k(i_l1)-sqrt(k(i_l1).^2-1));
gain_matlab(i_l1,i_l2,i_c3) = abs(gms(i_l1)).*(1-k_max)+(k_max).*abs(gma(i_l1));
u (i_l1)= abs(y21-y12).^2./(4*(real(y11).*real(y22)-real(y12).*real(y21)));
GMAX(i_l1) = 4.*u(i_l1);

if 10*log10(GMAX(i_l1)) > 0
if gain_matlab(i_l1,i_l2,i_c3) <= GMAX(i_l1) && gain_matlab(i_l1,i_l2,i_c3) >= approx_f1*GMAX(i_l1)
i_max = i_max +1;
l1_max(i_max) = l1; % the value of the lg at the peak of the GMAX
l2_max(i_max) = l2; % the value of the ld at the peak of the GMAX
c3_max(i_max) = c3; % the value of the Cn at the peak of the GMAX

l1_max_index(i_max) = i_l1; % the position of the lg at the peak of GMAX
l2_max_index(i_max) = i_l2; % the position of the ld at the peak of GMAX
c3_max_index(i_max) = i_c3; % the position of the Cn at the peak of GMAX
end
end

for i_l2 =1:length(ld)
    l2 = ld(i_l2);
    x1  =  w .* l1 ;
    x2 = w .* l2 ;
    x3 = -1./(w .* c3) ;

    %     adding Quality factor for inductance

rlx1= qg.*2.*22./7.*freq.*l1 ; % parallel resistance
rlx2= qd.*2.*22./7.*freq.*l2 ; % parallel resistance
rlx3= 2.*22./7.*freq.*lparasitic./L_parastc_q ; % series resistance
rlx4= 2.*22./7.*freq.*lparasitic./L_parastc_q ; % series resistance

    y12z1 = -1/1i./x1-1/rlx1;
    y12z2 = -1/1i./x2-1/rlx2;

    y21z1 = -1/1i./x1-1/rlx1;
    y21z2 = -1/1i./x2-1/rlx2;

    y11z1 =  1/1i./x1+1/rlx1;
    y22z1 =  1/1i./x1+1/rlx1;

    y11z2 =  1/1i./x2+1/rlx2;
    y22z2 =  1/1i./x2+1/rlx2;

    % add  parasitics to the comlex neutrlization traces
    y11z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));
    y12z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));
    y21z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));
    y22z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));

    y11 =  (y11m./y21m + (y11m.*y22m - y12m.*y21m)./(y21m.*y11z2))./((y22m./y21m + (y11m.*y22m -
y12m.*y21m)./(y21m.*y11z1))./y11z2 + 1./y21m + y11m./(y21m.*y11z1))+y11z3;
    y22 = (y22m./y21m + (y11m.*y22m - y12m.*y21m)./(y21m.*y11z1))./((y22m./y21m + (y11m.*y22m -
y12m.*y21m)./(y21m.*y11z1))./y11z2 + 1./y21m + y11m./(y21m.*y11z1))+y22z3;
    y12 = ((y12m.*y12z1.*y12z2)./((y11m+y22z1).*(y22m+y11z2)-y12m.*y21m))+y12z3;
    y21 = ((y21m.*y21z1.*y21z2)./((y11m+y22z1).*(y22m+y11z2)-y12m.*y21m))+y21z3;


A(i_l2) = y21 ./ y12 ;
gms(i_l2)= abs(y21 ./ y12) ;
k(i_l2) = (2*real(y11).*real(y22)-real(y12.*y21))./abs(y12.*y21);
    if k(i_l2)>=1
        k_max = 1;
    else
```

```
        k_max =0 ;
    end
gma(i_l2)= gms(i_l2).*(k(i_l2)-sqrt(k(i_l2).^2-1));
gain_matlab(i_l1,i_l2,i_c3) = abs(gms(i_l2)).*(1-k_max)+(k_max).*abs(gma(i_l2));
u(i_l2) = abs(y21-y12).^2./(4*(real(y11).*real(y22)-real(y12).*real(y21)));
GMAX(i_l2) = 4.*u(i_l2);

if 10*log10(GMAX(i_l2)) > 0
if gain_matlab(i_l1,i_l2,i_c3) <= GMAX(i_l2) && gain_matlab(i_l1,i_l2,i_c3) >= approx_f1*GMAX(i_l2)
i_max = i_max +1;
l1_max(i_max) = l1; % the value of the lg at the peak of the GMAX
l2_max(i_max) = l2; % the value of the ld at the peak of the GMAX
c3_max(i_max) = c3; % the value of the Cn at the peak of the GMAX

l1_max_index(i_max) = i_l1; % the position of the lg at the peak of GMAX
l2_max_index(i_max) = i_l2; % the position of the ld at the peak of GMAX
c3_max_index(i_max) = i_c3; % the position of the Cn at the peak of GMAX
end
end

for i_c3 =1:length(cneut)

    c3 = cneut(i_c3);
    x1  =  w .* l1 ;
    x2 = w .* l2 ;
    x3 = -1./(w .* c3) ;

    %     adding Quality factor for inductance
rlx1= qg.*2.*22./7.*freq.*l1 ; % parallel resistance
rlx2= qd.*2.*22./7.*freq.*l2 ; % parallel resistance
rlx3= 2.*22./7.*freq.*lparasitic./L_parastc_q ; % series resistance
rlx4= 2.*22./7.*freq.*lparasitic./L_parastc_q ; % series resistance
    y12z1 = -1/1i./x1-1/rlx1;
    y12z2 = -1/1i./x2-1/rlx2;

    y21z1 = -1/1i./x1-1/rlx1;
    y21z2 = -1/1i./x2-1/rlx2;

    y11z1 =  1/1i./x1+1/rlx1;
    y22z1 =  1/1i./x1+1/rlx1;

    y11z2 =  1/1i./x2+1/rlx2;
    y22z2 =  1/1i./x2+1/rlx2;

    % add  parasitics to the comlex neutrlization traces
    y11z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));
    y12z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));
    y21z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));
    y22z3 =  1./(1./(+1i.*w.*c3)+2.*1i.*w.*lparasitic+L_parastc_q_en.*(rlx3+rlx4));

    y11 =  (y11m./y21m + (y11m.*y22m - y12m.*y21m)./(y21m.*y11z2))./((y22m./y21m + (y11m.*y22m -
y12m.*y21m)./(y21m.*y11z1))./y11z2 + 1./y21m + y11m./(y21m.*y11z1))+y11z3;
    y22 = (y22m./y21m + (y11m.*y22m - y12m.*y21m)./(y21m.*y11z1))./((y22m./y21m + (y11m.*y22m -
y12m.*y21m)./(y21m.*y11z1))./y11z2 + 1./y21m + y11m./(y21m.*y11z1))+y22z3;
    y12 = ((y12m.*y12z1.*y12z2)./((y11m+y22z1).*(y22m+y11z2)-y12m.*y21m))+y12z3;
    y21 = ((y21m.*y21z1.*y21z2)./((y11m+y22z1).*(y22m+y11z2)-y12m.*y21m))+y21z3;


A(i_c3) = y21 ./ y12 ;
gms(i_c3)= abs(y21 ./ y12) ;
k(i_c3) = (2*real(y11).*real(y22)-real(y12.*y21))./abs(y12.*y21);
    if k(i_c3)>=1
        k_max = 1;
    else
        k_max =0 ;
    end
gma(i_c3)= gms(i_c3).*(k(i_c3)-sqrt(k(i_c3).^2-1));
gain_matlab(i_l1,i_l2,i_c3) = abs(gms(i_c3)).*(1-k_max)+(k_max).*abs(gma(i_c3));
u(i_c3) = abs(y21-y12).^2./(4*(real(y11).*real(y22)-real(y12).*real(y21)));
GMAX(i_c3) = 4.*u(i_c3);

if 10*log10(GMAX(i_c3)) > 0
if gain_matlab(i_l1,i_l2,i_c3) <= GMAX(i_c3) && gain_matlab(i_l1,i_l2,i_c3) >= approx_f1*GMAX(i_c3)
i_max = i_max +1;
l1_max(i_max) = l1; % the value of the lg at the peak of the GMAX
l2_max(i_max) = l2; % the value of the ld at the peak of the GMAX
c3_max(i_max) = c3; % the value of the Cn at the peak of the GMAX
l1_max_index(i_max) = i_l1; % the position of the lg at the peak of GMAX
l2_max_index(i_max) = i_l2; % the position of the ld at the peak of GMAX
c3_max_index(i_max) = i_c3; % the position of the Cn at the peak of GMAX
end
end
end
end

end
break
end

   embedding_NW = [l1_max*1e12;l2_max*1e12;c3_max*1e15];
```

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