

**TOWARDS A UNIVERSAL HOT CARRIER DEGRADATION
MODEL FOR SIGE HBTS SUBJECTED TO ELECTRICAL STRESS**

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The Academic Faculty

by

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TABLE OF CONTENTS

ACKNOWLEDGEMENTS	iv
LIST OF TABLES	xi
LIST OF FIGURES	xii
LIST OF SYMBOLS AND ABBREVIATIONS	xx
SUMMARY	xxii
CHAPTER 1 Introduction	1
1.1 Motivation and Background for Using SiGe HBTs.....	1
1.2 Reliability Challenges of SiGe HBT Scaling.....	2
1.3 Thesis Outline	4
CHAPTER 2 Silicon-Germanium BICMOS Technology and Reliability	6
2.1 Brief History of Silicon-Germanium Technology	6
2.2 Overview of Competing Degradation Effects in SiGe HBTs.....	7
2.2.1 Avalanche-Generated Hot Carriers.....	10
2.2.2 Auger-Generated Hot Carriers	11
2.2.3 Trap Annealing	13
2.3 Extent of SiGe HBT Reliability Modeling in Literature	14
CHAPTER 3 Accumulated Stress Modeling of Mixed-mode damage in Sige HBTs	17
3.1 Motivation.....	17
3.2 Damage Physics of Mixed-Mode Stress Degradation	18
3.3 Impact-Ionization Calibration.....	19
3.4 Mixed-Mode Damage Temperature Dependence	21
3.5 Damage Calibrations Over Electrical Bias and Temperature	25
3.6 Accumulated Stress Damage	30
3.7 Summary	35

CHAPTER 4 Modeling of High-Current Damage in SiGe HBTs Under Pulsed Stress	37
4.1 Motivation.....	37
4.2 Physics of High-Current Damage.....	39
4.3 High-Current Pulsed Stress Measurements	41
4.4 Modeling High-Current Auger Damage.....	45
4.5 Summary.....	49
CHAPTER 5 Physical Differences in Hot Carrier degradation of oxide interfaces in complementary (NPN+PNP) SiGe HBTs.....	51
5.1 Motivation.....	51
5.2 Mixed-Mode Damage Mechanism in NPN and PNP SiGe HBTs.....	54
5.3 Damage due to Polarity of Hot Carriers	56
5.4 Interface Dependence of Damage.....	57
5.5 Hot Carrier Damage Sources and Significance of Model Parameter	63
5.6 Discussion of Results and Calibrations.....	67
5.7 Summary.....	70
CHAPTER 6 Hot-Carrier-Damage-Induced Current Gain Enhancement (CGE) Effects in SiGe HBTs	73
6.1 Motivation.....	73
6.2 Current Gain Due to Polysilicon.....	76
6.2.1 Hot Carrier Damage of Polysilicon.....	77
6.2.2 Vulnerabilities for CGE Due to Polysilicon Dopants.....	79
6.2.3 Simplified TCAD Simulations showing CGE	80
6.3 Measured Response to Polysilicon Damage.....	86
6.3.1 Evidence for CGE in DC Stress Measurements	86
6.3.2 Evidence for Polysilicon Degradation	91

6.4 Summary	95
CHAPTER 7 High Temperature Degradation Effects in SiGe HBTs	97
7.1 Motivation.....	97
7.2 Background on Current Gain Enhancement	98
7.3 TCAD Modeling of Polysilicon Degradation.....	100
7.4 Capturing Electrical Response to Polysilicon Degradation	103
7.5 High Temperature Measurements.....	105
7.6 Summary.....	111
CHAPTER 8 Emitter-Base Profile Optimization of SiGe HBTs for Improved Thermal Stability and Frequency Response at Low-Bias Currents	113
8.1 Motivation and Background on Electro-Thermal Feedback.....	113
8.2 Temperature-Invariant Current Gain Physics	116
8.3 Methods for Improving Large-Signal Performance.....	119
8.4 Emitter-Base Optimized Device Profiles.....	121
8.5 Measurements and Discussion.....	123
8.6 Summary.....	129
CHAPTER 9 On the Reliability and Increased Variability of SiGe HBTs Under Cryogenic Temperature Operation.....	131
9.1 Motivation for Cryogenic Studies in SiGe HBTs.....	131
9.2 Reliability Scaling at Low Temperatures	133
9.3 Variability Challenges for Cryogenic Applications.....	136
9.4 TCAD Verification of Electrical Variability	142
9.5 Summary.....	144
CHAPTER 10 Conclusion.....	145
10.1 Summary of Contributions.....	145
10.2 Future Work	147

REFERENCES.....	150
VITA.....	164

LIST OF TABLES

Table 4.1:	Comparison of equations used in the lucky electron model for generating high-field and high-current hot carriers. After [29].	47
Table 5.1:	Technology specifications of the NPN and PNP devices in this work.	53
Table 6.1:	Performance Metrics of Measured Devices	86
Table 8.1:	Profile Differences of Measured Devices	123
Table 8.2:	Device Performance FoMs	129
Table 9.1:	List of Devices Measured	139

LIST OF FIGURES

Figure 1.1:	Simulated SOA of forward-Gummel characteristics degradation in an NPN SiGe HBT after 100,000 s of stress with various T-dependent damage regions outlined. Various dynamic load lines that change the EOL of the device due to hot carrier damage are overlaid (after [3]).....	3
Figure 2.1:	TCAD cross section showing current density through a fourth generation SiGe HBT under a high power condition of $J_E = 50 \text{ mA}/\mu\text{m}^2$ and $V_{CB} = 4 \text{ V}$. Current constricts towards the center of the device under high voltage operation, eventually triggering catastrophic thermal runaway of the device.	8
Figure 2.2:	TCAD simulation of increasing base leakage current due to hot carrier damage following a high voltage stress. Forward and inverse mode operation of the SiGe HBT samples the base leakage due to EB and STI oxide traps (after [29]).	9
Figure 2.3:	Measured change in the Gummel characteristics of a NPN SiGe HBT following high-current stress of $V_{CB} = 2 \text{ V}$, $J_E = 15 \text{ mA}/\mu\text{m}^2$ (after [16]).	10
Figure 2.4:	Hot carrier generation and transport to oxide interfaces under mixed-mode stress (after [29]).	11
Figure 2.5:	Probability distribution of hot electrons with multiple simultaneous Auger transition energies in silicon.	12
Figure 2.6:	Auger hot carrier generation and transport to oxide interfaces under high-current stress.	13
Figure 3.1:	Calibration of avalanche multiplication across varying current levels and across temperature.	20
Figure 3.2:	Distinct trap states in Silicon and the associated activation energies required for diffusion of hydrogen.	23
Figure 3.3:	Five points for damage calibration marked on the left with numbers 1-5. Six points for measuring accumulated damage marked on the right with letters A-F. Two paths for accumulating stress damage are marked with pink and black arrows.	26
Figure 3.4:	Degradation (I_B increase) from forward-Gummel characteristics measured at $I_C = 0.1 \text{ nA}/\mu\text{m}^2$ for the 5 calibration points from Figure 3.3.....	27

Figure 3.5:	Calibration of simulations to measurements for I_B degradation over temperature for a stress condition of $V_{CB} = 8.5$ V and $J_E = 0.464$ mA/ μm^2 . The base current degradation is extracted at $J_C = 10$ nA/ μm^2 from forward-Gummel Characteristics. Vertical error bars show the spread of data across 3 devices.....	28
Figure 3.6:	Temperature dependence of λ and λ_r . These are the values used for the calibrations in Figure 3.5.	28
Figure 3.7:	Simulated Hot carrier impingement rates at EB spacer over temperature.	29
Figure 3.8:	Simulated Hot carrier generation rate at EB spacer after 10 s of stress on the left. 2-D cross-section of the rate for stress points A and E shown on the right.	31
Figure 3.9:	Peak Trap concentration at EB spacer over the two different stress sweeps. The stress condition associated with each stress period of 1000 s has been identified with labeling convention from Figure 3.3.	31
Figure 3.10:	Degradation from forward-Gummel characteristics at EB spacer over the two different stress sweeps for $V_{BE} = 0.5$ V. The stress condition associated with each stress period of 1000 s has been identified with labeling convention from Figure 3.3. The solid lines show the mean value of measured data and the vertical cross-lines show the spread of the data over a sample of six devices for each stress sweep.....	33
Figure 3.11:	Degradation from forward-Gummel characteristics at EB spacer over two different temperature stress sweeps for a stress condition of $V_{CB} = 8.5$ V and $J_E = 0.464$ mA/ μm^2 . The temperature associated with each stress period of 1000 s is labeled. The base current degradation is extracted at $J_C = 10$ nA/ μm^2 from forward-Gummel Characteristics. The solid lines show the mean value of measured data and the vertical cross-lines show the spread of the data over a sample of 3 devices for each stress sweep.....	34
Figure 4.1:	Contour map of hot-carrier production due to high-fields (Impact-ionization) and high-currents (Auger generation) at room temperature incorporating self-heating of the device.	38
Figure 4.2:	(a) One and two electron transitions followed by a photon emission in an atom. (b) One and two electron transitions in bulk semiconductors resulting in energetic excitation of carriers.....	40
Figure 4.3:	Temperature dependence of the hot-carrier energy distribution assuming a phonon-assisted process for the two electron transitions. After the device has enough thermal energy from self-heating, Auger process has enough probability of producing hot carriers that can overcome the 2.3 eV energy required for breaking Si-H bonds.	41

Figure 4.4:	Variations in pulsed stress damage for a DC equivalent stress condition of $J_E = 20 \text{ mA}/\mu\text{m}^2$ and $V_{CB} = 1.5 \text{ V}$. I_B degradation was extracted from forward-Gummel characteristics at $J_C = 1 \text{ }\mu\text{A}/\mu\text{m}^2$. Damage from pulse width variation compared to DC stress for a fixed 50% duty cycle.	42
Figure 4.5:	Stress damage evolution plotted against pulse width for a fixed 50% duty cycle for the conditions in Figure 4.4. The transition from dark blue to dark brown indicates increasing time from 0.1 s to 10000 s.....	43
Figure 4.6:	High-current stress degradation under pulsed-mode for $V_{CB} = 0 \text{ V}$. I_B degradation extracted from forward-Gummel characteristics at $J_C = 0.1 \text{ }\mu\text{A}/\mu\text{m}^2$. Pulsed-mode stress degradation with 50 ms width and 50% duty cycle.	44
Figure 4.7:	High-current stress degradation under DC for $V_{CB} = 0 \text{ V}$. I_B degradation extracted from forward-Gummel characteristics at $J_C = 0.1 \text{ }\mu\text{A}/\mu\text{m}^2$	45
Figure 4.8:	Comparison of the calibration of V_{BE} roll-off in TCAD and measurements to account for self-heating.	47
Figure 4.9:	Calibration of TCAD to a measured pulsed condition with a pulse width of 2.5 ms and a duty cycle of 30%. I_B degradation was extracted from forward-Gummel characteristics at $J_C = 1 \text{ }\mu\text{A}/\mu\text{m}^2$	49
Figure 5.1:	Calibrated forward-Gummel characteristics of the PNP and NPN devices in this work. All devices used have $A_E = 0.3 \text{ }\mu\text{m} \times 6.4 \text{ }\mu\text{m} \times 2$	53
Figure 5.2:	Relative level of impact ionization seen in the PNP and NPN SiGe HBTs for $J_E = 464 \text{ }\mu\text{A}/\mu\text{m}^2$ at 300 K. Level of bias determines which device sees more impact ionization.	55
Figure 5.3:	Relative effective field strength in NPN and PNP SiGe HBTs at the CB junction for $J_E = 464 \text{ }\mu\text{A}/\mu\text{m}^2$ and $V_{CB} = 7.5 \text{ V}$ at 300 K. The peak field is larger in the PNP.	55
Figure 5.4:	Respective secondary hot carriers responsible for damage at the EB interface for an NPN and PNP SiGe HBT under mixed-mode stress.....	56
Figure 5.5:	Hot carrier impingement along the EB oxide interface in NPN and PNP SiGe HBTs for a stress condition of $V_{CB} = 8.5 \text{ V}$ and $J_E = 400 \text{ }\mu\text{A}/\mu\text{m}^2$ at 300 K.....	57
Figure 5.6:	Qualitative functions for the passivation and de-passivation activation energies required as a function of the local E_{fermi} of the trap to alter the Si-H bond. The actual shape of these functions is dependent on interface orientation and quality. (a) Qualitatively derived from [66]. (b) Follows the values reported in [37] and the assumptions in [36].	60

Figure 5.7:	Simulated (a) activation energies and (b) hot carrier rates along the EB interface for NPN and PNP devices for a stress condition of $V_{CB} = 8.5$ V and $J_E = 0.400$ mA/ μm^2 at 373 K. The sharp transitions of activation energies and hot carrier rates along the interface indicate the carrier population inversion.....	62
Figure 5.8:	Difference in measured mixed-mode damage between NPN and PNP across temperature for a stress condition of $V_{CB} = 8.5$ V and $J_E = 0.400$ mA/ μm^2 . Each temperature curve is averaged over 4 devices of NPN and 4 devices of PNP.....	64
Figure 5.9:	Damage due to high-current stress at 323 K for $V_{CB} = 0$ V and $J_E = 20$ mA/ μm^2	65
Figure 5.10:	Damage due to reverse EB stress condition of 3.5V at 300 K. All damages were extracted from forward-Gummel characteristics at $J_C = 10$ nA/ μm^2	65
Figure 5.11:	Inverse-mode (STI) degradation due to forward-mode high-current stress at 323 K for $J_E = 20$ mA/ μm^2 . Extracted at $J_C = 10$ nA/ μm^2	69
Figure 5.12:	Mixed-mode degradation of a PNP device. Calibration of TCAD to measurements for I_B degradation over temperature for a mixed-mode stress condition of $V_{CB} = 8.5$ V and $J_E = 0.400$ mA/ μm^2 . The base current degradation is extracted at $J_C = 10$ nA/ μm^2 from forward-Gummel characteristics. Vertical error bars show the spread of data across 4 devices.	70
Figure 6.1:	Measured degradation of Gummel characteristics and β in a NPN SiGe HBT following a high-current stress of $V_{CB} = 0$ V, $J_E = 21.5$ mA/ μm^2 . ..	74
Figure 6.2:	Current components contributing to and limiting current gain.....	76
Figure 6.3:	(a) High-current stress induced Auger hot carrier damage to oxide interfaces and polysilicon, and hydrogen movement. (b) Grain boundary damage of polysilicon emitter. Overall polysilicon resistance a function of local hydrogen distribution.	78
Figure 6.4:	TCAD simulation of the total recombination rate (Auger + SRH) when μ and τ are independently degraded by 10x.	81
Figure 6.5:	TCAD simulation of forward-Gummel characteristics for a 1 st generation SiGe HBT. (a) With μ reduction (b) With μ and contact resistance reduction. Original series resistance of 100 Ω at the emitter and 500 Ω at the base.....	83
Figure 6.6:	TCAD simulation of current gain while independently reducing the mobilities in the emitter and base poly by 10x to qualitatively see damage dependence under (a) forward and (b) inverse modes of operation.....	84

Figure 6.7:	TCAD cross-section of 10x polysilicon μ degradation affecting (a) hole injection from the base into the emitter and (b) electron injection from the emitter into the base.	85
Figure 6.8:	TCAD simulation of current gain under forward mode while independently considering the polysilicon and oxide interface damage mechanisms.	85
Figure 6.9:	Measured forward mode CGE in NPN1 with $A_E = 15.36 \mu\text{m}^2$ following high-current stress at $T = 300 \text{ K}$ with $V_{CB} = 0 \text{ V}$. Colors from blue to red indicate increasing stress current density. β extracted from Gummel characteristics at $J_C = 1 \text{ mA}/\mu\text{m}^2$	87
Figure 6.10:	Measured forward mode CGE in NPN1 and PNP1 with $A_E = 3.84 \mu\text{m}^2$ following high-current stress of $V_{CB} = 0 \text{ V}$ and $J_E = 21.5 \text{ mA}/\mu\text{m}^2$. β extracted from Gummel characteristics at $J_C = 7\text{e-}4 \text{ A}/\mu\text{m}^2$. NPN is given by solid lines and PNP by dotted ones.	88
Figure 6.11:	Measured current gain degradation and enhancement for a high-current stress condition of $J_E = 21.4 \text{ mA}/\mu\text{m}^2$ and $V_{CB} = 0 \text{ V}$ across various emitter areas at $T = 300 \text{ K}$. β extracted at $J_C = 1 \text{ mA}/\mu\text{m}^2$	89
Figure 6.12:	Measured current gain degradation and enhancement for a mixed-mode condition of $J_E = 21.5 \text{ mA}/\mu\text{m}^2$ and $V_{CB} = 1.5 \text{ V}$ for NPN2 across various temperatures under (a) inverse and (b) forward modes of operation. β extracted at $J_C = 1 \text{ mA}/\mu\text{m}^2$. 4 device samples per temperature.	90
Figure 6.13:	Measured inverse mode complementary β degradation following reverse EB stress at $T = 300\text{K}$. Colors from blue to brown indicate increasing stress condition from $V_{BE} = 0$ to 4 V in steps of 0.5 V . Extracted from inverse-Gummel characteristics at $J_C = 7\text{e-}4 \text{ A}/\mu\text{m}^2$. NPN is given by solid lines and PNP by dotted ones.	91
Figure 6.14:	Evolution of the extracted RB as a function of frequency during a stress of $V_{CB} = 10 \text{ V}$ and $V_{BE} = 1.3 \text{ V}$ on NPN3 at $T = 323 \text{ K}$. S-Parameters were measured for $V_{BE} = 1 \text{ V}$. Colors from blue to red indicate increasing stress period from 0 to 100,000 s. During the stress period, the extracted RB changes by as much as 15Ω	92
Figure 6.15:	Correlated degradation of (a) AC and (b) DC FoMs during a stress of $V_{CB} = 10 \text{ V}$ and $V_{BE} = 1.3 \text{ V}$ on NPN3 at $T = 323 \text{ K}$. Peak f_T/f_{max} extracted from S-Parameters. RB extracted from open-circle plots based on S-Parameters at $V_{BE} = 1 \text{ V}$. J_B , J_C , and β degradation are extracted from forward-Gummel characteristics.	94
Figure 7.1:	Flow diagram of models for simulating polysilicon degradation in Synopsys Sentaurus.	100

Figure 7.2:	Simulated change of passivation level in the polysilicon emitter in response to high-current stress of $J_E = 21.5 \mu\text{A}/\mu\text{m}^2$ and $V_{CB} = 0 \text{ V}$. Blue to red color indicate increasing stress time from 1 μs to 215 s.	102
Figure 7.3:	Simulated hydrogen concentration within polysilicon emitter in response to high-current stress of $J_E = 21.5 \mu\text{A}/\mu\text{m}^2$ and $V_{CB} = 0 \text{ V}$. Blue to red color indicate increasing stress time from 1 μs to 215 s.	103
Figure 7.4:	Reduction of potential barriers at grain boundaries by passivation and doping.	104
Figure 7.5:	Changes in electron and hole mobilities using the spatial mobility degradation model for the condition in Figure 7.2 after a stress period of 100 s.	105
Figure 7.6:	Simulated Gummel characteristics using the spatial mobility degradation model for the condition in Figure 7.2 after a stress period of 100 s.	105
Figure 7.7:	Parallel shifts in collector current under forward and inverse mode operation. Indicates boron neutralization.	107
Figure 7.8:	Increase in collector current at a fixed V_{BE} corresponding to an initial low injection condition of $J_C = 1 \mu\text{A}/\mu\text{m}^2$. Indicates parallel collector current shifts due to boron neutralization.	108
Figure 7.9:	Increase in base current degradation at a fixed V_{BE} corresponding to an initial low injection condition of $J_C = 1 \mu\text{A}/\mu\text{m}^2$. Indicates oxide interface damage.	109
Figure 7.10	Increase in CGE at a fixed V_{BE} corresponding to an initial high injection condition of $J_C = 1 \text{ mA}/\mu\text{m}^2$. Indicates polysilicon minority mobility degradation.	110
Figure 7.11:	Collector current enhancement at a fixed V_{BE} corresponding to an initial high injection condition of $J_C = 1 \text{ mA}/\mu\text{m}^2$. Indicates changes in polysilicon resistance.	111
Figure 8.1:	Heat distribution in a multi-transistor array. (after [89])	115
Figure 8.2:	Unequal current distribution in a multi-transistor array following the heat distribution in Figure 8.1. Length and color of arrows indicate the magnitude of the current. (after [])	116
Figure 8.3:	TCAD simulations of the temperature dependence of β for different collector current densities.	118
Figure 8.4:	TCAD-simulated temperature coefficient of β for different collector current densities as EB Ge percentage is varied for a fixed doping profile.	119

Figure 8.5:	(a) Reduction of EB and CB junction doping for reduced capacitance. Reduction of base width and increased base doping peak for improved speed.	120
Figure 8.6:	Measured f_T/f_{max} improvement from the control profile N1 to the optimized N2 profile with reduced EB and CB capacitance, reduced base width and increased base doping.	122
Figure 8.7:	(a) Constantly doped EB ledge for increased EB separation, reduced doping intercept and reduced C_{EB} . (b) Ge ledge at the EB junction consisting of a constant Ge percentage.	122
Figure 8.8:	Measured and extracted BV_{CEO} for EB optimized profiles from the base current reversal point at different fixed emitter current density inputs. .	124
Figure 8.9:	Measured β at $T = 300$ K for the different profiles. β -optimized profiles consistently show reduced β	125
Figure 8.10:	Measured temperature coefficient of β ($\Delta \beta$ w.r.t temperature) for different profiles versus J_C . Extracted over 300 to 400 K.	126
Figure 8.11:	Measured current gain of different profiles extracted at $J_C = 1 \mu A/\mu m^2$ for different temperatures.	126
Figure 8.12:	Measured improvement in f_{max} over the control profile for $V_{CB} = 4$ V..	128
Figure 8.13:	Measured f_T and f_{max} curves for the different profiles for $V_{CB} = 4$ V.....	128
Figure 8.14:	Measured Peak $f_{max} \times BV_{CEO}$ FoM for the different profiles for $V_{CB} = 4$ V.	129
Figure 9.1:	Increase in mean base current degradation seen across four device samples for cryogenic temperatures following a mixed-mode stress of $J_E = 100 \mu A/\mu m^2$ and $V_{CB} = 2$ V. I_B extracted at $J_C = 1 \mu A/\mu m^2$. Colors from blue to red indicate increasing stress time from 0.1 s to 10,000s. Regions of damage limited by hydrogen diffusion and phonon scattering indicated.....	134
Figure 9.2:	Temperature dependence of electron scattering length and diffusion coefficient of hydrogen following the calibration in [3].....	135
Figure 9.3:	Measured variabilities of aged base currents plotted as standard deviations from the normalized mean value for the mixed-mode stress condition in Figure 9.1. Colors from blue to red indicate increasing stress time from 0 s to 10,000s.....	136
Figure 9.4:	Measured variability of Gummel characteristics in a fourth-generation SiGe HBT across 12 sample devices under FM and IM operation at 25 K.....	137

- Figure 9.5: Measured FM and IM electrical variabilities plotted as standard deviations from the normalized mean value for different generations of SiGe HBTs and a ring diode. (a) J_C and (b) J_B extracted at fixed V_{BE} . (c) β extracted at fixed J_C . All extractions at or near $J_C = 1 \mu A/\mu m^2$ 140
- Figure 9.6: Measured FM electrical variability plotted as standard deviations from the normalized mean value for J_C and J_B extracted at fixed V_{BE} near $J_C = 1 \mu A/\mu m^2$ with and without an applied $V_{CB} = 2.5$ V. 141
- Figure 9.7: TCAD simulations of (a) profiles consisting of 9 total Gaussian base variations in width and peak doping. (b) Simulated σ_{J_C} (black) and σ_{J_B} (blue), and σ_{β} (red), under FM (solid) and IM (dotted). (c) Cross-sectional variability of significant TCAD parameters under FM. (d) Spatial variation of electric field with decreasing temperature under FM. 143

LIST OF SYMBOLS AND ABBREVIATIONS

BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
SiGe	Silicon-Germanium
HBT	Heterojunction Bipolar Transistor
CB	Collector-Base
EB	Emitter-Base
BV_{CEO}	Breakdown voltage at the point of base current reversal
TCAD	Technology Computer-Aided Design
EOL	End of lifetime
SOA	Safe Operating Area
R-D	Reaction-Diffusion
CGE	Current Gain Enhancement
NBTI	Negative bias temperature instability
QC	Quantum Computing
M-1	The measure of Avalanche multiplication from electric fields
FoM	Figure of Merit
H	Hydrogen
FM	Forward Mode operation of SiGe HBT
IM	Inverse Mode operation of SiGe HBT
λ	Scattering length of a carrier
ϕ_{hot}	Hot carrier activation energy for depassivating Si-H bond
β	Current Gain
μ	Mobility

τ Recombination Lifetime

σ Standard Deviation or variation

SUMMARY

The objective of this work is to develop a generalizable understanding of the degradation mechanisms present in Silicon-Germanium (SiGe) heterojunction bipolar transistors (HBTs) that can be used to not only predict the reliable end of lifetime (EOL) of these devices but also overcome some of these aging limitations using clever device engineering. Presently, Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) foundries impose very pessimistic restrictions on how much a SiGe HBT's performance can be pushed before facing adverse aging effects. While these foundries supply compact device models for circuit designs, a universal degradation model (currently unavailable) with push-button reliability prediction for these devices using hot-carrier physics could enable design optimizations that maximize performance while meeting the EOL requirement. This broad motivation for understanding and improving SiGe HBT device reliability is explored through the following specific goals: 1) develop an understanding of the dominant hot carrier degradation sources across temperature (25 K – 573 K); 2) develop a broad understanding of all potentially vulnerable regions of damage within a SiGe HBT using electrically measured data, and how these degradations can be captured in a modeling framework; and 3) design optimized SiGe HBTs that can potentially overcome some of these device-level limitations in reliability across temperature.

The following is a summary of accomplishments towards the above goals:

1. An introduction to the history and making of SiGe HBTs, and their relevance in modern high-speed communication systems. The challenges of SiGe HBT operation under extreme biasing and temperature conditions are summarized.

2. A preliminary demonstration of a TCAD-based aging model for simulating SiGe HBT aging under dynamic bias and temperature – This work fully explores the physics of impact-ionization-induced (by high electric fields) hot-carriers in SiGe HBTs using a physics-based TCAD model. This was first presented at SRC TECHON © 2013 [1], published in the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) © 2013 [2] and later extended in the IEEE Transactions on Electron Devices (TED) © 2015 [3].
3. First physics-based high current damage model for SiGe HBTs – This work explores the bias and temperature dependence of the Auger hot carrier generation under high current operation, and uses pulsed current stress measurements to see the effect on electrical degradation. This model is the first of its kind in both the CMOS and bipolar communities, and complements the electric field driven degradation model that was previously available. This was published in IEEE BCTM © 2016 [4].
4. Differences in the aging of complementary transistors (NPN+PNP) – This work explains how the differences in activation energies for the damage of the oxide interfaces of the two devices is the primary cause for accelerated degradation seen in PNP SiGe HBTs, and generalizes an analytical model for simulating complementary aging. This work was published in the IEEE TED © 2017 [5].
5. Hot-carrier-damage-induced current gain enhancement effects in SiGe HBTs – This work shows how hot carrier generation can damage both oxide interfaces and polysilicon regions of the emitter and base. A new current gain enhancement (CGE) effect is proposed that affects carrier mobilities in

polysilicon. In turn, this affects the series resistances and current gain (β) at high injection, where circuits are typically biased to extract maximum device performance. This work was published in the IEEE TED © 2018 [6].

6. Comprehensive modeling of high-temperature aging effects in SiGe HBTs – This work implements a Hydrogen diffusion model within TCAD to simulate the passivation and degradation within polysilicon, and in turn verify the electrical predictions of CGE effects in [6]. While existing aging models in the industry only predict current gain degradation due to oxide interface damage, this work identifies all relevant physical parameters in a device that can degrade at high temperatures due to hot carrier damage. This work is currently waiting for approval to submit to the IEEE TED.
7. Emitter-Base profile optimizations in SiGe HBTs for improved thermal stability and improved frequency response at low-bias currents – This work explores profile designs that look at improving device reliability by reducing power consumption and engineering temperature-independent current gain, which can be useful for minimizing thermal runaway mechanisms. This work was published in the IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) © 2018 [7].
8. A preliminary study of reliability and electrical variability in SiGe HBTs at cryogenic temperatures – This paper presents the first measurements of variability in currents due to cryogenic temperature operation for a Si diode and three different SiGe HBT platform nodes. The physics behind increased variability at low temperatures is explained with the help of TCAD. The

implications of variability on SiGe HBT reliability is also addressed. This work is currently under peer review for publication in IEEE TED.

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CHAPTER 1

INTRODUCTION

1.1 Motivation and Background for Using SiGe HBTs

In the last two decades, there have been many emerging applications requiring high-frequency circuits including radar, communication (terrestrial and satellite), and imaging and sensing using mmWave to terahertz (THz) frequency bands [8]. These applications target different audiences, including consumer gadgets, industry (automotive and aviation), military, scientific research, space exploration, and medicine, and require elegant system designs that consider the overall cost, size, and efficiency [9], [10]. For such applications, silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technology is increasingly becoming an attractive platform because of its ability to deliver III-V-transistor-like performance using a bipolar CMOS (BiCMOS) process platform that offers high levels of integration with reduced design complexity at a significantly lower cost. A wide variety of example circuits employing SiGe HBTs for mmWave and sub-mmWave applications are already available today [11]. The adoption of SiGe BiCMOS technology for low-cost high-speed mixed-signal systems continues to increase, and to support the technological front, several foundries like IHP, GLOBAL-FOUNDRIES, Tower Jazz, STMicro, NXP, and Texas Instruments are major contributors. Although it is a relatively new technology compared to traditional silicon CMOS processing, the idea of exploiting bandgap engineering to induce a drift field in the base for enhanced speed goes back to the 1950s. These graded-base SiGe HBTs can be designed with significantly better analog and RF properties (gain, transconductance per unit area, output resistance, linearity, speed, and

noise) compared to a Si BJT, while offering good compatibility and yield using standard CMOS processing [12]. These device-level advancements along with optimizations for passives [13], [14], allow for improved circuit designs for RF and analog applications.

1.2 Reliability Challenges of SiGe HBT Scaling

Just like CMOS devices, SiGe HBTs also have enjoyed the benefits of scaling, including increased speed and performance. Recent state-of-the-art SiGe HBTs showcase maximum oscillation and maximum unity-gain power frequencies (f_T / f_{max}) of 505 GHz / 720 GHz at room temperature and the barrier to THz operation continues to decrease with technology scaling [15], [16]. However, the scaling-induced reduction of operating voltages has proven to be a major reliability concern, since devices need to operate close to the safe operating area (SOA) boundaries that set the functional EOL limits for a given device. A scaled SiGe HBT with reduced breakdown voltage is more susceptible to hot carrier effects (avalanche and Auger generation) and must be carefully evaluated before being utilized in a circuit that needs a device with high-performance and reliably good EOL. Critical devices that operate in typical RF and mixed-signal circuits are subjected to mixed-mode stress (simultaneous application of both high current and high voltage stress) and can operate dynamically in various regions on the output plane consisting of either damaging or annealing regions, as shown in Figure 1.1. These regions are also driven by distinct physical processes with different temperature dependencies as operation deviates from room temperature [17], [18]. At medium to high currents, the traps created by hot carrier damage are annealed due to self-heating of the device, which can be enhanced at high temperatures. At very high currents, on the other hand, hot carrier damage caused by

Auger recombination is more prominent, and similarly has a positive dependence on temperature as shown experimentally in [18]. At even higher current levels below the electromigration limits of metal layers, the high power operation of the device causes catastrophic failures due to thermal runaway mechanisms [19]. For low to medium currents, at voltages much higher than BV_{CEO} (breakdown voltage defined by the base current reversal point), hot carrier damage is caused by impact-ionization and has a negative dependence on temperature. Being able to simulate the aging of devices following complex load lines shown in Figure 1.1 is an invaluable tool for any circuit designer needing high performance and robust reliability. First, however, a good universal physics-based model capable of predicting the accumulated stress damage seen by a device over time, electrical bias and temperature is mandatory at the device level.

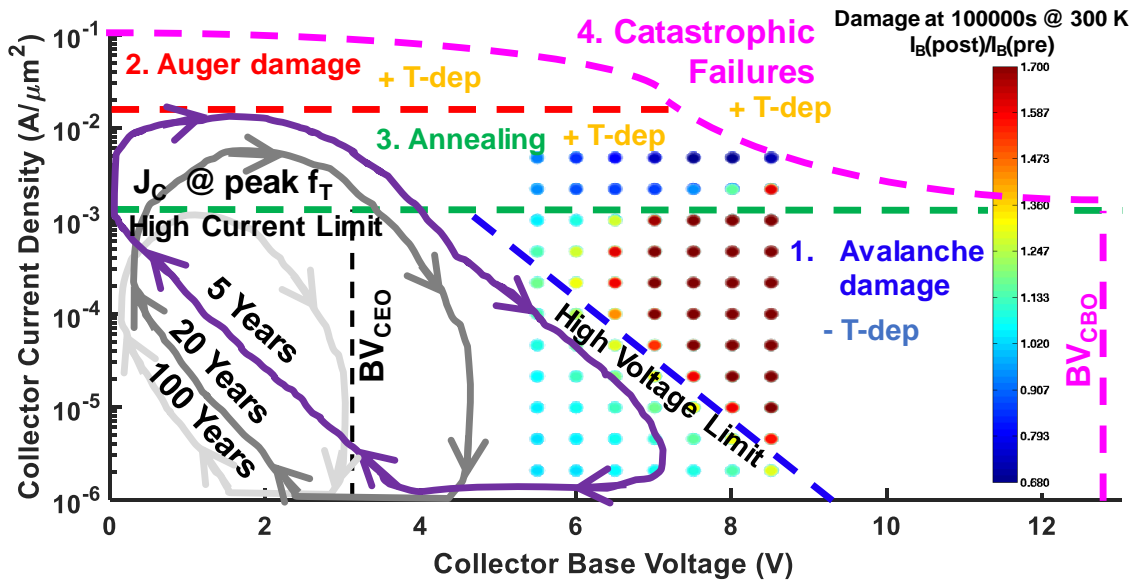


Figure 1.1: Simulated SOA of forward-Gummel characteristics degradation in an NPN SiGe HBT after 100,000 s of stress with various T-dependent damage regions

outlined. Various dynamic load lines that change the EOL of the device due to hot carrier damage are overlaid (after [3]).

1.3 Thesis Outline

The goal of this work is to develop a good understanding of degradation mechanisms in SiGe HBTs across temperature and overcome some limitations in device reliability with device profile engineering. The contents of this work are organized as follows:

Chapter 1 – an introduction to the SiGe HBT reliability problem.

Chapter 2 – an overview of SiGe HBT history and known degradation mechanisms.

Chapter 3 – describes a TCAD model for high field damage.

Chapter 4 – provides a TCAD model for high current damage.

Chapter 5 – shows how to adapt NPN models for PNP devices.

Chapter 6 – shows the physical basis for current gain enhancement and polysilicon resistance degradation effects in SiGe HBTs.

Chapter 7 – gives a TCAD model for capturing the effects in Chapter 6, along with extensive packaged measurements of high current damage at high temperatures.

Chapter 8 – discusses emitter-base profile optimizations in SiGe HBTs to overcome thermal and power limitations that can affect reliability.

Chapter 9 – explores the reliability and electrical variability of SiGe HBTs at cryogenic temperatures.

Chapter 10 – concludes the findings in this work and indicates future research directions.

CHAPTER 2

SILICON-GERMANIUM BICMOS TECHNOLOGY AND RELIABILITY

2.1 Brief History of Silicon-Germanium Technology

The structure of a modern SiGe HBT transistor is constructed with various characteristic features today for a reason. Ever since the development of the P-N junction and bipolar transistor theories by William Shockley, and the first demonstration of a point contact transistor in 1947, transistors have undergone extensive research, development, adoption, and evolution. Because of the initially insignificant speed and gain achievable in bipolar transistors, in 1957, Herbert Kroemer proposed using the following: 1) built-in electric fields independent of applied bias, and 2) a narrow bandgap base for improved emitter injection efficiency [20]. The latter is achieved by changing the alloy composition, and the former by grading the doping concentration or the bandgap. Although Kroemer's theory looked promising, due to the deficient technological development for SiGe epitaxy, the first successful demonstration (in 1987) of a SiGe HBT had to wait nearly three decades [21].

After the first proof of concept, several innovations in microfabrication methods from generation-to-generation, combined with CMOS processing methods, were needed to allow the rapid growth of faster SiGe HBT technology platforms over the years as shown by several roadmaps [8]–[10]. Beginning with the advancement of a low thermal budget (< 600 °C) UHVCVD process for SiGe HBTs in 1988, a high throughput, yet commercially

reliable production of SiGe HBTs was a possibility since December of 1994 [22], [23]. The first-generation process (> 50 GHz f_{max}) integrated the bipolar base after the CMOS gate flow to minimize the thermal cycle. Although the first-generation devices avoided the conventional high thermal Si epitaxy (> 1000 °C) of the 1980s, building narrow base widths in the second generation onwards (> 100 GHz f_{max}) required the incorporation of carbon during the epitaxy for suppressed boron diffusion [24]–[26]. In many second-generation devices, improvement of f_{max} came at the expense of a lowered f_T due to increasing parasitic capacitances and resistances with lateral (aimed at CMOS process flow) and vertical optimizations (steep doping and SiGe alloy grading) [27]–[29]. This problem was addressed in the third- (> 200 GHz f_{max}) and fourth- (> 400 GHz f_{max}) generation SiGe BiCMOS platforms with the introduction of a raised extrinsic base, which reduced the base resistance while also minimizing the collector-base and emitter-base overlap capacitances with better separation [30]. Lastly, adding lower doped regions to the emitter-base and base-collector transitions (for lowered parasitic capacitance) have allowed the creation of faster transistors (720 GHz f_{max}) that continue to bridge the gap to the THz barrier [15].

2.2 Overview of Competing Degradation Effects in SiGe HBTs

The vertical and lateral scaling of SiGe HBTs has led to junctions with large built-in fields and also smaller isolation layers (oxides and nitrides) separating the different terminals. As a result, for the same bias condition, this has led to the generation of more energetic hot carriers in scaled technologies. In addition, since these hot-carriers have less distance to traverse and physically damage vulnerable regions of a device, they can cause significantly more damage. As a result, scaling imposes restrictions on breakdown voltages

and SOAs for devices. In order to quantify the reliable EOL and also quickly observe the electrical tolerance and degradation of SiGe HBTs, aggressive bias (high electric field and high current) and temperature conditions (well above and below room temperature) are often used to stress devices at an accelerated pace. The effects of these stresses can be categorized into “hard” and “soft” damage. The former consists of a catastrophic failure triggered by the high power operation of a device [19]. During this failure process, under very high current or very high voltage conditions, a device undergoes electro-thermal feedback and current pinch-in mechanisms as shown by Figure 2.1. Such conditions can physically melt and fuse the collector, base and emitter junctions, effectively turning the transistor into a resistor [19]. In contrast, “soft” damage is described by the degradation of electrical performance (current gain, noise and frequency response) over time due to physical damage by hot carriers. Figure 2.2 shows that the transistor nature in the Gummel characteristics is preserved despite the “soft” damage (trap accumulation) in the device.

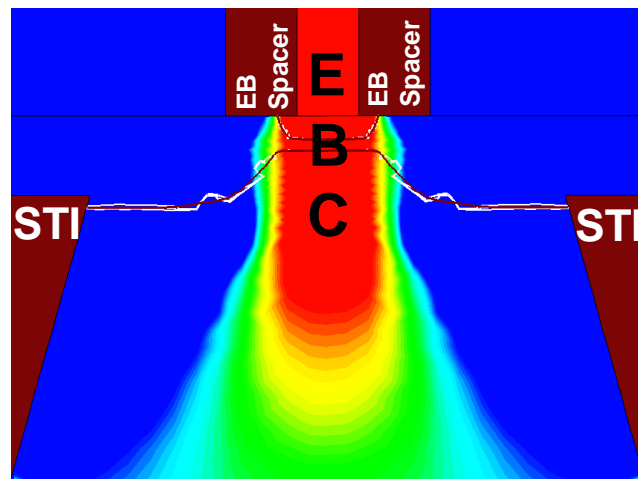


Figure 2.1: TCAD cross section showing current density through a fourth generation SiGe HBT under a high power condition of $J_E = 50 \text{ mA}/\mu\text{m}^2$ and $V_{CB} = 4 \text{ V}$. Current constricts towards the center of the device under high voltage operation, eventually triggering catastrophic thermal runaway of the device.

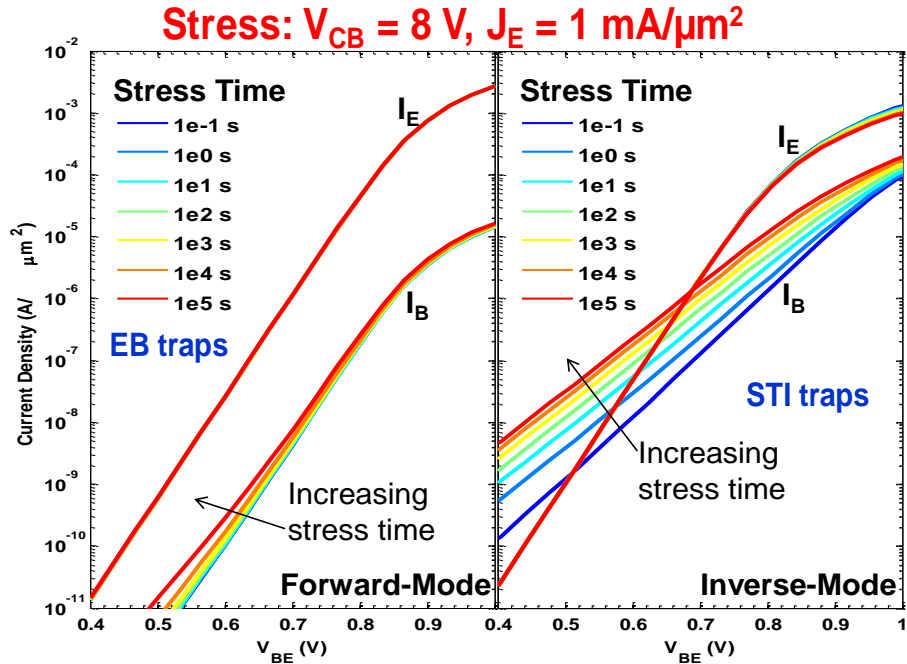


Figure 2.2: TCAD simulation of increasing base leakage current due to hot carrier damage following a high voltage stress. Forward and inverse mode operation of the SiGe HBT samples the base leakage due to EB and STI oxide traps (after [31]).

This thesis will primarily focus on providing models for transient performance degradation due to hot carriers in SiGe HBTs. Physical damage translates to electrical changes in a SiGe HBT that can broadly be recognized by three distinguishable regions in the change of Gummel characteristics shown in Figure 2.3. Of the three regions indicated, Region 1 has been the most studied and modeled. It is characterized by a strong increase in the base leakage current that degrades current gain, and can be described by the classical depassivation of the Si-H bonds along the emitter-base (EB) and shallow-trench (STI) oxide-silicon interfaces. The hot carrier sources and mechanisms that are capable of altering electrical behavior in this region will be discussed briefly in Sections 2.2.1 to 2.2.3, and more in detail in Chapters 3, 4 and 5. In contrast to Region 1, Region 2 is characterized by a decrease in the base current, suggesting an enhancement in current gain. In addition, Region 3 shows an increase in base and collector currents, suggesting a change in the

emitter resistance. The cumulative behaviors of Regions 2 and 3 have largely been attributed to the degradation of the polysilicon emitter [18]. Chapters 6 and 7 will demonstrate how the hot carrier sources that affect Region 1 can also cause changes in Regions 2 and 3.

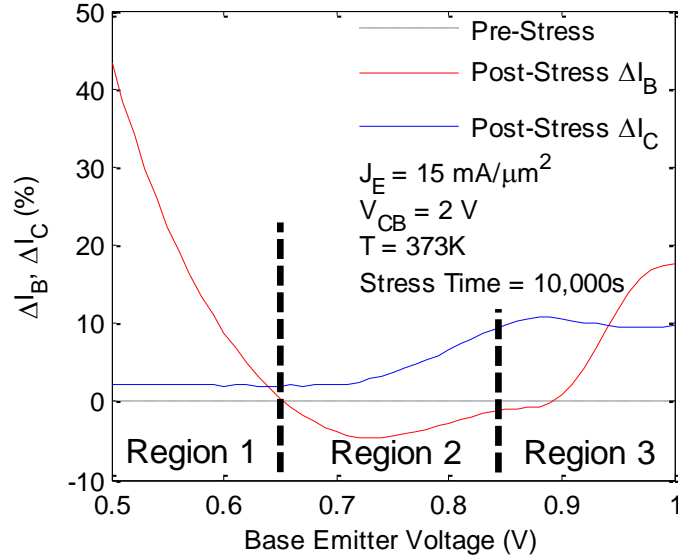


Figure 2.3: Measured change in the Gummel characteristics of a NPN SiGe HBT following high-current stress of $V_{CB} = 2$ V, $J_E = 15$ mA/ μm^2 (after [18]).

2.2.1 Avalanche-Generated Hot Carriers

High electric field stresses (mixed-mode and reverse-EB) have been the most commonly used and well-studied methods for inducing hot carrier damage in SiGe HBTs [17], [32]–[34]. During mixed-mode stress, hot carriers are generated in the collector-base (CB) space-charge region due to the acceleration of injected minority carriers by the high electric-fields as shown in Figure 2.4. These carriers can once again produce electron-hole pairs via impact ionization, thus leading to a temperature-dependent avalanche generation of energetic carriers. If these carriers have sufficient energy from the field acceleration, they can travel towards the EB and STI oxides and displace hydrogen (H) atoms used to

passivate the Si dangling bonds at the oxide-silicon interfaces. This causes H atoms to diffuse away from the interface, producing a net increase in interface traps. This ultimately leads to an increase in base current to compensate for trapping and de-trapping events occurring at the EB and STI interfaces as shown by Figure 2.2. Under reverse-EB bias stress, the large electric field across the EB junction enables band-to-band tunneling and also accelerates the generated carriers, making them capable of damaging oxide interfaces in a process similar to mixed-mode stress.

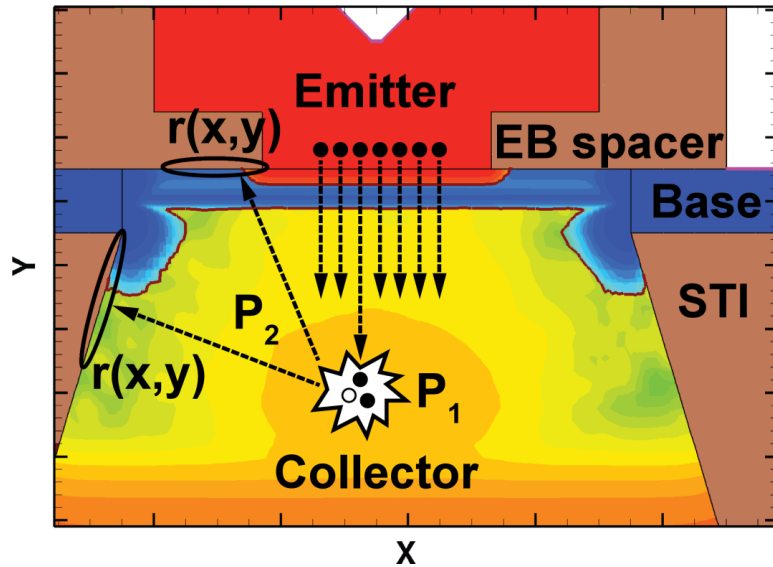


Figure 2.4: Hot carrier generation and transport to oxide interfaces under mixed-mode stress (after [31]).

2.2.2 Auger-Generated Hot Carriers

Similar to the high-field stresses, high-current stresses have also been known to cause damage to the Gummel characteristics [18], [35]–[37]. When SiGe HBTs are operated close to or beyond the peak f_T current density, the emitter-base (EB) field collapses and the neutral base and emitter are filled with carriers recombining via the Auger process. In the Auger process, an electron-hole pair recombines and donates the energy to

a nearby carrier. The recipient hot carrier will roam about the low-field region until it loses kinetic energy through momentum robbing collisions. In order for the hot carrier to cause damage to oxide interfaces, it must have sufficient energy to break Si-H bonds, and is known to be around 2.3 eV [38]. As the Auger hot carrier will have kinetic energy close to the bandgap (E_g), an Auger hot carrier generated in silicon ($E_g = 1.1$ eV) should not have sufficient energy for producing damage. If current density within the device is high enough, however, simultaneous recombination events can lead to a single carrier receiving the energy of multiple recombination events (with limited probability) as illustrated in Figure 2.5. This generation of energetic hot carriers near the EB junction via the Auger process was first offered as an explanation by [37] to explain the electrical degradation seen under high-current stress in Si BJTs. The Auger-generated hot carriers at the EB junction can travel to the oxide interfaces and cause damage in a manner similar to the avalanche-generated hot carriers as shown in Figure 2.6.

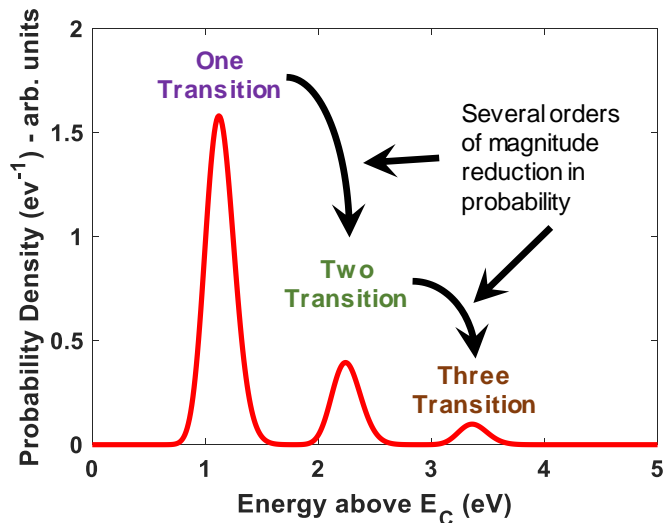


Figure 2.5: Probability distribution of hot electrons with multiple simultaneous Auger transition energies in silicon.

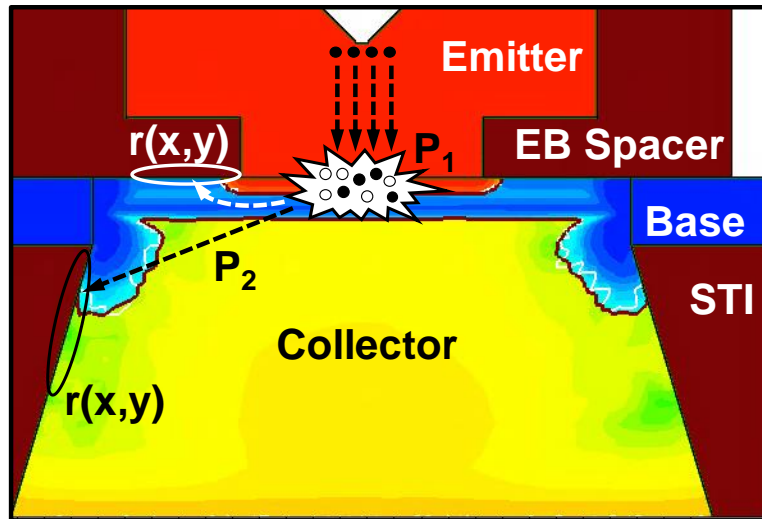


Figure 2.6: Auger hot carrier generation and transport to oxide interfaces under high-current stress.

2.2.3 Trap Annealing

Dangling bonds at oxide interfaces are passivated in SiGe HBTs with atomic hydrogen, which helps move the trap states outside of the semiconductor bandgap [39]. When the Si-H bonds are broken due to impingement by energetic carriers, an equal concentration of hydrogen and traps are created at the oxide interface that can subsequently participate in the annealing reaction of recreating this Si-H bond. Regardless of the mechanism responsible for damage at oxide interfaces, post-damage, this annealing phenomenon is always present and will try to counter any further damage, provided there is sufficient thermal energy. However, this thermal energy can go both ways in that it not only facilitates the creation of the Si-H bond, but also aids in diffusing the atomic hydrogen deeper within the oxide. Even slight changes to the local interface temperature due to different bias conditions can swing the reaction rate either way. The overall effect of self-heating can have a complex effect on the short term and long-term device degradation and

recovery on the output plane due to the temperature dependencies of the different dynamic damaging and annealing components.

2.3 Extent of SiGe HBT Reliability Modeling in Literature

Modeling the different hot carrier degradation mechanisms in Section 2.2 consists of two main components: 1) the process by which hot carriers are generated (indicated by P_1 in Figure 2.4 and Figure 2.6) and transported (indicated by P_2 in Figure 2.4 and Figure 2.6) to vulnerable regions (oxide interfaces and polysilicon) of the device and 2) the dynamic degradation and annealing processes at those regions. The lucky-electron (carrier) model was originally proposed for the first component in MOSFETs, and captured the field-induced hot-electron tunneling and gate leakage currents [40]–[42]. This model has been in use for several years and was also adapted for modeling mixed-mode stress degradation in SiGe HBTs under both compact modeling and TCAD environments [31], [43]. For the second modeling component, the reaction-diffusion (R-D) formalism was first proposed for MOSFETs in order to track the interface trap creation along the gate oxide interface that is responsible for bias temperature instability [44]. This model too was assimilated for SiGe HBTs and has helped in monitoring the trap creation at the EB and STI interfaces, which increases low-injection base current leakage [31], [43].

Although the lucky-electron model is advantageous in terms of simulation time, it can be inaccurate as it assumes instantaneous hot carrier generation and transport to oxide interfaces primarily based on the local electric field and current density. In reality, however, the creation of energetic hot carriers responsible for damage involves multiple excitations. An accurate solution for the energy distribution of carriers at an oxide interface

would require a full-band solution to the Boltzmann Transport Equation (BTE). Using spherical harmonic expansion (SHE), the BTE can be solved without resorting to Monte Carlo methods, which can be time-consuming and noisy [45]. An approach coupling carrier energies using the SHE method to multistate trap configurations has also been applied for modeling SiGe HBT aging [46].

While accurate hot carrier generation and transport models are important, they also need to be coupled with accurate interface degradation models for simulating device aging. At the hearts of all interface degradation models are some variant of the depassivation of the Si-H bond. According to the R-D model, which has been in use for nearly four decades, the interface degradation is limited by the diffusion of hydrogen inside the oxide. In the last decade, however, the accuracy of this model for predicting the amount of recovery under negative bias temperature instability (NBTI) in MOSFETs has been questioned. For NBTI, the leading alternative explanation for R-D is the trapping and de-trapping of pre-existing hole traps at the oxide interface without involving any hydrogen diffusion [47]. This process shows very minimal annealing even at elevated temperatures, suggesting a damage mechanism that is reaction-limited [48]. Instead of a diffusion-limited process, this reaction-limited approach for modeling hot carrier damage has also been applied in SiGe HBTs using SHE for hot carrier energy calculation [46]. Given the differences in the size and shape of the oxides, the electric fields along the oxides can differ by several orders of magnitude in SiGe HBTs and MOSFETs. Moreover, the degradation mechanisms for NBTI and hot carrier damage differ vastly in terms of temperature dependence, the carrier energies in play, and degradation in SiGe HBTs usually cannot be recovered [49]. This is

one of the main reasons why the degradation mechanisms in MOSFETs and SiGe HBTs may not necessarily be the same, and that R-D may still be applied for SiGe HBTs.

Aside from the TCAD based degradation models, in recent years, compact models incorporating different power laws for aging have also been proposed [49], [50]. However, they are often technology-specific and would require measurement of reliability and an empirical model calibration before the device EOL can be estimated. Moreover, most of the models have only been calibrated for estimating oxide interface damage and have not explored current gain enhancement and polysilicon resistance degradation as suggested by Regions 2 and 3 in Figure 2.3. Many of these models are very simplistic and are either good at predicting the short-term aging effects or the long-term effects, but not both. Lastly, the modeling efforts in SiGe HBTs have been predominantly only in NPN devices. The investigation in [34] examined the aging of complementary SiGe HBTs and concluded that a bias dependent mismatch in the degradation of complementary devices exists. For both aggressive and equal mixed-mode and reverse-EB stress conditions, PNP SiGe HBTs showed accelerated degradation compared to their NPN counterparts. Previous literature offers very little conclusive and experimental evidence to explain this behavior. A universal TCAD degradation model with push-button reliability for both NPN and PNP SiGe HBTs capable of predicting high injection gain enhancement effects, resistance degradation, and oxide interface damage across temperature due to multiple biasing schemes does not exist as of today.

CHAPTER 3

ACCUMULATED STRESS MODELING OF MIXED-MODE DAMAGE IN SiGe HBTs

This work uses a physics-based TCAD degradation model from [31] to examine the accumulated stress damage of SiGe HBTs under pseudo-dynamic mixed-mode stress as a function of both electrical stress bias and temperature. The temperature dependence of mixed-mode stress damage is fully explored, beginning with impact-ionization calibration, and then by identifying and calibrating the dependence of scattering length and hydrogen diffusion parameters of the degradation model. After calibrating the model across electrical bias and temperature, the effectiveness and limitations of accumulated stress damage while varying electrical bias and while varying temperature are identified, and the implication of this aging model for circuit designers is discussed. The analysis in this chapter resulted in three published works [1]–[3].

3.1 Motivation

In [31], a physics-based TCAD degradation model built in the Synopsys Sentaurus environment was first presented and used to calculate the bias dependence of hot carrier generation and arrival at various oxide interfaces for trap formation during electrical stress [42], [43], [51], [52]. Figure 1.1 shows the simulated mixed-mode stress map using this model for a single device exposed to various mixed-mode stress conditions. To demonstrate the effectiveness and usefulness of this model in predicting the damage response due to dynamic stress conditions illustrated in Figure 1.1, the accumulated stress

degradation due to time-dependent pseudo-dynamic mixed mode stress will be examined. The temperature dependencies in the model are also calibrated to measured damage responses. To verify these refinements in the model, stress damage accumulated across temperatures is compared between both measurements and simulations. Having an accurate temperature dependence for the damage physics is necessary not only for circuits operating over finite temperature ranges, but also for considering inherent self-heating effects with operating devices. The accuracy and limitations associated with this calibrated TCAD model for predicting the degradation of devices with dynamic operation in circuits are identified.

3.2 Damage Physics of Mixed-Mode Stress Degradation

As mentioned in Section 2.2.1, high electric fields under mixed-mode stress accelerate carriers and provide them with the energy necessary for depassivating oxide interfaces and generating trap states. From the time that a carrier is generated by impact ionization, the entire trap formation sequence can be given as a product of three probabilities using the lucky electron model. In order to create a trap, a carrier must: 1) obtain sufficient energy to create a trap; 2) get redirected to the EB or STI oxide; and 3) not undergo a subsequent energy-robbing collision before finally reaching the oxide [40], [42], [53]. These requirements are implemented in the model by probability equations (3.1), (3.2), and (3.3), respectively. All three of these probabilities are dependent upon temperature, with the dependence coming from the mean-free-path lengths (λ and λ_r) between collisions. The hot carrier probability depends on the effective electric field (F_{eff}) based on hydrodynamic transport. Here, ϕ_{hot} is the energy required to liberate a H atom

from the Si-H bond and produce a trap at the interface. Both the avalanche generation process and the sequential transport of hot carriers to oxide interfaces are essential to the trap formation and the temperature dependencies of both will be analyzed after proper calibration to data.

$$P_{hot, e/h}(\epsilon, x, y) = \frac{1}{\lambda F_{eff}(x, y)} e^{\frac{\epsilon}{\lambda F_{eff}(x, y)}} d\epsilon \quad (3.1)$$

$$P_{red}(\epsilon) = \frac{1}{\lambda_r} \left(1 - \sqrt{\frac{\phi_{hot}}{\epsilon}} \right) \quad (3.2)$$

$$P_{dist}(x, y) = e^{-\frac{d}{\lambda}} \quad (3.3)$$

3.3 Impact-Ionization Calibration

Before examining the temperature dependence of the damage physics, it is important to first ensure that avalanche generation is calibrated properly within the TCAD model, as this is the source for the hot carriers that ultimately cause damage at the oxide interfaces. The Okuto-Crowell impact-ionization model was calibrated to measurements and further used to simulate the avalanche generation process, as it provides a good empirical fit across a wide range of temperatures. In this work, the device used for simulations and measurements has a BV_{CEO} of 3.5 V, BV_{CBO} of 16.8 V, and J_C of 1 mA/ μm^2 at peak f_T . Figure 3.1 shows the calibration of avalanche multiplication (M-1) across different current injection levels and across temperatures for an NPN SiGe HBT. In order to suppress high current induced effects such as self-heating on the avalanche process, low

current injection was used for the temperature calibration of M-1. It is evident from the figure that shifting to a higher operating temperature reduces M-1 due to energetic phonons obstructing carriers from undergoing avalanche multiplication. In particular, voltage margin is available when shifting to a higher temperature before seeing a comparable level of impact ionization. For example, moving from 300 K to 373 K for an M-1 of 0.4 yields a margin of 0.45 V. As a result, the net quantity of hot carriers reaching the EB and STI oxide interfaces at elevated temperatures is reduced, impeding the trap creation at the oxide interfaces during stress.

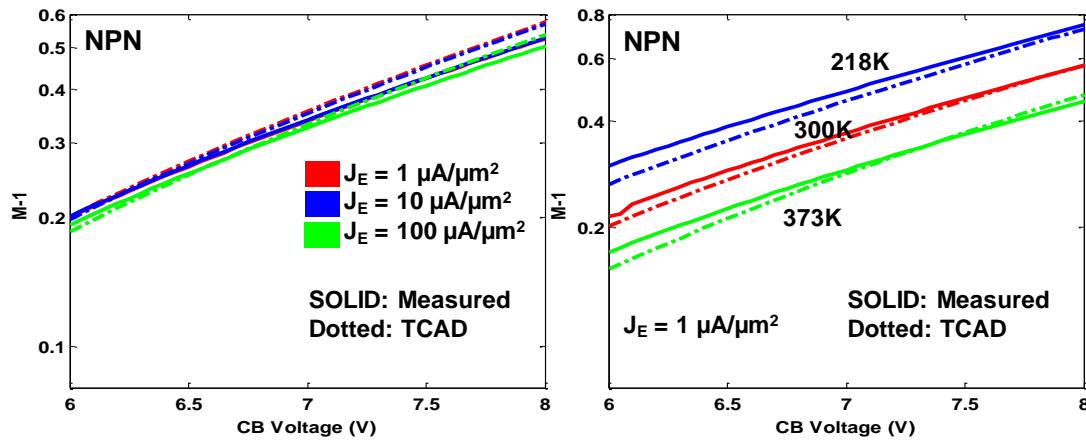


Figure 3.1: Calibration of avalanche multiplication across varying current levels and across temperature.

The effects of impact ionization can be readily visualized on a stress map, as shown in Figure 1.1. Mixed-mode stress to a device causes damage to commence at aggressive stress conditions at high voltages and high currents, and then slowly escalate to low voltage and current conditions over time. High voltage directly translates to high electric fields, which enhances impact ionization. High currents also increase the availability of hot carriers until impeded by Kirk and barrier effects, which not only reduce the peak F_{eff} by widening the base but also by pushing the peak F_{eff} deeper within the CB space-charge

region and away from the EB oxide interface [31]. These high current effects impede hot carrier generation and transport to the EB spacer and define the high current SOA boundary around J_c at peak f_T . The SOA boundary at low voltages is largely a function of the stress time used to evaluate the device due to low electric fields and hot carrier rates at these conditions. Longer EOL stress conditions will yield a smaller SOA boundary in voltage. Thus, the SOA boundary is limited at low voltages due to stress time and at high currents due to high injection effects. This SOA as defined by the high damage region with two bounding limits follows impact ionization and shifts higher in voltage when a device is operated at an elevated temperature. With the M-1 model calibrated, the temperature dependence of the degradation model can now be analyzed.

3.4 Mixed-Mode Damage Temperature Dependence

The net temperature dependence of the damage response to mixed-mode stress is a product of three steps. First, impact-ionization, as the generation source of hot carriers, is a temperature dependent process as shown above. Next, the fraction of hot carriers reaching the oxide interfaces is also a temperature dependent process governed by the mean-free-path length between collisions for hot carriers at each temperature. Lastly, the diffusion of hydrogen away from an interface is also a complex temperature dependent process. In this section, the models used for hydrogen diffusion and the temperature dependence of mean-free-path length will be discussed. This work assumes the R-D model given by (3.4) for trap creation, and uses the analytical approximation given by (3.5) to analyze the temperature dependence of important parameters and conveniently perform damage calibrations [44]. The trap evolution at an oxide interface is given as a function of the

impingement rate of hot carriers (K_F), the maximum interface trap concentration (N_0), trap annealing rate at a given temperature (K_R), hydrogen concentration (H_2), and hydrogen diffusion constant (D).

$$\frac{\partial N_{it}}{\partial t} = K_F(N_0 - N_{it}) - K_R N_{it} H_2 \quad (3.4)$$

$$N_{it} \approx 1.16 \sqrt{\frac{K_F N_0}{K_R}} (Dt)^\alpha \quad (3.5)$$

Hydrogen in a crystalline lattice produces two kinds of traps. One is a shallow-level trap associated with a H atom occupying an interstitial site (also called Bond Center or BC) of a bond between two silicon (Si) atoms. The other trap is a deep-level trap associated with a physical bond between a Si atom and a H atom. Just like the dichotomy in states due to the formation of conduction and valence bands in a semiconductor, H in the crystalline Si system manifests itself as a system of two states [54], [55]. Each state has an energy distribution centered on the peak trap energy, as shown in Figure 3.2. At the minimum between the two energy distributions of trap states lies the chemical potential of H. Below this energy level, H trap states are mostly occupied, and above this level, the traps associated with the dangling bond are mostly empty.

In order for interstitial diffusion of H to take place, the H atom must gain sufficient energy to be promoted to the saddle point for migration. H diffuses by hopping over an energy barrier E_M from one interstitial site to another. This energy E_M takes on values from 0.2 eV to 0.6 eV depending on the process that was used to grow the Si and embed the H

[55]. In this study, the following Arrhenius relationship is used, with $D_0 = 9.41 \times 10^3 \text{ cm}^2/\text{s}$ and $E_M = 0.48 \text{ eV}$ to take into account the thermally-activated process of interstitial diffusion [56]. The following behavior introduces temperature dependence into the interface trap creation, as given by (3.6):

$$D(T) = D_0 e^{-\frac{E_M}{kT}}. \quad (3.6)$$

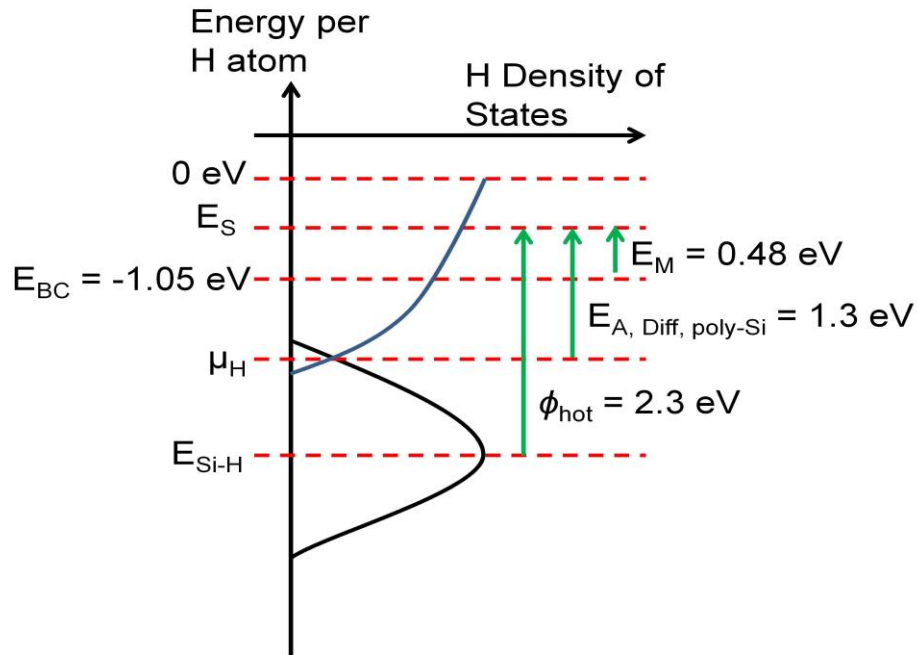


Figure 3.2: Distinct trap states in Silicon and the associated activation energies required for diffusion of hydrogen.

H diffusion at an oxide-Si interface is a two-step process. First, a H atom must be liberated from a Si-H bond to create a dangling bond and occupy an interstitial site. The H atom can begin diffusing only then. The energy of the trap associated with a dangling bond (E_{Si-H}) is 1.9 - 2.5 eV below the energy for the Bond Center (E_{BC}) depending on the temperature at which the interface was passivated [57]–[59]. A higher passivation

temperature results in a dangling bond trap with a lower energy with respect to the free space energy of H. Therefore, a higher passivation temperature increases the spacing between E_{BC} and E_{Si-H} . In this work, the activation energy (φ_{hot} in the degradation model) required to promote a deep trap to a shallow trap was assumed to be 2.3 eV, following the analysis in [38]. Although a transition of a H atom from a deep trap to a shallow trap is occurring in energy, the actual transition must happen physically by breaking a Si-H bond, leaving a dangling bond behind and subsequently moving the H atom to the nearest Si-Si interstitial site. The physical movement is a diffusion limited step and is temperature dependent. At very low temperatures, the H atom has great difficulty in making the spatial transition and therefore has great difficulty in making the transition from E_{Si-H} to E_{BC} , even when supplied with sufficient energy. The only way to increase the chances of creating a trap at low temperatures is by bombarding the interface with more hot carriers. Despite the reduction in diffusion constant, more traps are created at low temperatures in a SiGe HBT because of the increase of hot carriers reaching oxide interfaces due to the increase in mean-free-path length below 300 K. This will be shown in the next section.

In the damage physics model for the SiGe HBT, the three probability equations (3.1) – (3.3) involve two different mean-free-path lengths (λ and λ_r). Here, λ is an average of optical phonon scattering, impact-ionization, and long-wavelength acoustic phonon scattering, and λ_r is an average of long-wavelength acoustic phonon and intervalley scattering [60]. Optical phonon scattering is the dominant inelastic scattering suffered by carriers in the collector-base space charge region during impact ionization. On the other hand, in order for a carrier to be redirected, an elastic collision must take place between the lattice and carrier. Redirecting collisions happen with a lesser frequency and therefore λ_r is

a factor of 5 - 10 larger than λ at room temperature [41]. However, the exact value of λ_r is not as significant since λ is a more sensitive parameter since it occurs in the exponents of the driving functions. To minimize any scattering of carriers from a crystalline Si lattice, the ideal temperature to operate is 0 K. At very low temperatures, the maximum mean free path length (λ_0) is determined based on the geometry of the lattice. As the temperature is increased, phonons are introduced into the lattice with different harmonics and begin to interact with one another and with the flow of carriers. The operating temperature is directly proportional to the number of phonons introduced, and the number of phonons in the lattice is directly proportional to the collision frequency of phonons in the lattice. As collision frequency increases with temperature, the mean distance traveled by a carrier decreases inversely. Thus, at very high temperatures the mean free path length is expected to drop as T^{-1} . (3.7) gives an analytical expression for the temperature dependence of both mean scattering lengths [41], [60]. The implementation of the above-mentioned physics in calibrated TCAD models and the limitations will be discussed in the next sections.

$$\lambda(T) = \lambda_0 \tanh\left(\frac{E_p}{2kT}\right) \quad (3.7)$$

3.5 Damage Calibrations Over Electrical Bias and Temperature

Before examining the effectiveness of the TCAD model in predicting the accumulated stress damage of a SiGe HBT, it is necessary to define the boundaries of the electrical bias space and temperature space over which the device will be compared for accuracy between simulations and measurements. Figure 3.3 shows 5 points that have been

chosen on the output plane for calibration across different bias at room temperature. For the bias dependent stress damage calibration at room temperature, Figure 3.4 shows a good fit between measurements and simulation were achieved by tuning (λ) to 6 nm. The degree of damage experienced by each point is determined by F_{eff} and impact ionization. The temperature range examined in this study is from 218 K to 373 K. The base current degradation from the Gummel characteristics under forward-mode operation is used as a figure-of-merit (FoM) for stress damage.

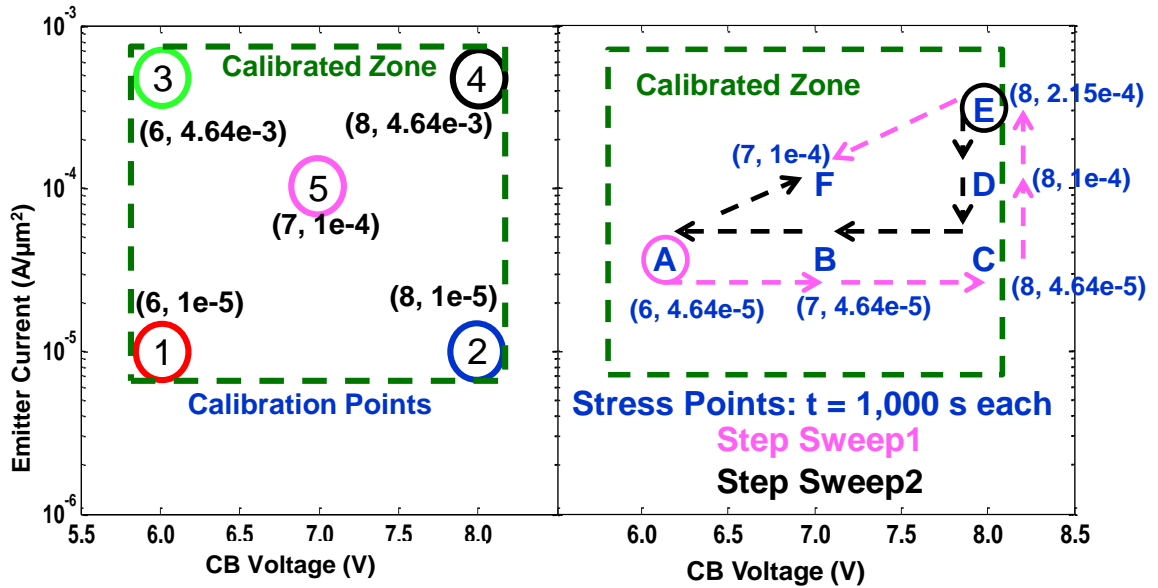


Figure 3.3: Five points for damage calibration marked on the left with numbers 1-5. Six points for measuring accumulated damage marked on the right with letters A-F. Two paths for accumulating stress damage are marked with pink and black arrows.

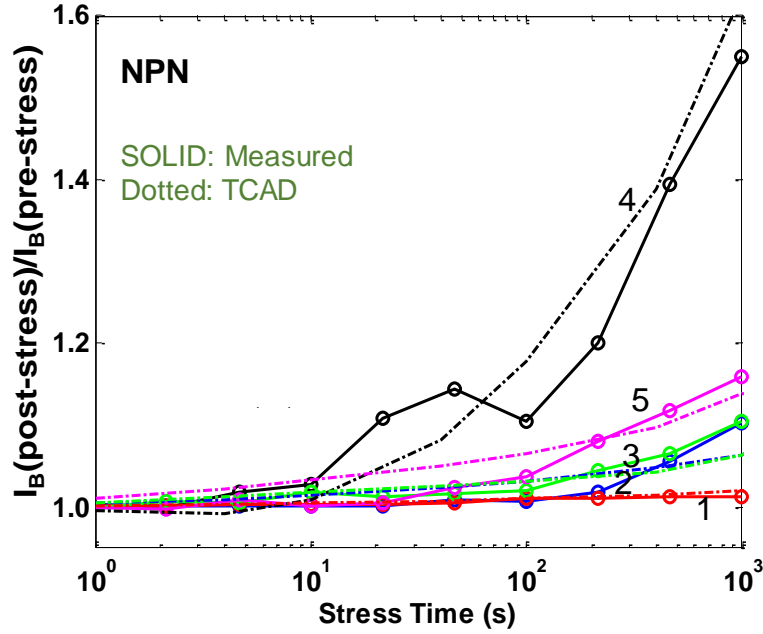


Figure 3.4: Degradation (I_B increase) from forward-Gummel characteristics measured at $I_C = 0.1 \text{ nA}/\mu\text{m}^2$ for the 5 calibration points from Figure 3.3.

The inverse temperature dependence of mean-free-path length predicted by physics was observed when calibrating the measured damage to the simulated damage using different mean-free-path lengths for different temperatures. Figure 3.5 shows the calibration of mixed-mode damage across three different conditions. A stress condition in the impact-ionization dominated region was chosen such that enough damage could be observed within 1000 s across the three temperatures. Figure 3.6 shows a good correlation between a T^{-1} curve and the mean-free-path lengths used at three temperatures for calibrating mixed-mode-damage. Figure 3.7 shows the hot carrier rates at each temperature. The exponential reduction in hot carrier rates with temperature was enabled by the exponential enhancement of the diffusion coefficient. Although there is increased damage at 218 K, this behavior is not expected at lower temperatures because of the saturation of λ due to geometrical limits.

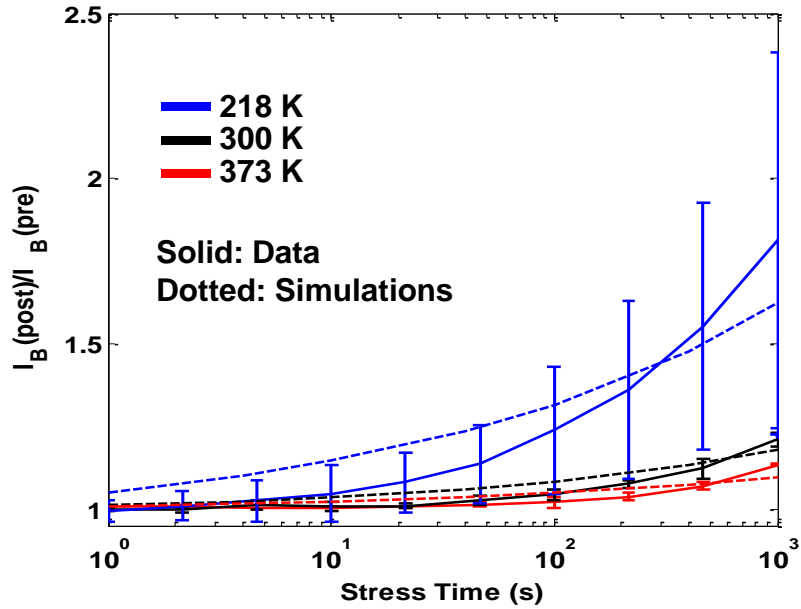


Figure 3.5: Calibration of simulations to measurements for I_B degradation over temperature for a stress condition of $V_{CB} = 8.5$ V and $J_E = 0.464$ mA/ μm^2 . The base current degradation is extracted at $J_C = 10$ nA/ μm^2 from forward-Gummel Characteristics. Vertical error bars show the spread of data across 3 devices.

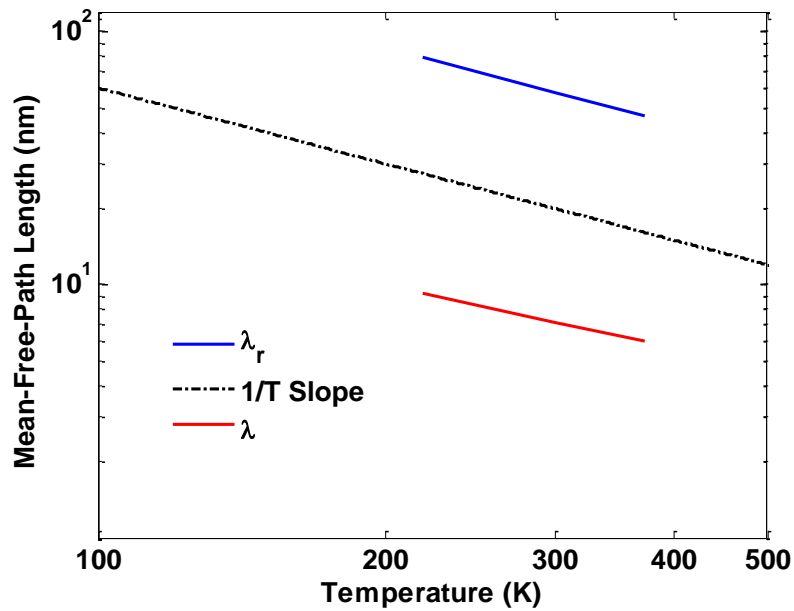


Figure 3.6: Temperature dependence of λ and λ_r . These are the values used for the calibrations in Figure 3.5.

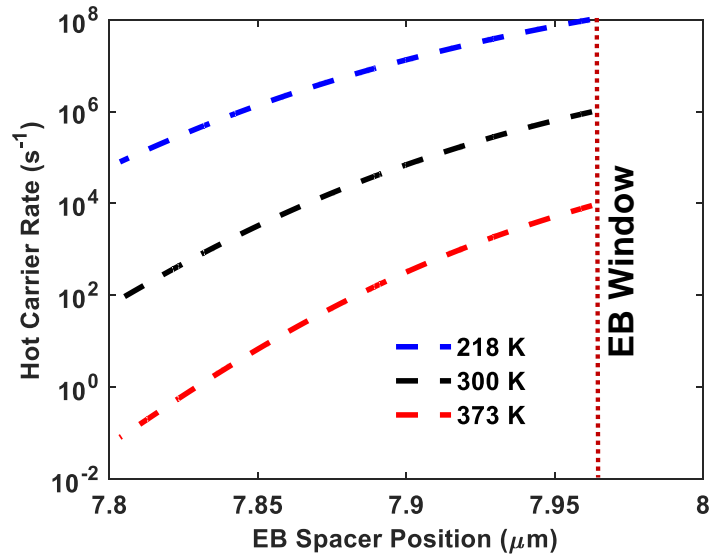


Figure 3.7: Simulated Hot carrier impingement rates at EB spacer over temperature.

In Figure 3.5, although it appears that the simulation is initially overestimating the damage during the first 200 s of stress, this is an artifact of assuming diffusion-limited trap creation, (3.5), and a constant annealing rate for K_R . In reality, annealing is a very dynamic process dependent on both the hydrogen and trap concentrations at or near the oxide-silicon interface. Due to the growth process of SiGe epitaxy, hydrogen is inherently present in the epitaxial layers and can diffuse and anneal traps. Measurements show very minimal damage for all three temperatures during the initial 10 - 100 s of stress. This can be attributed to a dynamic equilibrium between damaging and annealing reactions due to the local presence of hydrogen. As this hydrogen concentration falls with diffusion, the trap creation then becomes diffusion limited as seen during longer stress periods in measurements. The current TCAD model cannot capture the dynamic equilibrium behavior since it assumes a constant annealing behavior and does not monitor the concentrations of hydrogen within the device. Once proper hydrogen diffusion and annealing models are in place, the simulation should more closely resemble the measured behavior.

3.6 Accumulated Stress Damage

After calibration to data across electrical bias and temperature, stress sweeps need to be defined for looking at the accumulated stress damage seen by a device. The bias sweeps used in this study at room temperature are given by six points labeled A-F in Figure 3.3. The two sweeps will comprise of stressing the six points in clockwise and counterclockwise directions on the output plane starting at points E and A, respectively, and ending at stress point F. For over-temperature sweeps, five equally spaced temperatures have been taken from 218 K to 373 K for sequential stressing in both ascending and descending temperatures for a stress bias of $V_{CB} = 8.5$ V and $J_E = 0.464$ mA/ μm^2 .

For the bias sweeps, points E and A have the most aggressive and least damaging stress conditions, respectively, as clearly seen from the impingement rate of hot carriers at the EB spacer, as shown in Figure 3.8. Similarly, 218 K and 373 K have the most and least damaging mixed mode stress conditions, as seen from the hot carrier rates shown in Figure 3.7. As these rates are integrated sequentially over the different stress conditions, traps evolve over time as shown by the accumulated traps at the EB interface for the different bias sweeps in Figure 3.9. A key point to note is that the traps accumulated over the two different sweeps clearly show a bifurcation at the start of the stress sweeps due to the disparity in the hot carrier rates between the two initial conditions (A and E). More importantly, the trap accumulation across the two sweeps converges after 5000 s and overlaps during the final common stress sweep E. Although not shown, a similar diverging and converging behavior is expected for the trap accumulation across the two different

temperature sweeps since they both start at two different extremes of temperatures and end similarly at the extremes.

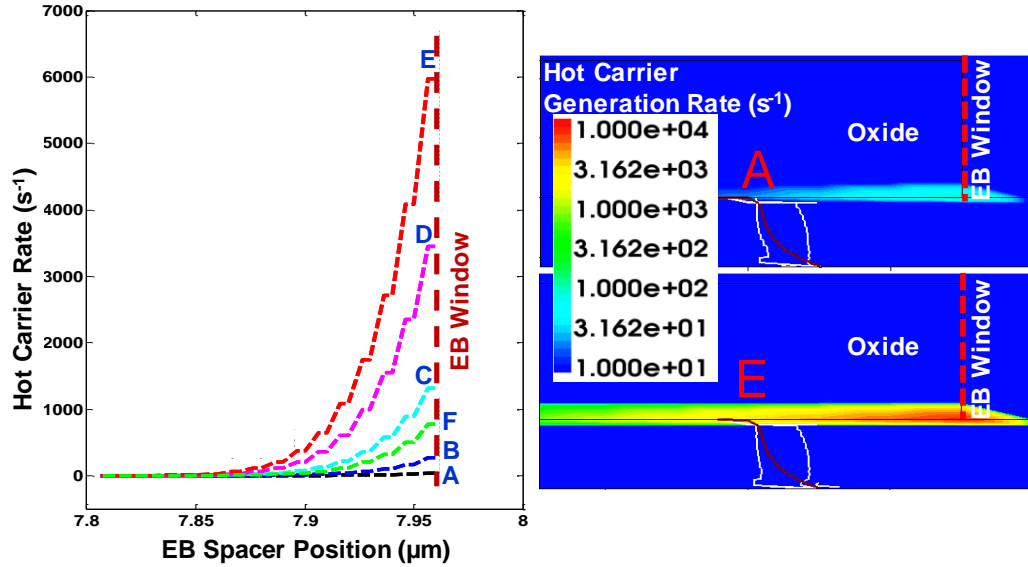


Figure 3.8: Simulated Hot carrier generation rate at EB spacer after 10 s of stress on the left. 2-D cross-section of the rate for stress points A and E shown on the right.

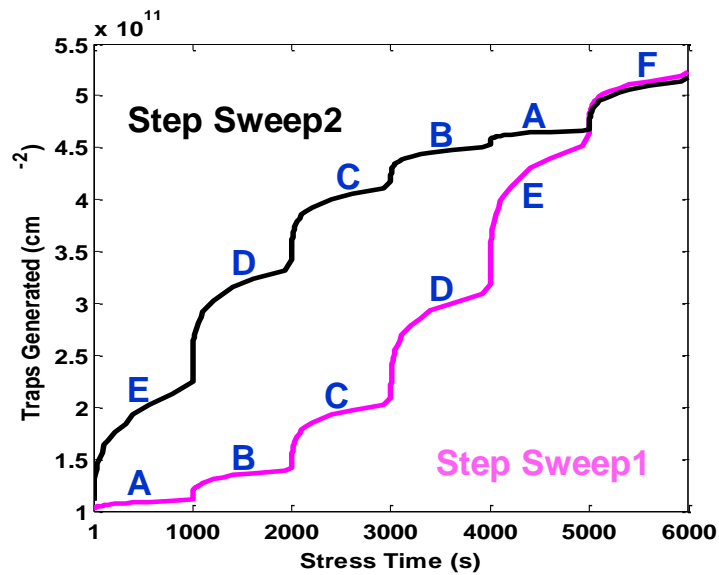


Figure 3.9: Peak Trap concentration at EB spacer over the two different stress sweeps. The stress condition associated with each stress period of 1000 s has been identified with labeling convention from Figure 3.3.

The diverging and converging behavior seen in the trap accumulation directly manifests itself in both measured and TCAD accumulated damages, as shown by the base leakage degradation for the bias sweeps at room temperature in Figure 3.10. From this, [2] offered the idea that while simulating the degradation seen by a device over a dynamic load line confined to the damage region defined by impact ionization, a simple integration of traps can be carried out to arrive at the total damage independent of the stress path direction. However, circuits often times require devices to operate dynamically over multiple damaging and annealing regions and therefore calculating the total damage seen by a device becomes extremely challenging as the entire history of a device needs to be tracked, starting with the initial trap and H concentrations and taking into account the dynamic temperature and bias stresses. Moreover, RF stress indirectly leads to device self-heating and the accumulated effects of temperature on mixed-mode stress degradation becomes important.

Figure 3.11 illustrates the effect of changing temperatures under constant mixed-mode stress. Although the measured and simulated accumulated degradation of the two temperature sweeps follows the overall diverging and converging behavior of the bias sweeps in Figure 3.10, as expected from the differences in the hot carrier rates at the different temperatures, the different sequence of stress temperatures affects a device very differently. In ascending temperature stresses, although a device becomes damaged sooner at lower temperatures, the diffusion of H atoms away from the interface happens at a much slower rate. Thus, there is a well of H atoms that gets formed at the interface and is available for annealing traps as soon as a threshold temperature favorable for annealing is reached. This can be seen in Figure 3.11 for the measured ascending temperature sweep during the 373 K stress period (temperatures below 373 K show a gradual increase in damage whereas

at 373 K there is sudden annealing of damage). In contrast, the descending temperature sweep shows a gradual increase in damage with no signs of sudden annealing. This is expected, since at high temperature, despite an enhanced diffusion of H atoms at high temperatures, the damage creation rate is minimal and there are very few H atoms and traps left for annealing. With decreasing temperature, the device shows increasing damage due to bombardment by more and more energetic carriers.

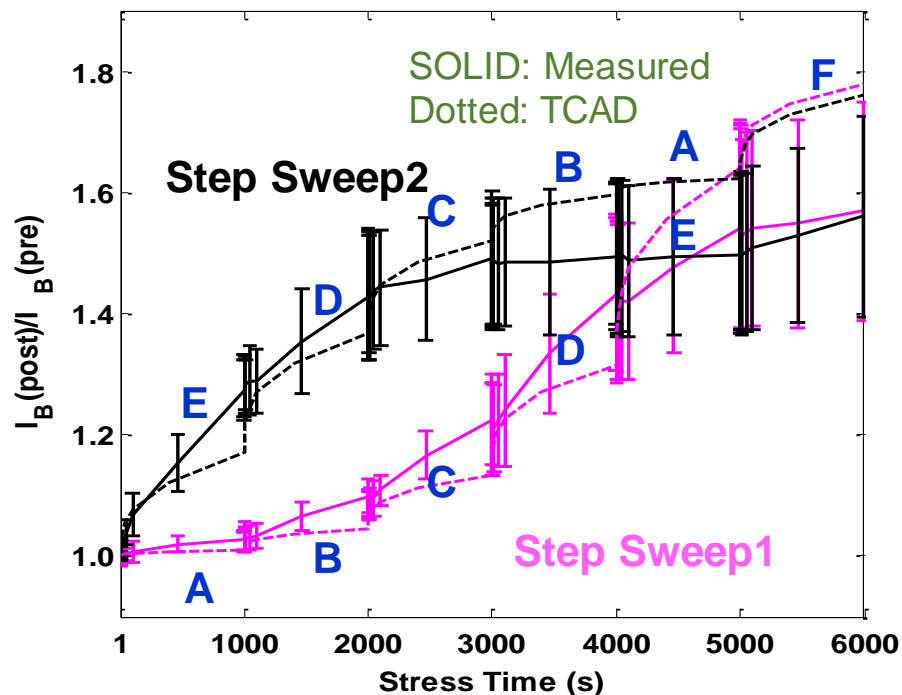


Figure 3.10: Degradation from forward-Gummel characteristics at EB spacer over the two different stress sweeps for $V_{BE} = 0.5$ V. The stress condition associated with each stress period of 1000 s has been identified with labeling convention from Figure 3.3. The solid lines show the mean value of measured data and the vertical cross-lines show the spread of the data over a sample of six devices for each stress sweep.

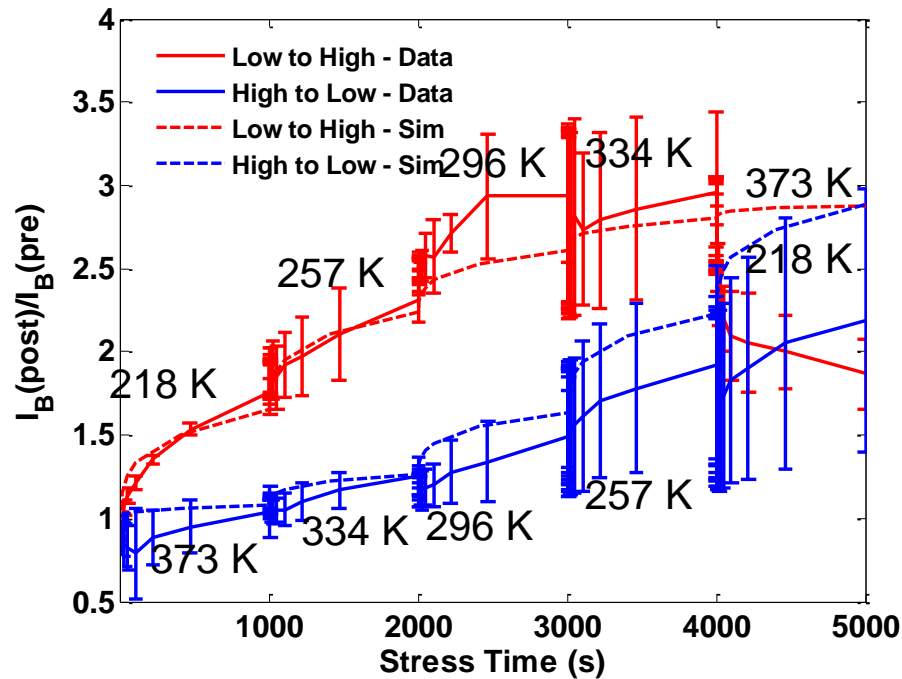


Figure 3.11: Degradation from forward-Gummel characteristics at EB spacer over two different temperature stress sweeps for a stress condition of $V_{CB} = 8.5$ V and $J_E = 0.464$ mA/ μm^2 . The temperature associated with each stress period of 1000 s is labeled. The base current degradation is extracted at $J_C = 10$ nA/ μm^2 from forward-Gummel Characteristics. The solid lines show the mean value of measured data and the vertical cross-lines show the spread of the data over a sample of 3 devices for each stress sweep.

The results from this study have serious implications for modeling the aging of devices in complex RF circuits. While examining the accumulated stress damage over dynamic electric bias alone shows a simple way to tally the damage seen by a device operating on a dynamic load line independent of the stress path direction on the output plane, taking into account the effects of temperature complicates the problem. The presence of changing temperatures in the case of self-heating introduces hysteresis into a device and must be carefully accounted for when calculating the overall damage. Although both the simulated temperature sweeps match the data reasonably well for the first four temperature steps, during the final step the ascending sweep fails to capture the annealing and the descending sweep shows too much disparity between simulation and measurement. The

difference between TCAD and measurements can be once again attributed to the limitations and assumptions in this model as mentioned in section V. The error can be reduced by calibrating self-heating, tracking the hydrogen concentrations and implementing a robust annealing model. At present, the simulations assume isothermal operation and assume a constant annealing rate for K_R . At high temperatures, self-heating would change the average lattice temperature seen by a hot carrier from its origin to its destination. Based on this new average lattice temperature, the scattering length will change according to (3.7) because of more phonon scattering. This becomes more of an issue at high temperatures as the effects of self-heating will result in more annealing and also less hot carrier damage.

3.7 Summary

In this work, the temperature dependence of mixed-mode damage was explored in detail, beginning with the calibrations to the impact ionization-model which helped understand the dynamics of the SOA boundary with respect to temperature. The temperature dependence of the lucky carrier model was further improved to include the Arrhenius T dependence for hydrogen diffusion and T^{-1} dependence of mean-free-path lengths. Then, the TCAD degradation model was calibrated at room temperature across bias levels and also over temperature for a fixed stress bias to study the accumulated stress damage across electrical bias and temperature. While TCAD simulations predict the accumulated stress degradation across electrical bias for isothermal conditions very well, when looking at the accumulated stress damage during changing temperatures, the model fails to capture hysteresis effects. Nonetheless, the model still captures the overall expected

degradation behavior across different stress bias and temperature sweeps very well. The accuracy of the simulations can definitely be improved by calibrating the self-heating effects and dynamically solving the full R-D equation given in (4) to account for damage recovery (trap annealing) by considering the local temperature, and local concentrations of traps and hydrogen. The present study uses step-wise pseudo-dynamic load lines to study the accuracy of TCAD degradation models under mixed-mode stress. However, device operation in practical circuits spans a wide range of operating conditions and is not restricted to any particular region on the output plane. Certainly, a point stress response cannot be equated with a continuously dynamic stress response. Still, DC stress degradation across bias and temperature serves as a quick check for device reliability in circuit-level operation. Once proper models accounting for all damage and annealing regions are implemented, the stress degradation from any continuous dynamic load line can be simulated. This will be a powerful and indispensable design tool for advanced circuit designs.

CHAPTER 4

MODELING OF HIGH-CURRENT DAMAGE IN SIGE HBTs

UNDER PULSED STRESS

In this work, high-current pulsed stress measurements are performed on SiGe HBTs to characterize the damage behavior, and create a comprehensive physics-based TCAD damage model for Auger-induced hot-carrier damage to oxide interfaces. The Auger hot-carrier generation is decoupled from classical mixed-mode damage and annealing on the output plane by using pulsed stress conditions to modulate the self-heating within the device under stress. The physics of high-current degradation is analyzed, and a temperature-dependent degradation model is presented. This model is the first of its kind in both the CMOS and bipolar communities and solves a significant portion of the puzzle for predictive modeling of SiGe HBT safe-operating-area (SOA) and reliability. The analysis in this work resulted in a publication [4].

4.1 Motivation

A SiGe HBT in an amplifier circuit swings dynamically over a wide range of currents and voltages on the output plane. Each electrical bias condition along the dynamic amplifier load line for the device will have different damaging or annealing effects depending on the extremes of currents and voltages involved, as illustrated in Figure 4.1. The high-voltage region above BV_{CEO} and below J_C at peak f_T is typically associated with hot-carrier damage due to impact-ionization [3]. At current densities above J_C at peak f_T , a device will undergo significant self-heating, and depending on the magnitude of this

heating, a device can experience either annealing or degradation from hot carriers due to Auger recombination and generation [61]. With scaling, the boundaries in current and voltage for each of these regions soften due to each physical mechanism acting simultaneously.

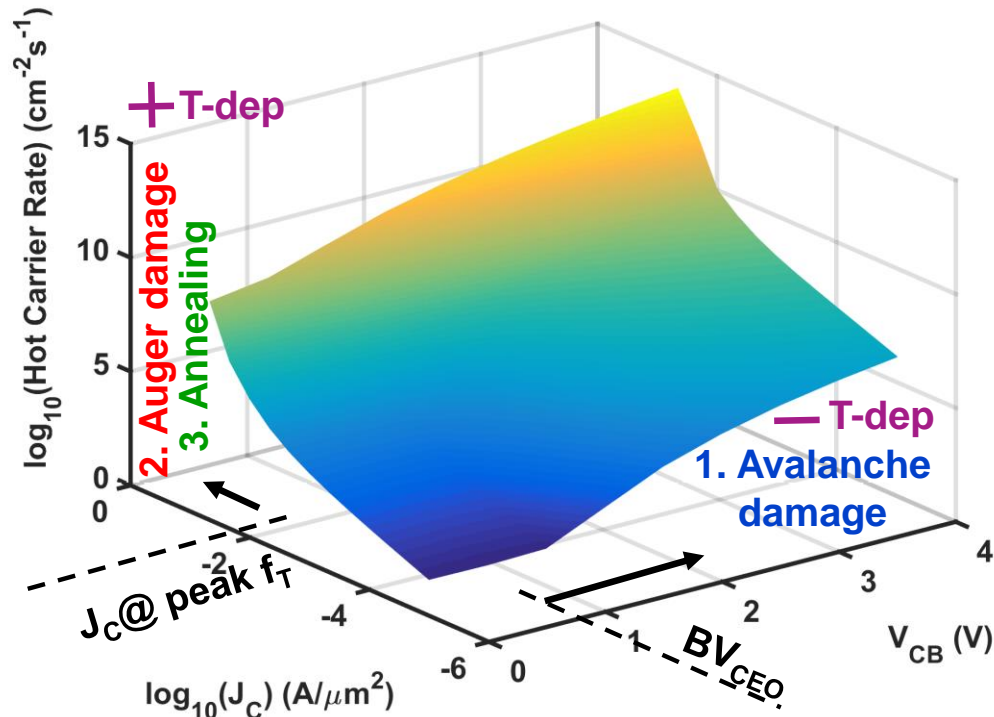


Figure 4.1: Contour map of hot-carrier production due to high-fields (Impact-ionization) and high-currents (Auger generation) at room temperature incorporating self-heating of the device.

In [3], accumulated stress degradation was modeled in TCAD across bias and temperature using a physics-based hot-carrier degradation model along with reaction-diffusion formalism to calculate trap creation at the various oxide interfaces. Although the forward reaction (trap creation) was modeled with bias and temperature dependences, the reverse reaction (annealing) was held constant based on the assumption of diffusion-limited trap creation. However, this reverse reaction is a function of electrical bias as well as the local temperature and local concentrations of hydrogen and traps at the interface.

Under dynamic electrical biasing of a device, the lattice temperature and the concentrations of hydrogen and traps will vary with time. Therefore, the annealing rate can also vary greatly. In the present work, annealing is decoupled from the high-current and mixed-mode damage mechanisms in measurement by using pulsed stresses of DC-equivalent conditions. In the process, self-heating within the device is modulated at room temperature conditions. The reliability effects relating to varying levels of self-heating are analyzed to delineate the limiting dominant damage mechanisms in the different bias regions. The physics of high-current damage is explored in depth here, expanding on the understandings offered in [61]. A new TCAD-based model, which improves upon the one developed in [3], [31] is presented here to model high-current damage. This work details the second of three significant models (high-field damage, high-current damage, annealing) necessary for enabling “push-button” reliability modeling for SiGe HBT circuits. The present work addresses the validity of these degradation models when moving from DC to AC biasing conditions and also shows how to calibrate the Auger hot-carrier rates at high current densities.

4.2 Physics of High-Current Damage

When SiGe HBTs are operated close to or beyond the peak f_T current density, the emitter-base (EB) field collapses and the neutral base and emitter are filled with carriers recombining via the Auger process. In the Auger process, an electron-hole pair recombines and donates the energy to a nearby carrier. The recipient hot carrier will roam about the low-field region until it loses kinetic energy through momentum robbing collisions. In order for the hot carrier to cause damage to oxide interfaces, it must have sufficient energy

to break Si-H bonds, and is known to be around 2.3 eV [38]. As the Auger hot carrier will have kinetic energy close to the bandgap E_g , an Auger hot carrier generated in silicon ($E_g = 1.1$ eV) should not have sufficient energy for producing damage.

If current density within the device is high enough, however, simultaneous recombination events can lead to a single carrier receiving the energy of multiple recombination events. This mechanism is illustrated in Figure 4.2. This process was first proposed in [62] for electron transitions in single atoms, but in principle, this can be extended to bulk semiconductors with bandgaps. Measurements in [63], [64] confirm this two-electron single-photon emission process in Si. Thus, as the probability for simultaneous transitions increases, the number of energetic emissions also increases. In turn, these emissions create hot carriers with sufficient energy ($E \approx 2 * E_g$) and probability to cause damage to a SiGe HBT.

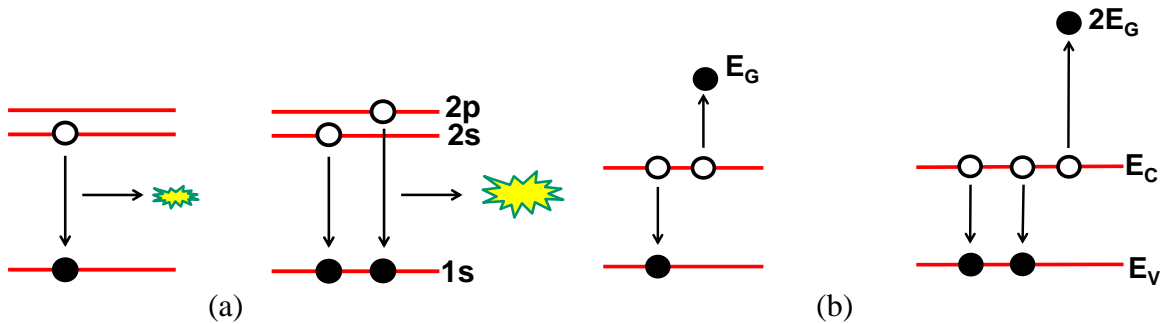


Figure 4.2: (a) One and two electron transitions followed by a photon emission in an atom. (b) One and two electron transitions in bulk semiconductors resulting in energetic excitation of carriers.

These emissions follow a Maxwell-Boltzmann distribution, which has a significant temperature dependence, and affects the temperature dependence of high-current damage of SiGe HBTs. As temperatures rise, the energy distribution gets wider, and at low temperatures, this distribution becomes a narrow peak, as evident from the

photoluminescence measurements in [65]. Assuming a phonon-assisted process, as the distribution widens, the high-energy tail increases, which results in an increase in hot carriers with sufficient energy to break Si-H bonds at oxide interfaces, as shown in Figure 4.3. This increase leads to the positive temperature coefficient for high-current stress damage seen experimentally in SiGe HBTs [61].

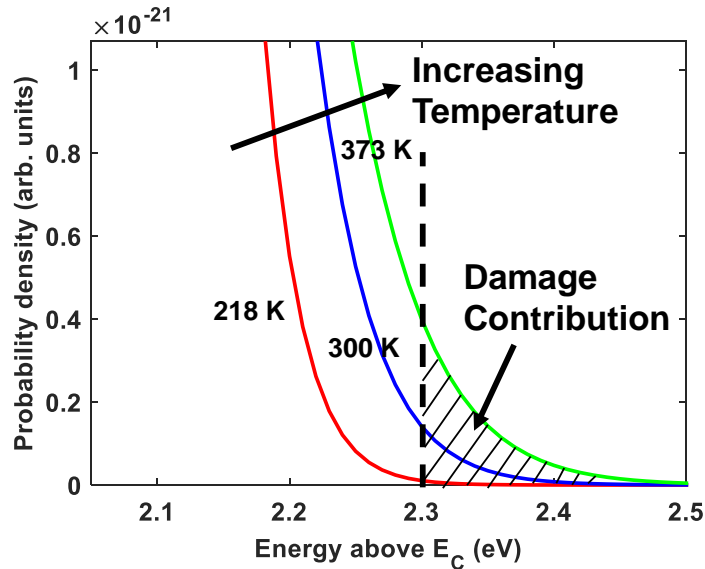


Figure 4.3: Temperature dependence of the hot-carrier energy distribution assuming a phonon-assisted process for the two electron transitions. After the device has enough thermal energy from self-heating, Auger process has enough probability of producing hot carriers that can overcome the 2.3 eV energy required for breaking Si-H bonds.

4.3 High-Current Pulsed Stress Measurements

As both annealing and high-current damage have a positive temperature dependence, identifying the conditions under which these effects dominate is crucial. One method to do this is to perform isothermal measurements of DC stress response at different ambient temperatures. This method is not ideal, however, because the thermal resistance of the device changes with temperature and the self-heating of the device cannot be easily

captured. To decouple the Auger damage from the annealing reaction, the device self-heating was modulated by pulsing the emitter current and keeping V_{CB} constant.

In the present work, all measurements were performed at room temperature on a GlobalFoundries 0.1- μm SiGe HBT platform (9HP) with a $BV_{CEO}/BV_{CBO} = 1.5/5.2$ V, $f_T/f_{Max} = 314/378$ GHz, and J_C at peak $f_T = 15$ $\text{mA}/\mu\text{m}^2$. Initially, pulsed measurements were made for a constant high-current electrical stress condition of $J_E = 20$ $\text{mA}/\mu\text{m}^2$ and $V_{CB} = 1.5$ V. Non-zero V_{CB} was used to produce sufficient heating at ambient room temperature. The pulse-widths (DC equivalent ON-time) and the duty cycle (percentage of ON-time) were each varied while keeping the other variable fixed. Figure 4.4 and Figure 4.5 illustrate the measurement results.

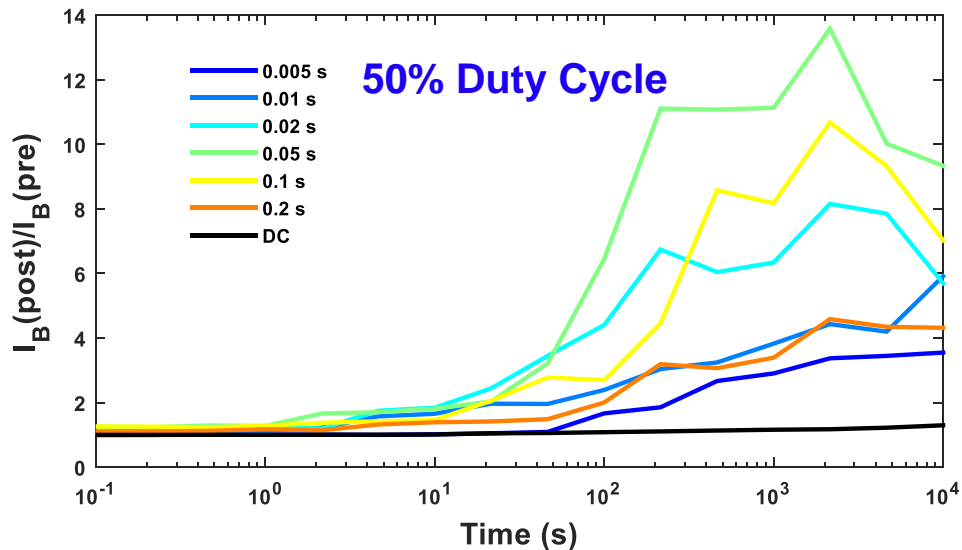


Figure 4.4: Variations in pulsed stress damage for a DC equivalent stress condition of $J_E = 20$ $\text{mA}/\mu\text{m}^2$ and $V_{CB} = 1.5$ V. I_B degradation was extracted from forward-Gummel characteristics at $J_C = 1$ $\mu\text{A}/\mu\text{m}^2$. Damage from pulse width variation compared to DC stress for a fixed 50% duty cycle.

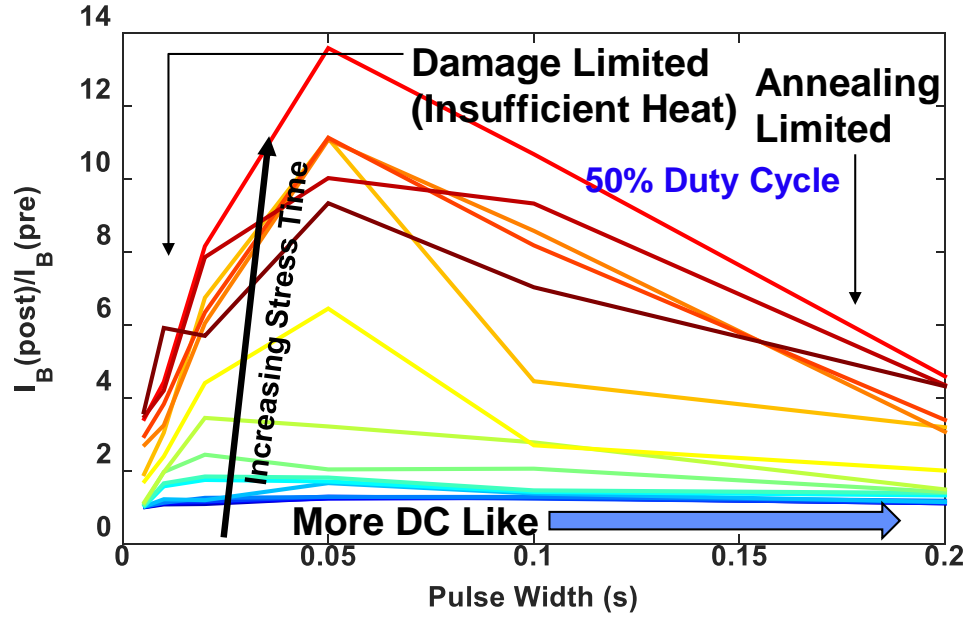


Figure 4.5: Stress damage evolution plotted against pulse width for a fixed 50% duty cycle for the conditions in Figure 4.4. The transition from dark blue to dark brown indicates increasing time from 0.1 s to 10000 s.

By varying the pulse-width, it can be seen that there is a pulse-width that maximizes damage, even exceeding the DC condition by 20x. At small pulse-widths, heating is insufficient in the device to produce significant high-current damage due to a small high-energy tail in the energy distribution. The damage at small pulse-widths is limited to the weak mixed-mode damage that might be seen at low V_{CB} bias. Considering that mixed-mode stress has a negative temperature coefficient for damage, as seen in [3], the increased damage due to increased self-heating at larger pulse widths cannot be attributed to mixed-mode degradation, and thus, the only source for the increased damage is Auger generation. As pulse widths are increased, the damage decreases due to increased annealing and approaches the DC condition. Other than seeing a damage disparity between DC and

pulsed-mode, no obvious trends were observed when varying the duty cycle while keeping the pulse width constant.

Noting the pulsed condition maximizing the Auger damage, more pulsed measurements were done to see if aggressive damage could be observed even after eliminating mixed-mode damage completely. The results in Figure 4.6 and Figure 4.7 show that stress damage indeed exists under both DC and pulsed-mode even after setting V_{CB} to 0 V. Similar to the results in Figure 4.4, pulsed-mode shows more damage compared to DC. In addition, increasing the stress current produces more damage due to an increase in the Auger generated hot carriers.

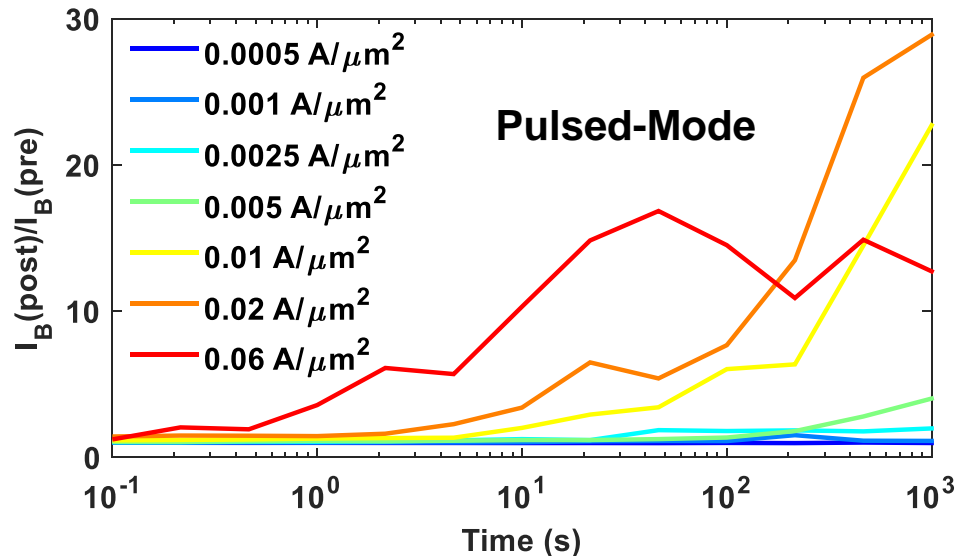


Figure 4.6: High-current stress degradation under pulsed-mode for $V_{CB} = 0$ V. I_B degradation extracted from forward-Gummel characteristics at $J_C = 0.1 \mu\text{A}/\mu\text{m}^2$. Pulsed-mode stress degradation with 50 ms width and 50% duty cycle.

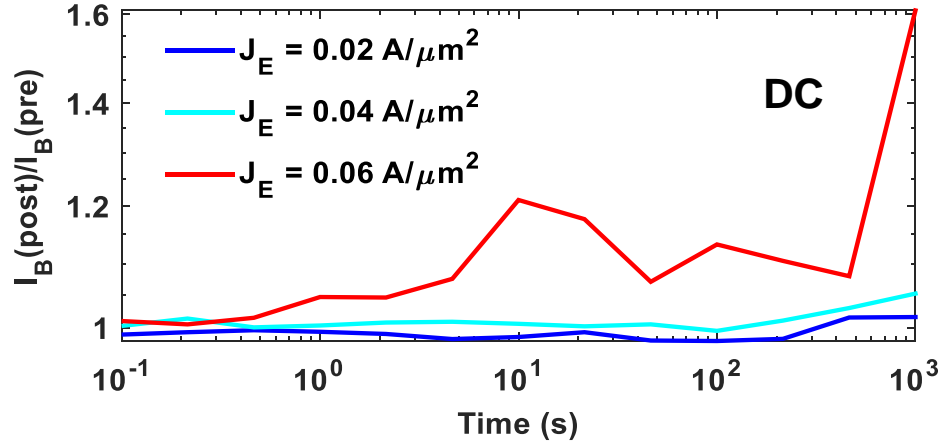


Figure 4.7: High-current stress degradation under DC for $V_{CB} = 0 \text{ V}$. I_B degradation extracted from forward-Gummel characteristics at $J_C = 0.1 \mu\text{A}/\mu\text{m}^2$.

These results prove that stressing devices at a DC condition has a combination of damaging and annealing reactions. Models that are purely based on DC measurements alone cannot be scaled for calculating the accumulated damage under RF conditions, as they do not capture the various degrees of damage and annealing present due to self-heating for a given electrical stress condition at a particular temperature. Using a condition limited by annealing would underestimate the calibration of hot carriers generated through the Auger process. Additionally, the measurements done in this study had a sample size of one in order to obtain the overall trend in damage for various heating conditions. More samples would certainly reduce the noise seen in the measurements and give a clearer trend for calibration.

4.4 Modeling High-Current Auger Damage

The first step in modeling high-current damage is to calibrate self-heating. In TCAD simulations, this process is done by setting the appropriate thermal boundary conditions to produce necessary self-heating within the device. These boundary conditions are calibrated by adjusting the contact thermal conductivity of each device terminal to match the measured V_{BE} roll-off at high currents. The calibration of TCAD to data is shown in Figure 4.8. The differences between measurement and the 2D TCAD deck can be attributed to the assumption of heat traveling only through the contacts as opposed to the entire top. Nonetheless, the self-heating can now be simulated at a very basic level for estimating the heating within the device, and thereby used for validating our Auger hot carrier damage model. The lucky electron model from [3], [31] is modified to account both classical hot carriers resultant from high electric fields and Auger generated hot carriers. Table 4.1 shows a comparison of the equations and quantities that changed in the model from [31] to account for high-current Auger damage. The hot-carrier probability given by (4.1) (obtained from [63]), the hot-carrier driving force (Auger generation rate, R_{Auger}), and the hot-carrier impingement rate at the oxide interfaces given by (4.2) are different from the corresponding components for high-field hot carriers.

$$P_{hot,e/h} = A(E - 2E_g)^{7/2} e^{-(E-2E_g)/kT} \quad (4.1)$$

$$r_{e/h}(x, y) = R_{Auger}(x, y) P_{1\frac{e}{h}}(x, y) P_{dist}(x, y) V(x, y) \quad (4.2)$$

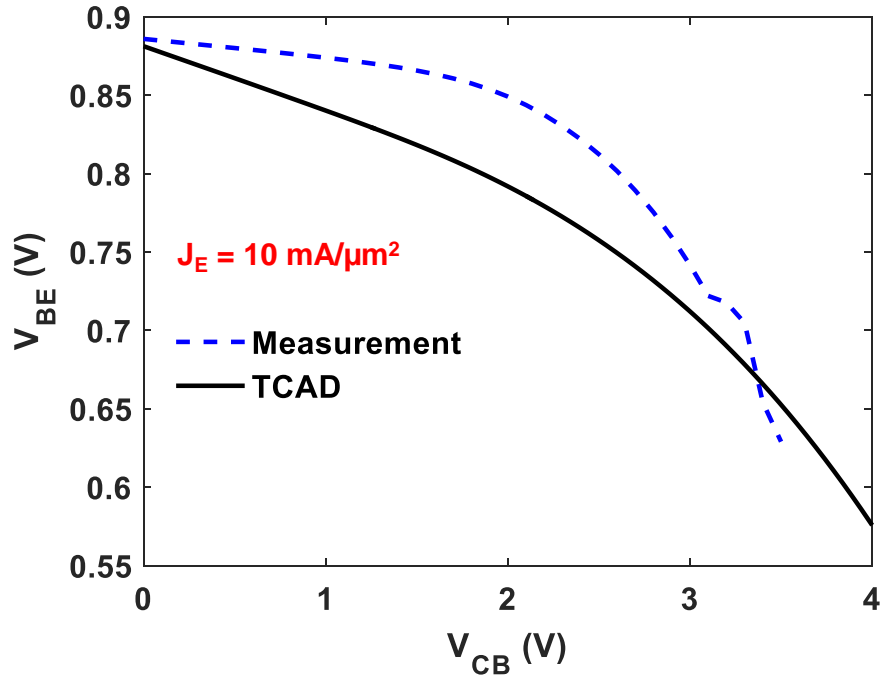


Figure 4.8: Comparison of the calibration of V_{BE} roll-off in TCAD and measurements to account for self-heating.

In (4.1), A is a unit-less fitting parameter, E_g is the bandgap of silicon, and the equation computes the probability that a carrier gains an energy E for causing damage. This equation takes into account the T-dependence of the Auger energy distribution. In (4.2), $V(x, y)$ represents the equivalent 3-D volume of a vertex. $P_{1,e/h}(x, y)$ and $P_{dist}(x, y)$ are the hot-carrier redirection and distance probabilities, respectively, and they do not change form in the adapted model for Auger damage [31].

Table 4.1: Comparison of equations used in the lucky electron model for generating high-field and high-current hot carriers. After [31].

High-Field (Impact-Ionization) Damage	High-Current (Auger) Damage
--	--------------------------------

$P_{hot,e/h}(\boldsymbol{\varepsilon}, \mathbf{x}, \mathbf{y})$	$\frac{1}{\lambda F_{eff}(\mathbf{x}, \mathbf{y})} e^{\boldsymbol{\varepsilon}/\lambda F_{eff}(\mathbf{x}, \mathbf{y})} d\boldsymbol{\varepsilon}$	$A(E - 2E_g)^{7/2}$ * $e^{-(E-2E_g)/kT}$
$P_{red}(\boldsymbol{\varepsilon})$	$\frac{1}{2\lambda_r} \left(1 - \sqrt{\frac{\phi_{hot}}{\boldsymbol{\varepsilon}}} \right)$	
$P_{dist}(\mathbf{x}, \mathbf{y})$	$e^{-d/\lambda}$	
$P_{1,e/h}(\mathbf{x}, \mathbf{y})$	$\int_{\phi_{hot}}^{\infty} P_{hot,e/h}(\boldsymbol{\varepsilon}, \mathbf{x}, \mathbf{y}) P_{red}(\boldsymbol{\varepsilon})$	
Source of carriers	Current Density(A/cm ²)	Auger Generation (cm ⁻³)
$r_{e/h}(\mathbf{x}, \mathbf{y})$	$\frac{\ \vec{J}_{n,p}(\mathbf{x}, \mathbf{y})\ }{q} P_{1,\frac{e}{h}}(\mathbf{x}, \mathbf{y}) P_{dist}(\mathbf{x}, \mathbf{y})$ * <i>Area</i>	$R_{Auger}(\mathbf{x}, \mathbf{y})$ * $P_{1,e/h}(\mathbf{x}, \mathbf{y}) P_{dist}(\mathbf{x}, \mathbf{y})$ * <i>Volume</i>

As degradation at high current bias involves both Auger damage and annealing, modeling this region will not be complete without the inclusion of the annealing reaction. However, the validity of the model in the regions that do not involve severe self-heating can still be checked. As a preliminary proof of concept for the high-current model, Figure 4.9 shows the calibration of TCAD damage to the maximum available damage (a pulsed condition that produced the greatest damage) from high-current stress for the electrical condition studied at room temperature. This was achieved by tuning the free parameter A to 1000. This calibration now captures the maximum amount of Auger hot carriers that can be generated from a particular electrical bias and temperature condition and is not limited by annealing. It should be noted that this damage calibration is valid only under pulsed conditions. Although the Auger hot carrier rate may be correct, in order to model DC damage, the positive temperature dependence of annealing needs to be modeled. This addition is an area of future work.

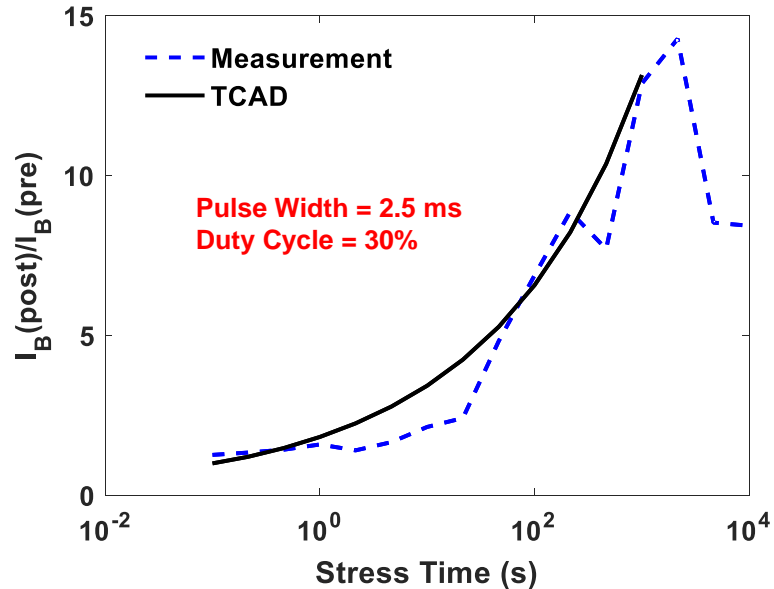


Figure 4.9: Calibration of TCAD to a measured pulsed condition with a pulse width of 2.5 ms and a duty cycle of 30%. I_B degradation was extracted from forward-Gummel characteristics at $J_C = 1 \mu\text{A}/\mu\text{m}^2$.

4.5 Summary

This work presented the background physics and model for simulating hot-carrier damage due to Auger generation at high current densities. Equations from the lucky electron model were adapted to simultaneously solve hot-carrier damage contributions from impact-ionization and Auger generation.

By performing pulsed stress measurements, this work showed the co-existence of annealing and damaging reactions when a device is operated at high current. This implies that DC stress measurements that have previously been used for calibrating mixed-mode stress damage cannot be used for isolating and calibrating the high-current damage mechanism, as the self-heating driven annealing mechanism needs to be decoupled. Although the accumulated damage from mixed-mode stress can be calculated by

integrating over different points on the output plane as demonstrated in [1], doing the same for high-current stress is challenging due to changes in self-heating. Both Auger-generated hot carriers and hydrogen diffusion within oxides need to be modeled from the beginning to account for any hysteresis effects.

While it can be argued that variations in high-current damage occur only for small frequencies (20-100 Hz), due to the time constants associated with transient self-heating, the frequency dependence of damage in response to changes in other electrical biases and temperatures remains to be tested. Direct relevance of these results may be limited to applications such as low-frequency power electronics, particularly those that use high-breakdown silicon-on-insulator (SOI) platforms predisposed to more self-heating. Nevertheless, this work outlines the proper sequence for isolating and calibrating Auger damage and represents an important step towards full predictive reliability modeling in SiGe HBTs. The bias and temperature dependence of high-current damage as it pertains to both oxide interface damage and polysilicon degradation will be explored more in Chapters 6 and 7.

CHAPTER 5

PHYSICAL DIFFERENCES IN HOT CARRIER DEGRADATION OF OXIDE INTERFACES IN COMPLEMENTARY (NPN+PNP) SiGe HBTS

This work examines the fundamental reliability differences between NPN and PNP SiGe HBTs. The device profile, hot carrier transport, and oxide interface differences between the two device types are explored in detail as they relate to device reliability. After careful analysis under identical electrical stress conditions for NPN and PNP, the differences in activation energies for the damage of the oxide interfaces of the two devices is determined to be the primary cause for accelerated degradation seen in PNP SiGe HBTs. An analytical model has been adapted for simulating these aging differences between PNP and NPN devices. This work resulted in a publication [5] and has significant implications for predicting the degradation of complementary SiGe HBTs and even engineering future generations with well-matched NPN and PNP device-level reliability.

5.1 Motivation

Having access to both NPN and PNP variants of SiGe HBTs in any SiGe technology platform is a very desirable option, as it empowers circuit designers to build complementary circuits (RF, analog and high-speed digital) with simplicity and versatility. The symmetry provided by complementary devices enables a large variety of interesting circuits; however, well-matched complementary devices are difficult to manufacture due to the fundamental differences between NPN and PNP SiGe devices. Imbalances in device

performance lead to imbalances in the AC (gain, speed, noise and linearity) and DC (quiescent output current and voltage levels) performance of such circuits, which are highly undesirable.

In highly scaled technologies, the effects of hot carrier degradation have become a serious reliability concern. The NPN and PNP devices not only can be damaged, but they also can be damaged unevenly (i.e., one more than another) and thereby lose the desirable initial symmetry that the technology began with. This makes the design of reliable high-performance complementary circuits challenging, as the degradation response of a circuit over its expected EOL needs to be kept in mind at the time of design. The investigation presented in [34] examined the aging of complementary SiGe HBTs, and concluded that a bias dependent mismatch in the degradation of complementary devices exists. For both aggressive and equal mixed-mode and reverse-EB stress conditions, PNP SiGe HBTs showed accelerated degradation compared to their NPN counterparts. Previous literature offers very little conclusive and experimental evidence to explain this behavior.

In order to clarify the inherent aging differences observed in complementary SiGe HBTs, this work examines the device level differences using measured stress data and TCAD simulations on a first-generation complementary SiGe HBT platform. The specification of the complementary technology is given in Table 5.1, and the DC calibration to the measured data for the matched TCAD model is given in Figure 5.1. The device profile, hot-carrier transport, and interface-level dependencies contributing to hot carrier damage in these devices will be studied with the help of a lucky-electron-based model built for SiGe HBTs, as demonstrated in [3], [31]. Differences in bias dependence for impact-ionization between the two devices will first be examined, and then the

significant degradation model parameters in [31] will be identified and modified to account for oxide interface damage in the two HBT types.

Table 5.1: Technology specifications of the NPN and PNP devices in this work.

	PNP	NPN
BV_{CEO} / BV_{CBO}	3 V / 10 V	3 V / 13 V
f_T / f_{max}	56.4 GHz / 66.3 GHz	60.5 GHz / 73.4 GHz

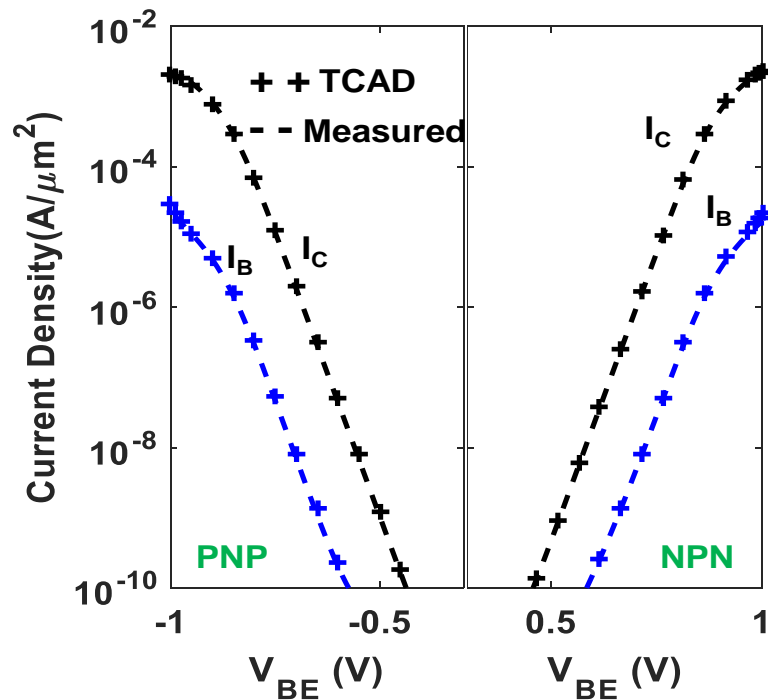


Figure 5.1: Calibrated forward-Gummel characteristics of the PNP and NPN devices in this work. All devices used have $A_E = 0.3 \mu\text{m} \times 6.4 \mu\text{m} \times 2$.

In [3], [31] the primary device for study has only been the NPN variant. Although the lucky electron model is applicable to both devices, obtaining a unifying model that can accurately capture the degradation behavior of both devices using a common set of parameters is certainly challenging. The present work highlights the significant parameters for simultaneously modeling NPN and PNP aging.

5.2 Mixed-Mode Damage Mechanism in NPN and PNP SiGe HBTs

Mixed-mode biasing conditions during circuit operation lead to an avalanche generation of hot carriers in the CB junction. The amount of carriers generated directly determines the amount of damage suffered by a given device. Figure 5.2 compares M-1, which measures the relative level of impact-ionization between the matched NPN and PNP devices. The matched PNP SiGe HBT has more impact ionization than the NPN at high V_{CB} due to the way it is engineered. For a fixed integrated Ge content, the minority hole mobility in a PNP device is lower when compared to the minority electron mobility in an NPN device. As a result, the PNP often needs to be engineered with a higher Ge content. This in turn creates a significant heterojunction barrier at the CB metallurgical junction in a PNP device that needs to be suppressed with higher collector doping. This in turn leads to more impact-ionization in PNP at high V_{CB} due to increased fields, as shown in Figure 5.3, which makes the PNP more prone to hot carrier damage.

Apart from the differences in the hot carrier generation rates in the two device types, the transport of carriers to different oxide interfaces is dependent on the carrier type. The opposite polarities of electric fields in the two devices selectively facilitate the transport of different hot carriers generated in the CB junction following impact-ionization. When considering the hot carrier damage to the EB spacer oxide in the NPN, secondary hot holes are the dominant carriers expected to cause damage, as demonstrated in [66]. In contrast, for the PNP, the hot electrons are the carriers favored by the local electric fields to cause

damage to EB spacer [33]. This difference in the favored damaging carrier type is illustrated in Figure 5.4, and adds to the complexity of the damage response.

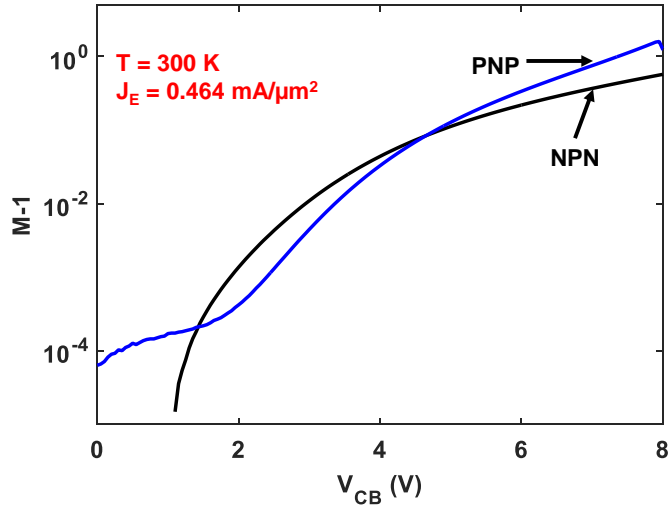


Figure 5.2: Relative level of impact ionization seen in the PNP and NPN SiGe HBTs for $J_E = 464 \mu\text{A}/\mu\text{m}^2$ at 300 K. Level of bias determines which device sees more impact ionization.

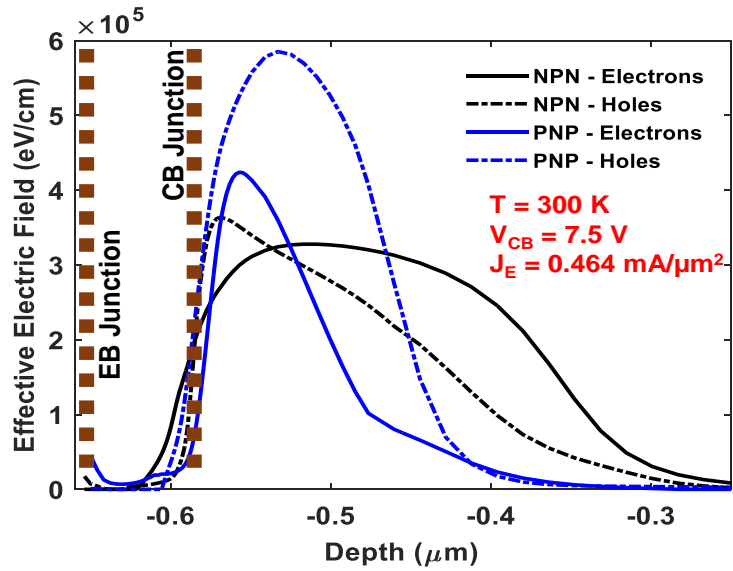


Figure 5.3: Relative effective field strength in NPN and PNP SiGe HBTs at the CB junction for $J_E = 464 \mu\text{A}/\mu\text{m}^2$ and $V_{CB} = 7.5 \text{ V}$ at 300 K. The peak field is larger in the PNP.

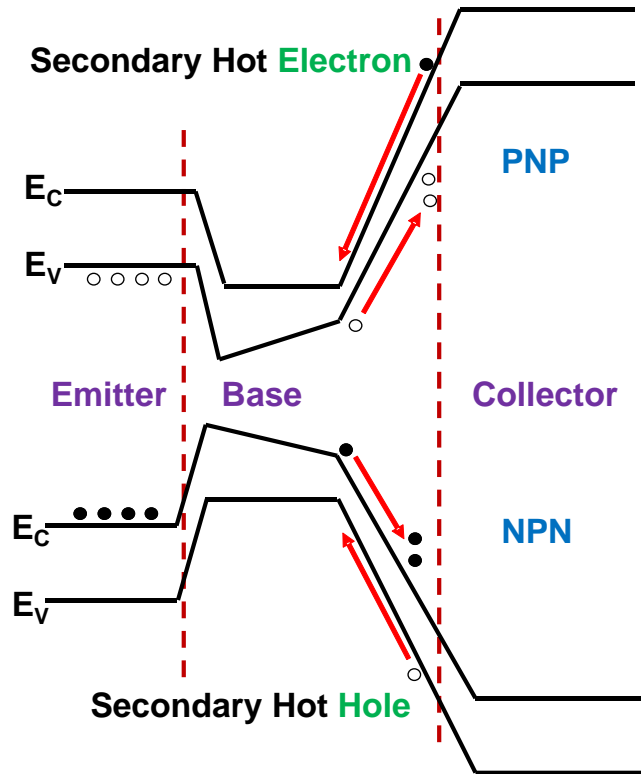


Figure 5.4: Respective secondary hot carriers responsible for damage at the EB interface for an NPN and PNP SiGe HBT under mixed-mode stress.

5.3 Damage due to Polarity of Hot Carriers

Based on the lucky carrier model used to calculate the hot carrier degradation in SiGe HBTs [31], the success of hot carriers reaching the oxide interfaces is dependent on hot carrier generation with sufficient energy, redirection of hot carriers to the oxide interface, and subsequent transport of the hot carrier to the interface without collisions. Equations (3.1)- (3.3) model these requirements as different probabilities. The overall probability of a hot carrier reaching an oxide interface point (x, y) gets enhanced if the scattering length is greater and when the transport distance (d) of a hot carrier is minimal. The study in [67] gives scattering length of electrons to be greater than that of holes, by a factor of 1.63x in Si. This naturally causes more hot electrons to reach the EB oxide interface in PNP SiGe HBTs and undergo more severe hot carrier damage.

Figure 5.5 shows the simulated hot carrier rates along the EB oxide interface for both NPN and PNP devices undergoing an equivalent mixed-mode stress of 7.5 V. As expected, not only does the PNP have a greater rate of hot carrier impingement at the EB interface, but both devices show the correct dominant hot carrier at the EB window; that is, holes for NPN and electrons for PNP. This was achieved for a λ_h/λ_e ratio of 0.9 in the lucky carrier model. In addition to the transport physics of each carrier, even the interaction by a hot carrier with interfaces having a varying ϕ_{hot} can lead to differences in damage, as will be visited in the next section.

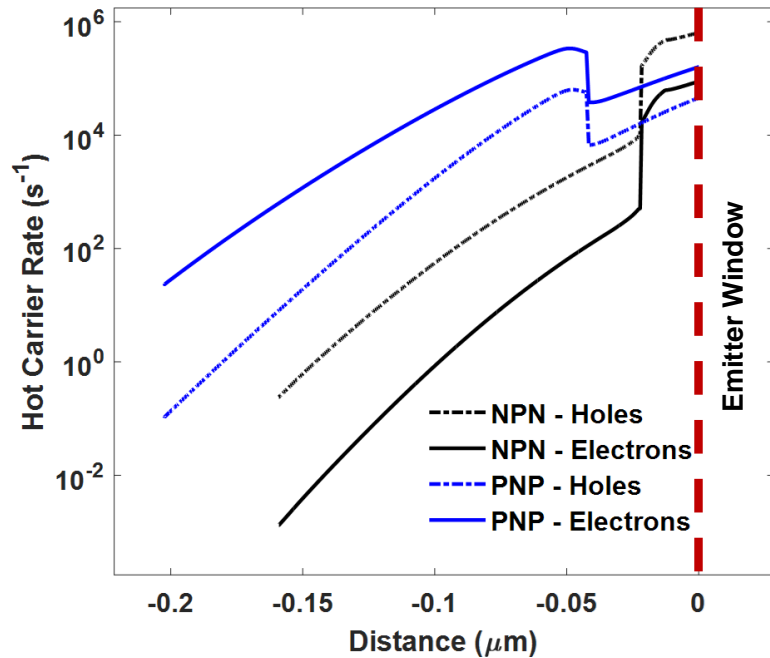


Figure 5.5: Hot carrier impingement along the EB oxide interface in NPN and PNP SiGe HBTs for a stress condition of $V_{CB} = 8.5$ V and $J_E = 400 \mu\text{A}/\mu\text{m}^2$ at 300 K.

5.4 Interface Dependence of Damage

The actual damage creation process in a SiGe HBT happens as a hot carrier knocks off hydrogen atoms that passivate dangling bonds at the oxide-silicon interface, resulting in traps that cause base current degradation. The lucky carrier model uses the reaction-diffusion formalism to calculate the interface trap generation over time as given by (3.5) – an approximation that assumes a forward reaction dominated stress condition [3], [31]. Both the forward (K_F) and reverse (K_R) reaction rates are important to the overall generation of traps, which happens as hydrogen (H_2) diffuses away from the interface. The forward reaction of hydrogen being liberated from a Si-H bond due to an impingement by a hot carrier is given by (5.1).



The energy required for breaking this bond changes depending on the charge type of the traps involved. This charge dependence of the activation energy has been modeled using molecular orbital theory in [39]. That work reports that negatively charged traps associated with the Si-H bond can be created with an activation energy of 1.62 eV and that positively charged traps can be created with an activation energy of 2.70 eV. The energy required to create a trap has also been determined experimentally to be 2.3 eV for MOSFETs (using p-type wafers) [38]. The measured energy for trap creation in p-type wafers matches well with the simulated 2.7 eV for Si-H bonds having positively charged traps. Positively charged traps can be thought of as positive free charge from a p-type silicon interacting with the Si-H bond at the oxide interface and thereby influencing the activation energy for trap creation. Although there is a measured value for the activation energy for damage creation in p-type wafers there has been no other experiment performed

using n-type wafers to confirm the lower simulated activation energy for negatively charged traps. Still, this difference can be a major factor for producing device-level differences in reliability, and the following sections will demonstrate the necessity for this disparity in activation energies. For simulating and comparing the device degradation mechanisms seen between NPN and PNP SiGe HBTs, the values used for the activation energies for damage for positive trap and negative traps were 2.3 eV and 1.6 eV, respectively.

Although the present work assumes a constant K_R for simplicity, in order to correctly simulate the reverse (annealing) reaction, the activation energy for (5.2) must also be modeled well. The simulations in [39] indicate that the reverse reaction rate is also dependent on the local charge of the trap. This has also been confirmed experimentally for a range of traps spanning the bandgap of Si. The negative charges increase the activation energy required to anneal the traps and positive charges decrease the activation energy [68]. The qualitative effect of the local charge on both of these reactions is shown in Figure 5.6.



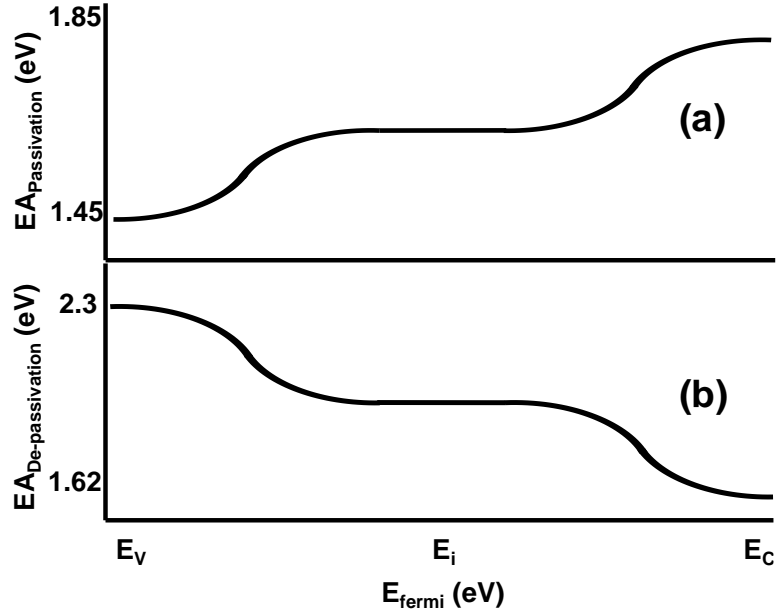


Figure 5.6: Qualitative functions for the passivation and de-passivation activation energies required as a function of the local E_{fermi} of the trap to alter the Si-H bond. The actual shape of these functions is dependent on interface orientation and quality. (a) Qualitatively derived from [68]. (b) Follows the values reported in [39] and the assumptions in [38].

In essence, negative charges not only make it easier to break the Si-H bond by reducing the activation energy to create traps, but they also increase the activation energy for annealing the traps through the reverse reaction process. The opposite holds for positively charged traps: Si-H bonds are much harder to break and are also very easy to form due to the increased and lowered activation energies for the forward and reverse reactions, respectively. The equilibrium relation (K_F/K_R) between the forward and reverse reaction rates is given by the following equation [69]:

$$K_{eq} = \exp(E_{\text{diss}}/kT) . \quad (5.3)$$

Here, E_{diss} is the difference between the activation energies for the forward and reverse reactions given by (5-6). As evident from Figure 5.6, the difference becomes greater for trap levels close to the valence band (-0.85 eV) and smaller for trap levels close to the conduction band (0.23 eV). This difference determines the relative ease with which traps can form along an interface. For traps situated close to the valence band, this leads to a miniscule equilibrium ratio and therefore a small effective trap formation rate and more robust reliability. The overall shape seen in Figure 5.6 follows the distribution of the paramagnetic bond (P_b) centers at the interface [68]. The distribution of P_b centers changes between different crystal planes [68], [70]. The exact values of activation energies around mid-bandgap are not as important as the values near E_C and E_V because population inversion of carriers along the EB interface happens very abruptly. The resulting local Fermi levels force the activation energies for hot carrier damage to also transition abruptly along the EB interface as seen in Figure 5.7. For CB junctions with high breakdown, the transition is expected to be more gradual due to a lightly doped collector.

This inherent difference between the effects of positive and negative traps on the oxide interface damage substantially alters the energy requirements for a hot carrier and makes the negatively charged trap regions (which can be thought of as an N-doped semiconductor adjacent to the oxide interface) more vulnerable for reliability issues. A PNP device has much of the space charge region (SCR) at the EB interface consisting of the N-type doping, making it more vulnerable to hot carrier damage, whereas for an NPN, much of the SCR is p-type, which is very robust from a reliability perspective. The activation energy dependence on the local Fermi level was incorporated into the degradation model and the resulting hot carrier rate difference between NPN and PNP can

be seen in Figure 5.7. In contrast to the NPN, the PNP develops two peaks of hot carriers, the first one due to the proximity to the emitter window, and the second one due to a lowered activation energy for damage in the base. As a result of the second peak, the PNP has significantly more trap formation and recombination occurring in the base region of the interface than the NPN does.

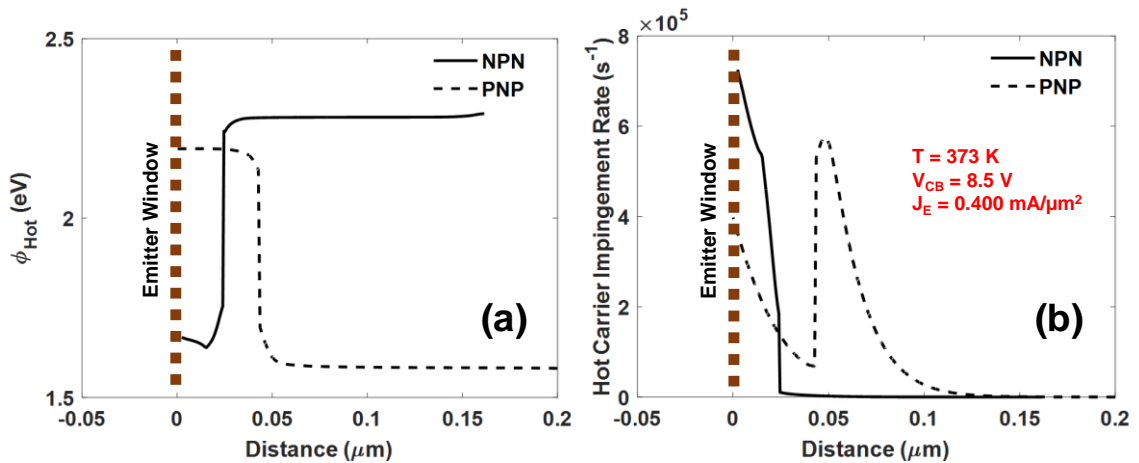


Figure 5.7: Simulated (a) activation energies and (b) hot carrier rates along the EB interface for NPN and PNP devices for a stress condition of $V_{CB} = 8.5 \text{ V}$ and $J_E = 0.400 \text{ mA}/\mu\text{m}^2$ at 373 K . The sharp transitions of activation energies and hot carrier rates along the interface indicate the carrier population inversion.

Thus, for matched complementary SiGe HBTs, not only does a PNP possess inherent vulnerabilities for reliability due to increased impact ionization and increased hot carrier scattering lengths, but also due to lowered activation energies for damage in the oxide interface. During mixed-mode stress, these properties make the PNP very sensitive to increasing electric fields and cause significant interface damage for bias conditions much less than the levels required for producing comparable damage in an NPN. Following the calibrations to impact-ionization in NPN and PNP, the free parameters to tune for predicting damage in both devices using the lucky carrier model are the scattering lengths

for the different carriers and the activation energies for the different reactions. The issues of calibrating the two parameters will be analyzed in the following sections.

5.5 Hot Carrier Damage Sources and Significance of Model Parameter

Classical hot carrier damage has always been attributed to the acceleration of carriers due to high electric fields. This high field driven hot carrier source is responsible for causing damage under mixed-mode stress and reverse EB stress. However, there is also a less studied hot carrier source that is also equally prominent in SiGe HBTs when a device is operated at very high current densities (greater than J_C at peak f_T) with very little local field presence. Such bias conditions result in the Auger recombination of carriers. In turn, these events lead to the production of Auger generated hot carriers that can also damage at the oxide interfaces, in a manner similar to how hot carriers from mixed-mode stress damage the oxide interfaces [61]. Given these two independent physical damage mechanisms, it is important to identify which of the above-mentioned degradation parameter (λ, ϕ_{hot}) differences between NPN and PNP devices contributes most significantly to the observed aging differences.

Figure 5.8, Figure 5.9 and Figure 5.10 show the measured aging differences between NPN and PNP SiGe HBTs under mixed-mode, reverse EB and low-voltage, high-current (Auger) stress conditions. In all of these conditions, regardless of the presence of large electric fields, the PNP device degrades sooner than the NPN counterpart does. This suggests that the origin of the hot carrier, whether it be somewhere in the EB (reverse EB stress) or CB (mixed-mode) junctions or the neutral base (high-current stress), does not have much importance. As [61] points out, Auger recombination and impact-ionization due

to reverse EB generation are opposite effects (low-field vs. high-field triggered). The fact that a PNP device has more damage under both conditions shows that there must be some other factor influencing its damage in addition to the hot carrier generation from Auger recombination and impact-ionization.

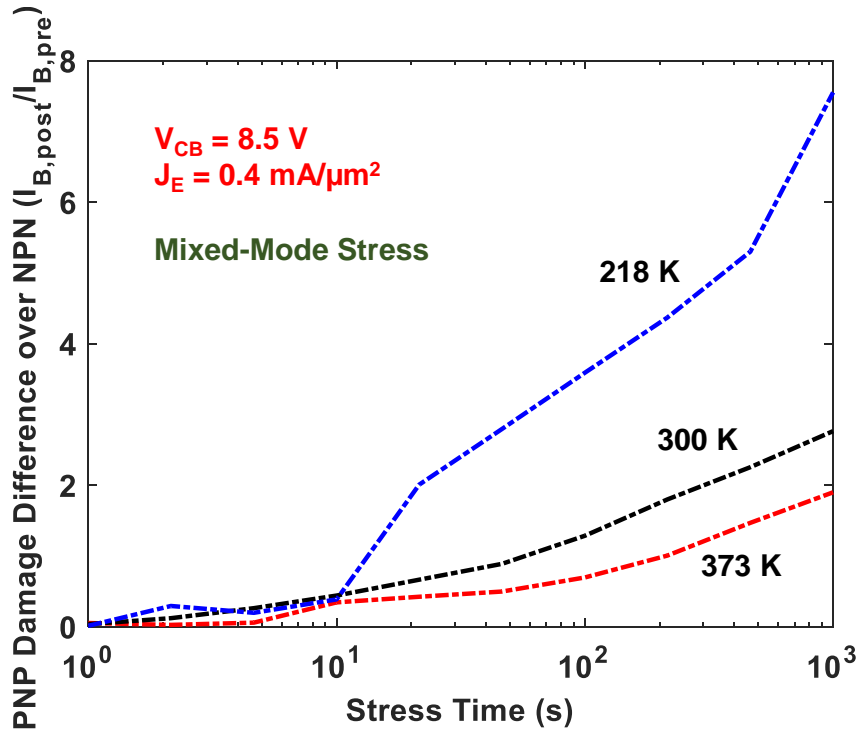


Figure 5.8: Difference in measured mixed-mode damage between NPN and PNP across temperature for a stress condition of $V_{CB} = 8.5 \text{ V}$ and $J_E = 0.400 \text{ mA}/\mu\text{m}^2$. Each temperature curve is averaged over 4 devices of NPN and 4 devices of PNP.

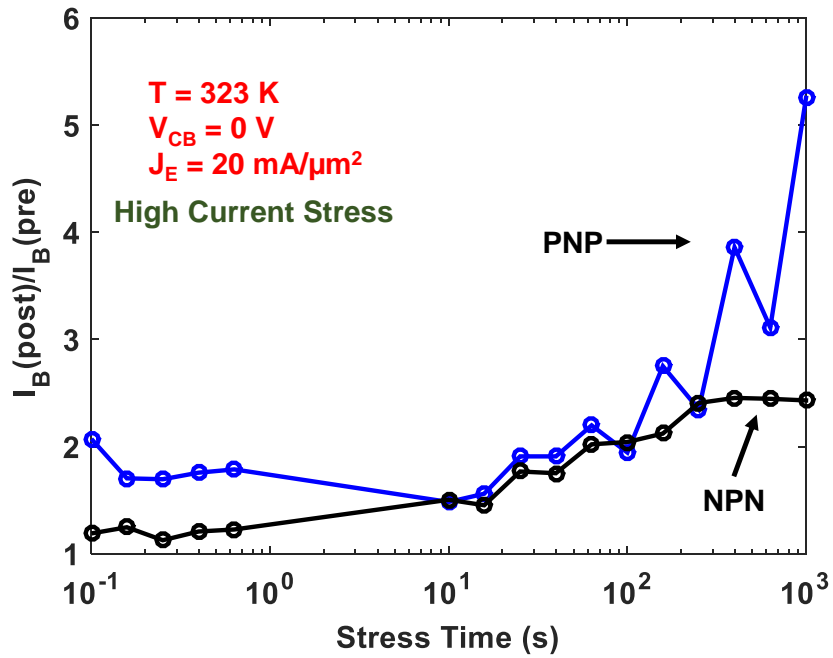


Figure 5.9: Damage due to high-current stress at 323 K for $V_{CB} = 0 \text{ V}$ and $J_E = 20 \text{ mA}/\mu\text{m}^2$.

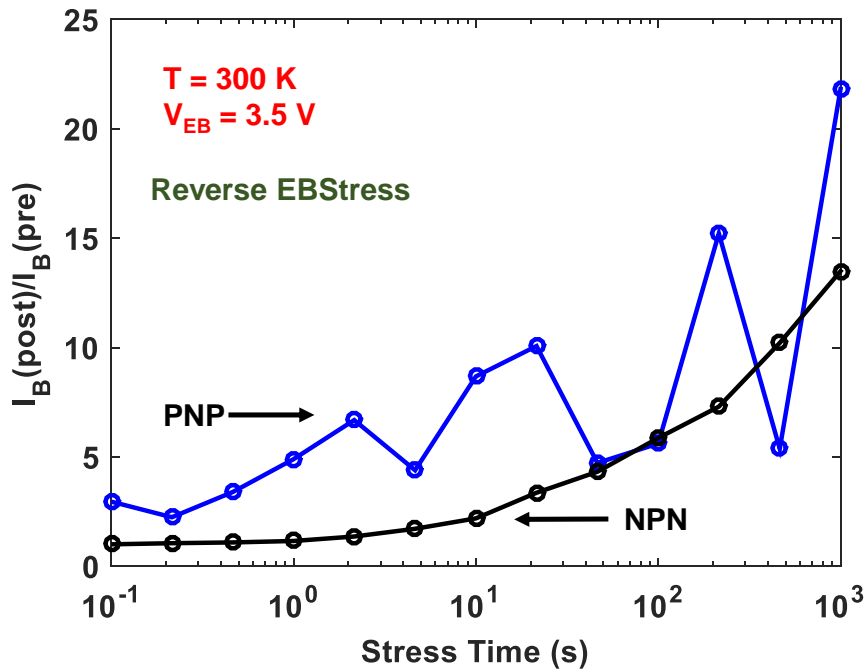


Figure 5.10: Damage due to reverse EB stress condition of 3.5V at 300 K. All damages were extracted from forward-Gummel characteristics at $J_C = 10 \text{ nA}/\mu\text{m}^2$.

After the carrier generation, the transport of the hot carrier becomes important. As mentioned earlier, the scattering length is the limiting parameter for the number of energetic carriers reaching the oxide interface. As the distance between the source and the oxide interface increases, the transport losses become very significant. In the case of high-current stress, transport loss differences between electrons and holes are not that significant since the source (neutral base) and sink (EB interface) are situated very close to each other (within 2-3 multiples of the scattering length) for the devices being studied. Assuming an equal number of hot electrons and hot holes are generated during Auger recombination in the neutral base, after transport losses, the number of electrons and holes reaching the oxide should roughly be the same order of magnitude. So, the fact that high-current stress also shows accelerated PNP degradation means that hot carrier activation energy for trap production at the oxide interface is the only significant physical parameter left for causing the PNPs to age sooner.

Lastly, it is important to note that the PNP device needs to have significantly more integrated germanium than the NPN variant to achieve comparable DC and AC performance. Scattering lengths of carriers in Ge, when compared to those of Si, are enhanced slightly (5%), similar to the enhancement of mobility [67]. Although it can be argued that under mixed-mode stress the PNP device exhibits increased damage due to electrons with enhanced scattering lengths (allows higher retention of carrier energy), it is still not enough to account for the observed damage disparity between the two devices. If a hot carrier activation energy identical to that of NPN (2.3 eV) is used in the PNP, the scattering length needs to be increased to unphysically large values (over 8 nm) to produce

equivalent damage at room temperature, and this nullifies the calibration at other temperatures as well.

5.6 Discussion of Results and Calibrations

In the sections above, the PNP SiGe HBT was argued to have worse reliability compared to the NPN SiGe HBT due to its larger N region for the SCR at the EB interface. However, the EB junction consists of both N and P-type regions and is not unipolar. Therefore, one side of the junction undergoes accelerated damage, whether it be in the NPN or the PNP. In the case of the NPN, the N region does get damaged sooner. However, the N portion of the SCR in an NPN is very small in comparison to the P region. In addition, once damaged, this N region requires greater thermal energy to be annealed when compared with the P region. Thus, the degradation in the NPN becomes limited by the damage to the P region (which is diffusion limited). Therefore, the NPN device sees a more gradual increase in damage over time even when operated at high currents and high temperatures, as seen in Figure 5.9.

In comparison, the PNP SiGe HBT is filled with regions of annealing and damage with much higher magnitudes. This can be attributed to the dynamics of the two damage peaks in the PNP at the EB interface, as well as the relative ease of annealing the P regions of the SCR in a PNP. At high currents and elevated temperatures, hydrogen molecules are able to diffuse laterally within the oxide from the N region and anneal the P regions of the interface. The electrical effect of the P region being annealed is more pronounced in the PNP than in the NPN due to a larger concentration of holes in the P region of the PNP than in the P region of the NPN (due to doping differences). This changes the steady diffusion

limited damage seen in the NPN to an aggressive damage intertwined with aggressive annealing in the PNP. These effects become exaggerated at high temperatures, which favor the annealing reaction.

To further validate the claims in this section, the inverse mode electrical degradation of the transistor to high-current stress is considered. Unlike the PN junction at the EB, the PN junction of the BC region has a SCR consisting of a longer P region than N. As a result, in inverse mode, the P region becomes the limiting region for the damage rate. Based on the above predictions, the PNP device is expected to show less inverse-mode degradation than the NPN device in response to high-current stress at high temperature. As expected, this exact behavior was observed in measurements, as shown in Figure 5.11. In [61] it was concluded that an energy well formation due to high germanium content is present in SiGe HBTs that amplifies Auger recombination and high current damage. If this were true, the PNP device with the higher germanium content should experience more forward and inverse mode degradation compared to the NPN when subjected to high-current stress. However, the diminished inverse-mode degradation for the PNP strongly supports the theory for non-constant activation energy for damage along the oxide interface.

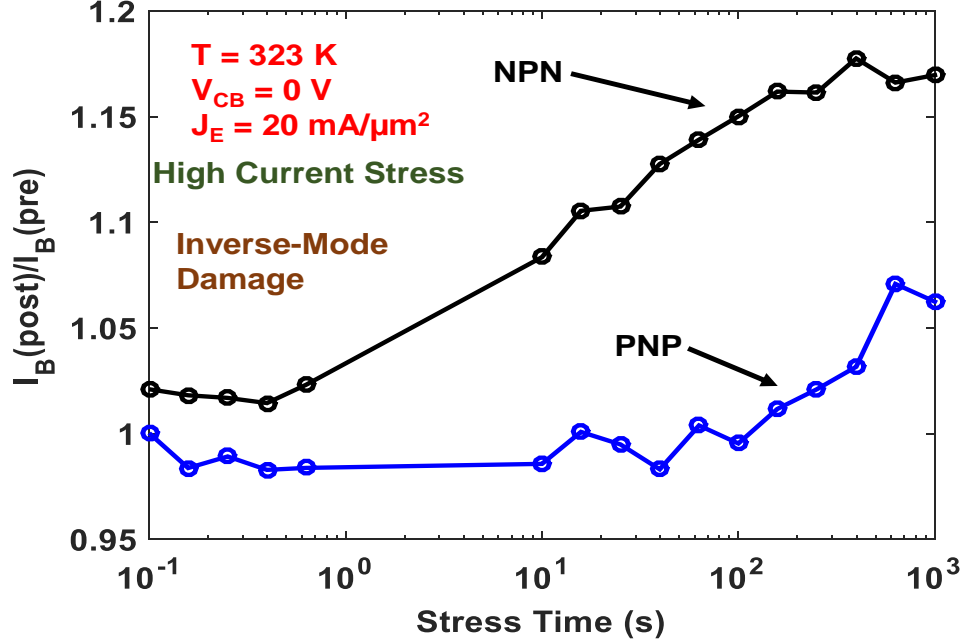


Figure 5.11: Inverse-mode (STI) degradation due to forward-mode high-current stress at 323 K for $J_E = 20 \text{ mA}/\mu\text{m}^2$. Extracted at $J_C = 10 \text{ nA}/\mu\text{m}^2$.

To calibrate the PNP degradation across temperature, a common mixed-mode stress condition of $V_{CB} = 8.5 \text{ V}$ and $J_C = 400 \mu\text{A}/\mu\text{m}^2$ was used. The base current degradation seen under forward mode of operation has been used as a FoM to compare the magnitude of the induced damage. Figure 5.12 shows the damage calibration of simulations to data for the PNP device. The ϕ_{hot} used in this work and in [3] are 1.6 eV and 2.3 eV, respectively. A constant ϕ_{hot} was used as an approximation to the limiting base doping type, as this produced sufficient calibration. The scattering length used for the PNP in this work and the NPN in [3] are 6.75 nm and 6 nm, respectively. The higher value for the PNP is permissible due to the increased Ge content, and these scattering lengths are well within the 5-7 nm range reported in [71].

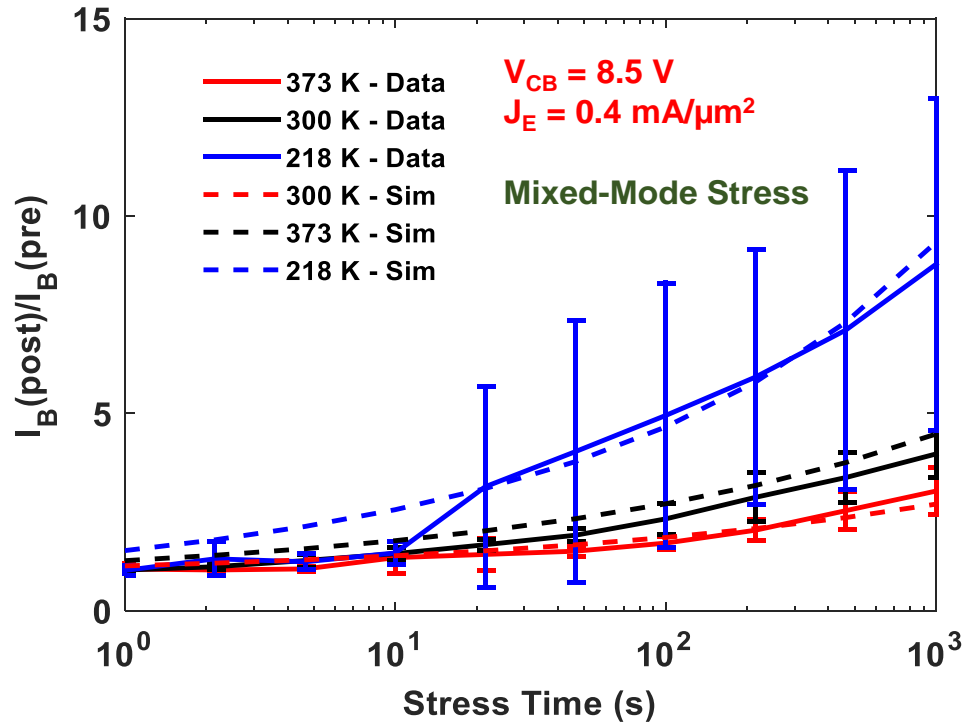


Figure 5.12: Mixed-mode degradation of a PNP device. Calibration of TCAD to measurements for I_B degradation over temperature for a mixed-mode stress condition of $V_{CB} = 8.5$ V and $J_E = 0.400$ mA/ μm^2 . The base current degradation is extracted at $J_C = 10$ nA/ μm^2 from forward-Gummel characteristics. Vertical error bars show the spread of data across 4 devices.

5.7 Summary

In this work, the reliability differences between matched complementary SiGe HBTs were investigated in-depth using experiments in conjunction with calibrated TCAD. First, the device-level differences between the two devices were detailed, beginning with the issue of matched performance and the necessity to incorporate more Ge and collector doping in the PNP. The electrical disparity between the two devices in terms of higher fields, impact-ionization, and hot carrier rates were examined and it was understood why the PNP was naturally predisposed to more serious reliability issues. Next, the carrier-level differences (scattering length ratios) for hot carrier damage between the two devices were

further expanded to account for selective facilitation of carriers by fields within the two devices.

Finally, the interface level damaging and passivating reaction differences between N and P-type regions adjacent to an oxide interface was explored in detail to help explain why a PNP damages sooner: 1) even when operated at stress conditions (high current) that do not produce high electric fields; and 2) irrespective of producing hot carriers that are close (within 2-3 multiples of scattering length; i.e., from reverse EB stress or high-current stress) or away (mixed-mode stress) from the EB interface. Based on simulated and measured values in the literature, qualitative functions for activation energies required for the two reactions were shown for further refinement in modeling. This work essentially brings to light that P-type regions adjacent to oxide interfaces are more resistant to hot carrier damage and are more receptive to being annealed compared to their N-type counterparts. This has important implications for future designs of matched and reliable complementary SiGe HBTs in scaled C-SiGe technologies.

This physical difference between the two region types produces a bifurcated reliability response in the case of PN junctions and their SCRs near an oxide interface. For junctions that have longer N regions and shorter P regions, the long-term reliability is contingent on the N region (as in the case of PNP under forward mode bias) and the interface will experience accelerated aging compared to a junction with identical but inverted doping polarity. Similarly, junctions that have longer P regions and shorter N regions have their long-term reliability set by the P region (similar to NPN under forward mode bias).

Under electrical stress, both regions of a PN junction do get damaged along the interface. The relative damage of each region depends heavily on the electrical bias, temperature, the level of hot carrier energy produced, and the proximity of a hot carrier to a particular region. This in turn determines the lateral flow (P to N vs N to P) of hydrogen along an interface and the relative magnitude of annealing a device experiences at a particular temperature. This complex interplay between the high current Auger damage and annealing can be modeled once proper models are in place for H transport. Once complete, this will be an invaluable design aid for circuit designers requiring reliability estimates for the matched performance of complementary SiGe HBT circuits.

CHAPTER 6

HOT-CARRIER-DAMAGE-INDUCED CURRENT GAIN

ENHANCEMENT (CGE) EFFECTS IN SiGe HBTs

This work investigates high-current stress mechanisms and demonstrates how Auger hot carriers can damage both oxide interfaces and polysilicon regions of the emitter and base. A new current gain enhancement (CGE) effect is proposed, which involves hot-carrier damage to the polysilicon emitter and extrinsic base leading to the degradation of the associated minority carrier mobilities. The different CGE mechanisms in SiGe HBTs under forward and inverse modes of operation are demonstrated. The hot-carrier damage responsible for CGE at high injection is explored in depth with the help of TCAD simulations. Evidence for this effect has been gathered with good statistical significance from various stress conditions, various technologies, complementary (NPN+PNP) devices, and from DC and AC measurements. The new polysilicon degradation mechanism proposed in this work has been generalized and is important for accurately modeling the changes in base resistance and current gain (β) at high injection, where circuits are typically biased to extract maximum device performance. The analysis in this work resulted in a publication [6].

6.1 Motivation

Traditionally, hot carrier damage in SiGe HBTs has been associated with the physical damage of oxide interfaces. Mixed-mode (high voltage stress above BV_{CEO} at modest currents) and reverse emitter-base stress have been known to cause damage to the

EB and STI oxides due to hot carriers generated by large electric fields. These damage mechanisms produce an increase in the non-ideal base current over time under both forward and inverse mode operations at low injection. However, the degradation of the Gummel characteristics due to high-current stress has shown non-classical behavior. At low injection, the base current rises, but previous studies show that in the medium to high injection regime, the base current can go up, go down, or do both over time. The measured Gummel characteristics in Figure 6.1 show the different degradation regions as described following a high-current stress condition. Several authors have attributed such electrical degradation to damaging of the polysilicon emitter but have not given conclusive or detailed evidence of the process by which the device characteristics degrade [35], [36], [61], [72].

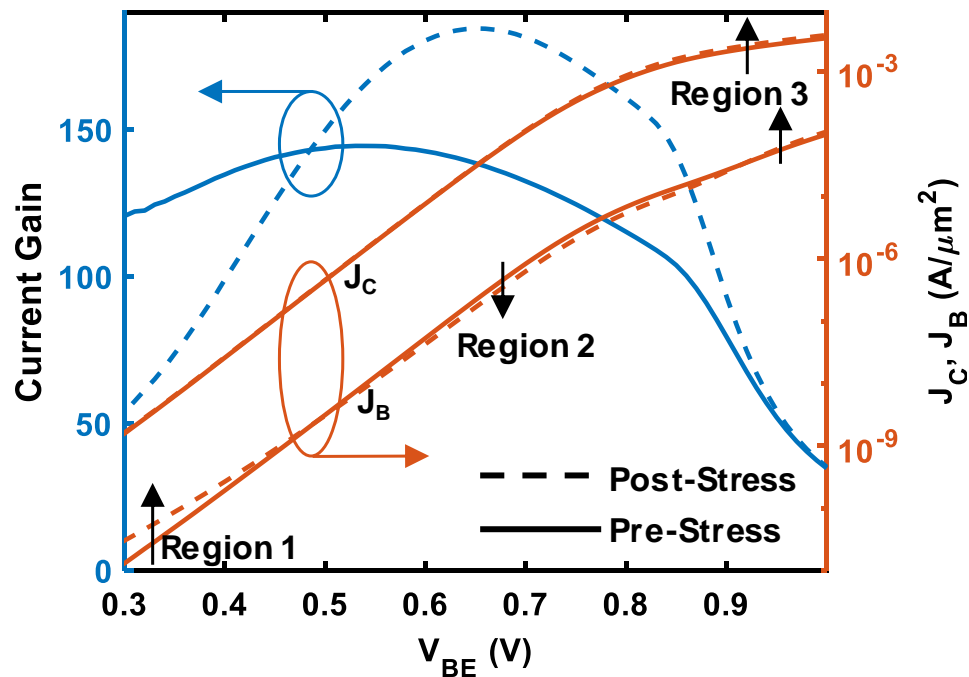


Figure 6.1: Measured degradation of Gummel characteristics and β in an NPN SiGe HBT following a high-current stress of $V_{CB} = 0$ V, $J_E = 21.5$ mA/ μm^2 .

Previous models have generally only predicted the base current degradation at low injection (Region 1 in Figure 6.1) due to high field stress conditions [3]. Individual SiGe HBTs in amplifier circuits sweep over a wide range of currents and voltages on the output plane that can span several distinct annealing and damage regions. Therefore, having an accurate model that can also predict the high injection region is essential for designing and optimizing circuits for both optimal reliability and performance. The present work provides an explanation for a current gain enhancement (CGE) process (Region 2 in Figure 6.1) that occurs in SiGe HBTs during hot carrier damage. This behavior was first explained using a model considering extrinsic base surface inversion due to high density of embedded oxide charge and oxide interface traps [73], [74]. Although that early model showed CGE, it did not sufficiently capture resistance changes (Region 3 in Figure 6.1). Experiments in [72] showed that the hydrogenation of polysilicon affects both Region 2 and 3. However, the exact material parameter responsible for electrical degradation was not identified. In [4], a physics-based TCAD degradation model demonstrated for the first time how Auger hot carrier damage to oxide interfaces under high-current stress degrades the low injection current gain (β) in a manner similar to the high electric field stress. The present work builds on [4], [35], [36], [61], [72] and explains how Auger hot carriers can also depassivate the grain boundaries of emitter and base polysilicon, degrade the minority carrier mobilities, and thereby increase the high injection β under forward and inverse modes. Experimental evidence from three different SiGe HBT platforms, complementary (NPN + PNP) devices, as well as a multitude of stress conditions are used in validating the generality of the CGE process. Full mathematical formalism for polysilicon depassivation and annealing will be addressed in Chapter 7.

6.2 Current Gain Due to Polysilicon

SiGe HBTs predominantly use polysilicon emitters due to the ability of polysilicon to block base current injection and increase β [75]. Due to the unstructured (multi-grain) nature of polysilicon, the mobility (μ) and minority carrier lifetimes (τ) in polysilicon are both smaller than that of comparably doped crystalline silicon. Because of this, minority carriers diffuse much shorter lengths in polysilicon and contribute less to the current flow.

Figure 6.2 shows the current components in a bipolar transistor that contribute to β . Similar to minority carrier injection from the base into the emitter, there is a small amount of minority carrier injection from the emitter that contributes to the base current. Both minority injection currents limit the β of the transistor. Unlike the low injection non-ideal base current from recombination at oxide interface traps, this ideal diffusion current affects the β at all injection levels. When polysilicon has fine grains near the polysilicon-silicon interface, the local μ suppresses the minority carrier injection and dominates the effective recombination velocity at the polysilicon-silicon interface [76], [77].

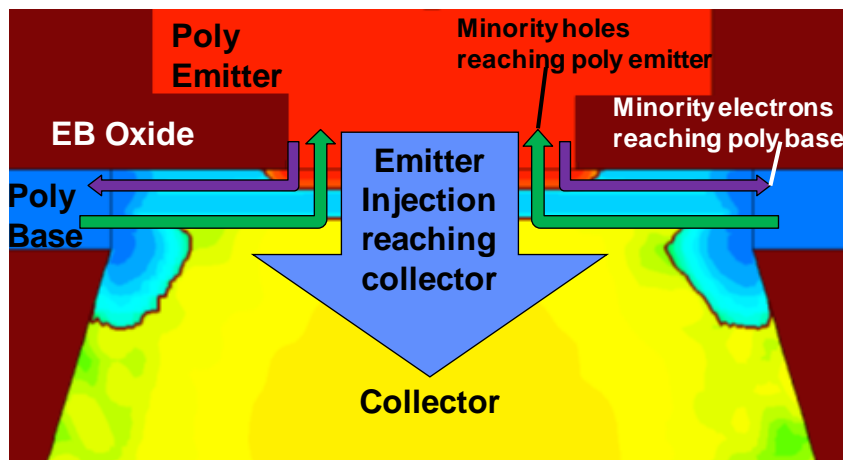


Figure 6.2: Current components contributing to and limiting current gain.

6.2.1 Hot Carrier Damage of Polysilicon

In well-engineered devices, and in the absence of an intentional interfacial oxide, minority carrier injection into the polysilicon is determined by the quality of the growth process and the physical properties of polysilicon. Literature shows that hydrogen plays a large role in the passivation of dangling bonds along the grain boundaries in polysilicon and thereby reduces the resistivity, improves the mobility of carriers, and even improves dopant activation. A 3x reduction in passivation can translate to 1000x increase in resistivity, and passivated polysilicon can have 3.5x longer diffusion lengths for minority carriers [78], [79]. Through interactions with hot carriers, hydrogen atoms passivating the grain boundaries of polysilicon can become dislodged, similar to trap state creation at Si-SiO₂ interfaces. This depassivation causes the local mobility of carriers within the polysilicon to degrade and in turn reduces the diffusion length of minority carriers injected in polysilicon. Both polysilicon emitter and polysilicon base are susceptible to such hot carrier damage. As the minority carrier injection into the polysilicon emitter and base is reduced, the base current goes down and the β is enhanced beyond the initial value of a device.

Polysilicon mobility degradation and CGE in SiGe HBTs can occur because of hot carriers generated from different driving mechanisms, such as impact-ionization or Auger generation. Because the scattering length for hot-carriers in polysilicon is expected to be much smaller than crystalline silicon due to the grain structure, hot carriers produced under mixed-mode stress in the CB junction or reverse EB stress are more likely to stop near the polysilicon-silicon interfaces of the emitter and base, and cannot penetrate further. In

contrast, under high-current stress, Auger hot carrier generation can happen deep within the polysilicon emitter and base as seen in Figure 6.3(a), which can produce damage spatially within the polysilicon.

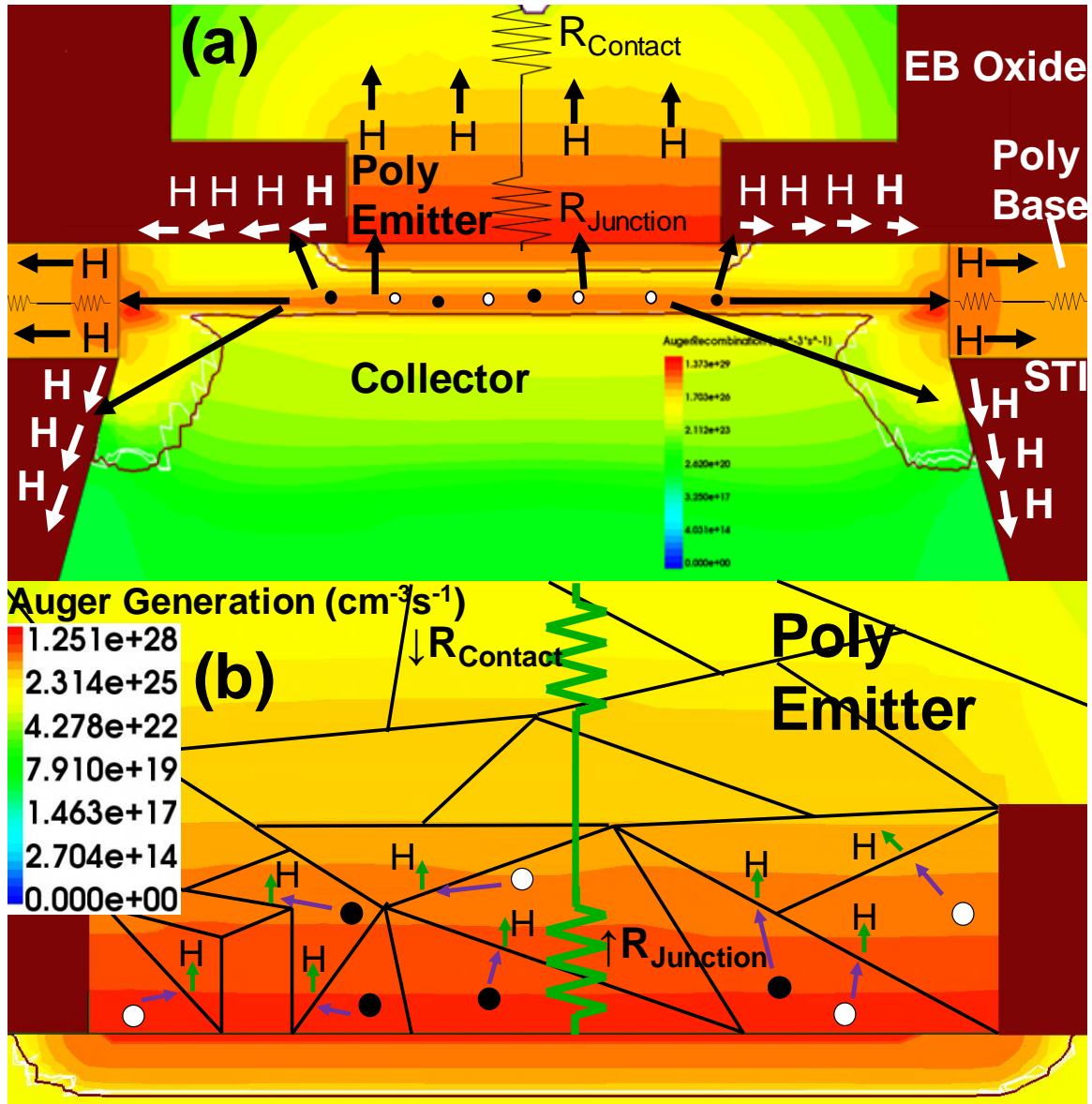


Figure 6.3: (a) High-current stress induced Auger hot carrier damage to oxide interfaces and polysilicon, and hydrogen movement. (b) Grain boundary damage of polysilicon emitter. Overall polysilicon resistance a function of local hydrogen distribution.

6.2.2 Vulnerabilities for CGE Due to Polysilicon Dopants

Ignoring β contributions from oxide interface damage, the gain enhancements under forward and inverse modes depend on how the minority carrier diffusion lengths in the polysilicon emitter and base compare with the dimensions of those polysilicon stacks. This carrier diffusion length is sensitive to the majority dopant type. The electron diffusion length associated with an acceptor doping of $1 \times 10^{20} \text{ cm}^{-3}$, is greater than the hole length of an equivalent donor doping by 3.5x due to μ differences [79], [80]. As a result, for the same polysilicon geometry and μ degradation, P-type regions are initially more susceptible to CGE.

While P-type doped regions have longer electron diffusion lengths that favor the minority charge collection, N-type doped polysilicon regions are vulnerable to long-term physical damage. It is known from [5] that N-type doped oxide interface regions can be depassivated with a lower activation energy (1.6 eV) than the P-regions (2.3 eV). Similarly, lowered activation energy for depassivating N-type doped polysilicon can also be deduced from the measured formation energies of deep states associated with different dopants in polysilicon, with a difference in formation energies of 0.3 eV for a hydrogen concentration of $1 \times 10^{20} \text{ cm}^{-3}$ and a dopant concentration of $1 \times 10^{18} \text{ cm}^{-3}$ at 350 °C [81]. As the N dopant has the higher formation energy, the hydrogen Si-H bond is less stable and requires a smaller activation energy to produce a free hydrogen atom. The formation energy of deep traps (E_{form}) in polysilicon at temperature T and hydrogen concentration C_H is given as

$$E_{form} = E_f^0 - kT * \ln\left(\frac{N_H}{C_H}\right), \quad (6.1)$$

where E_f^0 is the actual formation energy of deep traps at absolute temperature, N_H is the concentration of interstitial diffusion sites, and k is the Boltzmann constant [81]. The value for C_H changes with Fermi energy, which drives the difference in formation energy in N- and P-type polysilicon. These differences due to doping can pose reliability issues to NPN and PNP devices under forward and inverse modes of operation depending on the geometry, stress condition and operating temperature of the device.

6.2.3 Simplified TCAD Simulations showing CGE

In order to qualitatively understand the effects of polysilicon depassivation on CGE, a SiGe HBT was simulated in the Synopsys Sentaurus TCAD environment using varying polysilicon properties. The hydrodynamic transport scheme was used in the simulations to strike a balance between simulation speed and accuracy, without having to resort to the over-simplified drift-diffusion approach, or solve the full Boltzmann transport equation noise-free using Monte-Carlo techniques.

Polysilicon μ and τ have a similar effect on the minority carrier diffusion length, which in turn governs minority carrier injection and recombination. The effects of independently reducing the two parameters by 10x on recombination events is shown in Figure 6.4. Reducing τ decreases recombination away from the interface while increasing it near the polysilicon-silicon interface. Whereas, changing the μ reduces recombination throughout the polysilicon. Although polysilicon depassivation could affect τ , in this work,

due to the stronger effect of μ on reducing recombination, only μ is varied and τ is assumed to be constant.

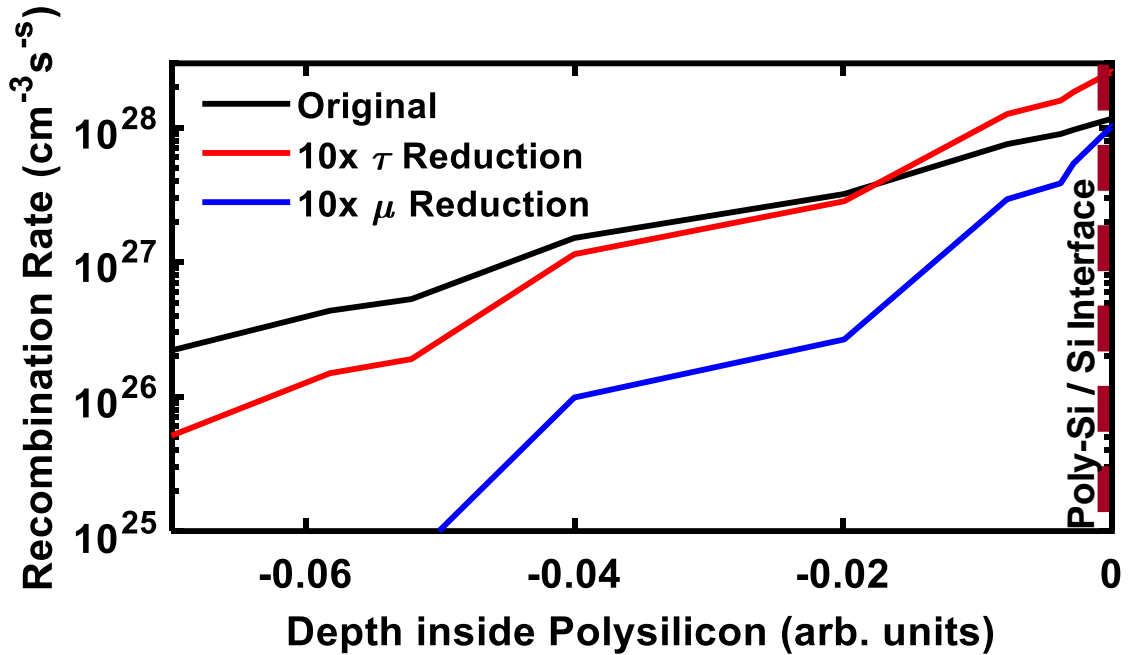


Figure 6.4: TCAD simulation of the total recombination rate (Auger + SRH) when μ and τ are independently degraded by 10x.

Under high-current stress at elevated temperatures, not only is polysilicon getting depassivated near the silicon-polysilicon interface, but also the evolving hydrogen is free to diffuse. Considering the hydrogen diffusion coefficient is greater in polysilicon than in silicon, and assuming the polysilicon-oxide interfaces are passivated sufficiently, the free hydrogen diffuses deeper within polysilicon [82]. Because of this hydrogen diffusion, the minority carrier μ and polysilicon resistivity (which depends mostly on majority carrier mobility) degrade in certain regions and improve in others. The total polysilicon resistance from the contact to the silicon-polysilicon interface is spatially dependent on the local passivation as shown in Figure 6.3(b). In this work, the model was given a finite series

contact resistance and uniform polysilicon μ in each device region for simplicity. This way, the polysilicon μ controlling minority carrier injection and CGE, and the contact resistor controlling changes in polysilicon resistance can be varied independently.

The degree of change in μ and series resistances used in these simulations is not by any means calibrated and does not follow well defined relationships. However, they serve to qualitatively illustrate that Regions 2 and 3 from Figure 6.1 can easily be captured with a single parameter (μ) degrading spatially. To exaggerate the effects of depassivation on β , a 10x reduction in polysilicon μ was taken as a liberal estimate for the 1000x reduction in resistance mentioned in [78]. Figure 6.5(a) shows that decreasing the polysilicon μ alone by 10x decreases the base current under forward mode, reproducing Region 2. Because the polysilicon μ is uniformly changed, the currents at high injection become limited by the high resistance of the polysilicon and Region 3 is not captured. To sufficiently negate the effects of μ degradation on the total series resistance, additional simulations were performed by simultaneously reducing polysilicon μ and the contact resistances by 10x. The contact resistance values were adjusted until the desired Region 3 behavior was obtained. Figure 6.5(b) illustrates the effects of these changes to forward-Gummel characteristics. The medium injection region ($V_{BE} = 0.6-0.8$ V) is characterized by the CGE effect. In the high injection region above 0.8 V, β not only increases, but the polysilicon resistance decreases, facilitating increased current flow.

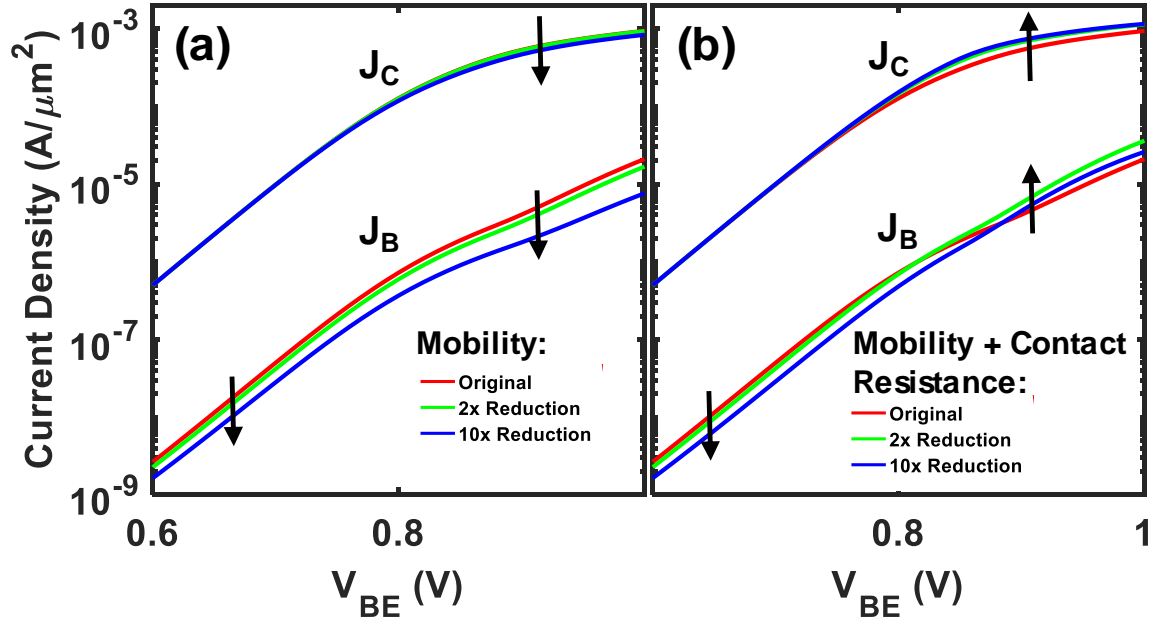


Figure 6.5: TCAD simulation of forward-Gummel characteristics for a 1st generation SiGe HBT. (a) With μ reduction (b) With μ and contact resistance reduction. Original series resistance of 100Ω at the emitter and 500Ω at the base.

Under inverse mode operation, the physical crystalline silicon collector acts as the electrical emitter. Because the crystalline silicon cannot get damaged under high-current stress, the minority carrier injection into the collector does not change. Although the polysilicon emitter can get damaged, there is no minority carrier injection into the emitter under inverse mode for base current contribution. The polysilicon extrinsic base is the only region left that can be damaged and contribute to changes in the minority carrier injection into the base. This behavior was verified in TCAD simulations by reducing the mobilities in the emitter and base polysilicon regions independently and looking at the gain enhancements under forward and inverse modes in Figure 6.6. Under forward mode, CGE is largely driven by the degradation of emitter μ , and to a lesser extent by the base μ . On the other hand, inverse mode gain enhancement shows no dependence on the emitter μ . Only the base μ degradation enhances inverse mode β .

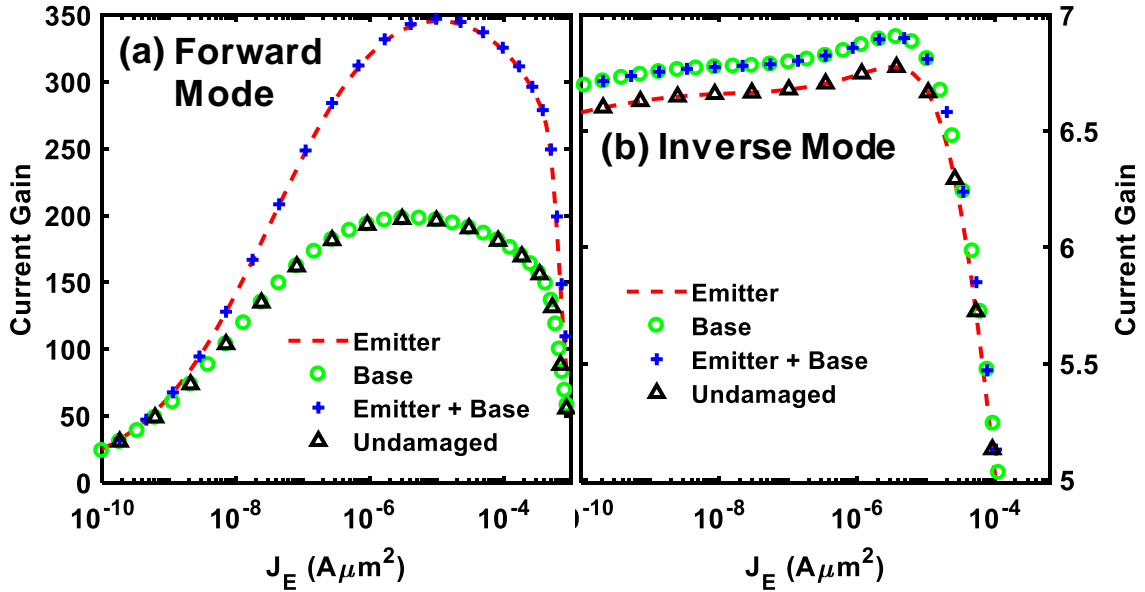


Figure 6.6: TCAD simulation of current gain while independently reducing the mobilities in the emitter and base poly by 10x to qualitatively see damage dependence under (a) forward and (b) inverse modes of operation.

The depassivation-induced μ degradation affecting the minority carrier injection can be easily visualized in Figure 6.7. It is important to point out that advanced technologies employing tall and highly crystalline emitter stacks with contacts well separated from the polysilicon-silicon boundary should be less susceptible to the described CGE effect under forward mode. Nonetheless, the overall β of a device depends on both the oxide and polysilicon damages. To qualitatively illustrate the effect of both damage processes influencing β , a generic degraded interface trap density of $4 \times 10^{11} \text{ cm}^{-3}$ and 10x degraded polysilicon mobilities were chosen. The independent and cumulative effects of these altered device parameters influencing the β under forward mode is shown in Figure 6.8. A model considering of only the oxide interface damage clearly overestimates the gain degradation at high injection.

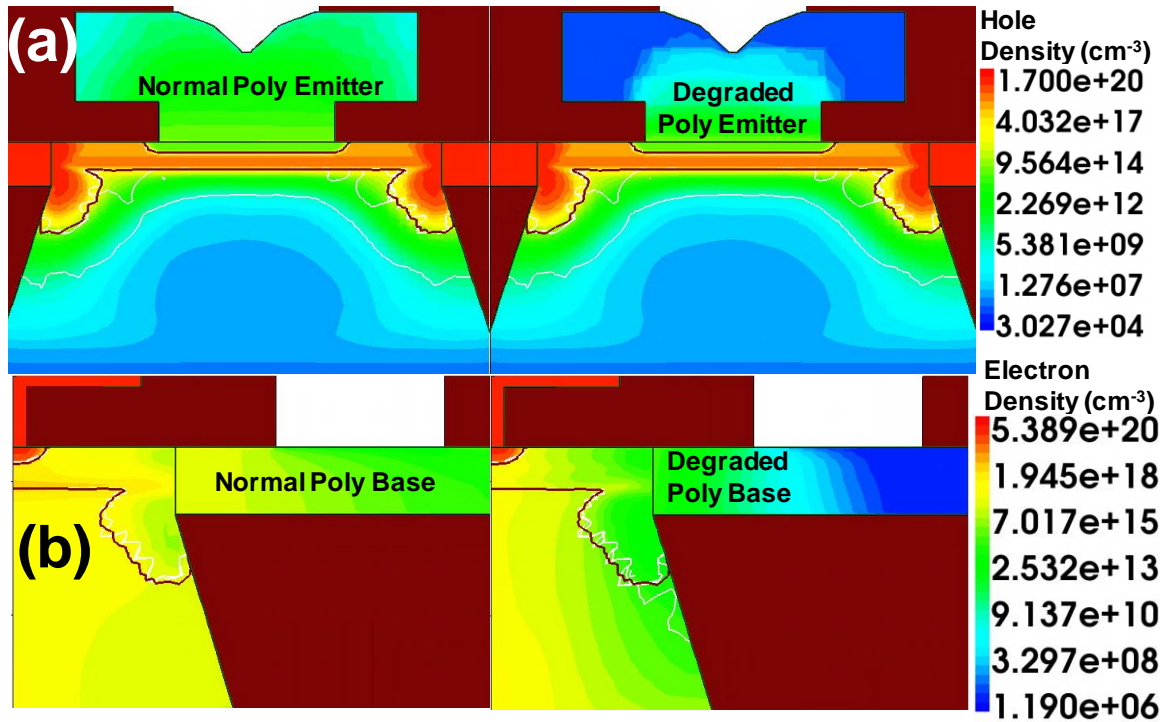


Figure 6.7: TCAD cross-section of 10x polysilicon μ degradation affecting (a) hole injection from the base into the emitter and (b) electron injection from the emitter into the base.

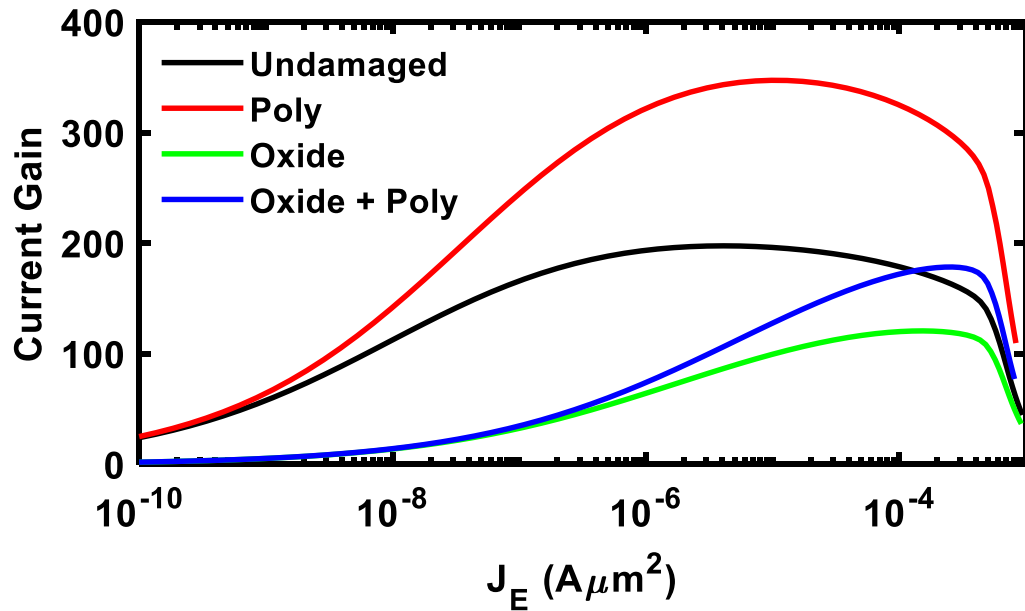


Figure 6.8: TCAD simulation of current gain under forward mode while independently considering the polysilicon and oxide interface damage mechanisms.

6.3 Measured Response to Polysilicon Damage

To substantiate the polysilicon degradation and CGE mechanism described in Section III, various measurements were performed on three different technologies, comprising of the devices in Table 6.1. Unless stated otherwise, the measurements have a sample size of one.

Table 6.1: Performance Metrics of Measured Devices

Device	BV_{CEO} / BV_{CBO}	f_T / f_{max}	$J_C, \text{Peak } f_T$
NPN1^a	3 / 13 V	60.5 / 73.4 GHz	1 mA/ μm^2
PNP1	3 / 10 V	56.4 / 66.3 GHz	1 mA/ μm^2
NPN2	1.7 / 5.2 V	314 / 378 GHz	20 mA/ μm^2
NPN3	12 / 25 V	3.5 / 7.5 GHz	100 $\mu\text{A}/\mu\text{m}^2$

^a The number denotes the technology the device is from

6.3.1 Evidence for CGE in DC Stress Measurements

Auger hot-carrier generation goes up with increasing current density and increasing temperature [4]. The depassivation of grain boundaries in polysilicon is spatially related to the Auger hot carrier production through the current density profile. In order to induce sufficient heating at room temperature for Auger hot carrier generation, NPN1 was chosen with a large emitter area (A_E). Figure 6.9 shows that with increasing current density stress in NPN1, CGE increases. It is worth noting that for sufficiently low current density stress conditions, the device begins with gain degradation due to oxide interface damage such as in the 15 mA/ μm^2 condition. Although these conditions are well above the peak f_T current density, a similar effect with oxide damage dominating early changes and CGE developing slowing can be imagined considering a 10-year EOL with a less aggressive bias.

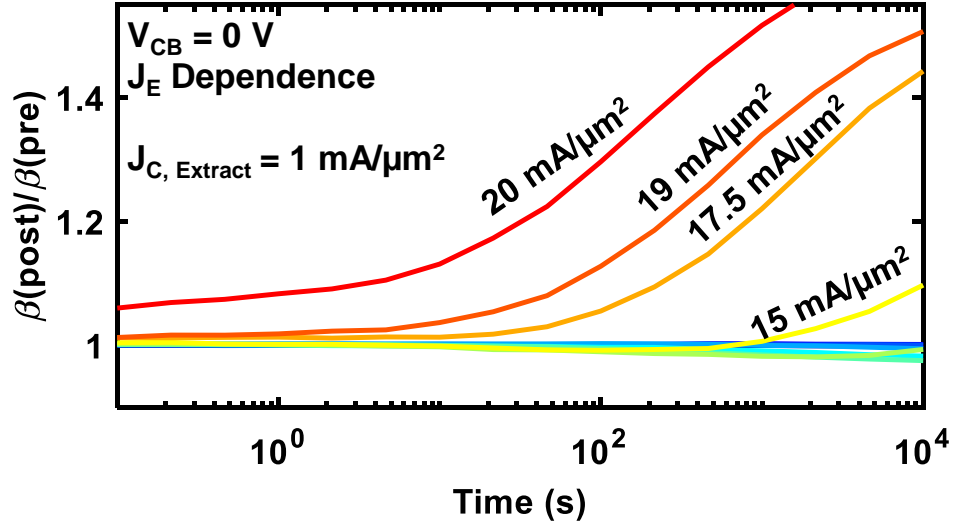


Figure 6.9: Measured forward mode CGE in NPN1 with $A_E = 15.36 \mu\text{m}^2$ following high-current stress at $T = 300 \text{ K}$ with $V_{CB} = 0 \text{ V}$. Colors from blue to red indicate increasing stress current density. β extracted from Gummel characteristics at $J_C = 1 \text{ mA}/\mu\text{m}^2$.

To study the temperature dependence of CGE, a high-current stress condition of $V_{CB} = 0 \text{ V}$ and $J_E = 21.5 \text{ mA}/\mu\text{m}^2$ was applied to NPN1 and PNP1. With high-current stress at elevated temperatures, there is enhanced Auger hot carrier generation that leads to depassivation in polysilicon. In addition, the elevated temperatures combined with self-heating allows hydrogen to rapidly diffuse away from the depassivated boundaries. The degree of depassivation with temperature directly translates to minority μ reduction and gain enhancement. Figure 6.10 shows that this positive temperature dependence of the CGE effect is observable in both NPN and PNP devices. Unlike the NPN device, however, the PNP device undergoes more changes at the very beginning and undergoes a more gradual increase over time. These temporal differences between the two devices are likely due to the different minority carrier diffusion lengths (short-term) and activation energies (long-term) associated with emitter dopants mentioned in section II.

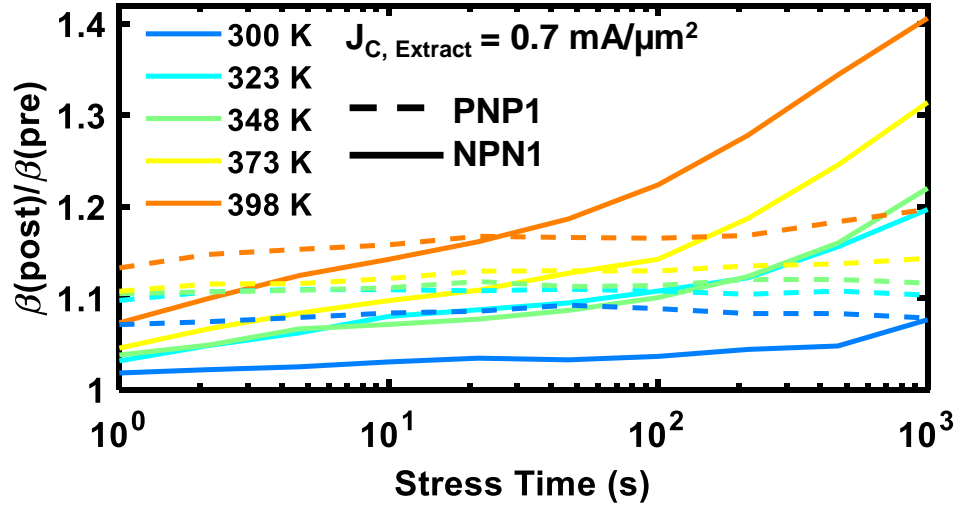


Figure 6.10: Measured forward mode CGE in NPN1 and PNP1 with $A_E = 3.84 \mu\text{m}^2$ following high-current stress of $V_{CB} = 0 \text{ V}$ and $J_E = 21.5 \text{ mA}/\mu\text{m}^2$. β extracted from Gummel characteristics at $J_C = 7e-4 \text{ A}/\mu\text{m}^2$. NPN is given by solid lines and PNP by dotted ones.

Similar to how the ambient temperature influences Auger hot carrier generation and hydrogen diffusion in polysilicon, the magnitude of self-heating in a given device size can also influence CGE. A device with a smaller perimeter to area ratio reaches the same level of lattice heating for less aggressive biasing conditions. As a result, for identical bias conditions, devices with different aspect ratios would have varying levels of oxide and polysilicon damages. The device size variation in CGE at high injection for NPN1 stressed at very high current is shown in Figure 6.11. With stress, all devices initially exhibit a slight decrease in β due to oxide interface damage. Over time, the larger devices switch from exhibiting gain degradation to enhancement while the smaller devices only exhibit the degradation phase. This shows that the polysilicon damage is a much slower process compared to the oxide interface damage. However, with sufficient self-heating, CGE can be a more dominant effect at high injections. This is confirmed by the large device ($3.84 \mu\text{m}$) having more CGE ($> 20\%$) compared to its initial degradation ($< 5\%$).

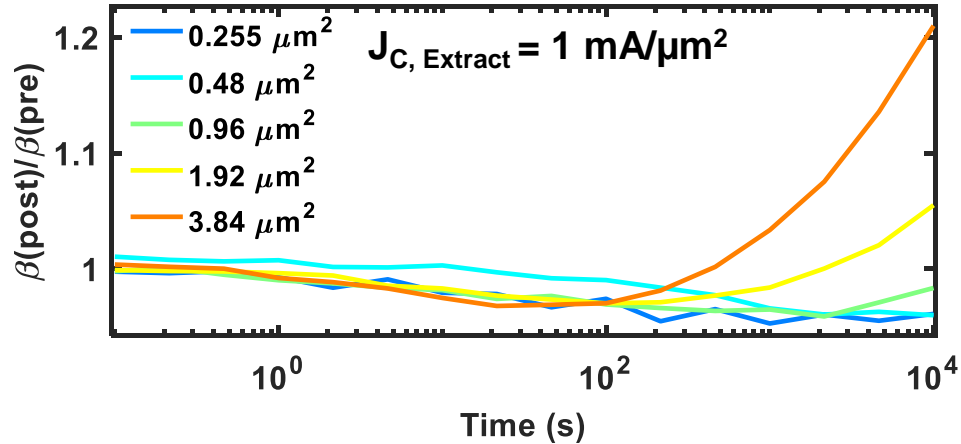


Figure 6.11: Measured current gain degradation and enhancement for a high-current stress condition of $J_E = 21.4 \text{ mA}/\mu\text{m}^2$ and $V_{CB} = 0 \text{ V}$ across various emitter areas at $T = 300 \text{ K}$. β extracted at $J_C = 1 \text{ mA}/\mu\text{m}^2$.

Depending on the bias condition, stress degradation at high temperatures can have a lot of device-to-device variability due to enhanced and competing mechanisms that are either gain-degrading (oxide interface damage due to Auger generation) or gain-enhancing (polysilicon depassivation due to Auger generation or annealing of oxide traps). To illustrate this, NPN2 was stressed under mixed-mode with a constant V_{CB} of 1.5 V and $J_E = 21.5 \text{ mA}/\mu\text{m}^2$ at different temperatures. Under these conditions, hot carrier production is driven by a mix of impact ionization and Auger generation. As the two mechanisms have opposite temperature dependencies, and also since oxide damage cancels the gain from polysilicon degradation, the degradation trends in Figure 6.12 are not monotonic with temperature [4], [61]. NPN2 has significant CGE under inverse mode (5%) and very little change under forward mode (1.5%). The reason for the diminished CGE under forward mode could be because of a tall and highly crystalline emitter design. The fact that inverse mode shows this effect sufficiently over 4 samples at 348 K (one sample showed 10% change) irrespective of forward mode suggests that the spatial degradation of the

polysilicon mobilities, especially in the base, is necessary to explain the measured electrical behavior.

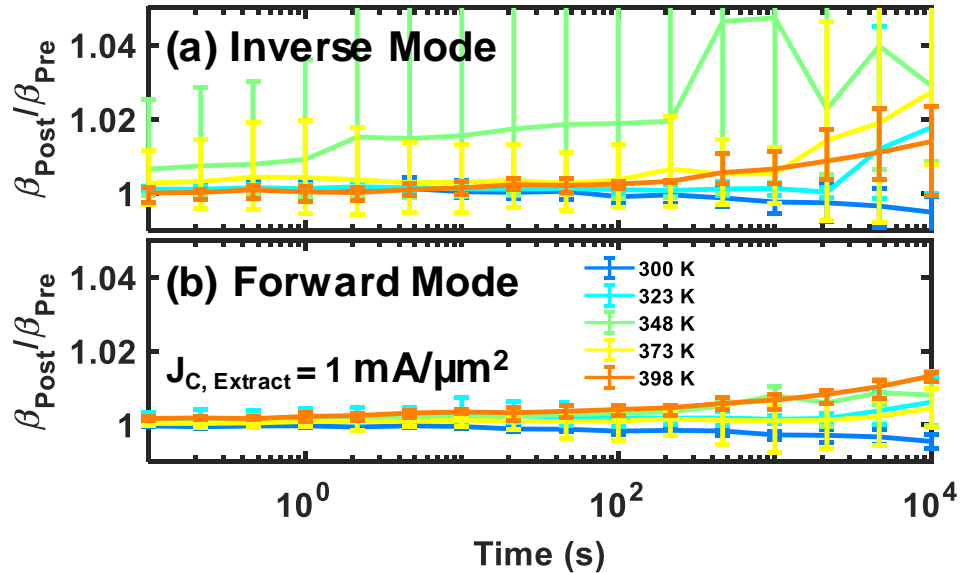


Figure 6.12: Measured current gain degradation and enhancement for a mixed-mode condition of $J_E = 21.5 \text{ mA}/\mu\text{m}^2$ and $V_{CB} = 1.5 \text{ V}$ for NPN2 across various temperatures under (a) inverse and (b) forward modes of operation. β extracted at $J_C = 1 \text{ mA}/\mu\text{m}^2$. 4 device samples per temperature.

Polysilicon depassivation is not limited to Auger hot carrier production. In Figure 6.13, NPN1 and PNP1 were stressed at identical reverse EB stress conditions and their inverse mode degradations were measured. While NPN1 showed the classical β degradation even at high injection, PNP1 showed noticeable CGE (4%) at multiple conditions with increased stress. Considering reverse EB stress does not produce hot carriers with sufficient probability to penetrate the extrinsic base like high-current stress, the damage is limited to silicon-polysilicon interface depassivation. As the activation energy required for depassivating the N-poly base of the PNP device is lower than the P-poly base of the NPN device, the PNP device undergoes more base degradation and shows inverse mode CGE. Besides, it was already established in [5] that PNP device undergoes less STI damage due to the long P collector region adjoining the oxide. Thus, the oxide

interface damage is minimized and the CGE is maximized in PNP1. On the other hand, NPN1 undergoes less CGE and more oxide interface damage.

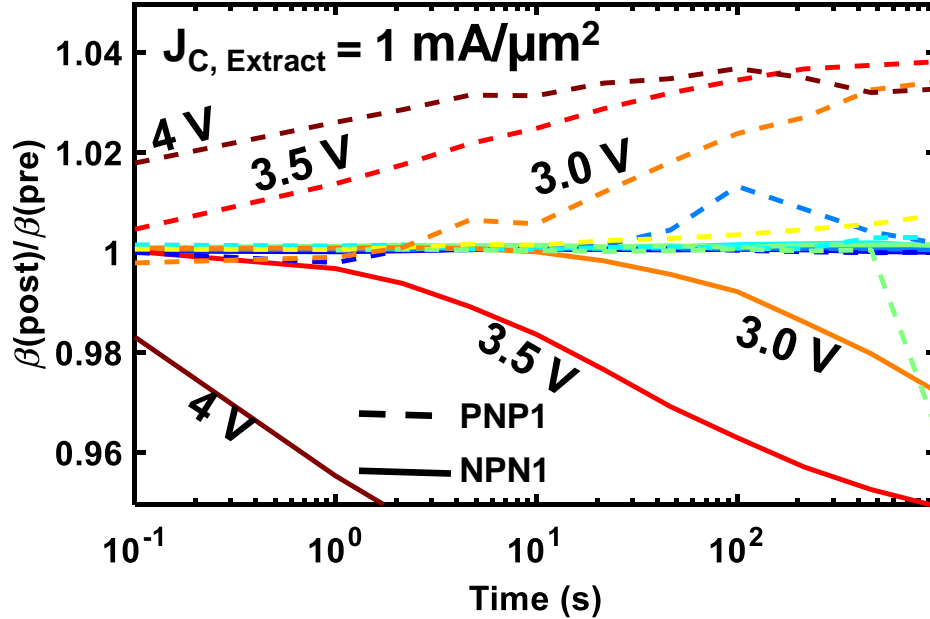


Figure 6.13: Measured inverse mode complementary β degradation following reverse EB stress at $T = 300\text{K}$. Colors from blue to brown indicate increasing stress condition from $V_{BE} = 0$ to 4 V in steps of 0.5 V . Extracted from inverse-Gummel characteristics at $J_C = 7e-4\text{ A}/\mu\text{m}^2$. NPN is given by solid lines and PNP by dotted ones.

6.3.2 Evidence for Polysilicon Degradation

Although [35], [36], [61], [72] suggest the degradation of the polysilicon emitter to be the major driving factor for the changes in Region 2 and Region 3, the exact parameter driving the dynamics of the currents was not fully understood. The μ degradation due to polysilicon depassivation proposed in this model also affects the extrinsic polysilicon base, which has never been mentioned in the literature. One way to demonstrate the change in the μ of the extrinsic base is by showing evidence for change in the extrinsic base resistance (R_B) with stress. Since the DC method for R_B extraction in [82] is destructive and inaccurate, the open-circle AC method from [83] is used instead in this work.

Subsequently, the direct effect of R_B change on AC metrics like f_T/f_{max} were also determined.

NPN3 was stressed under a common-emitter condition of $V_{CB} = 10$ V and $V_{BE} = 1.3$ V (equivalently $J_E = 10$ mA/ μm^2) at 323 K over a period of 100,000 s. For this device, the condition is a high-current stress that is well below the BV_{CEO} of the device and the V_{CB} merely enhances the self-heating to accelerate the damage. S-parameters were measured after each stress interval and the R_B extracted using the open-circle impedance method, as shown in Figure 6.14. Although the extracted value is the sum of base and emitter resistances, R_B is assumed to be much larger than the emitter resistance in these devices. Moreover, f_{max} would only change if R_B changes. During the stress period, the extracted R_B increases by as much as 15 Ω .

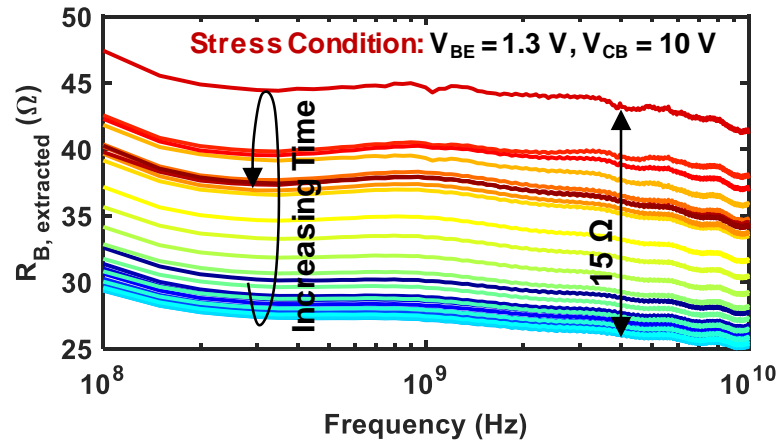


Figure 6.14: Evolution of the extracted R_B as a function of frequency during a stress of $V_{CB} = 10$ V and $V_{BE} = 1.3$ V on NPN3 at $T = 323$ K. S-Parameters were measured for $V_{BE} = 1$ V. Colors from blue to red indicate increasing stress period from 0 to 100,000 s. During the stress period, the extracted R_B changes by as much as 15 Ω .

In Figure 6.15, the correlated degradation of important AC and DC FoMs have been plotted over the stress period. The fact that $f_{T,Peak}$ is insignificantly affected (-2%)

compared to the degradation of $f_{\max, \text{Peak}}$ ($< -20\%$) suggests that the capacitances at the BE and BC junctions are not affected much despite the damage to polysilicon base and emitter. As β gets enhanced by 30% due to polysilicon μ degradation, R_B correspondingly increases by as much as 60%, confirming the earlier suggestion that R_B must increase with μ degradation in the extrinsic base. Base current densities at low and high injections initially start off with an increase due to Auger hot carrier damage to EB oxide. Low injection J_B starts with a much larger degradation ($> 20\%$) compared to the high injection J_B due to the stronger effect of oxide interface damage at low injection. With time, both quantities decrease due to polysilicon μ degradation, almost maintaining the same difference of 15% between them. This suggests a near parallel decrease in base current. The collector current density extracted at $V_{BE} = 1 \text{ V}$ represents high injection and is very much influenced by series resistances that keep changing with polysilicon depassivation and passivation at emitter and base. For a common-emitter condition of $V_{BE} = 1.3 \text{ V}$, the device certainly does not maintain the same current density during stress.

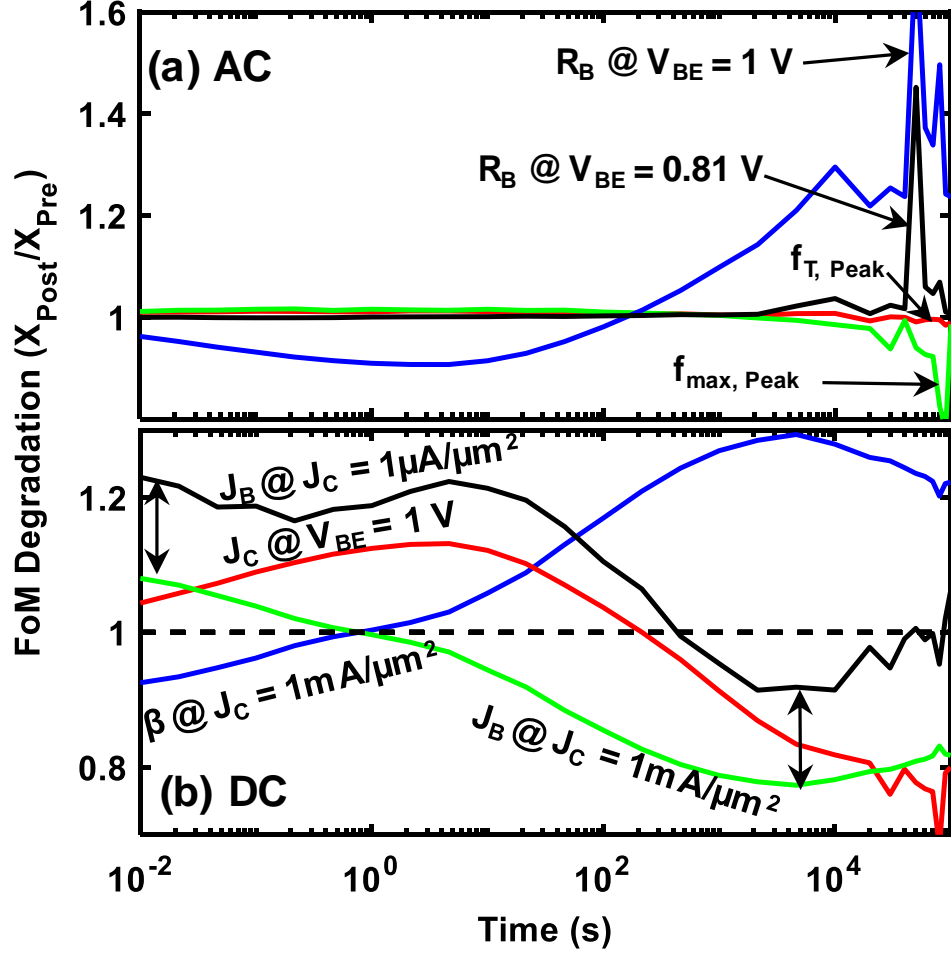


Figure 6.15: Correlated degradation of (a) AC and (b) DC FoMs during a stress of $V_{CB} = 10$ V and $V_{BE} = 1.3$ V on NPN3 at $T = 323$ K. Peak f_T/f_{max} extracted from S-Parameters. R_B extracted from open-circle plots based on S-Parameters at $V_{BE} = 1$ V. J_B , J_C , and β degradation are extracted from forward-Gummel characteristics.

Compared to R_B (evaluated at $V_{BE} = 1$ V, a resistance dominated regime), which quickly changes with changing β , $f_{max, Peak}$ changes only after 1000 s. The reason for this is the $J_{C, Peak}$ for the device is only $100 \mu A/\mu m^2$, which corresponds to $V_{BE} = 0.81$ V. As R_B is a function of the applied bias, at smaller V_{BE} , the device is less resistance dominated. Thus, the magnitude of change in R_B is less and takes longer to develop a significant level of change. Measuring NPN1 or NPN2 would allow a better alignment of the current densities for $f_{max, Peak}$ and the resistance-limited region. However, getting stable and noise-free measurements in a fast technology platform at elevated temperatures for elongated

stress periods was challenging due to drifting probe contacts and S-parameter calibrations. Nonetheless, CGE is present in NPN3 at both current levels under DC conditions. Although β changes very slowly after hitting its peak, R_B , J_C , and high injection J_B fluctuate quite a bit. This can be explained by the constant redistribution of hydrogen deeper within the polysilicon at high temperatures. During stress, the portion of polysilicon close to the silicon-polysilicon interface produces the most amount of Auger hot carriers. As a result, this region constantly gets depassivated and the minority μ associated with this region stabilizes at a low value. Because β largely depends on the minority injection peak set by the μ at the interface, it too stabilizes. Whereas, the free hydrogen atoms diffuse and redistribute themselves deeper within polysilicon. In the process, the grain boundaries away from the silicon-polysilicon interfaces constantly get passivated and depassivated. This causes a fluctuation of series resistances and currents at the terminals without altering β significantly.

6.4 Summary

This work explains how β enhanced by hot carrier damage to polysilicon is fundamentally different from oxide interface damage. The components of β and the process by which it is enhanced under forward and inverse modes during hot carrier damage is detailed. The overall aging of the base current and β at medium to high injections is determined by not only oxide interface damage, but also the spatial degradation of μ in polysilicon, which influences minority carrier injection in emitter and base. A new current gain enhancement (CGE) effect along with a polysilicon resistance degradation is proposed with the help of simplified simulations verified in TCAD. The reliability limitations of N-

type and P-type doped polysilicon regarding CGE are explored for better polysilicon stack design.

CGE under high current, mixed-mode and reverse EB stress conditions were measured to establish this effect under different hot carrier generation mechanisms with good statistical significance. As high-current stress has the strongest impact on CGE, its temperature and self-heating dependencies are detailed. The generality of this effect is validated across NPN and PNP devices under the forward and inverse modes of operation. This work is the first to present evidence for CGE under inverse mode and also show evidence for why base μ and R_B must change. To correlate CGE with polysilicon μ degradation, AC measurements are provided to show the dynamics of R_B during stress.

Aging models only considering oxide damage cannot capture the high injection CGE under aggressive short-term stress, and would overestimate the EOL β degradation for analog circuits under normal operation. The changes in polysilicon resistance affect current mirrors, impedance matching and premature device breakdown. These limit performance and SOA for high speed circuits and power amplifiers (PAs). Thus, accurately predicting β and R_B is essential for circuit reliability. This requires mathematically modeling the full reaction mechanics of polysilicon damage, and is addressed in Chapter 7.

CHAPTER 7

HIGH TEMPERATURE DEGRADATION EFFECTS IN SIGE HBTs

This work shows a spatial mobility degradation model for grain boundary passivation in polysilicon and how CGE and resistance degradation effects described in Chapter 6 can be captured in SiGe HBTs. Extensive high temperature measurements on packaged Kelvin structures are done to accurately capture changes at high injection. The findings in this work determine a comprehensive list of parameters that must be modeled to correctly predict aging in devices, which determines the aging of circuits. The results from this study are waiting for approval for submission in IEEE TED.

7.1 Motivation

While SiGe HBTs have been shown to operate over a wide range of temperatures spanning almost 600 K [84], [85], multiple hot carrier mechanisms identified in Figure 1.1 start causing problems when deviating from room temperature operation. With increasing temperatures up to 573 K, damage due to mixed-mode stress and high-current stress have been shown to decrease and increase respectively [86]. The FoM for measuring degradation in Figure 1.1 is base current leakage due to oxide interface traps. However, SOAs for other FoMs like resistance degradation can be very different across bias and temperature. As summarized in [6], resistance changes are even more problematic for circuit designs as they can cause bias shifts and AC performance degradation. The primary method for inducing degradation in polysilicon resistance is high-current stress as it helps generate hot carriers sufficiently deep within polysilicon emitter and base. In addition, the positive

temperature dependence of Auger hot carrier production gets complemented by the positive temperature dependence of hydrogen diffusion, which helps create damage within polysilicon and at oxide interfaces. At extreme temperatures, the annealing reaction mentioned in Section 2.2.3 also starts to dominate and restricts further creation of damage.

The present work investigates to what extent oxide interface damage and polysilicon resistance degradation can be correlated, and also explores whether Auger hot carrier damage sees any form of saturation behavior at high temperatures up to 573 K. To support the understanding of polysilicon degradation due to hot carrier damage from [6], this work also shows simulations of hydrogen diffusion during high-current stress and how grain boundary passivation evolves with time. From this aged passivation information, this work demonstrates how majority and minority mobilities in polysilicon must change to produce the Region 2 and 3 behaviors seen in Figure 2.3 and Figure 6.1. Finally, based on the measurements in this work, a list of important device parameters is identified for capturing relevant DC and AC degradation information for circuit designers.

7.2 Background on Current Gain Enhancement

To capture the CGE enhancement effects, multiple possible theories have been offered. The work in [73], [74] suggest that embedded oxide charge near the extrinsic base can pinch base current flow and increase current gain. However, this method doesn't provide a satisfactory explanation for resistance changes. The theory mentioned in [35], [87] is that hydrogen trapped at the metal/polysilicon interfaces can release hydrogen, which would diffuse towards the polysilicon/silicon interface and reduce the recombination velocities. This method can capture both CGE and resistance changes and attributes the

source of damage to Auger hot carriers induced by a current density threshold. However, the location of hot carrier production in [35] is loosely defined and fails to offer an explanation for high-field stresses which can also produce CGE, as shown in [6]. Auger hot carrier generation is expected to be the greatest in the neutral base and at the polysilicon/silicon interface. But [35] does not sufficiently explain where the hot carriers are initiated, and why, despite having a low Auger hot carrier generation probability near the metal, there can be hydrogen evolution from this region.

Under reverse-EB and mixed-mode stress, hot carriers typically will lose energy because of grain boundary scattering before even reaching the metal/poly interface. Even if hot carriers do reach the metal interface, the analysis in [35] suggests that hydrogen must diffuse sufficiently into the polysilicon to passivate pre-existing grain boundary traps. Without the self-heating available under high current conditions, the diffusion of hydrogen is limited. Yet, the reverse-EB measurements in [6] demonstrate CGE. Decrease in base current is governed by minority carrier injection, which is determined by the recombination activity happening near the silicon/polysilicon interface. If the hydrogen cannot sufficiently diffuse from the metal interface to the silicon/polysilicon interface to reduce the recombination velocities there, the model in [35] cannot capture CGE. Instead of the hydrogen diffusion downwards from the metal, [6] suggests an evolution of hydrogen with hot carrier damage near the polysilicon/silicon interface, and a diffusion of hydrogen towards the metal contact as illustrated in Figure 6.3. Because the diffusivity of hydrogen is greater in polysilicon, hydrogen diffuses more into the polysilicon as opposed to going towards crystalline silicon. The loss of hydrogen in the polysilicon/silicon interface results

in minority mobility degradation and CGE, and a gain of hydrogen towards the metal interface results in the reduction of resistance.

7.3 TCAD Modeling of Polysilicon Degradation

To validate the behavior in Figure 6.3, the passivation of polysilicon was simulated in Synopsys Sentaurus TCAD environment using the existing multi-state configuration and hydrogen diffusion models. Using the programmer modeling interface (PMI), a capture emission model was implemented for Auger hot carriers to simulate high-current stress. Following this transient simulation, aged Gummel characteristics can be simulated using the passivation information as illustrated in Figure 7.1.

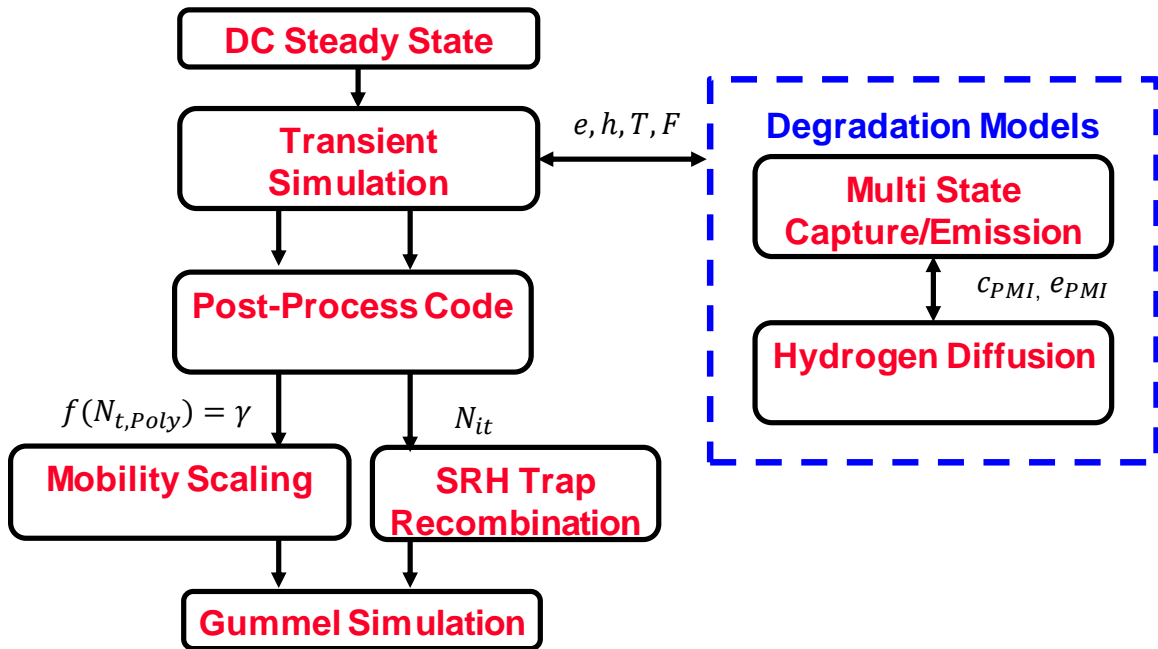


Figure 7.1: Flow diagram of models for simulating polysilicon degradation in Synopsys Sentaurus.

The depassivation reaction was modeled as an electron capture process given by the capture rate

$$c = c_0 * R_{Auger}, \quad (7.1)$$

where R_{Auger} is the Auger generation rate and c_0 is the fraction of Auger generated hot carriers that are capable of causing damage. c_0 is given as

$$c_0 = \int_{\phi_{Hot}}^{\infty} A * (E - 2 * E_g)^{7/2} * e^{-(E-2*E_g)/kT} dE, \quad (7.2)$$

which is integrated over hot carrier energies for the probability distribution of Auger generation given in (4.1) [63]. The emission rate is given as

$$e = e_0 * \exp\left(-\frac{E_r}{kT}\right) * [H], \quad (7.3)$$

where e_0 is a passivation rate constant, E_r is the activation energy for passivation, and $[H]$ is the hydrogen concentration. The passivation process does not involve hot carriers. The initial passivation levels in polysilicon was assumed to be 50 % along with a maximum trap concentration of $1 \times 10^{19} \text{ cm}^{-3}$.

Figure 7.2 shows the simulated damage evolution within the polysilicon emitter during a high-current stress of $J_E = 21.5 \text{ } \mu\text{A}/\mu\text{m}^2$ and $V_{CB} = 0 \text{ V}$. As expected in [6], passivation levels do decrease near the polysilicon/silicon interface and increase near the metal contact with increasing stress time. To support this process, Figure 7.3 illustrates the diffusion of free hydrogen which mediates passivation. When the device is stressed for 1 μs , the peak in the initial hydrogen concentration profile happens at the polysilicon/silicon boundary and decreases towards the metal contact. With increasing stress time, the free

hydrogen concentration levels initially rise due to hot carrier damage, and later decrease due to the annealing process (7.3), which restores the passivation. Although hydrogen diffuses less in silicon compared to polysilicon [82], with increasing stress time, Figure 7.3 shows that hydrogen does out-diffuse from the silicon. This out-diffusion of hydrogen can also happen via the oxides surrounding the polysilicon, and over long periods of stress, this loss in hydrogen could contribute to an eventual increase in the polysilicon resistance. The diffusion front seen in the passivation level is strongly governed by the reaction rates for the capture and emission processes and does not have the same diffusion speed as hydrogen.

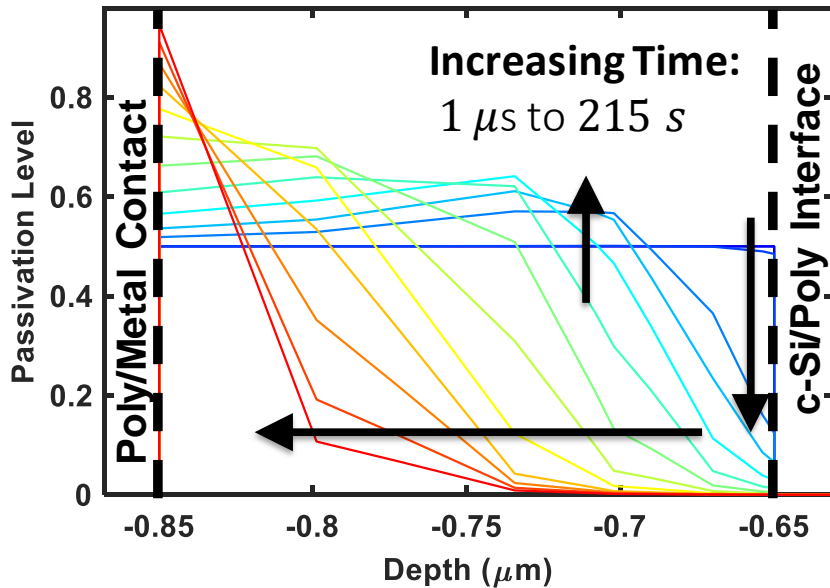


Figure 7.2: Simulated change of passivation level in the polysilicon emitter in response to high-current stress of $J_E = 21.5 \mu\text{A}/\mu\text{m}^2$ and $V_{CB} = 0 \text{ V}$. Blue to red color indicate increasing stress time from $1 \mu\text{s}$ to 215 s .

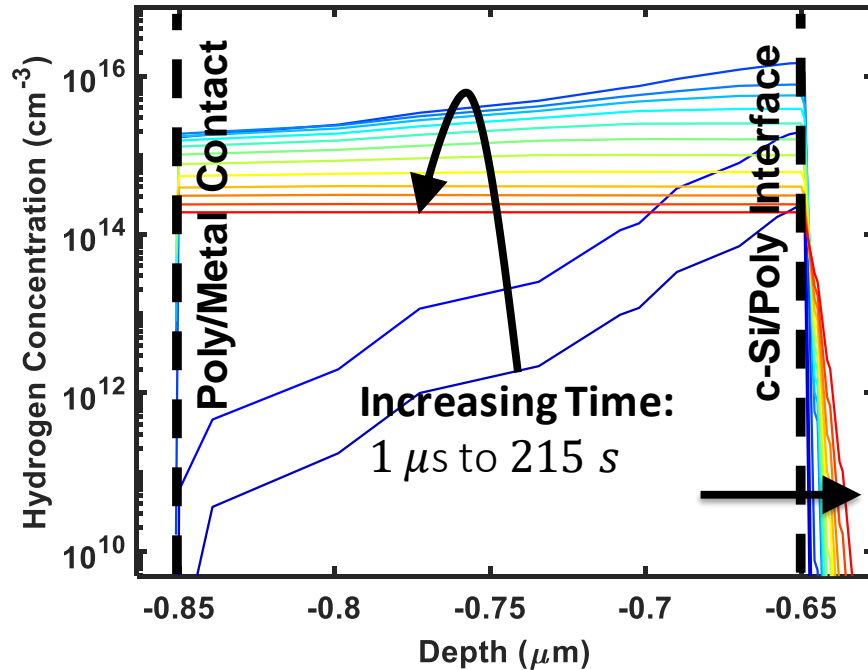


Figure 7.3: Simulated hydrogen concentration within polysilicon emitter in response to high-current stress of $J_E = 21.5 \mu\text{A}/\mu\text{m}^2$ and $V_{CB} = 0 \text{ V}$. Blue to red color indicate increasing stress time from $1 \mu\text{s}$ to 215 s .

7.4 Capturing Electrical Response to Polysilicon Degradation

To simulate the cumulative effects of the spatial passivation information in polysilicon, a mobility degradation model is implemented as a function of passivation, following the analysis in [6]. Mobilities in polysilicon are affected by doping, grain boundary passivation, and grain size. While plenty of quantitative literature exists on doping and grain size, there is currently only qualitative literature on grain boundary passivation. De-passivated grain boundaries in polysilicon increase the barrier height for carriers, and are known to decrease the majority carrier mobilities and increase the recombination velocities of minority carriers as shown in Figure 7.4. But, when polysilicon is highly doped, despite high levels of defects in polysilicon, barrier heights at grain

boundaries can be minimized, which helps maintain high mobilities for majority carriers. Under high doping conditions, increasing passivation in polysilicon is known to reduce the resistivity by 1000x, which is largely driven by the changes in majority mobility [78]. However, there exists very little literature on the effects of passivation on the differences between majority and minority carrier mobilities.

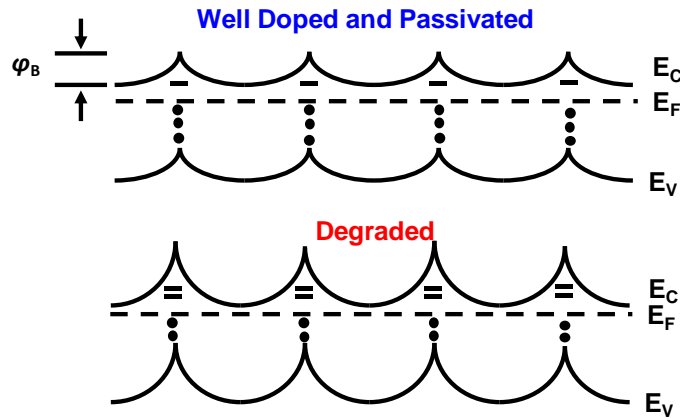


Figure 7.4: Reduction of potential barriers at grain boundaries by passivation and doping.

To capture the qualitative behavior of the CGE and decreased resistance changes from Figure 6.1, in this work, the minority and majority mobilities are scaled logarithmically and independently of each other in response to changes in passivation. The effects of mobility changes in response to passivation levels are shown in Figure 7.5. With these changes, the simulated electrical response in Figure 7.6. demonstrates both CGE and emitter resistance decrease as seen in Figure 6.1. Presently these simulations are uncalibrated to data. Once accurate degradation data at high injection is gathered, the temperature dependencies of the model including the Auger energy distribution, diffusion constant of hydrogen, and activation energies of the forward and reverse reactions can be tuned.

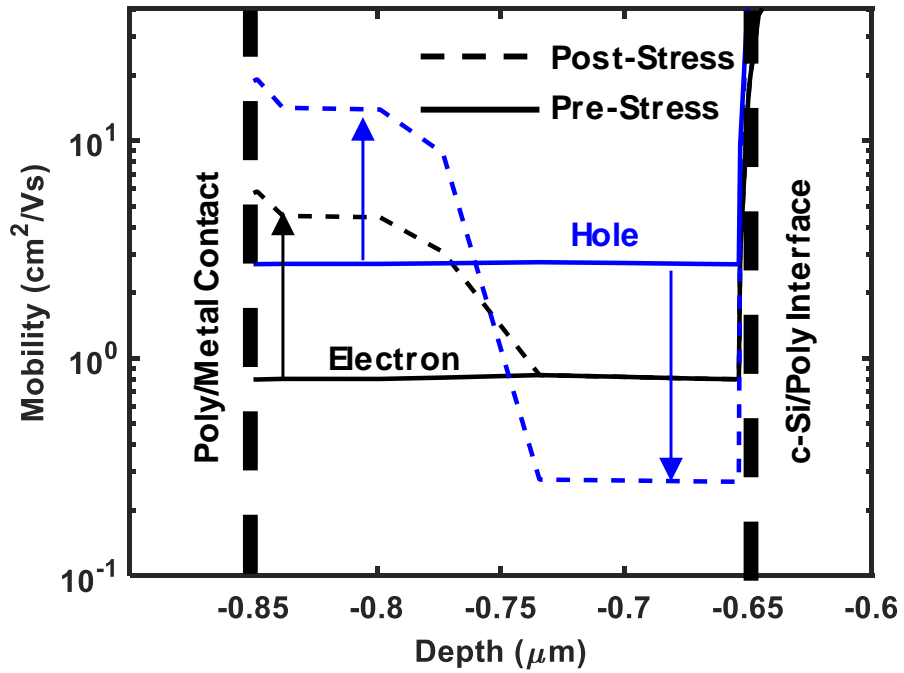


Figure 7.5: Changes in electron and hole mobilities using the spatial mobility degradation model for the condition in Figure 7.2 after a stress period of 100 s.

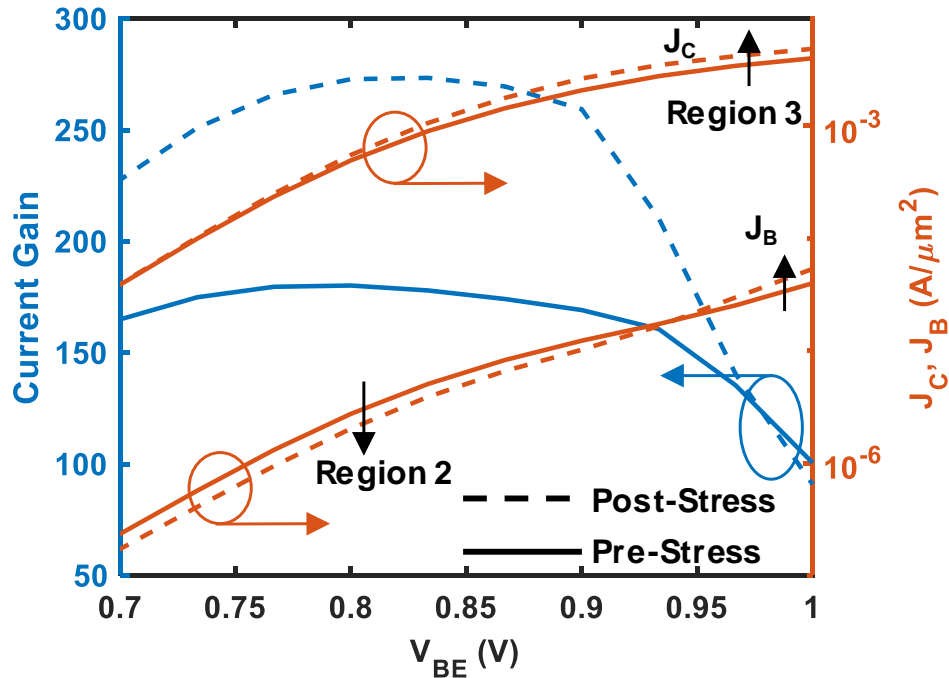


Figure 7.6: Simulated Gummel characteristics using the spatial mobility degradation model for the condition in Figure 7.2 after a stress period of 100 s.

7.5 High Temperature Measurements

The experiments in this work were done on packaged Kelvin structures to accurately capture the high injection effects described in the previous sections. The device studied in this work is a first-generation NPN SiGe HBT with a BV_{CEO}/BV_{CBO} of 3 V / 13 V, and a f_T/f_{max} of 60.5 GHz / 73.4 GHz. All devices have an emitter area of $0.3 \times 6.4 \mu\text{m}^2$ and were stressed at $V_{CB} = 0$ V and $J_C = 21.5 \text{ mA}/\mu\text{m}^2$. The packaged devices were measured inside an oven made by Delta Design from 300 K to 573 K. The goal of these measurements is to not only obtain data to fit simulations, but also explore the limits of Auger hot carrier damage to polysilicon and oxide interfaces. The measurements in a high breakdown SiGe HBT platform already showed that high-current stress causes base leakage currents to increase with temperature up to 573 K [86]. In addition to the base leakage current, the measurements in this section explore CGE and collector current changes at high and low injections.

To compare between temperatures, base current degradation is typically extracted at a constant collector current density. However, for the high current condition used ($21.5 \times J_C @ f_{T, peak}$) in these devices, temperatures at or above 400 K caused parallel shifts in the collector current at FM and IM operation as shown in Figure 7.7. Such shifts in current have been attributed to the neutralization of boron dopants by diffusing hydrogen atoms that get released from oxide interfaces due to hot carrier damage [88]. Because the active doping from the extrinsic and intrinsic regions of the base decrease, the base potential barrier for injection decreases and allows a higher flow of collector current. These changes in the base doping affect the EB capacitance, base resistance, and can ultimately affect both f_T and f_{max} . These parallel shifts in collector current are detectable even at lower temperatures near 300 K operation as shown by the low injection extraction of collector

current degradation in Figure 7.8. With increasing temperature, the parallel shifts in collector current get worse as explained by the increased Auger hot carrier damage to oxide interfaces and polysilicon, which release hydrogen that neutralize the boron in the intrinsic and extrinsic bases. At higher temperatures, hydrogen not only diffuses further, but there's a higher likelihood for creating the bond between boron and hydrogen, which has an activation energy of 1.1 eV [89]. The work in [88] already provides a model for capturing these effects, which can be important for modeling AC degradation in SiGe HBTs.

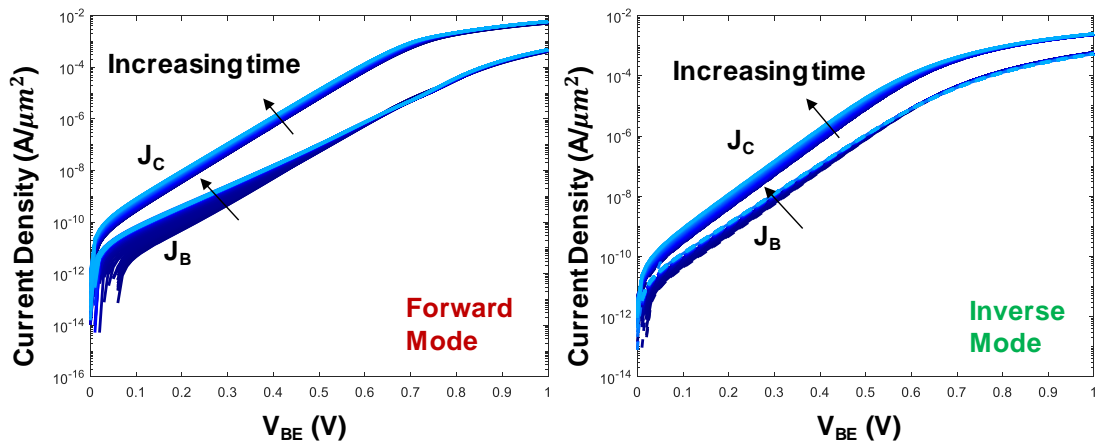


Figure 7.7: Parallel shifts in collector current under forward and inverse mode operation. Indicates boron neutralization.

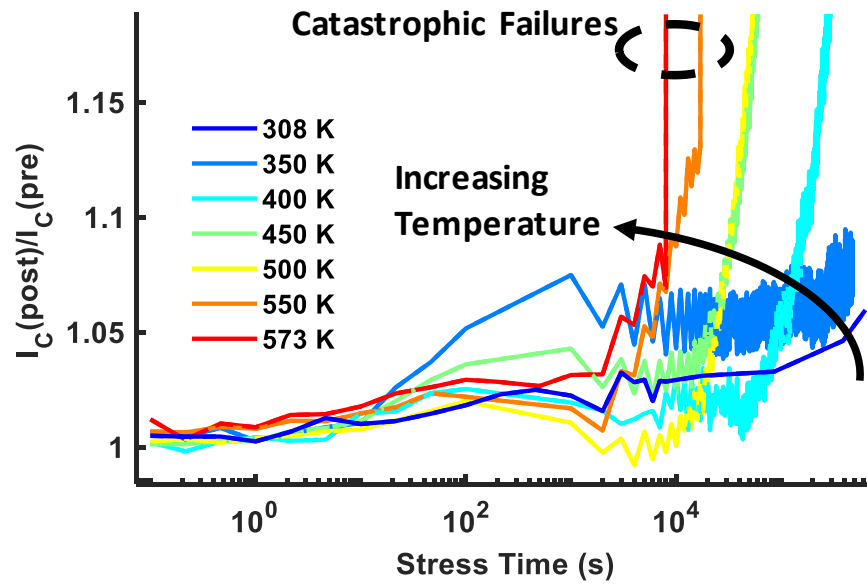


Figure 7.8: Increase in collector current at a fixed V_{BE} corresponding to an initial low injection condition of $J_C = 1 \mu\text{A}/\mu\text{m}^2$. Indicates parallel collector current shifts due to boron neutralization.

As a result of these parallel shifts, base current degradation at low injection is extracted at a fixed V_{BE} as shown in Figure 7.9. Similar to the measurements in [86], base current degradation increases with temperature following the widened energy distribution of Auger hot carriers at high temperatures [4]. This behavior is seen up to 100 s, after which period, the annealing reaction starts to dominate the damage at higher temperatures similar to the observations in [86]. As a result, for extended periods of stress, the higher temperatures do not produce the most oxide interface damage. Following the same reasoning for low injection base current extraction, CGE is also extracted for a fixed V_{BE} at a higher injection level, as shown in Figure 7.9. Similar to the trends in oxide interface damage, CGE also increases initially with stress temperature up to 100 s. Afterwards, the high temperature conditions also show a tapering behavior similar to oxide interface damage. This is likely due to the interaction of parallel current shifts that affect CGE and the annealing of polysilicon itself. The complex forward and reverse reaction processes for

the polysilicon passivation processes develop more variation at high temperatures due to the rapid diffusion and exchange of hydrogen.

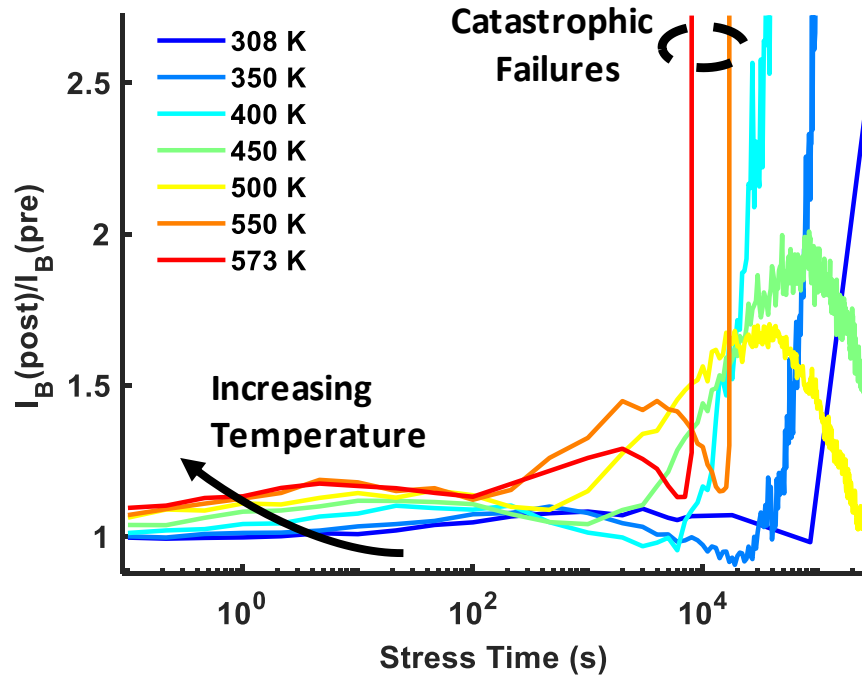


Figure 7.9: Increase in base current degradation at a fixed V_{BE} corresponding to an initial low injection condition of $J_C = 1 \mu\text{A}/\mu\text{m}^2$. Indicates oxide interface damage.

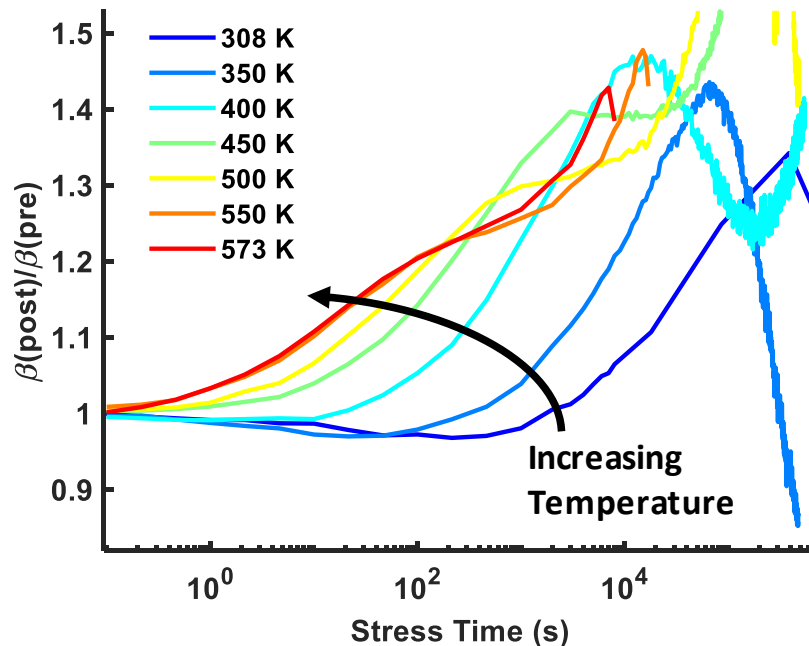


Figure 7.10 Increase in CGE at a fixed V_{BE} corresponding to an initial high injection condition of $J_C = 1 \text{ mA}/\mu\text{m}^2$. Indicates polysilicon minority mobility degradation.

In addition to the parallel current shifts at low injection, Figure 7.11 plots the collector current enhancement (CCE) at high injection. Similar to the positive temperature dependence of base current degradation and CGE, CCE also shows the same trend for the initial ten seconds of stress. Later, the decrease in resistance also saturates due to out-diffusion via crystalline silicon, as illustrated in Figure 7.3, and via oxide. Finally, the out-diffusion of hydrogen causes the polysilicon resistances to increase to more than the initial levels, causing CCE to plummet. The device struggles to maintain the stress currents due to increased polysilicon resistances, and the devices face catastrophic thermal runaway as indicated by the conditions at 573 K and 550 K. Despite having degraded polysilicon resistances, the device stressed at a less aggressive condition of 500 K survived because of the compliance limits set.

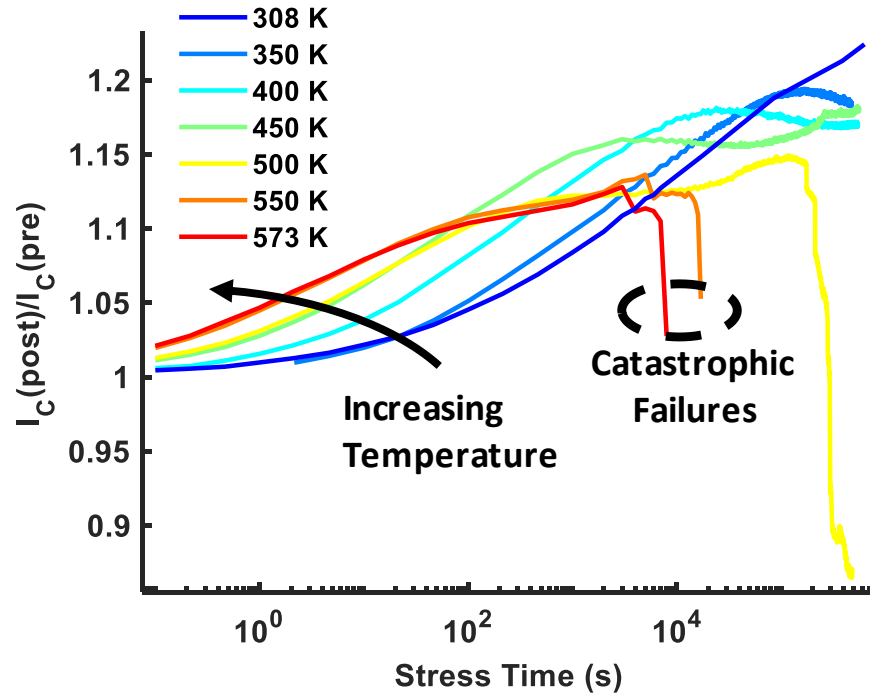


Figure 7.11: Collector current enhancement at a fixed V_{BE} corresponding to an initial high injection condition of $J_C = 1 \text{ mA}/\mu\text{m}^2$. Indicates changes in polysilicon resistance.

7.6 Summary

This work provides a TCAD framework for simulating Auger hot carrier damage to oxide interfaces and polysilicon. Using rate equations for capture and emission processes that affect passivation, the movement of hydrogen in polysilicon is modeled with the temperature dependencies coming from Auger energy distribution, hydrogen diffusion constant, and activation energies for the forward and reverse reactions. This work also demonstrated the difference in speeds for the diffusion of hydrogen and the diffusion of passivation.

To understand the physics of Auger hot carrier damage better and generalize it for polysilicon degradation and oxide interface damage, high current measurements were performed on packaged Kelvin structures to gather clean data at high injection. The

experiments show over the initial 100 s of stress that oxide interface damage (base current degradation at low injection), polysilicon minority mobility degradation (CGE), and polysilicon majority mobility changes (CCE) are strongly governed by temperature, which affects the Auger energy distribution and damage creation. After this initial period, a number of complex processes affect damage creation including 1) annealing, which restores passivation at oxide interfaces and polysilicon with the increase in hydrogen concentration; 2) parallel current shifts due to boron compensation or neutralization by hydrogen atoms that get released during hot carrier damage to oxide interfaces and polysilicon, 3) out-diffusion of hydrogen at elevated temperatures due to enhanced diffusion that affects the overall resistances in polysilicon, and even causes catastrophic failures.

To model the measured changes, a universal model must account for shifts in collector and base currents at low and high injections. The well-studied non-ideal base current degradation due to oxide interface damage cannot fully explain the degradation seen in devices and circuits. Sophisticated models need to be implemented to fully account for changes in the ideal base current (CGE); changes in EB capacitance and intrinsic base resistance (parallel shifts in collector current); and resistance changes in the extrinsic polysilicon resistance at the base and emitter (CCE). The key to capturing all these effects is to track hydrogen concentration. These refinements in reliability models would allow for a better prediction of both AC and DC degradation of devices and circuits in the future.

CHAPTER 8

EMITTER-BASE PROFILE OPTIMIZATION OF SIGE HBTS FOR IMPROVED THERMAL STABILITY AND FREQUENCY RESPONSE AT LOW-BIAS CURRENTS

This work investigates profile designs for improving the reliability of power cells in PAs. These power cells often face thermal runaway mechanisms under high power operation and are susceptible to both “soft” and “hard” damage. To alleviate these problems, different vertical profile designs are leveraged with optimized emitter-base (EB) junctions targeting both constant current gain (β) across temperature and broadened f_T/f_{\max} curves for improved large-signal linearity. This work explicitly examines achieving a temperature-independent β via profile design in SiGe HBTs, and explores the limitations using triangular and ledge-based Ge profiles at the EB junction. The effects of base width and the EB junction separation length are also investigated for reduced parasitic capacitance and improved frequency response at low-bias currents. This work presents the underlying theory, along with the measured results for the two optimization targets, both of which should aid in designing circuits with better linearity and stability across bias and temperature corners. The analysis in this work resulted in a publication [7].

8.1 Motivation and Background on Electro-Thermal Feedback

In the last two decades, silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) have emerged as a leading technology for a diverse range of applications including high-speed analog, mixed-signal, and mm-wave circuits [10]. As SiGe HBTs continue to

see improvements from vertical and lateral scaling, separate technology variants have been developed that target specific speed (5 to 500 GHz peak f_T) and breakdown (1.5 – 55 V) requirements [15], [86]. These wide-ranging SiGe platforms offer a low-cost solution for building highly integrated systems comprising multiple components such as low noise amplifiers, phase shifters, PAs, and digital circuitry on the same chip.

In order to ease the design of stable and reliable circuits, having devices that change linearly with environmental conditions, such as temperature, is essential. For many applications, the ideal device would have temperature-invariant parameters such as transconductance, current gain, output resistance and breakdown voltages. Engineering practical devices with such temperature-invariant performance poses great difficulty, however, and temperature variation must be overcome and compensated for at the circuit level, with added design overhead. Although circuits using negative feedback can compensate for minor variations in temperature, robustness of operational amplifiers, reference voltages and currents often rely on the precision of the matching between devices as a function of temperature.

As temperature changes due to self-heating, β and temperature can vary across a power cell, creating unequal current distributions as shown in Figure 8.1 and Figure 8.2. Under constant collector current bias, the changing β will cause the base current to drift and thereby vary the resistive voltage drops across the extrinsic base [90]. This can pose problems, especially in base-ballasted power cells [91]–[94]. Ultimately, because of the temperature dependence of β , there is current “hogging” by the transistors in the center of a power cell array. As a result of the imbalance in current loads, the central transistors can prematurely face “hard” damage due to thermal runaway mechanisms and bias instabilities

[19], [95]. Moreover, even if the devices withstand the unequal current load, as shown in Chapter 6 [6], self-heating due to high current and high power operation is expected to cause Auger hot carrier damage to devices facing the most load. Unevenly degraded transistors in a power cell array could develop mismatches in the series resistances and β , which would in turn limit the ability of the transistors to maintain even currents with stress time. Decreasing β with temperature has been shown to distort linearity in PAs due to electrothermal feedback [96]. To compensate for the temperature dependence of β , [96] integrated a thermal sensor to apply the optimal bias to maintain stable currents across transistors. However, in the presence of “soft” damage, unequal aging of transistors in an array could still pose problems for maintaining high linearity. In all of these scenarios, device-level temperature compensation can enable higher tolerance for temperature mismatch between adjacent devices, enabling circuits to track wider temperature corners, and maintain improved circuit ruggedness, both of which make meeting design targets easier.

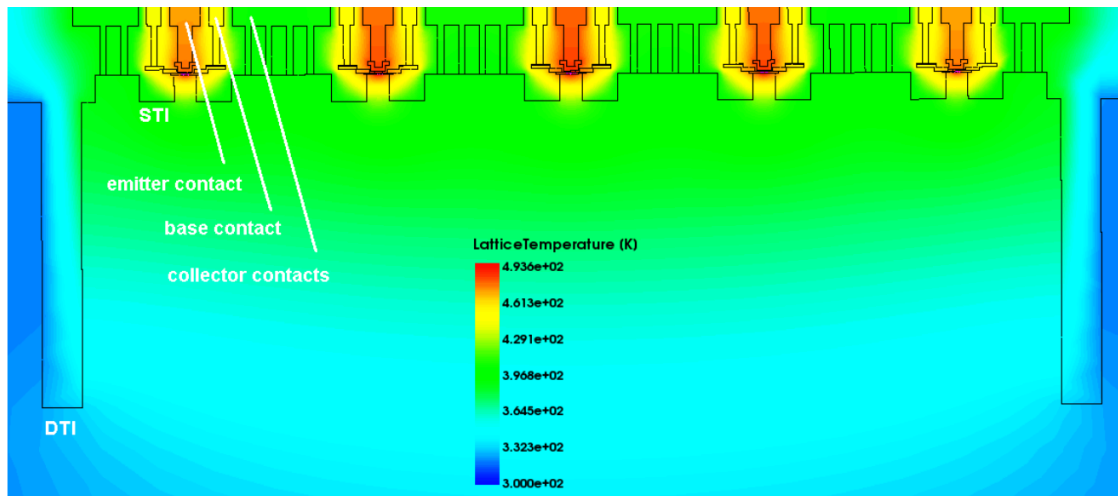


Figure 8.1: Heat distribution in a multi-transistor array. (after [95])

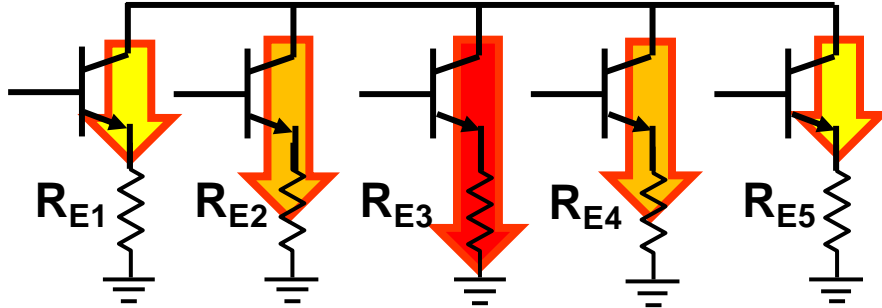


Figure 8.2: Unequal current distribution in a multi-transistor array following the heat distribution in Figure 8.1. Length and color of arrows indicate the magnitude of the current. (after [1])

Previous works on over-temperature operation of SiGe HBTs have looked at the improvements offered by Ge over pure Si BJTs, as well as the behavior of different Ge profiles [97]–[100]. Explicit attempt to create a profile offering temperature-independent β over a wide range of currents was shown in [101]. The present work takes multiple intuitive approaches for designing such devices without actually simulating or measuring large-signal linearity, which will be done in a future work. Multiple profiles targeting emitter-base (EB) junction optimization have been designed and fabricated with the following goals: 1) flattening response of β over temperature, and 2) improving low collector current density (J_C) response of f_T/f_{max} by reducing EB capacitance. The latter approach offers several benefits including broadened f_T/f_{max} curves w.r.t J_C , lower shot noise at reduced J_C , larger bandwidth matching due to reduced parasitics, and also reduced power consumption and thermal dissipation due to the ability to operate at backed-off current levels, which could help reduce Auger hot carrier damage and benefit high-speed digital circuits. Broadened f_T/f_{max} curves can help improve the power added efficiency under large-signal operation [102]. The considerations of the above two design approaches will be analyzed after a brief overview of the dominant physical mechanisms.

8.2 Temperature-Invariant Current Gain Physics

In a Si BJT, the ratio of doping across the EB junction (emitter is always doped higher than the base) drives the ratio of bandgap narrowing, which ultimately leads to temperature dependence (enhancement) of β . In contrast, a SiGe HBT deals with competing mechanisms that enhance (bandgap narrowing) and degrade (bandgap grading) the current gain over temperature. The current gain in a SiGe HBT relative to a Si BJT as a function of temperature can be expressed as

$$\beta_{SiGe}(T) = \tilde{\gamma}\tilde{\eta}\beta_{Si} \frac{\frac{\Delta E_{g,Ge(grade)}}{kT} \exp\left(\frac{\Delta E_{g,Ge(0)} - \Delta E_{g,EB}^{app}}{kT}\right)}{1 - \exp\left(\frac{-\Delta E_{g,Ge(grade)}}{kT}\right)}, \quad (8.1)$$

where $\tilde{\gamma}$ and $\tilde{\eta}$ are the ratios of effective density of states and minority carrier diffusivities across the EB junction, $\Delta E_{g,Ge(grade)}$ is the grading in the base, $\Delta E_{g,Ge(0)}$ is the valence band offset at the EB junction, and $\Delta E_{g,EB}^{app}$ is the difference in the apparent bandgap narrowing between emitter and base [97]. Assuming that $\Delta E_{g,Ge(grade)} \gg kT$ and that the exponential terms are dominant, constant β is achieved when $\Delta E_{g,EB}^{app}$ cancels $\Delta E_{g,Ge(0)}$. When this happens, β is roughly equivalent to the ratio of doping across the EB junction. In vertically scaled technologies, the base is often doped aggressively to minimize resistance. This leads to a poor doping ratio, however, making it very difficult to achieve a high β . As the doping ratio increases, $\Delta E_{g,EB}^{app}$ also increases, and this necessitates higher $\Delta E_{g,Ge(0)}$.

The challenge with designing and fabricating such a profile lies in accurately estimating the effective $\Delta E_{g,EB}^{app}$ while also compensating it with the necessary Ge percentage at the

EB junction. Even with such compensation, β will vary with J_C , which behavior can be either enhanced or degraded at different temperatures as shown by the TCAD simulations in Figure 8.3. For a well-engineered device, the collector profile should contribute negligibly to the temperature dependence of β . Figure 8.4 shows the simulated temperature coefficient of β for a fixed doping profile, as $\Delta E_{g,Ge(0)}$ is varied. An optimum Ge percentage at the EB junction minimizes the change in β as predicted by the above physics. Once the doping profile has been locked, the primary design parameters for achieving temperature-invariant β are the shape and percentage of Ge at the EB junction.

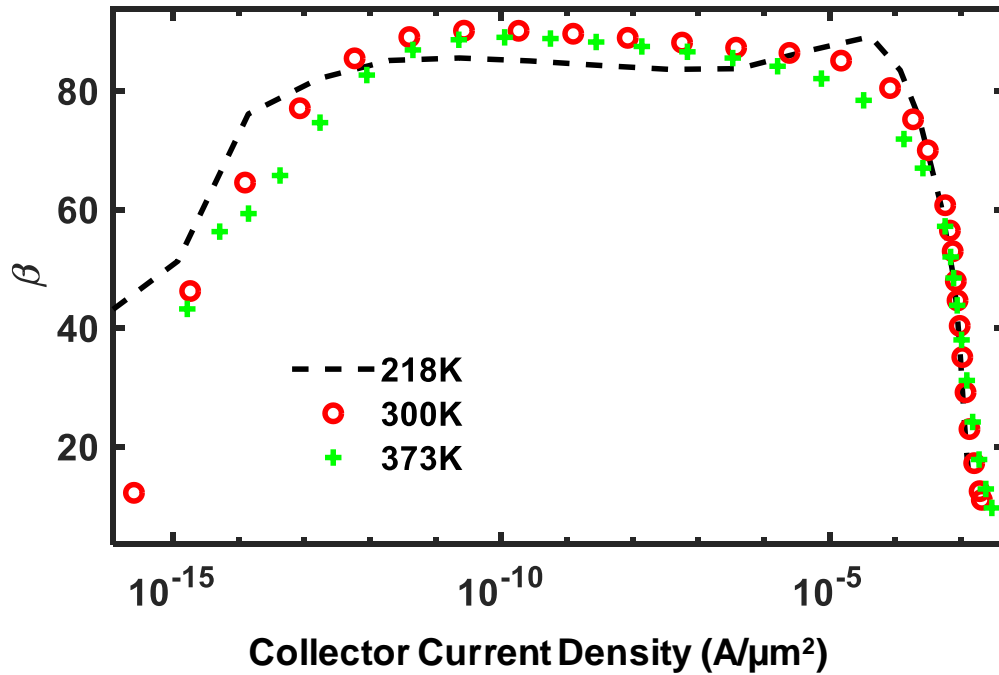


Figure 8.3: TCAD simulations of the temperature dependence of β for different collector current densities.

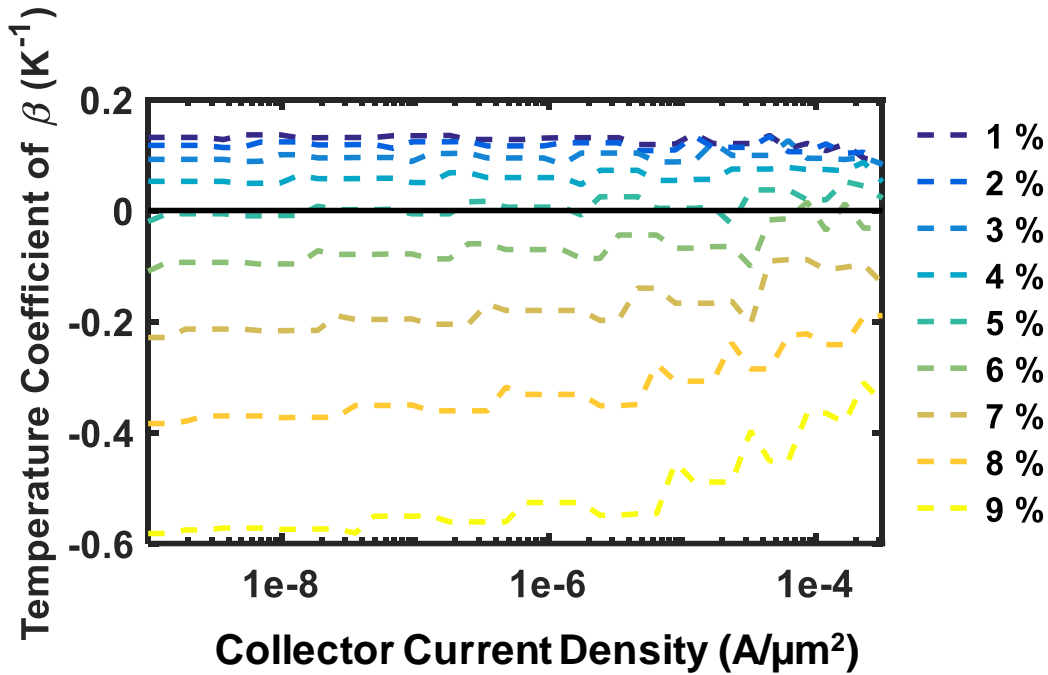


Figure 8.4: TCAD-simulated temperature coefficient of β for different collector current densities as EB Ge percentage is varied for a fixed doping profile.

8.3 Methods for Improving Large-Signal Performance

Simulating large-signal linearity at the device level using TCAD can be very time consuming, and compact model representations of a device are necessary to quickly optimize a device profile for linearity. Using a Volterra series approach, the overall nonlinearity of the device is dominated by the avalanche multiplication current, CB capacitance (C_{CB}), and EB capacitance (C_{EB}) distortions [103]. Intuitively, a more linear device can be built by decreasing the EB and CB doping intercepts by segregating the n- and p-type dopants, effectively reducing the junction capacitances as seen in Figure 8.5. Additionally, the nonlinearity associated with avalanche multiplication can also be manipulated with the collector profile shape.

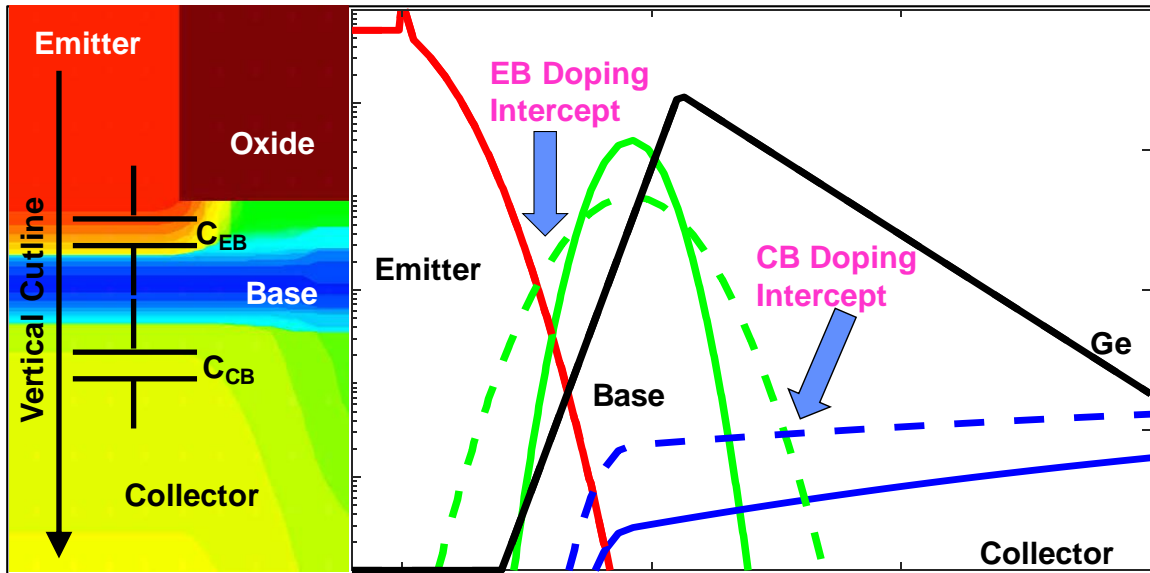


Figure 8.5: (a) Reduction of EB and CB junction doping for reduced capacitance. Reduction of base width and increased base doping peak for improved speed.

Although collector implants can be selectively enabled for additional performance, the following optimizations are worth considering: improving linearity without sacrificing much speed, improving low J_C speed, and improving the speed over wider current and voltage ranges. For all of these optimizations, reducing the parasitic capacitances C_{EB} and C_{CB} is vital. Well-segregated emitter and base dopants could initially help reduce C_{EB} and intrinsic base resistance for improved f_{max} . However, additional vertical optimization to minimize base transit time will be necessary to compensate for the increase in transit time due to lowly doped EB and CB regions as shown in [10]. In order to improve the voltage handling and reduce the C_{CB} nonlinearity, a superjunction can be built into the collector as illustrated in [104]. Superjunctions can be beneficial as they distribute the electric field in the CB junction and minimize avalanche multiplication without sacrificing much speed at high V_{CB} . With these optimizations, devices with better large-signal performance can be achieved for designing more power efficient and linear amplifiers.

8.4 Emitter-Base Optimized Device Profiles

Profile experiments were conducted by first building a control profile that approximated the GlobalFoundries 5PAE SiGe HBT, which has a BV_{CEO} of 6 V and f_T/f_{max} of 35/80 GHz [105]. Then, six other profiles were incrementally designed to explore optimization of temperature-invariant β and low J_C speed improvement via C_{EB} optimization. To begin, a control profile (N2) was created through improvements to the base profile of N1, which has been previously presented in [104]. N2 has a higher base doping and smaller base width, resulting in significantly decreased EB and CB doping intercepts and parasitics for improved f_T and f_{max} , as seen in Figure 8.6. N3-N7 all make incremental changes to N2 to explore the tradeoff space in speed and β variance when moving from N1 to N2. Profiles N3-N7 make use of Ge and EB ledges which consist of constantly doped regions or constantly held Ge percentages as illustrated in Figure 8.8 (a) and Figure 8.8 (b). N3, N4, and N6 each use variations of a Ge ledge for β variance. N4, N5, and N6 use variations of an EB ledge for reduced C_{EB} . N7 takes the EB profile of N5 and introduces a superjunction structure for improved breakdown performance. A summary of each profile variant is found in Table 8.1.

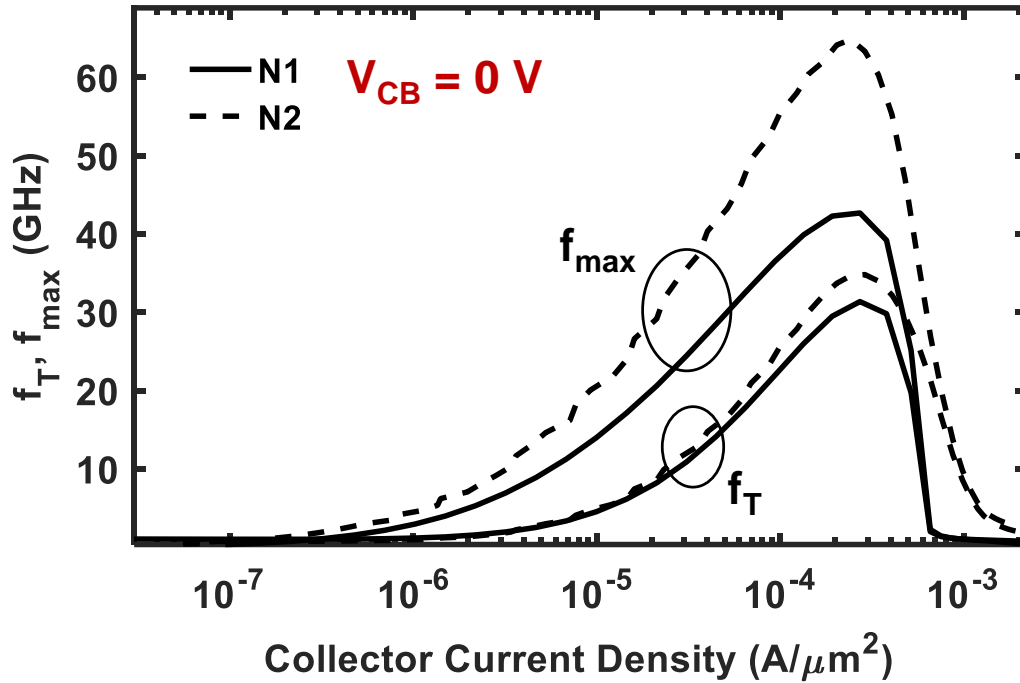


Figure 8.6: Measured f_T/f_{max} improvement from the control profile N1 to the optimized N2 profile with reduced EB and CB capacitance, reduced base width and increased base doping.

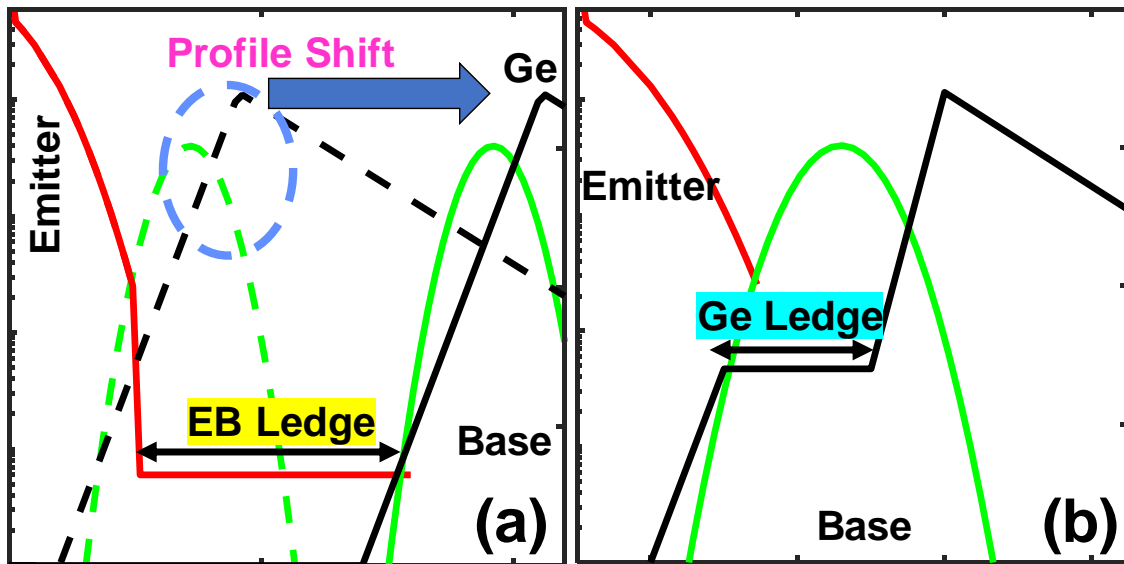


Figure 8.7: (a) Constantly doped EB ledge for increased EB separation, reduced doping intercept and reduced C_{EB} . (b) Ge ledge at the EB junction consisting of a constant Ge percentage.

Table 8.1: Profile Differences of Measured Devices

Device	Ge Type	Ge Ledge Width	EB Ledge Thickness	SJ Collector	EB Intercept	CB Intercept
N1	Tri.	-	-	-	$2 \times 10^{18} \text{ cm}^{-3}$	$6 \times 10^{16} \text{ cm}^{-3}$
N2	Tri.	-	-	-	$1 \times 10^{17} \text{ cm}^{-3}$	$1 \times 10^{16} \text{ cm}^{-3}$
N3	Ledge	10 nm	-	-	$1 \times 10^{17} \text{ cm}^{-3}$	$1 \times 10^{16} \text{ cm}^{-3}$
N4	Ledge	15 nm	30 nm	-	$1 \times 10^{17} \text{ cm}^{-3}$	$1 \times 10^{16} \text{ cm}^{-3}$
N5	Tri	-	27.5 nm	-	$1 \times 10^{17} \text{ cm}^{-3}$	$1 \times 10^{16} \text{ cm}^{-3}$
N6	Ledge	10 nm	7.5 nm	-	$1 \times 10^{17} \text{ cm}^{-3}$	$1 \times 10^{16} \text{ cm}^{-3}$
N7	Tri	-	27.5 nm	Yes	$1 \times 10^{17} \text{ cm}^{-3}$	$6 \times 10^{16} \text{ cm}^{-3}$

8.5 Measurements and Discussion

This section presents results on profiles that were individually optimized for β and speed, and some hybrid profiles that try to incorporate both. DC and AC measurements were performed on profiles N2 to N7, using a device with an emitter area of $0.8 \times 10 \mu\text{m}^2$. The optimizations for β and speed built in these profiles represent first iterations and may not necessarily be optimal, as the base profile significantly changed from N1, which served as the starting point for these designs. Nonetheless, the following results can offer valuable insights for designing improved devices.

Since device breakdown is the positive feedback interplay between avalanche multiplication in the collector and the current gain from the EB junction, improved breakdown can only come at the cost of either a reduced β or speed. Figure 8.8 shows the increase in BV_{CEO} from the new optimized control profile compared to the other profiles. The β -optimized profiles surprisingly see a boost in BV_{CEO} , possibly due to insufficient Ge

percentage at the EB junction. As all the EB optimized profiles utilize a constantly doped EB ledge with varying lengths, getting the correct amount of Ge for each profile was challenging, and this resulted in diminished β as shown in Figure 8.9, but this can be easily corrected in future experiments. As expected, the profile with both β optimization and superjunction collector shows the highest BV_{CEO} .

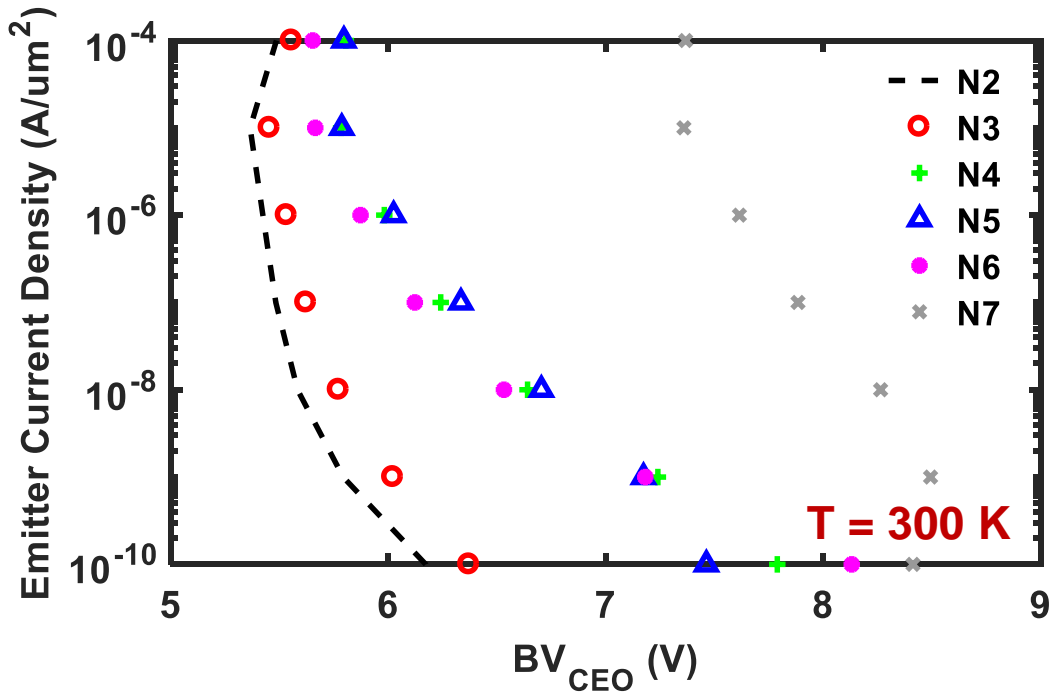


Figure 8.8: Measured and extracted BV_{CEO} for EB optimized profiles from the base current reversal point at different fixed emitter current density inputs.

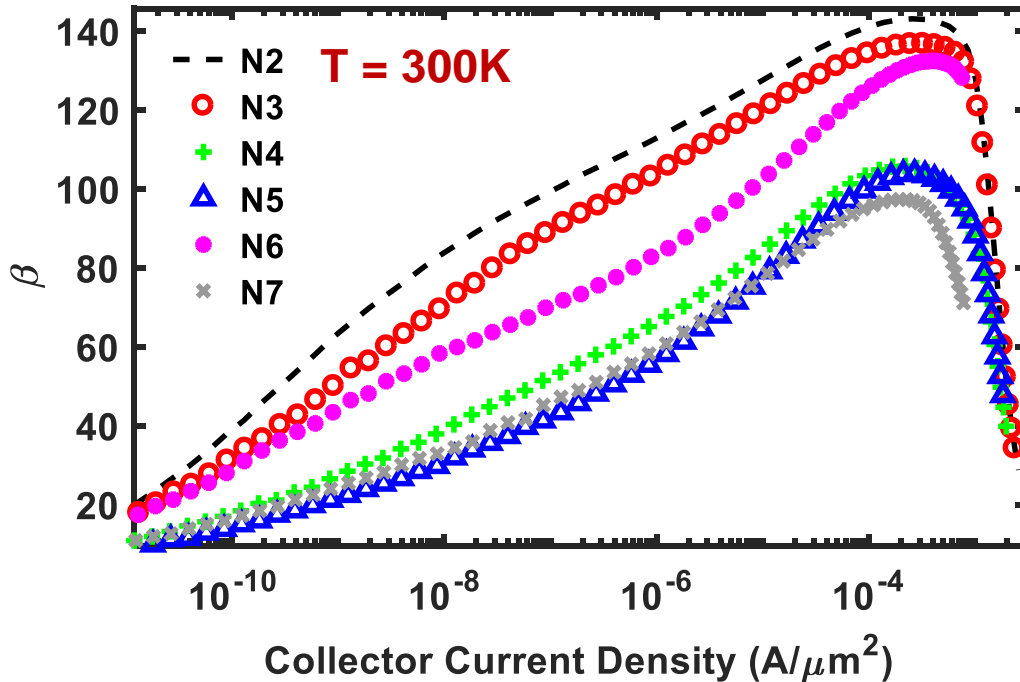


Figure 8.9: Measured β at $T = 300$ K for the different profiles. β -optimized profiles consistently show reduced β .

The temperature coefficient of β (change in β w.r.t temperature) extracted with a linear fit over temperatures points from 300 K to 400 K, was measured for the different profiles, and is shown in Figure 8.10. The optimized control profile shows the largest temperature dependence, especially near the peak f_T current density. In contrast to the simulations in Figure 8.4, measured β is seemingly able to only achieve temperature independence at a singular current density. Profiles with the Ge ledge and Ge triangle show the most improvement in the temperature coefficient over N2, and almost perform identically, except for the slight improvement in β extracted at $J_C = 1 \mu\text{A}/\mu\text{m}^2$ for the ledge profile, as shown in Figure 8.11. This confirms that EB Ge percentage, which is common for the two profiles, is the most important parameter for achieving temperature independence. The other β -optimized profiles fall functionally in between the triangular β profile and the control profile.

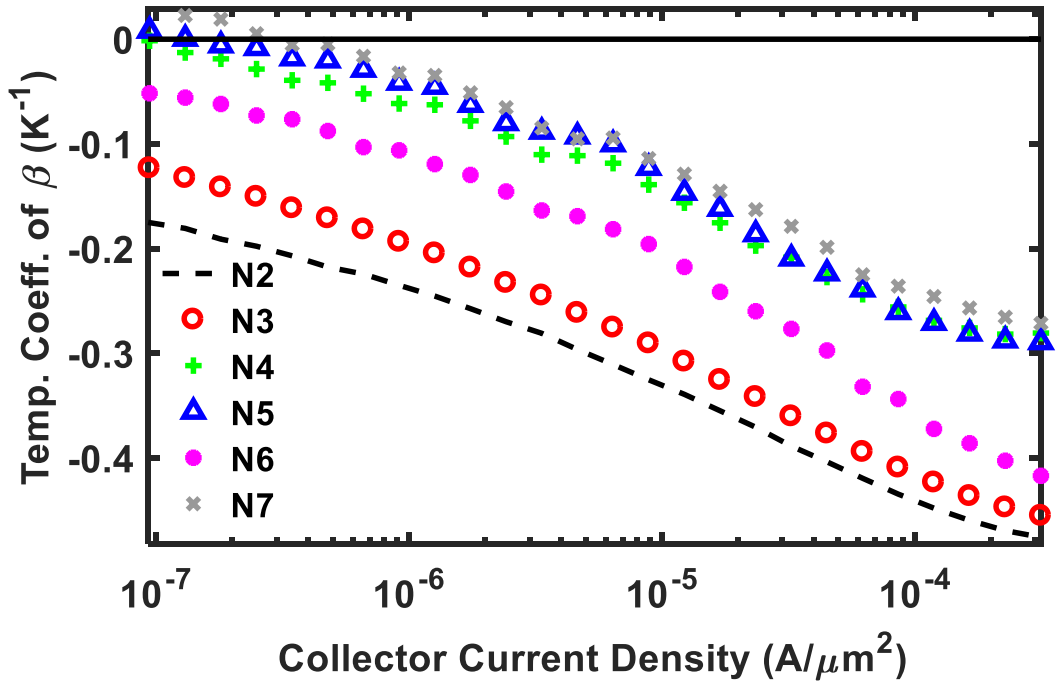


Figure 8.10: Measured temperature coefficient of β ($\Delta \beta$ w.r.t temperature) for different profiles versus J_c . Extracted over 300 to 400 K.

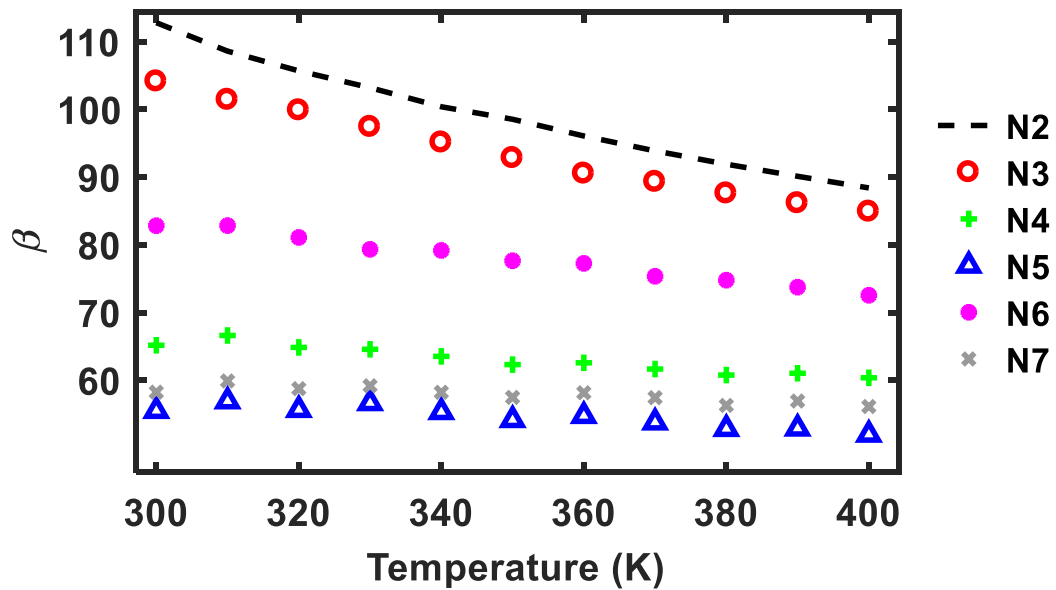


Figure 8.11: Measured current gain of different profiles extracted at $J_c = 1 \mu\text{A}/\mu\text{m}^2$ for different temperatures.

As some of the β -optimized profiles inherently incorporate additional EB spacing to reduce C_{EB} , they are also good candidates for improving low-bias performance as shown in Figure 8.12. Considering the expected peak current swing on these devices to be 0.4

mA/ μm^2 , profile N7 shows the most improvement in speed directly below this current level. In addition, it has the widest current range for f_{max} improvement, signifying a broadened f_{max} curve, which can potentially help in improving linearity across current. The $f_{\text{T}}/f_{\text{max}}$ curves measured in Figure 8.13 for $V_{\text{CB}} = 4 \text{ V}$ highlight the improvements offered by a superjunction collector to go along with EB spacing and β optimizations. Despite a worse peak f_{T} performance, this profile has the highest $f_{\text{max}} \times \text{BV}_{\text{CEO}}$ FoM across V_{CB} as shown in Figure 8.14. This is an improvement over the previously designed profiles, which performed poorly at low V_{CB} [104]. A summary of important FoMs for each profile is given in Table 8.2. Triangular Ge profiles (N5 and N7) see the most improvement in f_{max} at low J_{C} . Surprisingly, despite having an earlier roll-off in current, N7 shows the second highest $J_{\text{C}} (\text{Peak } f_{\text{T}}) \times \text{BV}_{\text{CEO}}$ FoM. The Ge ledge profiles are not necessarily optimally shaped for speed and similarly suffer significant peak f_{T} degradation. Even when additional collector doping is added, as in the case of N6, the low current f_{max} performance is not sufficiently improved over a wide current range, as seen in Figure 8.12.

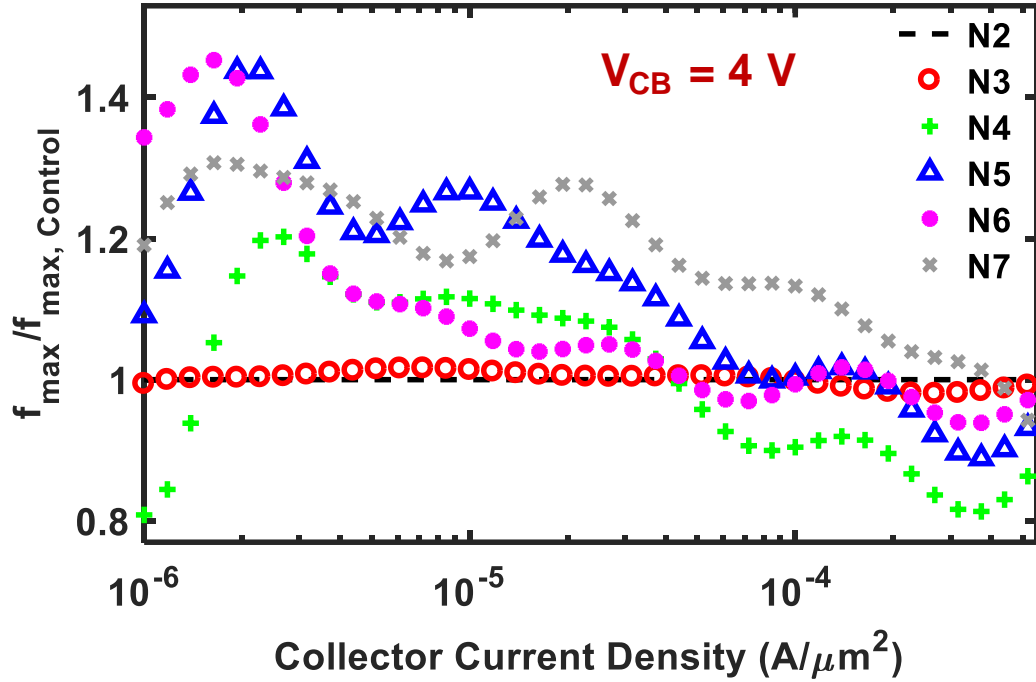


Figure 8.12: Measured improvement in f_{\max} over the control profile for $V_{CB} = 4$ V.

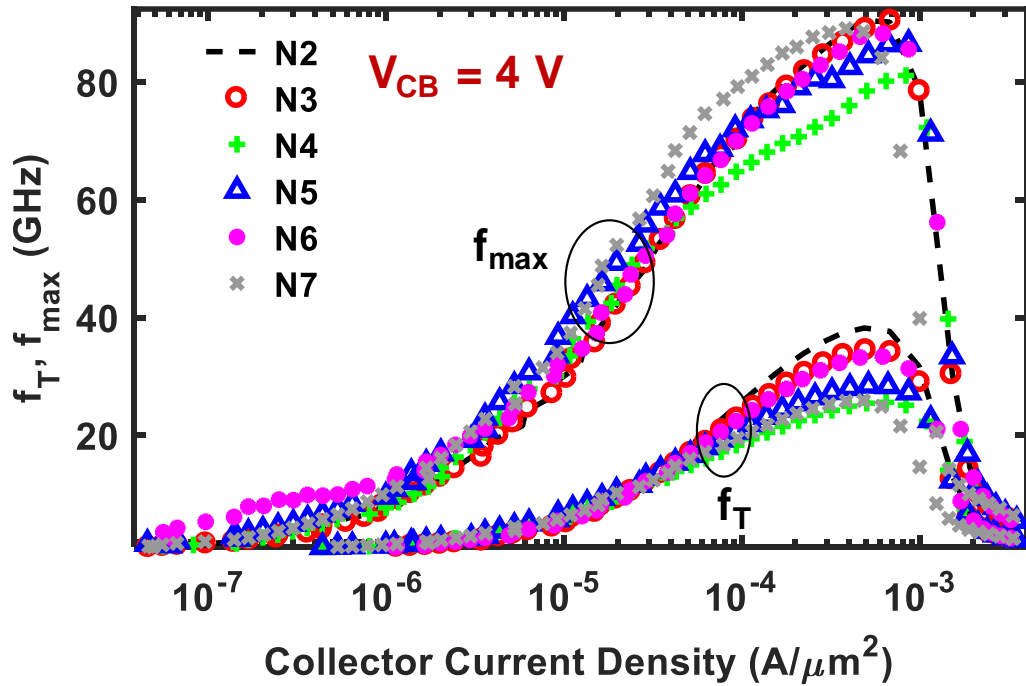


Figure 8.13: Measured f_T and f_{\max} curves for the different profiles for $V_{CB} = 4$ V.

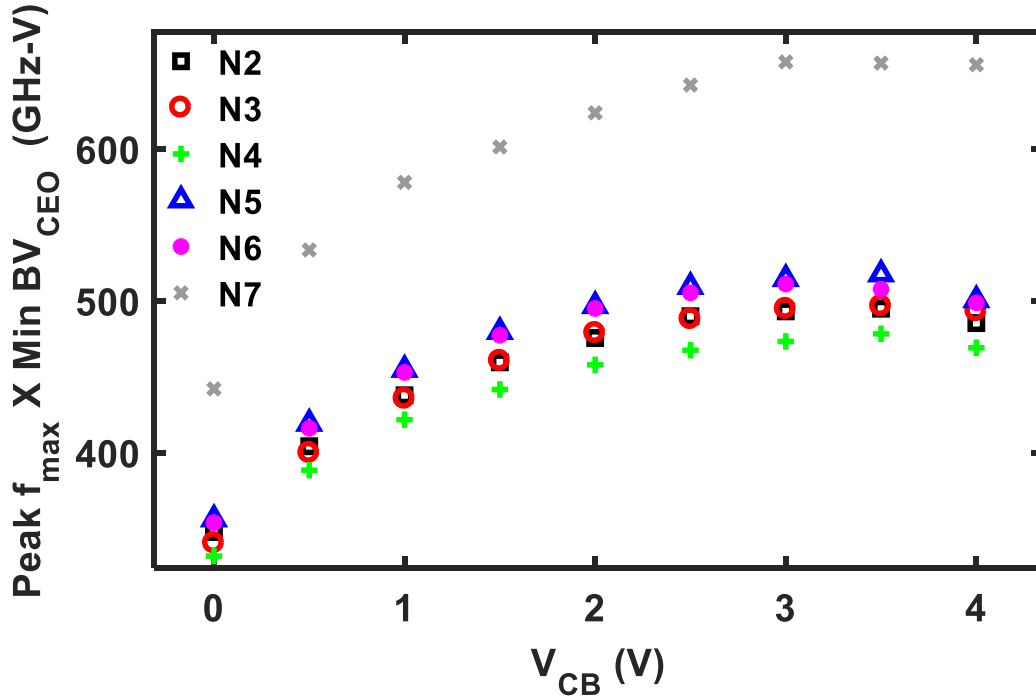


Figure 8.14: Measured Peak $f_{\max} \times BV_{\text{CEO}}$ FoM for the different profiles for $V_{\text{CB}} = 4$ V.

Table 8.2: Device Performance FoMs

	N2	N3	N4	N5	N6	N7
$f_{\max}/f_{\max, \text{N2}} @$ $J_{\text{C}} = 20 \mu\text{A}/\mu\text{m}^2$	1x	1x	1.08x	1.16x	1.03x	1.28x
$\Delta\beta/\text{K}$	-0.48	-0.46	-0.28	-0.29	-0.42	-0.27
$J_{\text{C}} (\text{Peak } f_{\text{T}}) \times BV_{\text{CEO}}$ ($\text{mW}/\mu\text{m}^2$)	2.6	2.7	3.7	3.0	3.5	3.6
BV_{CEO} (V)	5.36	5.45	5.78	5.79	5.65	7.36

f_{T}/f_{\max} data for this table was measured at $V_{\text{CB}} = 4$ V.

8.6 Summary

This work investigated profile designs for achieving constant β over temperature and improved low current operation via C_{EB} reduction using intuitive design approaches.

From the measurements, triangular Ge profiles seem to be equally effective as Ge ledge profiles for achieving temperature-invariant β , and are preferred over the Ge ledge profiles, since they do not have an impact on peak f_T/f_{max} . In contrast to the simulations, which showed a near-zero slope of temperature coefficient of β with respect to current density, temperature invariance in measurement was only achievable at narrow ranges of current density. Nonetheless, optimized profiles in this work demonstrate a 0.21 K^{-1} improvement over control in temperature coefficient of β near peak f_T current density. This represents a 43.8% improvement. Additional gains can be obtained in the next iteration with a tighter control over the optimal EB Ge percentage.

Reduction of EB and CB capacitances offered improvements in f_{max} at low currents for almost all the profiles in addition to the reduction of the base transit time in profile N2. This helped broaden the f_T/f_{max} curves over a wider current range. Profile N7 shows a 2 V improvement in BV_{CEO} over the control, while offering the β optimizations and similar peak f_{max} at a 45% lower current density, which is very desirable from a power perspective. The success of the hybrid profile employing superjunction and β optimization shows promise that better temperature stability and large-signal performance can be simultaneously incorporated within devices for robust and efficient PA designs.

From a reliability perspective, these results are promising for PA power cells as thermal runaway mechanisms will be minimized due to reduced power requirements. Because of more equally distributed currents, linearity of a power cell can be well-preserved. Even if the individual transistors were to undergo hot carrier damage, because of equal current distributions, the devices would degrade more equally, again preserving cell linearity.

CHAPTER 9

ON THE RELIABILITY AND INCREASED VARIABILITY OF SiGe HBTs UNDER CRYOGENIC TEMPERATURE OPERATION

This work presents the first measurements of SiGe HBT reliability at cryogenic temperatures (25 K – 300 K). With the preliminary findings from cryogenic reliability, the electrical variability is identified to be a more serious problem at low temperatures. This work also presents the first measurements of variability in currents due to cryogenic temperature operation, for a Si diode and three different SiGe HBT platform nodes. Irrespective of dopant freeze-out, statistical variance of minority carrier injection is shown to fundamentally increase at low temperatures and is confirmed with TCAD simulations. Process variation, impact-ionization from applied electric fields, and the Ge profile are determined to be the main sources for variability in SiGe HBTs at low temperatures. The findings in this work have direct implications for the design of integrated circuits employing cryogenically-optimized SiGe HBTs for quantum computing and space applications. The results from this study are under peer review for publication in IEEE TED.

9.1 Motivation for Cryogenic Studies in SiGe HBTs

Cryogenic temperature operation of SiGe HBTs has been well studied, showing an enhancement to the frequency response, output conductance, current gain and noise performance of a device with cooling [12]. Leveraging these benefits with those of scaling represents a viable pathway for the first THz transistor operation in Si, as suggested in [16],

[106]. The effects of low temperatures on practical circuit applications have also been explored [107]–[111]. Beyond preliminary demonstrations of those potential uses, however, rigorous studies on the reliability or statistical variability of these devices and circuits at low temperatures (below the 218 K reliability studies in Chapters 3 and 5 [3], [5]) are non-existent. Given the rapidly growing interest in quantum computing (QC), integrated circuits (ICs) operating at cryogenic temperatures for qubit readout are essential building blocks [112]. Since these ICs need to demonstrate high fidelity and reliability, designing them first requires understanding the low-temperature limitations of the candidate devices used in circuits. Similarly, space exploration also demands the stability of devices across a wide range of temperatures.

Chapters 3 and 5 showed that mixed-mode stress degradation increases in SiGe HBTs with decreasing temperatures between 218 K to 373 K due to the reduction of phonon scattering. Unlike mixed-mode stress degradation in SiGe HBTs, which enhances the hot carrier damage below 300 K through increased impact-ionization, NBTI in MOSFETs actually has the opposite temperature dependence [38], [44]. The capacitance-voltage measurements of gate voltage shifts through NBTI show that reduction in hydrogen diffusion at low temperatures must reduce interface trap generation. However, even without interface state generation, there is evidence that carrier trapping in the oxide from hot carrier production could severely reduce device performance at low temperatures in MOSFETs [113]. Studies of cryogenic performance degradation following stresses at room temperature have been performed in SiGe HBTs [32]. However, in-situ cryogenic reliability studies at temperatures near the required levels for QC is still lacking, and could help understand the feasibility of SiGe HBTs for these applications.

In addition, several reports on MOSFETs show degradation of device matching with decreasing temperature [114]–[117]. Considering this immediate problem of device mismatch at low temperatures, it is reasonable to evaluate other candidate devices like SiGe HBTs for emerging QC applications. Prior work has already demonstrated the potentiality of SiGe HBTs for temperature sensing and QC readout circuitry at low temperatures [84], [118], [119]. Unlike the research in MOSFETs, the statistical studies on SiGe HBTs have lacked over-temperature measurements [120]–[122]. The following sections explore the challenges of reliability and device-to-device variability in SiGe HBTs for cryogenic applications, and also provides insight into the fundamental mechanisms driving the measured behaviors using TCAD. This is not only important for cryogenic circuit design, but also the optimization of SiGe HBT vertical profiles targeting cryogenic applications.

9.2 Reliability Scaling at Low Temperatures

All measurements in this work were performed in a closed-cycle cryostat made by Advanced Research Systems on packaged devices. To get a preliminary understanding of how hot carrier degradation affects SiGe HBTs at cryogenic temperatures from 25 K to 300 K, a mixed-mode stress condition of $J_E = 100 \mu\text{A}/\mu\text{m}^2$ and $V_{CB} = 1.5 \text{ V}$ is performed on a fourth generation device [123]. Four device samples were gathered for each stress temperature, and Figure 9.1 shows the mean degradation over time in the base current of forward mode Gummel characteristics due to trap generation, at a low injection level of $J_C = 1 \mu\text{A}/\mu\text{m}^2$. While the degradation increases initially with decreasing temperature below 300 K due to increasing scattering lengths, it reaches a peak between 75 K and 125 K. This maximization in base current predicted in [3] is likely driven by the saturation of scattering

lengths of carriers, which drive hot carrier production. This saturation behavior of scattering lengths due to the geometrical limits in the silicon lattice, and the Arrhenius behavior of diffusion constant of hydrogen are illustrated in Figure 9.2 using (3.6) and (3.7). As the hot carrier generation does not see an enhancement below 75 K (remains roughly constant), the reduction in hydrogen diffusion constant becomes the limiting factor in this region, and has also been shown to decrease degradation in MOSFETs at cryogenic temperatures [38], [113]. The limiting mechanisms that drive the temperature dependence of base current degradation in different temperature regimes are indicated in Figure 9.1.

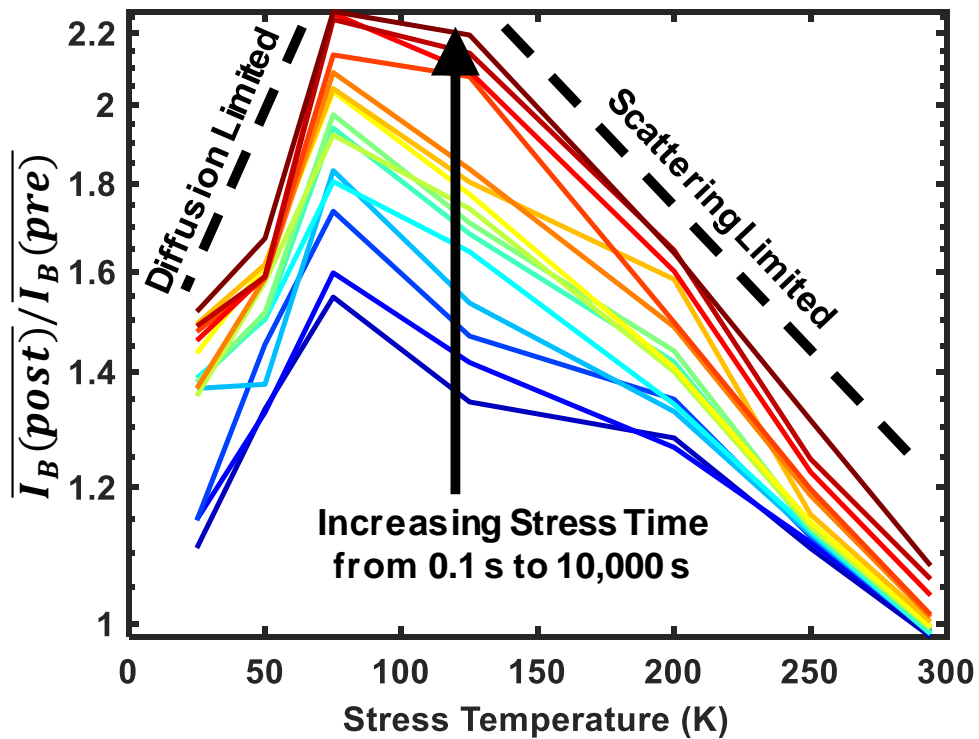


Figure 9.1: Increase in mean base current degradation seen across four device samples for cryogenic temperatures following a mixed-mode stress of $J_E = 100 \mu\text{A}/\mu\text{m}^2$ and $V_{CB} = 2 \text{ V}$. I_B extracted at $J_C = 1 \mu\text{A}/\mu\text{m}^2$. Colors from blue to red indicate increasing stress time from 0.1 s to 10,000s. Regions of damage limited by hydrogen diffusion and phonon scattering indicated.

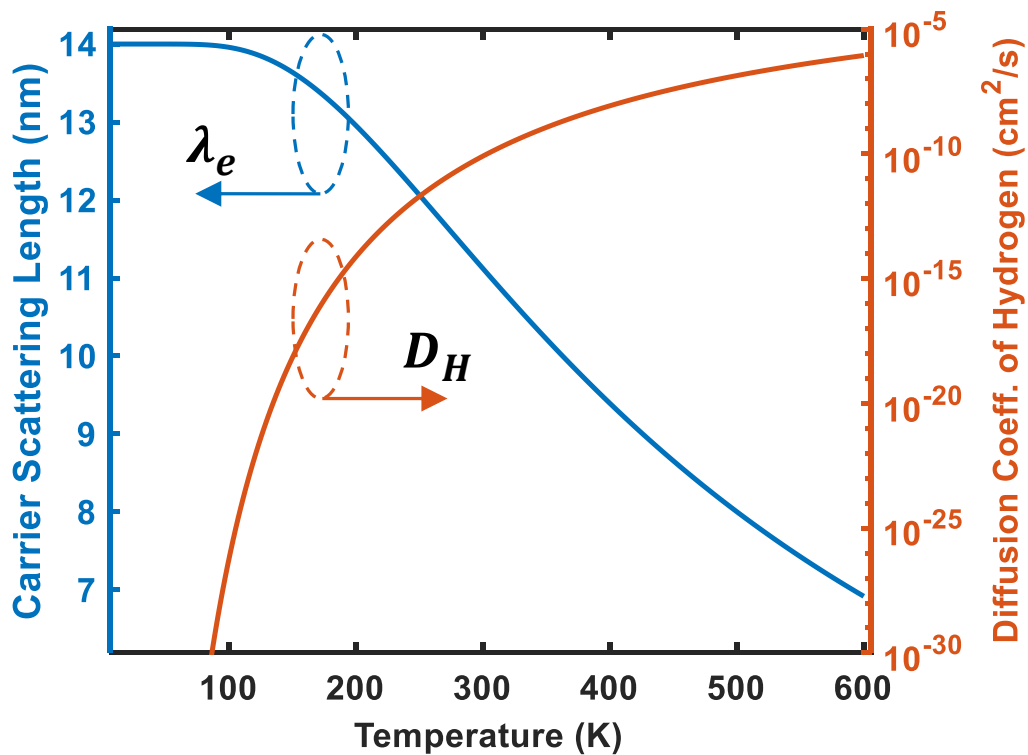


Figure 9.2: Temperature dependence of electron scattering length and diffusion coefficient of hydrogen following the calibration in [3].

Even though the trends in Figure 9.1 generally exhibit an increased damage with stress time, the device-to-device variation in damage increases at low temperatures as illustrated by the normalized standard deviation of base current degradation in Figure 9.3. Such increased variability of degradation has been measured in both NPN and PNP devices as shown in Figure 3.5 and Figure 5.12 [3], [5]. Figure 9.3 shows that variability in base current is almost two orders of magnitude higher for temperatures below 200 K when compared to the variability of base current at 300 K under un-stressed conditions. To understand these discrepancies, the following sections explore the physics of electrical variability in SiGe HBTs. Variability in currents can affect the current gain, breakdown behavior and eventually couple into the reliability of devices at low temperatures. Thus, cryogenic variability is a more important topic for devices and circuits before reliability.

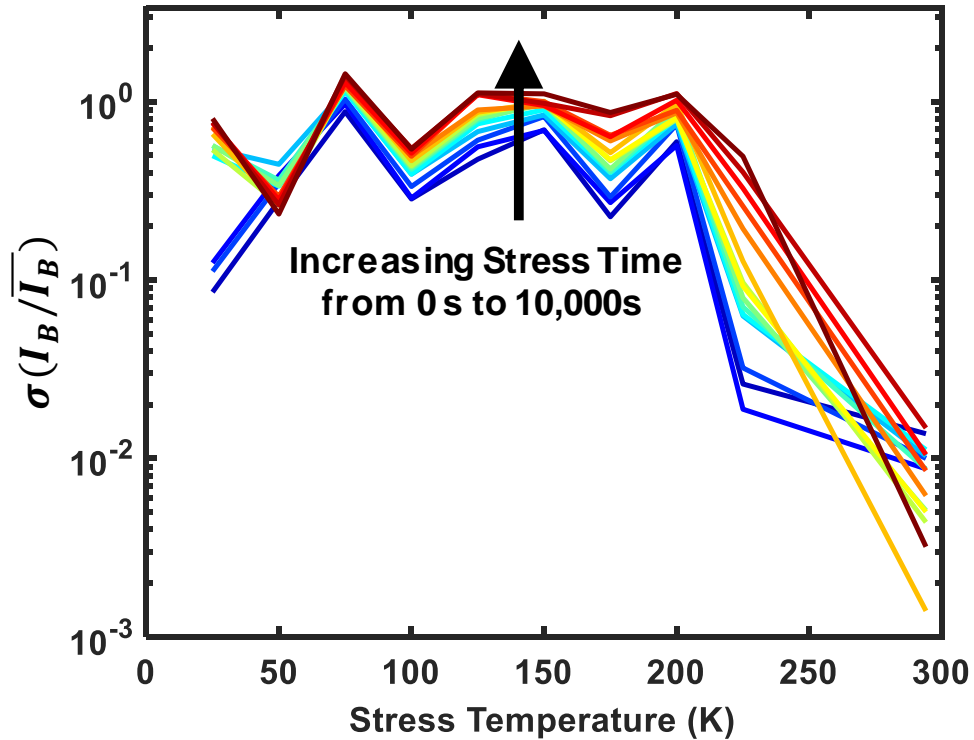


Figure 9.3: Measured variabilities of aged base currents plotted as standard deviations from the normalized mean value for the mixed-mode stress condition in Figure 9.1. Colors from blue to red indicate increasing stress time from 0 s to 10,000s.

9.3 Variability Challenges for Cryogenic Applications

At low temperatures, with subtle variations in device processing, large differences in device currents can be measured for fixed voltage in MOSFETs [114], [115]. This is also seen in SiGe HBTs, as illustrated by Figure 9.4, which plots the Gummel characteristics for twelve identical devices on the same die of a fourth-generation technology under forward mode (FM) and inverse mode (IM) operation at 25 K. Even though peak cut-off frequency (f_T) performance is usually achieved at high current levels, this work primarily focuses on low to medium injection levels ($< 1 \mu A/\mu m^2$), as these are of importance to QC interface ICs requiring minimal thermal loading on cooling systems. Observe that at a V_{BE} of 0.95 V, there is almost an order of magnitude variation in collector

current density (J_C) and base current density (J_B) under FM operation, which can be potentially problematic for designing reference circuits.

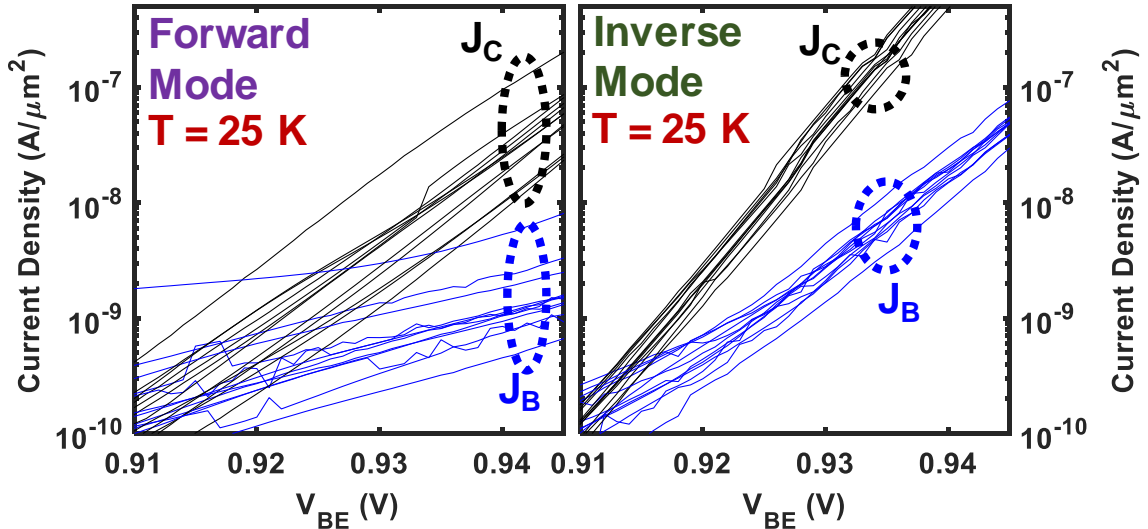


Figure 9.4: Measured variability of Gummel characteristics in a fourth-generation SiGe HBT across 12 sample devices under FM and IM operation at 25 K.

At low temperatures, incomplete ionization due to dopant “freeze-out”, process variations in doping, and Coulomb scattering have been suggested to be the source of measured electrical variability [114]–[116]. The critical doping for freeze-out (Mott transition) in Si is measured to be $2.8 \times 10^{18} \text{ cm}^{-3}$ for n-type dopants and $5.9 \times 10^{18} \text{ cm}^{-3}$ for p-type dopants [124]. However, the peak doping across the emitter, base and subcollector of the present SiGe HBTs is well-above these thresholds, as inferred from calibrated TCAD models for the device in Figure 9.4. The fact that this device still shows substantial variability suggests minimal impact of freeze-out.

To thoroughly understand this, the effects of generational scaling of SiGe HBTs in Table 9.1 on the electrical variability under cryogenic temperature operation is shown in Figure 9.5. First-, third-, and fourth-generation SiGe HBTs are compared against a Si ring

diode structure. Figure 9.5 generally indicates that current variability (σ_j) increases towards absolute zero temperature, irrespective of technology generation or device type. To qualitatively understand this behavior, the variance of the diode or bipolar currents can be expressed after [120] as

$$\sigma_I^2 = \sigma_{I_0}^2 e^{\frac{2qV_B}{kT}}, \quad (9.1)$$

where I_0 is the ideal saturation current, q is the electron charge, V_B is the applied bias, k is the Boltzmann constant and T is the ambient temperature. Irrespective of freeze-out and ignoring the temperature dependence in I_0 , the Shockley boundary conditions indicate that decreasing temperature enhances electrical variance, confirming the trends in measurements. The fact that σ_j increases even in a two-terminal diode structure suggests that electrical variations are a result of inherent limitations in diffusive transport at low temperatures, and not on the non-classical collector current transport mechanisms reported in SiGe HBTs [125]. Most importantly, the Si diode's σ_j is lower than that of the SiGe HBT currents, highlighting the possible role of Ge in shaping electric fields in the space charge region and thereby affecting mismatch [121].

Table 9.1: List of Devices Measured

Device	Size	Samples	SiGe HBT
1st Gen.	0.50 x 1 μm^2	8	[126]
3rd Gen.	0.12 x 15 μm^2	10	[127]
4th Gen.	0.10 x 6 μm^2	12	[123]
Si Diode	2 x (3.84 + 6.84) μm	12	-

Collector doping scales upward with generational node in SiGe HBTs. However, σ_{J_C} in Figure 9.5(a) does not follow any particular technological trend, which implies minimal dependence on freeze-out modulated by doping concentration. Compared to σ_{J_C} , which steadily increases with decreasing temperature, σ_{J_B} has a more complex behavior. This can be attributed to the non-ideal components of J_B , including Poole-Frenkel tunneling and emitter-base (EB) oxide interface trap recombination [32], [120]. With scaling, these low-injection non-idealities become more important as the intrinsic base region is brought closer to the emitter. Figure 9.5(b) shows that scaling-induced non-idealities steadily increase σ_{J_B} across generations between 125 K and 300 K.

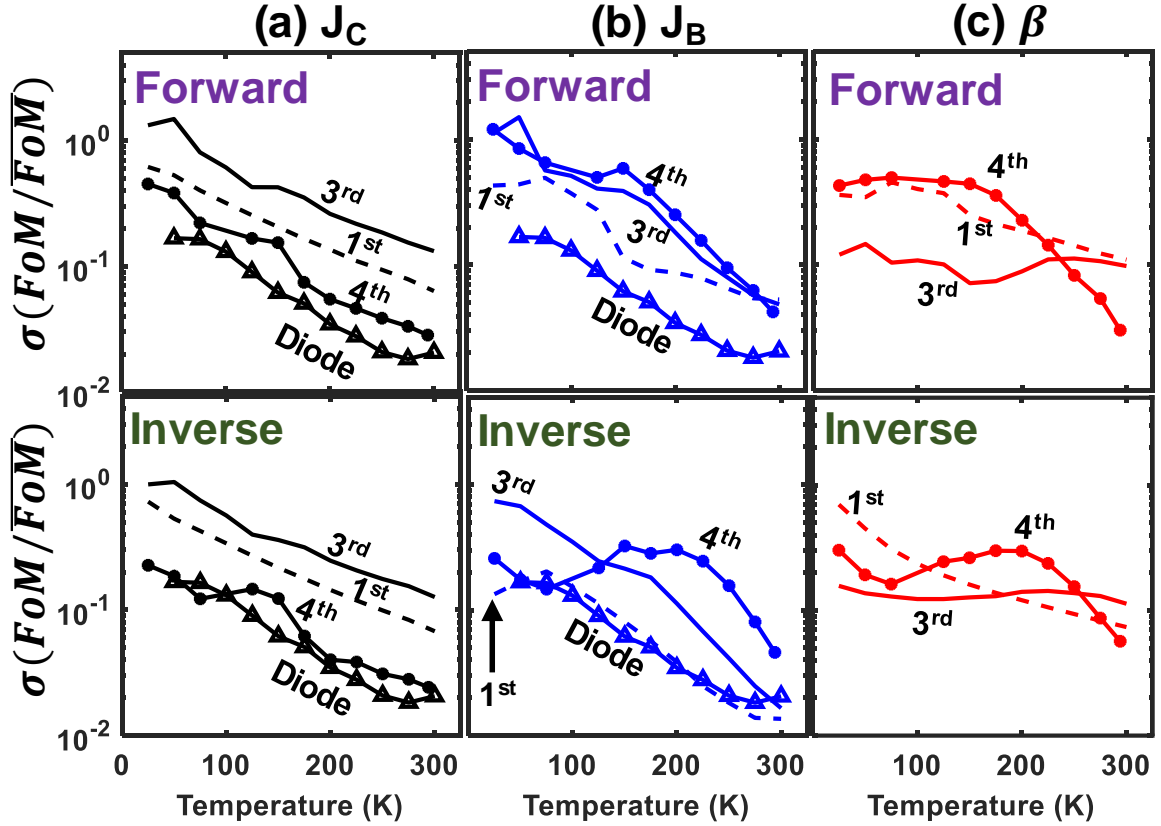


Figure 9.5: Measured FM and IM electrical variabilities plotted as standard deviations from the normalized mean value for different generations of SiGe HBTs and a ring diode. (a) J_C and (b) J_B extracted at fixed V_{BE} . (c) β extracted at fixed J_C . All extractions at or near $J_C = 1 \mu A/\mu m^2$.

Note that the individual variabilities in the base and collector currents with cooling do not necessarily translate into a well-defined variability in current gain (β) (e.g., the third-generation SiGe HBT displays an almost flat response across temperature in Figure 9.5(c) under FM and IM operation). Although not plotted, measured voltage variability for a fixed J_C was relatively flat across temperature as well, and not as significant ($\sigma = 0.001 - 0.006$) in all of the devices; whereas, the variability in transconductance ($\sigma = 0.02 - 2$), although also not plotted, mostly follows σ_{J_C} and can be important for circuit design. Since the current transport directions for the ring diode and SiGe HBTs are

different, the variability data for the ring diode is extracted at a low enough current level that it is not limited by resistive saturation due to dopant freeze-out across the temperature range measured.

To study the $\sigma_{J_{B,C}}$ dependence on impact-ionization (Coulomb scattering), the Gummel characteristics for a first-generation device (with collector doping below critical freeze-out levels) was measured, with and without a collector-base (CB) field, as shown in Figure 9.6. With this additional field applied, σ_{J_B} increases even more at low temperatures, which can perturb breakdown and reliability. Although field-induced dopant ionization can be used to reduce and modulate the effects of freeze-out ([128]) at the CB junction, σ_{J_C} experiences no difference from the applied CB field as it is largely still dependent on the process variations at the EB junction.

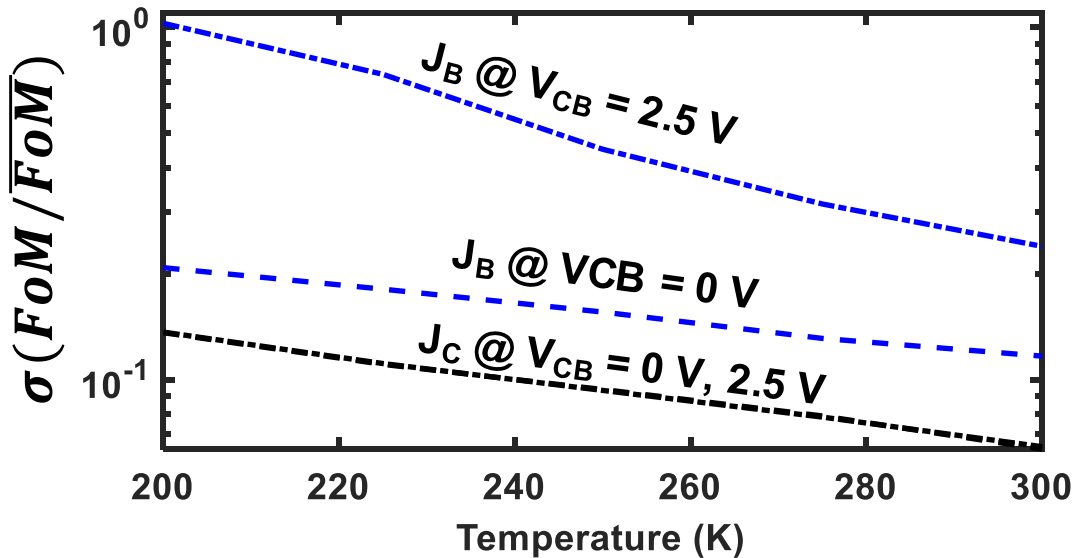


Figure 9.6: Measured FM electrical variability plotted as standard deviations from the normalized mean value for J_C and J_B extracted at fixed V_{BE} near $J_C = 1 \mu A/\mu m^2$ with and without an applied $V_{CB} = 2.5 V$.

Apart from variations in doping, the significantly reduced $\sigma_{J_{B,C}}$ under IM in Figure 9.4 indicates that the shape of the Ge profiles at the EB and CB metallurgical junctions plays a large role in the electric field distributions, and controlling the injection of currents, as mentioned in [121]. Although not generalizable, the more advanced third- and fourth-generation SiGe HBT technologies used in this study display larger $\sigma_{J_{B,C}}$ under FM, suggesting the alternate use of IM for better matching (with AC performance loss). Due to technology specifications, the differences in available emitter widths for each SiGe HBT generation may have contributed to additional differences, as mentioned in [114]. Nonetheless, it does not diminish the generality of the increased electrical variability measured under cryogenic operation.

9.4 TCAD Verification of Electrical Variability

To obtain a physical understanding of how process variations in doping affect $\sigma_{J_{B,C}}$ across temperature, TCAD simulations were performed on a calibrated SiGe HBT profile resembling the performance of the fourth-generation device. The Gaussian base doping profile was varied in TCAD, as illustrated in Figure 9.7(a), to qualitatively emulate and exaggerate the actual process variations during fabrication. Even without enabling incomplete ionization models, increasing $\sigma_{J_{B,C}}$ was achieved with decreasing temperature using hydrodynamic simulations, as seen in Figure 9.7(b). Similar to the measurements, the IM currents have less variability compared to FM, owing to the shape of the Ge profile. To understand the driving factors of variability, important device parameters were extracted from TCAD, and their maximum spatial variabilities in the base and emitter regions are plotted in Figure 9.7(c). Similar to the variability of diffusive transport

suggested by (9.1), the variability of minority carrier density in the quasi-neutral emitter and base regions increases at low temperatures. Additionally, Ge grading, and the temperature dependence of bandgap and bandgap-narrowing can affect the spatial variation of the electric field, as indicated in Figure 9.7(d). This can affect the ideal saturation current in (9.1) by altering field-dependent parameters such as carrier velocities, mobilities, and recombination, as shown in Figure 9.7(c).

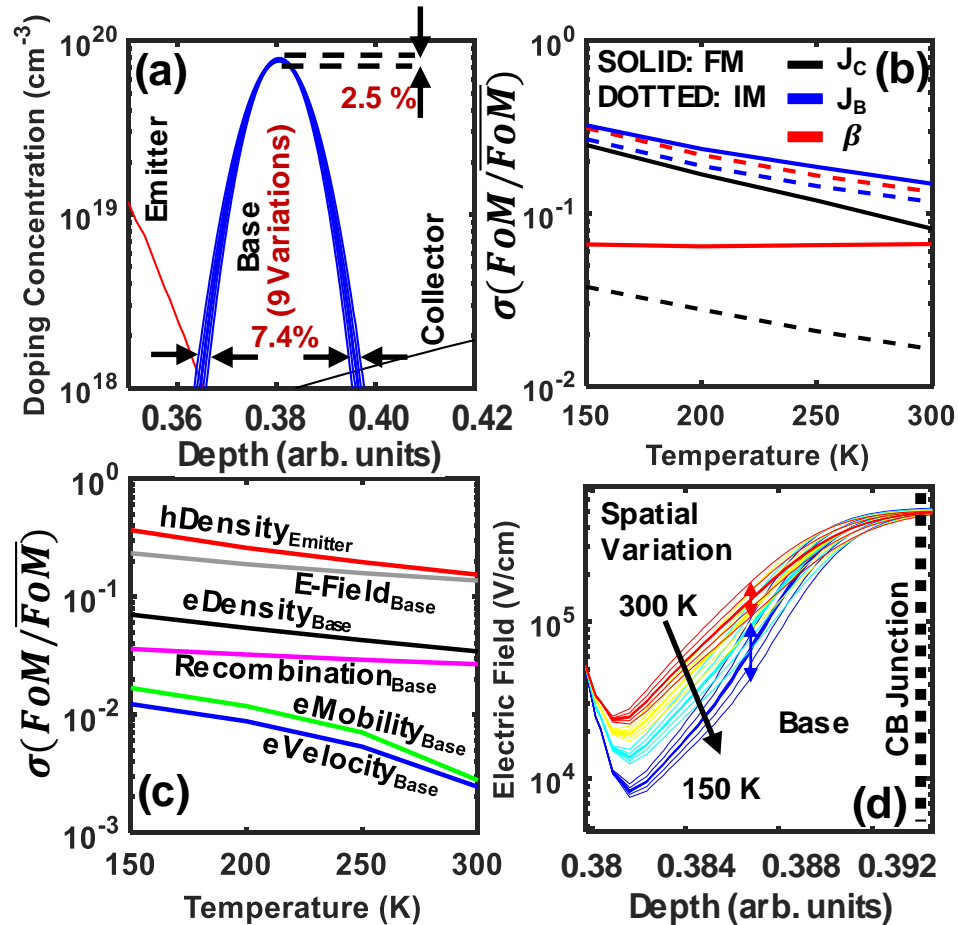


Figure 9.7: TCAD simulations of (a) profiles consisting of 9 total Gaussian base variations in width and peak doping. (b) Simulated σ_{J_C} (black) and σ_{J_B} (blue), and σ_{β} (red), under FM (solid) and IM (dotted). (c) Cross-sectional variability of significant TCAD parameters under FM. (d) Spatial variation of electric field with decreasing temperature under FM.

9.5 Summary

This work showed the first results of cryogenic reliability of SiGe HBTs under mixed-mode operation and the first measurements of electrical variability in SiGe HBTs down to 25 K. The maximum degradation in SiGe HBTs was observed between 75 K and 125 K. Above these temperatures, reduced scattering length of carriers due to phonon scattering decreases degradation. Below 75 K, the saturation of scattering lengths of hot carriers and reduced hydrogen diffusion limit the degradation. The variability observed in the reliability data highlighted the importance of the inherent variability in un-stressed devices at low temperatures. Variability ultimately perturbs reliability by affecting current gain, breakdown behavior and hot carrier generation in devices.

To explore the physics of variability, the electrical variability in three different generations of SiGe HBTs from 25 K to 300 K was measured and compared against the variability in a Si diode. Important findings from measurements and TCAD simulations include: 1) increased variability in diffusive transport at low temperatures, independent of dopant freeze-out; 2) enhanced base current variability due to impact-ionization, which can affect reliability; 3) reduced IM mismatch in advanced SiGe HBT nodes; and 4) ability of Ge in shaping fields and affecting variability.

CHAPTER 10

CONCLUSION

10.1 Summary of Contributions

This thesis investigated a number of degradation effects in SiGe HBTs being operated at extreme bias and temperature conditions (spanning almost 600 K!). While these devices offer considerable performance enhancements with the incorporation of bandgap grading in the base region, continued scaling of these devices poses a real challenge on reliability. As a result, building robust circuits and systems with high performance using these devices requires a deeper understanding of the different aging mechanisms. To more accurately predict these mechanisms and optimize for the limitations, this work contributed to the knowledge base of SiGe HBT reliability physics by demonstrating the following:

1. Accumulated stress damage across bias and temperature can indeed be predicted over simple point-to-point integration.
2. High-voltage stress damage is driven by impact-ionization and gets enhanced at low temperatures due to minimized phonon scattering. At cryogenic temperatures, despite a reduction in hydrogen's diffusion constant and saturation of scattering lengths, high-field stress damage still present from 25 K – 300 K, possibly indicating a combination of switching oxide traps and Si-H bonds responsible for oxide interface damage.
3. High-current stress damage is driven by Auger Hot carriers and gets enhanced at high temperatures due to the widening of the hot carrier energy distribution.

Although annealing also becomes a factor at high temperatures, enhanced degradation of oxide interfaces and polysilicon regions is still present from 300 K – 573 K.

4. PNP and NPN devices degrade differently due to the differences in activation energies associated with the polarity of doping near oxide interfaces and inside polysilicon regions. N-type doping is worse for reliability as it has a lower activation energy for damage compared to P-type doping. Similarly, N-type doping also has a higher activation energy for annealing compared to P-type doping.
5. Current gain enhancement happens with hot carrier damage in SiGe HBTs due to the depassivation of polysilicon, which reduces minority mobilities and minority injection.
6. Collector current enhancement happens with hot carrier damage in SiGe HBTs due to the redistribution of free hydrogen in polysilicon, which allows for regions of high passivation within polysilicon. Passivation affects majority and minority mobilities differently. Regions with high passivation improve majority carrier mobility, reduce effective polysilicon resistance and increase collector current.
7. Hydrogen can also neutralize Boron doping at high temperatures, reducing the base barrier. This causes parallel shifts in the collector current, and can affect the EB capacitance and peak f_T performance.
8. EB profiles can be designed with reduced capacitance for improving frequency response at low bias currents. This could enable current back-offs for reduced damage from Auger hot carriers. Profiles designed with temperature-independent

current gain could also reduce current crowding in power cells and further reduce uneven Auger damage and thermal runaway mechanisms.

9. Reliability at cryogenic temperatures is compounded by the increased variability. Variability increases at low temperatures due to coulombic scattering, doping variations, and incomplete-ionization. Variability present in CMOS, SiGe HBTs and even in diodes. Variability affects breakdown behavior and causes differences in aging across samples.

10.2 Future Work

The findings in this thesis have generated a rich list of interesting topics for research. These consist of measurements, modeling and design work as listed below:

1. Fully calibrated TCAD model with polysilicon and oxide interface degradation using the full hydrogen diffusion model. This model could potentially show the nuances between degradation and annealing over long duration stresses at high temperatures. Effects of self-heating on the scattering-lengths of the lucky electron model would give a further refinement in damage.
2. A natural next step would be to use some simplifications and build a compact model for simulation in circuits. The changes in gain and resistance could be very useful in accurately simulating circuit reliability. A list of parameters that need to be aged with stress includes non-ideal base current, ideal base current, base and emitter resistances, and EB capacitance.
3. Quantifying the effects of DC degradation (CGE, resistance degradation, oxide interface degradation, and parallel collector current shift) on RF performance at the

device and circuit levels. The performance vs. reliability trade-off space must be investigated.

4. Looking at the validity of quasi-static approximation to device degradation at high frequencies, across temperature, and in the presence of self-heating. DC measurements need to be compared with pulsed stress measurements with varying pulse widths and duty cycles.
5. Explore the relationship between hard failures and soft failures. Devices often times do not immediately die when stressed. However, they may fail after tens, hundreds or even thousands of seconds. This is likely due to an increase of power density within the device due to “soft” damage. With aging, the device struggles to maintain a fixed current or voltage stress condition because of damage to the intrinsic (ideal base current, oxide traps, EB capacitance) and extrinsic (polysilicon resistances) portions of the device.
6. Engineering PNP devices with better reliability that is more matched to the NPN devices. The understanding of how doping polarity affects the activation energies for damage and annealing reactions at oxide interfaces and polysilicon grain boundaries should help in creating isolation layers for sensitive regions of a device.
7. Measuring the linearity of the EB optimized profiles. Demonstrate the robustness of the optimized devices under high power operation. Also, investigate the reliability of power cells using these devices.
8. Measuring the EB optimized Ge ledge profiles at cryogenic temperatures, and also exploring other optimizations at the device level for reduced signs of variability. The AC variability must be measured and correlated to the DC degradation seen.

9. Investigating the effects of high-current stress at cryogenic temperatures. Even though the energy distribution for Auger hot carriers narrows with decreasing temperature, the increase in silicon's bandgap may help in creating a hot carrier with the energy of two simultaneous Auger transitions - this may be sufficient for oxide interface damage. This effect needs to be investigated exhaustively below room temperature.
10. Investigating CGE, polysilicon resistance degradation and EB capacitance degradation at cryogenic temperatures.

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VITA

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