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Reconfigurable Load-Modulated Power Amplifier For Energy- and Spectrum-Efficient Wireless Communications

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RECONFIGURABLE LOAD-MODULATED POWER AMPLIFIER FOR ENERGY- AND SPECTRUM-EFFICIENT WIRELESS COMMUNICATIONS

by

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ABSTRACT

With the increasing demand for faster date rates and extensive user connectivities, the complex modulation schemes and large-scaled arrays have been widely researched and employed in the modern wireless links e.g., 5G and beyond-5G systems. These pose major challenges to design the power amplifiers (PAs) to accommodate the system level evolution. As the critical part, the power amplifiers (PAs) dominate the output power, efficiency, linearity and reliability of the radio frequency (RF) transmitter. Consequently, the PA's capability of maintaining an efficient, linear and reliable signal amplification operation is essential to the communication systems. On the other hand, due to the deployment of massive multiple input/multiple output (MIMO) technique, the highly integrated active antenna systems replaced traditional 50Ω-based PA with sectorized antenna architectures. This brings the fact that, as the beam is steered in the antenna array, the dynamic load impedance observed from PAs can be up to 2: 1 Voltage Standing Wave Ratio (VSWR) due to the time-varying phasing and output power between the adjacent antenna elements and PAs, thus severely deteriorate PAs' performance.

To resolve aforementioned challenges, a novel design theory of Quasi-balanced Doherty power amplifier (QB-DPA) is first presented in this dissertation, which opens a new vision to counteract the mismatch-induced degradation using reconfigurable PA architectures. In this QB-DPA design, the isolation port of the PA's output coupler is alternatively terminated to 50-Ω load and ground to enable the balanced and Doherty modes. With the implementation of the silicon-on-insulator (SOI)-based single-pole-double-throw (SPDT) switch to realize the reconfiguration, the physical prototype is demonstrated exhibiting remarkable DPA performance, in terms of the linearity, efficiency and output power.

Subsequently, a series/parallel QB-DPA theory that not only can improve the back-off efficiency

of QB-DPA, but also significantly restore the load-mismatch degradation is proposed. This novel topology includes and unifies QB-DPA modes at balanced, series and parallel Doherty, respectively. Moreover, a novel linearity-enhanced combiner is introduced for nominal 50-Ω load to improve the linearity at both series and parallel QB-DPA modes. The reconfiguration between series and parallel operations largely restore the performance degradation when the PAs suffer a dynamic antenna mismatch condition.

Finally, a wideband mismatch-resilient QB-DPA is presented. Through parallel/series reconfiguration and reciprocal biasing, it is for the first time shown that the QB-DPA is able to maintain a stable output power as well as enhanced efficiency and linearity across $2:1$ VSWR circle, and this operation can be seamlessly extended to a wide bandwidth which holds promising potential for application to array-based massive MIMO systems.

To my wife Minyi Zhang and my family

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CHAPTER 1: INTRODUCTION

1.1 Motivation of Mismatch-Resilient PAs

The modern wireless systems, i.e., 5G and beyond-5G, featured as ultra-fast data rates and ever-increasing user connectivity, have stimulated the research and development of new technologies of the radio frequency front-end (RFFE) to cope with the challenges. It is envisioned that the wider instantaneous bandwidth and spectrally efficient modulation schemes will be widely employed for the future communication ecosystem. As the key device in the RF transmitter, power amplifiers (PAs) play a critical role to amplify the RF signals to the antennas, which dominate the many performance aspects of the entire system [2]. Therefore, the PAs are expected to achieve an ultimate balance of energy efficiency and linearity as well as other specs in the wireless links.

To achieve a maximum channel throughput, modern communication standards and applications extensively employ complex modulation schemes, such as Orthogonal frequency division multiplexing (OFDM), high-order quadrature amplitude modulation (QAM) and carrier aggregations, which exhibits large dynamic ranges featured with high peak-to-average-power ratio (PAPR). This, however, causes a dramatic degradation of average efficiency of power amplifier (PA), since it has to routinely operate in significant power back-off regions. Conventional PAs (basic classes of A-C and harmonic tuned classes E,F and J) are designed target for high peak power efficiency at saturation level, which brings in the concern about the thermal management when amplifying such high-PAPR signals. Moreover, due to the complex constellations requirements, the PA linearity are also mandatory to ensure the signal fidelity and the communication link Quality-of-Service (QoS) to transmit high-PAPR signals.

Meanwhile, with the proliferation of communication bands, more and more spectrum fragments

are being incorporated into wireless communications. In order to accommodate the ever-increasing number of allocated frequency bands, the RF bandwidth of power amplifiers and transmitters need to be as wideband as possible to support the multi-band/multi-mode operations without suffering from non-affordable hardware complexity, size, and cost. Therefore, broadband and highly-performance PA technologies are of crucial importance for next-generation wireless systems. Extensive research regarding PA architectures to enhance the PA efficiency over the broad bandwidth have been proposed and developed including supply modulation (envelope tracking) and load modulation. However, due to the bandwidth limitation and time constraints of the current dc-dc converter techniques to track the modulation signal envelope, load modulation PA architectures becomes a hot topic that draws more interests. Various of load-modulation architectures have been proposed and employed in realistic systems, including Doherty PA (DPA), out-phasing PA, and load modulated balanced amplifier (LMBA).

Doherty PAs are amongst the most widely adopted in cellular base station due to its enhanced efficiency at significant power back-offs as well as simple and mature architecture. The original Doherty PA (DPA) topology invented by William H. Doherty in 1936 consists of two different biased amplifiers (Class AB for main and Class C for auxiliary) combined with two quarter-wave transmission lines (TLs). Compared with conventional PAs (mentioned above), the DPA's back-off efficiency can be substantially enhanced, which makes it be a competitive candidate to amplify signals with complex modulation. However, due to the quarter-wave transformer employed ,strong nonlinearity is accompanied during the load modulation process. Consequently, external linearization techniques such as digital predistortion (DPD) are required to maintain the signal's quality and comply with the communications standards. Since DPD is quite energy consuming, especially when accommodating wide modulation bandwidths of signals, intrinsically linear DPAs are more preferred in emerging array-based communication systems, e.g., 5G.

On the other hand, to further enhance the spectral efficiency, array-based spatial multiplexing tech-

nique has been widely exploited in 5G base stations that leverages the spatial differences to enable concurrent transmission of multiple signals at the same frequency, also known as massive multiple-input multiple-output (MIMO). Compared with small-scale MIMO systems, the massive MIMO serve more subscribers with the expansion of the array scale to produce the required effective isotropically radiated power (EIRP) towards receivers through the digital (Sub-6-bands) or hybrid (mm-Wave) beamformer. However, the high-density antenna array inevitably brings about strong mutual couplings between the co-located antennas as the beam is steered in the array. These couplings result in a high-speed antenna impedance variation as well as a large time-varying change of voltage standing wave ratio (VSWR) and therefore, the antenna presents a sub-optimal loadline to the associated PA in the RF chain that engender a significant performance (e.g., efficiency, linearity, and OP1dB) degradation of PA. A more severe issue is the main beam distortion due to the accumulated PA non-linearity among the array in which different AM-AM and AM-PM distortion generated for different element location, and it render (DPD) ineffective to be applied at array level considering the power, cost and complexity.

While meeting all the aforementioned requirements, the future PA architectures are expected to improve the efficient and linear operations when exposed to substantial load mismatch, while maintaining a large achievable bandwidth for sustainable cost and space. To solve these challenges, a generalized coupler-based Quasi-balanced Doherty PA (QB-DPA) theory was first proposed. This novel PA architecture can be reconfigured from balanced mode to Doherty modes (B2D) through a SOI voltage-controlled single-pole double-throw (SPDT) switch to counteract the load mismatch, while high efficiency and linearity can be maintained over the VSWR variations. More importantly, this theory analytically proves that the load modulation behavior of the QB-DPA is mathematical equivalent to the conventional DPA, which provides a new design methodology of linear and efficient DPA.

The discovery of QB-DPA theory enables the PA reconfiguration between Doherty and balanced

modes to mitigate the performance impairment induced by dynamic antenna impedance variation. In order to enhance the back-off efficiency due to the identical drain bias conditions applied for PAs at balanced mode, a series and parallel QB-DPA theory is then proposed. Through reciprocally exchanging the main and auxiliary amplifiers and alternatively terminating the isolation port of the output coupler to a small reactance (close to short circuit) and susceptance (close to open circuit), the QB-DPA can significantly alleviate the load mismatch related degradation. This expanded theory reveals that the series and parallel modes have different sensitivity to load mismatch in a complementary way. In conjunction with a first-ever proposed reactive loadline tuning at the coupler's isolation port, the series/parallel QB-DPA can be utilized to counteract the arbitrary load mismatch up to $2.5:1$ of VSWR with a state-of-the-art performance. Although the proposed series/parallel QB-DPA in the second part of this dissertation presents a distinctive performance improvement in terms of power efficiency, linearity, and output power, it is presently limited to the relative narrow bandwidth operation. The last part of the dissertation will focus on a bandwidth extension for the PA based on the QB-DPA theory to counteract the load mismatch.

1.2 Chapter Outline

This dissertation will focus on the mode-reconfigurable Quasi-balanced Doherty PA against load mismatch for massive MIMO application. Chapter 1 gives a brief introduction of modern wireless systems architecture and the performance specifications required for future PA's design. The balanced-to-Doherty PA theory will be derived and established in chapter 2 with proposed linear DPA design methodology. The chapter 3 explores the series/parallel QB-DPA theory that can largely mitigate the degradation due to the dynamic impedance variation. The wideband active antenna array friendly QB-DPA is introduced in chapter 4. Summary will then be drawn in chapter 5 with projected future works.

CHAPTER 2: BALANCED-TO-DOHERTY MODE-RECONFIGURABLE POWER AMPLIFIER WITH HIGH EFFICIENCY AND LINEARITY AGAINST LOAD MISMATCH

[1]A design methodology of load insensitive PA has drawn extensive interests recently due to the massive MIMO deployment. In particular, load modulation PAs with high average efficiency, linearity over VSWR variation are a competitive candidate to be applied in the 5G or beyond 5G systems. This chapter will systematically investigate a first-ever proposed mismatch-resilient load modulation PA architecture.

2.1 Introduction

The evolution of wireless communications has triggered ever-increasing demands for higher data rate and enhanced spectral efficiency, which are typically realized through widened modulation bandwidths and advanced modulation techniques, such as orthogonal frequency-division multiplexing (OFDM) and high-order quadrature amplitude modulation (e.g., 1024 QAM). These modulation schemes introduce large peak-to-average power ratio (PAPR) that not only substantially degrade the power-amplifier (PA) efficiency but also impose stringent linearity requirements on PAs. Consequently, the PA's capability of efficiently and linearly transmitting high-PAPR signals is critical to modern communication systems towards ultra-fast speed and high energy efficiency.

In the past two decades, the Doherty PA (DPA) architecture has been widely employed in wireless

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communications infrastructures (e.g., base stations) due to its enhanced efficiency at significant power back-offs. Until now, numerous DPA techniques and demonstrations have been reported, exhibiting significant progress towards realizing highly efficient DPAs in various semiconductor technologies [3–9] together with extended application horizons, e.g., from single-band to multi-band [10–15] and from microwave frequencies to millimeter-wave frequencies [16–22].

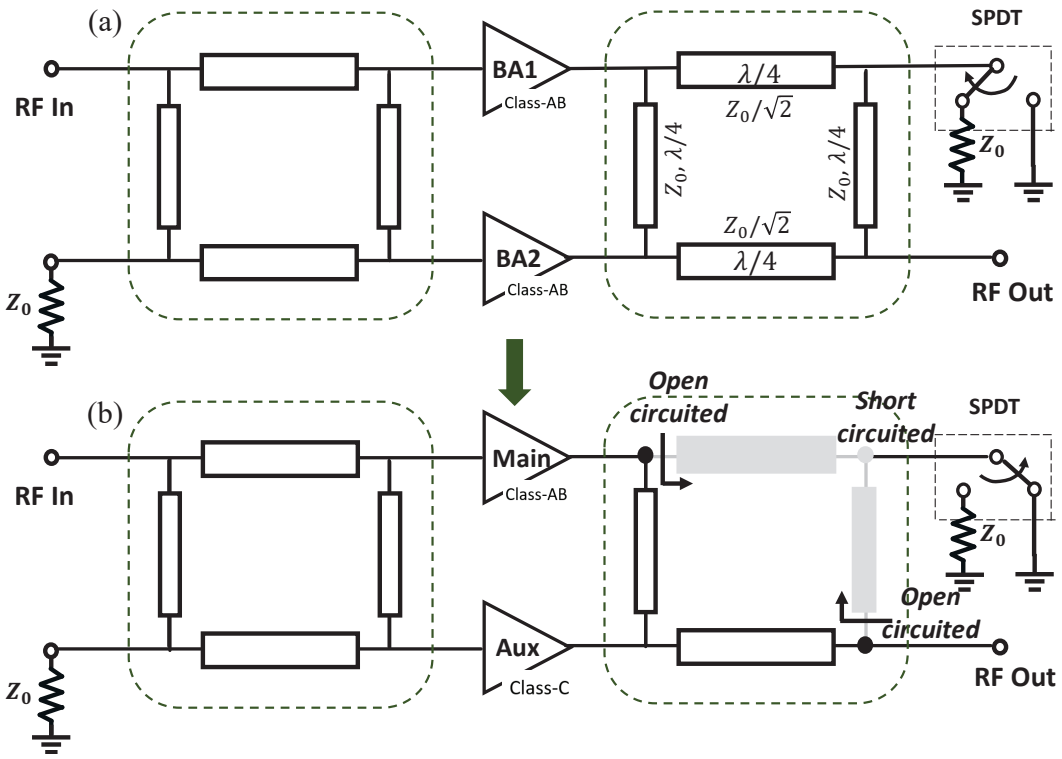


Figure 2.1: Conceptual architecture of the proposed B2D mode-reconfigurable power amplifier. A SOI-based SPDT switch terminates the isolation port of the output coupler to 50-Ω load and ground alternatively. (a) Balanced mode. (b) Doherty mode.

In realistic communications, due to the non-linear nature of DPAs, external linearization using digital pre-distortion (DPD) is usually applied to DPAs to maintain the transmission signal's fidelity and to comply with specific communications standards. In the future generations of wireless communications, e.g., 5G, the cell size is expected to be reduced significantly (e.g., from Marco cell to Micro/Femto cell) leading to much higher base-station densities and considerably lower power

levels. Since DPD is quite energy consuming, especially when accommodating wide modulation bandwidths of signals [23], PAs at lowered power level are strongly desired to be intrinsically linear. Recently, several linear DPAs have been presented in terms of both theoretical analysis and practical design demonstrating enhanced linearity as well as high efficiency [24–27].

On the other hand, the spatial multiplexing/combining techniques, such as multi-input multi-output (MIMO) antennas and active antenna array, have been widely applied in the 5G communications to further increase the data rate, radiation distance, and overall system capacity. However, the mutual coupling between different antennas under concurrent MIMO transmissions and/or beam steering can lead to ongoing variation of antenna impedance at very fast time scales [28–31]. As a result, the current solution of discrete antenna tuners based on phase-detection and feedback control will in-all-likelihood not be able to seamlessly respond to such a rapid impedance variation [32]. Although the circulators/isolators can be placed between PA and antenna element, they introduce extra loss and are too costly and bulky for massive-array applications [29,31]. Therefore, the PAs in future communications systems are expected to maintain efficient and linear operations against substantial load mismatch by themselves. Different from the conventional impedance tuning method, new paradigms of mismatch recovery at PA stage have been investigated, such as specialized control of digital Doherty PAs against load variation [33] and direct impedance measurement using distributed sensors [34]. Until now, there has not been a solid solution that is able to cover a large impedance variation range and is readily compatible with the existing systems as a "drop-in" module.

To solve the aforementioned challenges, a balanced-to-Doherty (B2D) mode-reconfigurable PA is proposed in this paper, as conceptually illustrated in Fig. 2.1. The isolation port of the output coupler is alternatively terminated to 50-Ω load and ground to enable balanced mode and Doherty mode, as shown in the Fig. 2.1(a), (b) respectively, which can be physically realized by a single-pole double-throw (SPDT) switch. In our related conference paper [35], we have pre-

liminarily presented a proof-of-concept demonstration of the B2D reconfigurable PA. This paper significantly expands our previous works [35, 36] in the following aspects. **First**, a generalized theory of the quasi-balanced Doherty PA (Doherty mode of the B2D reconfigurable PA) is analyzed based on the ideal mathematical model of quadrature coupler, and it is analytically proven that the load modulation behavior of QB-DPA is equivalent to the conventional Doherty PA. This generalization inclusively explains and verifies the designs using branch-line hybrids in [35, 36]. **Second**, a systematical design methodology of the B2D PA is presented targeting for high linearity and efficiency at both the balanced and Doherty modes. Based on the QB-DPA theory and the proposed design methodology, a prototype is developed using GaN technology at 3.5 GHz demonstrating state-of-the-art DPA performance in terms of linearity and efficiency at the nominal 50-Ω load condition. **Third**, a comprehensive mismatch evaluation using modulated signals is experimentally presented. It is remarkably discovered that the linear and efficient PA performance can be well maintained up to $2:1$ (predicted in typical MIMO operations [28, 37]) of voltage standing wave ratio (VSWR) by using B2D reconfiguration.

In actual MIMO systems [31, 38], the transmitter system performance (e.g., ALCR and EVM) is monitored in real time, and the PA can be adapted from QB-DPA mode to balanced mode when an abnormal linearity is detected. In phased-array applications, the impedance of each antenna element could be pre-characterized as a function of scan angle [31]. For a particular antenna element, the associated PA can be adapted according to scan angle. Envisioning these scenarios, the B2D adaption can be applied seamlessly without having to detect the phase and amplitude of mismatch.

2.2 Quasi-Balanced Doherty PA Theory

In this section, based on the new quasi-balanced Doherty PA (QB-DPA) configuration, the operation of active load-modulation is theoretically analyzed. In this circuit topology, the essential Doherty combining network is implemented using a specially configured quadrature coupler in a balanced amplifier topology, as illustrated in Fig. 2.1. In [39, 40], by leaving the isolation port of the branch-line coupler as open circuit, the possibility of implementation hybrid coupler as a output combining network for the DPAs is introduced. In this section, a new methodology of quadrature hybrid modularization is theoretical analyzed.

Assuming a system impedance of Z_0, the voltage and current relationship of the four-port coupler network can be expressed using an impedance matrix constructed with Z-parameters, given by

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} & 0 \\ +j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & +j \\ 0 & -j\sqrt{2} & +j & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \tag{2.1}$$

To theoretically model this new type of DPA, a simplified output combining network is constructed based on an ideal 3-dB quadrature hybrid coupler model, as shown in Fig. 2.2, including the excitation and loading. The isolation port (Port 2) is terminated to ground, and the output port (Port 1) is loaded to a 50-Ω terminal. Two ideal current sources I_{M} and I_{A}, which represent main and auxiliary amplifiers, are connected to the two excitation ports (Port 4 and Port 3) of the coupler, respectively.

As the isolation port is grounded, the associated port voltage is thus zero. By applying this condition ($V_2 = V_{\mathrm{Iso}} = 0$) on the first row expansion of the matrix operation in Eq. 2.1, the dependence

of the main amplifier current and load current can be determined by:

$$I_{\mathrm{M}} = \frac{\sqrt{2}}{2} I_0. \tag{2.2}$$

where $I_{\mathrm{M}} = I_4$ and $I_0 = I_1$. Meanwhile, the load current and voltage of the RF-output port can be expressed by

$$V_0 = -Z_0 I_0. \tag{2.3}$$

In this design, to ensure reconfiguration between Doherty mode and balanced mode, the main PA and auxiliary PA in Doherty mode are identical in terms of the current/voltage scaling, because this symmetry has to be enforced in balanced mode. Nevertheless, the main and auxiliary PAs can be asymmetrical in Doherty-only designs based on this quasi-balanced configuration. The theoretical analysis on the QB-DPA operation is performed at both back-off and saturation.

2.2.1 QB-DPA Operation at 6-dB Power Back-off and Below

In the power region at 6-dB back-off and below, the equivalent circuit can be modeled as Fig. 2.2(a). As the auxiliary amplifier is turned off, it presents an ideal open circuit to Port 3 with no current injection from the auxiliary path ($I_{\mathrm{A}} = I_3 = 0$). With this boundary condition, the matrix operation in Eq. (2.1) can be re-written as

$$\begin{bmatrix} V_0 \\ 0 \\ V_{\mathrm{A,bo}} \\ V_{\mathrm{M,bo}} \end{bmatrix} = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} & 0 \\ +j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & +j \\ 0 & -j\sqrt{2} & +j & 0 \end{bmatrix} \begin{bmatrix} I_0 \\ I_{\mathrm{Iso}} \\ 0 \\ I_{\mathrm{M,bo}} \end{bmatrix} \tag{2.4}$$

where $V_{\mathrm{M,bo}}$ and $I_{\mathrm{M,bo}}$ denote the back-off voltage and current of the main amplifier, respectively, and $V_{\mathrm{A,bo}}$ represents the voltage swing at the floating auxiliary amplifier port. By substituting the condition of $I_{\mathrm{A}} = 0$ into the above matrix operation in Eq. (2.4), it leads to the following dependencies:

$$V_{\mathrm{M,bo}} = -j\sqrt{2}I_{\mathrm{Iso}}Z_0 \quad \& \quad I_{\mathrm{Iso}} = jI_0. \tag{2.5}$$

Together with Eq. (2.2), the impedance seen by the main and auxiliary amplifiers can be expressed as

$$\begin{aligned} Z_{\mathrm{M,bo}} &= \frac{V_{\mathrm{M,bo}}}{I_{\mathrm{M,bo}}} \\ &= \frac{-j\sqrt{2}I_{\mathrm{Iso}}}{I_{\mathrm{M,bo}}}Z_0 \\ &= 2Z_0, \\ Z_{\mathrm{A,bo}} &= \infty. \end{aligned} \tag{2.6}$$

From the above Eq. (2.6), it is interesting to note that this quasi-balanced DPA is functionally equivalent to the standard Doherty PA at the power back-off condition.

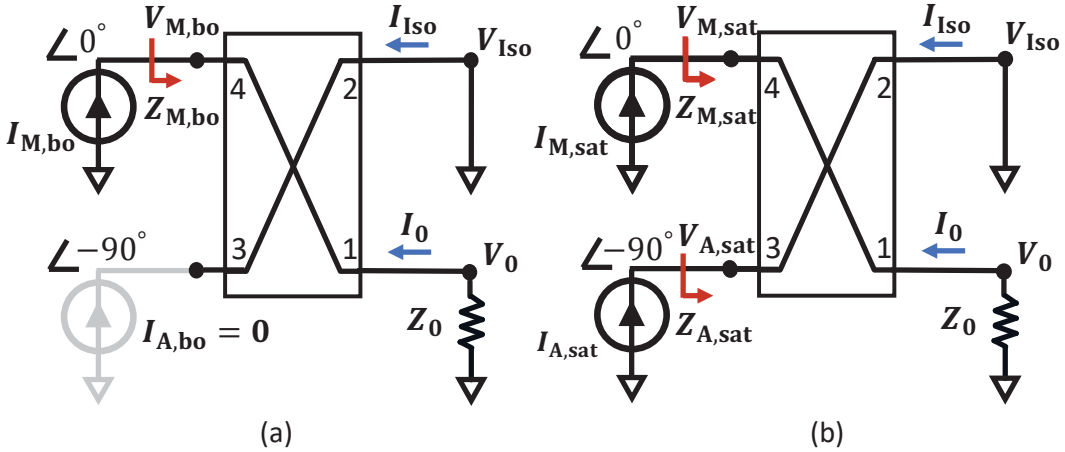


Figure 2.2: Generalized schematic of the output combining network for analyzing the proposed QB-DPA architecture at (a) 6-dB power back-off and below and (b) power saturation.

2.2.2 QB-DPA Operation at Power Saturation

At the saturated power level, both the main and auxiliary amplifiers are fully operating towards saturation of voltage and current so that the impedance matrix can be re-arranged as

$$\begin{bmatrix} V_0 \\ 0 \\ V_{\mathrm{A,sat}} \\ V_{\mathrm{M,sat}} \end{bmatrix} = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} & 0 \\ +j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & +j \\ 0 & -j\sqrt{2} & +j & 0 \end{bmatrix} \begin{bmatrix} I_0 \\ I_{\mathrm{Iso}} \\ I_{\mathrm{A,sat}} \\ I_{\mathrm{M,sat}} \end{bmatrix} \tag{2.7}$$

Since the two amplifiers are designed identically, the saturation voltages and currents between the main and auxiliary path have the same magnitude. By conducting the matrix operation using Eq. 2.7, the following dependencies are formed

$$I_{\mathrm{M,sat}} = jI_{\mathrm{A,sat}} \quad \& \quad I_{\mathrm{Iso}} = 0. \tag{2.8}$$

The 90° phase difference between the I_{M} and I_{A} is due to the ideal 3-dB quadrature-coupler divider at the input. It is also interesting to note that the isolation port becomes an electrical "null" in this condition, since it has zero voltage and zero current, simultaneously. Based on Eqs. (2.3) and (2.8), the load impedance seen by the main amplifier, i.e., $Z_{\mathrm{M,sat}}$, can thus be calculated using the associated saturation voltage, $V_{\mathrm{M,sat}}$, and current, $I_{\mathrm{M,sat}}$, given by

$$\begin{aligned} Z_{\mathrm{M,sat}} &= \frac{V_{\mathrm{M,sat}}}{I_{\mathrm{M,sat}}} \\ &= \frac{jI_{\mathrm{A,sat}} - j\sqrt{2}I_{\mathrm{Iso}}}{I_{\mathrm{M,sat}}} Z_0 \\ &= Z_0. \end{aligned} \tag{2.9}$$

For the auxiliary path, the exhibited load $Z_{\mathrm{A,sat}}$ can be derived as

$$\begin{aligned} Z_{\mathrm{A,sat}} &= \frac{V_{\mathrm{A,sat}}}{I_{\mathrm{A,sat}}} \\ &= \frac{jI_{\mathrm{M,sat}} - j2I_{\mathrm{M,sat}}}{I_{\mathrm{A,sat}}} Z_0 \\ &= Z_0. \end{aligned} \tag{2.10}$$

Eqs. (2.9) and (2.10) underline that the quasi-balanced DPA operation at saturation level is again equivalent to a standard DPA.

The load modulation behaviors of the main and auxiliary PAs at both power back-off and power saturation reveal a remarkable discovery: when loading the isolation port of the output quadrature coupler to ground, the balanced PA can be fully converted into an ideal Doherty PA. This finding not only enables PA reconfiguration between Doherty and balanced modes, but it also exhibits promising potential of the quasi-balanced DPA for extension to wideband implementations, since the balanced amplifier configuration is considered bandwidth-friendly by nature [41], [42].

2.3 Practical Design Methodology of Linear B2D Mode-Reconfigurable PA

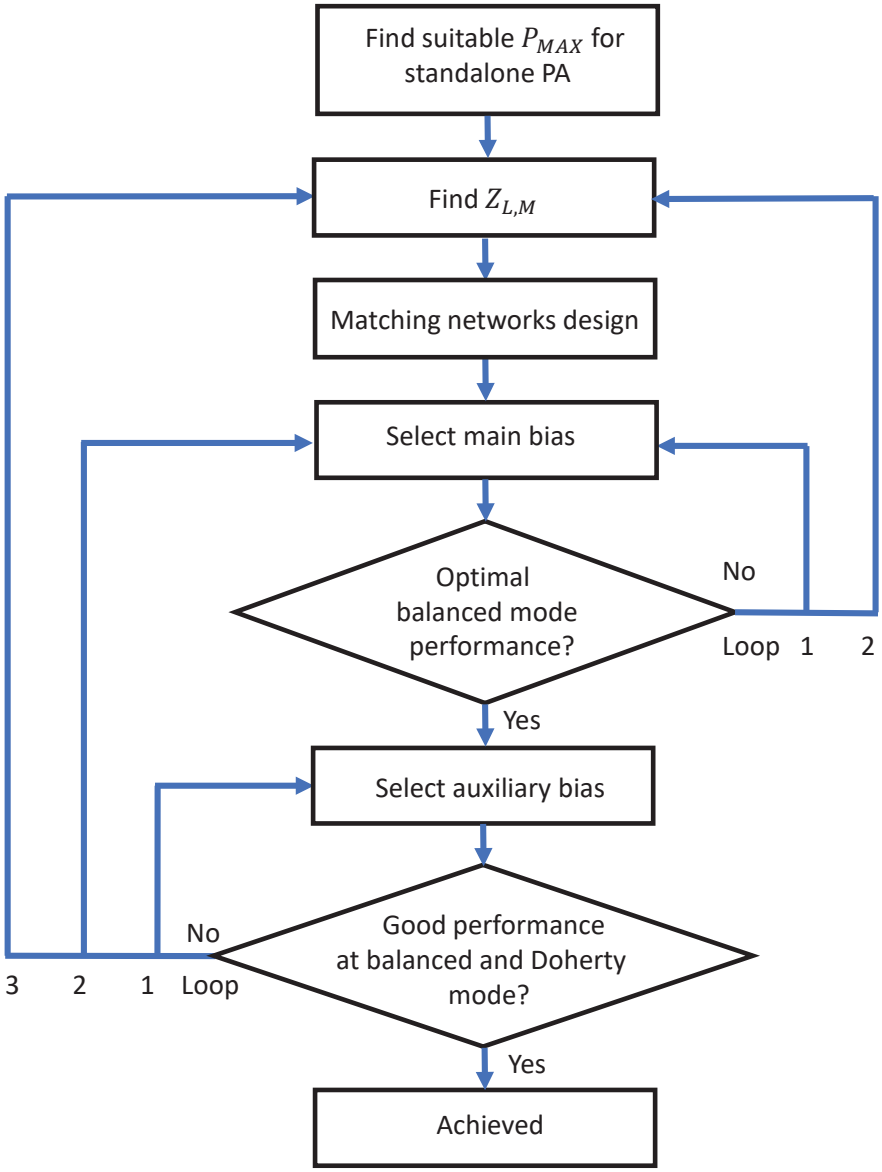


Figure 2.3: Systematic design flow of the B2D mode-reconfigurable PA.

The derivation described in the previous section shows the possibility of converting a balanced PA to an ideal Doherty PA by terminating the isolation port of the output coupler to ground. Based upon the proposed theory, the design methodology of linear balanced-to-Doherty mode-

reconfigurable PA is presented in this section. It is worth noting that the two standalone PAs in the QB-DPA architecture should be designed identically and, thus, the device periphery ratio is equalized between the main and auxiliary transistors. The flowchart in Fig. 2.3 describes the detailed design procedure, which includes the following key steps:

- **Step 1:** *Determination of* P_{Max}. The maximum power is usually determined by the target application in which the maximum rated power (P_{Rated}) is specified by the particular communications standard. P_{Rated} can be approximately expressed as

$$P_{\mathrm{Rated}} = P_{\mathrm{1dB}} - \mathrm{PAPR}. \tag{2.11}$$

  where P_{1dB} is the 1-dB compression point, and PAPR represents the peak-to-average ratio of the modulated signal. In this linear PA design, P_{Max} is selected to allow sufficient headroom for linear amplification of modulated signals. In real-world implementations, this P_{Max} is physically realized by properly selecting semiconductor technology and transistor size.

- **Step 2:** *Loadline Selection.* Since the balanced mode requires two amplifier branches to be fully symmetrical, the loadlines of main and auxiliary amplifiers are identically selected ($Z_{\mathrm{M}} = Z_{\mathrm{A}}$). A full power utilization transistor designed in **Step 1** is ideally associated with a unique load impedance for a particular class of PA which generates optimized power and efficiency, which can be determined using load-pull at the operation frequency. However, the linearity is usually not optimal following the conventional load-pull evaluation. Given the fact that PA linearity is the key factor in determining whether a system is compliant to a certain communication standard, the possible impedance selection (at both fundamental and harmonic frequencies) in this design is prioritized for linearity with a meanwhile balance for efficiency, gain, and power.

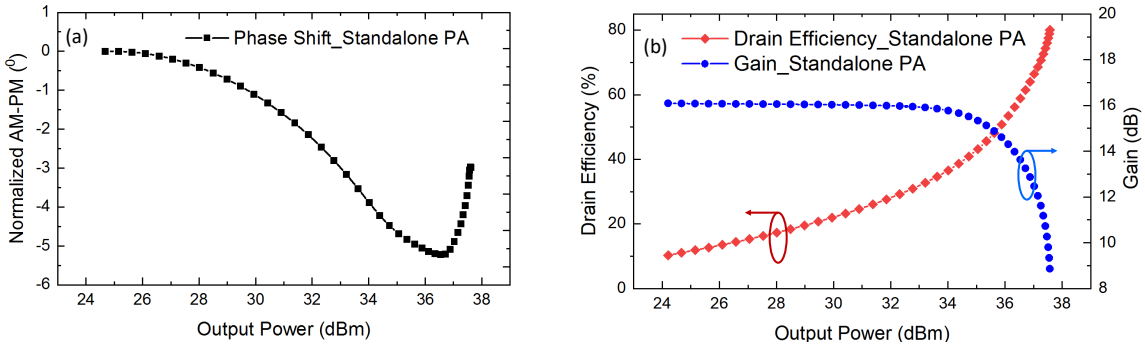
- **Step 3:** *Matching Networks Design.* After determining the optimal loadline, the output

matching network is designed to physically realize the target impedance at both fundamental and harmonic frequencies. It is important to note that the output matching network (OMN) also plays an important role in determining the load modulation behaviors of main and auxiliary PAs in Doherty mode [24], which needs to be co-designed with the coupler-based combiner for achieving efficient and linear performance in Doherty mode. The source impedance can also affect the PA gain and linearity. A conjugate match is desired for maximized gain, while a slight mismatch (if properly designed) can lead to optimized linearity [43]. Therefore, the input matching network design should take into account both aspects, and a compromise is necessary. To enforce the symmetry of balanced mode, the IMN and OMN are designed identically for the two amplifiers.

- **Step 4:** *Bias Selection for Balanced Mode.* In the balanced mode, the two PAs are biased identically for both gate and drain. Therefore, the behavior of the entire balanced amplifier can be treated the same as a standalone PA. In addition to the loadline impedance, the PA linearity profile across the entire power range is also strongly influenced by the gate bias level of the main transistor. Empirically, the PA is biased at Class-AB mode to yield a good balance between efficiency and linearity, and a bias sweep can be performed to eventually determine the value.

- **Step 5:** *Bias Selection for Doherty Mode.* In the Doherty mode, the main and auxiliary amplifiers are biased in Class-AB and Class-C, respectively. The linearity and efficiency are highly dependent on the combination of these two bias voltages, because the turn-on point of auxiliary PA determines the back-off efficiency, while the interaction (i.e., load modulation) between main and auxiliary PAs dominates the AM-AM and AM-PM profiles. Therefore, the bias voltages are carefully selected based on a nearly exhaustive search to identify an optimal combination. If the linearity requirement cannot be met, we need to revisit the loadline selection and conduct the process from **Step2**.

Overall, the design method considers the PA performance of both Doherty and balanced modes in terms of linearity, efficiency, power, gain, etc. It is important to emphasize that if the linearity can be maintained in both modes, the B2D reconfiguration can greatly extend the operation space of the PA into a large variation of load impedance, as the balanced amplifier has been well proven to be insensitive to load mismatch [41, 42].



(a) (b)

Figure 2.4: Simulation results of the standalone PA at 3.5 GHz. (a) Normalized AM-PM. (b) DE and gain.

2.4 Prototype Design and Demonstration

The methodology presented in the above Section 2.3 is implemented to design and realize a prototype of the proposed balanced-to-Doherty mode-reconfigurable PA with high efficiency and enhanced linearity at both balanced mode and Doherty mode. In this design, two 6-W GaN packaged transistors CGH40006P from Wolfspeed are utilized as the power device of a PA operating at a center frequency of 3.5 GHz.

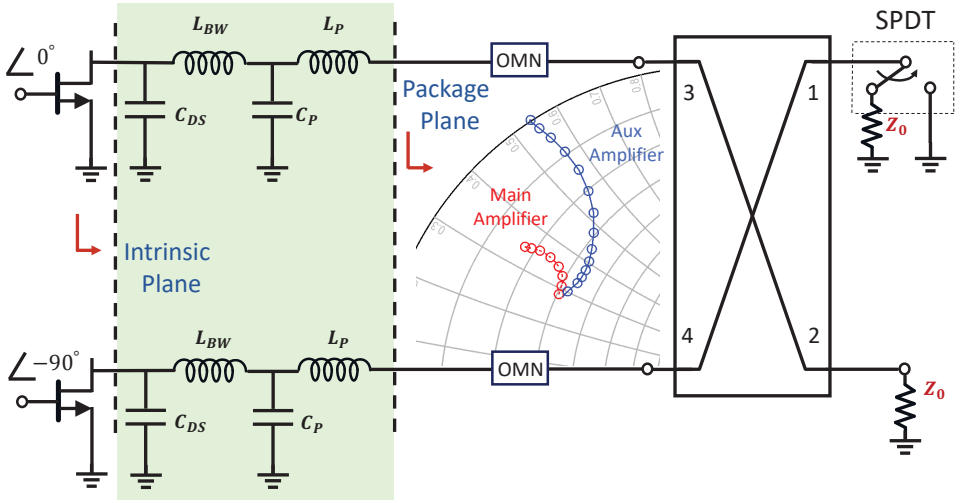
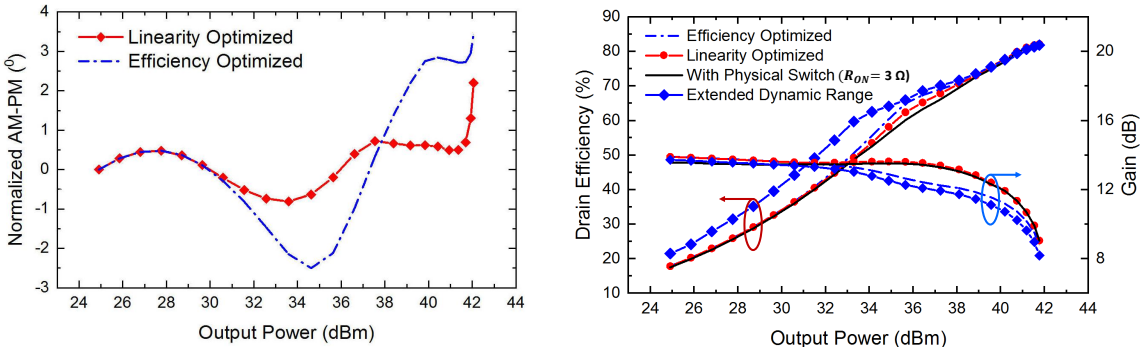


Figure 2.5: Designed output combiner network with device parasitics. The inset Smith chart illustrates the desired dynamic load trajectories at package plane for the main and auxiliary amplifiers.



(a) (b)

Figure 2.6: Linearity- and efficiency-optimized designs of QB-DPA (Doherty mode of B2D PA). (a) Normalized AM-PM. (b) DE and gain.

2.4.1 Design of the Standalone GaN PA

A load-pull simulation was conducted using the selected transistor model with ADS for the standalone PA, in which the device parasitics have been taken into account. At the device package plane, the optimal load impedances for fundamental and second harmonic for this design were chosen to be $13 + j9\ \Omega$ and $j65\ \Omega$, respectively, in order to allow for an optimal linearity to meet

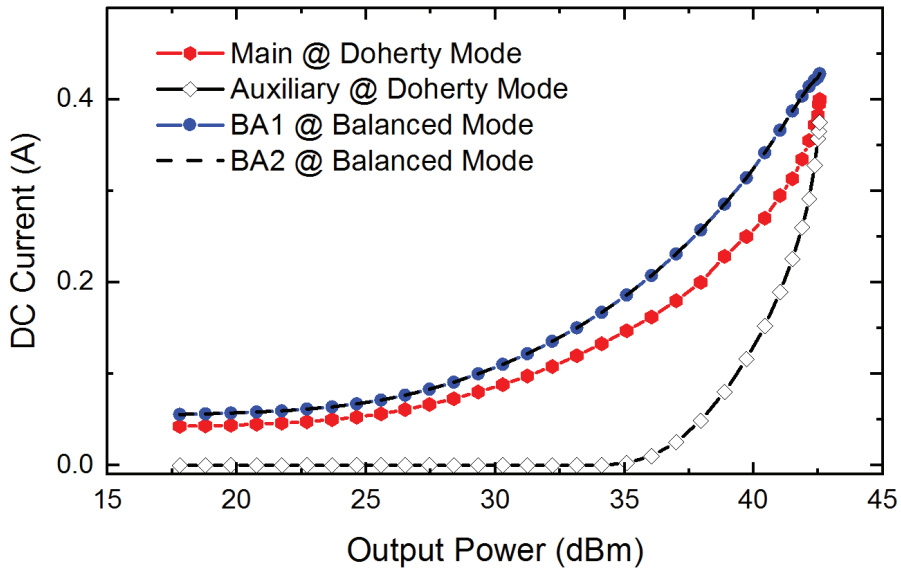


Figure 2.7: Comparison of simulated drain dc currents between the balanced mode and Doherty mode.

the communication standard. To physically realize the target fundamental and harmonic terminations, a 2nd harmonic trap is properly designed together with synthesized fundamental matching using a stepped multi-section transmission-line (TL) matching network which also absorbs the drain bias line.

The design of input matching network (IMN) for the standalone PA is targeted for perfecting the linearity performance without considerably compromising the gain capability. Practically, the desired source impedance of the transistor is extracted from the source-pull simulation, while a slight mismatch is carefully conducted in the IMN design in order to achieve an enhanced AM-PM. Meanwhile, a Class-AB mode of gate bias was selected for achieving a balance of linearity and efficiency consideration. The linearity profile of the designed standalone PA is shown in Fig. 2.4, including a linearized AM-PM profile which is normalized with respect to the small-signal value in Fig. 2.4(a) and a flat AM-AM profile (gain versus output power) in Fig. 2.4(b). The complete design of the standalone PA exhibits an efficient performance at 3.5 GHz with a simulated maximal

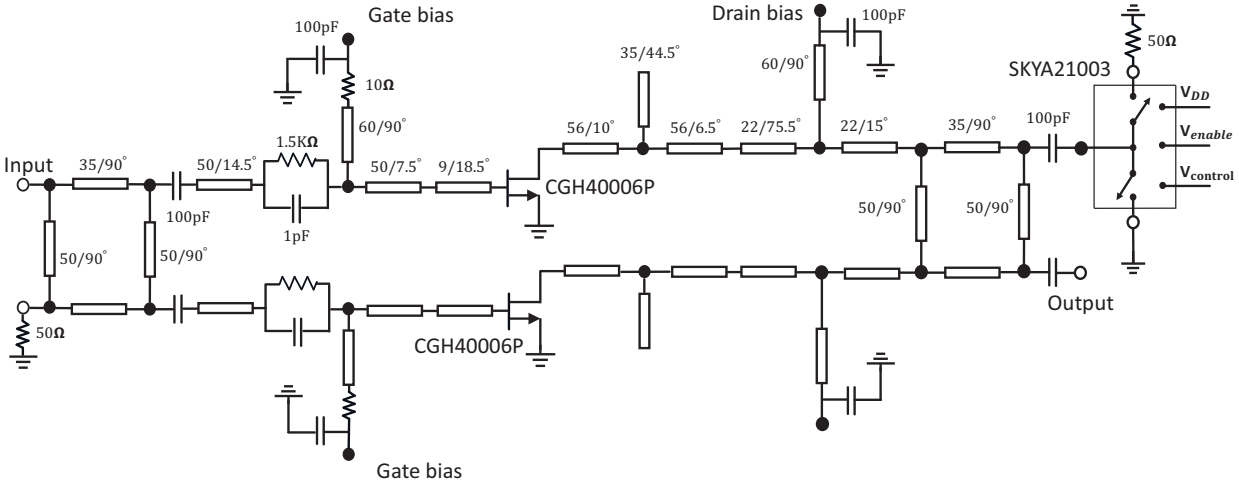


Figure 2.8: Overall schematic of the designed B2D mode-reconfigurable PA with an implemented SOI-based SPDT switch.

drain efficiency (DE) of 80% towards power saturation, as depicted in Fig. 2.4(b).

2.4.2 Design of B2D Reconfigurable PA with Optimized Efficiency and Linearity

Based upon the initial design of the standalone PA, a linear and high efficiency balanced amplifier is formed by coupling two such PAs with 90° of phase offset through two quadrature couplers as the input power splitter and output combiner, respectively. Due to its highly symmetrical characteristics, a balanced PA presents the same linearity characteristic as a single standalone PA with doubled output power.

As the isolation port is short circuited to ground, the operation of the B2D PA is reconfigured to Doherty mode by enabling of the switch. Due to the parasitics of the transistors resulting from the GaN chip and package as shown in Fig. 2.5, the desired load trajectory can deviate from the optimal path, which could be exacerbated especially when the effect of OMN and output combiner are taken into consideration. This may eventually lead to a degradation of linearity and efficiency. In order to perfect the load modulation behavior, a co-design of the OMN and combiner is essential,

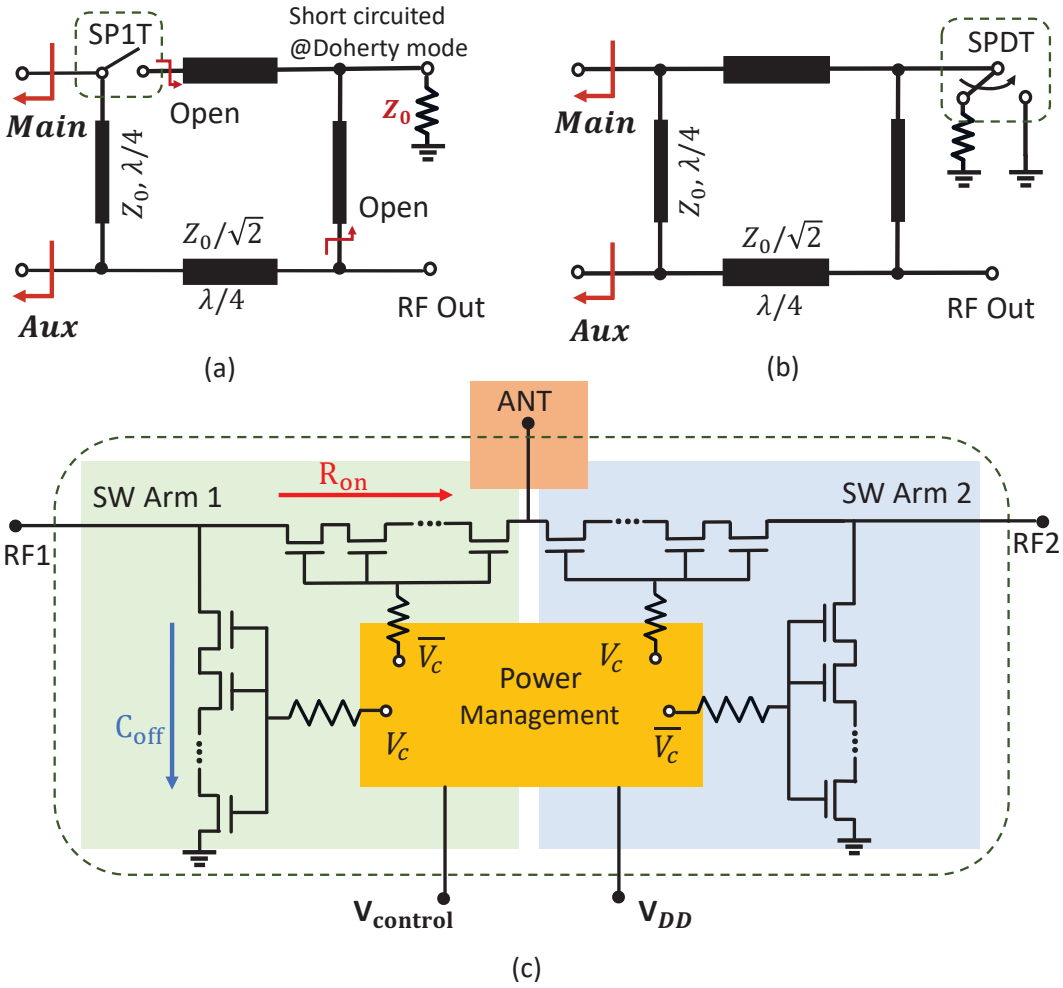
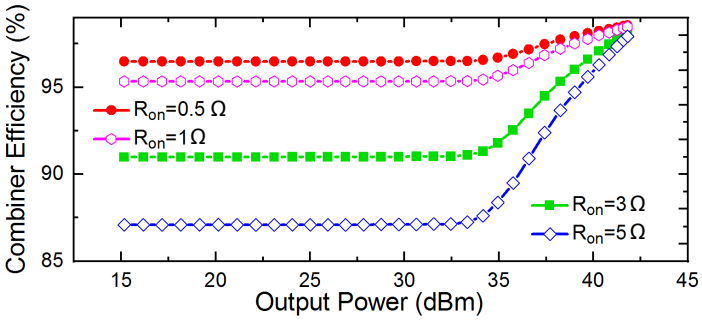


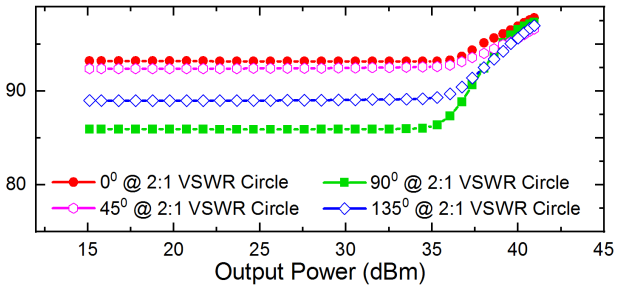
Figure 2.9: Realization of reconfigurability using RF switch(es). (a) Alternative circuit topology with a single switch. (b) Design using a SPDT switch. (c) Schematic of the SOI-COMS SPDT switch.

and a global optimization is performed with the overall circuit schematic following the procedure depicted in Section 2.3. The finalized schematic of B2D reconfigurable PA is shown in Fig. 2.8 including the parameters of all the circuit components.

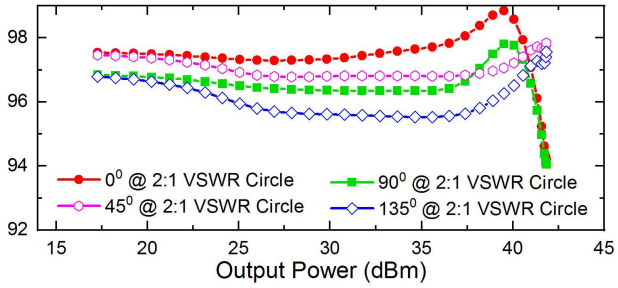
Moreover, an optimal biasing combination of main and auxiliary PAs is carefully chosen for perfecting linearity as exhibited in Fig. 2.6. In this linearity optimized mode,a linear AM-PM can be achieved with $< 2^\circ$ of variation from low power to $P_{1\text{dB}}$ shown in Fig. 2.6(a). Meanwhile, a flat



(a)



(b)



(c)

Figure 2.10: Investigation on output combiner efficiency (insertion loss). (a) Effect of switch R_{on} resistance for shorting the isolation port in Doherty mode. (b) Over $2:1$ VSWR circle in Doherty mode $R_{\text{on}} = 3\ \Omega$. (c) Over $2:1$ VSWR circle in balanced mode.

AM-AM is also realized, as depicted in Fig. 2.6(b), while achieving a saturation efficiency as high as 80% and a 62% efficiency at 6-dB power back-off. The back-off efficiency can be further improved with a different bias setting oriented for optimized efficiency, while slightly compromising the linearity. This mode can be applied when digital pre-distortion (DPD) is available. Meanwhile, an extended 9-dB power back-off dynamic range can be achieved with a properly adjusted drain biases of main and auxiliary amplifiers in QB-DPA mode.

The power-dependent DC currents of main and auxiliary amplifiers are shown in Fig. 2.7. It is observed that the auxiliary current rises sharply after turning on, and it reaches to the same level as the main amplifier current in saturation region. This is mainly due to the strong expansion behavior of GaN device under Class-C bias condition. This is achieved with an equal input power split ratio

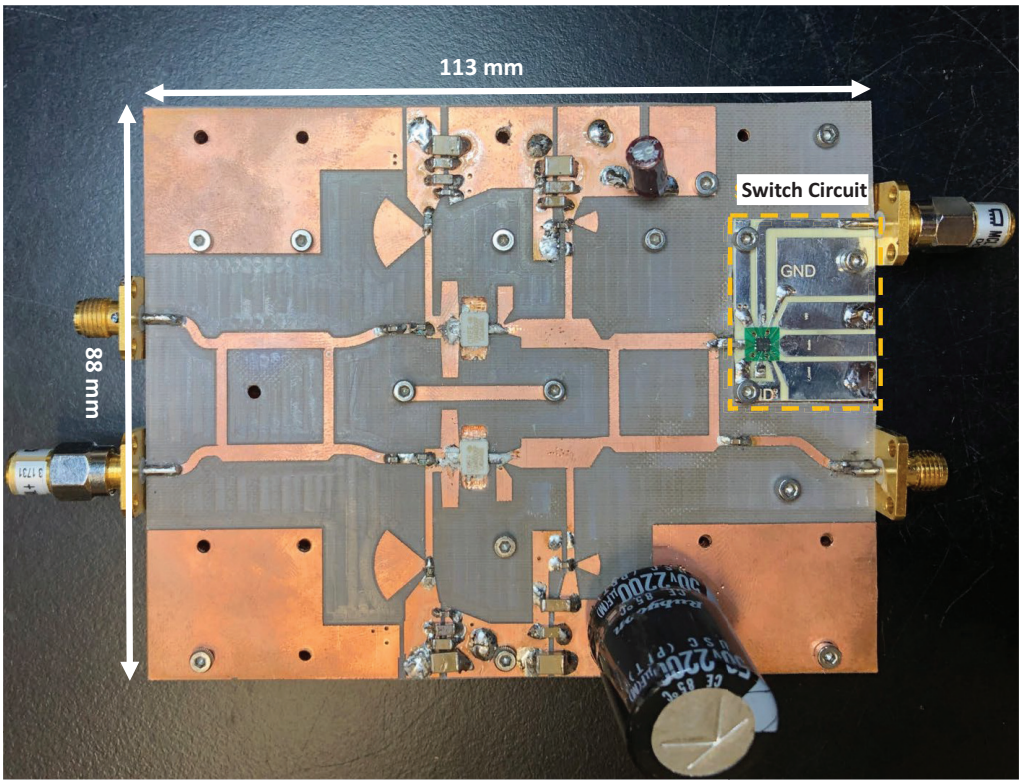


Figure 2.11: Top view of the fabricated circuit board.

using the quadrature coupler. In comparison with balanced mode, the saturation currents are the nearly the same due to the saturation of two sub amplifier, while the QB-DPA mode significantly reduces the current consumption at power back-off.

2.4.3 Qudrature Coupler and RF Switch Implementations

The reconfigurability of this B2D PA is realized with the implementation of a quadrature coupler and an RF switch. For the single-section branch-line hybrid coupler used in this design, there is an alternative topology to realize the switchable B2D combiner, as shown in Fig. 2.9(a), in which a single switch is placed between the main amplifier node and the top quarter-wave branch line. An open circuit needs to be created by the switch to enable Doherty mode. This open circuit can

be converted to short circuit at the isolation node through the top $\lambda/4$ TL, bypassing the 50-Ω resistor and eventually presenting an open circuit towards the RF output port. However, among commercially available switch devices including MEMS, SOI, PIN diode, etc., such a "pure" open circuit can only be realized using MEMS switch which is not widely available now, and the power handling of MEMS devices is a general concern for high-power applications especially under high load mismatch.

Therefore, this demonstration design follows the default topology (Fig. 2.9(b)) where a SPDT switch is placed at the isolation port to alternately enable connection to the 50-Ω loading and ground. A commercial SOI-based RF switch (SKYA21003) is utilized as the SPDT, which consists of three ports: antenna (ANT), RF1, and RF2. As the switch topology shown in Fig. 2.9(c), the ANT port is connected to the isolation port of the output coupler, while the RF1 and RF2 ports are terminated to the 50-Ω loading and ground, respectively. Between ANT and RF ports, two switch arms are connected and controlled by a management unit. In the "ON" state, the switch introduces certain series resistance, i.e., $R_{\rm on}$. To model this effect, a switch model with 3-Ω $R_{\rm on}$ is established based on [44], and the switch is co-simulated with the QB-DPA. It is interesting to note that such an $R_{\rm on}$ does not lead to considerable impact on the QB-DPA performance, as shown in Fig. 2.6(b). The simulation results verifies the feasibility of this default switch design topology. It is interesting to note that, for a typical multi-throw SOI switch, there is typically a shunt arm at each switch port which shorts the node to ground at "OFF" state leading to an improved isolation. Thus, this type of switch cannot offer a complete open circuit at "OFF" state, which cannot be used in the first switchable combiner topology in Fig. 2.9(a).

The overall insertion loss of the quadrature coupler under dynamic PA operation is further studied, as shown in Fig. 2.10. To fully evaluate the switch effect on insertion loss, the combiner loss in the form of passive efficiency is extracted from large-signal Harmonic Balanced simulation. The passive combiner efficiency versus output power of Doherty mode is shown in Fig. 2.10(a). At

saturation power, the value of switch $R_{\rm on}$ has negligible impact to insertion loss, since the isolation port is an electrical "null" as mathematically proven. Meanwhile, the increase of $R_{\rm on}$ leads to higher loss at power back-off. In the mismatch condition as shown in Figs. 2.10(b) and (c), the balanced mode leads to better combiner efficiency compared to Doherty mode.

2.4.4 Fabrication

The overall layout is generated from circuit schematic, and it is modeled using 3D electromagnetic simulator. The EM model is then co-simulated with active components, and the layout is optimized until the co-simulation results match the schematic-only case. The fabricated B2D PA is shown in Fig. 2.11 which is developed on the Rogers 5880 substrate, and the entire PCB is mounted on a copper substrate and fastened using screws. The RF switch module is placed on another small PCB board, and it is mounted on the same copper substrate with RF connection to the isolation node of the output quadrature coupler. By applying different bias setting of the switch control, the ANT port of the SPDT switch can be routed to RF1 (ground) and RF2 (50-Ω termination) alternatively.

2.5 Measurement Results and Analysis

2.5.1 Continuous-Wave Measurement

In the Doherty-mode measurement, the gate bias of the main device is primarily set to -2.6 V in Class-AB in order to improve the linearity at low power range. The auxiliary gate bias voltage is set to -4.5 V for linearity-optimized operation. A proper combination of bias setting can generate complimentary non-linear behaviors of main and auxiliary amplifiers that cancel each other leading to enhanced linearity of the overall Doherty PA, as reported in [45]. In the balanced-mode measurement, the two PAs are biased identically in Class AB with $V_{\rm GS} = -2.5$ V for primarily

optimized linearity.

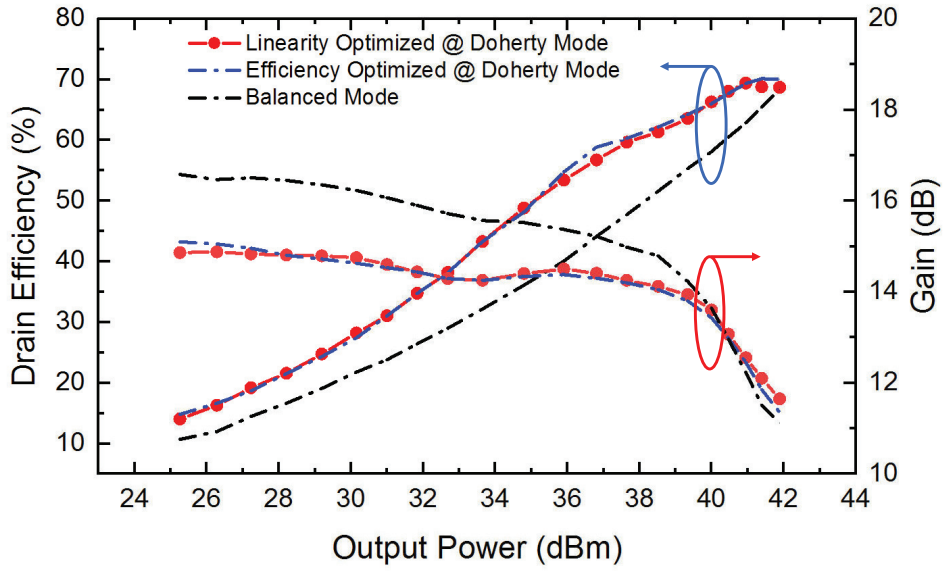
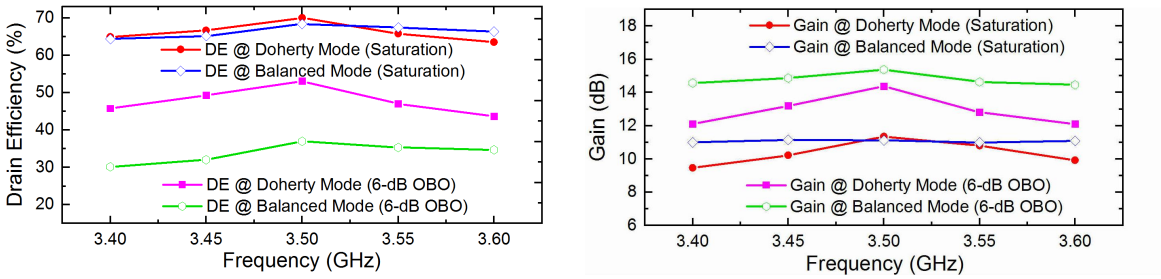


Figure 2.12: Measured DE and gain of Doherty mode and balanced mode.

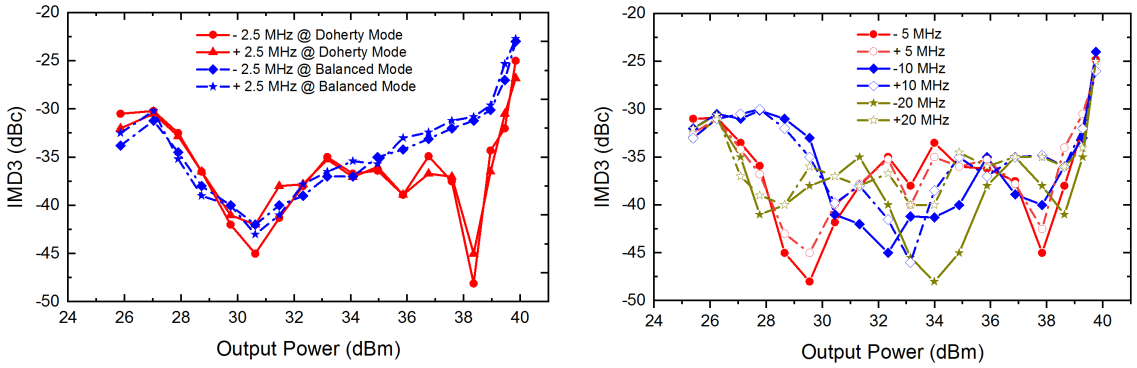


(a) (b)

Figure 2.13: Measured frequency response of (a) DE and (b) gain at saturation and 6-dB OBO for both Doherty and balanced modes.

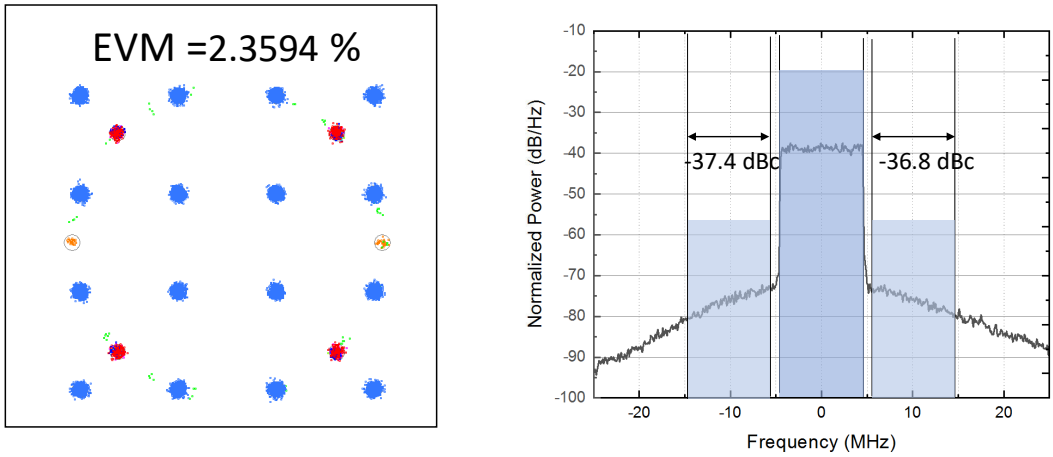
2.5.2 Modulated Measurement for Nominal 50-Ω *Termination*

Fig. 2.12 shows the measured drain efficiency, gain versus the output power at different operation frequencies of the B2D reconfigurable PA, driven by a power-swept Continuous-Wave (CW)



(a) (b)

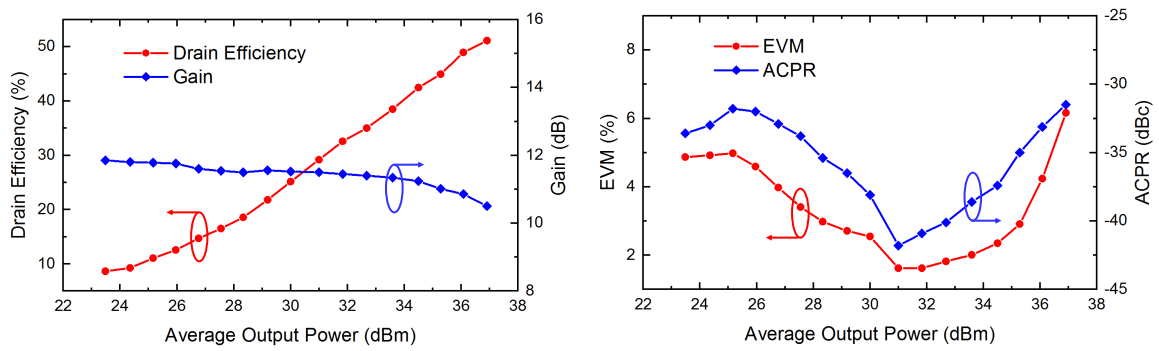
Figure 2.14: Two-tone measurement centered at 3.5 GHz. (a) IMD3 of Doherty and balanced modes with 5-MHz tone spacing. (b) IMD3 of Doherty mode with variable tone spacing.



(a) (b)

Figure 2.15: Measured modulated signal at Pout = 34.5 dBm without DPD. (a) 16-QAM constellation diagram corresponding to an efficiency of 42.4%. (b) Normalized PSD for a 10-MHz LTE signal at 3.5 GHz.

stimulus at balanced mode and Doherty mode respectively. A desired Doherty profile is experimentally obtained in Doherty mode. The measured gain at center frequency 3.5 GHz is around 14 dB at low-power range, and it remains almost flat up to $P_{1\text{dB}}$. Such an AM-AM behavior ensures a good linearity of the Doherty mode. The efficiency and gain of balanced mode are also plotted in Fig. 2.12. A higher gain is achieved in balanced mode given the fact that there is no turn-off



(a) (b)

Figure 2.16: Measured modulated signal versus average output power. (a) DE and Gain. (b) EVM and ACPR.

of auxiliary PA wasting half of the input power at low-power region, which also leads to a better backoff-efficiency behavior at Doherty mode. The measured efficiency at P_{Max} is almost the same for both Doherty and balanced modes at the operating center frequency due to the identical loadline at saturation region. Fig. 2.13 illustrates the frequency response of the B2D across $3.4 - 3.6$ GHz. In Doherty mode, at peak output power, the measured drain efficiency is 64%-70% and the gain is $9.5 - 11.35$ dB, whereas, at 6-dB OBO, the measured gain and drain efficiency are $12.1 - 14.4$ dB and 46%-55%, respectively. The balanced mode experiences a decent performance in terms of drain efficiency and gain as well.

2.5.3 Two-Tone Measurement

The third-order intermodulation (IMD3) is measured with two-tone stimulus at a center frequency of 3.5 GHz to evaluate the linearity of the designed B2D PA. Due to the innate characteristic of soft saturation, the balanced mode presents a slight IMD3 degradation as compared to the Doherty mode near the saturation region, where the Doherty PA experiences a clear gain expansion (see Fig. 2.12). Nevertheless, the overall IMD3 of balanced mode remains below -30 dBc with frequency spacing of 5 MHz for output power lower than 39 dBm, as can be seen from Fig. 2.14(a).

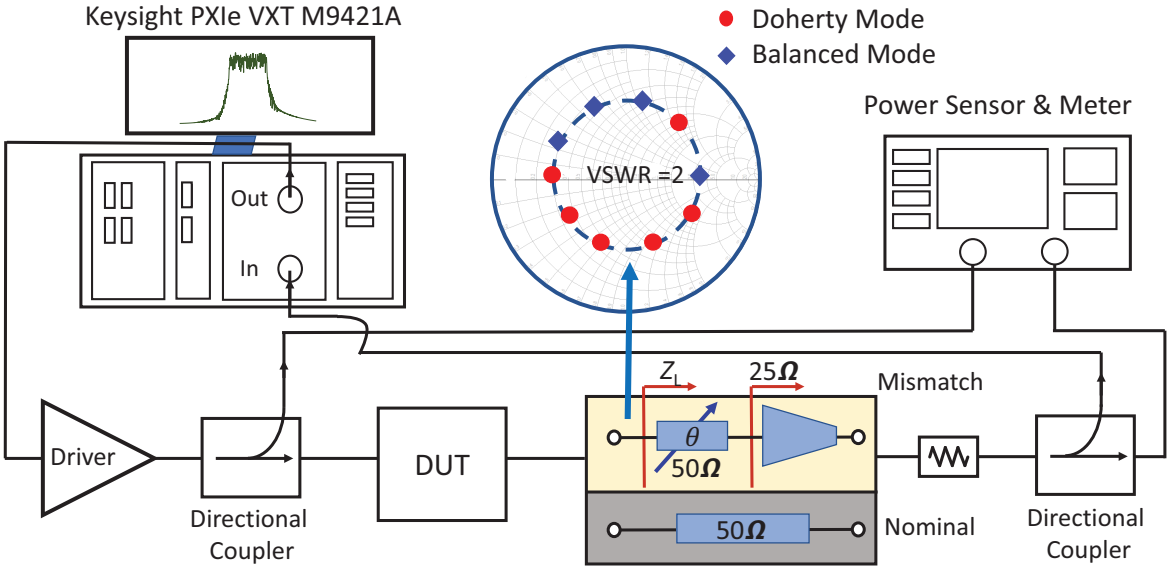


Figure 2.17: An illustrative measurement setup for characterization of the B2D mode-reconfigurable PA under nominal 50-Ω and mismatch ($2:1$ VSWR) loading conditions. Inset Smith chart presents a system-level operation scenario when the B2D PA switches between Doherty and balanced modes to maintain the optimized performance over load variation.

Meanwhile, the Doherty-mode PA maintains a low IMD3 (i.e., < -35 dBc) across a large power range from saturation to 10-dB back-off, which is crucial to achieve linear amplification of high-PAPR modulated signals. As the frequency spacing increases to 10 MHz, 20 MHz and 40 MHz, according to Fig. 2.14(b), a low IMD3 of Doherty mode is maintained with minimum deviation of lower and upper IMD3 components. This indicates that the memory effect is well suppressed when amplifying high-bandwidth signals.

To evaluate the efficiency and linearity performance of the B2D PA in realistic communication scenarios, a modulated measurement using an LTE signal with 10 MHz bandwidth and 8.4 dB PAPR is performed. A Keysight PXIe vector transceiver (VXT M9421) is used as modulated signal generator and analyzer. The generic LTE signal is then boosted by a pre-amplifier (ZHL-5W-422+) to a sufficient level for driving the PA. The measured power spectral density (PSD) and error vector magnitude (EVM) are presented in Figs. 2.15(a) and (b), respectively. The designed

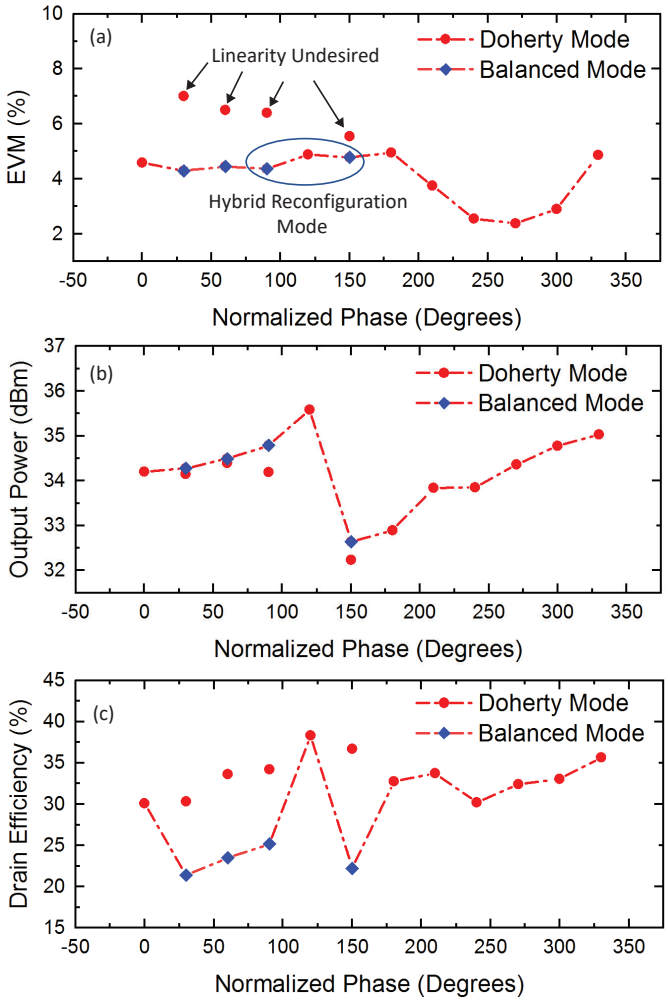


Figure 2.18: Measurement of reconfigurable mode B2D PA under $2:1$ VSWR over entire phase range. (a) EVM. (b) Output power. (c) Average DE.

B2D PA presents an average efficiency of 42.4% and ACPR around -37 dBc at a rated average output power of 34.5 dBm without any DPD applied. A low corresponding error vector magnitude (EVM) of 2.36% is measured in this condition, as shown in Fig. 2.15(b).

The PA is further tested using a power-swept LTE signal with the same modulation, and the drain efficiency and gain versus the average output power are plotted in Fig. 2.16(a). The profile of EVM and ACPR are presented as well in Fig. 2.16(b). It can be seen that the EVM versus P_{out}

profile agrees well with the two-tone measurement when tone spacing is at 10 MHz. Based on the measurement in Fig. 2.16, the designed Doherty mode PA maintains a low EVM below 3.5% and a raw ACPR between -33.8 and -41.8 dBc over a large power range from 27.5 to 35.6 dBm, while the corresponding average efficiency is between 20% and 45%.

This design exhibits a state-of-the-art PA performance as compared to other contemporary linear GaN-based PAs published recently, as listed in Table 2.1. The Doherty mode of the proposed B2D PA offers a very competitive efficiency and linearity at the maximum rated output power, which well verifies the effectiveness of the proposed QB-DPA theory.

2.5.4 Reconfigurable-Mode Measurement under Load Mismatch

To experimentally demonstrate the reconfigurable operation, the designed B2D PA is evaluated with the same LTE modulated signal (used in Sec. 2.5.2) under load mismatch at a constant VSWR of $2:1$. Using the measurement system setup in Fig. 2.17, the PA output is connected to a mismatched load which covers the $2:1$ VSWR circle on Smith Chart with the phase swept at 30° step. This is physically realized using a $2:1$ transformer in series with a series of transmission lines with different electrical lengths.

The Doherty-mode PA is first tested with a constant input driving power of 21 dBm. Fig. 2.18 illustrates the EVM, output power, and efficiency versus the varying phase along the $2:1$ VSWR circle. In Fig. 2.18(a), a low EVM ($< 5\%$) can be achieved for the majority of phases on the $2:1$ VSWR circle with corresponding output power between $32.5-35.1$ dBm. In this prototype demonstration, a $< 5\%$ of EVM is set as the target, while this system benchmark can be re-defined according to specific communication standards. For the rest of phases not meeting the linearity spec, the balanced mode is activated through adjusting the control voltage of SPDT to connect RF2 to a 50-Ω load. As illustrated in Fig. 2.18(b), the balanced mode recovers the linearity of those

phases, exhibiting a $< 5\%$ EVM with a slightly higher maximum linear power compared with the Doherty mode. In terms of the efficiency performance presented in Fig. 2.18(c), the efficiency of Doherty mode slightly degrades compared to nominal 50-Ω condition, while the efficiency is further compromised for linearity when reconfigured to balanced mode. It is important to point out that a failure in linearity usually overwhelms the failure of a communication link, so that a slight compromise of efficiency can be well justified for ensuring the overall quality-of-service (QoS).

In summary, when a practical transmitter system is subject to antenna mismatch, this B2D mode reconfiguration is able to maintain a high PA linearity consistently complying to the particular communication standard while maintaining a stable output power and decent efficiency. More importantly, this mode reconfiguration can be seamlessly implemented without having to physically detect the actual mismatch impedance. This feature is expected to be highly desirable for MIMO and active array applications where the antenna impedance variation is anticipated to be in very rapid time-scale.

Table 2.1: Comparison with State-of-the-Art of Recently-Reported Linear GaN PAs

Ref.	f_0 (GHz)	P_{avg} (dBm)	Mod. BW (MHz)	Average DE (%)	ACPR w/o DPD (dBc)
[24]	5	32	$40/80/120$	42	$-43.8/-44.1/-43.1$
[25]	0.8	33	$20/30/40$	$33.2/30.9/29.6$	$-42.5/-42.3/-40.7$
[26]	2.14	35.5	$5/10/20$	44	$-41.5/-40.8/-40.5$
[46]	7	32	56	41	-36
[47]	2.3	35.2	10	46	-35.6
[48]	3.5	35.8	20	62	-27.9
[49]†	5	36	5	57.8^{*}	-30
[50]	2.0	33	5	54	-30
[4]	7	27.7	20	43	-41
This Work	3.5	34.5	10	42.4	-37

† Measured using two-tone signal with 5-MHz tone spacing. $*$ Maximum CW PAE at an IMD3 of -30 dBc.
$**$ QB-DPA mode.

2.6 Conclusion

In this chapter, a novel B2D mode-reconfigurable PA is proposed and analyzed, which is targeted to maintain high linearity and high efficiency overcoming the load mismatch. It is for the first time theoretically derived that a QB-DPA mode can function equivalently to a standard DPA. Moreover, with an SOI-based SPDT switch, a reconfigurable B2D PA prototype is implemented to verify the proposed concept at 3.5 GHz. In the nominal case where the B2D PA is driven by an LTE modulated signal with 10-MHz bandwidth, the measured PA exhibits -37 dBc ACPR, allowing it to achieve 2.36 % EVM at the maximum P_{rated} = 34.5 dBm without any additional linearization techniques. Meanwhile, when suffering from the load mismatch, the designed B2D PA also demonstrates its resilience and capability of maintaining high linearity and high efficiency over entire Smith Chart at VSWR $2:1$. It is worth mentioning that this switchable B2D PA shows promising potential to extend to broadband implementations due to naturally bandwidth-friendly feature of balanced PA. Furthermore, the unique characteristic of the seamless reconfigurable operation when handling rapid load mismatch makes the proposed technique very suitable for use in the 5G Micro cell and compatible with MIMO antennas and active antenna arrays.

CHAPTER 3: LINEARITY-ENHANCED QUASI-BALANCED DOHERTY POWER AMPLIFIER WITH MISMATCH RESILIENCE THROUGH SERIES/PARALLEL RECONFIGURATION FOW MASSIVE MIMO

[1] As analyzed in the chapter 2, mismatch-recovery DPAs are mainly dependent on the tunable gate bias (input drive adjustment) and mode-reconfiguration (supply voltage modulation) to provide VSWR resilience, which are the general method employed in other researches as well [51, 52]. This chapter introduces a reactive loadline tuning methodology to improve the performance specs both at nominal 50Ω and various VSWR conditions.

3.1 Introduction

The evolution of modern wireless communications, featured as ever-increasing user capacity and spectral efficiency, has triggered the development of advanced modulation techniques, including higher-order quadrature amplitude modulation(e.g.,1024 QAM) and orthogonal frequency division multiplexing (OFDM). These complex modulation schemes have been extensively utilized to increase the bit/symbol rate and mitigate the exacerbating spectrum congestion. Besides the benefits, one of the byproducts is the large peak-to-average power ratio (PAPR) of signals, which require the power amplifiers (PAs) to operate efficiently and linearly across a large power back-off range. The Doherty PA (DPA) has been the most widely adopted technique in the modern wireless communication systems due to its capability of significant back-off efficiency enhance-

[1]This chapter was published as
Haifeng Lyu *et al.*, "Linearity-enhanced Quasi-balanced Doherty Power Amplifier with Mismatch Resilience through Series/Parallel Reconfiguration for Massive MIMO" *IEEE Transaction on Microwave Theory and Techniques)* 69(4) Feb. 2021: 2319-2335.
Haifeng Lyu *et al.*, "Linearity-Enhanced and Highly Efficient Doherty Power Amplifier: 16th High Efficiency Power Amplifier Student Design Competition" *IEEE Microwave Magazine)* 22(10) Sep. 2021: 62-69.

ment [6, 11, 20, 22, 53–59]. Despite the non-linear nature of DPA because of the load modulation, external linearization techniques, such as digital predistortion (DPD), can be applied at the digital backend to ensure a good signal fidelity and to suppress the out-of-band spectrum regrowth for meeting the emission requirements of the emerging wireless communication standards. The recently reported load modulated balanced amplifier (LMBA) [1, 60–67] and quasi-balanced Doherty power amplifier (QB-DPA) in [35, 36, 68] have also been demonstrated as effective platforms to perform load modulation with $\geq$ 9-dB power back-off range.

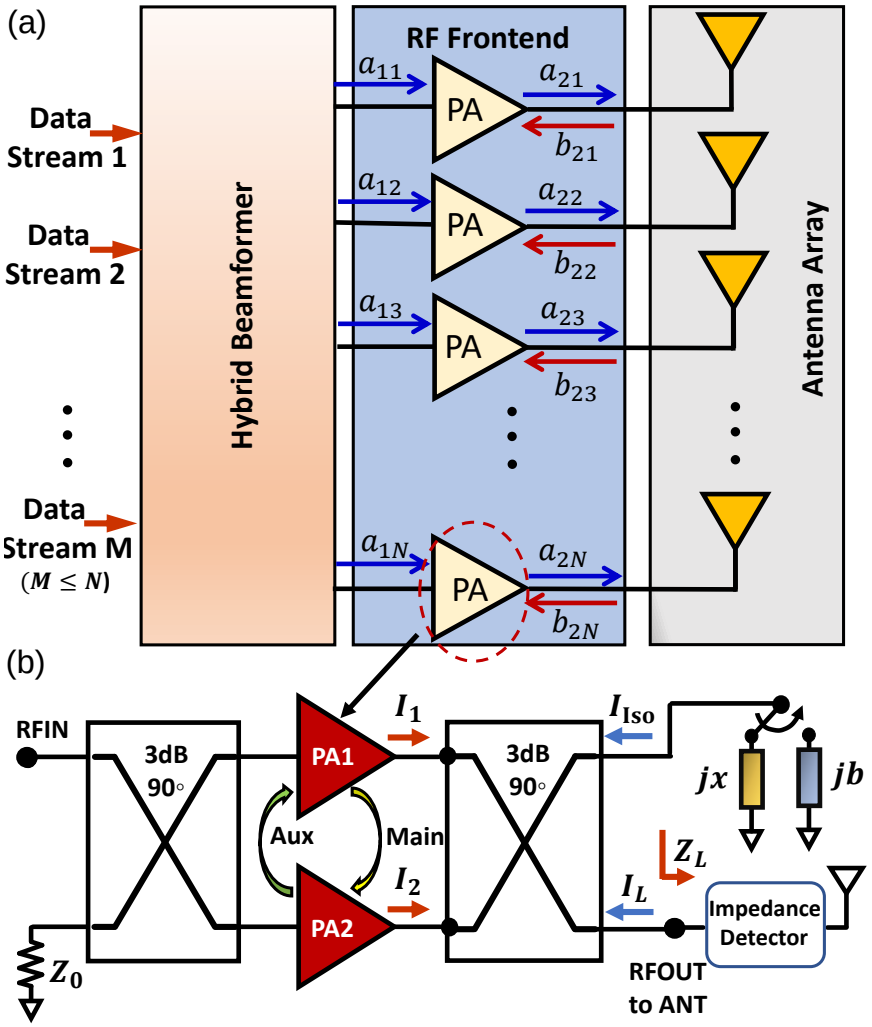


Figure 3.1: Conceptual illustration: (a) MIMO antenna array with mutual coupling affecting the PA loading, (b) proposed reconfigurable series/parallel QB-DPA for load mismatch resilience.

On the other hand, to expand the user channel capacity, radiation coverage, and overall system capability, the spatial multiplexing and combining techniques, i.e., massive multiple input/multiple output (MIMO) based on active antenna arrays, have been widely deployed in the emerging communication systems [69, 70]. Massive MIMO offers significantly enhanced spectral efficiency to accommodate the ever-growing number of subscribers within the highly congested sub-6-GHz spectrum. However, with high density of antennas in a massive MIMO array, the mutual coupling between adjacent elements is sufficiently strong to engender dynamic variations of the antenna impedance at very short beam scanning periods [29, 30, 37], and therefore, the antenna presents a sub-optimal loadline to the associated PA instead of a matched 50-Ω as shown in Fig. 4.1(a). Consequently, the PA as a load-sensitive device can suffer from drastic performance degradation during massive MIMO operations. Moreover, the impedance variations of different antenna elements are inhomogeneous among the entire array, leading to major difficulty and complexity in performing DPD on the large number of massive MIMO PAs [71–74].

Therefore, the PAs in future communication systems are expected to maintain the efficient and linear operations when exposed to substantial load mismatch. Available solutions are mostly based on discrete antenna tuners on mobile platforms and PA-antenna isolators/circulators in the base stations. The former method is bottle-necked by the tuning speed, which is insufficient to track the fast antenna impedance variations in MIMO operations; the later one is bulky, non-linear, expensive, and lossy, inhibiting its feasibility for the massive-scale array integration [28, 31, 32]. Recently, new attempts targeted to recover the mismatch directly at the PA stage have demonstrated promising potential [33, 51, 52, 75]. In [51], a Doherty-like PA use multi-port network synthesis approach to restore the VSWR-induced the degradation by largely compromising output power and linearity, while only selected measurement performance of VSWR points are presented. In [52], a parallel/series switchable DPA is reported with reconfigurable weighting of main/auxiliary-PA currents and phase offset to recover the linearity and efficiency up to $3:1$ VSWR, but this method

has not been systematically and analytically studied. Meanwhile, the low-power implementation in Silicon at mm-Wave frequencies is very different from the prevailing GaN technology mainly adopted in based stations where the massive MIMO is primarily deployed.

The balanced-to-Doherty mode-reconfigurable PA presented in the authors' previous works [35, 68] analytically proves that the QB-DPA functionally is equivalent to an ideal DPA. This discovery enables the PA reconfiguration between Doherty and balanced modes to counteract the performance impairment introduced by load mismatch. However, the efficiency at balanced mode is significantly degraded since no load modulation is performed. In this article, it is for the first time discovered that the QB-DPA is reconfigurable between series mode and parallel mode [13] through reciprocally exchanging the main and auxiliary amplifiers and alternatively terminating the isolation port of the output coupler to a small reactance (close to short circuit) and susceptance (close to open circuit), respectively. Compared with [68], a novel linearity-enhanced combiner is proposed for nominal 50-Ω load to improve the linearity at both series and parallel modes. Further, the reconfiguration between series and parallel operations significantly alleviate the performance degradation (e.g., EVM and DE) when suffering a load mismatch condition. Based on the circuit architecture conceptually illustrated in Fig. 4.1(b), this paper systematically establishes the linearity-enhanced QB-DPA theory for both series and parallel modes with the elegant mathematical symmetry. Moreover, the QB-DPA theory reveals that the series and parallel modes have different sensitivity to load mismatch in a complementary way. Therefore, a hybrid operation over two modes can be utilized to counteract the arbitrary load mismatch up to $2:1$ of VSWR, as normally expected in massive MIMO operations [28,31]. Based on the established theory, a prototype developed at 3.5 GHz demonstrates excellent performance at matched load with the lowest EVM (1.5%) as compared to the state-of-the-art of linear GaN PAs [4,24–26,46], while the efficient and linear DPA operation can be maintained against substantial load mismatch up to $2.5:1$ VSWR.

In realistic system, the PA load impedance can be monitored in real time using the impedance

sensors. For open-loop operation, the optimal setting of DPA mode, gate biasing and impedance can be pre-characterized and stored in a look-up table (LUT), so that the reconfiguration is triggered according to the sensing results and LUT. For close-loop operation, the output signal is also monitored besides the load impedance, and a few iterations may be conducted until the output signal fidelity meets the specs. Once the load mismatch is detected for a specific antenna condition, this mismatch can then be transferred to the local PA load through the interconnections to further process. The length of the feeding line between PA and antenna can induce considerable delay that affects the system response time. However, in the latest massive MIMO systems, e.g., 5G base stations, the antenna array and PAs are integrated within the same module, known as active antenna unit (AAU), where the PA-antenna interconnection is minimized.

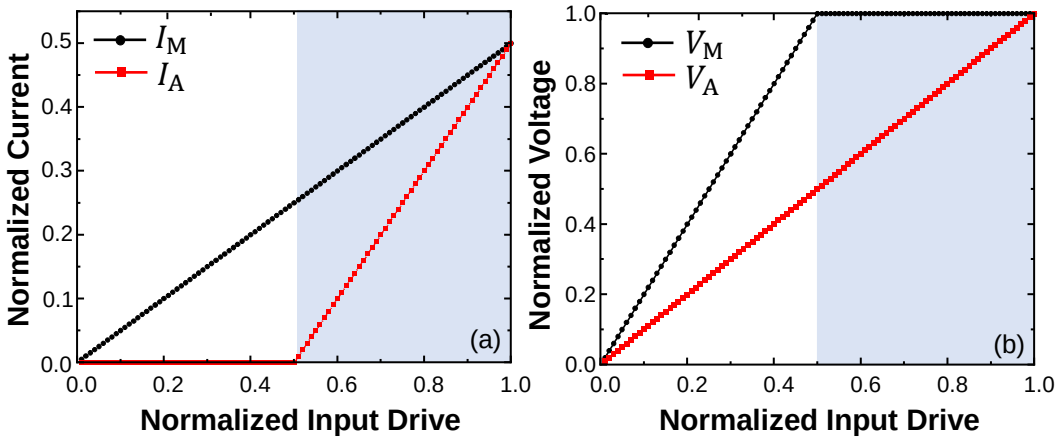


Figure 3.2: Fundamental current and voltage profiles for the ideal DPA.

3.2 Series & Parallel Quasi-Balanced Doherty PA Theory and Linearity Enhancement

The concept of series/parallel reconfigurable QB-DPA through the switching of short-/open-circuit loading of isolation port of the output 90° coupler and the role exchanging of main and auxiliary PAs is presented in the following analysis. Originated from the recently reported ideal QB-DPA [35, 68] (equivalent to the conventional series DPA), this theory is not only generalized by

incorporating an arbitrary reactive isolation-port loading for analog linearization, but also dualized with a symmetrical mode, linearity-enhanced parallel QB-DPA.

3.2.1 Transistor Modeling

The analytical study begins with the transistor model establishment. Following the widely adopted paradigm [76], a simplified but general model is set up with following assumptions.

1. The transistors are considered as piecewise linear transconductive current sources with zero knee voltage and zero output reactance (i.e., package and device parasitics).

2. The transistors' harmonic currents are properly short-circuited to achieve the maximum fundamental efficiency according to the theory [76] and optimal loads are presented to the Class-B and Class-C cells.

Besides the above assumptions, as the driving stimulus, the drain current is defined only with the magnitude information at this stage, the phase relationship will be considered when analyzing the load modulation behaviors. Therefore, the main current can be expressed as

$$I_{\text{main}}(\beta) = \begin{cases} \beta I_{\max} \cos\theta, & -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ 0 & \text{otherwise} \end{cases} \tag{3.1}$$

where β ($0 \leq \beta \leq 1$) is the normalized magnitude of the input voltage drive, and $I_{\max}$ is the maximum channel current that can be supported by the transistor device. Subsequently, by using

Fourier transform, main transistor's fundamental and DC currents are given by

$$I_{\text{main}}[0] = \frac{\beta}{\pi} I_{\max} \tag{3.2}$$

$$I_{\text{main}}[1] = \frac{\beta}{2} I_{\max}. \tag{3.3}$$

Based on the assumption 2), both the main and auxiliary transistors maintain full voltage and current swings at the peak power level. Assuming that the auxiliary transistor remains turned-off in the low-power region ($\beta < \beta_{\text{th}}$) and the same $I_{\max}$ as the main transistor can be achieved at peak-power level, the auxiliary fundamental current can be expressed as follow

$$I_{\text{aux}}[1] = \begin{cases} \frac{\beta - \beta_{\text{th}}}{1 - \beta_{\text{th}}} I_{\max}, & \beta_{\text{th}} \leq \beta \leq 1 \\ 0 & 0 < \beta < \beta_{\text{th}} \end{cases} \tag{3.4}$$

In the conventional DPA configuration, β_{th} defines the threshold for the auxiliary amplifier turn-on point. In practice, different β_{th} values indicate the back-off levels. Specifically, for $\beta_{\text{th}} = 0.5$, it corresponds to a 6-dB power back-off range for a classical DPA. Fig. 3.2 exhibits the current and voltage profiles for an ideal DPA, in which the output RF voltage swings are normalized to V_{DD}.

3.2.2 QB-DPA Theory: Series and Parallel Topologies

A conceptual model shown in Fig. 3.3(a) illustrates the block schematic of the conventional series DPA proposed in [53]. It has been theoretically verified that the generic series QB-DPA in Fig. 3.3(b) is functionally equivalent to the conventional series DPA [35, 36, 68]. This generic QB-DPA architecture is developed from an ideal balanced amplifier with the isolation port of output branch-line quadrature coupler terminated to the ground. Ideally, the main and auxiliary amplifiers

are sized symmetrically inheriting the nature of balanced amplifier topology. The phase of main amplifier in this configuration is in $+90^{\circ}$ offset to auxiliary one, which is necessary to ensure an in-phase combination of main and auxiliary signals at the output. It is interesting to note that the generic series QB-DPA in Fig. 3.3(b) can be treated as a special case, where the isolation port of the quadrature coupler in Fig. 3.3(c) is loaded with a reactive termination, jx.

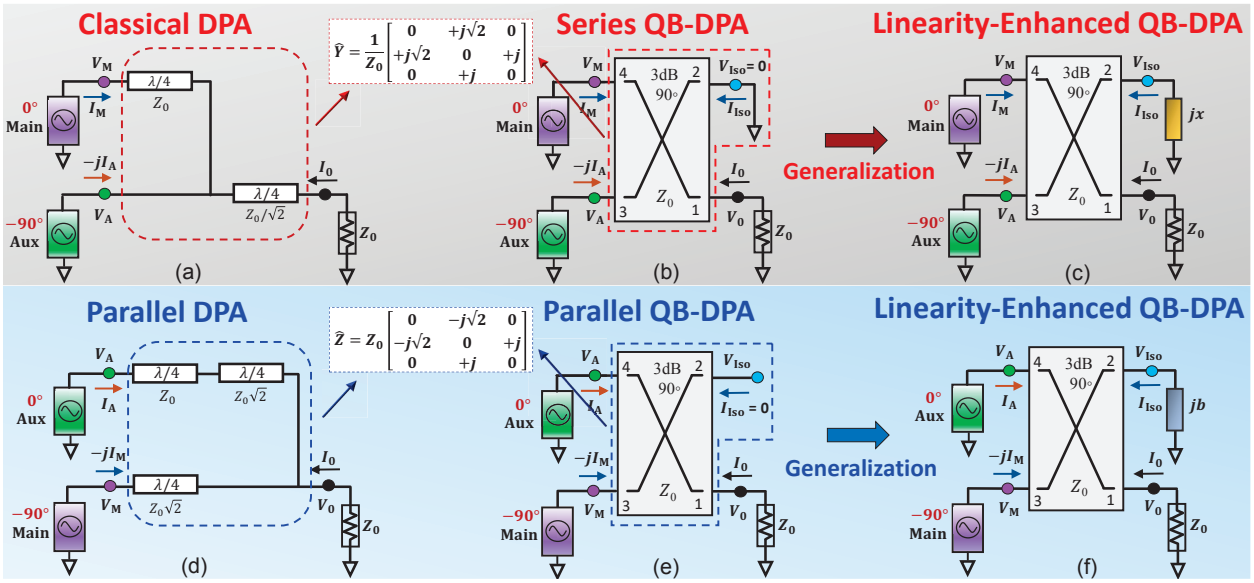


Figure 3.3: Derivation of DPA architectures: (a) classical DPA, (b) series QB-DPA, (c) linearity-enhanced series QB-DPA, (d) parallel DPA, (e) parallel QB-DPA, (f) linearity-enhanced parallel QB-DPA.

To simplify the analysis, the main and auxiliary PA cells are represented with two current sources I_{M} and $-jI_{\mathrm{A}}$, respectively. Therefore, in a system with characteristic impedance Z_0 (non-50-Ω of Z_0 may be used in practical designs as part of transistor matching), the voltage and current

relationship on the output coupler can be expressed as

$$\begin{bmatrix} V_0 \\ -jXI_{\mathrm{Iso}} \\ V_{\mathrm{A}} \\ V_{\mathrm{M}} \end{bmatrix} = \hat{\boldsymbol{Z}}_{\mathbf{coupler}} \begin{bmatrix} I_0 \\ I_{\mathrm{Iso}} \\ -jI_{\mathrm{A}} \\ I_{\mathrm{M}} \end{bmatrix} \tag{3.5}$$

where V_0 and I_0 denote the output voltage and current when the load port Z_0 is matched and $jx = jX/Z_0$ is the normalized reactance value. The generic series QB-DPA in Fig. 3.3(b) can be expressed with Eq. (3.5) as $jx = 0$ with the expression of $\hat{\boldsymbol{Z}}_{\mathbf{coupler}}$ for the ideal 3-dB quadrature coupler matrix as presented blow

$$\hat{\boldsymbol{Z}}_{\mathbf{coupler}} = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} & 0 \\ +j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & +j \\ 0 & -j\sqrt{2} & +j & 0 \end{bmatrix} \tag{3.6}$$

It is further discovered that by leaving the output coupler's isolation port open circuited and swapping the roles of main and auxiliary amplifiers as depicted in Fig. 3.3(e), the ideal balanced amplifier can be converted to another DPA configuration equivalent to the conventional parallel DPA of Fig. 3.3(d) first introduced in [13]. Thus, this new DPA mode is named parallel QB-DPA. Similarly, a generalization in Fig. 3.3(f) with the isolation termination jb under the stimulus current

sources $-jI_{\mathrm{M}}$ and I_{A} can be formulated as

$$\begin{bmatrix} V_0 \\ V_{\mathrm{Iso}} \\ V_{\mathrm{M}} \\ V_{\mathrm{A}} \end{bmatrix} = \hat{\boldsymbol{Z}}_{\mathbf{coupler}} \begin{bmatrix} I_0 \\ -jBV_{\mathrm{Iso}} \\ -jI_{\mathrm{M}} \\ I_{\mathrm{A}} \end{bmatrix} \tag{3.7}$$

Likewise, V_0 and I_0 represent the output voltage and current as well at the nominal load Z_0 condition and $jb = jBZ_0$ denotes the normalized susceptance, where $jb = 0$ corresponds to the generic parallel QB-DPA.

One can find the symmetry from the above equations Eqs. (3.5) and (3.7) that the load-modulation profiles of the main and auxiliary amplifiers for generic series and parallel QB-DPA modes can be obtained as

$$Z_{\mathrm{M,bo}} = 2Z_0 \quad \& \quad Z_{\mathrm{A,bo}} = \infty; \tag{3.8}$$

$$Z_{\mathrm{M,sat}} = Z_0 \quad \& \quad Z_{\mathrm{A,sat}} = Z_0. \tag{3.9}$$

The subscripts “bo” and “sat” specify the variable evaluated at the back-off and saturation regions, while ”M” and ”A” represent main and auxiliary transistors, respectively. Based on the load-modulation behaviors given by the above Eqs. (3.8) and (3.9), it is interesting to note that the generic series/parallel QB-DPA with the isolation port short-/open-circuited is mathematically equivalent to a classical/parallel DPA through the three-port Y/Z-matrix analysis, as depicted in Fig. 3.3.

Furthermore, as derived from Eqs. (3.5) and (3.7), the output voltage V_0 of both generic typologies

($jx = 0, jb = 0$) can be expressed with same form as

$$V_0 = -Z_0 I_0 = -\sqrt{2} I_{\mathrm{M}} Z_0. \tag{3.10}$$

Since the magnitude and phase of V_0 represent the AM–AM and AM–PM of the overall system, Eq. (3.10) reveals a fact that the overall linearity of the QB-DPA is directly determined by the main amplifier's distortion. As reported in [24, 26], the non-linearity of the transistor mainly lies in the AM-PM distortion due to the strongly non-linear parasitic capacitors (e.g., C_{DS}). In other words, if a complementary phase characteristic can be properly designed to compensate for the main transistor's AM-PM behavior, the overall system AM-PM will be improved.

3.2.3 Linearity-Enhanced Series and Parallel QB-DPAs

Multiple methodologies have been proposed to minimize the overall AM-PM distortion through generating a predefined AM–PM characteristic of the DPA combiner that is complementary to the main transistor [24, 26].

As previously mentioned, the generic QB-DPA, which can be switched between series and parallel modes gracefully, presents identical characteristics with standard DPAs in terms of the active load modulation behaviors and inducement of PA non-linearity. In this section, further exploration is presented on the feasibility and versatility of the reconfigurable QB-DPA for linearity enhancement. In order to generate the desired AM-PM at the combiner stage to compensate the main transistor's non-linearity, the quadrature coupler with reactive loading of the isolation port as depicted in Figs. 3.3 is thereby investigated. In the series mode, instead of directly short-circuited to ground, the isolation port is terminated with a small reactance (jx), as shown in Fig. 3.3(c). When the QB-DPA is reconfigured to the parallel mode, the isolation port loading is switched to a small

susceptance (jb) slightly deviated from the ideal open circuit together with the role exchange of main and auxiliary PAs in Fig. 3.3(f).

It is discovered that the reactive loading of isolation port changes the combiner characteristics, which can be leveraged for QB-DPA linearization. From Eqs. (3.5) and (3.7), this load-modulation behaviors for main and auxiliary cells can be obtained as

$$Z_{\mathrm{M_{SE}},\mathrm{bo}} = \frac{2}{jx+1} Z_0 \quad \& \quad Z_{\mathrm{A_{SE}},\mathrm{bo}} = \infty; \tag{3.11}$$

$$Z_{\mathrm{M_{SE}},\mathrm{sat}} = Z_0 \quad \& \quad Z_{\mathrm{A_{SE}},\mathrm{sat}} = Z_0. \tag{3.12}$$

where "SE" specifies the series operation mode.

As for the linearity-enhanced parallel QB-DPA with the susceptance loading of jb, depicted in Fig. 3.3(f), the load modulation seen for the main and auxiliary amplifiers are formed by

$$Z_{\mathrm{M_{PL}},\mathrm{bo}} = \frac{2}{jb+1} Z_0 \quad \& \quad Z_{\mathrm{A_{PL}},\mathrm{bo}} = \infty; \tag{3.13}$$

$$Z_{\mathrm{M_{PL}},\mathrm{sat}} = Z_0 \quad \& \quad Z_{\mathrm{A_{PL}},\mathrm{sat}} = Z_0. \tag{3.14}$$

in which "PL" represents the parallel operation mode.

Comparing two sets of the above equations, i.e., [(3.11), (3.12)] and [(3.13), (3.14)], one can recognize that the load-modulation behaviors of the series and parallel linearity-enhanced QB-DPA are perfectly symmetrical in math, if the values of jx and jb are equalized. This graceful duality can be further verified with the analytical expressions of main and auxiliary voltages, V_{M} and V_{A}, derived from Eqs. (3.5) and (3.7) as well:

$$V_{\mathrm{M_{SE}}} = \frac{2I_{\mathrm{M}} + jxI_{\mathrm{A}} - I_{\mathrm{A}}}{jx+1} Z_0. \tag{3.15}$$

$$V_{\mathrm{A_{SE}}} = -j\frac{I_{\mathrm{M}} - jxI_{\mathrm{M}} + j2xI_{\mathrm{A}}}{jx+1}Z_0. \tag{3.16}$$

$$V_{\mathrm{M_{PL}}} = -j\frac{2I_{\mathrm{M}} + jbI_{\mathrm{A}} - I_{\mathrm{A}}}{jb+1}Z_0. \tag{3.17}$$

$$V_{\mathrm{A_{PL}}} = \frac{I_{\mathrm{M}} - jbI_{\mathrm{M}} + j2bI_{\mathrm{A}}}{jb+1}Z_0. \tag{3.18}$$

It is interesting to note that the formulas of V_{M} and V_{A} not only indicate the retained symmetry between series and parallel modes for their magnitudes, but also reflect the relative phase offsets between the main and auxiliary PAs in both modes, respectively. Moreover, the output voltages of the linearity-enhanced QB-DPAs can be obtained as

$$V_{0_{\mathrm{SE}}} = \frac{-\sqrt{2}I_{\mathrm{M}} - j\sqrt{2}xI_{\mathrm{A}}}{jx+1}Z_0. \tag{3.19}$$

$$V_{0_{\mathrm{PL}}} = \frac{-\sqrt{2}I_{\mathrm{M}} - j\sqrt{2}bI_{\mathrm{A}}}{jb+1}Z_0. \tag{3.20}$$

Again, the symmetrical output voltage profiles unveil a remarkable fact that the equalized reactance/susceptance loading (i.e., $jx = jb$) at the isolation port functions equivalently to engender the predefined AM-PM characteristic in series and parallel linearity-enhanced QB-DPA modes, respectively.

Based upon the solid mathematical derivations of load modulation together with the driving current expressions of Eqs. (3.1) and (3.4), the theoretical models of series and parallel QB-DPAs are established using MATLAB to verify the linearity enhancement in a graphical method. Theoretical

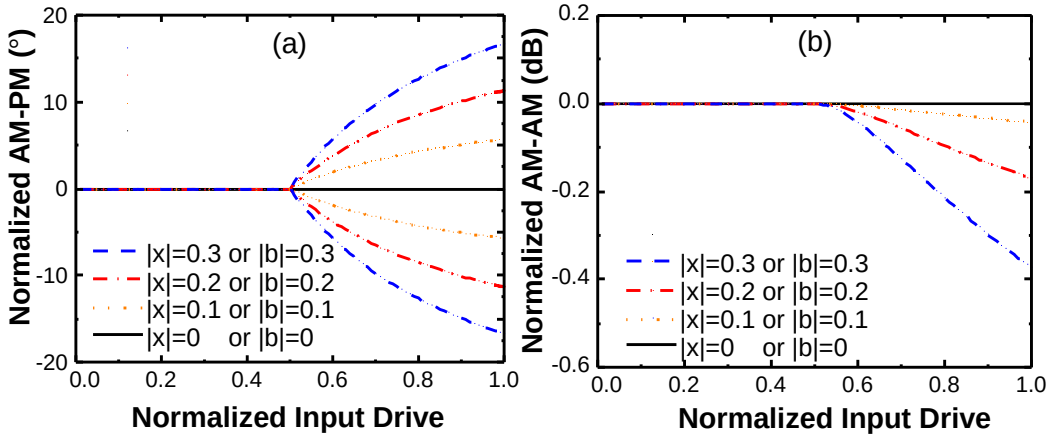


Figure 3.4: Calculated dynamic PA behaviors of the linearity-enhanced architecture: (a) AM-PM profiles, (b) AM-AM profiles.

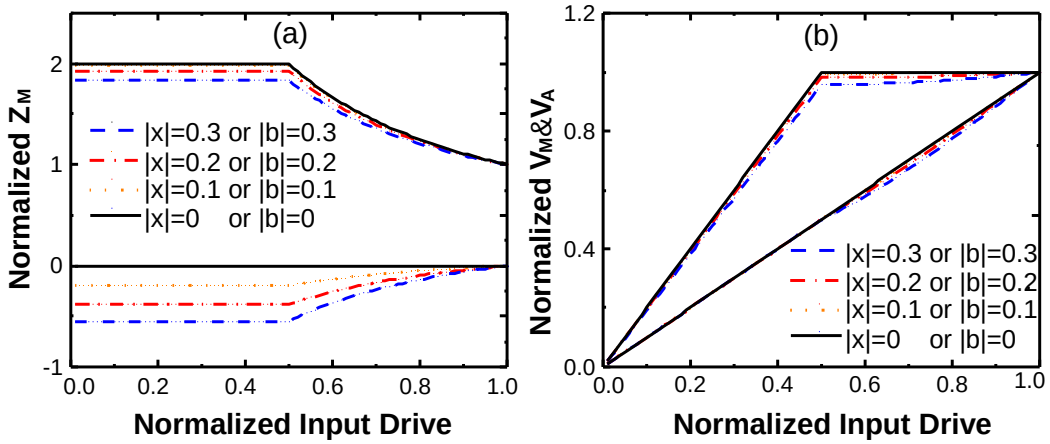


Figure 3.5: (a) Load and (b) voltage behaviors of the symmetric series and parallel QB-DPA modes.

calculation results will be presented to intuitively visualize the theory. Fig. 3.4(a) shows the QB-DPA generates dedicated AM-PM profiles corresponding to different values of $|jx|$ ($|jb|$), these predefined AM-PM characteristics can be used to counteract the phase distortions exhibited by the main transistor. Ultimately, this will lead to an overall linear AM-PM when the two non-linearity mechanisms coexisting in the DPA are complementary. Moreover, as shown in Fig. 3.4(b), the linearity compensation for AM–PM profiles using the reactance (susceptance) loading only induces a limited AM–AM distortion of 0.2 dB when generating a 10° AM-PM profile. This

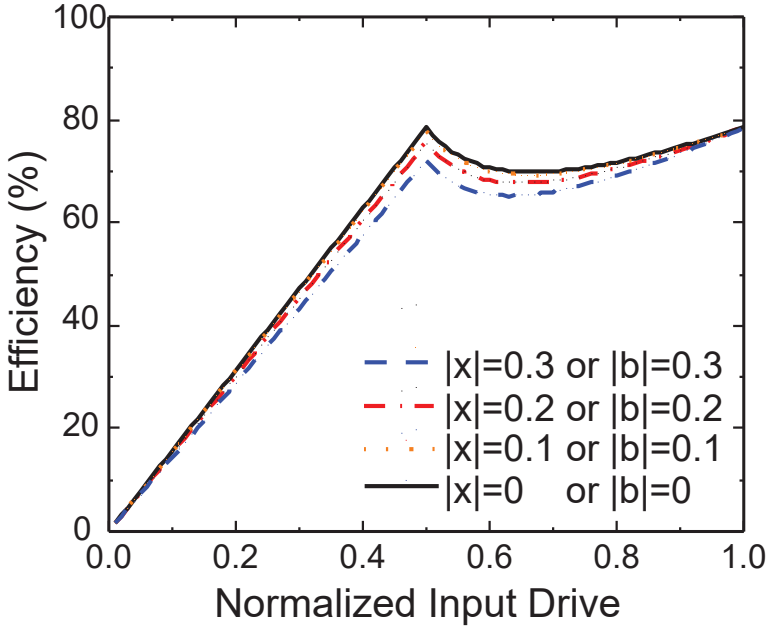


Figure 3.6: Efficiency calculation based on the proposed reconfigurable QB-DPA.

feature significantly alleviates the gain compression during load modulation even for a large 15° AM-PM compensation, exhibiting clear advantage compared to the dB-level gain droop for the same compensation strength as reported in [24, 26].

Fig. 3.5 depicts the calculated drain load and the voltages under various jx (jb) induced phase offset values between 0° and 20°. As for Fig. 3.5(a), the value of jx (jb) may also affect the extent of load modulation. Unlike the generic QB-DPA, the load behavior of the main transistor in linearity-enhanced QB-DPA is not a purely resistive profile, which means the main transistor experiences a continuous load trajectory in Smith chart. This engenders a slight degradation of V_{M} and V_{A} less than V_{DD} over the Doherty region when the jx (jb) is varied, as is presented in Fig. 3.5(b). It is worthy note that the incorporation of the reactance (susceptance) tuning significantly relieves the potential of stronger voltage swing over the entire Doherty region, whereas with minor back-off efficiency sacrifice, and consequently peak efficiency operation is maintained for the Doherty region, as shown in Fig. 3.6. Based on the above analysis, the synthesis network of an AM–PM with

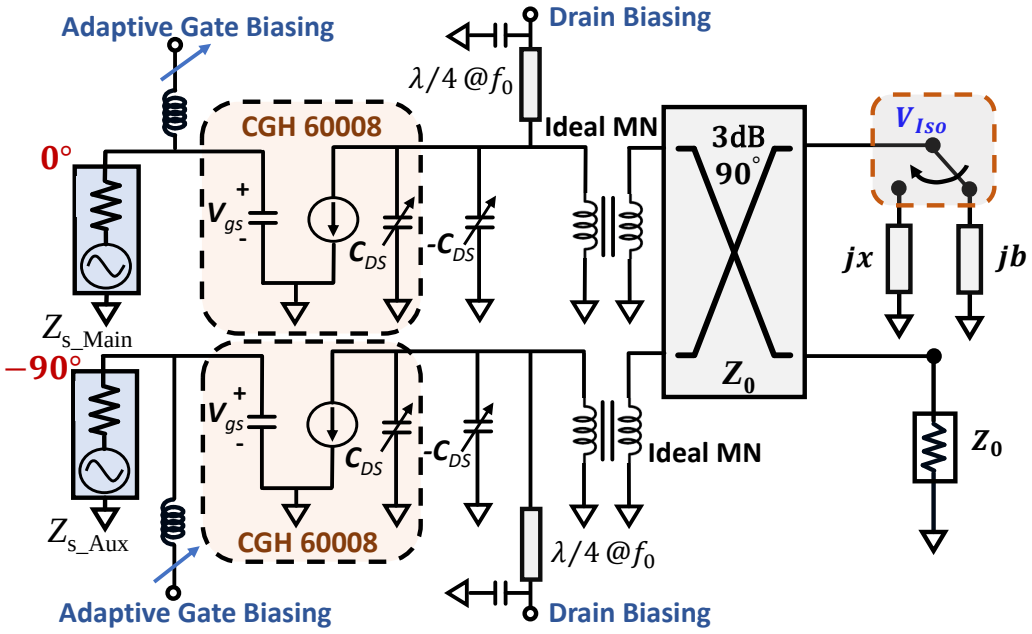


Figure 3.7: Setup of the emulated QB-DPA model.

of up to 15° distortion to compensate for an AM–PM characteristic of the main transistor brings in slight influence on back-off efficiency and limits AM–AM compression to a few decibel (0.4 dB).

In summary, the proposed linearity-enhanced reconfigurable QB-DPA relies on reactance/susceptance loading at the isolation port of the output quadrature coupler, which is a generalized architecture compared with [35, 68] in terms of the performance and design freedom.

3.2.4 Verification using Emulated QB-DPA Model

The derivation described in the previous subsections demonstrates the possibility of utilizing reconfigurable reactive tuning at isolation port to enhance the overall QB-DPA linearity. To verify the theory, an emulated model of linearity-enhanced QB-DPA is established using bare-die GaN transistors, as shown in Fig. 3.7. The CGH60008 model from Wolfspeed is employed for the main and auxiliary transistor cells. The source impedances for main and auxiliary transistors are set

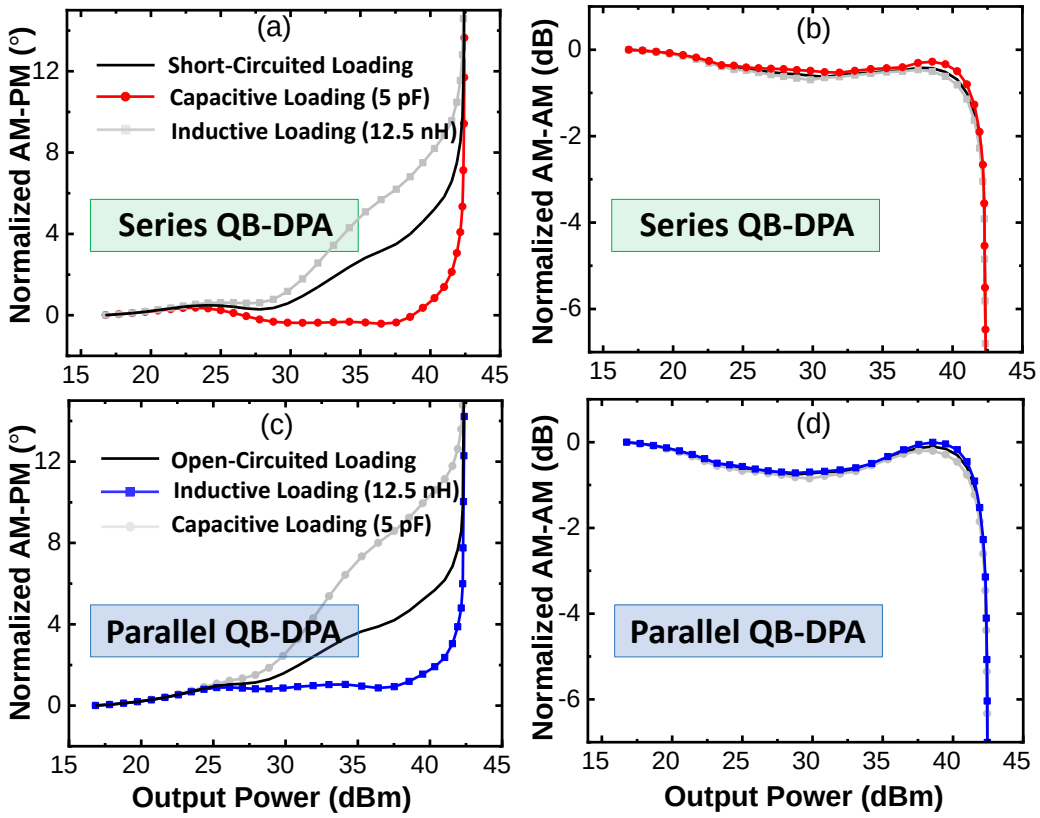


Figure 3.8: Simulated AM-PM and AM-AM profiles of the emulated QB-DPA model in series and parallel modes.

equally based on the source-pull results to suit the symmetry of two modes in reconfiguration. Two ideal transformers are utilized to provide optimal loadline impedances for main and auxiliary transistors, respectively. A compensation $-C_{\mathrm{DS}}$ is utilized to de-embed the parasitic capacitance of the transistor, and the second harmonic impedance termination is set to short circuit by the quarter-wave bias line. Lastly, the reconfigruable reactive loading is connected to the isolation port of the coupler for linearity enhancement.

The main amplifier is biased in Class-AB mode to better mimic the realistic case. Fig. 3.8 depicts the AM–PM and AM-AM behaviors of the QB-DPA emulated mode. The AM-PM variation in-

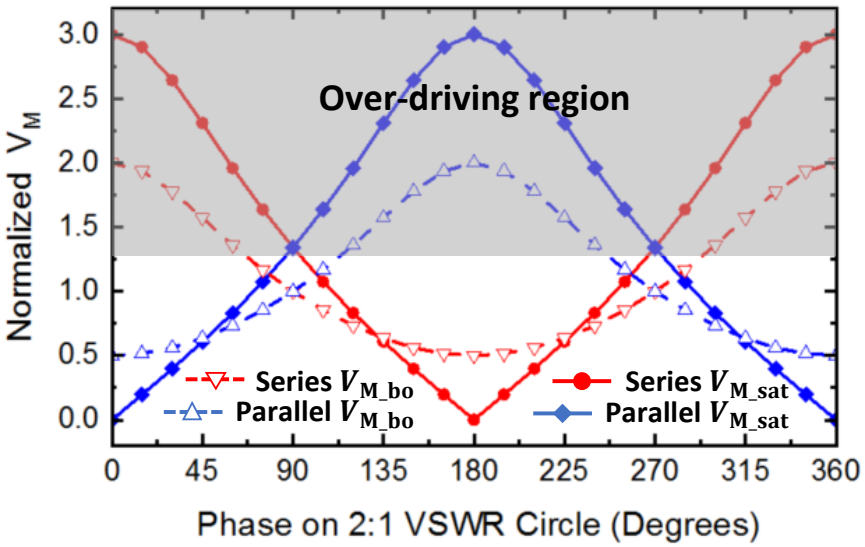


Figure 3.9: Sketch of main amplifier voltage at series/parallel modes due to load mismatch.

duced by (primarily) the power-dependent C_{DS} and (secondarily) the Class-AB biasing of main PA can be substantially restored at load-modulation region. For the series mode shown in Figs. 3.8(a) and (b), a 5-pF capacitor ($x = -0.18$) loading at isolation port offers the optimal compensation effect leading to a flat AM-PM profile with meanwhile negligible impact on AM-AM property. Similarly, for the parallel mode in Figs. 3.8(c) and (d), a symmetric inductance of 12.5 nH ($b = -0.18$) is loaded at the isolation port that leads to the same AM-PM distortion cancellation. The simulation results well agree with the mathematical derivation and results, which solidly prove the theory.

3.3 Series/Parallel Mode Reconfiguration for Mismatch Recovery

The ability for series/parallel reconfiguration of linearity-enhanced QB-DPA can be utilized to counteract the load impedance mismatch effects. As the conceptual illustration depicted in Fig. 4.1(a), antenna impedance variations can severely affect the desired PA operation and degrade its output power, efficiency, linearity, and reliability. In this section, the mechanism of mismatch recovery

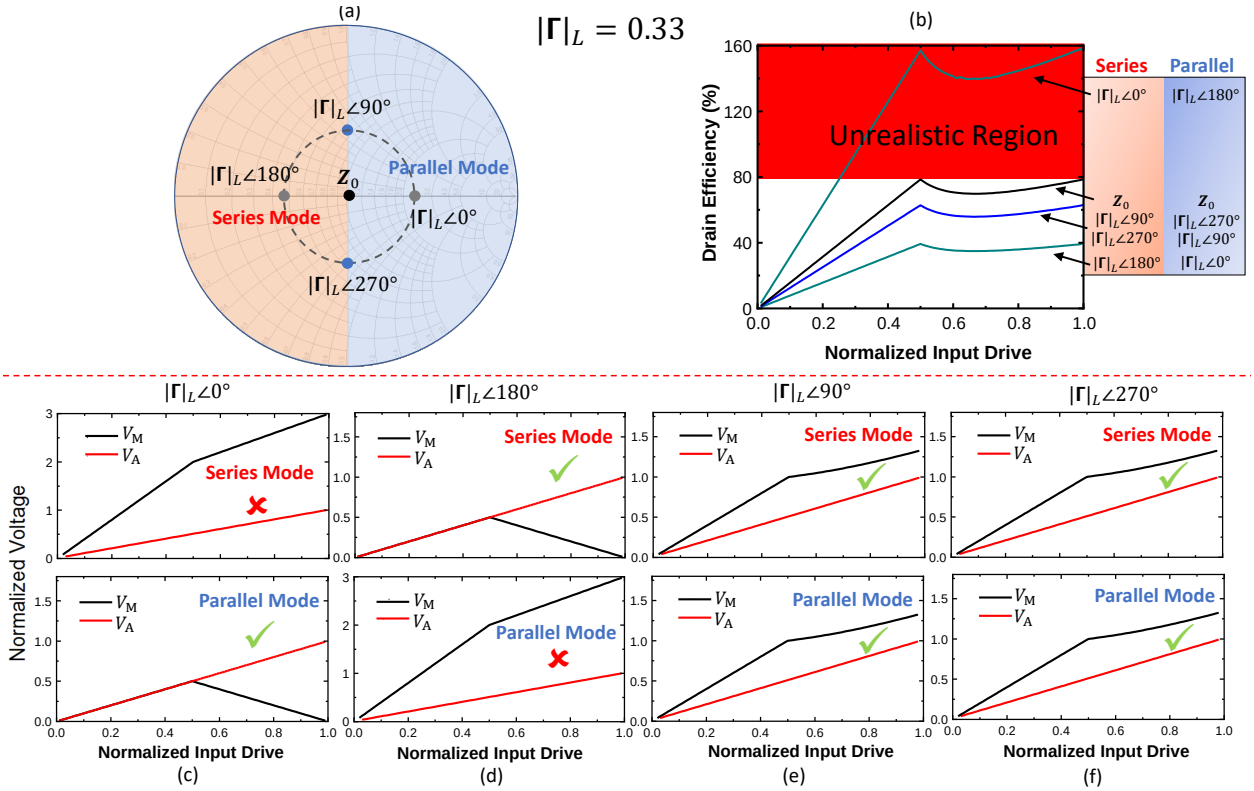


Figure 3.10: Load mismatch analysis: (a) representative cases on VSWR $2:1$ circle, (b) DE profile induced by the mismatched load and voltages at series/parallel modes for the corresponding loads, (c) $|\Gamma_L|\angle 0°$, (d) $|\Gamma_L|\angle 180°$, (e) $|\Gamma_L|\angle 90°$, and (f) $|\Gamma_L|\angle 270°$.

through series/parallel DPA reconfiguration will be analytically formulated for the first time. As a specific case study, the mismatch compensation on the $2:1$ VSWR circle will be presented based on the established theoretical model.

3.3.1 Analysis of Impedance Mismatch Effects

For simplicity, the load-mismatch effects will be first studied for the generic series and parallel QB-DPA modes with ideal isolation-port loading ($jx = 0, jb = 0$), respectively. Using the conditions given by Eqs. (3.5) and (3.7) and based on the voltage/current dependence of load ($Z_{\rm L} = V_0/I_0$),

the load impedances observed by main and auxiliary PAs of series QB-DPA are derived as

$$\begin{aligned} Z_{\mathrm{M_{SE},bo}}(z_{\mathrm{L}}) &= 2z_{\mathrm{L}}Z_0 \ \ \& \ \ Z_{\mathrm{A_{SE},bo}} = \infty; \\ Z_{\mathrm{M_{SE},sat}}(z_{\mathrm{L}}) &= (2z_{\mathrm{L}} - 1)Z_0 \ \ \& \ \ Z_{\mathrm{A_{SE},sat}} = Z_0. \end{aligned} \tag{3.21}$$

where z_{L} denotes the normalized value of Z_{L}. Likewise, for parallel mode, the main and auxiliary impedances due to the current/voltage dependence ($Y_{\mathrm{L}} = I_0/V_0$) are formed as

$$\begin{aligned} Z_{\mathrm{M_{PL},bo}}(y_{\mathrm{L}}) &= 2y_{\mathrm{L}}Z_0 \ \ \& \ \ Z_{\mathrm{A_{PL},bo}} = \infty; \\ Z_{\mathrm{M_{PL},sat}}(y_{\mathrm{L}}) &= (2y_{\mathrm{L}} - 1)Z_0 \ \ \& \ \ Z_{\mathrm{A_{PL},sat}} = Z_0. \end{aligned} \tag{3.22}$$

in which y_{L} represents the normalized value of Y_{L}. The magnitude and phase of main and aux voltages due to load mismatch can be obtained as

$$\begin{aligned} V_{\mathrm{M_{SE}}}(z_{\mathrm{L}}) &= (2I_{\mathrm{M}}z_{\mathrm{L}} - I_{\mathrm{A}})Z_0 \ \ \& \ \ V_{\mathrm{A_{SE}}} = -jI_{\mathrm{M}}Z_0; \\ V_{\mathrm{M_{PL}}}(y_{\mathrm{L}}) &= -j(2I_{\mathrm{M}}y_{\mathrm{L}} - I_{\mathrm{A}})Z_0 \ \ \& \ \ V_{\mathrm{A_{PL}}} = I_{\mathrm{M}}Z_0. \end{aligned} \tag{3.23}$$

Remarkably, the mathematical symmetry between series and parallel modes is derived from the main $\&$ auxiliary voltages (in magnitude) as well as the load modulation behaviors, by exchanging z_{L} and y_{L}. In other words, under the mismatched loads when $z_{\mathrm{L,SE}} = y_{\mathrm{L,PL}} = 1/z_{\mathrm{L,PL}}$, the series and parallel QB-DPA are functionally equivalent. The phase difference of V_{M} and V_{A} between series and parallel modes are due to the interchanged positions of main and auxiliary amplifiers. It is also important to note that the voltage of auxiliary amplifier (V_{A}) is independent to the load mismatch that can be seen from Eq. (4.7), and thus, only the main amplifier of both modes will be analyzed under different load conditions. The V_{M} magnitude over the full VSWR $2:1$ circle of back-off and saturation is illustrated in Fig. 3.9. If an upper limit of $V_{\mathrm{M}} \leq 1.25V_{\mathrm{DD}}$ (slight voltage

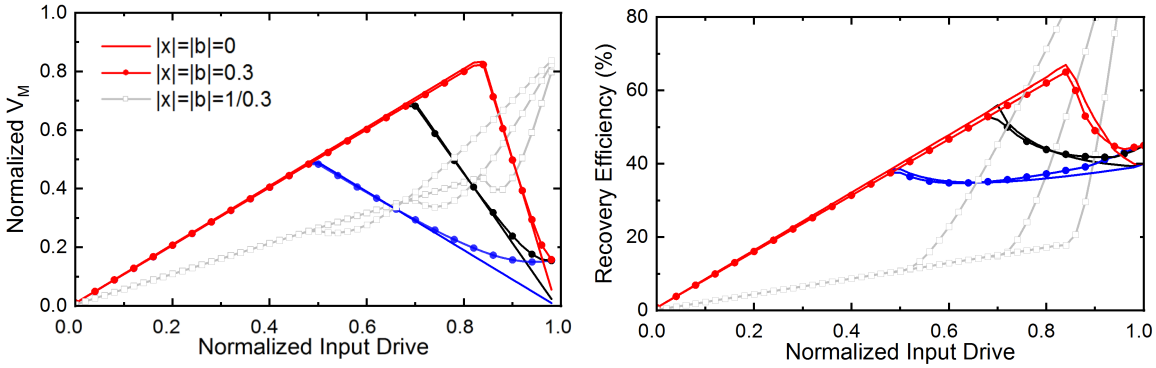
overdriven) is set in order to avoid reliability issues, the mismatch-induced voltage over-driving is inevitable in either series mode (for large $z_{\rm L}$) or parallel mode (for large $y_{\rm L}$). Given the fact that $z_{\rm L}$ and $y_{\rm L}$ ($= 1/z_{\rm L}$) normally complement each other, a reconfiguration between series/parallel modes in different mismatched load can maintain the main amplifier voltage below the highest acceptable value, i.e. $1.25V_{\rm DD}$, as indicated by the unshaded region of Fig. 3.9.

Overall, to avoid the voltage over-driving of the main amplifier as indicated by Eq. (4.7), the QB-DPA should operate in series mode for the left half plane of Smith chart, while the parallel mode is desired in the right half, as illustrated in Fig. 3.10(a). To better present the load modulation of both modes under mismatch, the DPA operation behaviors are extracted using the theoretical model for several special and representative loads on the $2:1$ VSWR circle, indicated in Fig. 3.10(a). The associated efficiency profiles of these four sample cases are plotted in Fig. 3.10(b). The reflection coefficient of load is represented as $\Gamma_L = |\Gamma_L|\angle\phi$, where $|\Gamma_L|$ = 0.33 and $\phi \in [0°, 360°]$.

(1) *Resistive Loads*: For the load impedance corresponding to $\Gamma_L = 0.33\angle 0°$, i.e., $z_{\rm L} = 2$, $|V_{\rm M}|$ of the series mode exceeds the predefined limit and reaches to $3V_{\rm DD}$, shown in Fig. 3.10(c). This leads to hard compression of the PA, which strongly degrades the fidelity of waveform for radio transmission and causes reliability issues such as breakdown of the main device. However, if the QB-DPA is reconfigured to parallel mode at $z_{\rm L} = 2$, $|V_{\rm M}|$ can be well maintained below $V_{\rm DD}$, as shown in shown in Fig. 3.10(c), because of the respective $y_{\rm L} = 0.5$ applied to the $|V_{\rm M_{PL}}|$ expression in Eq. (4.7). For the symmetric resistive load, i.e., $z_{\rm L} = 0.5$ and $\Gamma_L = 0.33\angle 180°$, the series mode is selected in which the main voltage $|V_{\rm M}| < V_{\rm DD}$ is enforced for the entire operation region, as depicted in Fig. 3.10(d).

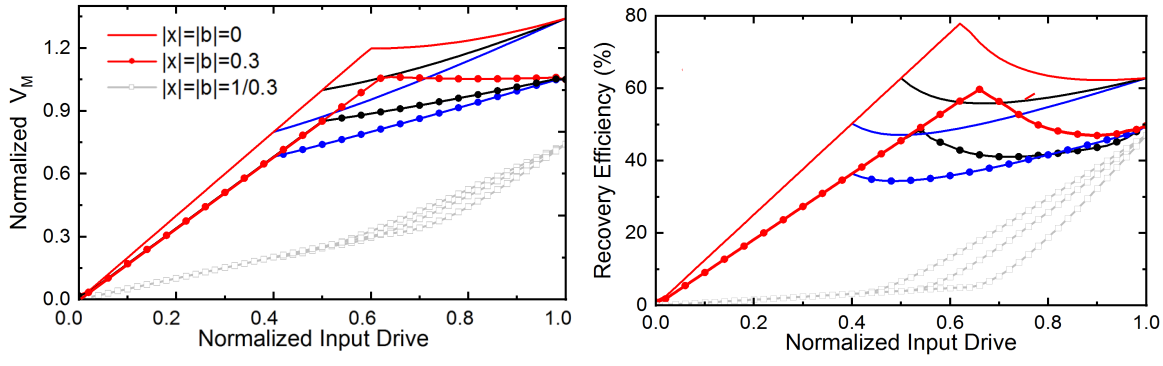
(2) *Complex Loads*: For the conditions of $\Gamma_L = 0.33\angle 90°$ and $\Gamma_L = 0.33\angle 270°$, which correspond to the two reactive points $z_{\rm L} = 0.8 + j0.6$ and $z_{\rm L} = 0.8 - j0.6$, the main voltage profiles of series mode are the same for both loads, as shown in Fig. 3.10(e) and Fig. 3.10(f),

respectively. Meanwhile, the $|V_{\mathrm{M}}|$ increases beyond V_{DD} after the auxiliary amplifier is turned on, but it remains $< 1.25V_{\mathrm{DD}}$ towards the peak power. By replacing z_{L} with y_{L}, the above analysis can be repeatedly applied to the parallel mode. As a result, either series or parallel mode can be selected for these two sample complex loads, which are actually on the boundary of triggering mode reconfiguration as indicated by Fig. 3.10(a).



(a) (b)

Figure 3.11: Illustration of (a) voltage and (b) efficiency recovery for $\Gamma_L = 0.33\angle 0°$ at parallel mode and $\Gamma_L = 0.33\angle 180°$ at series mode, respectively.



(a) (b)

Figure 3.12: Illustration of (a) voltage and (b) efficiency recovery for $\Gamma_L = 0.33\angle 90°$ and $\Gamma_L = 0.33\angle 270°$ at both series and parallel modes.

In addition to the voltage profiles, the symmetry between series and parallel modes is reflected with calculated efficiency in Fig. 3.10(b) as well. The efficiency can exceed the 100% which is

realistically impossible due to the unlimited voltage over-driving (in theoretical model) in certain load conditions, such as $Z_{\rm L} = 2Z_0$ for series mode and $Y_{\rm L} = 2Y_0$ for parallel mode. As a result, the selection of PA mode in a specific load condition should be prioritized for maintaining a non-over-driven $|V_{\rm M}|$. This is depicted with green tick in Fig. 3.10(c)-(f) as well, where for complex loads, both modes can be activated in view of the threshold of $|V_{\rm M}|$. It is also interesting to note that, in both of the series & parallel configurations, $|V_{\rm A}|$ remains below than $V_{\rm DD}$ and is independent to the load mismatch, as verified in Eq. (4.7).

3.3.2 Performance Enhancement for Mismatch Conditions: Analog Approach

As discussed in the above Subsec. 3.3.1, series/parallel mode reconfiguration can be leveraged to avoid the over-driving of the main amplifier device, but the efficiency is considerably degraded, especially for the resistive loads as shown in Fig. 3.10(b). It is discovered that such a degradation can be mitigated through changing the gate bias of auxiliary amplifier and reactance/susceptance loading of the coupler at output. Expanding the ideal series/parallel modes in mismatch conditions described in Eqs. (3.21)-(4.7), the detailed theoretical derivations with jx (jb) loading are derived and provided in the Appendix.

Graphical illustrations in Figs. 3.11 and 3.12 describe the effects of auxiliary gate biasing and jx (jb) loading on the QB-DPA operation under mismatch conditions. For the resistive mismatched loads, parallel mode for $z_{\rm L} = 2$ ($\Gamma_L = 0.33\angle 0°$) and series mode for $y_{\rm L} = 2$ ($\Gamma_L = 0.33\angle 180°$) are selected for avoiding the over-driving. With the ideal gate bias setting (corresponding to the driving currents in Figs. 3.2 (a)), the auxiliary amplifier turns on when the voltage swing of main amplifier is only half of saturation, while the load modulation further degrades the RF voltage to zero towards the maximum input driving level. Consequently, as indicated by the blue lines in Figs. 3.11(a) and (b), the overall DPA efficiency remains low. By increasing the auxiliary threshold

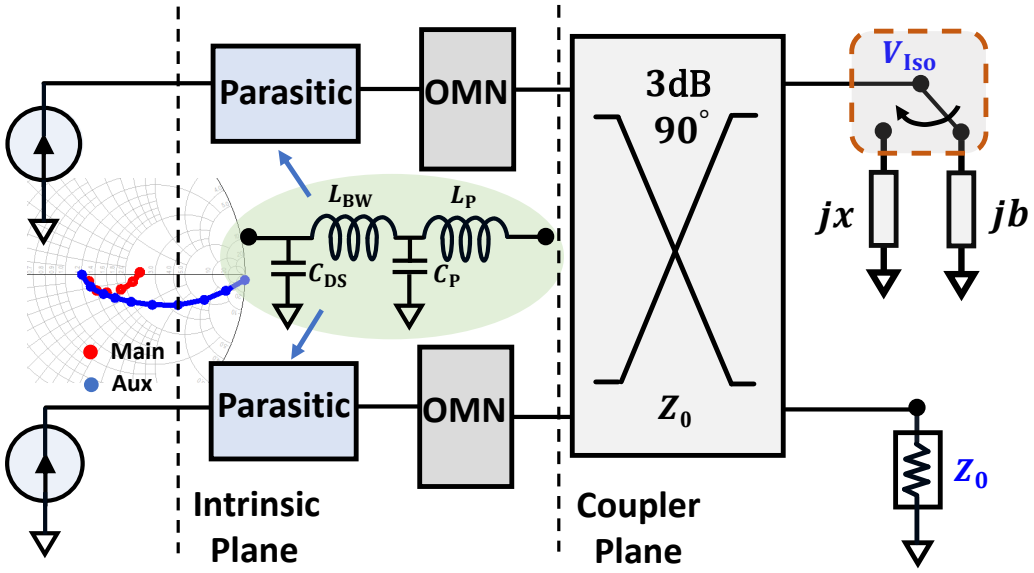


Figure 3.13: Symmetrical series and parallel load modulation behaviors at device plane in realistic design.

(late turn-on), i.e., β, the main amplifier voltage can continue increasing towards the full saturation, leading to a enhanced efficiency (i.e. $> 60\%$) over the entire dynamic range, as indicated by the red lines in Figs. 3.11(a) and (b). Moreover, an appropriately small reactance (susceptance) at isolation port can be utilized to further shape the main voltage and efficiency profiles of series (parallel) mode, but an excessively large jx (jb) can lead to failure of the load modulation, as illustrated in in Figs. 3.11(a) and (b).

For the complex mismatched loads of $z_{\mathrm{L}} = 0.8 \pm j0.6$, the main voltage is slightly over-driven for ideal series/parallel QB-DPA mode, i.e., $|V_{\mathrm{M}}| = 1.25|V_{\mathrm{DD}}|$ around saturation point. Though this is possibly tolerable with harmonic tuning, the reactance/susceptance loading at isolation port can be leveraged to mitigate this over-driving issue, as depicted in Fig. 3.12(a). In series mode for example, by setting $|x| = 0.3$ and slightly increasing the turn-on threshold to $\beta = 0.6$ as the red dotted line shown in Fig. 3.12, the profile of $|V_{\mathrm{M}}|$ can be flattened throughout the load-modulation region and maintained below $|V_{\mathrm{DD}}|$, leading to enhanced QB-DPA efficiency of up to

60%, correspondingly. Due to the symmetrical distribution of the complex loads in Smith chart, the effects of the performance recovery is identical for $\Gamma_L = 0.33\angle 90°$ and $\Gamma_L = 0.33\angle 270°$, while either series or parallel mode can be selected with the same performance.

To sum up, it is proved feasible to exploit adaptive gate biasing synthesis of auxiliary amplifier in conjunction with reactance (susceptance) loading at isolation port for compensating the efficiency and linearity under certain extent of load mismatch, e.g., VSWR $2:1$ loads. It is also important to point out that this quasi-short/quasi-open loading resonates perfectly with the linearity-enhanced QB-DPA theory presented in previous section. In practical designs, the jx (jb) loading and gate biasing can be utilized as tuning knobs for optimizing the efficiency and linearity for both matched and mismatched conditions.

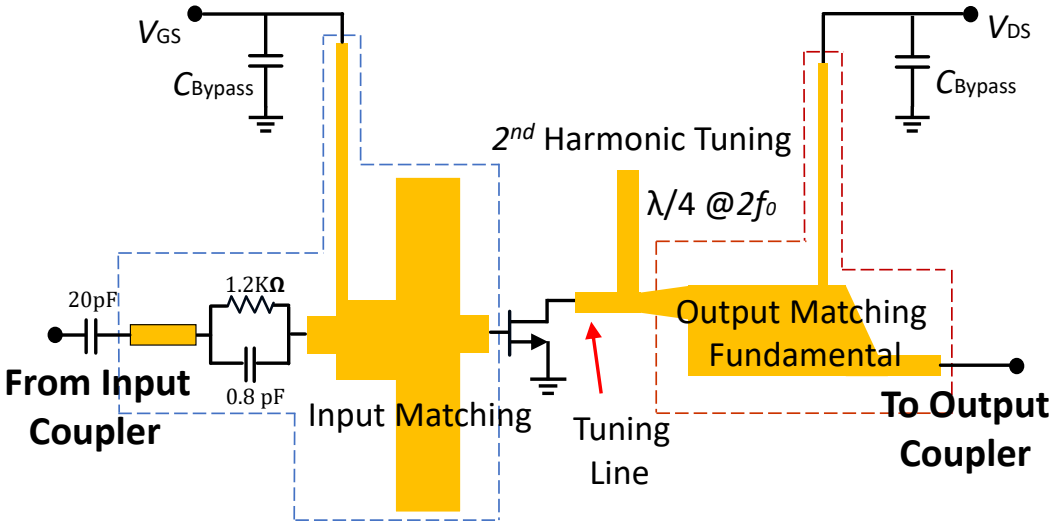


Figure 3.14: Schematic of the designed IMN and OMN of standalone PA.

3.4 Prototype Design and Demonstration

Based on the linearity-enhanced QB-DPA theory and the mismatch-resilient series/parallel mode reconfiguration, the practical design methodology is presented. A physical prototype is designed

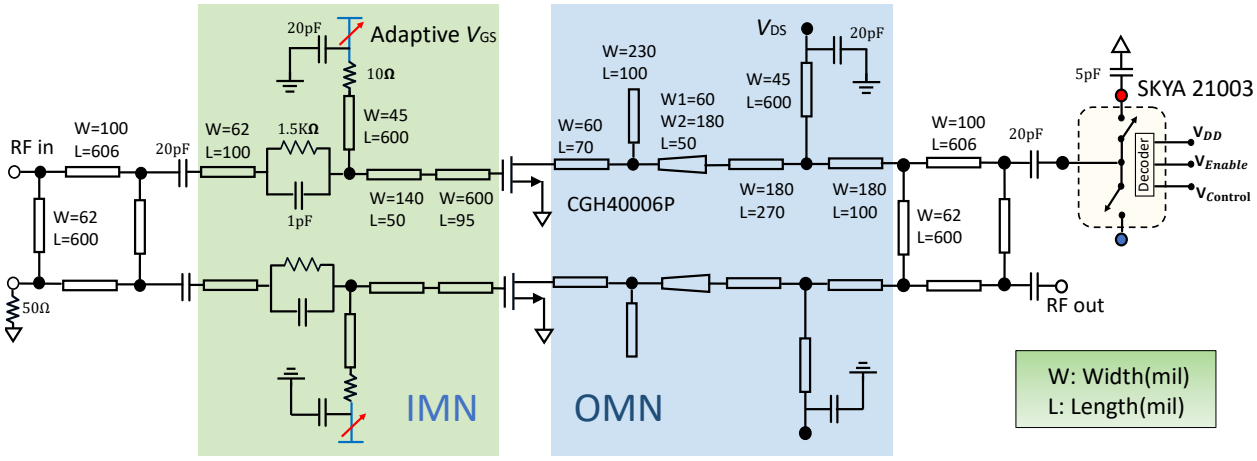
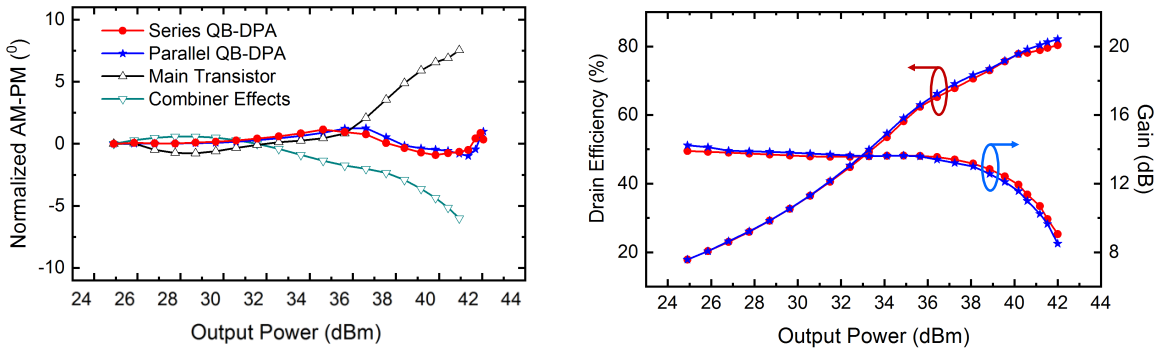


Figure 3.15: Full Schematic of the designed reconfigurable QB-DPA with an SOI-based SPDT switch.

and implemented using GaN devices and branch-line quadrature couplers operating at a center frequency of 3.5 GHz.



(a) (b)

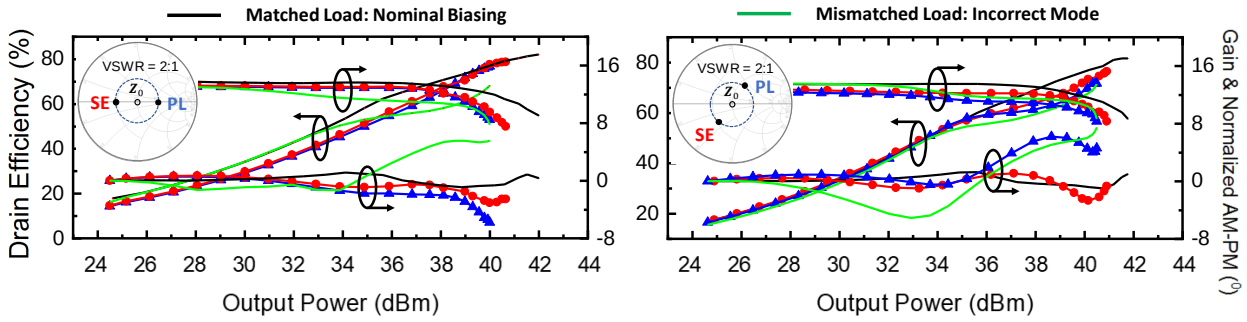
Figure 3.16: Simulation results of the QB-DPA at 3.5 GHz: (a) AM–PM, (b) DE and gain.

3.4.1 Design of Linearity-Enhanced QB-DPA at Nominal Condition

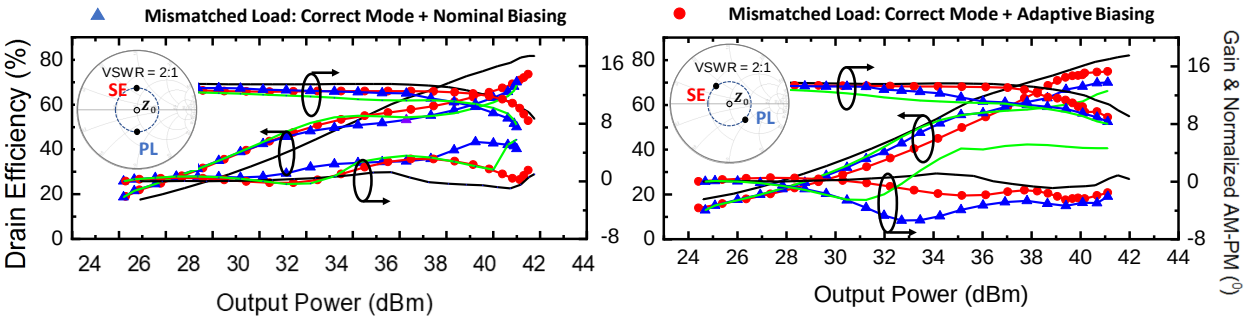
Fig. 3.13 depicts the output combiner of the linearity-enhanced QB-DPA including the parasitics of the transistors contributed by the GaN chip and package. The output matching network (OMN) of

the two paths is designed with identical topology for maintaining the consistent QB-DPA behavior over series/parallel alternation. Moreover, the reconfiguration for series/parallel linearity-enhanced QB-DPA can be realized through adaptive gate biasing and switching the isolation-port loading of output quadrature coupler. Practically, the RF switch can be implemented with a commercial SPDT SOI-based (SKYA21003), which consists of three ports: antenna (ANT), RF1, and RF2. The analysis of the switch implementation has been thoroughly elaborated in [35, 68]. The symmetry between series and parallel QB-DPAs is still valid (from the coupler plane to intrinsic drain plane), if two sub-PAs are designed identically, as illustrated in Fig. 3.13.

The OMN is devised to offer linearity-prioritized matching at both fundamental and second harmonic frequencies as is shown in Fig. 3.14. A tuning line lays between the drain term and 2nd



(a)



(b)

Figure 3.17: Simulated gain, DE and AM-PM recovery for the illustrative mismatched-loads. (Minor differences in results between symmetrical conditions, i.e., SE mode @z_{L} and PL mode @$1/z_{\mathrm{L}}$, are omitted for clarity of plotting.)

order frequency stub can supply an optimal imaginary part for the transistor, while ensuring the fundamental output matching presenting minimum influence with the harmonic matching [77]. Meanwhile, the design of input matching network (IMN) provides certain mismatch for perfecting the linearity with slightly AM-AM compression using the similar approach presented in [68], which is not discussed in detail here.

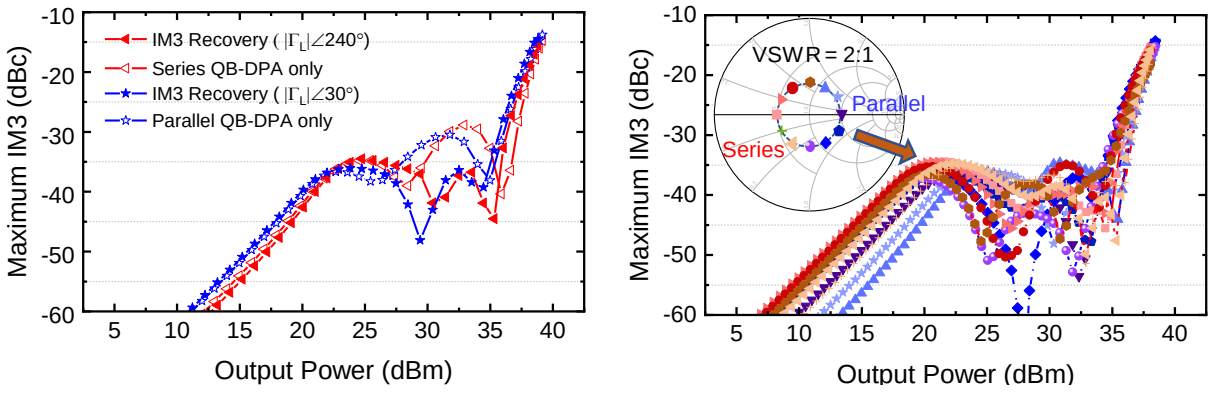
According to the above design considerations, the entire circuit is co-simulated with the circuit models and electromagnetic model of layout using Keysight ADS. The overall schematic is presented in Fig. 4.9 with the the switchable loading at the isolation port of output coupler. Fig. 3.16 shows the simulated AM–PM, DE, and gain of the proposed DPA at 3.5 GHz. By terminating the isolation port of the output coupler to a large shunt capacitor of 5 pF, the proposed reactance combiner network provides a complementary AM-PM response to that of the main transistor with around 6°, leading to effective compensation of the overall phase distortion as can be seen from Fig. 3.16(a). Interestingly, through extensive optimization, a quasi-open-circuited isolation-port loading (0.1-0.2 pF of capacitance) is found to generate the best AM-PM compensation of parallel QB-DPA shown in Fig. 3.16(a). This capacitive loading can be physically realized by the off-state parasitics (C_{off}) of the CMOS SOI switch with the corresponding port (RF2) in floated connection, as shown in Fig. 4.9. It is worthy to note that the value of jx (jb) loading is determined through the overall circuit simulation, and the discrepancy from theory and emulation is mainly due to the use of realistic matching circuits. Similar to the series mode, the parallel mode also presents minimized distortion of the AM-PM profile in Fig. 3.16(a). Overall, the AM–PM variation is maintained within $\pm 1^{\circ}$ across the entire dynamic power range for both series and parallel modes. Meanwhile, a 80% saturation efficiency and a 60% efficiency at 6-dB power back-off are simultaneously achieved, as depicted in Fig. 3.16(b), while achieving a flat AM-AM response for both modes.

3.4.2 Mode Reconfiguration for VSWR Resilience

As discussed earlier, the PA linearity can be enhanced in either series mode or parallel mode at nominal 50-Ω load, especially in the load-modulation region. For an arbitrary mismatched load, $Z_{\rm L}$ (or $Y_{\rm L}$), a proper operational mode (series/parallel) should be configured in order to optimize the DE, linearity and output power. Fig. 3.17 illustrates how the mismatch-induced degradation is mitigated through mode reconfiguration and adaptive biasing over the entire $2:1$ VSWR circle. Since the mismatch effects on series and parallel modes are symmetrical to $z_{\rm L}$ and $y_{\rm L}$, respectively, the simulation results presented in each of the sub-figures from Fig. 3.17(a)-(b) correspond to a pair of loads that are symmetric with respect to the origin of Smith chart.

Specifically, for the mismatched resistive loads $|\Gamma_L|\angle 0^\circ$ and $|\Gamma_L|\angle 180^\circ$ in Fig. 3.17, with the modes reconfiguration, the efficiency can be well recovered at saturation and 6-dB back-off regions along with an improved gain profile (early compression modified), which effectively compensate for the incorrect-mode-induced degradation. Moreover, the AM-PM distortions are significantly mitigated to $< \pm 2.8^\circ$ for the load-modulation region, which varies only $< \pm 1^\circ$ in the matched load scenario due to the adaptive gate biasing. Complex loads exhibit the corresponding improvements as well, while both modes can be applied for the mismatched loads of $|\Gamma_L|\angle \pm 90^\circ$ in Fig. 3.17(b), which agrees with the theoretical illustration in Figs. 3.10(e) and (f).

To further evaluate the linearity of reconfigurable QB-DPA, a two-tone simulation with frequency spacing of 10 MHz centered at 3.5 GHz is conducted to extract the third-order intermodulation (IM3) under load mismatch at $2:1$ VSWR circle. The simulated maximum IM3 is plotted in Fig. 3.18. With the mode reconfiguration and the bias voltage adjustment of main/aux PAs, the IM3 level can be kept consistently below -35 dBc (before compression) all over the entire $2:1$ VSWR circle.



(a) (b)

Figure 3.18: Two tone simulation to verify IM3 recovery through reconfiguration of series/parallel modes.

3.5 Fabrication and Measurement Results

The overall layout is generated from circuit schematic, and it is electromagnetically modeled using ADS Momentum simulator. The EM model is then co-simulated with active components, and the layout is optimized until the co-simulation results match the schematic-only case. The fabricated QB-DPA is shown in Fig. 4.12 which is developed on the Rogers 5880 substrate, and the entire PCB is mounted on a copper substrate and fastened using screws. The RF switch module is placed on another small PCB board, and it is mounted on the same copper substrate with RF connection to the isolation node of the output quadrature coupler. By applying different bias setting of the switch control, the ANT port of the SPDT switch can be routed to RF1 (5 pF) and open circuit (both RF1 and RF2 are off via the enable function of switch) alternatively. The design implemented with two identical transistor devices for main and auxiliary PAs. To experimentally demonstrate the reconfigurable operation, the designed QB-DPA is evaluated with both the continuous waveform (CW) and LTE modulated signal at series and parallel mode, respectively.

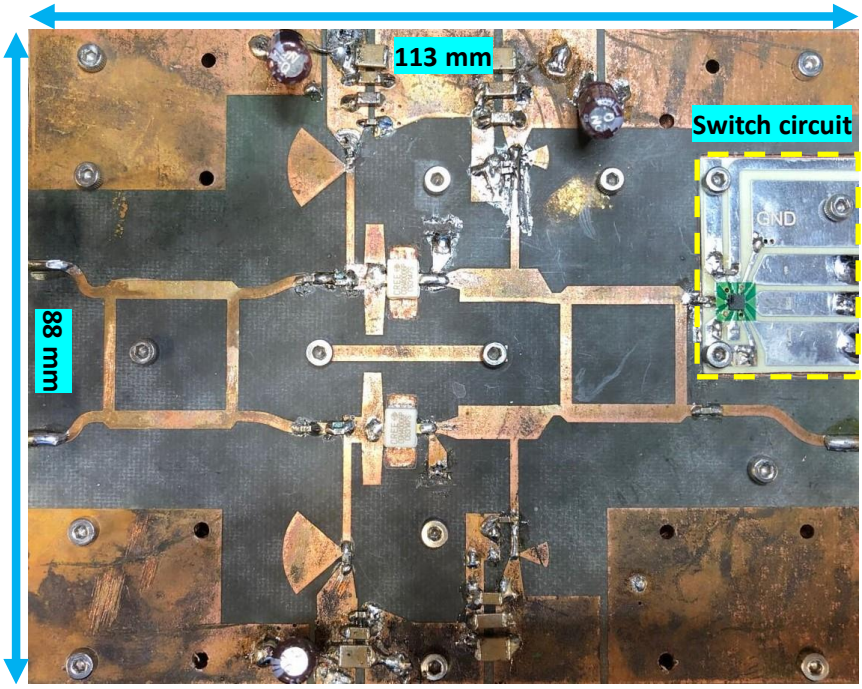


Figure 3.19: Top view of the fabricated circuit board.

3.5.1 Continuous-Wave Measurement

In the series QB-DPA mode measurement, the gate bias of the main device is primarily set to -2.55 V in Class-AB in order to improve the linearity at low power range. The auxiliary is set to class-C type with gate bias voltage as -4.55 V to compensate for overall AM-PM. In the parallel QB-DPA mode measurement, the gate biases of two PAs are exchanged and slightly adjusted with V_{GS} set as -4.65 V for the auxiliary device and -2.5 V for the main cell, respectively.

Fig. 3.20 shows the measured drain efficiency (DE) and gain versus the output power driven by a power-swept continuous-wave (CW) stimulus at both series and parallel mode. A desired Doherty profile is experimentally obtained with efficiency-optimized bias in both modes. It is important to note that the the designed QB-DPA presents a high low-power gain around 14 dB at the center frequency of 3.5 GHz, and it remains flat up to P_{1dB} region. Such a linear AM-AM behavior

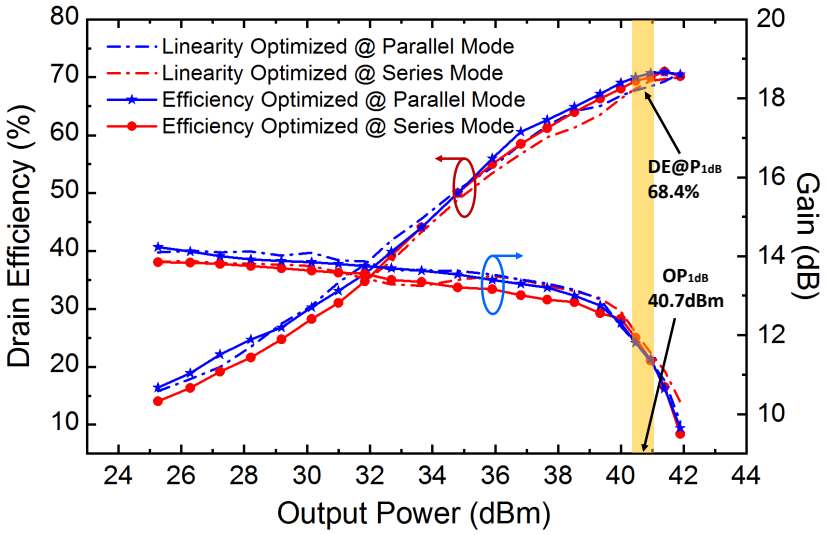
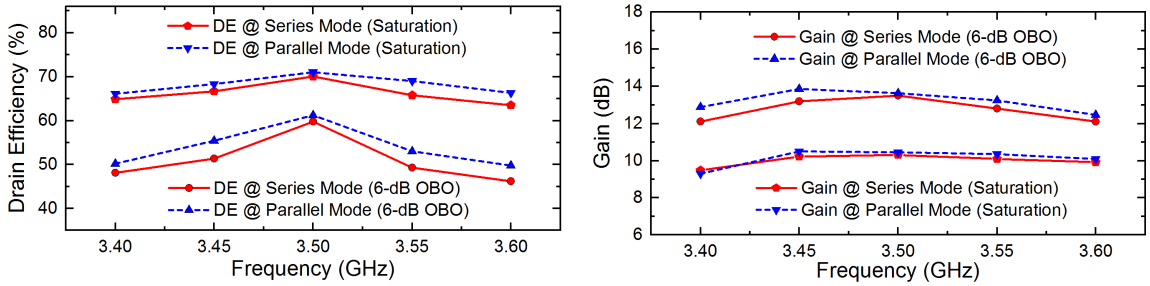


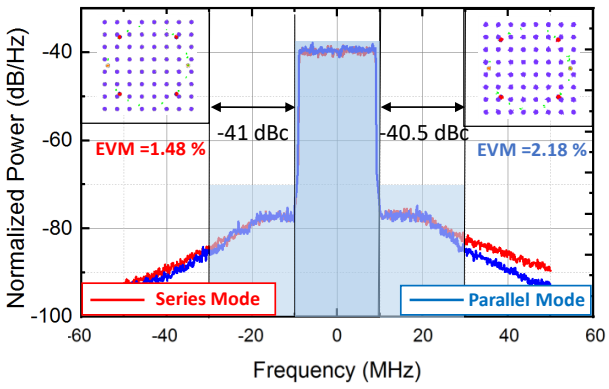
Figure 3.20: Measured DE and gain versus output power centered at 3.5 GHz.



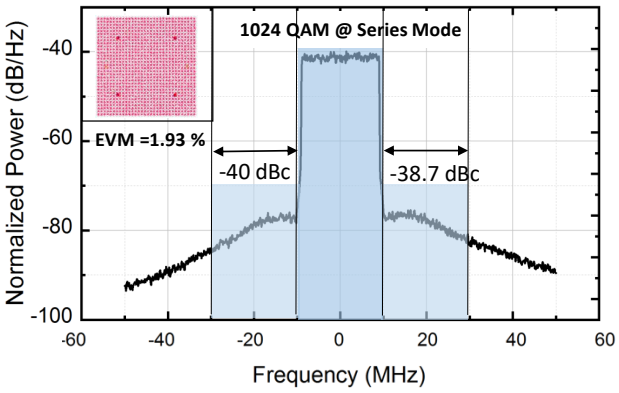
(a) (b)

Figure 3.21: Measured frequency response at peak and 6-dB OBO for series and parallel modes: (a) DE, (b) gain.

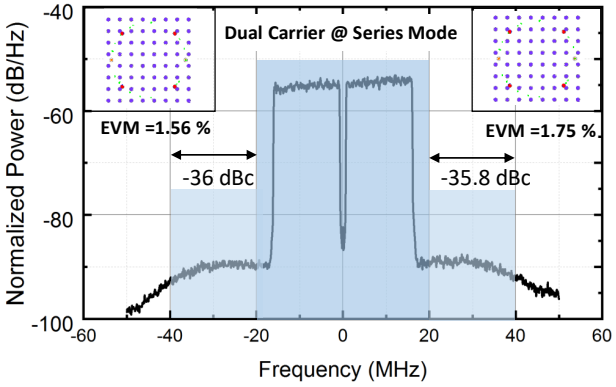
agrees well with the simulation results in Fig. 3.16(b). The measured efficiency at P_{Max} is almost the same for both modes at the operating center frequency attributed to the identical loadline at saturation region, while a higher DE profile at 6-dB back off region is presented at parallel mode due to a smaller current consumption. Meanwhile, the frequency response of the PA is evaluated across $3.4 - 3.6$ GHz as shown in Fig. 3.21. In the series mode, the measured drain efficiency is $63.5\% - 70.1\%$ at the peak output power, and the gain is $9.4 - 10.3$ dB. At 6-dB OBO, the measured gain and drain efficiency are $12.1 - 13.5$ dB and $46.2\% - 59.8\%$, respectively. The



(a)



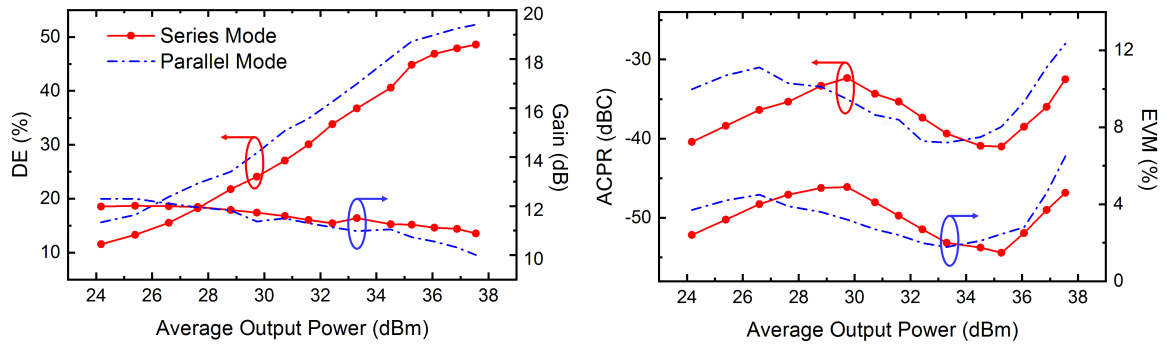
(b)



(c)

Figure 3.22: Measured PSD, ACPR and EVM at 3.5 GHz without DPD: (a) At series/parallel modes under a 20MHz modulated signal with 64-QAM, (b) At series mode under a 20-MHz modulated signal with 1024-QAM, (c) At series mode under dual carrier 40-MHz modulated signal for 64-QAM.

realistic parallel mode is not exactly symmetrical to series mode, which presents a comparatively higher performance in terms of drain efficiency and gain over the entire dynamic power range. This is mainly due to the fabrication tolerance and part-to-part variation of two GaN transistors.



(a) (b)

Figure 3.23: (a) DE and gain, (b) EVM and ACPR versus average output power under modulated signal with 20MHz modulation bandwidth and 64 QAM.

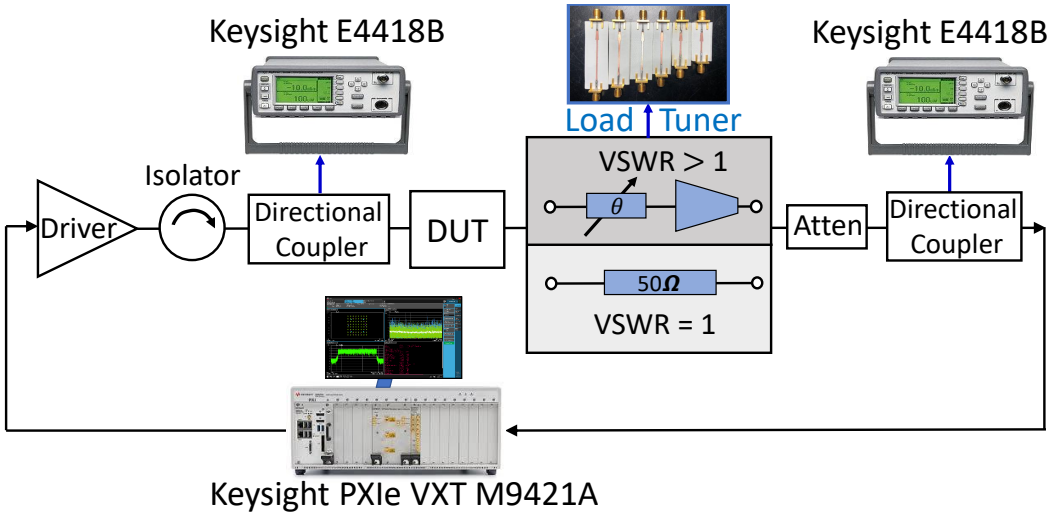


Figure 3.24: Measurement setup for characterization of the series/parallel QB-DPA under nominal 50-Ω and mismatch loading (VSWR $>$ 1) conditions.

3.5.2 Modulated Measurement with Nominal 50-Ω Termination

The efficiency and linearity of the reconfigruable series/parallel QB-DPA was assessed under various modulation bandwidth (e.g., 20 and 40 MHz) and QAM formats (e.g., 64 QAM, 1024 QAM) using an LTE signal with 9.6 dB PAPR. The measured power spectral density (PSD) and error vector magnitude (EVM) are depicted in Fig. 4.18. At series mode, the designed QB-DPA PA presents

Table 3.1: State-of-the-Art of Linear and Efficient GaN PAs

Ref.	f_0 (GHz)	P_{avg} (dBm)	Mod. BW (MHz)	Average DE (%)	ACPR w/o DPD (dBc)
[68]	3.5	34.5	10	42.4	-37
[24]	5	32	120	42	-43.1
[26]	2.14	35.5	20	44	-40.5
[25]	0.8	33	20	33.2	-42.5
[4]	7	27.7	20	43	-41
[46]	7	32	56	41	-36
[48]	3.5	35.8	20	62	-27.9
[47]	2.3	35.2	10	46	-35.6
[49]§	5	36	5	57.8*	-30
[50]	2.0	33	5	54	-30
[78]	2.1	40	5	55	-30
This Work	3.5	35	20	45	-41

† QB-DPA mode. § Measured using two-tone signal with 5-MHz tone spacing. $*$ Maximum CW PAE at an IMD3 of -30 dBc. $**$ Series QB-DPA mode.

an average efficiency of 45% and ACPR around -41 dBc at a rated average output power of 35 dBm without any DPD applied. A low corresponding error vector magnitude (EVM) of 1.48% is measured in this condition, as shown in Fig. 4.18(a), whereas, a EVM of 2.18% at parallel mode is obtained corresponding to a -40.1 dBc ACPR at 33.8 dBm output power region. The measurements results under 20-MHz with 1024 QAM at series mode are expressed in Fig. 4.18(b). A decent linearity of 1.93% EVM and -40 dBc is achieved. Furthermore, the designed PA is evaluated under carrier-aggregated 40-MHz modulated signal, EVM of 1.56% and 1.75% and ACPR of -36 dBc and -35.8 dBc are recorded at adjacent power channels, respectively.

The PA is further tested using a power-swept LTE signal with the same 20-MHz bandwidth and 64 QAM modulation, and the drain efficiency and gain versus the average output power are plotted in Fig. 3.23(a). The profile of EVM and ACPR are presented as well in Fig. 3.23(b). Based on the measurement in Fig. 3.23, at both series/parallel modes, the designed QB-DPA maintains a low EVM less than 4.2% and a raw ACPR between -30.6 and -41 dBc below 37.2 dBm output power area, while the corresponding average efficiency can be up to 47.3%.

Table 4.1 summarizes the state-of-the-art of series/parallel QB-DPA compared to other contemporary linear GaN-based PAs published recently. The proposed QB-DPA offers a very competitive design achievement in terms of the maximum rated output power, average DE and raw ACPR. Specifically, compared with the designs in [68] and [4, 25, 26, 46], the proposed QB-DPA exhibits the lower ACPR evaluated with the same modulation bandwidth while maintaining larger DE. Meanwhile, excellent output power and average DE are obtained with an impressive ACPR comparable to [24, 47–50, 78], which clearly exhibits better linearity–efficiency and well verifies the effectiveness of the proposed theory.

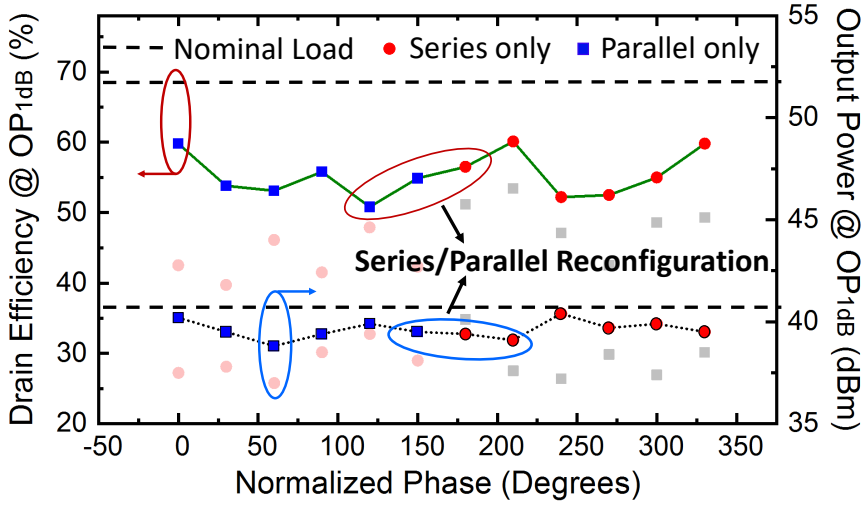


Figure 3.25: Measured DE and $\mathrm{OP_{1dB}}$ over 2:1 VSWR with CW signal.

3.5.3 Reconfigurable-Mode Measurement under Load Mismatch

The designed QB-DPA is evaluated with CW as well as single-carrier 64 QAM 20-MHz bandwidth modulated signal (used in Sec. 4.4.2) under load mismatch at various VSWR up to $2.5:1$ to demonstrate the reconfigurable operation. A functional configuration of the measurement system setup is shown in Fig. 4.15. A driver stage (ZHL-5W-422+) provides power level and a directional coupler after isolator is used to accurately sample and measure the input power. The DUT output,

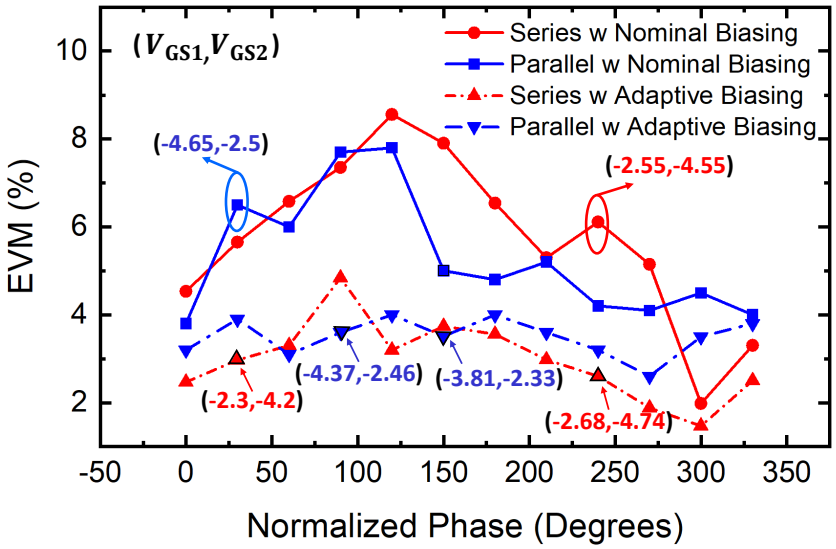


Figure 3.26: EVM at 2:1 VSWR with modulated signal under nominal biasing and adaptive biasing, respectively.

at this stage, is connected to a mismatched load where VSWR > 1 spanning the 360 phase with the designed impedance transformer. Finally, a Keysight PXIe vector transceiver (VXT M9421) is used as CW/modulated signal generator and analyzer.

The designed QB-DPA is first characterized with a CW signal covering 2:1 VSWR circle with a 30° step of the phase swept. The load tuner as illustrated in Fig. 4.15 is physically realized using an impedance transformer in series to a set of transmission lines with different electrical lengths. As shown in Fig. 3.25, with reconfiguration, the DE at the 1-dB compression point ($\mathrm{OP_{1dB}}$) can be significantly improved over entire $2:1$ VSWR. Moreover, a consistent $\mathrm{OP_{1dB}}$ of $38.8-40.4$ dBm is maintained guaranteeing a stable output power to mitigate the impedance mismatch-induced power degradation. Then the modulation measurement is conducted which begins with series/parallel modes of QB-DPA under $2:1$ VSWR. An EVM comparison between the nominal biasing (retained biasing setting as in Fig. 4.18 for certain realistic scenarios with fixed biasing) and adaptive biasing (biasing re-combination for best EVM at the same input power level) is illustrated in Fig. 3.26 , where the bias voltages are indicated for certain points to show the lin-

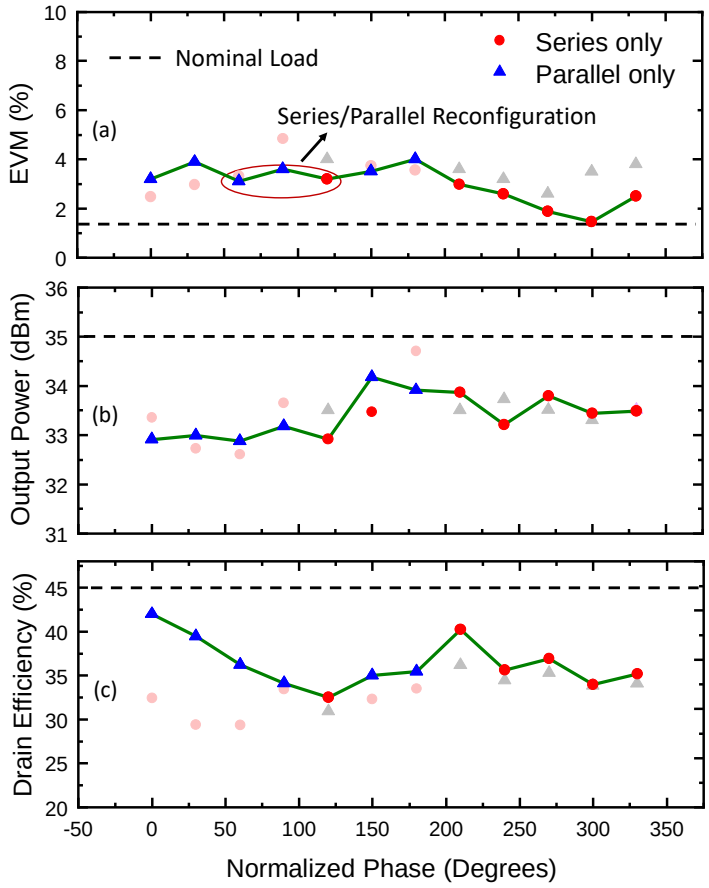


Figure 3.27: Modulation signal Measurement of reconfigurable series/parallel PA under $2:1$ VSWR over entire phase range: (a) EVM, (b) output power, and (c) average DE.

earity enhancements obtained. It should be noted that the above results along with the following varied VSWR test are driven with a constant input power of 21 dBm for the fair and meaningful comparison.

Fig. 3.27 illustrates the EVM, output power, and DE versus the varying phase along the $2:1$ VSWR circle. A $< 4\%$ of EVM is set as a specific benchmark in this design, which can be re-specified based on the various communication standards. In Fig. 3.27(a), at series mode, a low EVM ($< 4\%$) can be achieved for the majority of phases on the $2:1$ VSWR circle, with corresponding output power between $32.6 - 34.5$ dBm shown in Fig. 3.27(b). For the rest of phases

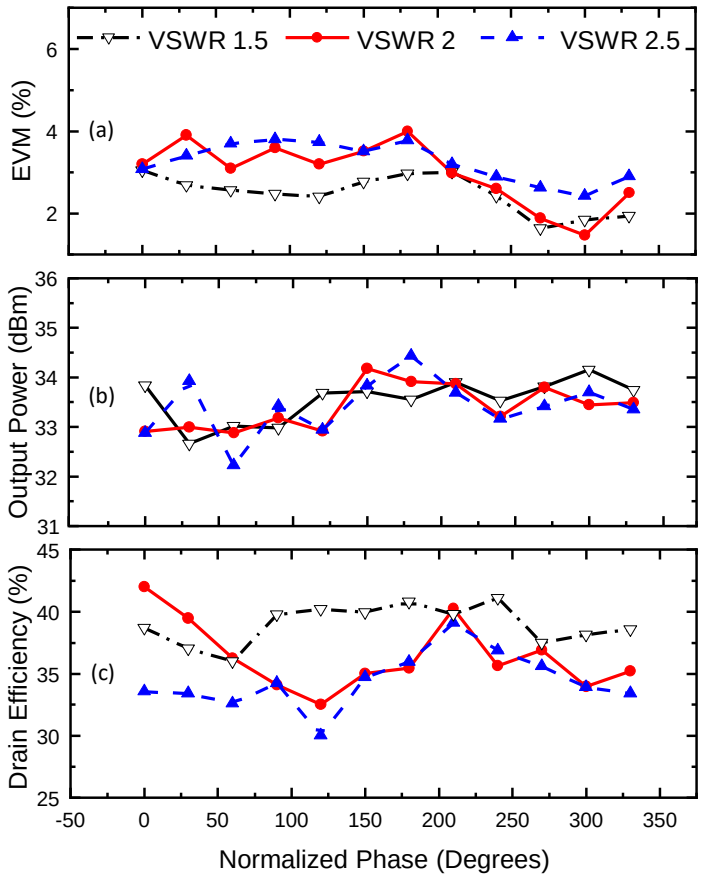


Figure 3.28: Modulation signal Measurement of series/parallel QB-DPA under variable VSWR over entire phase range: (a) EVM, (b) output power, and (c) Average DE.

not meeting the linearity spec, the parallel mode is activated through the switching between main and auxiliary biasing and coupler isolation port at out-end via the SPDT switch. It is worthy to point out that an efficiency priority is targeted for certain phase points that EVM is comparable between series/parallel modes, which can be seen in Fig. 3.27(c). The EVM of parallel mode slightly degrades, while a significant improvement of efficiency can be observed. To further experimentally demonstrate the reconfigurable operation, the designed QB-DPA is evaluated under variable VSWR up to $2.5:1$. Note that a fine adjustment of gate biasing is implemented to optimize the linearity of the dedicated QB-DPA modes towards different mismatch conditions. Fig. 3.28 depicts the optimal results obtained via series/parallel reconfiguration on the full VSWR circle of $1.5:1$,

$2:1$ and $2.5:1$, respectively. The proposed series/parallel QB-DPA presents the capability to constantly maintain a low EVM, stable output power and substantially recover the DE when subjected to the load mismatch.

3.6 Conclusion

In this chapter, a series/parallel mode-reconfigurable QB-DPA is proposed and analyzed. It is for the first time theoretically verified that a QB-DPA can be reconfigured between series and parallel modes by switching the roles of main and auxiliary amplifiers along with the isolation loading of output coupler. Further, the theory of linearity-enhanced series/parallel QB-DPA is analyzed as an extension from generic QB-DPA. Moreover, by leveraging the symmetry of series/parallel modes with complementary sensitivities to load impedance/admittance, the QB-DPA is analytically proven to be VSWR-resilient. A reconfigurable QB-DPA prototype is implemented to verify the proposed concept at 3.5 GHz. In the nominal case driven with the LTE modulated signal with 20-MHz bandwidth, the measured PA exhibits -41 dBc ACPR at series mode, allowing it to achieve 1.48% EVM at the maximum P_{rated} = 35 dBm without any additional digital linearization performed. In the parallel mode, a 2.18% EVM corresponding to -40.1 dBc ACPR is obtained at P_{rated} = 33.8 dBm. Meanwhile, when suffering from the load mismatch, the designed QB-DPA also maintains the high linearity and efficiency up to $2.5:1$ VSWR circle via the two-state reconfiguration of the loading capacitor and optimized gate biasing. Overall, the proposed reconfigurable QB-DPA offers a compelling solution for realizing energy efficient and highly robust massive MIMO system.

3.7 Appendix

In Sec. 3.3.1, when the output coupler driven with a mismatched load ($z_{\rm L}$ or $y_{\rm L}$) and reactance/suscpetance (jx or jb) at the isolation port, the impedance observed by the main and auxiliary transistors have the following solutions at series mode:

$$Z_{\rm M_{SE},bo} = \frac{2}{jx + \frac{1}{z_{\rm L}}} Z_0 \quad \& \quad Z_{\rm A_{SE},bo} = \infty; \tag{3.24}$$

$$\begin{aligned} Z_{\rm M_{SE},sat} &= \frac{2z_{\rm L} - 2}{jxz_{\rm L} + 1} Z_0 + Z_0, \\ Z_{\rm A_{SE},sat} &= \frac{2x - 2xz_{\rm L}}{xz_{\rm L} - j} Z_0 + Z_0. \end{aligned} \tag{3.25}$$

Meanwhile, the voltages $V_{\rm Main}$ and $V_{\rm Aux}$ can be expressed as

$$V_{\rm M_{SE}}(x, z_{\rm L}) = \frac{2I_{\rm M}z_{\rm L} + jxI_{\rm A}z_{\rm L} - I_{\rm A}}{jxz_{\rm L} + 1} Z_0. \tag{3.26}$$

$$V_{\rm A_{SE}}(x, z_{\rm L}) = -j\frac{I_{\rm M} - jxI_{\rm A}z_{\rm L} + j2xI_{\rm A}}{jxz_{\rm L} + 1} Z_0. \tag{3.27}$$

Furthermore, the output voltage of the proposed QB-DPA represented by the following equation

$$V_{\rm L_{SE}}(x, z_{\rm L}) = \frac{-\sqrt{2}I_{\rm M}z_{\rm L} - j\sqrt{2}xI_{\rm A}z_{\rm L}}{jxz_{\rm L} + 1} Z_0. \tag{3.28}$$

Similarly, at parallel mode,

$$Z_{\mathrm{M_{PL},bo}} = \frac{2}{jb + \frac{1}{y_{\mathrm{L}}}} Z_0 \quad \& \quad Z_{\mathrm{A_{PL},bo}} = \infty; \tag{3.29}$$

$$Z_{\mathrm{M_{PL},sat}} = \frac{2y_{\mathrm{L}} - 2}{jby_{\mathrm{L}} + 1} Z_0 + Z_0,$$

$$Z_{\mathrm{A_{PL},sat}} = \frac{2b - 2by_{\mathrm{L}}}{by_{\mathrm{L}} - j} Z_0 + Z_0. \tag{3.30}$$

And the voltages V_{Main} and V_{Aux} can be shown to be

$$V_{\mathrm{M_{PL}}}(b, y_{\mathrm{L}}) = -j \frac{2I_{\mathrm{M}} y_{\mathrm{L}} + jbI_{\mathrm{A}} y_{\mathrm{L}} - I_{\mathrm{A}}}{jby_{\mathrm{L}} + 1} Z_0. \tag{3.31}$$

$$V_{\mathrm{A_{PL}}}(b, y_{\mathrm{L}}) = \frac{I_{\mathrm{M}} - jbI_{\mathrm{A}} y_{\mathrm{L}} + j2bI_{\mathrm{A}}}{jby_{\mathrm{L}} + 1} Z_0. \tag{3.32}$$

$$V_{\mathrm{L_{PL}}}(b, y_{\mathrm{L}}) = \frac{-\sqrt{2}I_{\mathrm{M}} - j\sqrt{2}bI_{\mathrm{A}}}{jby_{\mathrm{L}} + 1} Z_0. \tag{3.33}$$

CHAPTER 4: ANALYSIS AND DESIGN OF RECONFIGURABLE MULTI-BAND MISMATCH-RESILIENT QUASI-BALANCED DOHERTY POWER AMPLIFIER FOR MASSIVE MIMO SYSTEMS

[1] To support the high data-rate communications link, large bandwidth with highly linear performance transmitters are of utmost importance. In previous chapters, the mismatch resilience of the QB-DPA is studied within narrow bandwidth. This chapter introduces a broadband mismatch-resilient QB-DPA architecture that can maintain stable linear output power over multi-bandwidth to restore the PA performance.

4.1 Introduction

With the insatiable demand for high-speed wireless data transmission, the wideband and spectrally-efficient modulation schemes are ubiquitously adopted in modern wireless systems. However, the high peak-to-average power ratio (PAPR) caused by the increasing number of sub-carriers and high modulation order in these advanced schemes leads to the fact that power amplifiers (PAs) have to operate at a large power backed-off range most of the time. As a result, PA architectures with back-off efficiency enhancement are highly desired to amplify such high-PAPR signals. Moreover, with the proliferation of communication bands, the PAs are expected to support multiband/multimode operations in order to minimize the number of PAs in a wireless platform for sustainable cost

[1]This chapter was published as
Haifeng Lyu *et al.*, "Wideband Quasi-Balanced Doherty Power Amplifier with REciprocal Main/Auxiliary Setting and Mismatch-Resilient Parallel/Series Reconfiguration" *2021 IEEE MTT-S International Microwave Symposium* June. 2021: 736-739.
Haifeng Lyu *et al.*, "Analysis and Design of Reconfigurable Multi-Band Mismatch-Resilient Quasi-Balanced Doherty Power Amplifier for Massive MIMO Systems" *IEEE Transaction on Microwave Theory and Techniques)* 70(10) Oct. 2022: 4410-4421.

and space at system level. Therefore, broadband and highly-performance PA technologies are of crucial importance for next-generation wireless systems.

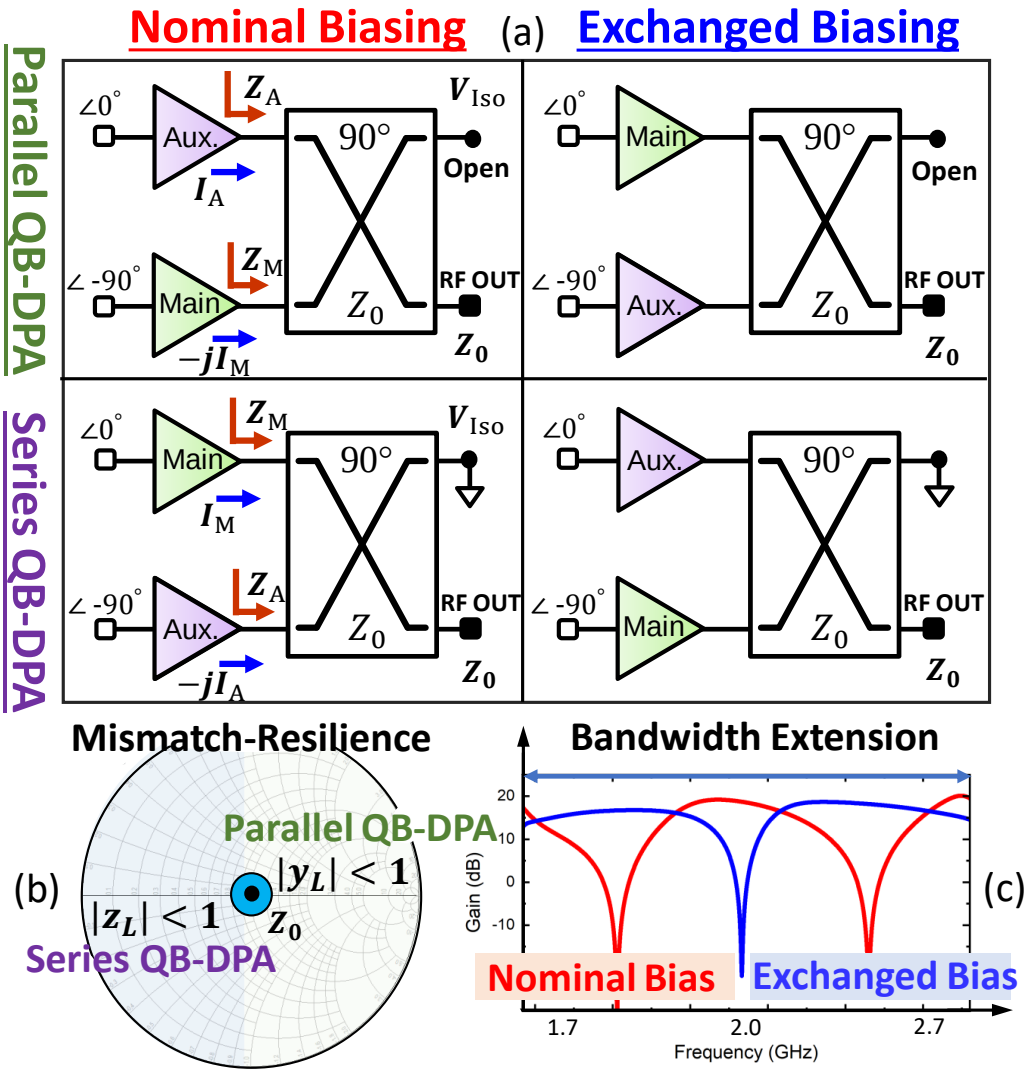


Figure 4.1: Proposed wideband QB-DPA: (a) Circuits mechanism for parallel/series switching and nominal/exchanged biasing alteration, (b) operation division for parallel/series QB-DPA to recover mismatch and (c) broadband realization with nominal/exchanged biasing.

Meanwhile, to further enhance the spectral efficiency, array-based spatial multiplexing technique has been widely exploited in 5G base stations that leverages the spatial differences to enable concurrent transmission of multiple signals at the same frequency, also known as massive multiple-input multiple-output (MIMO). However, the high-density antenna array inevitably brings about

strong mutual couplings between the co-located antennas due to the near field scattering (lattice spacing between elements) and limited isolation on substrate [28–30, 37, 69, 70]. Moreover, these couplings result in a high-speed antenna impedance variation as well as large voltage standing wave ratio (VSWR). Directly loaded by the antenna, the PAs in the array are load-pulled, and this load-pulling effect depends on both the scan angle and element location [31]. Consequently, the PAs can suffer from significant performance (e.g., efficiency, linearity, and OP_{1dB}) degradation, since the PA operation is governed by its loadline [76]. A more severe issue is the main beam distortion due to the accumulated PA non-linearity among the array, and it leads to a major challenge for digital pre-distortion (DPD) that has to be applied at array level [72, 73, 79, 80].

To improve the PAs' performance under mismatch, antenna isolation has been applied to block the effect of antenna-impedance variation from PA for decades. However, the isolators/circulators, typically based on magnetic materials, are bulky, expensive, and lossy prohibiting the large-scale integration in a massive MIMO system. Passive tunable matching networks (TMN) have been widely employed in handset devices to compensate for the dynamic load impedance [81–84]. However, the TMNs are typically lossy and bulky since extra building blocks are requires, leading to a major difficulty for array-level integration. To solve this issue, a promising solution is to merge this tuning-based approach into the PA stage. In [51], a broadband Doherty-like PA through active load pulling to a multi-port combiner is exploited to improve VSWR-related degradation at peak power. However, the presented architecture only exhibits Doherty-like performance across a narrow bandwidth with a 50-Ω load. More than 10% of power-added-efficiency (PAE) and 2-dB of output power degradation are reported for a single frequency operation over $4:1$ VSWR circle. A coupler-based hybrid series/parallel reconfigurable Doherty PA (DPA) is presented in [85], which utilizes exchangeable gate biasing, tunable phase offset at input, and adjustable current weighting of main/auxiliary PAs to counteract the load mismatch. The demonstrated prototype achieves a wideband small-signal $S21$ response at nominal load without large-signal and VSWR capability

over the bandwidth. Very recent works [86] based on load-dependent supply modulation adaption together with adjustable main-auxiliary phase offset also show a decent load insensitivity. Nevertheless, the realistic implementation of this approach requires extra DC-DC converters that may be challenging for integration into a massive array. Overall, while various techniques have been reported for PAs with tolerance to load-mismatch, a systematic design methodology is still necessary for PA with sustainable high efficiency and linearity not only against a large variation range of load impedance but also over a broad bandwidth.

This article presents a novel wideband reconfigurable quasi-balanced Doherty power amplifier (QB-DPA). Through parallel/series reconfiguration and reciprocal biasing, it is for the first time shown that the QB-DPA is able to maintain a stable OP_{1dB} as well as enhanced efficiency and linearity across $2:1$ VSWR circle, and this operation can be seamlessly extended to a wide bandwidth. Based upon the preliminary study in [87], this paper significantly expands the conference paper in the following aspects. First, a generalized theory of QB-DPA is analytically established and extended by including the effects of transistor parasitics and matching network, and it is mathematically proved that a wideband back-off efficiency enhancement can be achieved through a proper control of the phase dispersion from the realistic parasitic and output-matching networks. Second, a systematic design methodology is thoroughly explained in terms of matching topology selection and compensation for the parasitics. Third, a prototype design of a $1.7-2.7$ GHz wideband mismatch-resilient QB-DPA is presented, which not only exhibits back-off efficiency enhancements with 50-Ω load but also achieves a first-ever wideband mismatch-resilient operation with <1.9-dB OP_{1dB} fluctuation and $>46\%$ efficiency at P_{1dB} under $2:1$ VSWR. Furthermore, the measurement results using continuous-wave and modulated signals compare favorably with state-of-the-art for both nominal matched load and $2:1$ VSWR [51, 85, 86, 88–90], which further demonstrate the effectiveness of proposed method and holds promising potential for application to array-based massive MIMO systems.

4.2 Mismatch-Resilient and Wideband Quasi-Balanced Doherty Theory

As illustrated in Fig. 4.1(a), the reconfigurable QB-DPA architecture is composed of main/auxiliary PAs and a output-coupler combiner with a 90° input phase shift between the two PAs. Unlike the unbalanced PA architecture in [91], where the back-off efficiency enhancement at 50-Ω load is realized through adjustment of the transistor's width ratio (transistor size) and output Lange coupler's coupling coefficient, the QB-DPA is theoretically equivalent to the classical DPA [68,89], which is designed symmetrically with equal size of the main/aux. transistors and even 3-dB power splitter/combiner. Through the role-exchange of PAs (different gate-bias settings) and swapping of open-/short-circuit loading of isolation port, the QB-DPA maintain the OP_{1dB}, maximal achievable efficiency, and linearity against arbitrary variations of load impedance. To further extend this QB-DPA architecture to wideband operation, theoretical analysis considering transistors' parastics and the effects of realistic matching networks is performed. Meanwhile, a reciprocal biasing scheme is proposed to overcome the bandwidth limitation due to the imperfections of realistic quadrature coupler.

4.2.1 Ideal Parallel & Series Quasi-Balanced Doherty PA for Mismatch Recovery

The theoretical analysis of Doherty load modulation (LM) through the quadrature coupler is performed based on the impedance matrix (Z-matrix) of coupler. As shown in Fig. 4.1(a), to obtain the LM of main and auxiliary amplifiers, the PAs are modeled as ideal voltage-controlled current sources applied to the respective ports of Z-matrix of quadrature coupler. For parallel QB-DPA depicted in Fig. 4.1(a), the isolation port is open circuited with voltage only, and the voltages and

currents associated with the Z-matrix are expressed as

$$\begin{bmatrix} V_0 \\ V_{\rm Iso} \\ V_{\rm M} \\ V_{\rm A} \end{bmatrix} = \hat{\boldsymbol{Z}}_{\mathbf{coupler}} \begin{bmatrix} I_0 \\ 0 \\ -jI_{\rm M} \\ I_{\rm A} \end{bmatrix} \tag{4.1}$$

where V_0 and I_0 denote the output voltage and current of the output port that is matched to Z_0 in nominal condition, and $V_{\rm M/A}$ and $I_{\rm M/A}$ represent the voltage and current of main/auxiliary amplifier, respectively. The matrix of $\hat{\boldsymbol{Z}}_{\mathbf{coupler}}$ for the ideal 3-dB quadrature coupler matrix is given by

$$\hat{\boldsymbol{Z}}_{\mathbf{coupler}} = Z_0 \begin{bmatrix} 0 & +j & -j\sqrt{2} & 0 \\ +j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & +j \\ 0 & -j\sqrt{2} & +j & 0 \end{bmatrix} \tag{4.2}$$

Consequently, the LM behaviors of main and auxiliary amplifiers in parallel mode are derived as

$$Z_{\rm M_{PL}} = Z_0(2 + \frac{I_{\rm A}}{I_{\rm M}}) \quad \& \quad Z_{\rm A_{PL}} = Z_0 \frac{I_{\rm M}}{I_{\rm A}}. \tag{4.3}$$

For series QB-DPA mode shown in Fig. 4.1(a), the isolation port is short-circuited, and the main and auxiliary amplifiers are exchanged. Thereby, the voltage-current dependence with Z-matrix is re-written as

$$\begin{bmatrix} V_0 \\ 0 \\ V_{\rm A} \\ V_{\rm M} \end{bmatrix} = \hat{\boldsymbol{Z}}_{\mathbf{coupler}} \begin{bmatrix} I_0 \\ I_{\rm Iso} \\ -jI_{\rm A} \\ I_{\rm M} \end{bmatrix} \tag{4.4}$$

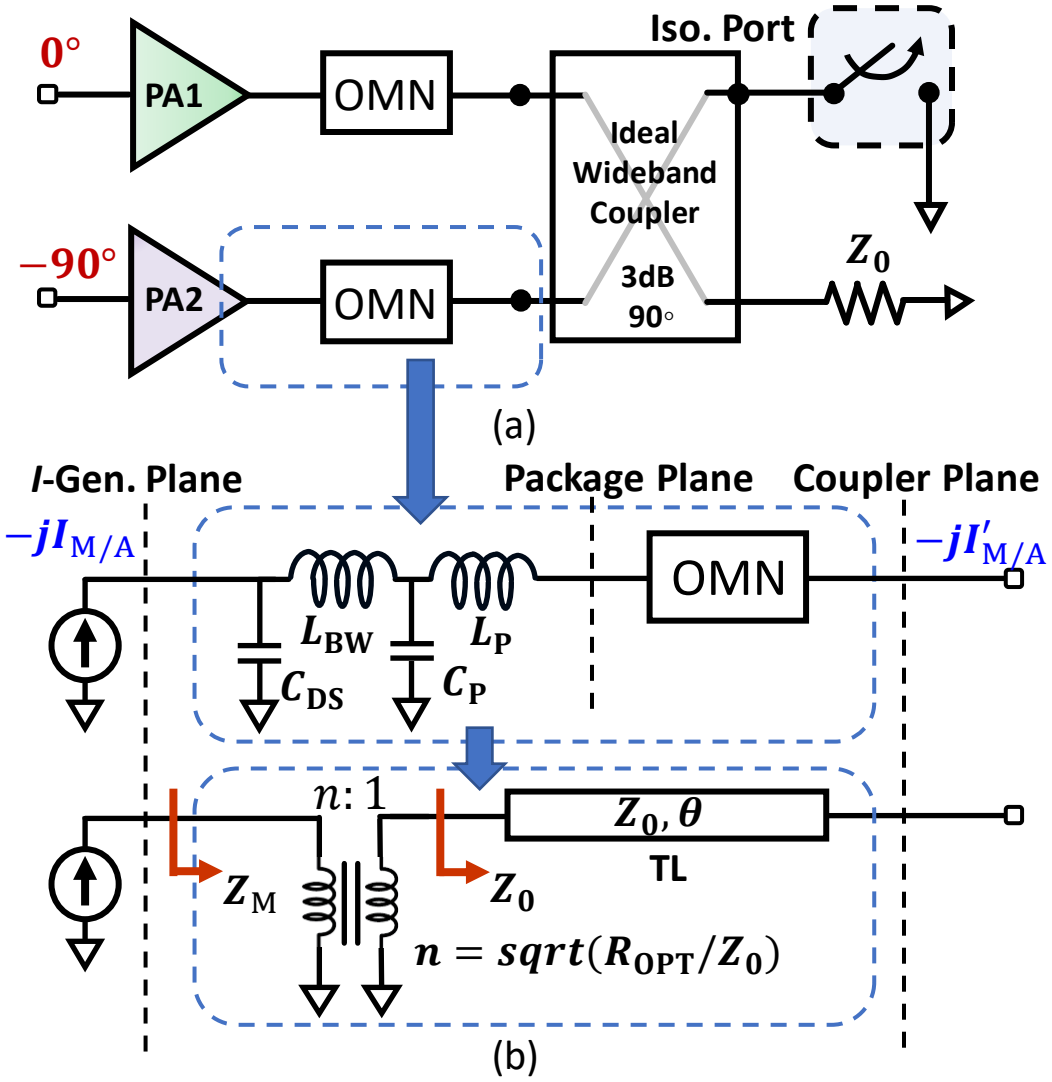


Figure 4.2: (a) Proposed wideband QB-DPA OMN, (b) equivalent OMN with ideal transformer and TL.

Nevertheless, the same (compared to the parallel mode) LM behaviors for main and auxiliary amplifiers are obtained

$$Z_{\mathrm{M_{SE}}} = Z_0(2 + \frac{I_\mathrm{A}}{I_\mathrm{M}}) \quad \& \quad Z_{\mathrm{A_{SE}}} = Z_0 \frac{I_\mathrm{M}}{I_\mathrm{A}}. \tag{4.5}$$

The parallel/series QB-DPA behaves symmetrically at the nominal condition with matched load.

More importantly, a complementary sensitivity under load mismatch can be utilized to create a mismatch-resilient QB-DPA as illustrated in Fig. 4.1(b). Given an arbitrary load admittance (impedance) of $Y_{\rm L}$ ($Z_{\rm L}$), the LM of parallel/series QB-DPA can be calculated as

$$\begin{aligned} Z_{\rm M_{PL}}(y_{\rm L}) &= Z_0\frac{2y_{\rm L}I_{\rm M}+I_{\rm A}}{I_{\rm M}} \;\;\&\;\; Z_{\rm A_{PL}} = Z_0\frac{I_{\rm M}}{I_{\rm A}},\\ Z_{\rm M_{SE}}(z_{\rm L}) &= Z_0\frac{2z_{\rm L}I_{\rm M}+I_{\rm A}}{I_{\rm M}} \;\;\&\;\; Z_{\rm A_{SE}} = Z_0\frac{I_{\rm M}}{I_{\rm A}}, \end{aligned} \tag{4.6}$$

in which $y_{\rm L}(z_{\rm L})$ represents the normalized form of $Y_{\rm L}(Z_{\rm L})$ to the matched admittance Y_0 (impedance Z_0). Further, the voltage expression at parallel/series mode of main/aux. PAs can be derived as below,

$$\begin{aligned} V_{\rm M_{PL}}(y_{\rm L}) &= -j(2I_{\rm M}y_{\rm L}-I_{\rm A})Z_0 \;\;\&\;\; V_{\rm A_{PL}} = I_{\rm M}Z_0;\\ V_{\rm M_{SE}}(z_{\rm L}) &= (2I_{\rm M}z_{\rm L}-I_{\rm A})Z_0 \;\;\&\;\; V_{\rm A_{SE}} = -jI_{\rm M}Z_0. \end{aligned} \tag{4.7}$$

It is worthy to note that the main amplifier can suffer from substantial RF voltage swing that $|V_{\rm M_{PL/SE}}| > |V_{\rm DD}|$ (DC rail voltage), due to the excessively high $y_{\rm L} > 1$ ($z_{\rm L} > 1$) in parallel (series) mode in Eq. (4.7), which leads to severe non-linearity, inefficiency, and reliability issues. Nevertheless, from Fig. 4.1(b), a non-voltage clipping load-impedance region can be reconfigured for parallel mode at $|y_{\rm L}| < 1$ (i.e., $|z_{\rm L}| > 1$) and for series mode at $|z_{\rm L}| < 1$ for VSWR tolerance, which indicates a full coverage of the entire Smith chart with a combined operation of two modes. Together with the fact that the auxiliary amplifier is naturally independent of the load in either mode, a completely clipping-free (mismatch-resilient) QB-DPA can be realized by leveraging the complementarity between parallel and series modes.

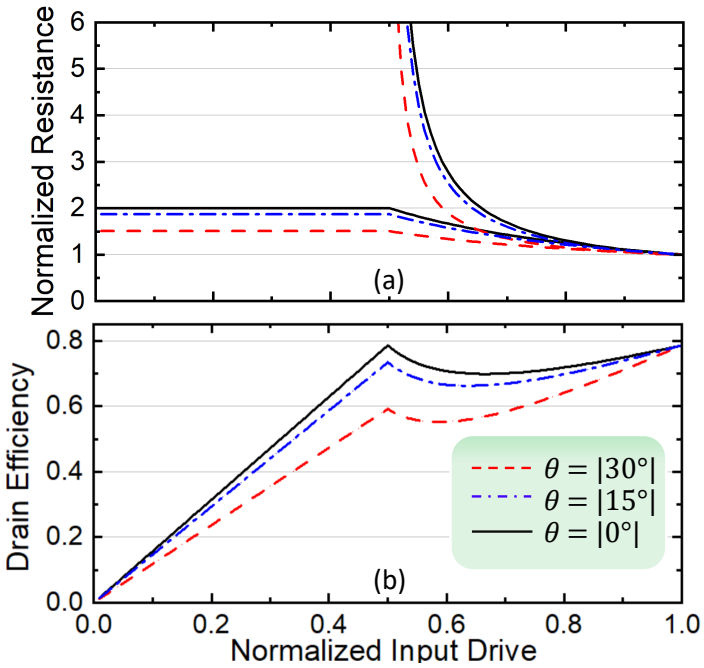


Figure 4.3: Calculated QB-DPA behaviors due to the θ dispersion for: (a) normalized resistance of Z_{M} and Z_{A}, (b) drain efficiency.

4.2.2 Effects of Transistor Parasitics and Matching Networks

The aforementioned generic QB-DPA architectures are based on ideal current sources directly coupled to the quadrature hybrid. Realistically, this model needs to be extended by including the effects of transistors' parasitics and output matching networks (OMNs), as is shown in Figs. 4.2. Each of the amplifiers is modeled as an ideal current source with parasitic network, which is connected to the quadrature coupler through a matching network. The combined passive network (parasitics + OMN) can be further modeled as an ideal transformer in conjunction with a transmission line (TL) of Z_0 characteristic impedance, offering functional equivalence in terms of impedance transformation and phase dispersion, as illustrated in Fig. 4.2(b).

To investigate the endurable phase θ variation range, theoretical study is performed on QB-DPA LM. This is particularly meaningful for wideband QB-DPA designs since the wideband OMNs

usually have large phase dispersion. Ideally, the effective load impedance of the main amplifier in the back-off power region should be maintained to the desired value (i.e., $2Z_0$) for the matched load condition. In reality, due to the loading of peaking amplifier's off-state impedance, the back-off load impedance observed by main amplifier can deviate from the optimal value, which leads to a distortion of LM behavior. To solve this issue, the OMN should ideally provide an opposing phase dispersion that compensates for the transistors' parasitic in order to maintain a desired Doherty profile. To mathematically evaluate the tolerable θ range, the ABCD matrix of the transmission line (Z_0 , θ) in Fig. 4.2(b) is thus expressed as

$$\boldsymbol{A}_{\mathbf{TL}} = \begin{bmatrix} \cos\theta & jZ_0\sin\theta \\ j\sin\theta/Z_0 & \cos\theta \end{bmatrix} \tag{4.8}$$

Subsequently, the ideal loadline seen at the intrinsic drain plane of main and auxiliary devices are derived through the interaction of output coupler and the TLs (Z_0, θ). Thus, by shifting the coupler matrix plane [41], Eqs. (4.3) and (4.5) can be re-derived as

$$Z_{\mathrm{M_{PL/SE}}} = n^2 Z_0 (2\cos\theta e^{-j\theta} + \frac{I_A}{I_M} e^{-j2\theta}), \tag{4.9}$$

$$Z_{\mathrm{A_{PL/SE}}} = n^2 Z_0 (\frac{I_M}{I_A} e^{-j2\theta} + 2j\sin\theta e^{-j\theta)}), \tag{4.10}$$

where n is the transformation coefficient for the ideal transformer in Fig. 4.2(b).

The fundamental RF power for main/auxiliary amplifier can be derived as

$$P_{\mathrm{M/A}} = \frac{1}{2}\mathrm{Re}\{V_{\mathrm{M/A}}[1] I^*_{\mathrm{M/A}}[1]\} = \frac{1}{2}|I_{\mathrm{M/A}}[1]|^2 \mathrm{Re}\{Z_{\mathrm{M/A}}\}. \tag{4.11}$$

Note that Z_{M} and Z_{A} expressed in Eqs. (4.5) and (4.6) can be complex numbers. Then, the DC power is calculated by multiplying V_{DD} with the corresponding DC current extracted using the

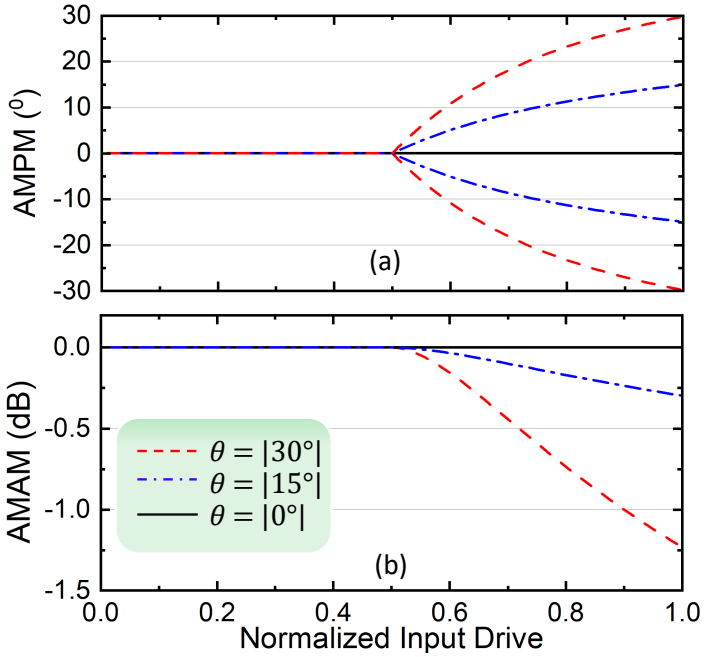


Figure 4.4: Calculated QB-DPA behaviors due to the θ dispersion for: (a) AM-PM, (b) AM-AM.

Class-B model [89, 92]. The normalized load resistance and efficiency are then calculated with a variation of θ. Fig. 4.3 indicates that once the phase variation due to the OMN and parastics can be controlled within $\pm 15°$, above 70% back-off and 78% peak efficiency can be maintained with main and auxiliary devices both described using piece-wise linear model, while a slightly distorted Doherty profiles are observed for the main and auxiliary PAs. Beyond the tolerable phase range of $\pm 15°$, a further degradation of Doherty performance occurs, which no longer provides sufficient efficiency enhancement at power back-off, e.g., $\theta = \pm 30°$ in Fig. 4.3. Moreover, the phase offset can be properly controlled through OMN design in order to generate a pre-distorted AMPM response to compensate for the overall DPA's AMPM distortion due to LM [24, 89], as is shown in Fig. 4.4. Meanwhile, less than 0.3 dB of AMAM distortion is achieved within $\pm 15°$ of θ variation, which is favorable for a linear DPA design. The above analysis applies for both parallel and series mode for their symmetry.

The theoretical model is verified using an emulated circuit model of the QB-DPA as shown in

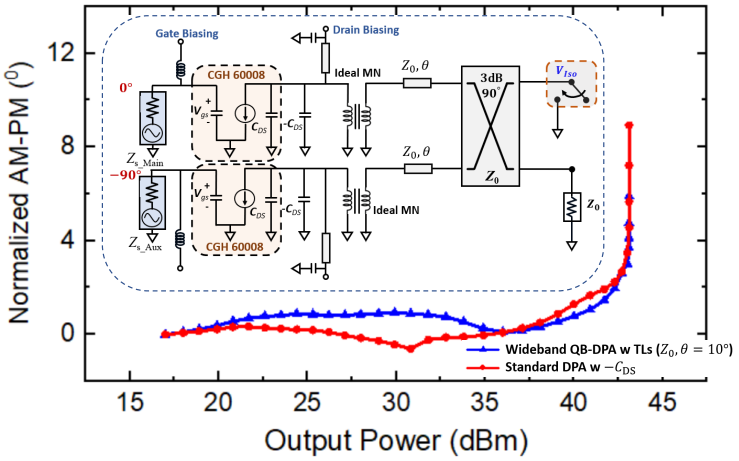


Figure 4.5: Simulated AM-PM responses using emulated QB-DPA circuit model [1] for different values of phase dispersion.

Fig. 4.5. The development of such an emulated circuit model has been elaborated in [1], in which bare-die transistor models are de-embedded by incorporating static negative parasitic components, e.g., $-C_{\mathrm{DS}}$. The AMPM responses are simulated with different phase dispersion values. It can be seen that the generic QB-DPA with $0°$ phase dispersion (red curve in Fig. 4.5) can suffer from large AMPM distortion, especially during load modulation, which is primarily due to the non-linear parasitics. Nevertheless, the AMPM (blue curve in Fig. 4.5) can be considerably linearized with proper phase dispersion from the main/auxiliary matching circuits, which generates a reverse AMPM distortion during load modulation to cancel the effect of non-linear parasitics as indicated by Fig. 4.4(a).

Note that the quadrature coupler can be designed as an impedance transformer as depicted in Fig. 4.5 [93], and thus, simplified matching circuits can be utilized to maintain a low phase dispersion (e.g., $< 15°$) over a wide frequency range. As such, the QB-DPA architecture can be extended to wideband operation with minimal impact on the Doherty load-modulation behavior and back-off efficiency enhancement. More importantly, the unique mismatch-resilient characteristic of QB-DPA can be effectively sustained over the same broad bandwidth through parallel/series

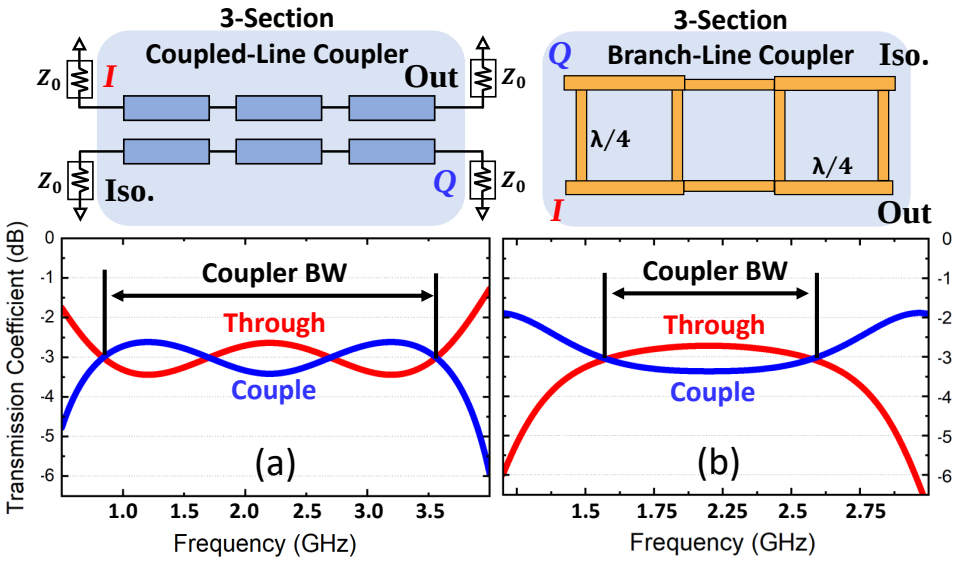


Figure 4.6: Wideband coupler with transmission coefficients: (a) coupled-line coupler, (b) branch-line coupler.

reconfiguration.

4.2.3 Exchangeable Biasing for Bandwidth Extension

Another factor that restricts the bandwidth extension in this coupler-based QB-DPA architecture is the frequency-dependent variation of the wide-band coupler as Doherty combiner. Two widely-used broadband couplers are analyzed to evaluate how the realistic coupler's frequency fluctuation impairs the DPA bandwidth. As shown the transmission (I) and coupling (Q) coefficients in Fig. 4.6(a), around 130% fractional bandwidth can be realized for a coupled-line coupler with four ports terminated to Z_0. However, in the parallel Doherty configuration, the main port connected to coupler is set to $2Z_0$, the auxiliary port is open-circuited at the back-off power region, and the isolation port is also open circuited, as shown in Fig. 4.7(a). The transmission coefficient between main-amplifier port and output port is shown with the red curve in Fig. 4.7(b), which clearly indicates that the bandwidth is significantly compromised as compared to the original coupler. To fully

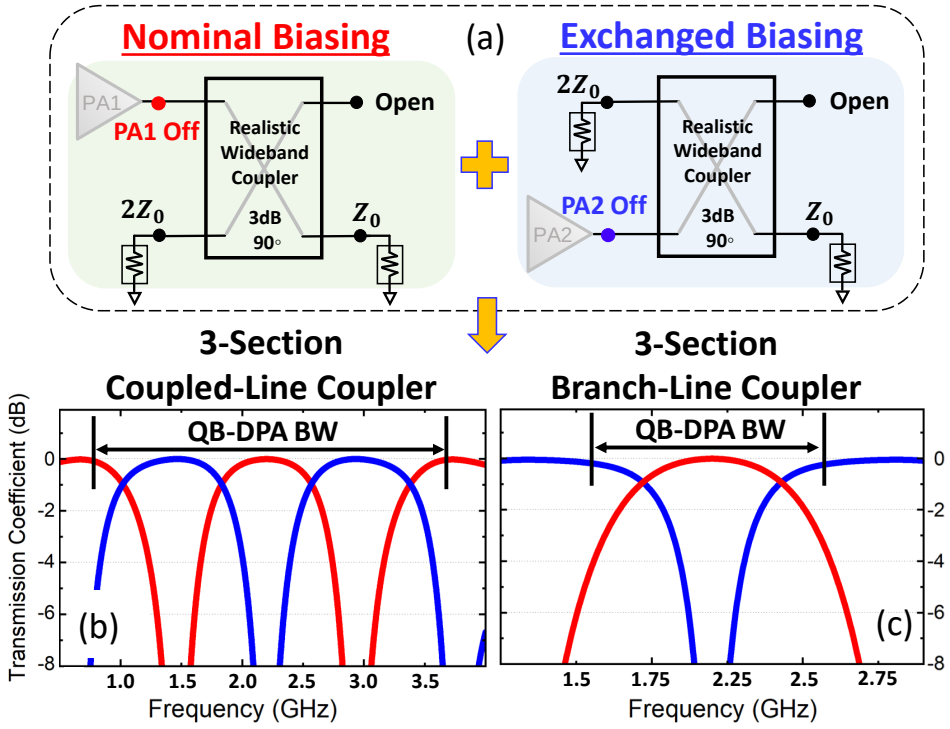


Figure 4.7: Wideband QB-DPA at parallel mode: (a) back-off power equivalent circuit with nominal/exchanged biasing, and bandwidth extension with combiner of (b) coupled-line coupler, (c) branch-line coupler.

utilize the achievable bandwidth of coupler, an approach of reciprocal biasing through exchanging the main/auxiliary settings is proposed. The transmission capacity can be restored with a complementary response over frequency as the blue curve illustrated in Fig. 4.7(a). With a combination of two biasing modes, the full coupler bandwidth can be exploited for Doherty design. The similar phenomenon is also observed for branch-line coupler, as presented in Fig. 4.6(b) and Fig. 4.7(c). Overall, by leveraging the exchangeable biasing, the frequency fluctuation due to the wideband coupler can be largely eliminated and then a broadband QB-DPA architecture is achieved. It is worthy to note that the above analysis is based on parallel QB-DPA, and it is also valid for series QB-DPA due to the symmetry between the two modes. Compared with the similar biasing mechanism used in [94], the proposed exchangeable biasing method can be gracefully compatible with the parallel/series mismatch-resilient QB-DPA.

In summary, through mode reconfiguration and biasing-setting reciprocity, the unique capability of mismatch recovery of the QB-DPA architecture can be extended to a wideband implementation. Meanwhile, with proper OMN and coupler coordination to absorb the device parastics and minimize the phase offset, a high back-off and peak efficiency are assured over the wide operational bandwidth. This proposed reconfigruable broadband capacitively QB-DPA platform, is the first-ever developed load-modulation PA that against the wideband dynamic mismatch through simply reconfiguration of voltage bias control (main/auxiliary settings and open/short for isolation port).

4.3 Prototype Design and Demonstration

In this section, based on the proposed theory, the practical design methodology is presented to achieve wideband and mismatch-resilient QB-DPA. The prototype is designed using GaN devices (CGH40006P) targeting for a frequency range from 1.7 to 2.7 GHz. In this realistic design, the parallel QB-DPA is configured as the primary mode at matched condition, while the reconfiguration to series mode is triggered at certain mismatch conditions.

4.3.1 Design of Wideband Matching Network

For the wideband QB-DPA OMN design, the fundamental goal is to achieve optimal matching quality for Doherty load modulation over the target bandwidth and meanwhile minimize the phase dispersion. Fig. 4.8(a) describes the generic OMN of the QB-DPA architecture. The selected CGH 40006P devices' package parasitics are extracted and modeled based on [95]. To design the wideband OMN, a variety of matching networks are investigated. In Figs. 4.8(b)$-$(d), the conventional multi-stage with different number (n) of stages low-pass and high-pass networks as well as their hybrid combination are designed together with the parasitics to perform an ideal

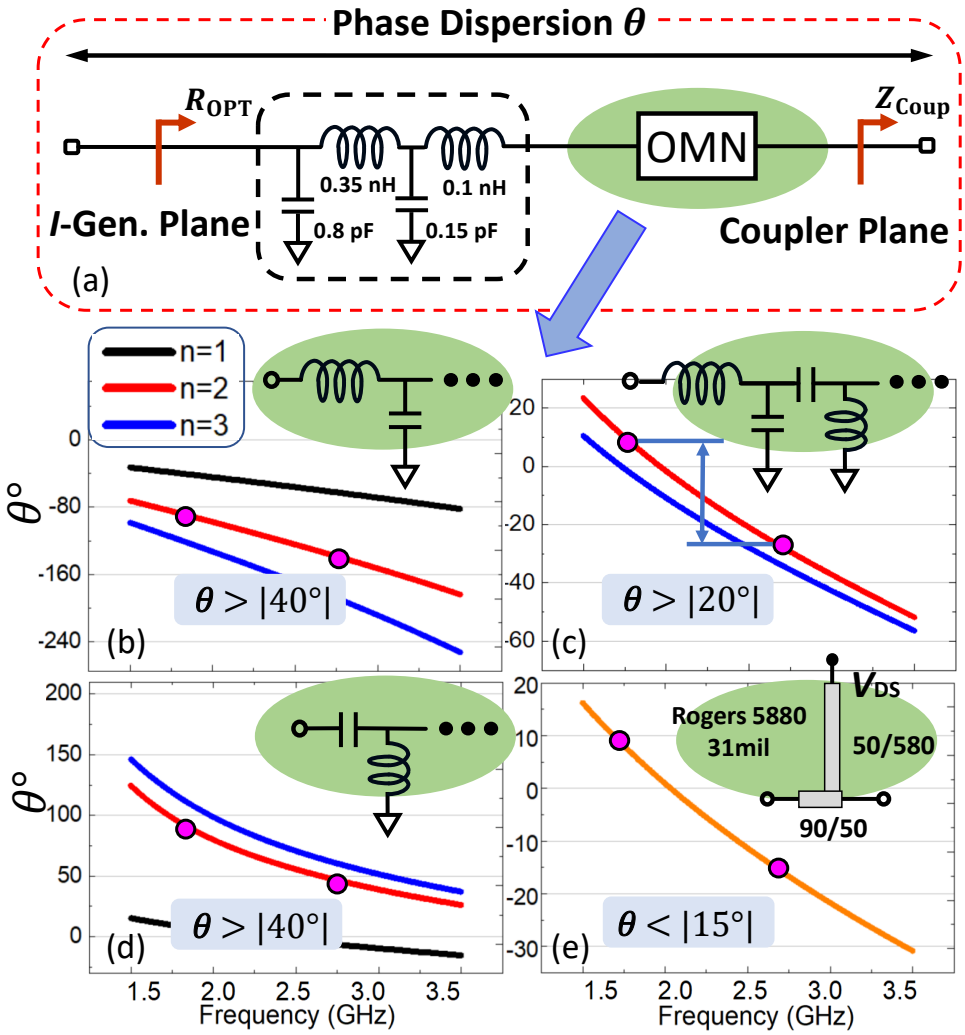


Figure 4.8: Analysis of the wideband OMNs and phase dispersion from current source plane to coupler plane: (a) concept of OMN design, (b) low-pass OMN, (c) low-pass plus high-pass OMN, (d) high-pass OMN and (e) proposed OMN.

impedance transformation from coupler plane ($Z_{\text{Coup.}}$) to intrinsic I-generator plane (R_{OPT}). For the OMN with only low-pass or high-pass, a two-stage design leads to a large phase dispersion of $|\theta| > 40°$ over the entire frequency range, which is not suitable for achieving the desired Doherty performance according to the mathematical analysis in Sec. 4.2.2. The two-stage OMN with hybrid low-pass/high-pass design also yields an unwanted phase dispersion of $|\theta| > 20°$ at the higher half of the target frequency range.

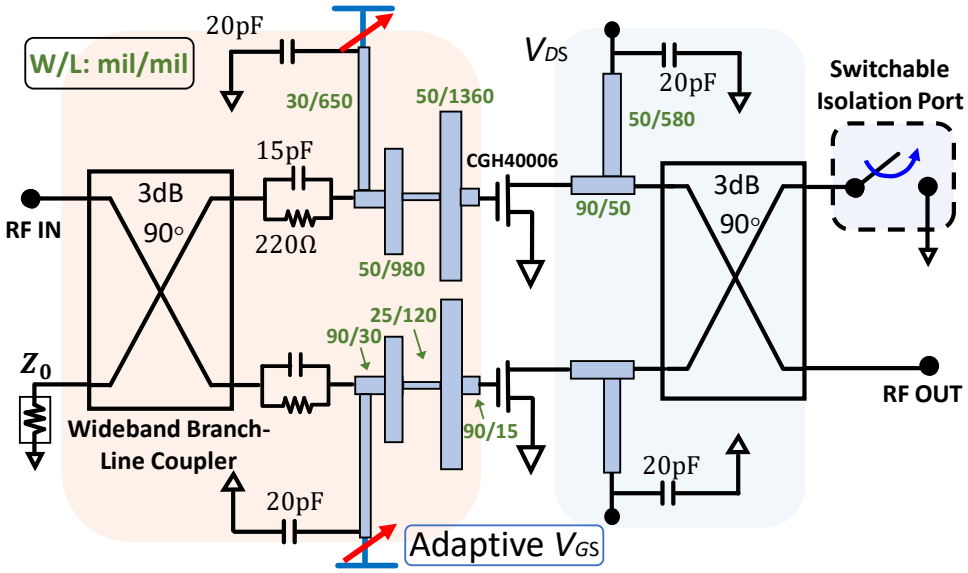


Figure 4.9: Full Schematic of the designed wideband mismatch-resilient QB-DPA architecture.

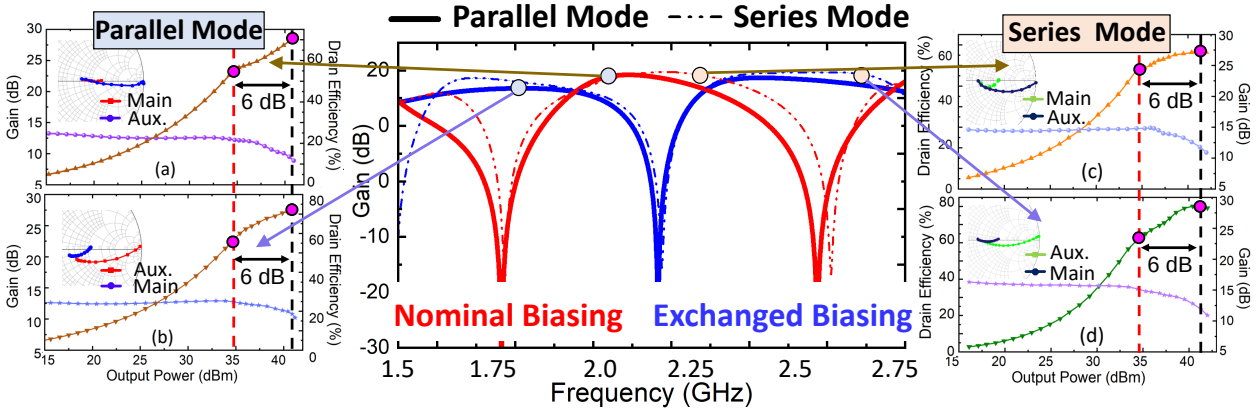


Figure 4.10: Small-signal and large-signal simulation results for wideband QB-DPA in parallel and series modes and with nominal/exchanged biasing.

On the other hand, it is discovered that the single-stage high-pass or low-pass OMN can offer the minimized phase dispersion. Thus, an quasi-single-stage OMN is proposed with a simple biasing line acting as a shunt inductor and a series tuning TL in Fig. 4.8 (e). The proposed OMN can effectively compensate for the parasitics across the operational bandwidth, and it can meanwhile offer a good matching quality over the target bandwidth in conjunction with the characteristic

impedance of quadrature coupler $Z_{\mathrm{Coup.}}$. Realistically, the 3-section wideband quadrature coupler is designed with an arbitrary real impedance, and the output port can be transformed to Z_0 with an wideband matching network. In this design with the 6-W GaN transistors, $Z_{\mathrm{Coup.}}$ is finally designed to $Z_0 = 50\Omega$ as the optimal value. As depicted in Fig. 4.8 (e), the overall phase offset θ from intrinsic I-generator plane to coupler plane is maintained within the tolerable range of $\theta < 15^\circ$ to result in a wideband Doherty performance. It is important to point out that this parasitics compensation methodology is generally applicable for different GaN transistors with similar parasitic networks by adjusting the design parameters [1, 96]. For the high-power PAs with a low optimal resistance $R_{\mathrm{OPT}} < 50\Omega$, the impedance transformation can be primarily provided by the quadrature coupler [97]. Thus, this "single-element" matching technique is capable to maintain a low phase dispersion for any $R_{\mathrm{OPT}} < 50\Omega$.

It is worthy to note that the overall OMN of the main/auxiliary paths are designed identically for mode reconfiguration that ensures a consistent QB-DPA performance between parallel and series modes in terms of OP_{1dB}, gain, efficiency and linearity profile (AM/AM and AM/PM) [68, 89]. Meanwhile, by means of the symmetrical topology, the phase delays of main and auxiliary paths are automatically equalized at the saturation power level, leading to the maximized power combining efficiency. The same wideband coupler is designed at the input side together with a two-stage low-pass input matching [98] transforming the 50-Ω across target bandwidth. Note that the wideband quadrature coupler can also be realized in many ways, e.g., using slow-wave structure as study in [99] for a miniaturized size and decent loss performance. To stabilize the designed QB-DPA architecture, both a RC network in series with the transistor and a resistor at the gate bias feed line are placed at main and auxiliary paths. Thereafter, the entire circuit is co-simulated with the transistors, components, and electromagnetic models of layout using Keysight ADS. The full circuit schematic is presented in Fig. 4.9 with all the circuit parameters illustrated.

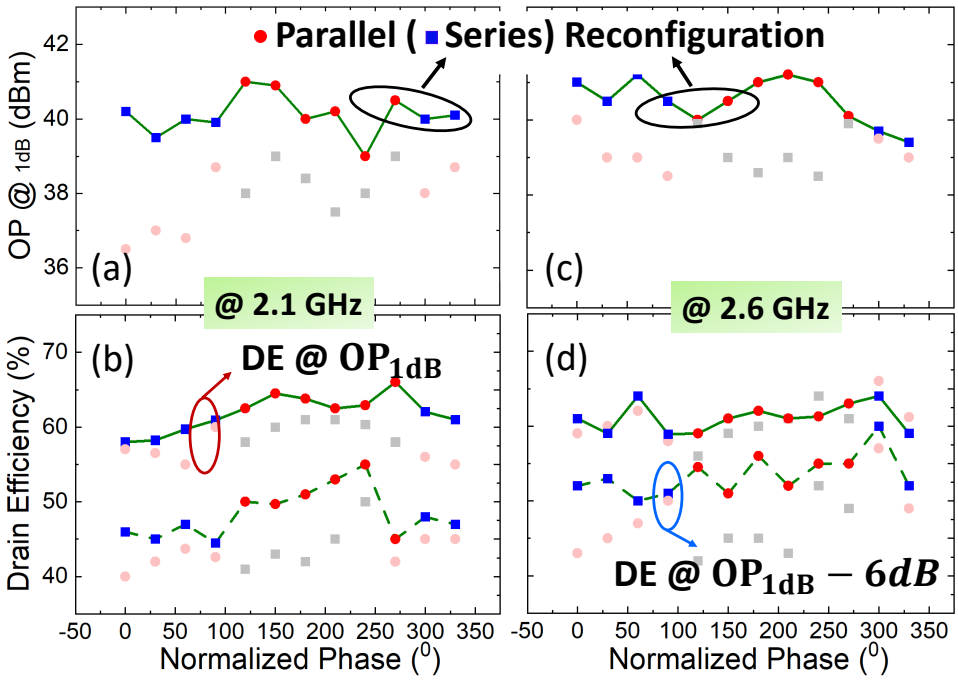


Figure 4.11: Simulation performance of wideband QB-DPA under $2:1$ VSWR for $\mathrm{OP}_{1\mathrm{dB}}$ and drain efficiency at $\mathrm{OP}_{1\mathrm{dB}}$ and 6-dB back-off region for (a) and (b) at 2.1 GHz, (c) and (d) at 2.6 GHz.

4.3.2 Exchangeable Biasing for Multi-Band Operation and Parallel/Series Reconfiguration Against Load Mismatch

The output matching and combiner networks set the foundation for the wideband QB-DPA architecture, while the reconfiguration between parallel & series modes and nominal & exchanged biasing is the key enabler to allow simultaneously broadband operation and mismatch resilience. Practically, the alternation between parallel and series QB-DPA can be realized through exchanging gate biasing and switching the isolation-port loading of output coupler by a RF switch. Meanwhile, the reciprocal reconfiguration between nominal-exchanged biasing is simply realized by swapping the role of main and auxiliary PAs within a single QB-DPA mode, e.g., the primary parallel mode. In the previous research [68, 89], the RF switch design and implementation at the isolation port for mode reconfiguration has been thoroughly elaborated, which is not repeated in this work. Thus, the

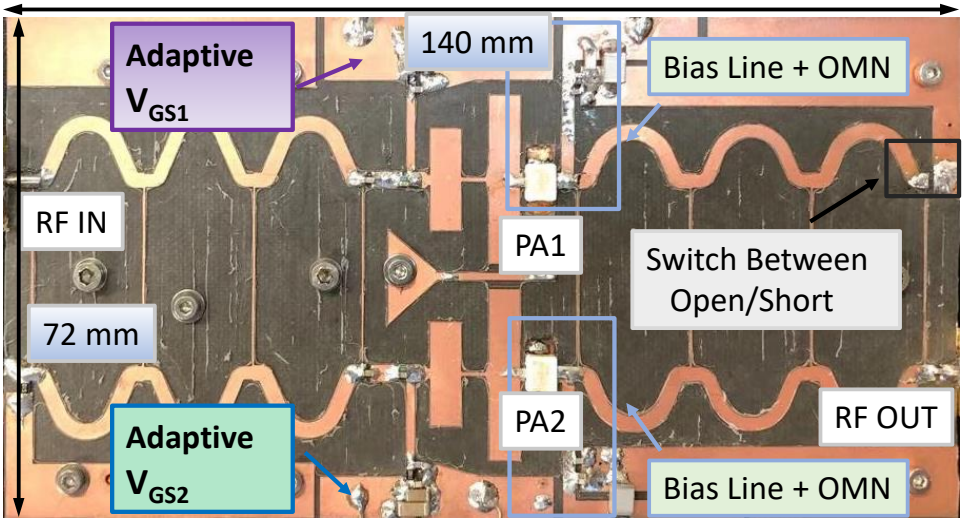


Figure 4.12: Top view of the fabricated PCB board.

switching from parallel to series mode in this prototype demonstration is performed by manually placing a bypass capacitor at the isolation port of output quadrature coupler.

The wideband performance of designed QB-DPA is firstly investigated at matched load condition. Fig. 4.10 presents the small-signal and large-signal simulations with both parallel and series modes. The small-signal $S11$ in the middle plot of Fig. 4.10 clearly illustrates a complementary frequency response with nominal and exchange biasing settings, which is observed for both parallel and series modes. In large-signal simulation, a desired DPA LM (on the inset Smith Chart) and efficiency profile are shown around the center frequency with nominal biasing, as shown in Fig. 4.10(a). Through exchanging the roles of main auxiliary amplifiers, the rest of operational bandwidth can be covered as illustrated by the gain, efficiency and load trajectory behaviors in Fig. 4.10(b), which perfectly reflects the complementary responses of the reciprocal biasing. The same complementary large-signal results are also simulated for series mode at the center and edge frequencies as shown in Figs. 4.10(c) and (d). Further, under load mismatch of $2:1$ VSWR, the QB-DPA is simulated for parallel and series modes at 2.1 GHz and 2.6 GHz, respectively. Fig. 4.11 summarized the results for comparison. For parallel mode at 2.1 GHz shown in Figs. 4.11(a) and (b), using the same

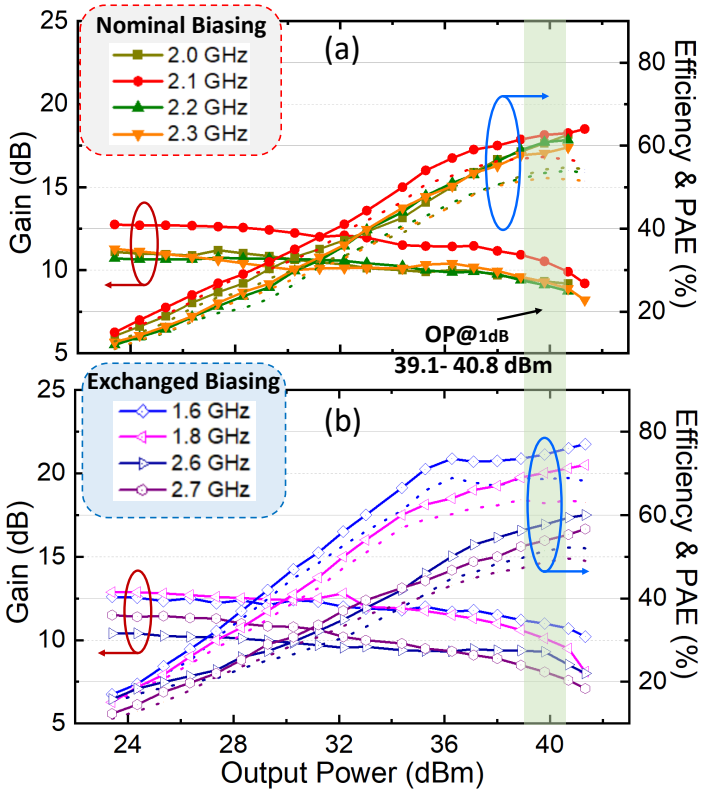


Figure 4.13: CW measurement of power-swept DE, PAE and gain over 1.6-2.7 GHz at matched-load condition for parallel QB-DPA.

bias setting as used in the 50-Ω condition, the QB-DPA suffers from clearly degradation of $OP_{\rm 1dB}$ and efficiency (both at $OP_{\rm 1dB}$ and 6-dB back-off). However, through reconfiguration, a nearly consistent $OP_{\rm 1dB}$ of the DPA ($39.2 - 40.9$ dBm) is achieved over the entire VSWR circle, and the drain efficiency at $OP_{\rm 1dB}$ and 6-dB back-off efficiency are improved to $> 59\%$ and $> 45.6\%$, respectively. It is interesting to point that the operational impedance regions for parallel and series modes calculated in theory (i.e., $|z_{\rm L}| > 1$ for parallel and $|z_{\rm L}| < 1$ for series) is still valid in the simulation. This mismatch recovery feature is demonstrated at 2.6 GHz as well in Figs. 4.11(c) and (d).

In the above design, the gate biasing voltages are set depending on both the operational frequency (nominal biasing for mid band and exchanged biasing for band edges) and mismatched load condi-

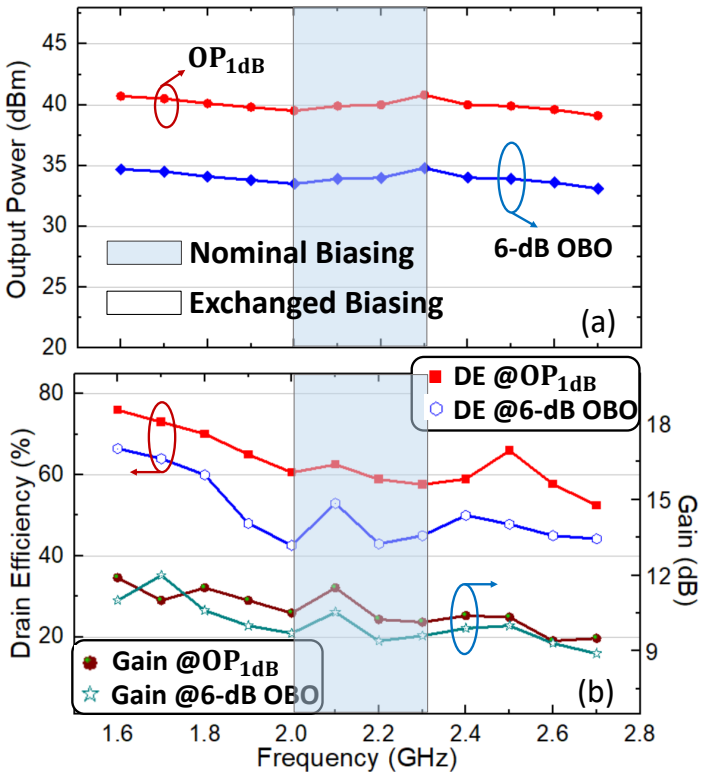


Figure 4.14: Frequency response with exchangeable biasing for (a) output power, (b) drain efficiency (DE) and gain.

tion (parallel for $|z_{\mathrm{L}}| > 1$ and series for $|z_{\mathrm{L}}| < 1$). Moreover, with the minimized phase dispersion of wideband matching networks, the simulation results well agree with the design equations described in Sec. 4.2.2.

4.4 Fabrication and Measurement Results

The designed circuit schematic is electromagnetically modeled using ADS Momentum simulator and co-simulated with active components to optimize the overall performance. The prototype QB-DPA is shown in Fig. 4.12 which is fabricated on the Rogers 5880 substrate with 31-mil thickness. Considering parallel QB-DPA as the primary mode, at the center frequency, PA2 is set as the main cell with V_{GS} to -2.9 V in class-AB, while PA1 is operated as the auxiliary cell with gate

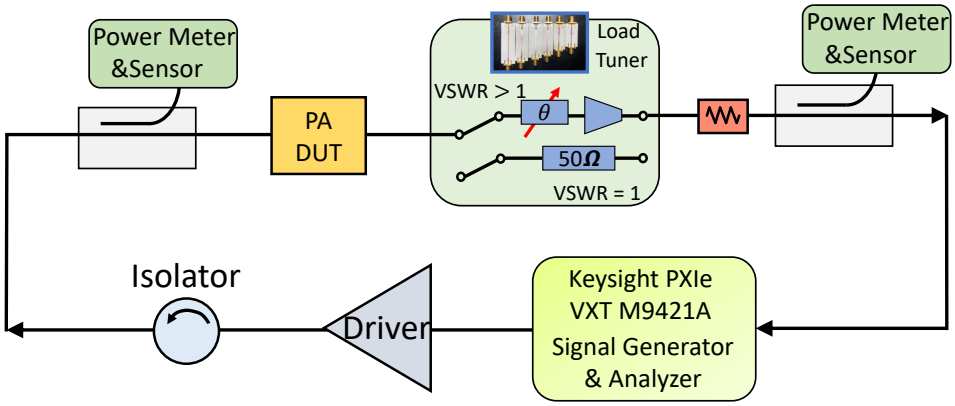


Figure 4.15: Measurement setup for characterization of the wideband QB-DPA under nominal 50-Ω and mismatched loading (VSWR $>$ 1) conditions.

bias of -4.8 V in class-C. The gate bias voltages of two PAs are exchanged and re-optimized experimentally at different frequencies and modes. The drain voltage is 28 V for both PAs. To experimentally verify the QB-DPA's wideband operation and mismatch-resilience, the designed QB-DPA is evaluated with both the continuous waveform (CW) and modulated signal, respectively.

4.4.1 Continuous-Wave Measurement

In the continuous-wave (CW) measurement, a single-tone power-swept input signal is generated to measure the QB-DPA performance at different power levels with a standard matched load impedance of 50-Ω. As the results shown in Fig. 4.13, a maximum efficiency of $58\% - 62\%$ is measured at OP_{1dB} with the nominal biasing setting from $2.0 - 2.3$ GHz, together with a $48\% - 51\%$ back-off efficiency at 6-dB OBO. To cover the rest of the operational bandwidth, the main and auxiliary gate bias voltages are swapped in the exchanged setting. Meanwhile, the measured peak efficiency is within a range of $56\% - 78\%$ over the complementary frequencies with the corresponding 6-dB OBO efficiency varying from $47\% - 67\%$. The PAE is presented as well with dot-line in Fig. 4.13 for the corresponding frequency. A clearly Doherty behavior is observed over the in-band frequencies that attributes to the nominal/exchanged biasing scheme. Further, a flat

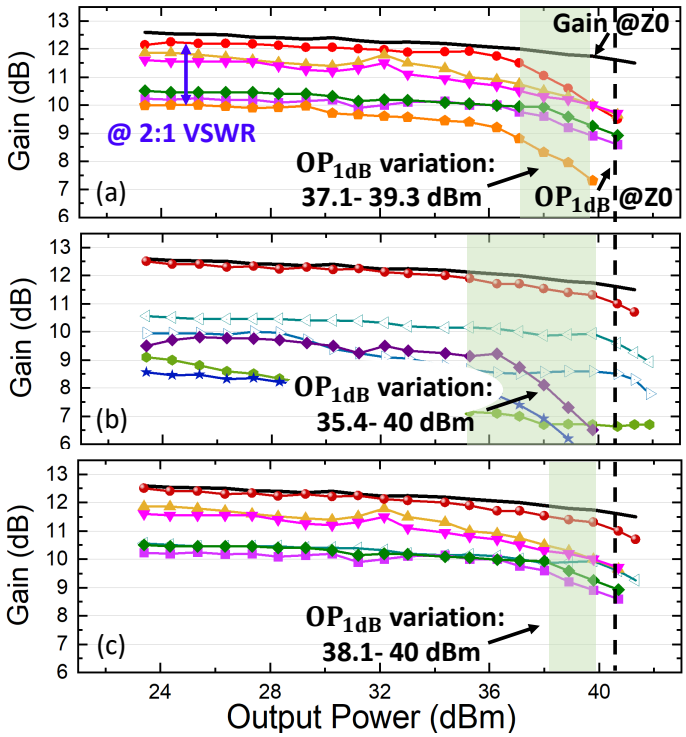


Figure 4.16: Measured $\mathrm{OP}_{1\mathrm{dB}}$ over 2:1 VSWR with CW signal at 1.7 GHz: (a) parallel only, (b) series only, (c) reconfiguration combination.

gain profile and $39.1 - 40.8$ dBm output power are obtained at $OP_{1\mathrm{dB}}$ in both biasing settings with the operation bandwidth extended from $1.6 - 2.7$ GHz, which are in good agreement with the simulation results in Fig. 4.10. Due to the symmetry, the CW measurement of series mode is not discussed here, while it will be performed in mismatched-load condition.

Next, to demonstrate the load-mismatch tolerance of QB-DPA architecture, the designed QB-DPA is further evaluated with a CW stimulus over the $2:1$ VSWR circle beginning from 1.7 GHz. The illustrative configuration of measurement setup is shown in Fig. 4.15. A driver amplifier (ZHL-5W-422+) provides sufficient input power, which is followed by an isolator. Two directional couplers are used to accurately sample and measure the input and output power. The DUT output is connected to a mismatched load which is swept over the entire $2:1$ VSWR circle using a delay line with variable length (swept from 0° to 180°) together with an $2:1$ impedance transformer. Finally,

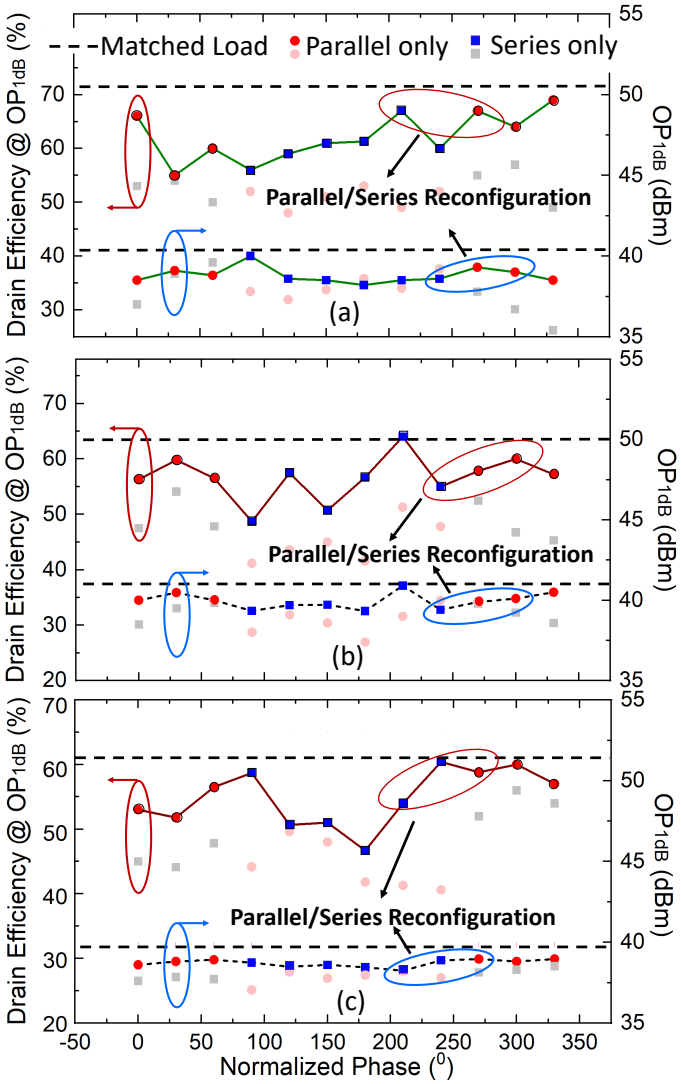


Figure 4.17: Measured DE and $\mathrm{OP_{1dB}}$ over 2:1 VSWR with CW signal at (a) 1.7 GHz, (a) 2.1 GHz and (c) 2.6 GHz.

a Keysight PXIe vector transceiver (VXT M9421) is used as CW/modulated signal generator and analyzer. Both parallel and series modes are test under the mismatch. The series QB-DPA mode is activated by connecting the isolation port to ground through a 20-pF RF bypass capacitor together with the gate biases swapped from parallel mode. As shown in Fig. 4.16 a single-mode QB-DPA suffers from excessive compression and AM–AM non-linearity for both the parallel/series modes, in which the gain profiles are extracted with the different phase points on the 2 : 1 VSWR

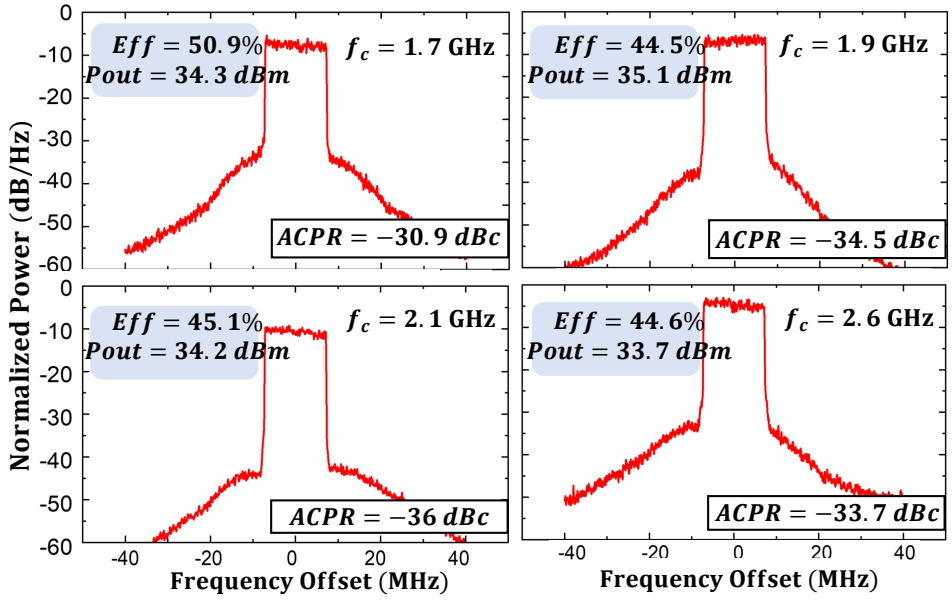


Figure 4.18: Modulation measurement under 20-MHz 64-QAM LTE signal over 1.7-2.6 GHz with 50-Ω load.

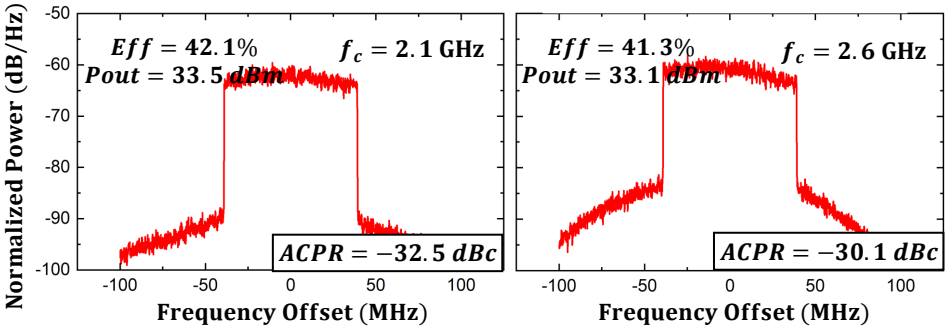


Figure 4.19: Modulation measurement under 80-MHz 5G-NR with 50-Ω load.

circle. Specifically, for parallel mode only, the OP_{1dB} variation is around 2.2 dB over 360° VSWR phases, and it is even worse for series mode where the gain variation can be as high as 4.6 dB. Nevertheless, through reconfiguration, a much more converged response with a nearly consistent OP_{1dB} of $38.1 - 40$ dBm is achieved over the full span of $2:1$ VSWR.

Then, the recovery capability of QB-DPA is further characterized at different frequencies in terms of the efficiency and P_{out} at 1-dB compression points under the same $2:1$ VSWR load mismatch. At center frequency 2.1 GHz in Fig. 4.17(b), the efficiency at OP_{1dB} can be significantly improved

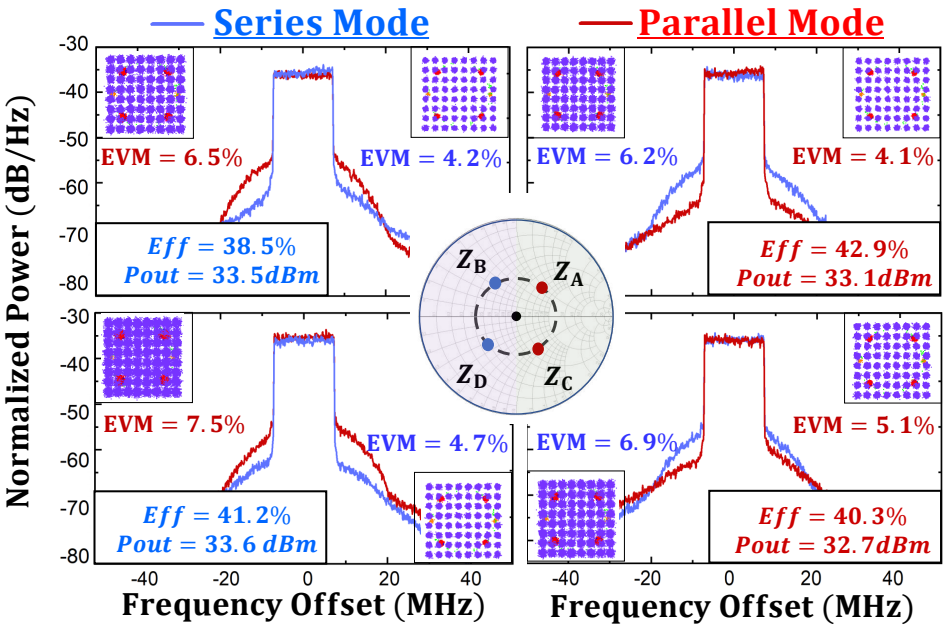


Figure 4.20: Measured ACPR, EVM, P_{OUT} and average efficiency over 2:1 VSWR with 64-QAM 20-MHz bandwidth signal at 2.1 GHz.

over the entire $2:1$-VSWR circle through modes reconfiguration with a well maintained consistent $OP_{1\mathrm{dB}}$ between $39.1-40.5$ dBm. Similar efficiency improvement and P_{out} recovery are measured at low-edge frequency 1.7 GHz and the high-edge side 2.6 GHz with mode reconfiguration as well. It is important to point out that the AM-AM and AM-PM can be distorted due to the load mismatch. Therefore, certain fine adjustment of biasing is needed to re-optimize the linearity of the dedicated DPA mode at different frequencies and load conditions. The above results clearly validate the wideband mismatch-recovery capability of the proposed QB-DPA technology.

4.4.2 Modulated Measurement

Similarly, the modulated measurement is started with the matched 50-Ω load condition at parallel mode. The dynamic performance, i.e., efficiency and linearity of the wideband QB-DPA, is firstly evaluated under 20-MHz modulation bandwidth using a single-carrier 64 QAM LTE signal

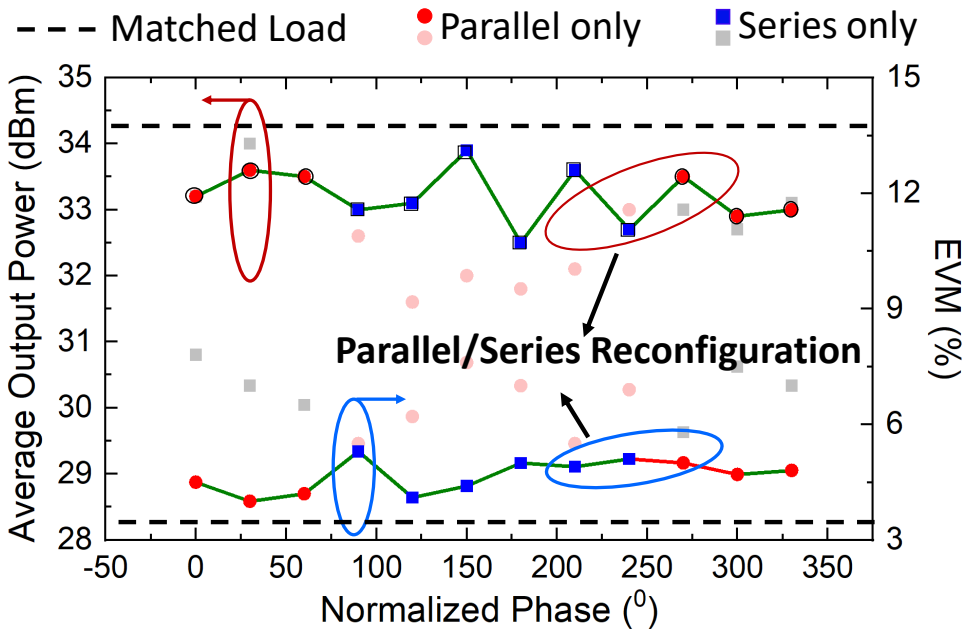


Figure 4.21: Modulated evaluation using 64-QAM 20-MHz bandwidth 4G LTE signal at $2:1$ VSWR at 2.1 GHz for average P_{OUT} and EVM.

with 9.6-dB PAPR. The measured power spectral density (PSD) and adjacent channel power ratio (ACPR) are depicted in Fig. 4.18 with various in-band frequencies are obtained. The lowest achievable ACPR is down to -36 dBc at the center frequency (2.1 GHz) without DPD applied. For the higher frequency where exchanged biasing triggered, the QB-DPA achieves an raw ACPR of -33.7 dBc with 44.6% efficiency at an average P_{out} of 33.7 dBm. A comparable efficiency, P_{out} and ACPR can be obtained for the lower in-band frequencies (1.7 and 1.9 GHz). A wideband 5G-NR 80-MHz modulated signal is characterized at center 2.1 GHz with nominal bias and exchanged the bias for 2.6 GHz as well. The proposed QB-DPA achieves average efficiency of 42.1%, and 41.3% with < -30.1-dBc ACPR around 33.1-dBm average P_{out} in Fig. 4.19.

The designed QB-DPA is further evaluated with single-carrier 64 QAM 20-MHz bandwidth modulated signal under load VSWR $2:1$ at 2.1 GHz to demonstrate the recovery of mismatch-induced degradation. The QB-DPA is tested with four symmetrical impedance points in Smith Chart on the $2:1$ VSWR circle. It should be noted that impedance points, $Z_{\mathrm{A-D}}$, plotted in Fig. 4.20 are

calibrated to the output port of the quadrature coupler. The measured $P_{\rm out}$, efficiency, ACPR and error vector magnitude (EVM) are presented for comparison. Specifically, at $Z_{\rm A}$ point, an inductive load with normalized impedance larger than 1 (i.e., $|z_{\rm L}| > 1$), the ACPR and EVM can be recovered when configured at parallel mode, with the average efficiency at 42.9% and $P_{\rm out}$ equals 33.1 dBm. While for $Z_{\rm B}$, where the normalized impedance $|z_{\rm L}| < 1$, the QB-DPA at parallel mode suffers from severely impairment of EVM and ACPR, which aligns with the degraded $OP_{\rm 1dB}$ observed in Fig. 4.11. In contrast, with parallel/series reconfiguration, the linearity-related specs are significantly improved with comparable achieved $P_{\rm out}$ and efficiency for both modes. Moreover, this effect can be validated for the capactive loads (e.g. $Z_{\rm C}$ and $Z_{\rm D}$) across the lower half part of the Smith chart as well. Similar to CW load mismatch measurement, the modulated EVM and average $P_{\rm out}$ can be significantly recovered versus load phase mismatch in Fig. 4.21, where the QB-DPA is characterized over 2:1 VSWR at -31-dBc ACPR (5.3% EVM). Through above CW and modulation measurements, the proposed QB-DPA achieves the competitive capability to restore the EVM, maintain a stable $OP_{\rm 1dB}$ and largely recover the efficiency when subjected to the load mismatch across the target bandwidth. In this design, the goal is to present the concept of wideband mismatch-resilient DPA, which is not targeted for any specific wireless standards. Thus, this article focuses on obtaining the best in-band performance specs, such as $P_{\rm out}$, PAE and EVM.

Table 4.1 summarizes the state-of-the-art of wideband QB-DPA compared to other mismatch-resilient PAs published recently. Besides its competitive achievements with 50-Ω load, the proposed PA demonstrates a wideband VSWR resilience across the full span of $2:1$ VSWR circle for the first time. Specifically, for the CW measurement, this design exhibits < 1.9-dB output power variation and $> 46\%$ efficiency at $OP_{\rm 1dB}$ over the designed bandwidth at $2:1$ VSWR. Meanwhile, comparing with the Doherty PAs in [89,90] using similar technology as in this design, the proposed QB-DPA achieves < 1.4-dB variation $P_{\rm out}$ and < -31 -dBc ACPR with modulation signal under mismatch, while maintaining a comparable average efficiency. Further, compared

with other contemporary narrow-band mismatch-resilient PAs [51, 85, 88], the designed QB-DPA still largely recovers the ACPR, average efficiency and reduces the P_{out} fluctuation, again well verifying the proposed theory.

Table 4.1: Comparison with State-of-the-Art of Recently-Reported Mismatch-Resilient PAs

Ref.	This Work				[17] TMTT-2021		[18] JSSC-2020		[20] TMTT-2021		[22] TMTT-2021		[23] TMTT-2021	
Technology	GaN-PCB				CMOS		CMOS		GaN-PCB*		LDMOS-PCB		GaN-PCB	
Freq (GHz)	1.7-2.7				26-42		39		3.6		0.9		3.5	
Load (Z_0/VSWR)	50Ω	2:1			50Ω	4:1**	50Ω	3:1	50Ω	2:1	50Ω	2:1	50Ω	2:1
		@1.7GHz	@2.1GHz	@2.6GHz										
OP_{1dB} (dBm)	39.1-40.8[II]	38.1-40	39.1-40.2	37.8-39.2	19.2	17.2*	20.2	18.5-19.1	43.5	42.6-43.4	29.4	29-29.6	40.7	38.8-40.4
DE @OP_{1dB} (%)	58-78	—	49-62	46-61	24[I]	16.5	33.3[I]	20.6-25.3	68[§]	54-64	59.1[§]	46.5-61.3	68.4[§]	51-59
Modulation Signal	64-QAM 20MHz				64-QAM 2GHz		64-QAM 3Gb/s		LTE 5MHz		64-QAM 3.8MHz		64-QAM 20MHz	
PAPR	9.6				—		—		5.5		6		9.6	
P_{out} (dBm)	33.7-35.1	32.6-33.9 @2.1 GHz			9.8	—	12.2	> 11.2	—		22	21.9-22.1	35	33-34.2
DE_{avg} (%)	44.5-50.9	38.1-42.9 @2.1 GHz			10.2[I]		16.1[I]	> 9.6	46.4	40.2-43	24.4	21-23	45	32.5-42.5
ACPR (dBc)	-36	-31 @2.1 GHz			-25		-25.4	< −22.8	-31.8	< −30.1	-48	-45	-41	—

*Graphically estimated ** Measured at one frequency [II] At center frequency [I] PAE [§] Peak efficiency

4.5 Conclusion

In this paper, a mode-reconfigurable QB-DPA platform is proposed for the first time with concurrent wide bandwidth and VSWR resilience. It presents a comprehensive theoretical analysis on the effects of OMN's phase dispersion on QB-DPA, the practical design of OMN to minimize the overall phase dispersion, and an exchangeable biasing scheme, all of which set the foundation for implementing broadband QB-DPAs. Meanwhile, the broadband design methodology well cooperates with the series/parallel reconfiguration that extends the operational frequency range of QB-DPA's mismatch resilience. A wideband QB-DPA prototype using GaN technology is designed and developed to verify the proposed concept ranging from $1.7-2.7$ GHz. In the case with standard 50-Ω load, the CW experimental results exhibit a $56\%-78\%$ efficiency at OP_{1dB} and $47\%-71\%$ 6-dB OBO back-off efficiency, respectively. Driven with a 20-MHz LTE modulated

signal with 9.6-dB PAPR, the measured PA achieves $44\% - 51\%$ average efficiency over the operation bandwidth and up to -36 -dBc ACPR at matched load condition together with a -32.5 -dBc ACPR achieved with 80-MHz 5G-NR signal. Moreover, when the PA loading is under $2:1$ VSWR, the designed QB-DPA can maintain a minimal variation of OP_{1dB} and gain as well as high linearity (EVM/ACPR) and average efficiency across the target bandwidth. For the realistic application scenarios, the output signal and the load impedance are sensed real time, and certain iterations by algorithms (searching for an optimal combination of DPA mode and gate biasing) can be performed to autonomously reconfigure the QB-DPA states. Alternatively, more cost-effective ways can be invented to reconfigure the PAs in the entire array. This is an emerging research area that falls out of the scope of this manuscript. Overall, the proposed wideband mismatch-resilient QB-DPA offers a compelling solution to realize a spectrum-efficient and performance-robust PA in MIMO system.

CHAPTER 5: SUMMARY AND OUTLOOK

As described in this dissertation, a novel Quasi-balanced Doherty power amplifier theory is proposed for the first time. The reconfiguration innovation is brought to the mismatch-resilient PAs that switched from balanced mode to Doherty modes (B2D) through a SOI voltage-controlled single-pole double-throw (SPDT) switch to counteract the dynamic load variations. Meanwhile, the mathematical equivalence between the conventional DPA and QB-DPA at Doherty mode offer a new design methodology of linear and efficient DPAs. Unlike the other ways that implement the output combiner of conventional DPA to improve the overall AMPM and AMAM specs, this proposed approach starts from linear standalone PA then through the proper combination to guarantee the power-dependent trajectory at intrinsic plane align with the standard Doherty load behavior. Then, by means of the AMAM characteristic of class-AB and class-C within the QB-DPA topology, a linear and efficient DPA can be obtained not only at nominal load but also provide tolerance for the varied VSWR scenarios.

The series and parallel QB-DPA theory is then proposed and established. Through reciprocally exchanging the main and auxiliary amplifiers and alternatively terminating the isolation port of the output coupler to a small reactance (close to short circuit) and susceptance (close to open circuit), the QB-DPA can significantly alleviate the load mismatch induced degradation. This unified theory provides a general methodology to design balanced, Doherty PAs and LMBA in a same core architecture. Furthermore, the reactive loadline solution to improve the PA efficiency and linearity reveals the potentials of implementation to performances and typologies at isolation of output coupler of the QB-DPA architecture.

As we described in the chapter 3, to improve the PAs' performance under mismatch, in addition to the conventional antenna isolation techniques, promising directions are implementation to tune

the PAs' loadline to accommodate the impedance VSWR. Besides the proposed QB-DPA theory, a broadband Doherty-like PA through active load pulling to a multi-port combiner is exploited to improve VSWR-related degradation at peak power. However, the presented architecture only allows Doherty-like performance across bandwidth with a 50-Ω load. More than 10% of power-added-efficiency (PAE) and 2-dB of output power degradation are reported for a single frequency operation over 4:1 VSWR circle. A coupler based hybrid series/parallel Doherty PA (DPA) is designed to contradict load mismatch through adaptive gate biasing, tunable phase offset at input and adjusted weighting of drain currents capability for main/auxiliary PAs . The practical implementation of this PA achieves a wideband small-signal $S21$ response at nominal load without large-signal and VSWR capability over the bandwidth. Above all, various techniques have been reported for mismatch-resilient PA design, while a complete methodology and physical demonstration haven't been proposed for PA with both high efficiency and linearity over a large impedance variation range and broad bandwidth. In chapter 4, based on the narrow-band QB-DPA theory, a new broadband reconfigurable QB-DPA design methodology is presented, which is able to maintain stable OP_{1dB} and mitigate dynamic VSWR fluctuations, while largely recovering the efficiency at back-off and peak power range over broadband operation.

In the future, several topics are proposed based on current research.

- **Topic 1:** For the realistic application of the reconfigurable QB-DPA, the antenna's impedance variation and true power delivered to the mismatched antenna loads are sensed real-time through the control loop to reconfigure the status of the QB-DPA for the optimal combination of QB-DPA mode and gate biasing. Power/impedance sensing scheme has been demonstrated via current/voltage detection of the coupler sensors [100, 101]. However, the methodology to close the feedback loop combing the sensing and control of the reconfigurable PA with an unprecedented latency (<5ms) and high speed is expected. By leveraging the unique

characteristics of series/parallel mode-switchable QB-DPA, together with the sensing circuit, control logic, and execution circuit, an autonomous reconfiguration of the mismatch-resilient QB-DPA system can be realized to minimize the power consumption and strongly facilitate the massive-scale integration.

- **Topic 2:** The current solution for the antenna mismatch is the controllable turner which is integrated between PA and antenna of the transmitter link. For the protection requirements, the PA turns off during the severe mismatch condition (VSWR $> 3:1$). Even reconfigurable PA can largely improve the performance degradation under mismatch, a sensing system is essential for the optimal operation condition search through the control loop with the algorithm. Therefore, a mismatch-resilient PA without complex sensing circuits and current/voltage process burden would be desirable. Meanwhile, the proper implementation of heat transfer due to the mismatch reflected wave imposed on the PA is also required in the future MIMO system.

- **Topic 3:** The hybrid load modulated balanced amplifier (HLMBA) is deemed to be a good candidate for amplifying high PAPR signal ($>$ 10 dB) with back-off efficiency enhancement. It also presents an excellent ACPR in [96] due to the linearization techniques utilized at QB-DPA stage. A novel PA architecture that incorporates feature of mismatch-resilience and large-dynamic-range is expected.

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