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Single-Phase Five-Level Multilevel Inverter Based on a Transistors Six-Pack Module

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Abstract: This article introduces a single-phase five-level multilevel inverter based on six switches and two transformers. The proposed converter requires a single dc input source with low voltage. The disposition of switches makes it possible to build the converter with a transistors six-pack module off-the-shelves, traditionally used to build three-phase inverters, which simplifies the manufacturing process. The converter increases the voltage with two transformers; for that reason, it does not require an auxiliary step-up converter. The use of transformers (with the transformer's turns ratio) allows for using the same topology for several input voltage levels. To verify the operation of the proposed multilevel inverter, a computer-based simulation was performed with PSIM, a software that considers parasitic components. The results show that the proposed converter can work properly.

Keywords: power converter; transformer-based multilevel inverter; single-phase inverter

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1. Introduction

Power electronics has become a key technology for renewable energy applications, electric and hybrid electric vehicles, and the advancement of electric and electronic appliances. One of the most recent advances in power electronics has been the development of multilevel inverters (MLI) [1–5]. They are already an established solution for developing medium- and high-power electronics applications. MLI has been applied in applications of ac-dc rectification, dc-ac inversion, dc-dc conversion, and as variable speed drives with combined conversion schemes (i.e., dc-ac-dc) [6,7].

Some of the advantages of high-power MLI are: (i) The output voltage is provided in a stepped output function that can be filtrated with smaller components than a two-level output; for this reason, MLI are considered to have a good power quality, for example, in the case of their application as an active front end (AFE) rectifier, the input current has low harmonic distortion. (ii) Low-voltage stress on devices, as will be further discussed, in low-voltage applications is not a big problem, but in high-voltage applications, this is a major concern. Their capability to operate with a relatively high-power quality and a relatively low switching frequency leads to high efficiency and small magnetic components [6–8].

The first three topologies studied as MLI were: (i) neutral point clamped or diode clamped [9–11], (ii) the flying capacitor topology [12,13], and (iii) cascaded cells' topology [1–7]. Recently, the (iv) modular multilevel converter (MMC) [14–16] has proven to have many advantages and can be considered the fourth topology of the main family of converters, for which the main characteristics are their applications in high-power applications.

There is another kind of MLI topologies, where the main applications are low-power converters, and they are characterized by having a larger number of output voltage levels (compared to the high-power ones) with a relatively reduced number of switches. In

this article, we will call high-voltage MLI (HV-MLI) the converters of the first family and low-voltage MLI (LV-MLI) the converters of the second family.

The HV-MLI are applied in applications such as variable speed drives for large motors, static VAR generators, and grid-tied applications [1–8]. They can be used to make flexible ac transmission systems (FACTS) and power conditioners [17], and renewable energy applications [17–19].

The first member of the family of MLI was the neutral point-clamped or diode-clamped converter, initially introduced in [9]. Its basic configuration is shown in Figure 1a. Figure 1b shows the basic configuration of the flying capacitor MLI.

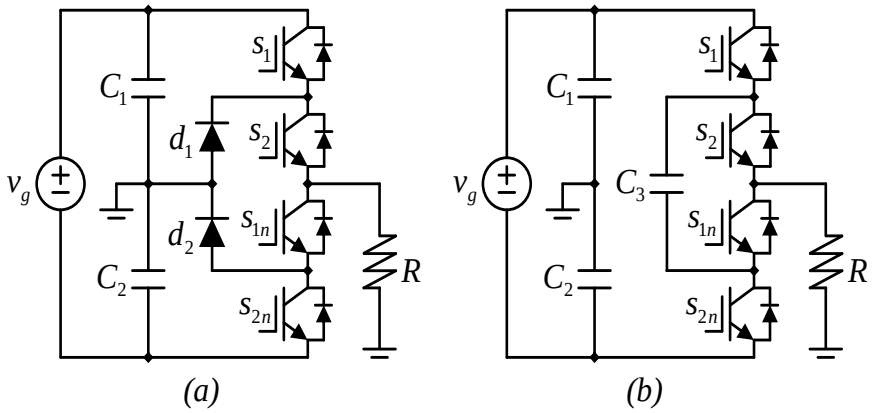


Figure 1. The two topologies of HV-MLI are (**a**) neutral point-clamped or diode-clamped and (**b**) flying capacitor or capacitor-clamped MLI.

The main advantage of the HV-MLI over the LV-MLI for medium- to high-power applications is that an HV-MLI has the same voltage stress on all switches, which is only a fraction of the output voltage. On the other hand, topologies of LV-MLI usually have a larger ratio of output voltage levels over the number of switches. Still, they usually have a larger ratio of voltage stress on devices over the output voltage. Furthermore, for low-voltage applications, HV-MLI has some limitations. Topologies with several voltage sources are more expensive than other low-voltage solutions (i.e., the traditional full-bridge inverter) since they require more than one input voltage source and require isolation among them. Topologies with a single voltage source usually require an additional mechanism to balance the voltage in capacitors.

This article introduces a single-phase five-level multilevel inverter based on six switches and two transformers. The proposed converter requires a single dc input source with low voltage, which is an advantage since no voltage balancing mechanisms are required. The disposition of switches makes it possible to build the converter with the widely known transistors six-pack modules since those packages are commercially available (off-the-shelves), and their use simplifies the manufacturing process. The converter increases the voltage with two transformers, for which the converter does not require an auxiliary step-up converter. The proposed converter features low-voltage stress on transistors. The main drawbacks are: (i) it uses two transformers; however, this allows using the same topology for several input voltage levels by changing the transformers' turn ratio, and (ii) if the switching method used is the line switching frequency, it requires an auxiliary boost converter to regulate the output voltage. Despite the requirements of an auxiliary converter to regulate the output voltage, most of the voltage gain can be performed with the transformer's turn ratios.

To verify the operation of the proposed multilevel inverter, a computer-based simulation was performed with PSIM, a software that considers parasitic components. The results show that the proposed converter can work properly.

2. The Proposed Topology

As mentioned before, the core of the switching stage is a full bridge or six-pack module of MOSFETS or IGBTs. Those six-pack modules are widely used to build low-power three-phase inverters (two levels); in this case, the inverter is a single-phase five-level inverter. Figure 2 shows a commercial six-pack module, indicating the output phases and dc input side, and the small connectors at the top are for gate drivers (a pair for each transistor).

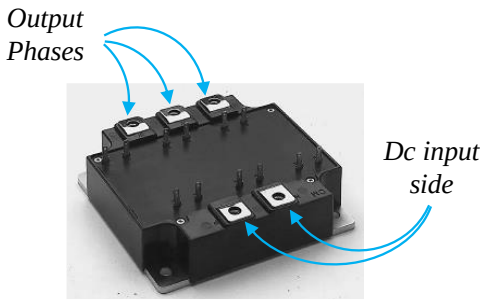


Figure 2. A commercial six-pack IGBT module.

Figure 3 shows the proposed five-level single-phase inverter in a full application. As mentioned before, the inverter requires its input to be regulated, and in this case, a dc-dc boost converter is used to regulate the voltage (an interleaved boost may be used if a large amount of power is handled).

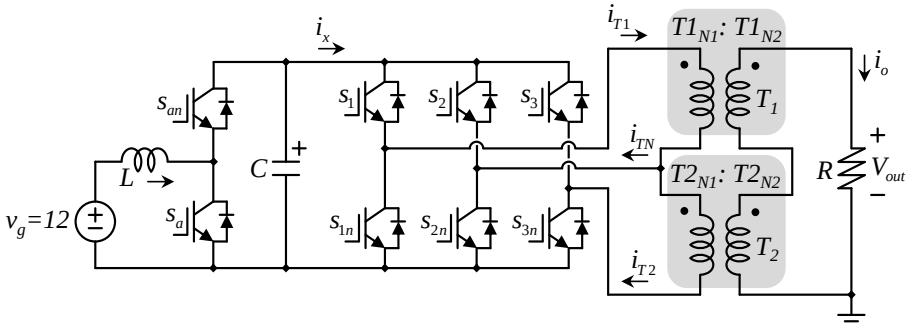


Figure 3. The entire conversion system with the proposed five-level inverter topology.

The six-pack is made, in this case, by s_1, s_2, s_3, s_{1n}, s_{2n}, and s_{3n}. The six-pack switching stage feeds two single-phase transformers, T_1 and T_2. The turn ratio can be selected according to the desired input and output voltage, and this can be customized according to the application. Let us consider that the power converter is made of a pre-regulator (boost converter), which is fed with a 12 V dc input. The boost converter regulates the voltage to feed the six-pack with 18 V and the inverter must generate a 127 V ac voltage (180 V peak). T_1 may have (for this example) a turn ratio of 1:10, while T_2 has a turn ratio of 1:5.

The six transistors are driven with three switching signals, and usually the two transistors of the same arm are complementary. The name of the transistors was assigned considering this. For example, s_1 is complementary to s_{1n}. When s_1 is closed, s_{1n} is open, and vice versa. This simplifies the description of the firing signals. We can describe the behavior with only three switching signals, considering that the other three are complementary. For the analysis, only the upper switching signals are described since the lower switches are the logical inverse of the upper ones.

The principle of operation of the proposed circuit can be explained in the following manner. If there are three firing signals that can take two possible states (zero or one), there is a total of eight possible switching states. The instantaneous output voltage depends on the state of the transistors, and each transformer can contribute with a positive, negative,

or zero voltage to the output, depending on how its primary winding is connected to the input voltage source.

Let us analyze the eight switching states one by one. We will consider the input voltage is the output of the boost converter, and it is regulated to 18 V, and the turn ratio of transformers is 1:10 for T_1 and 1:5 for T_2. Parameters may change depending on the applications, but it will help to explain the principle of operation.

From Figure 3, we can define the primary winding currents in terms of the output current and the transformer's turn ratio as in (1)–(3):

$$i_{T1} = \frac{T1_{N2}}{T1_{N1}} i_o. \tag{1}$$

$$i_{T2} = \frac{T2_{N2}}{T2_{N1}} i_o. \tag{2}$$

$$i_{TN} = i_{T1} - i_{T2} = \left(\frac{T1_{N2}}{T1_{N1}} - \frac{T2_{N2}}{T2_{N1}} \right) i_o. \tag{3}$$

Let us consider, for example, the input voltage of the transistor six-pack is the output of the boost converter, and it is regulated to 18 V. In this case, all transistors are rated to 18 V. Their current depends on two different factors, the loads' power factor and the switching state. Below, each switching state is analyzed to gain a better idea of the current through the switches.

2.1. The State {0, 0, 0}

When the three firing signals are zero, the three upper switches (s_1, s_2, and s_3) are open, and their complementary switches (s_{1n}, s_{2n}, and s_{3n}) are closed, and the circuit behaves like the one shown in Figure 4. Note that the primary winding of both transistors is in a short circuit, in other words, connected to zero voltage, for which their output winding provides zero voltage to the load. In this state, the output voltage is zero.

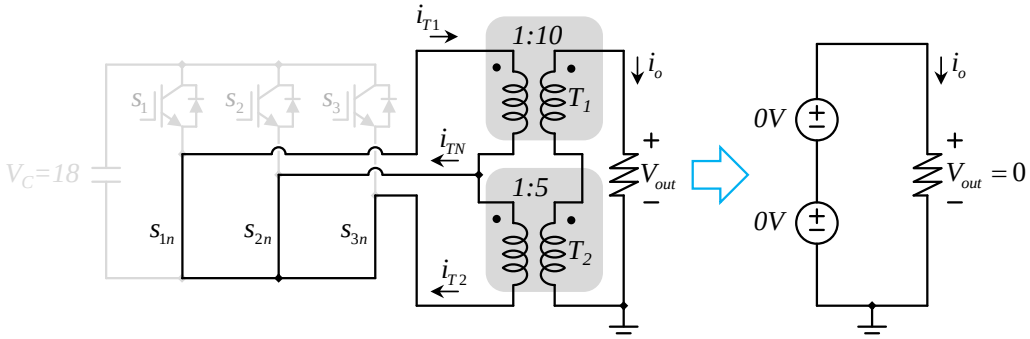


Figure 4. Equivalent circuit when $s_1 = 0$, $s_2 = 0$, and $s_3 = 0$ ($s_{1n} = 1$, $s_{2n} = 1$, and $s_{3n} = 1$).

The zero-voltage state does not mean that the load current is zero, and the output current has a path to flow in case an inductive load is connected. In this switching state, the current through transistors that are closed can be expressed in terms of the output current and the transformer's turn ratio as in (4)–(6):

$$i_{S1n} = i_{T1} = 10 i_o. \tag{4}$$

$$i_{S3n} = i_{T2} = 5 i_o. \tag{5}$$

$$i_{S2n} = i_{TN} = i_{T1} - i_{T2} = 5 i_o. \tag{6}$$

Notice that the output current may be different from zero even if the output voltage is zero. This would depend on the load's power factor. This state leads to zero current if the load is resistive; if the load is not resistive, it can be modeled as a current source that

may have either a positive or negative direction and the converter must be prepared to deal with any current direction (this effect is due to the power factor). In case the current is positive, the current paths on the converter would look like that in Figure 5a, otherwise it would look like that in Figure 5b.

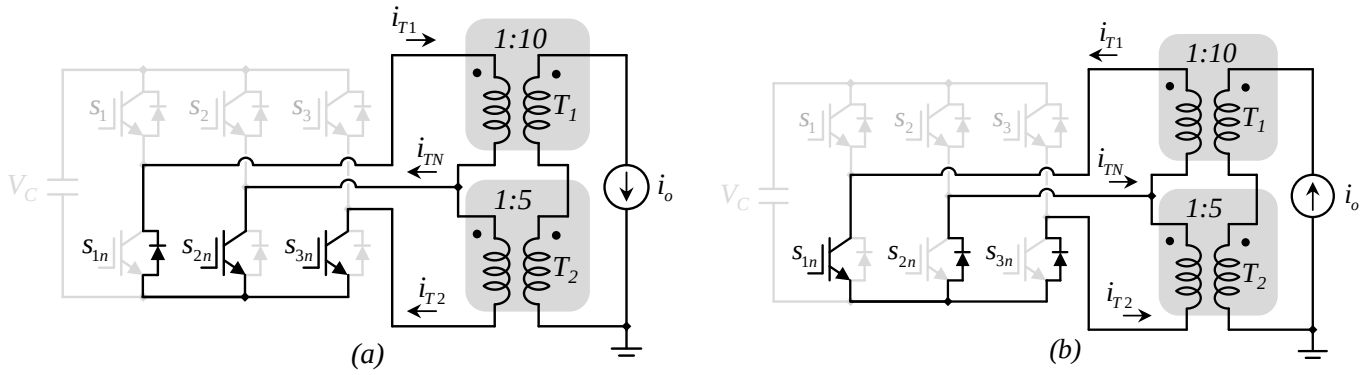


Figure 5. Current flow for different directions of the load current when $s_1 = 0$, $s_2 = 0$, and $s_3 = 0$. (**a**) when the load current is positive and (**b**) when the load current is negative.

Note that depending on the load current direction, in some switches, the current flows through the transistor, and in other cases it flows through the diode.

2.2. The State {0, 0, 1}

When the first two firing signals are zero and the third is one, two upper switches are open (s_1 and s_2) while s_3 is closed. Two lower switches are closed (s_{1n} and s_{2n}) while the third one (s_{3n}) is open. The circuit behaves like the one shown in Figure 6.

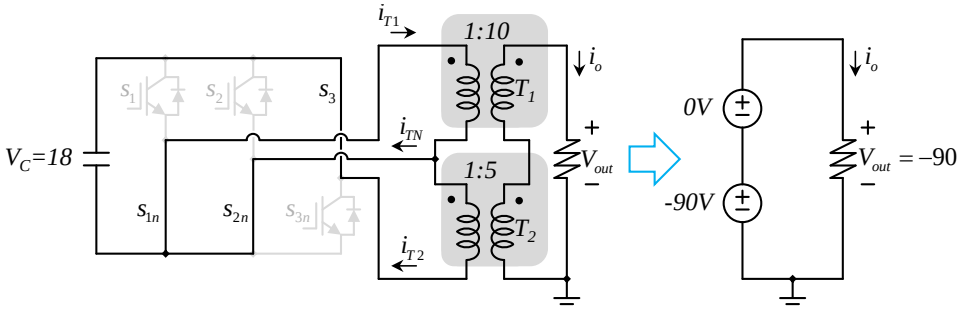


Figure 6. Equivalent circuit when $s_1 = 0$, $s_2 = 0$, and $s_3 = 1$ ($s_{1n} = 1$, $s_{2n} = 1$, and $s_{3n} = 0$).

The primary winding of the transformer T_1 is shorted (connected to zero volts), while the primary winding of the transformer T_2 is connected to the input source but in a way that provides a negative voltage (the dot coincides with the negative side of the power source). In this state, the inverter provides −90 V.

In this switching state, the current through transistors that are closed can be expressed in terms of the output current and the transformer's turn ratio as in (7)–(9):

$$i_{S1n} = i_{T1} = 10i_o. \tag{7}$$

$$i_{S3} = i_{T2} = 5i_o. \tag{8}$$

$$i_{S2n} = i_{TN} = i_{T1} - i_{T2} = 5i_o. \tag{9}$$

Similar to Figure 5, Figure 7 shows the current paths for the state {0, 0, 1}.

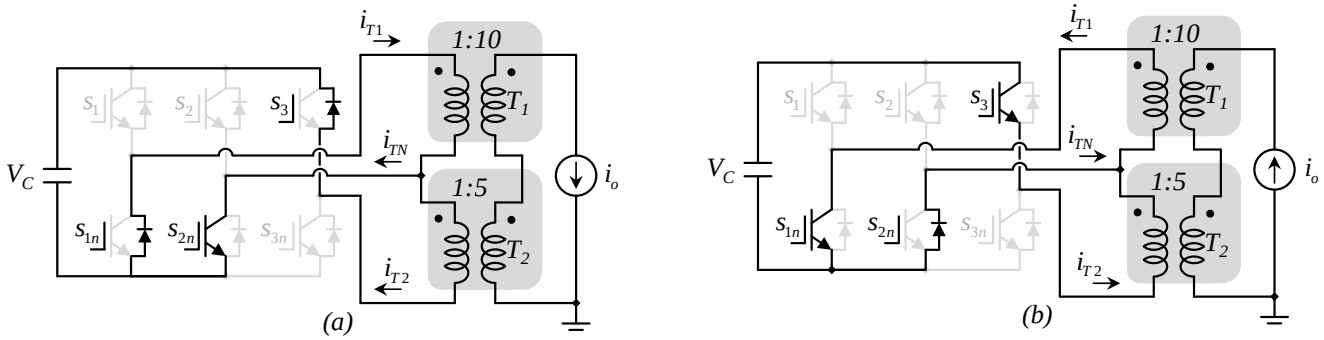


Figure 7. Current flow for different directions of the load current when $s_1 = 0$, $s_2 = 0$, and $s_3 = 1$. (**a**) when the load current is positive and (**b**) when the load current is negative.

As in the previous state, the converter must be able to operate with different output current directions to consider an operation with a power factor different than one. The load can be modeled as a current source. In case the current is positive, the current paths on the converter would look like that in Figure 7a, otherwise it would look like that in Figure 7b. Depending on the load current direction, in some switches, the current flows through the transistor, and in other cases it flows through the diode.

2.3. The State {0, 1, 0}

When the first and the third firing signals are zero, while the second one is one, two upper switches are open (s_1 and s_3) while s_2 is closed. Two lower switches are closed (s_{1n} and s_{3n}) while the third one (s_{2n}) is open, and the circuit behaves like in Figure 8.

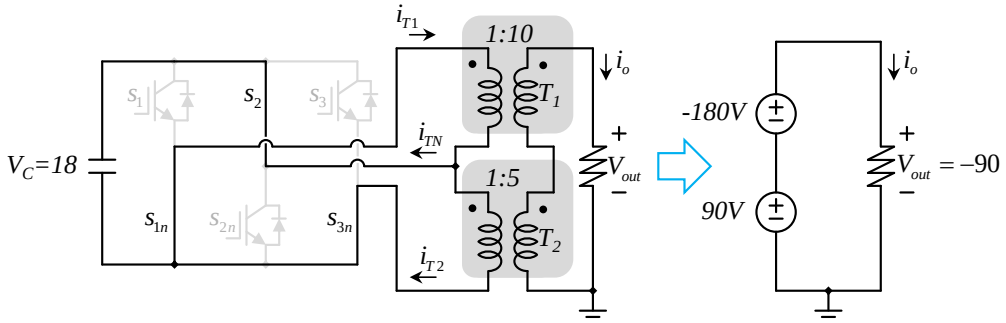


Figure 8. Equivalent circuit when $s_1 = 0$, $s_2 = 1$, and $s_3 = 0$ ($s_{1n} = 1$, $s_{2n} = 0$, and $s_{3n} = 1$).

The primary winding of the transformer T_1 is connected to the input source, but the dot at the primary winding coincides with the negative side of the input power source and T_1 provides a negative voltage (−180 V). In this state, the primary winding of the transformer T_2 is connected to the input source in a positive manner (the primary dot coincides with the positive side of the input power source). In this state, the inverter provides an output of 90 V.

In this switching state, the current through transistors that are closed can be expressed in terms of the output current and the transformer's turn ratio as in (10)–(12):

$$i_{S1n} = i_{T1} = 10i_o. \tag{10}$$

$$i_{S3n} = i_{T2} = 5i_o. \tag{11}$$

$$i_{S2} = i_{TN} = i_{T1} - i_{T2} = 5i_o. \tag{12}$$

As in previous states, the converter must be able to operate with different output current directions to consider an operation with a power factor different than one. The load can be modeled as a current source. In case the current is positive, the current paths on the converter would look like that in Figure 9a, otherwise it would look like that in Figure 9b.

Depending on the load current direction, in some switches, the current flows through the transistor, and in other cases it flows through the diode.

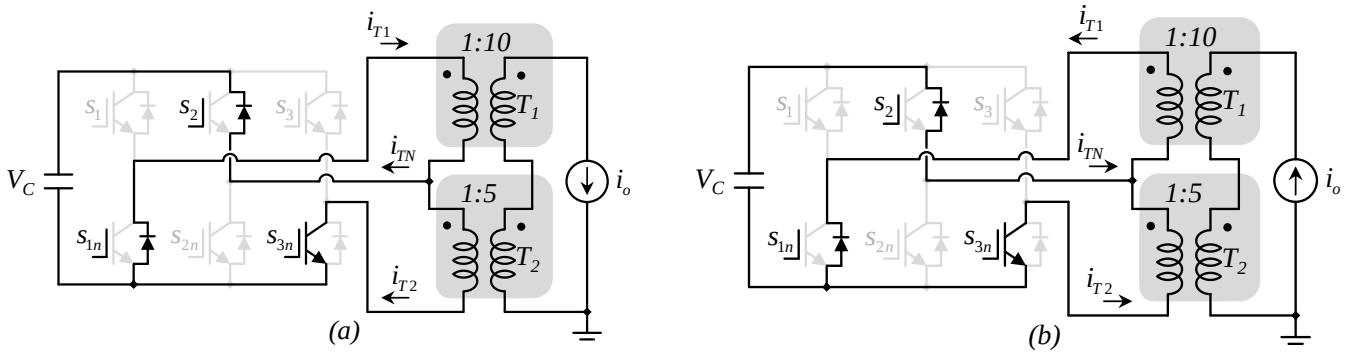


Figure 9. Current flow for different directions of the load current when $s_1 = 0$, $s_2 = 1$, and $s_3 = 0$. (**a**) when the load current is positive and (**b**) when the load current is negative.

2.4. The State {0, 1, 1}

When the first firing signal is zero, while the second and third are one, the first upper switch (s_1) is open, while the other two (s_2 and s_3) are closed. The first lower switch (s_{1n}) is closed, while the other two (s_{2n} and s_{3n}) are open. In this state the circuit behaves like in Figure 10.

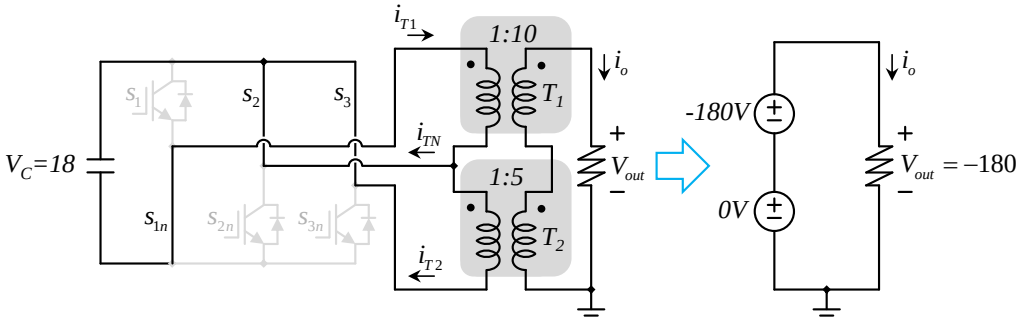


Figure 10. Equivalent circuit when $s_1 = 0$, $s_2 = 1$, and $s_3 = 1$ ($s_{1n} = 1$, $s_{2n} = 0$, and $s_{3n} = 0$).

The primary winding of the transformer T_1 is connected to the input source, but the dot at the primary winding coincides with the negative side of the input power source and T_1 provides a negative voltage (−180 V). The primary winding of the transformer T_2 is shorted or connected to zero volts (it is not contributing to the output voltage in this switching state). In this state, the inverter provides an output of −180 V.

In this switching state, the current through transistors that are closed can be expressed in terms of the output current and the transformer's turn ratio as in (13)–(15):

$$i_{S1n} = i_{T1} = 10 i_o. \tag{13}$$

$$i_{S3} = i_{T2} = 5 i_o. \tag{14}$$

$$i_{S2} = i_{TN} = i_{T1} - i_{T2} = 5 i_o. \tag{15}$$

As in previous states, the converter must be able to operate with different output current directions to consider an operation with a power factor different than one. The load can be modeled as a current source. In case the current is positive, the current paths on the converter would look like that in Figure 11a, otherwise it would look like that in Figure 11b. Depending on the load current direction, in some switches, the current flows through the transistor, and in other cases it flows through the diode.

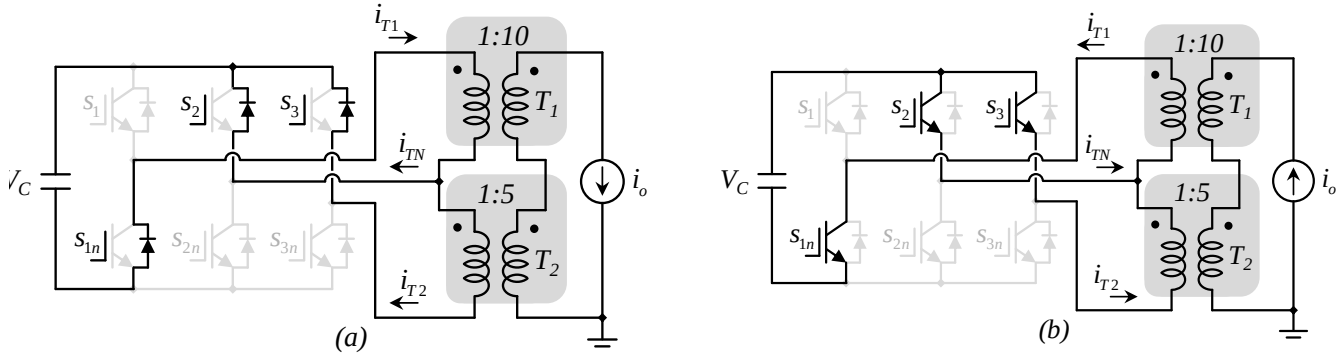


Figure 11. Current flow for different directions of the load current when $s_1 = 0$, $s_2 = 1$, and $s_3 = 1$. (**a**) when the load current is positive and (**b**) when the load current is negative.

2.5. The State {1, 0, 0}

When the first firing signal is one, while the second and third are zero, the first upper switch (s_1) is closed and the other two (s_2 and s_3) are open. The first lower switch (s_{1n}) is open, while the other two (s_{2n} and s_{3n}) are closed. In this state, the circuit behaves like in Figure 12.

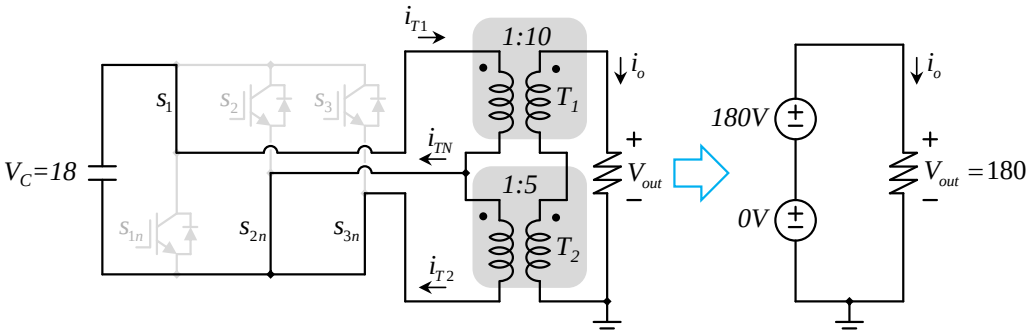


Figure 12. Equivalent circuit when $s_1 = 1$, $s_2 = 0$, and $s_3 = 0$ ($s_{1n} = 0$, $s_{2n} = 1$, and $s_{3n} = 1$).

The primary winding of the transformer T_1 is connected to the input source, in a positive manner (the dot is connected to the positive side of the input power source), then it provides 180 V to the output. The primary winding of the transformer T_2 is shorted or connected to zero volts (it is not contributing to the output voltage in this switching state). In this state, the inverter provides an output of 180 V.

In this switching state, the current through transistors that are closed can be expressed in terms of the output current and the transformer's turn ratio as in (16)–(18):

$$i_{S1} = i_{T1} = 10 i_o. \tag{16}$$

$$i_{S3n} = i_{T2} = 5 i_o. \tag{17}$$

$$i_{S2n} = i_{TN} = i_{T1} - i_{T2} = 5 i_o. \tag{18}$$

As in previous states, the converter must be able to operate with different output current directions to consider an operation with a power factor different than one. The load can be modeled as a current source. In case the current is positive, the current paths on the converter would look like that in Figure 13a, otherwise it would look like that in Figure 13b. Depending on the load current direction, in some switches, the current flows through the transistor, and in other cases it flows through the diode.

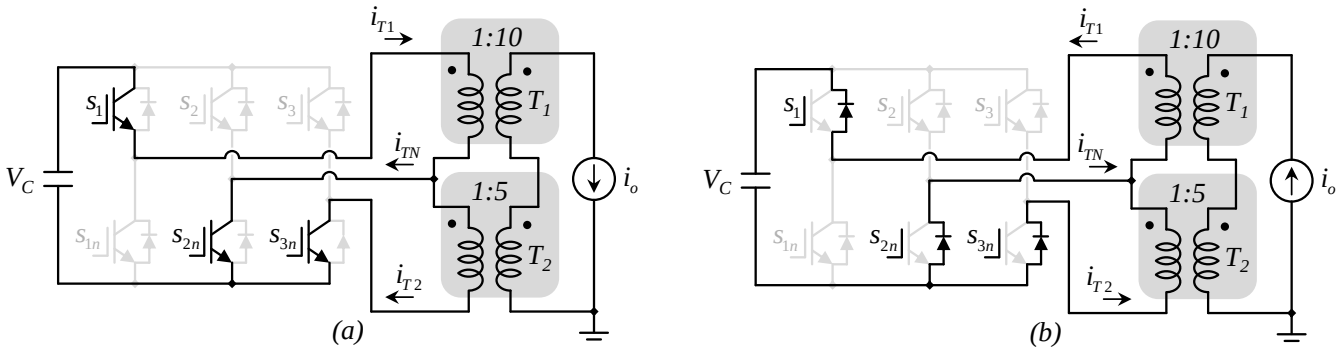


Figure 13. Current flow for different directions of the load current when $s_1 = 1$, $s_2 = 0$, and $s_3 = 0$. (**a**) when the load current is positive and (**b**) when the load current is negative.

2.6. The State {1, 0, 1}

When the first and the third firing signals are one, while the second signal is zero, the first and the third upper switches (s_1 and s_3) are closed while the second upper switch (s_2) is open. The first and the third lower switches (s_{1n}, and s_{3n}) are open, while the other switch (s_{2n}) is closed. In this state, the circuit behaves like in Figure 14.

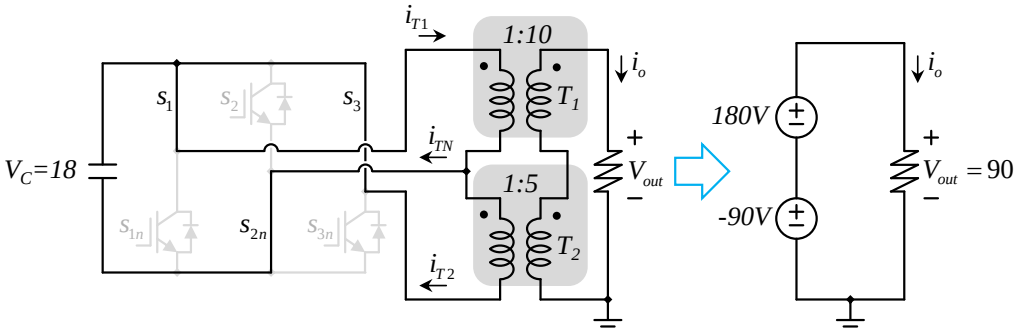


Figure 14. Equivalent circuit when $s_1 = 1$, $s_2 = 0$, and $s_3 = 1$ ($s_{1n} = 0$, $s_{2n} = 1$, and $s_{3n} = 0$).

The primary winding of the transformer T_1 is connected to the input source, in a positive manner (the dot is connected to the positive side of the input power source), then it provides 180 V to the output. The primary winding of the transformer T_2 is also connected to the input power source, but in a negative manner (the dot coincides with the negative side of the power source), and in this case, T_2 contributes with -90 V to the load. In this state, the inverter provides an output of 90 V.

In this switching state, the current through transistors that are closed can be expressed in terms of the output current and the transformer's turn ratio as in (19)–(21):

$$i_{S1} = i_{T1} = 10 i_o. \tag{19}$$

$$i_{S3} = i_{T2} = 5 i_o. \tag{20}$$

$$i_{S2n} = i_{TN} = i_{T1} - i_{T2} = 5 i_o. \tag{21}$$

As in previous states, the converter must be able to operate with different output current directions to consider an operation with a power factor different than one. The load can be modeled as a current source. In case the current is positive, the current paths on the converter would look like that in Figure 15a, otherwise it would look like that in Figure 15b. Depending on the load current direction, in some switches, the current flows through the transistor, and in other cases it flows through the diode.

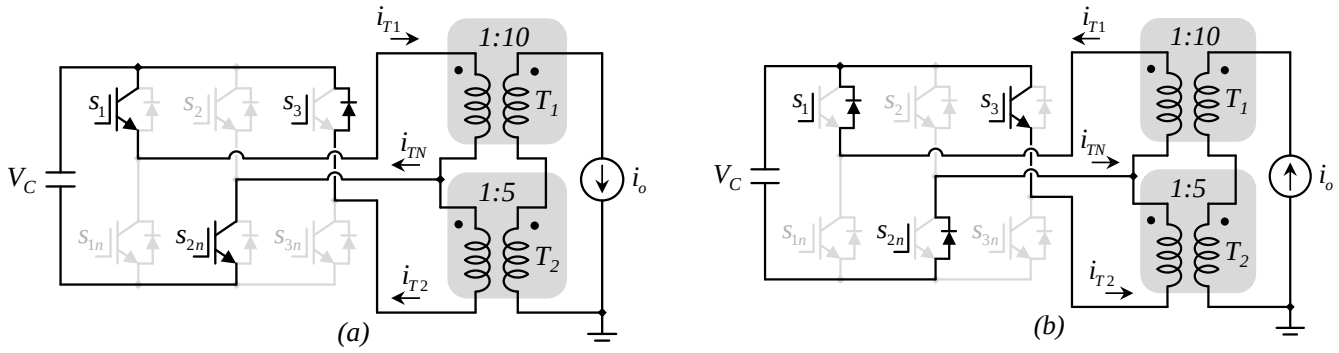


Figure 15. Current flow for different directions of the load current when $s_1 = 1$, $s_2 = 0$, and $s_3 = 1$. (**a**) when the load current is positive and (**b**) when the load current is negative.

2.7. The State {1, 1, 0}

When the first two firing signals are one, while the last one is zero, the first and the second upper switches (s_1 and s_2) are closed while the third upper switch (s_3) is open. The first and the second lower switches (s_{1n} and s_{2n}) are open, while the last one (s_{3n}) is closed. In this state, the circuit behaves like in Figure 16.

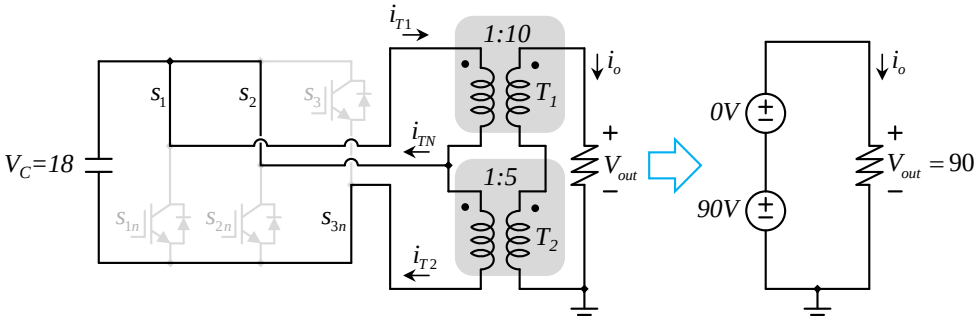


Figure 16. Equivalent circuit when $s_1 = 1$, $s_2 = 1$, and $s_3 = 0$ ($s_{1n} = 0$, $s_{2n} = 0$, and $s_{3n} = 1$).

The primary winding of the transformer T_1 is shorted and provides no voltage to the output side. The primary winding of the transformer T_2 is connected to the input power source in a positive manner (the dot coincides with the positive side), and in this case, T_2 contributes with 90 V to the load. In this state, the inverter provides an output of 90 V.

In this switching state, the current through transistors that are closed can be expressed in terms of the output current and the transformer's turn ratio as in (22)–(24):

$$i_{S1} = i_{T1} = 10i_o. \tag{22}$$

$$i_{S3n} = i_{T2} = 5i_o. \tag{23}$$

$$i_{S2} = i_{TN} = i_{T1} - i_{T2} = 5i_o. \tag{24}$$

As in previous states, the converter must be able to operate with different output current directions to consider an operation with a power factor different than one. The load can be modeled as a current source. In case the current is positive, the current paths on the converter would look like that in Figure 17a, otherwise it would look like that in Figure 17b. Depending on the load current direction, in some switches, the current flows through the transistor, and in other cases it flows through the diode.

2.8. The State {1, 1, 1}

When all firing signals are one, all upper switches (s_1, s_2, and s_3) are closed while all lower switches (s_{1n}, s_{2n}, and s_{3n}) are open. In this state, the circuit behaves like in Figure 18.

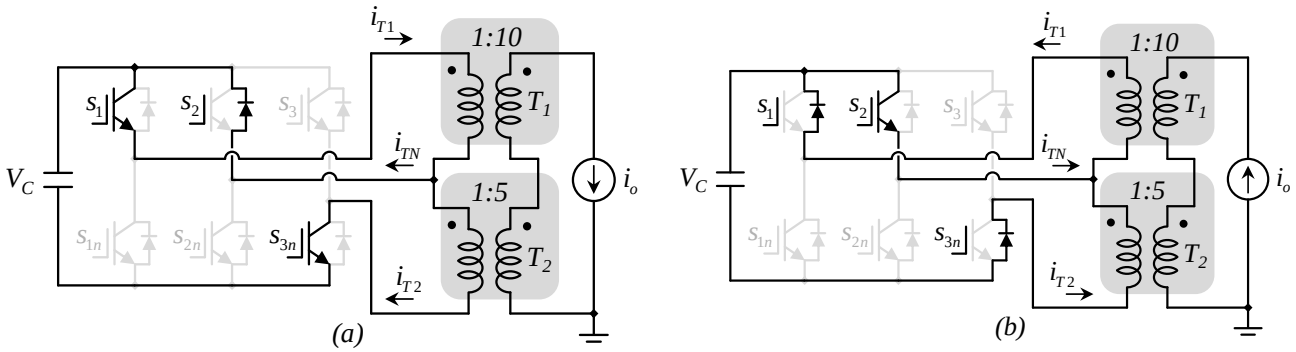


Figure 17. Current flow for different directions of the load current when $s_1 = 1$, $s_2 = 1$, and $s_3 = 0$. (**a**) when the load current is positive and (**b**) when the load current is negative.

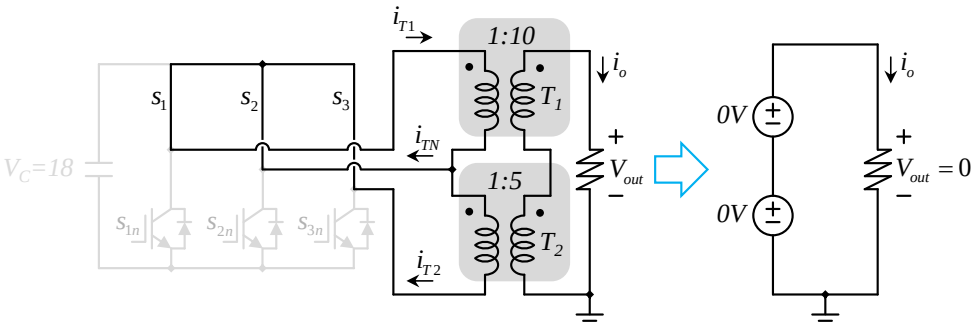


Figure 18. Equivalent circuit when $s_1 = 1$, $s_2 = 1$, and $s_3 = 1$ ($s_{1n} = 0$, $s_{2n} = 0$, and $s_{3n} = 0$).

Both transformers' primary windings are shorted and provide no voltage to the output side. In this state, the inverter provides an output of 0 V.

In this switching state, the current through transistors that are closed can be expressed in terms of the output current and the transformer's turn ratio as in (25)–(27):

$$i_{S1} = i_{T1} = 10 i_o. \tag{25}$$

$$i_{S3} = i_{T2} = 5 i_o. \tag{26}$$

$$i_{S2} = i_{TN} = i_{T1} - i_{T2} = 5 i_o. \tag{27}$$

As in previous states, the converter must be able to operate with different output current directions to consider an operation with a power factor different than one. The load can be modeled as a current source. In case the current is positive, the current paths on the converter would look like that in Figure 19a, otherwise it would look like that in Figure 19b. Depending on the load current direction, in some switches, the current flows through the transistor, and in other cases it flows through the diode.

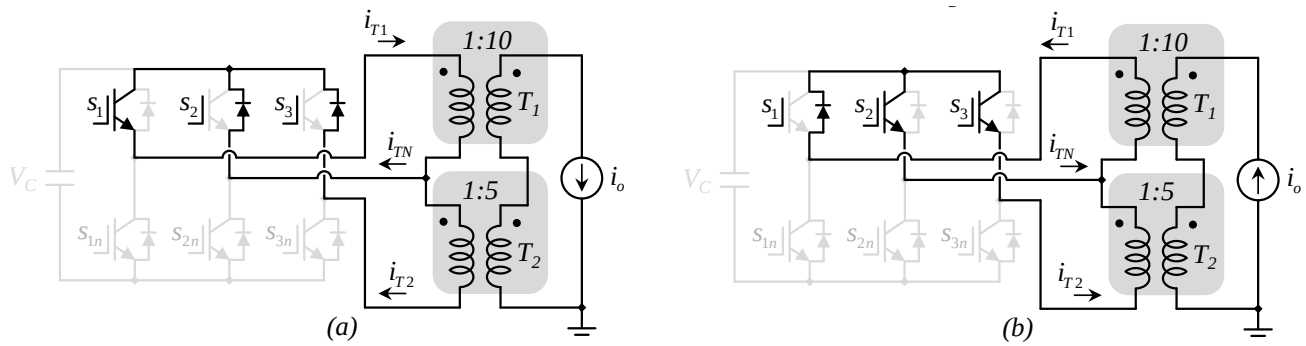


Figure 19. Current flow for different directions of the load current when $s_1 = 1$, $s_2 = 1$, and $s_3 = 1$. (**a**) when the load current is positive and (**b**) when the load current is negative.

2.9. Summary of the Converter's Equivalent Circuits

Table 1 shows a summary in which firing signals are shown with their respective output voltage.

Table 1. Firing signals and output voltage.

s_1	s_2	s_3	T_{1out}	T_{2out}	V_{out}
0	***0***	***0***	**zero**	**zero**	**0**
0	***0***	***1***	**zero**	**negative**	**−90**
0	*1*	*0*	negative	positive	−90
0	***1***	***1***	**negative**	**zero**	**−180**
1	***0***	***0***	**positive**	**zero**	**180**
1	*0*	*1*	positive	negative	90
1	***1***	***0***	**zero**	**positive**	**90**
1	*1*	*1*	zero	zero	0

Table 1 also includes the information about the contribution of transformers, whether it is positive, negative, or zero. The last column indicates the output voltage considering that the turn ratio of transformer T_1 is 1:10, the turn ratio of transformer T_2 is 1:5, and the input voltage (the capacitor's voltage) is 18 V.

We can see from the analysis that the converter has eight equivalent circuits, but only five different output voltage levels, since two pairs of states are redundant, which means they provide the same voltage. In this case, the states {0, 0, 1} and {0, 1, 0} both provide −90 V, and the states {1, 0, 1} and {1, 1, 0} both provide 90 V.

Evidently, the designer can choose some parameters, such as the turn ratio of transformers, and the input voltage may be different, but the converter can provide five different output voltage levels, which can produce a five-level stepped waveform.

The operation of the inverter requires the appropriate selection of switching functions. To operate the dc-ac inverter, we chose only the switching states marked in bold in Table 1.

Figure 20 shows important signals of the converter. From top to bottom, the first three signals are the selected switching functions and they are directly applied to the three upper switches (s_1, s_2, and s_3), while lower switches (s_{1n}, s_{2n}, and s_{3n}) have the opposite (complementary) logic signals.

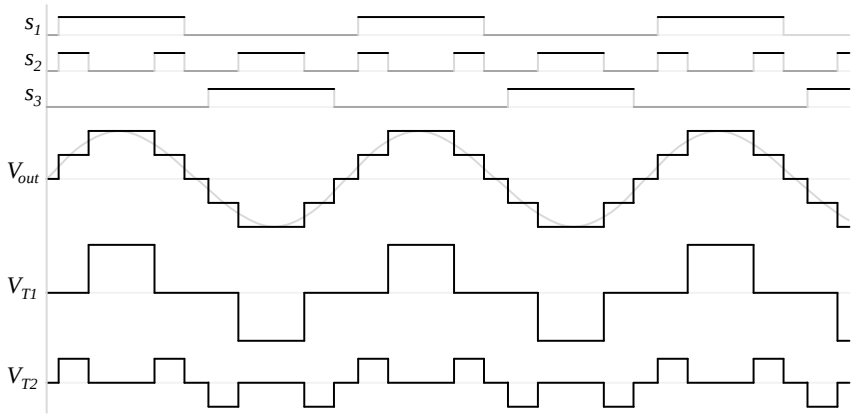


Figure 20. Important signals of the converter operation. From top to bottom: firing signals, output voltage, and voltage in transformers T_1 and T_2.

Figure 20 also shows the output voltage (V_{out}), the ideal sinusoidal waveform is shown in light gray, and the real stepped waveform is shown in black, and this is the multilevel waveform, with five levels. Finally, Figure 20 also shows the voltage at the secondary winding (output) of both transformers (T_1 and T_2). V_{T1} (180 V peak) has twice the peak amplitude of V_{T1} (90 V peak).

The output voltage can be expressed as the summation of the voltage at both transformers' secondary windings, as in (28):

$$V_{out} = V_{T1} + V_{T2}; \tag{28}$$

From the theoretical signals, we can also observe that four of the six transistors switch at the output frequency (i.e., 60 Hz), while two of them switch at three times the output frequency (i.e., 180 Hz); still, the switching frequency is relatively low for the capacity of a regular IGBT or a MOSFET.

The full-bridge power stage operates with a dead-time among the upper and lower transistors of the same phase, and this may cause a small distortion on the output current of a traditional PWM inverter, as described in [20]. In this case, since the switching frequency is low, the dead-time is negligible compared to the time in which transistors were on, and no effect was observed. However, if PWM is used, a dead-time elimination method (such as the one described in [20]) may be used to eliminate any current distortion.

2.10. Dynamical Model of the System

The elements that store energy in the system shown in Figure 3 are basically the inductor and capacitor of the boost converter, and despite that transformers have some stored energy in their magnetizing inductance, the amount of stored energy is relatively small. A simple mathematical model can be derived by analyzing the boost converter and then adding the input current of the six-pack module as the output current of the boost converter in the capacitor.

Figure 21 shows the boost converter with a current source as a load, and the load current i_x is the input current to the six-pack module, as shown in Figure 3.

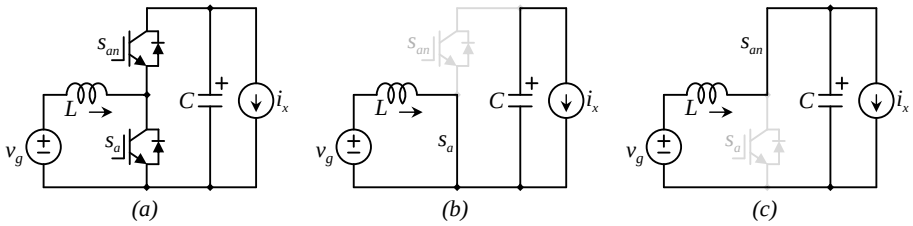


Figure 21. (**a**) The boost pre-regulators and their equivalent circuits according to the switching state, (**b**) when $s_a = 1$ ($s_{an} = 0$), and (**c**) when $s_a = 0$ ($s_{an} = 1$).

From the equivalent circuits, it is possible to use the standard averaging technique to describe the dynamics of the state variables. In this case, the state variables are the current through the inductor and the voltage across the capacitor [21]. The average voltage across the inductor and the average current through the capacitor would be expressed as in (29) and (30), respectively:

$$L\frac{di_L}{dt} = d(v_g) + (1-d)(v_g - v_C). \tag{29}$$

$$C\frac{dv_C}{dt} = d(-i_x) + (1-d)(i_L - i_x). \tag{30}$$

where d is the duty cycle of the switch s_a; in other words, the time in each switching cycle that the converter behaves like the circuit in Figure 21b, divided over the switching period.

Equations (29) and (30) can be simplified and rewritten as Equations (31) and (32):

$$L_1\frac{di_{L1}}{dt} = dv_g - (1-d)v_{C1}. \tag{31}$$

$$C_1\frac{dv_{C1}}{dt} = (1-d)i_{L1} - i_x. \tag{32}$$

From the dynamic Equations (31) and (32), the steady-state (or equilibrium) operation can be calculated. In a steady state, the derivative of state variables is zero, and then, making the derivatives in (31) and (32) equal to zero, the voltage in C_1 can be expressed as in (33) and the current through the inductor can be expressed as in (34):

$$V_C = \frac{1}{1-D} V_g. \tag{33}$$

$$I_{L2} = \frac{1}{(1-D)} I_x. \tag{34}$$

Upper case letters are used in (33) and (34) to indicate steady-state values or variables in the equilibrium condition.

3. Demonstrative Results

To corroborate the operation of the proposed converter, the converter was simulated in the software PSIM (2022-1) using a computer with an Intel i7 processor (11th Gen i7-1165G7 at 2.80 GHz), 32 GB of Ram memory, and Windows 11 Pro (64 bits). The simulation parameters are shown in Table 2.

Table 2. Simulation parameters.

Parameter	Value	Unit
Simulation time	1	s
Step	1	µs
Boost inductor	100	µH
Inductors ESR	50	mΩ
DC Link Capacitor	2	mF
Capacitors ESR	2	mΩ
Transistors Ron	100	mΩ
Diodes Forward voltage	0.9	V
Transf Magnetizing inductance	2	mH

Several tests were performed with and without magnetizing inductance (in parallel with the transformers' primary winding), and the difference was too small to be observed on the waveforms and only an increase of 0.05% on the THD was measured.

Figure 22 shows the simulation schematics, whereby the customizable power semiconductor element was used to simulate the transistors. All transistors have an antiparallel diode, which is a characteristic of the six-pack. The input voltage is 12 V, and the transformers' turn ratios are also the same as in the analysis (1:10 for T_1 and 1:5 for T_2).

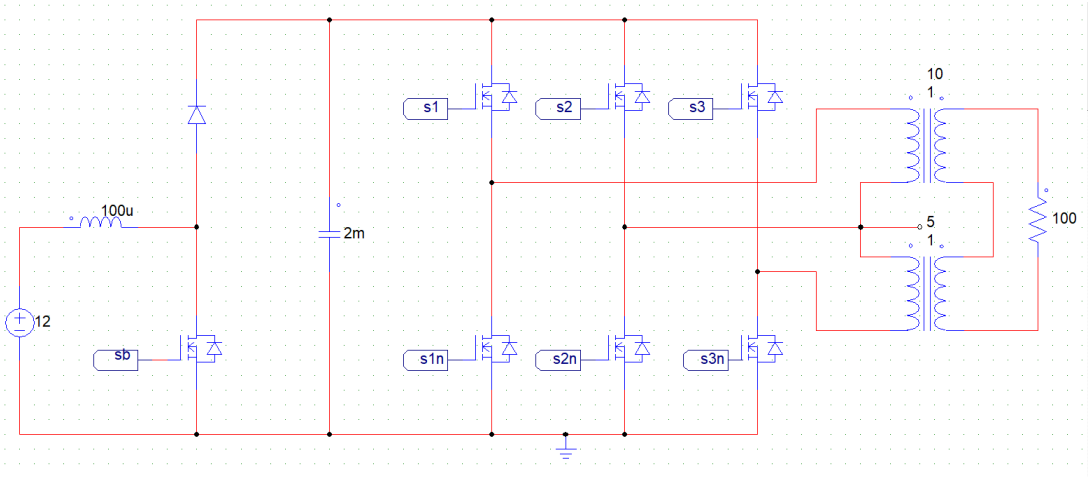


Figure 22. Schematic of the proposed inverter in the simulation program PSIM.

The simulator requires to have a reference (ground) in floating elements of the circuits, but in the application, the input side and the output side of transformers are naturally electrically isolated.

Figure 23 shows the switching signals (up) along with the output voltage, V_{out}. The voltage is consistent with what we expected, and with the waveform shown in Figure 20. The simulation shows that the proposed topology can make the voltage conversion from the dc input to the five-level output.

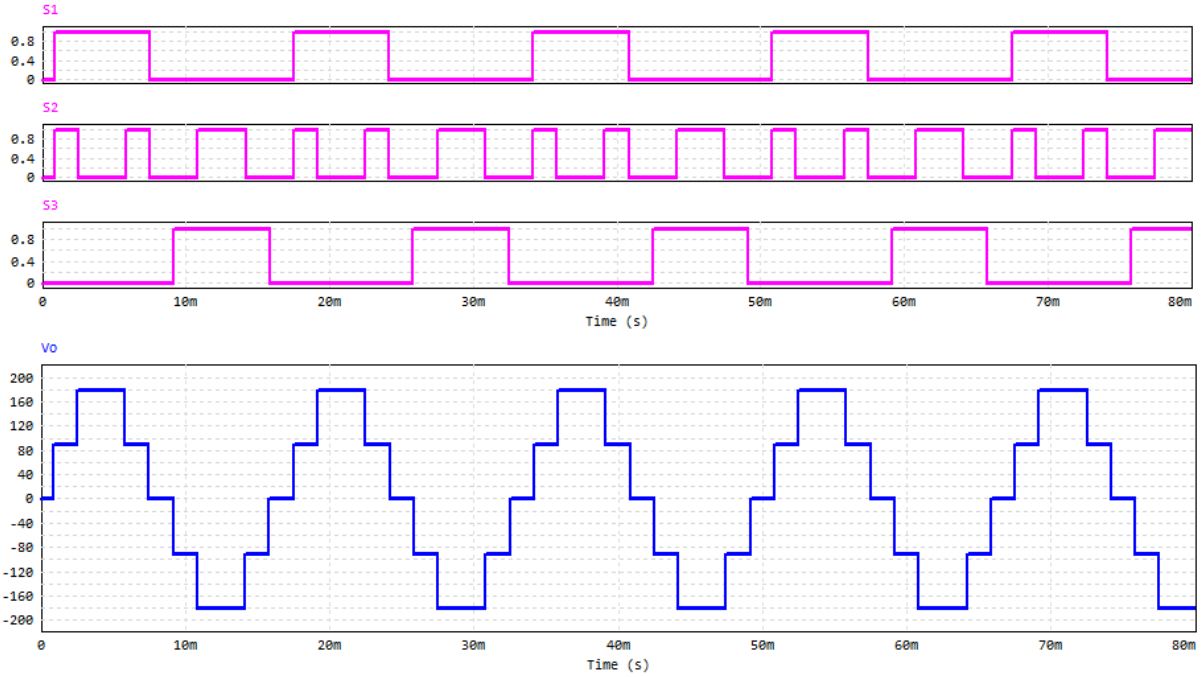


Figure 23. Switching signals and the output voltage.

The converter was used to generate a 60 Hz multilevel voltage output with a peak amplitude of 180 V (see Table 1). Figure 24 shows the voltage at transformers' secondary winding along with the output voltage, which is the sum of both transformers' output voltages. The measured total harmonic distortion (THD) of the staircase output voltage waveform generated by the converter was around 20%, although it can be improved by adding an output filter, increasing the number of levels, or implementing a PWM modulation.

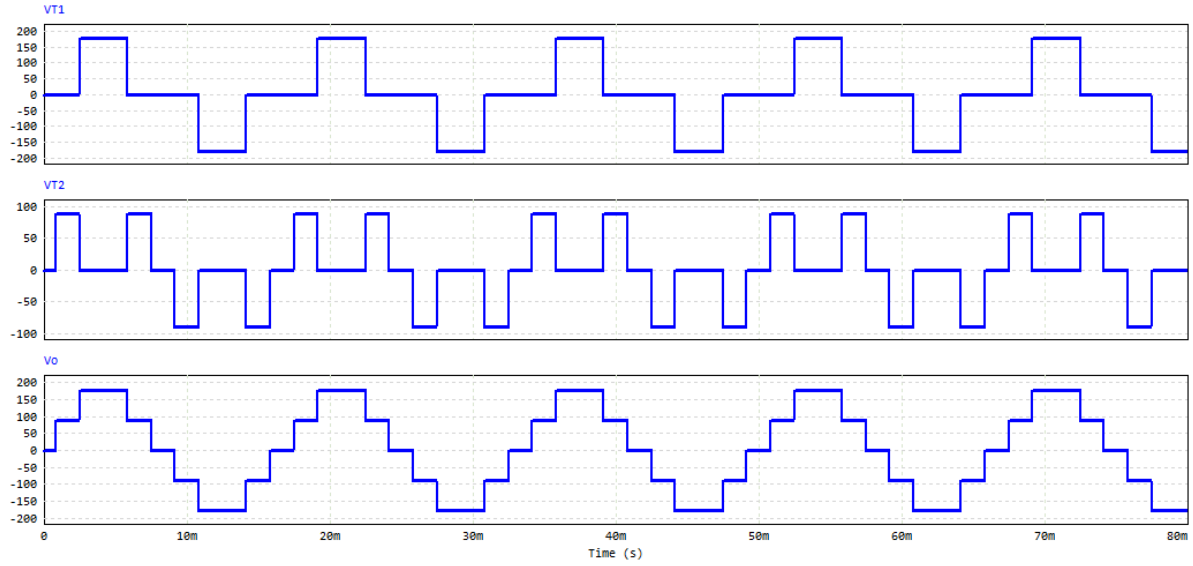
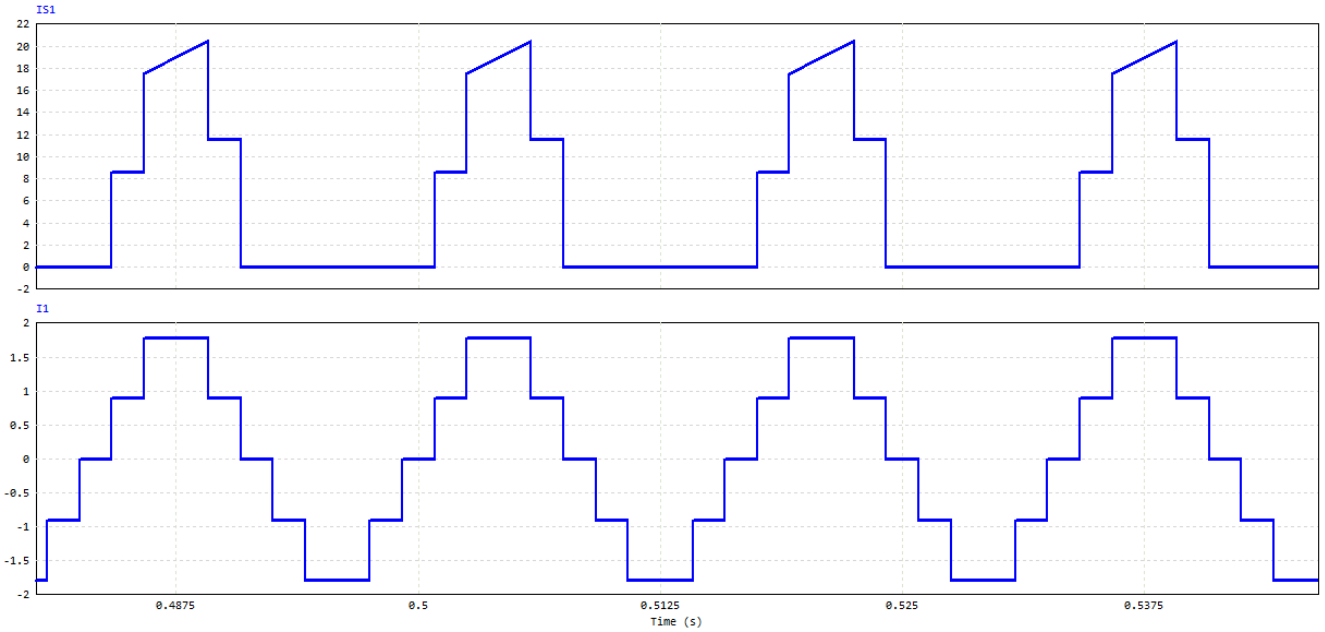
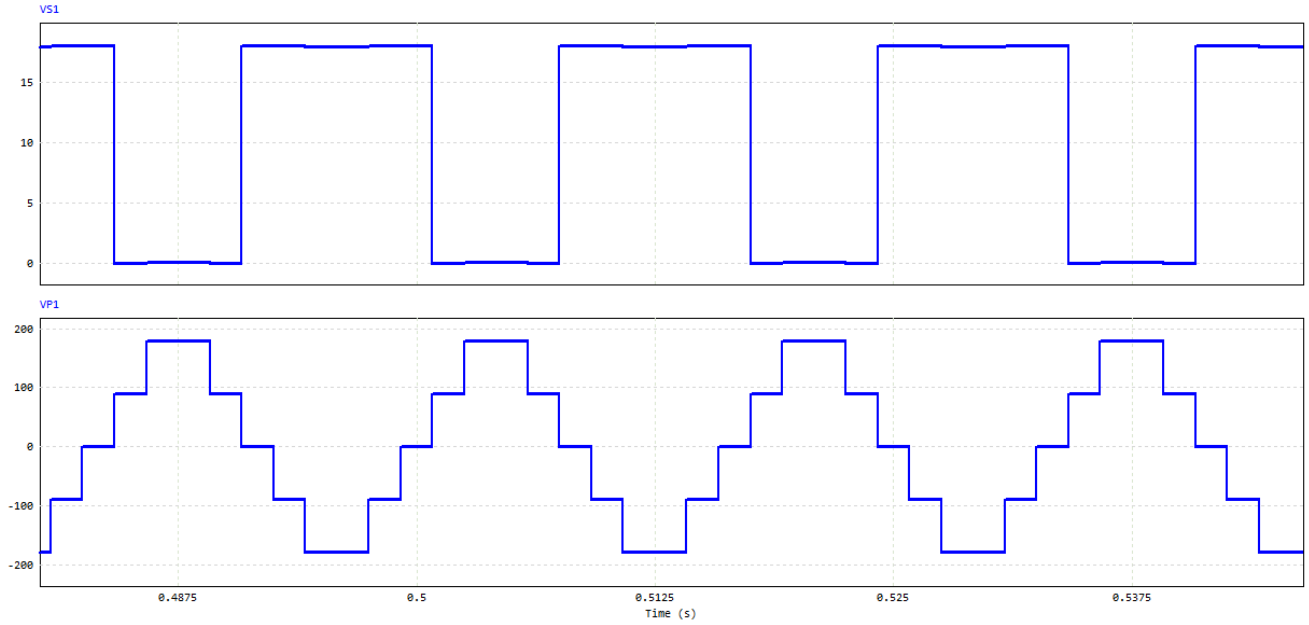


Figure 24. Voltages at transformers' output and the output voltage.

We have also included important waveforms for the semiconductors of the power converter, as can be observed in Figure 25, where the current through and voltage across the switch S_1 are compared to the current and voltage at the output, respectively.



(a)



(**b**)

Figure 25. Semiconductor's waveforms: (**a**) the current through switch S_1 compared to the output current, and (**b**) the voltage across switch S_1 compared to the output voltage.

It can be seen that the peak values of current and voltage in semiconductors correspond to the input current and voltage values. It is also important to notice that, as is expected in multilevel converters, the semiconductors only block a portion of the output voltage, which allows the selection of components with smaller voltage ratings.

The simulations were performed considering some parasitic components in the transformer, however the addition of non-idealities such as magnetizing and leakage inductance will not drastically affect the performance of the converter. For instance, these inductances could cause a small distortion in the levels of the converter that can be compensated by

increasing the dc bus capacitance. The simulation was performed in a specialized software which considers non-ideal models for semiconductors and other elements, and it showed that the converter can perform the proposed conversion and demonstrated that the inverter can be built with a six-pack IGBT module.

Operation of the Converter under Closed-Loop Control

Due to the nature of the output voltage waveform created by the proposed topology (staircase), which has the aforementioned advantages of low-frequency switching and low losses, the direct regulation of the output voltage is not permitted. However, the closed-loop operation of the converter is possible by including PWM modulation or by implementing a dc pre-regulator.

In this work, we chose to explore the option of the dc pre-regulator stage to demonstrate the regulation capability. It is worth noting that in most applications, this pre-regulator is required, for instance in PV grid-tied inverters and motor drivers.

The designed control scheme consists of a traditional PI controller which regulates the RMS value of the output voltage, by controlling the operation of the dc pre-regulator, as can be seen in Figure 26. The controller was tuned considering that the dc bus bulk capacitor presents slow dynamics. There exist multiple options for designing the control stage, however here we only show an alternative to demonstrate the application of the proposed topology if the closed-loop operation is required.

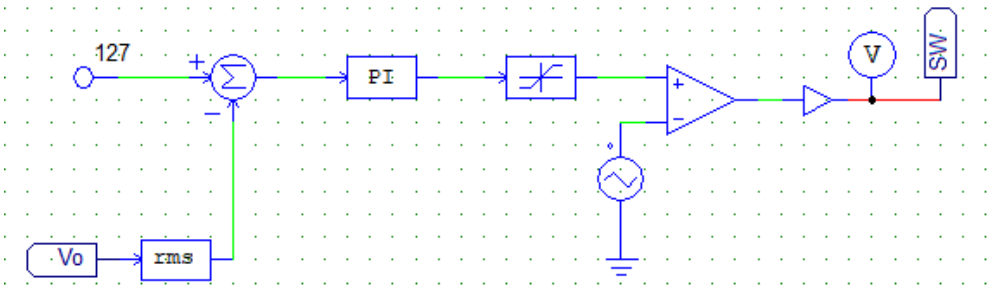


Figure 26. Controller diagram.

The RMS value in Figure 26 was calculated with the moving average or window strategy to ensure a precise measurement.

We performed two different tests to corroborate the performance of the converter under closed-loop operation. The first test was for changes at the input source. We changed the input voltage from the nominal 12 to 15 V and back, and from 12 to 9 V and vice versa, and the setpoint for the output voltage was fixed to 127 V_{RMS}. As can be seen in Figure 27, the output reaches its steady-state value after some milliseconds of the input voltage change. It can be seen that the output voltage is stably bounded and correctly regulated in spite of the abrupt input voltage changes.

The second test consisted in changing the output voltage setpoint reference of the converter while keeping the input voltage constant. The reference was changed from 127 to 160 V_{RMS} and back, and from 127 to 100 V_{RMS} and vice versa. The results of this test can be seen in Figure 28. As can be observed, the output voltage followed the reference after a short transient of a few milliseconds, and it is worth mentioning that although the changes in the reference were suddenly made, the converter followed the control commands properly.

To verify the stability margins of the closed-loop controller, we included the bode plots for the closed-loop system. The bode diagrams were obtained directly from the simulation by perturbing the reference signal with a frequency-varying sinusoidal waveform of around 10% of the nominal value of the reference. In Figure 29, we included the bode plots of two tests to characterize the effect of the output transformer in the closed-loop operation of the system. It can be seen from the plots that the closed-loop system presents a sufficient phase margin of around 70° which, alongside with the gain margin of around 20 dB,

guarantees a stable operation of the converter. It can be noticed that the addition of the output transformer slightly decreases the crossover frequency (bandwidth) of the closed-loop system but does not have a substantial impact on the stability of the converter.

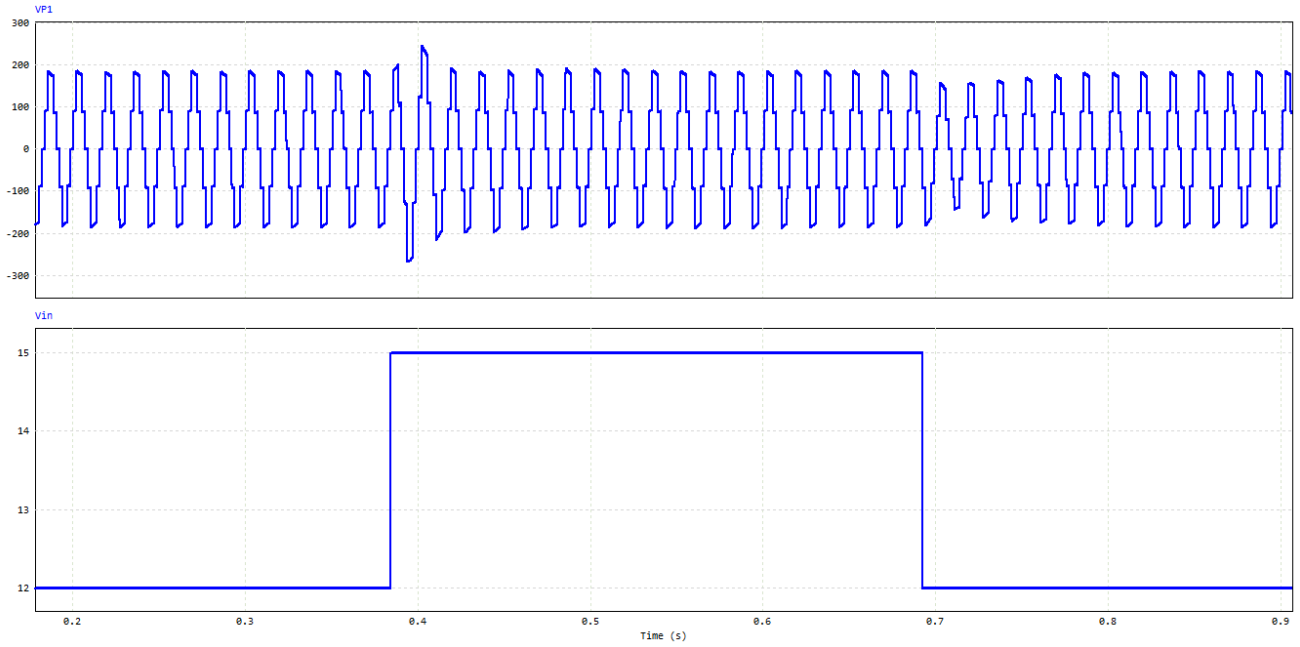


Figure 27. Operation of the converter under closed-loop control. Output voltage waveform when the input voltage source is changed from 12 to 15 V.

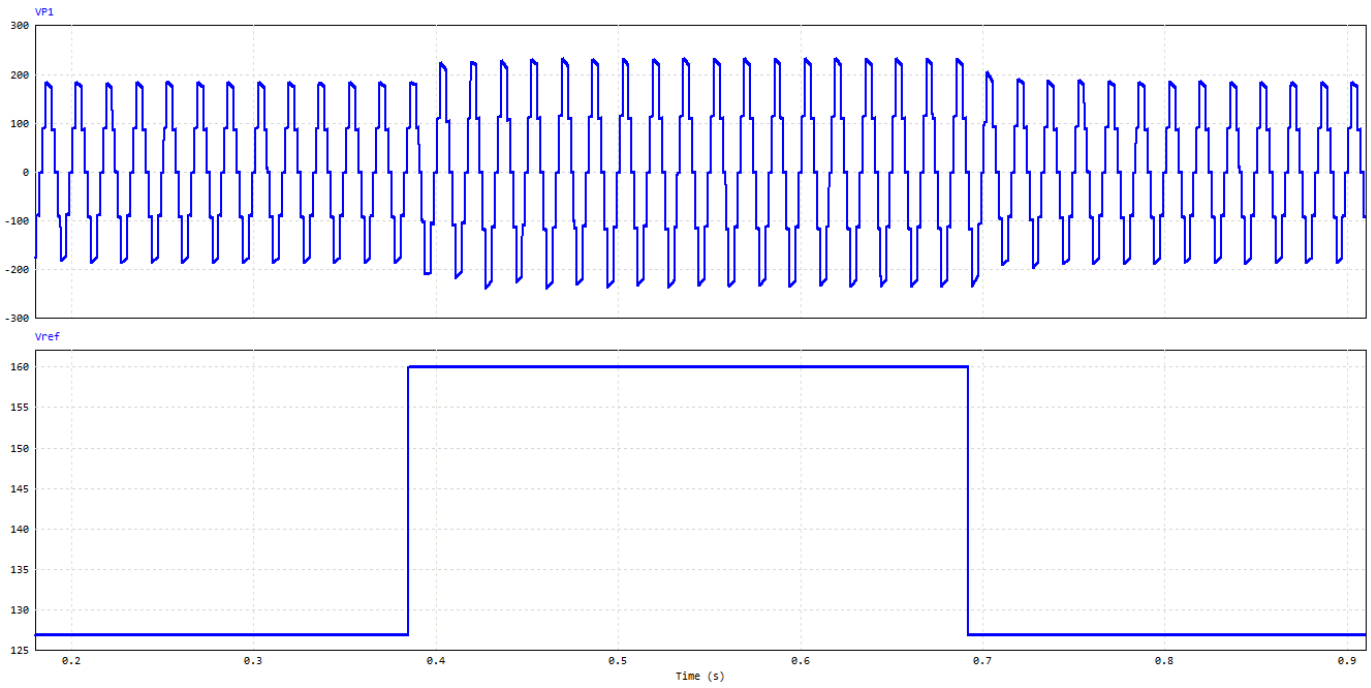


Figure 28. Operation of the converter under closed-loop control. Output voltage waveform when the control reference is changed from 127 to 160 V_{RMS}.

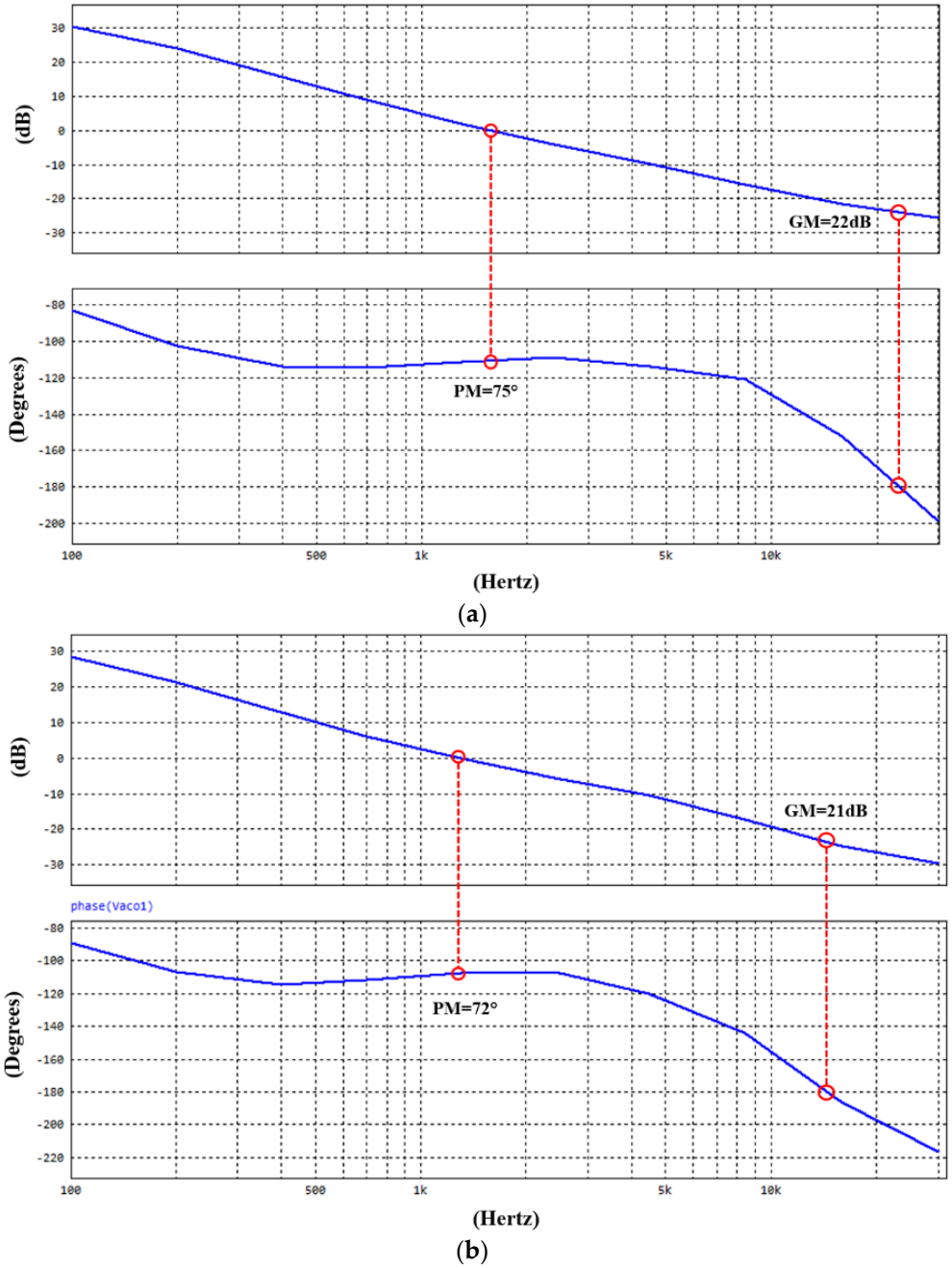


Figure 29. Bode plots of the power electronics system under closed-loop regulation. (**a**) Closed-loop bode without the output transformer, and (**b**) closed-loop bode with the output transformer.

4. Discussion

The proposed topology can be built with a six-pack transistors module, which is an advantage from the manufacturing point of view. Six-pack transistors modules are widely used in many applications, and they are available in a wide range of voltages, currents, power dissipation, and with several types of devices, such as MOSFETs, IGBTs, etc. They are off-the-shelf devices.

Four of the six transistors switched at the output frequency (60 Hz), while the other two switched at three times the switching frequency (180 Hz). However, three times the switching frequency is still considered a low frequency for IGBTs and MOSFETS.

The main disadvantage of the proposed topology is that it requires two transformers, but their turn ratios can be used as an extra degree of freedom during the design, to

customize the voltage gain according to the application. Furthermore, if one transformer is chosen with a 1:1 turn ratio, and no isolation is required, the transformers can be omitted while the converter performs the same application.

Compared to other topologies, the proposed one has a low-voltage stress on transistors; on the other hand, the current may be relatively large since it is proportional to the output current multiplied by the turn ratios of transformers. This makes the converter more suitable to be used for MOSFETs, whereby the on-resistance may help to reduce the conduction losses compared to other topologies.

5. Conclusions

This article introduced a single-phase five-level multilevel inverter topology which is based on a three-phase arrangement of transistors (what we usually call a six-pack module) and two transformers. The proposed converter requires a single dc input source, and the input source may have low amplitude since the turn ratio of transformers can be used to boost the voltage. Six-pack transistors modules are commercially available (off-the-shelves), and since those packages are widely used to build low-power three-phase inverters, their use simplifies the manufacturing process. The converter has low-voltage stress on transistors. Their main drawback is the use of two transformers, but those transformers allow using the same topology for several input voltage levels by changing the transformers' turn ratios. To verify the operation of the proposed multilevel inverter, a computer-based simulation was performed with the specialized software PSIM, a software that considers parasitic components (non-ideal). The results show that the proposed converter can work properly and perform the power conversion as expected.

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References

1. Kouro, S.; Malinowski, M.; Gopakumar, K.; Pou, J.; Franquelo, L.G.; Wu, B.; Rodriguez, J.; Perez, M.A.; Leon, J.I. Recent advances and industrial applications of multilevel converters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2553–2580. [CrossRef]
2. Rodriguez, J.; Lai, J.S.; Peng, F.Z. Multilevel inverters: A survey of topologies, control and applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 724–738. [CrossRef]
3. Bughneda, A.; Salem, M.; Richelli, A.; Ishak, D.; Alatai, S. Review of Multilevel Inverters for PV Energy System Applications. *Energies* **2021**, *14*, 1585. [CrossRef]
4. Alotaibi, S.; Darwish, A. Modular Multilevel Converters for Large-Scale Grid-Connected Photovoltaic Systems: A Review. *Energies* **2021**, *14*, 6213. [CrossRef]
5. Choudhury, S.; Bajaj, M.; Dash, T.; Kamel, S.; Jurado, F. Multilevel Inverter: A Survey on Classical and Advanced Topologies, Control Schemes, Applications to Power System and Future Prospects. *Energies* **2021**, *14*, 5773. [CrossRef]
6. Zhang, F.; Peng, F.Z.; Qian, Z. Study of the multilevel converters in DC-DC applications. In Proceedings of the 2004 IEEE 35th Annual Power Electronics Specialists Conference, Aachen, Germany, 20–25 June 2004; Volume 2, pp. 1702–1706.
7. Peng, F.Z. A generalized multilevel inverter topology with self voltage balancing. *IEEE Trans. Ind. Appl.* **2001**, *37*, 611–618. [CrossRef]
8. Lai, J.-S.; Peng, F.Z. Multilevel converters-a new breed of power converters. *IEEE Trans. Ind. Appl.* **1996**, *32*, 509–517.
9. Nabae, A.; Takahashi, I.; Akagi, H. A new neutral-point-clamped PWM inverter. *IEEE Trans. Ind. Appl.* **1981**, *IA-17*, 518–523. [CrossRef]

10. Chen, G.; Yang, J. A Modified Modulation Strategy for an Active Neutral-Point-Clamped Five-Level Converter in a 1500 V PV System. *Electronics* **2022**, *11*, 2289. [CrossRef]
11. Li, W.-J.; Li, D.-S.; Zhang, J.-W. Model-Based Design and Experimental Validation of Control System for a Three-Level Inverter. *Electronics* **2022**, *11*, 1979. [CrossRef]
12. Meynard, T.A.; Foch, H. Multi-Level Choppers for High Voltage Applications. *EPE J.* **1992**, *2*, 45–50. [CrossRef]
13. Hochgraf, C.; Lasseter, R.; Divan, D.; Lipo, T.A. Comparison of multilevel inverters for static var compensation. In Proceedings of the 1994 IEEE Industry Applications Society Annual Meeting, Denver, CO, USA, 2–6 October 1994; pp. 921–928.
14. Marquardt, R. Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications. In Proceedings of the 2010 International Power Electronics Conference, Sapporo, Japan, 21–24 June 2010; pp. 502–507.
15. Marquardt, R. Modular multilevel converter topologies with dc-short circuit current limitation. In Proceedings of the 8th International Conference on Power Electronics, Jeju, Republic of Korea, 30 May–3 June 2011; pp. 1425–1431.
16. Marquardt, R. Modular Multilevel Converters: State of the Art and Future Progress. *IEEE Power Electron. Mag.* **2018**, *5*, 24–31. [CrossRef]
17. Tolbert, L.M.; Peng, F.Z. Multilevel converters as a utility interface for renewable energy systems Power Engineering Society Summer Meeting. In Proceedings of the 2000 Power Engineering Society Summer Meeting, Seattle, WA, USA, 16–20 July 2000; pp. 1271–1274.
18. Ozpineci, B.; Tolbert, L.M.; Su, G.-J.; Du, Z. Optimum fuel cell utilization with multilevel DC-DC converters. In Proceedings of the Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 22–26 February 2004; Volume 3, pp. 1572–1576.
19. Walker, G.R.; Sernia, P.C. Cascaded DC-DC converter connection of photovoltaic modules. *IEEE Trans. Power Electron.* **2004**, *19*, 1130–1139. [CrossRef]
20. Chen, L.; Peng, F.Z. Dead-Time Elimination for Voltage Source Inverters. In *Communication Systems and Information Technology*; Springer: Berlin/Heidelberg, Germany, 2008; Volume 23, pp. 574–580.
21. Erickson, R.W.; Maksimovic, D. *Fundamentals of Power Electronics*; Springer: New York, NY, USA, 2001.