

PAPER • OPEN ACCESS

Design and preliminary results of a shunt voltage regulator for a HV-CMOS sensor in a 150 nm process

To cite this article: S. Powell *et al* 2023 *JINST* **18** C01009

View the [article online](#) for updates and enhancements.

ECS Toyota Young Investigator Fellowship



For young professionals and scholars pursuing research in batteries, fuel cells and hydrogen, and future sustainable technologies.

At least one \$50,000 fellowship is available annually.
More than \$1.4 million awarded since 2015!



Application deadline: January 31, 2023

Learn more. Apply today!

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS
BERGEN, NORWAY
19–23 SEPTEMBER 2022

Design and preliminary results of a shunt voltage regulator for a HV-CMOS sensor in a 150 nm process

S. Powell,* J. Hammerich, N. Karim,¹ E. Vilella and C. Zhang

The University of Liverpool, The Oliver Lodge Laboratory, Liverpool L69 7ZE, U.K.

E-mail: spowell@liv.ac.uk

ABSTRACT: This paper presents the design and preliminary results of a shunt voltage regulator and two different bandgap reference designs for use with a monolithic High Voltage CMOS (HV-CMOS) sensor in a 150 nm technology node. One bandgap reference design is based on Bipolar Junction Transistors (BJTs) as the reference element of the circuit — the rest of the circuit is entirely designed with Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs). The second bandgap reference design makes use of MOSFETs exclusively.

KEYWORDS: Particle tracking detectors; Radiation-hard detectors; Solid state detectors

*Corresponding author.

¹Now at Leonardo UK LTD, First Avenue, Southampton, SO15 0LG, U.K.

Contents

1	Introduction	1
2	Design	2
2.1	Bipolar Junction Transistor (BJT) bandgap reference design	2
2.2	MOSFET bandgap reference design	2
2.3	Shunt regulator design	3
3	Experimental setup	4
4	Evaluation and measurements	4
4.1	Bipolar Junction Transistor (BJT) bandgap reference design	4
4.2	MOSFET bandgap reference design	4
4.3	Shunt regulator design	5
5	Conclusions	6

1 Introduction

High-Voltage CMOS (HV-CMOS) sensors are one of the main candidate technologies for future tracking detectors in high luminosity colliders. In spite of their many advantages including material budget, pixel granularity and radiation tolerance, these sensors need further research to boost their performance parameters to meet the challenging requirements of future experiments [1]. UKRI-MPW0 is a proof-of-concept HV-CMOS pixel chip aimed at pushing the performance boundaries of these sensors manufactured in the LFoundry 150 nm process. The layout view of UKRI-MPW0 is shown in figure 1.

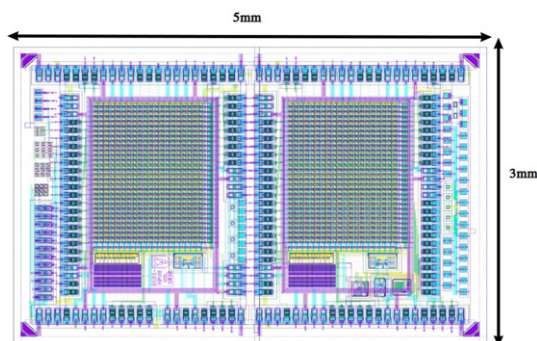


Figure 1. Layout view of UKRI-MPW0.

This chip implements a novel sensor cross-section optimised for backside biasing to unprecedented high voltages to improve radiation tolerance. High breakdown voltages beyond 600 V have been measured before and after irradiation. UKRI-MPW0 contains two active pixel matrices, one with linear transistors and another one with enclosed layout transistors, aimed at testing the novel sensor cross-section [2]. The chip implements, as well, a shunt voltage regulator to generate the various power supply levels locally on-chip to reduce external circuitry and improve the noise performance. The active matrix has been characterised using the Caribou DAQ system [3].

2 Design

2.1 Bipolar Junction Transistor (BJT) bandgap reference design

The schematic of the BJT based bandgap reference design is shown in figure 2 (left).

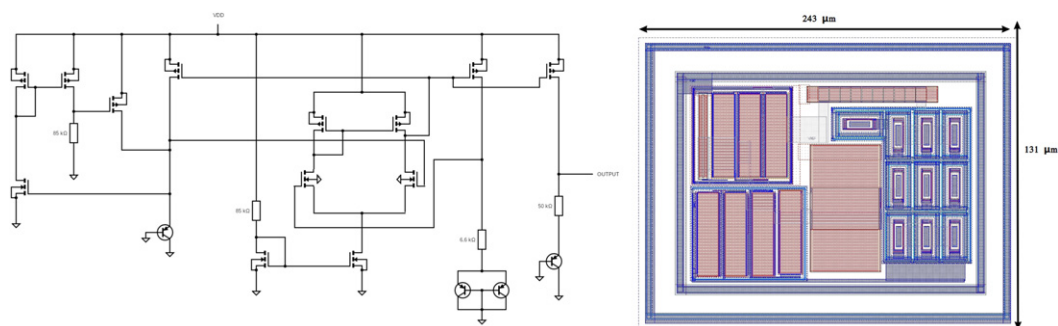


Figure 2. BJT bandgap reference schematic and layout view.

The circuit consists of a differential amplifier, startup circuit, diode connected PNP BJT transistors and two poly-silicon resistors. The circuit presented provides first order temperature correction. The corresponding layout of the BJT based bandgap reference design is shown in figure 2.

A common centroid topology is employed to improve matching between the BJTs. The BJT bandgap reference makes use of Proportional To Absolute Temperature (PTAT), derived from the emitter-base voltage differential of two BJTs, and Complementary To Absolute Temperature (CTAT) design components (derived from the emitter-emitter-base voltage of a BJT [4]), which cancel each other out and provide an output that is independent of temperature. The BJT bandgap provides a reference voltage of 1.2 V (close to the 1.12 eV bandgap of silicon [5]). The supply voltage (VDD) for this technology is 1.8 V, a reference voltage of 1.2 V leaves a comfortable margin. Monte-Carlo simulations show a mean value of 1.191 V and a sigma value of 7.32 mV.

2.2 MOSFET bandgap reference design

A fully MOSFET based bandgap was designed and manufactured due to the fact that MOSFETs in the LFoundry 150 nm process have been extensively characterised for their radiation tolerance [6],

the same is not true of BJT transistors in this technology. The schematic (left) and layout view (right) of the MOSFET based bandgap reference design are shown in figure 3. The MOSFET bandgap reference consists of a startup circuit, differential amplifier, three diode connected NMOS transistors and two poly-silicon resistors. The circuit presented provides first order temperature correction. Simulations show the fully CMOS bandgap provides a reference voltage of 350 mV, with a maximum voltage variation of 2 mV across an input range of 0.8 to 1.8 V and a maximum voltage variation of 8.4 mV between $-40\text{ }^{\circ}\text{C}$ and $120\text{ }^{\circ}\text{C}$. Monte-Carlo simulations show a mean value of 349.6 mV and a sigma value of 9.74 mV.

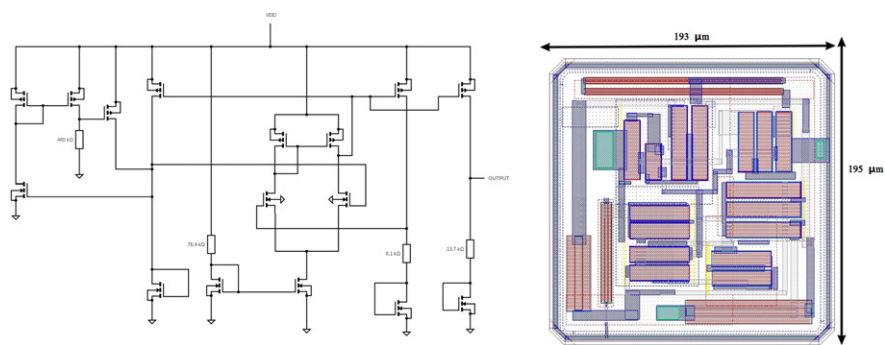


Figure 3. MOSFET bandgap reference schematic and layout view.

2.3 Shunt regulator design

The shunt regulator topology offers an advantage over the traditional series voltage regulator in that not all of the output current is required to flow through the regulator itself. This allows for a smaller transistor and a reduced heat load on the circuit. It also provides the possibility of performing serial powering [7]. The schematic (left) and layout view (right) of the shunt regulator circuit are shown in figure 4.

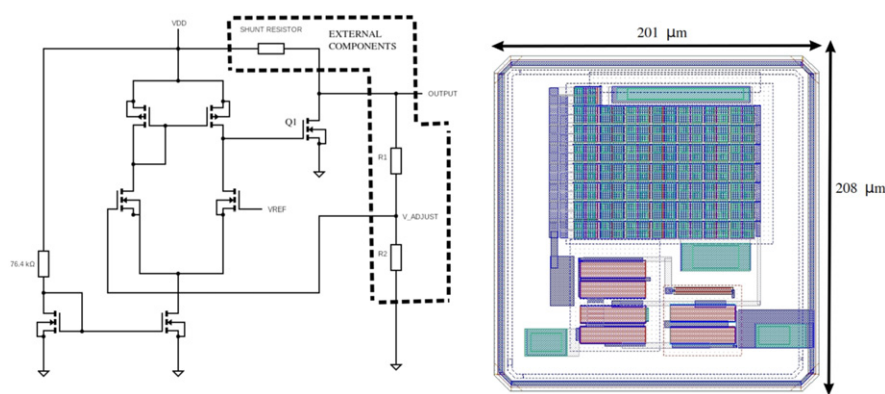


Figure 4. Shunt regulator schematic and layout view.

Three external resistors allow the shunt regulator output voltage and maximum current to be adjusted for different applications. A reference voltage input (VREF) allows either the MOSFET or BJT bandgap reference to be used to provide the reference level. The feedback network formed by R1 and R2, as shown in figure 4, maintains a constant output voltage by adjusting the current through the shunt transistor Q1. An increased current through Q1 causes an increased current through the shunt resistor reducing the output voltage (and vice versa) as necessary to keep the output voltage stable.

3 Experimental setup

The variation in output voltage as a function of input voltage, and output voltage as a function of output current, were measured using a custom Python script to control a Keithley 2410 SMU via Standard Commands for Programmable Instruments (SCPI) commands. The variation in output voltage as a function of temperature was measured using a custom Proportional Integral Derivative feedback (PID) [8] controlled temperature chamber consisting of a heater and Peltier element controlled by an Arduino based custom PCB via a custom Python script. The custom PID controlled temperature chamber is shown in figure 5.

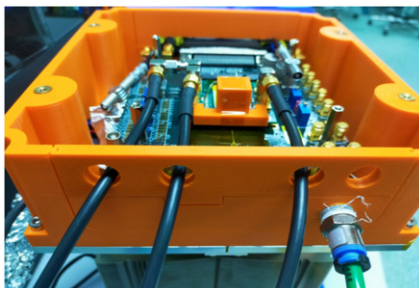


Figure 5. Custom PID controlled temperature chamber.

4 Evaluation and measurements

4.1 Bipolar Junction Transistor (BJT) bandgap reference design

Simulations show a maximum voltage variation of 7 mV across an input range of 1.4 to 1.8 V and a maximum voltage variation of 5 mV between $-40\text{ }^{\circ}\text{C}$ and $120\text{ }^{\circ}\text{C}$. The BJT based bandgap reference has been characterised for variations in both input voltage and temperature. The results are compared with simulation in figure 6.

It can be seen that there is a very close agreement between simulation and measurement for both variations in input voltage and temperature. A maximum difference of 3.3 mV was observed between simulation and measurements for variation in input voltage. For variations in temperature a maximum difference of 1.2 mV was observed between simulation and measurements.

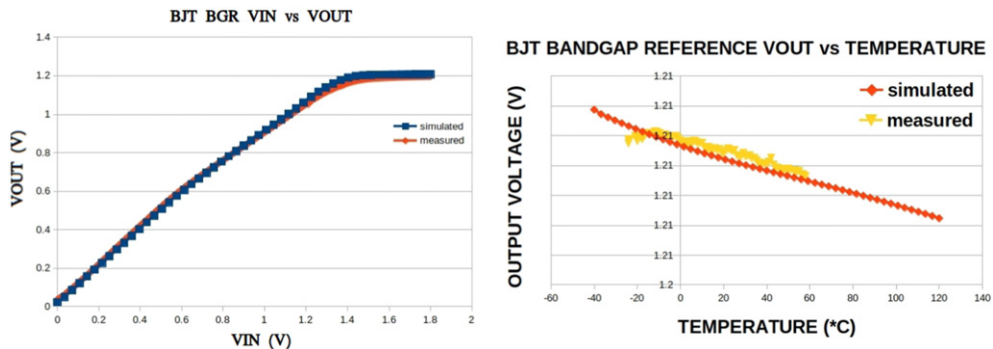


Figure 6. Simulation and measurement results compared for variations in input voltage (left) and temperature (right).

4.2 MOSFET bandgap reference design

A comparison of the results of simulation and measurements of the MOSFET bandgap reference is presented in figure 7. It can be seen that there is a close agreement between simulation and the measured results for both variations in input voltage (a maximum difference of 13.2 mV was observed) and temperature (a maximum difference of 2.4 mV was observed).

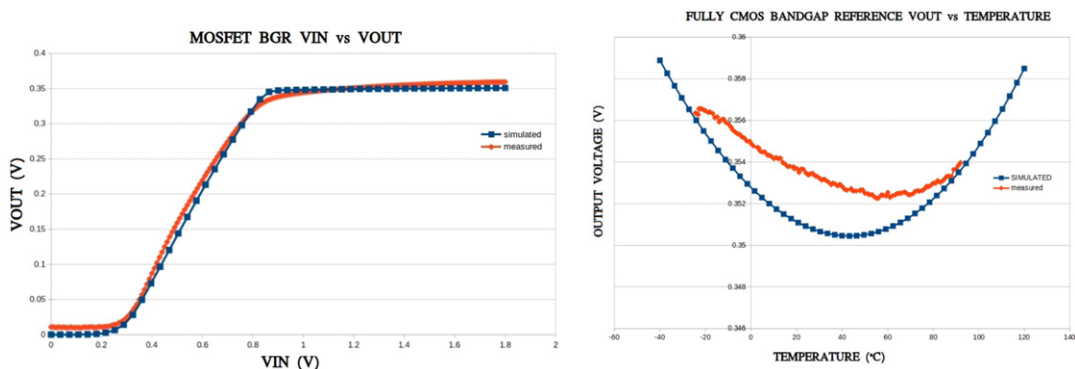


Figure 7. Simulation and measurement results compared for variations in input voltage (left) and temperature (right).

The difference in performance between simulation and measurement for temperature variation — figure 7 (right), may be due to an offset between the measured temperature and the actual chip die temperature. This is due to the physical constraints for the placement of the 3 temperature sensors with respect to the UKRI-MPW0 chip. The 3 temperature sensor readings are averaged to measure the chip temperature.

4.3 Shunt regulator design

The results of simulation and measurements of the shunt regulator are presented in figure 8.

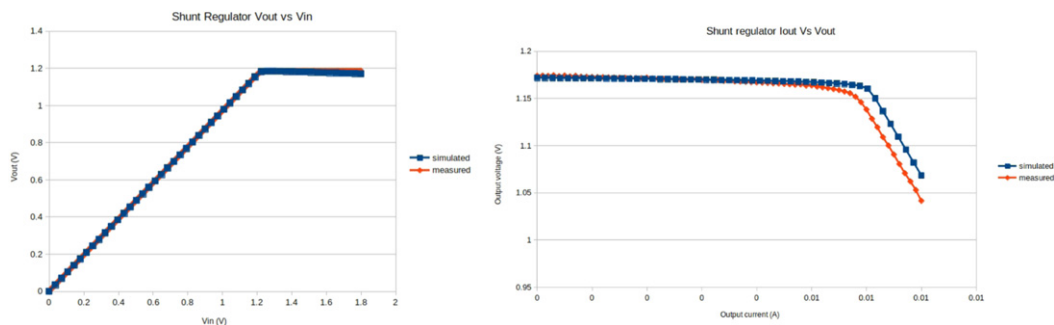


Figure 8. Simulation and measurement results compared for variations in input voltage (left) and output current (right).

It can be seen that there is a close agreement between simulation and measurement for both variations in input voltage (a maximum difference of 4.2 mV was observed between simulation and measurements) and output current (a maximum difference between simulation and measurement of 2.3 mV @ 10 mA output current).

Table 1 shows the specifications of the 3 circuits presented.

Table 1. Summary of specifications.

Parameter	BJT bandgap	MOSFET bandgap	Shunt regulator
Power consumption (μW)	478.8	478.8	Dependant on output current
Input voltage range (V)	1.4–1.8	0.8–1.8	0.8–1.8
Output voltage (V)	1.2	0.35	Adjustable
ΔV_{out} for input voltage range (mV)	7	2	Dependant on output
ΔV_{out} for temperature range (mV)	5	8.4	Dependant on output
Temperature range ($^{\circ}\text{C}$)	–40 to +120	–40 to +120	–40 to +120
Area ($\mu\text{m} \times \mu\text{m}$)	243×131	193×195	201×208

5 Conclusions

The BJT bandgap provides a reference voltage of 1.2 V, with a maximum voltage variation of 7 mV across an input range of 1.4 to 1.8 V and a maximum voltage variation of 5 mV between -40°C and 120°C . The fully CMOS bandgap provides a reference voltage of 350 mV, with a maximum voltage variation of 2 mV across an input range of 0.8 to 1.8 V and a maximum voltage variation of 8.4 mV between -40°C and 120°C . The combined power consumption of the BGRs is $478.8 \mu\text{W}$. The power consumption of the shunt regulator is dependant on the output voltage chosen, and the value chosen for the external shunt resistor.

Acknowledgments

This work has received funding from UK Research and Innovation (UKRI) under the Grant reference MR/S016449/1.

References

- [1] A. Miucci et al., *Radiation-hard active pixel sensors for HL-LHC detector upgrades based on HV-CMOS Technology*, 2014 *JINST* **9** C05064.
- [2] C. Zhang, M. Franks, J. Hammerich, N. Karim, S. Powell and E. Vilella, *Design and evaluation of UKRI-MPW0: an HV-CMOS prototype for high radiation tolerance*, *Nucl. Instrum. Meth. A* **1040** (2022) 167214.
- [3] T. Vanat, *Caribou — a versatile data acquisition system*, *PoS TWEPP2019* (2019) 100.
- [4] R. Widlar, *New developments in IC voltage regulators*, *IEEE J. Solid-State Circuits* **6** (1971) 2.
- [5] J. Low, M. Kreider, D. Pulsifer, A. Jones and T. Gilani, *Band gap energy in silicon*, *Am. J. Undergrad. Res.* **7** (2008) 6.
- [6] T. Hirono et al., *Depleted fully monolithic active CMOS pixel sensors (DMAPS) in high resistivity 150 nm technology for LHC*, *Nucl. Instrum. Meth. A* **924** (2019) 87 11th International Hiroshima Symposium on Development and Application of Semiconductor Tracking Detectors.
- [7] J. Matheson, *Serial power distribution for the atlas tracker upgrade*, *PoS RD09* (2009) 40.
- [8] K. Ang, G. Chong and Y. Li, *PID control system analysis, design, and technology*, *IEEE Trans. Control Syst. Technol.* **13** (2005) 559.