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High Speed Low Area DA Based FIR Filter Using EGDI Adder

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Abstract: In this paper we proposed a novel enhanced gate diffusion (EGDI) adder is designed and is implemented in Distributed Arithmetic (DA) based Finite Impulse Response (FIR) filter. Generally multipliers, adders and shift accumulators are the basic blocks present in the FIR filters. The hardware architecture of multipliers is very high. To get rid of this, multiplier less architecture are needed in FIR filter. So Distributed Arithmetic architecture place a key role in FIR filters which will occupy less area and increase the speed. To reduce the area further the adders in DA are designed using enhanced gate diffusion (EGDI) which increases the operation speed of FIR filter and at same time the area will be decreased. The proposed design is synthesized and implemented in Synapsis design compiler tool. The area, power delay product, frequency, area delay product and power of the proposed design are calculated. When we observe the synthesis results, the proposed design has 15% high frequency rate when compare with the existing design. Also the proposed design is more useful in signal processing applications like decision feed-back equalizer.

Keywords: Enhanced gate diffusion, finite impulse response, adders, and digital filters

1. Introduction

Inner product plays a surmount role in applications like multimedia, digital signal processing, hearing aids, ECG signals, wireless communication etc where in these multiplication operation will perform a major role. The operation of multiplier will consume more execution time for calculating addition, division, and some other performances. The area occupied by the multipliers is very high. Multiplier operation will determine the efficiency of any DSP systems. Digital filters are the essential block present in the DSP systems. To overcome these entire drawback, multiplier less architectures should be designed, which utilizes less area and less power. Several digital filters are designed to reduce the area, speed and power consumption. The Distributed Arithmetic (DA) architecture is a multiplier-free design that has a number of advantages over previous multiplier-based architectures. DA consists of the serial in parallel out shift register unit, memory unit and shift adder block. There are many techniques present in DA architecture. The two most common DA architectures are memory-based DA & memory-less DA. Memory-less DA architecture is more practical than memory-based DA architecture. Fig.1 gives us basic architecture of DA.

Nomenclature is included if necessary
DA Distributed Arithmetic
DSP Digital Signal Processing
GDI Gate diffusion input
EGDI Enhanced Gate Diffusion Input

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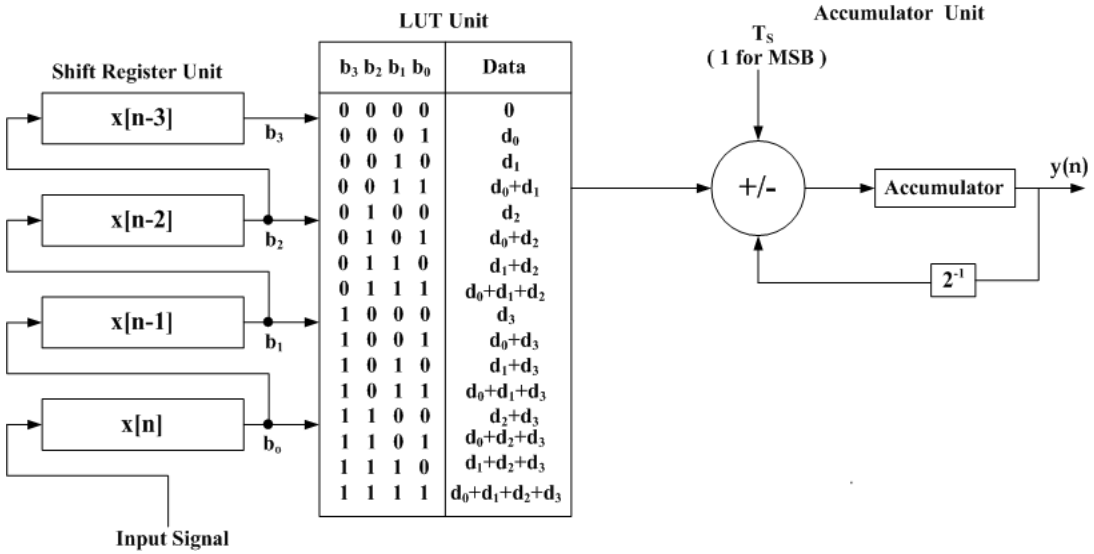
FA Full Adder HA Half Adder FIR Finite Impulse Response ADP Area delay Product OBC Offset Binary Code CSA Carry Save adder CLA Carry Look ahead adder CMOS Complementary metaoxide semiconductor



b_3 b_2 b_1 b_0	Data
0 0 0 0	0
0 0 0 1	d_0
0 0 1 0	d_1
0 0 1 1	d_0+d_1
0 1 0 0	d_2
0 1 0 1	d_0+d_2
0 1 1 0	d_1+d_2
0 1 1 1	$d_0+d_1+d_2$
1 0 0 0	d_3
1 0 0 1	d_0+d_3
1 0 1 0	d_1+d_3
1 0 1 1	$d_0+d_1+d_3$
1 1 0 0	d_2+d_3
1 1 0 1	$d_0+d_2+d_3$
1 1 1 0	$d_1+d_2+d_3$
1 1 1 1	$d_0+d_1+d_2+d_3$

Fig. 1 - Basic DA architecture

Minimizing, the Personal Computer in the digital system requires optimizing each step of the planning process. The technologies used to implement the digital circuit, as well as the circuit style, topology, and architecture, are discussed in this work.

This article describes in extension of multiplier less FIR filter with the following contribution.

1. In the multiplier less DA of the FIR filter, a thorough analytical framework is employed, which includes an EGDI method adder.
2. A new DA-based inner-product architecture is devised, complete with a suitable adder for decision feedback equalization.
3. A comprehensive synthesis investigation is described, with more precise results.

The remainder of the paper is rearranged in the following manner. The literature of the DA and EGDI is discussed in section.2. In section.3, the mathematical formulation of DA is explained. In section.4, the proposed EGDI adder approach for DA is developed. Section.5 contains a full explanation and comparison of the proposed design to the state of the art. The conclusion remarks are explained in section.6.

2. Literature Survey

Many researchers have been studied about Distributed Arithmetic architecture and its advantages. The author [1] proposed DA first time and a deep explanation have been explained by him. Later the formulation of DA and its advanced stage is explained by the author peled [2].

The memory less DA based FIR filter is explained in the article [3]. Also further the author explained the OBC DA filter for digital hearing aids application. DA architecture was more useful in decision feedback equalizer [4], image enhancement [5], for removing noises in the ECG signal analysis. In all these the DA based FIR filter plays a key role [6-9]. The basic block of GDI is explained in Fig.2. The truth table of the EGDI is shown in Fig.2.

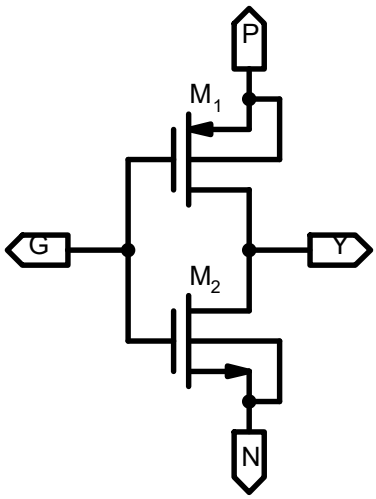


Fig. 2 - GDI technique

Table 1 - GDI tabular

P	N	G	D	Function
B	**Low**	**A**	**A'B**	**G_1**
High	**B**	**A**	**A'+B**	**G_2**
High	**Low**	**A**	**A'**	**NOT**
B	**High**	**A**	**A+B**	**OR**
Low	**B**	**A**	**AB**	**AND**
B	**C**	**A**	**A'B+AC**	**MUX**

When the, ' ***P'*** pin has input ' ***B'*** and the '***N'*** pin has input low or ground and A is given to the gate input of both NMOS and PMOSFETs then NMOS will be OFF mode and PMOS will be in ON state and finally output will be (**A'B)**. For next stage when ***P*** pin is high and ***N*** pin is B then the result will be **(A'+B).** Similarly when P pin is high and N pin is low then the result will be **A**'. When **P** pin is **B** and **N** pin is high then the output **Y** is OR gate. When **P** pin is Low, **N** pin is High then the result is AND gate. When **P** pin input is **B**, **N** pin is **C** then the result will act as a **MUX** gate.

2. 1 Functions of GDI

The GDI varies from the simple CMOS inverter structure as per the following:

1) Gate is common to both the NMOS and PMOS.
2) PMOS and NMOS are linked to N and P

The G1 and G2 functions were supported by the developed circuits, which are listed in Table.1 below. The reasons for this are as follows:

1. G1 and G2 are often referred to as complete logic families (allowing 2 input functions to be registered).
2. G1 is registered as a top-quality CMOS process (P) as a GDI function, with the N-MOS uniformly biased [10-14]

The main advantages of the GDI Technique are low area, low power, high speed and more flexibility to the designer.

A low-power design is better suited to the GDI Technique. The most major drawback of a GDI cell is that the O/P ratio is deteriorated. Strong logic 0 of weak logic 1 is produced by the NMOS. PMOS, on the other hand, generates either strong logic 1 or weak logic 0. It should be noted that the GDI Technique's main advantages are low power / high speed, smaller area, and greater flexibility. Modified logic is the most significant advantage in terms of production. On wave logic 1, NMOS produces stray logic 0, and on weak logic 0, PMOS produces stray logic 1. PMOS is turned on when G=0, and the P input is routed to the output. When G=1, NMOS is turned on for the input transferred to the output. While PMOS is turned on.

The input is logic 0, which results in a weak logic 0. When NMOS is turned on, however, input is at logic 1 in weak logic 1. As a result, PMOS produces weak logic 0 and NMOS produces Wave logic 1. The GDI cell is adjusted to supply stray logic 0, which can be deemed valid input to the subsequent stage. Sahoo and Deepesh proposed the study of different adders using full swing gate diffusion input and the Performance enhancements using swing restoration has been explained [15]. Forouzandeh *et.al*. proposed full adder design with GDI cell and independent double gate transistor. Using GDI cells reduces the number of transistors, and combining this technology with the double gate process reduces power and delay even further [16].

2.2. Formulation of DA

The inner product of 2 variables *C* and *x* are given as:

$$y = \sum_{k=1}^{K} C_k x_k \qquad (1)$$

$C_{k=}$ fixed coefficient,

$x_{k=}$ input signal

Nth bit 2's complement form *of* x_K is where $|x_k|<1$, & x_k is given as:

$$x_k = -b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \qquad (2)$$

$$x_k = \left\{ b_{k0}, \ldots\ldots\ldots b_{k(N-1)} \right\}$$

On substituting equ. (2) in (1), we get y as:

$$y = \sum_{k=1}^{K} C_k \left[-b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \right] \qquad (3)$$

The inner-product is shown in Equ. 3. On modifying summation, we get:

$$y = \sum_{n=1}^{N-1} \left[\sum_{k=1}^{K} C_k b_{kn} \right] 2^{-n} + \sum_{k=1}^{K} d_k (-b_{k0}) \qquad (4)$$

Equ.4 is our DA equation. The summing in equ.4 will only have 2^k potential options because each b_{kn} can have a value of 1 or 0. All of these values can be computed ahead of time and stored in memory. To accommodate the summing, memory must include all 2k possible combinations, where b_{k0} denotes the sign bit of the provided input in the summation. As a result, the ROM's overall size will be 2*2k. The input data is directly assign to memory and is demonstrated in Fig.1.

3. Proposed DA based FIR Filter using EGDI Technique:

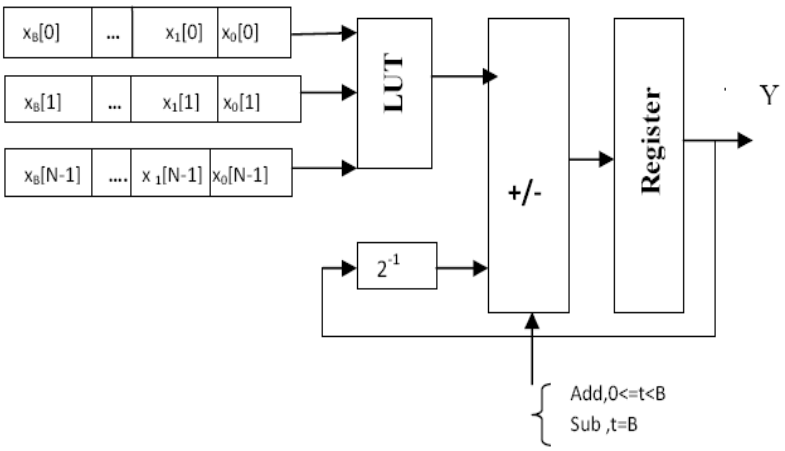


Fig. 3 - Proposed DA based FIR filter

A summation block, an accumulation block, and partial product generators are all included in the proposed DA block. In registers, the input samples and coefficients are preserved, as is the bracketed term in Eqn. By feeding partial products into the summation block, four potential combinations are formed online. The DA partial product generator is shown in Fig.3. Typical distributed arithmetic filters are driven by the input samples. The distributed arithmetic system in DA is driven by the coefficients, and the coefficients that drive the MUX are already multiplexed together to improve component reuse.

The summation block is made up of a tree-like arrangement of registered adders. The adders are registered at the outputs for convenience of implementation, which implies that the partial products advance one level in the tree every clock cycle. The output from the summation block is shifted and aggregated in the accumulation block (Fig. 3), with the result ready after R*B clock cycles.

3.1. Proposed EGDI Technique

This modification of GDI by enhancement of gate to salient features became noticeable. The bulk terminal of PMOS is continuously converted to the supply voltage, whereas NMOS reduces the bulk effect. The conductivity between the transistors is limited to deserve static power consumption. This design is amenable to twin well CMOS, SOI, and SOS technology. Fig.4 shows the primary EGDI cell having for terminal structure. Table 2 shows the logic function. One of the newest techniques for lowering power usage is the EGDI Technique. This enhanced gate diffusion input allows logic styles to scale back the world, power, and power consumption within the digital circuit. The basic improved GDI also includes less voltage, as seen in the diagram below, and the high voltage connector should be attached to the bottom. The PMOS transistor is linked to the enhanced GDI cell's high voltage, which is referred to as power supply or VDD.

The NMOS transistor is similarly attached to the bottom, which is nothing more than low supply voltage, or VDD. The GDI cell that was made is functional. All of the PMOS transistors in the proposed GDI cell are connected to the VDD using typical CMOS technology. The low constant voltage is connected to all of the NMOS transistors in the same way. Standard four-terminal PMOS and NMOS transistors are used in the enhanced GDI cell. Non-like twin-well CMOS technology, Silicon on Insulator (SOI) technology, and Silicon on Sapphire (SOS) technology can all be used to make the enhanced GDI cell. Table.2 shows the different logic functions in various input settings. The fundamental improved gate diffusion input cell is shown Fig.4.

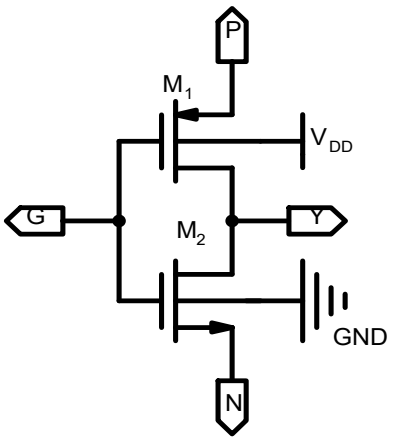


Fig. 4 - Proposed EGDI cell

Table 2 - Various logic functions implemented by using EGDI cell

P	N	S_P	S_N	G	D	Functions
1	0	1	0	A	A’	INVERTER
0	A	A	A	B	AB	AND
A	1	D	0	B	A+B	OR
A	A’	1	0	B	A’B+AB’	XOR
A’	A	1	0	B	AB+A’B’	XNOR
B	0	B	0	B	A’B	G1
1	B	1	0	A	A’+B	G2
B	C	1	0	A	A’B+AC	MUX

Fig.5 shows the GDI technique half adder and Fig.6 shows the proposed EGDI half adder. When we observe GDI HA it requires 10 transistors for design of HA. But by using EGDI technique it requires 8 transistors When A and B inputs are low the result is low and when any one of the input is high the output is high and finally when two inputs are high then sum will be zero and carry will be high. Two transistors are reduced when compared with existing HA design. For full adder design using EGDI technique it requires 10T and which is used in our proposed DA based FIR filter. The block diagram of the EGDI FA is shown in Fig.7. By using proposed EGDI HA and FA the area occupied by the circuit is less when compared with the normal full adder design used in DA FIR filter.

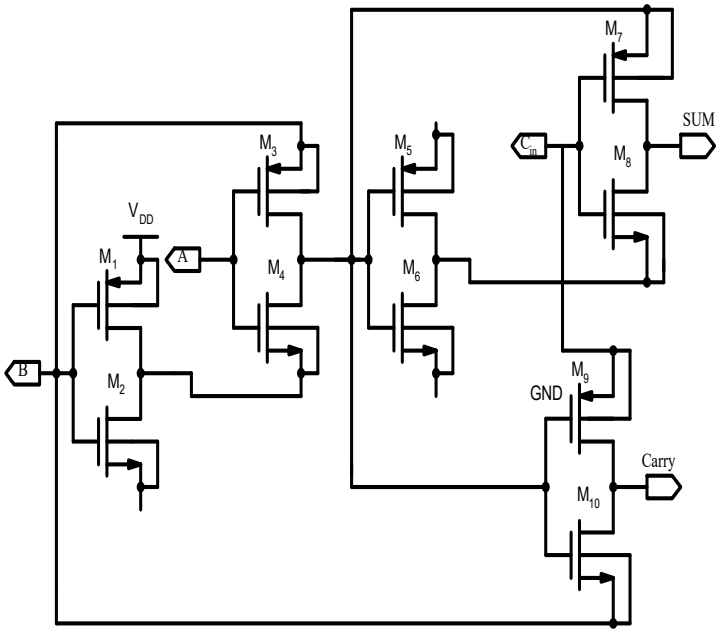


Fig. 5 - Half adder using GDI technique

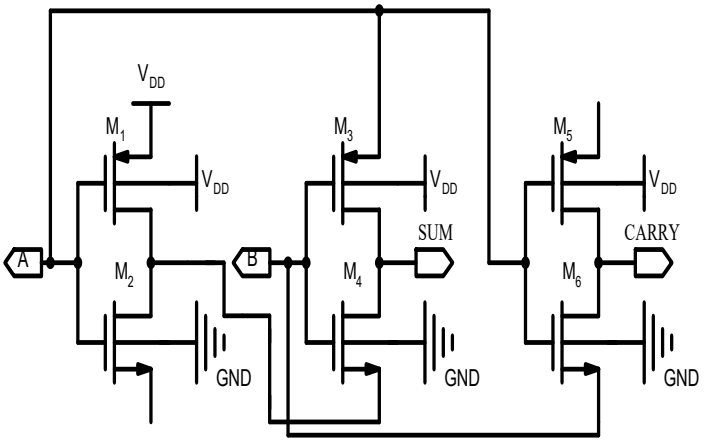


Fig. 6 - EGDI half adder

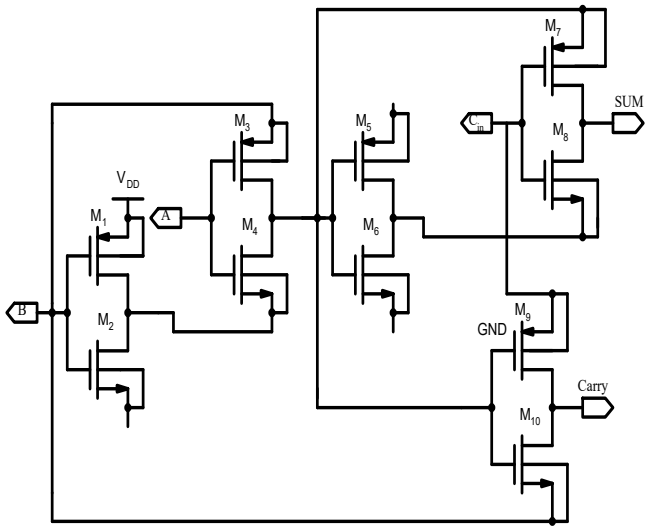


Fig. 7 - EGDI full adder

4. Result Analysis

The proposed EGDI based full adder used in DA based FIR filter has been implemented using Verilog HDL and synthesized in Synapsis design compiler tool. The synthesis results of the proposed EGDI full adder are shown in Table.3. When we observe the table the proposed EGDI full adder will have less number of transistors when compared with the other existing designs. Also the power consumption of our technique is less when compared with other designs.

As the delay time of the design is less it has high frequency when compare with other designs. This FA is used in our DA based FIR filter so that our design will occupy less area and power consumption when compared with other existing models. The area, power report and frequency are shown in Table.4 and Table.5. Fig.8 and Fig.9 gives show the area and power report of the proposed and existing designs.

Table 3 - Comparison full adder with different techniques

Hardware	64 bit Full adder		
	CMOS	GDI	EGDI
No.of Transistors	125	102	90
Power Dissipation	302.15 uW	100.25uW	56.55Uw
Delay	500.25ns	302.65ns	250ns

Table 4 - Power report of proposed and existing design in (mw)

	EGDI Full adder based DA FIR filter			
	CLA	CSA	4:2 Compressor	EGDI technique
4-TAP	115	114	111	100
8-TAP	136	135	129	112

CLA –Carry look Ahead adder CSA-Carry Save adder

The Carry Look Ahead (CLA) design is based on the notion of looking at lower input adder bits and adding if higher orders carry generated. This adder lowers carry delay by lowering the number of gates a carry signal must pass through. Three bits are added in parallel in the Carry Save Adder (CSA). The carry is not propagated through the stages

in this method. Carry is instead stored in the current stage and updated as an addend value in the subsequent stage. As a result, the carry latency is decreased in this method.

Table 5 - Area report of proposed EGDI FA based FIR filter (µm²)

	EGDI full adder based DA FIR filter			
	CLA	**CSA**	**4:2 Compressor**	**Approximate Compressor**
4-TAP	**2988**	**2897**	**2853**	**2812**
8-TAP	**4459**	**4381**	**4225**	**4121**

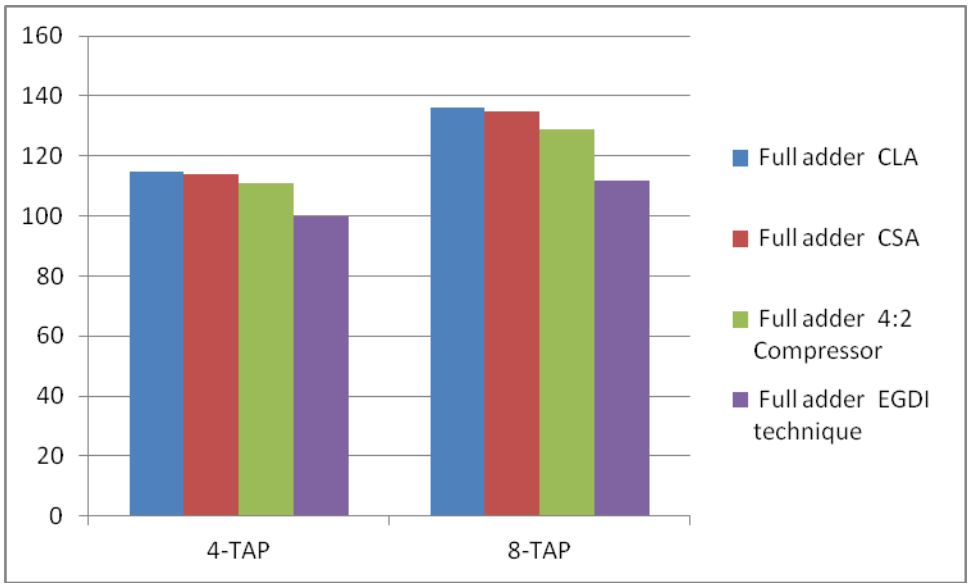


Fig. 8 - Power report

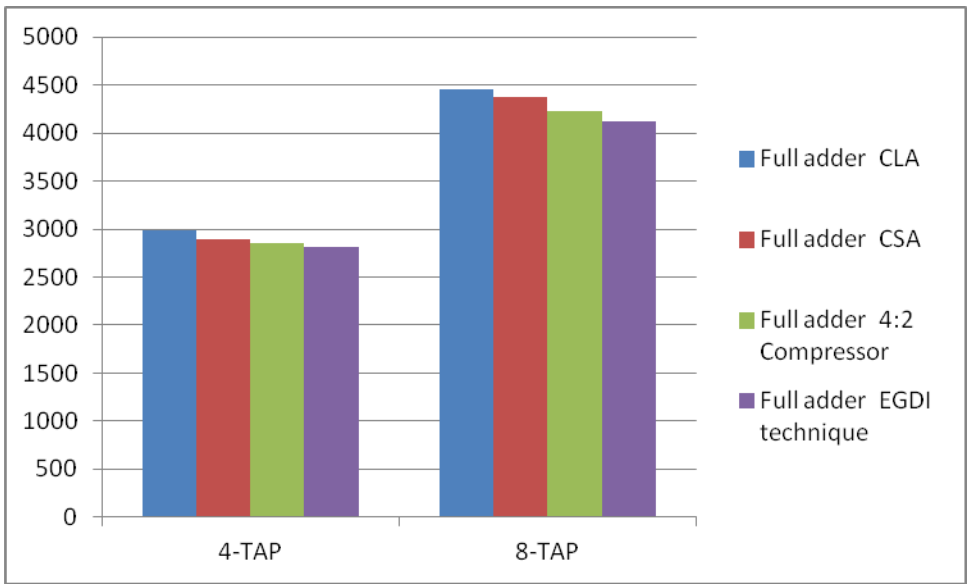


Fig. 9 - Area report

5. Conclusion

In this paper, our main aim is to design DA based FIR filter that has low power dissipation, more processing speed, and delay. After designing and simulation all the circuits present in the Synapsis design compiler. We made a relative analysis of the 4-tap, 8-tap. Using several Techniques Such as CMOS Technique, GDI Technique, and EGDI Technique few observations are achieved. The circuital work is feasible just because of using EGDI Technique over old-school Techniques, which reduces the power dissipation this makes a vast difference between the 3 Techniques high speed. The proposed EGDI full adder is used in our DA based FIR filter which will occupy less area and power consumption when compared with other designs. After a comparative analysis, the effective output has been observed, which was reached by comparing our multiplier by using a different technology such as EGDI to other primary techniques like GDI and CMOS.

Acknowledgement

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