Noname manuscript No.
(will be inserted by the editor)

A 70.7-dB SNDR 100-kS/s 14-b SAR ADC with Attenuation Capacitance Calibration in 0.35-μm CMOS

Stefano Brenna · Andrea Bonfanti · Andrea Leonardo Lacaita

Received: date / Accepted: date

Abstract In sensor applications, low-power and moderate-high resolution analog-to-digital converters (ADCs) are needed to convert the analog front-end signal output. Such systems are often multi-channel and require analog multiplexing. In these cases, even when high resolutions are required, continuous time $\Delta\Sigma$ ADCs can't be adopted, and an efficient data-conversion must be achieved relying on different topologies, typically Successive Approximation-Register (SAR) ADCs. Since these systems are often implemented in CMOS processes like 250-nm and 350-nm CMOS to benefit from a large supply voltage, the SAR ADC design is challenging due to the technology mismatch and to the limited number of metals available to optimize the layout.
This paper presents a SAR ADC implemented in 350-nm CMOS technology with a physical resolution of 14 bits using a binary weighted with attenuation (BWA) capacitor array. The proposed converter exploits a semi-custom and isotropic unit capacitance with ground shield to avoid proximity effects and parasitic capacitances across its terminals, an optimized capacitive array layout insensitive to both linear and radial oxide gradients, and an efficient calibration algorithm to compensate the parasitic capacitances that worsen the converter linearity. At 1.8-V supply and 100-kSps sampling frequency, the proposed ADC achieves an SNDR of 70.7 dB, an SFDR of 81.8 dB, an ENoB of 11.45 and a power consumption of 43.4 μW, corresponding to a Figure-of-Merit (FoM) of 155 fJ/conv.step. To the best of our knowledge, this figure is the best among SAR converters implemented in 350-nm or less scaled technologies, and in-line with other ADCs featuring an SNDR larger than 70 dB.

S. Brenna, A. Bonfanti, A.L. Lacaita
Dipartimento di Elettronica, Informazione e Bioingegneria
Politecnico di Milano
Via Golgi 40, 20133, Milano, Italy.
Tel.: +39-02-2399-3678; Fax: +39-02-2367604
E-mail: stefano.brenna@polimi.it, andrea.bonfanti@polimi.it, andrea.lacaita@polimi.it
S. Brenna is now with Intel Labs, 2111 NE 25th Ave, 97124 Hillsboro (OR), USA.

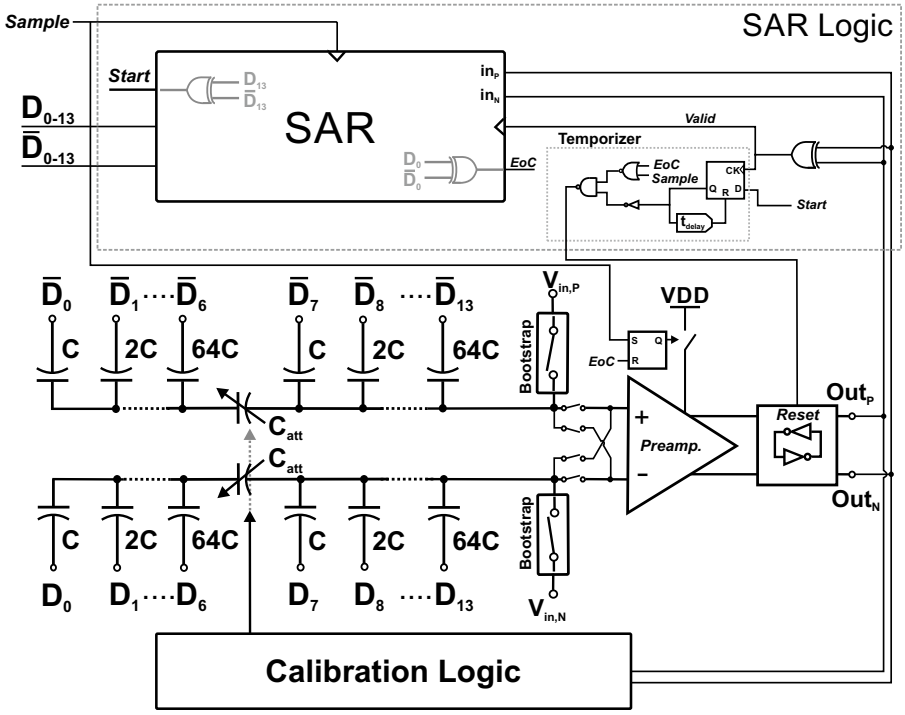

Fig. 1 Schematic of the proposed 14-bit converter.

Keywords ADC · analog-to-digital conversion · nonlinearity · mismatch · asynchronous logic · successive approximation register · calibration algorithm

1 Introduction

Analog-to-digital converters (ADCs) featuring moderate sampling rates (0.01-1 MSps) and relative high resolutions (SNDR>70 dB) are key components in energy-limited applications, such as implantable medical devices, smart sensors or portable systems. For such applications, successive approximation-register (SAR) converters are preferred over $\Delta\Sigma$ topologies due to their better trade-off between power efficiency and conversion accuracy [1] and when multiplexing of the front-end analog outputs is required to save area [2–4]. In such ADCs, the accuracy is mainly set by the capacitive array, serving as both digital-to-analog converter (DAC) and sample-and-hold. To reduce the statistical spread that can worsen the converter linearity, the size of the unit capacitor must be increased, eventually resorting to custom unit elements with high accuracy and low specific capacitance [5,6], at the cost of a larger switching energy and a lower sampling frequency. A possible alternative is the use of calibration algorithms or oversampling/dithering techniques, which however imply

an increased design complexity [6–8] and a typical non negligible power consumption [9,10]. Thus, as the converter resolution rises, both capacitive array dimensions and number of unit elements to be connected increase, leading to a more complex routing of the interconnections and to a larger sensitivity to linear and radial oxide gradients. This issue is exacerbated in CMOS processes like 250- or 350-nm CMOS, which are still the most widely adopted in sensing applications. In fact, because of the limited number of available metal levels, the capacitances are implemented close to the substrate being more subject to oxide gradients due to the surrounding active circuits [11,12].

In this work, a fully-differential 14-bit SAR ADC is proposed for moderate-high resolution sensing applications in a 350-nm CMOS technology (see Fig. 1). In order to reduce the total number of unit capacitors to be connected, keep the area as low as possible, and control the wiring parasitics, its capacitive DAC is implemented as a binary weighted with attenuation (BWA) capacitor topology, featuring an optimized layout geometry insensitive to linear and radial oxide gradients. The array exploits a shielded and isotropic semi-custom unit capacitance to greatly reduce the parasitics across its terminals, which can compromise the converter accuracy. The residual parasitic capacitance is compensated by a foreground calibration algorithm acting on the bridge capacitor.

The comparator is designed as a cascade of a static preamplifier and a dynamic latch to reduce the impact of kickback noise, capacitive feed-through and non-linear input capacitance. To limit its power consumption, the preamplifier is turned on only after the sampling phase during the evaluation of the 14 bits and switched off at the end of the conversion.

Finally, an asynchronous and fully-differential dynamic logic is adopted to minimize the power consumption of the digital circuit.

At 1.8-V supply and 100-kSps sampling rate, the proposed ADC achieves a peak SNDR of 70.7 dB, an ENoB of 11.45, and a power consumption of 43.4 μW. This corresponds to a Figure-of-Merit (FoM) of 155 fJ/conv.step, the best efficiency among converters in 350-nm CMOS process or less scaled technologies, and in line with other implementations featuring an SNDR larger than 70 dB.

The paper is organized as follows. Section 2 describes the implementation of the semi-custom capacitances, the layout of the capacitive array and the calibration technique that sets the attenuation capacitance value. Section 3 explains in detail the design of the sampling switches, the comparator and the asynchronous dynamic logic. Measurement results are shown in 4 where the proposed ADC is compared with a second converter designed without an optimized layout of the DAC and without any calibration algorithm. Finally, conclusions are drawn in Section 5.

2 Capacitive DAC

In SAR converters, the linearity of the capacitive DAC usually limits the overall accuracy. As the resolutions increases, this building block becomes more sensitive to mismatch and parasitics requiring a smart topology choice, a careful layout and a calibration circuit [13]. For the proposed capacitive DAC, the key choices to improve the accuracy-power trade-off are summarized as follows:

- the most convenient array topology is selected to reduce the wiring complexity;
- an isotropic semi-custom capacitor with a ground shield is adopted to avoid proximity effects and drastically reduce the top-to-bottom stray capacitances;
- an optimized capacitive array layout is implemented to mitigate the impact of linear and radial oxide gradients;
- the residual parasitic capacitances are compensated by an efficient calibration algorithm acting on the attenuation capacitor of the array;
- a modified monotonic switching algorithm [14] is applied to improve the conversion efficiency.

These features are analyzed in depth in the following.

2.1 Array structure

The capacitive DAC has been implemented with a BWA topology [15]. This architecture is commonly used for resolutions larger than 10 bits [7, 11] for sake of compactness and to reduce layout complexity, since the capacitive banks corresponding to the most-significant bits are built with a smaller number of unit elements than in the conventional binary-weighted (CBW) array. The attenuation capacitor, C_{att}, splits the array into two binary weighted sub-arrays: a main-DAC and a sub-DAC (see Fig.2). The proposed converter exploits equal main- and sub-DACs (i.e., with 7 bits each) and $C_{att} \cong C_u$, since it is the most energy-efficient solution [15]. Moreover, in order to further reduce the number of unit capacitances, saving area and power, a top-plate sampling technique has been adopted [14].

2.2 Non-linearity in capacitive DACs

The linearity of the capacitive DAC is limited by both parasitic capacitances and process mismatch affecting the unit elements. Regarding the parasitics effect, it has been shown [5] that the parasitic capacitance, $C_{par,main}$ (see Fig. 2), connected from the top-plate of the main-DAC to ground (or V_{DD}) only produces gain error, while the sub-DAC stray capacitance, $C_{par,sub}$, can degrade the linearity performance of the BWA converter. In fact, this parasitic

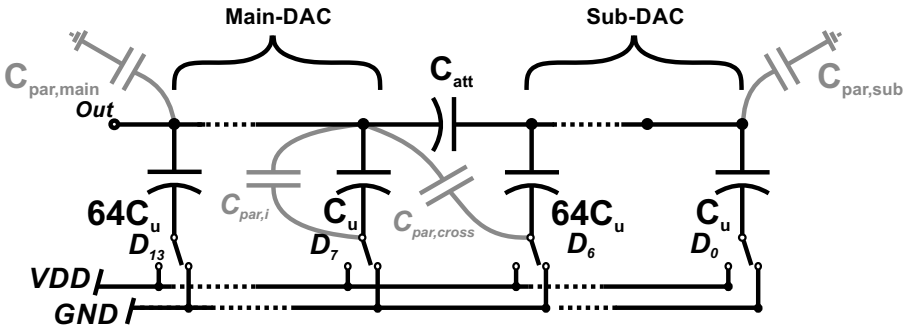

Fig. 2 14-bit BWA DAC with the main- and sub-DAC top-plate parasitic capacitances.

capacitance generates two equal peaks in the DNL pattern every $2^{\frac{N}{2}}$ codes, whose value, for the monotonic switching algorithm, is approximately [5]

$$DNL_{peak} \cong \frac{2^N \cdot C_{par,sub} - 2^{\frac{3N}{2}} \cdot (C_{att} - C_u)}{2^{N+1} C_u}, \tag{1}$$

where C_u and C_{att} are the unit and the attenuation capacitance, respectively. This contribution is deterministic and can be canceled by acting on the attenuation capacitor value.

Other parasitics that affect the converter linearity are those connected across top and bottom terminals of each capacitive bank and those connected from the bottom plate of the sub-DAC capacitors to the top-plate of the main-DAC. Examples of these parasitics are shown in Fig. 2 as $C_{par,i}$ and $C_{par,cross}$, respectively. In general, these parasitics should be minimized or, as for $C_{par,i}$, scaled accordingly to the corresponding capacitive bank since their calibration requires complex circuits [9].

With regard to capacitance mismatch, its effect can be quantified by the maximum standard deviations of the DNL ($\sigma_{DNL,max}$), which typically occurs at mid-code. For a BWA converter, this parameter has been analytically derived in [15] as function of the relative standard deviation of the unit capacitance, $\sigma\left(\frac{\Delta C}{C_u}\right)$

$$\sigma_{DNL,max} = 2^{\frac{3N}{4}} \cdot \sigma\left(\frac{\Delta C_u}{C_u}\right). \tag{2}$$

When considering two equal unit capacitances placed at a distance x, their relative $\sigma\left(\frac{\Delta C_u}{C_u}\right)$ can be assessed as [16]

$$\sigma\left(\frac{\Delta C_u}{C_u}\right) = \sqrt{\frac{k_c^2 c_{spec}}{C_u} + S_c^2 x^2}, \tag{3}$$

where k_c is the Pelgrom mismatch coefficient, c_{spec} the specific capacitance, and S_c a size-independent coefficient. The traditional approach [5,6] implies the choice (or design) of a capacitor with the minimum value of $k_c^2 c_{spec}$ and

to size the unit capacitance, C_u, so that $\sigma_{DNL,max} < 0.5$, neglecting the size-independent term ($S_c^2 x^2$ in Eq. (3) [5,6,15,17]). The unit capacitances are then arranged adopting a common-centroid layout to reduce the effects of linear process gradients. However, the presence of active circuits surrounding the array can produce non-linear (radial) gradients affecting the converter linearity. This effect is strongly influenced by the capacitors available in the process-design kit. In fact, if these capacitors, like poly-insulator-poly (PiP) capacitors, are implemented close to the silicon substrate, active devices nearby the DAC could modify the oxide thickness and thus the value of the capacitances throughout the array (see Fig. 3). Such radial gradients have already been addressed as a realistic source of non-linearity in [11,12] but no specific layout geometry has been proposed to mitigate their effect.
Thus, for high-resolution converters, the proper sizing of the unit capacitor according to Eq. (2) is not enough to guarantee the desired accuracy, and a careful layout of the array with an arrangement of the unit elements insensitive to process gradients, a custom unit capacitor design and a calibration of the parasitic capacitances affecting the array are often needed.

2.3 Unit capacitance and array implementation

In the chosen austriamicrosystems (AMS) 350 nm CMOS process, only PiP capacitors implemented between two layers of polysilicon are available. These capacitances, represented in Fig. 4, are non isotropic and their value strongly influenced by interconnect parasitics. In fact, the absence of any kind of shield between the metal wires connecting the top- and the the bottom-plate results in a high sensitivity to wiring parasitics. Since the required 14-bit physical resolution also imposes a careful disposition of the array capacitors to minimize the impact of the aforementioned gradients, the connection between the capacitive banks becomes complex and the resulting top-to-bottom parasitics can strongly degrade the converter linearity.

For this reason, in the proposed converter a different unit capacitor has been developed, as shown in Fig. 5. This topology is completely isotropic and shielded from wiring parasitics. The core of the proposed capacitance is a 200-fF PiP capacitor from the available design kit (AMS 350-nm CMOS process) with good matching properties, being its Pelgrom coefficient and its specific capacitance equal to $0.45\% \cdot \mu$m and $0.85\,\mathrm{fF}/\mu\mathrm{m}^2$, respectively. In theory, these properties should guarantee a σ_{DNL} (see Eq. 2) lower than 0.5 for the proposed converter considering the only proximity mismatch given by Eq. 3. However, to improve symmetry while making its value independent of the parasitics, the top-plate made in the highest level of polysilicon (POLY2 layer in Fig. 5) has been completely covered by a plate made of the first metal layer (MET1) connected to the bottom-plate in polysilicon (POLY1). This results in an isotropic "sandwich" capacitor, i.e., metal-insulator-poly-insulator-poly (MiPiP) capacitor, featuring an overall capacitance of 250 fF, according to the layout parasitic extractor (Cadence Assura). A shield in metal3 (MET3 in Fig.5) connected to

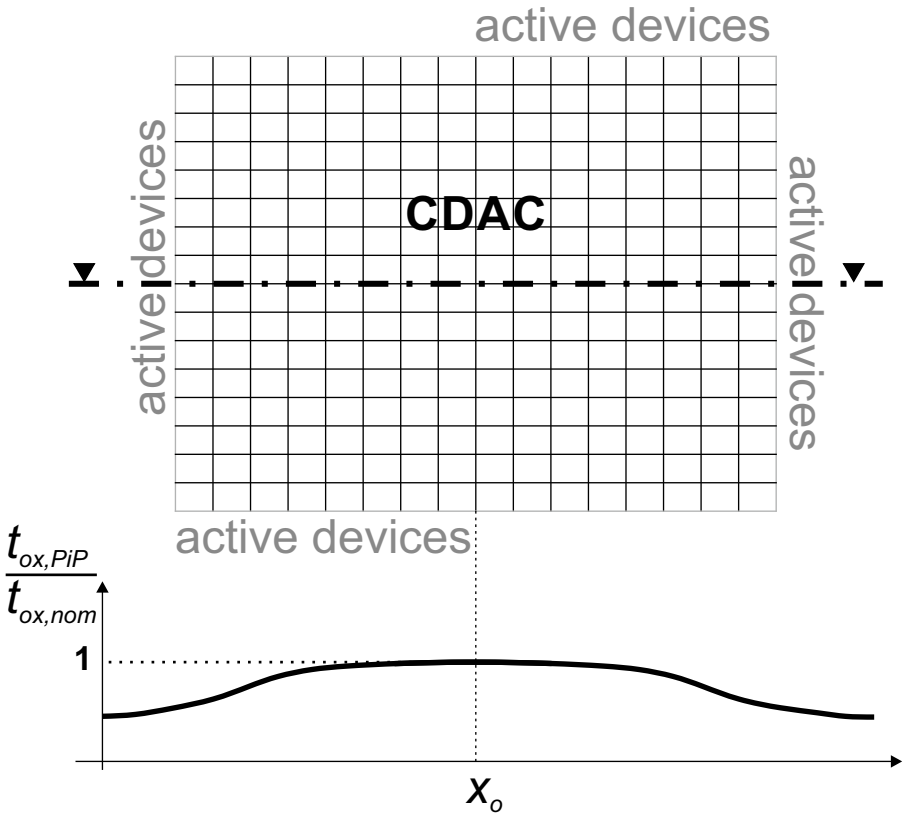

Fig. 3 Example of a possible radial gradient of the oxide thickness affecting a capacitive DAC.

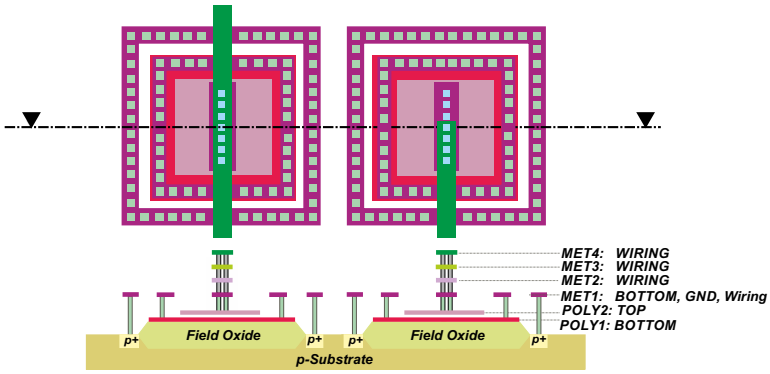

Fig. 4 Poly-insulator-poly (PiP) standard capacitors.

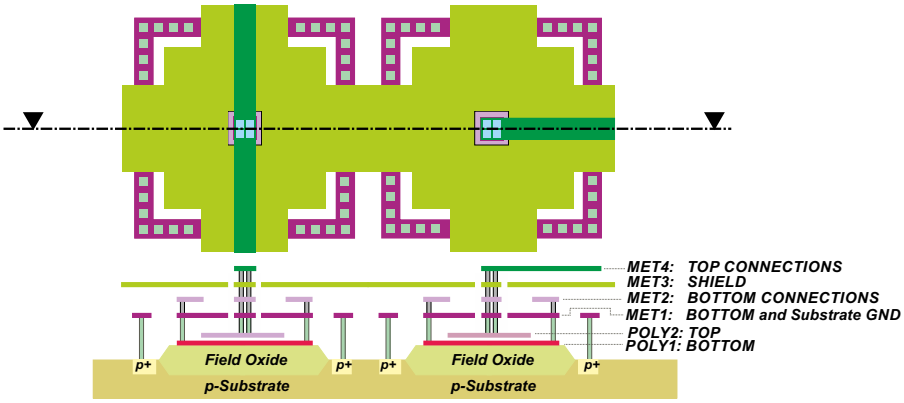

Fig. 5 Proposed shielded MiPiP "sandwich" capacitor.

ground covers the capacitor, while the wires that convey the signals to the top- and bottom-plate are implemented in metal4 (MET4) and in metal2 (MET2), respectively. In this way, a parasitic capacitance from top- to bottom-plate is avoided. The remaining parasitic capacitances are from the capacitor terminals to ground, which can contribute to $C_{par,main}$ and $C_{par,sub}$ of the proposed capacitive DAC. However, the former contribution does not affect the converter linearity and the latter can be compensated through a calibration algorithm acting on the attenuation capacitor (see Eq. 1). These unit elements have to be arranged in the array layout in order to take into account both linear and radial gradients.
For this purpose, a DAC layout completely symmetric to its origin (the physical center of the array) is designed as shown in Fig. 6. Moreover, dummy capacitances are placed at the boundary of the array and further separate the peripheral capacitors from the borders. Such a disposition makes the capacitive array insensitive to linear gradients in any directions, as in a traditional common-centroid layout, but also to the aforementioned radial gradients. The attenuation capacitor is placed close to the center since its value is set through a calibration algorithm, as discussed in the next section.

2.4 DAC parasitics compensation

Due to the aforementioned design choices, the array is expected to be rather insensitive to capacitance mismatch deriving from oxide gradients, while almost all parasitic capacitances have been concentrated into the sub-DAC top-plate contribution, $C_{par,sub}$. Its effect on the converter nonlinearity (see Eq. 1) can be compensated by setting the attenuation capacitance value to

$$C_{att} = C_u + \frac{C_{par,sub}}{2^{\frac{N}{2}}}. \tag{4}$$

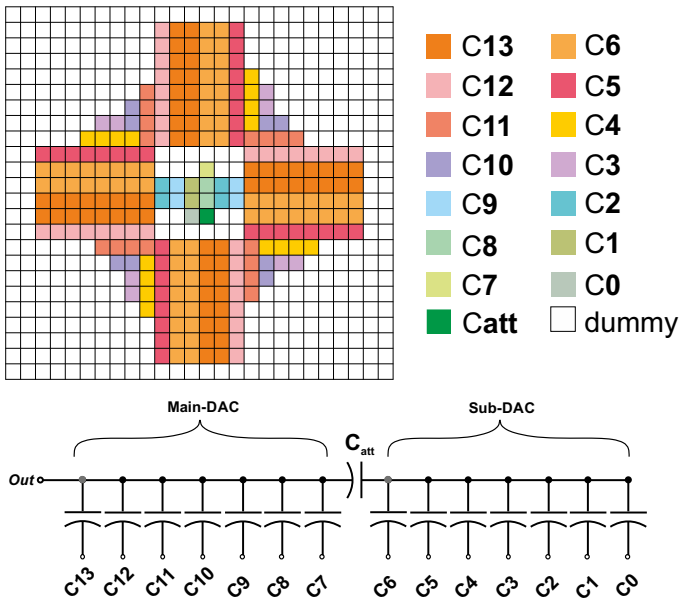

Fig. 6 CDAC layout insensitive to radial and linear oxide thickness gradients.

However, the spread affecting both the attenuation and the parasitic capacitances does not allow to set *a piori* the value of C_{att}, as in [18]. To this purpose, in the proposed converter the attenuation capacitance is sized through a calibration algorithm implementing a feedback mechanism [19,20]. The attenuation capacitance has been split in a fixed nominal capacitance, $C_{att,nom}$=215 fF, 15% lower than the value of C_u, and a bank of 64 capacitances, C_{cm}=1.35 fF, which can be connected in parallel to the nominal bridge capacitance by means of pass-transistors, as shown in Fig. 7(a). Their small value allows to compensate the DNL peaks with a resolution of 0.25 LSB. Simulations have been performed through a Matlab tool (CSAtool, [21]) in order to verify the validity of the proposed compensation method, considering the estimated value $C_{par,sub}$=600 fF. As shown in Fig. 8(a), for the nominal value of C_{att} the DNL pattern exhibits 2 consecutive positive peaks every $2^{\frac{N}{2}}$ codes of about 10 LSB, leading to a severe distortion in the static characteristic (see Fig. 8(b)). By increasing the value of C_{att}, the peak amplitude decreases and becomes negligible (< 0.1 LSB) when 29 modules are activated, resulting in an overall attenuation capacitance of 254.15 fF, close the value derived from Eq. 4 of 254.7 fF. For a further increase of the attenuation capacitance, the peaks eventually become negative yielding again linearity degradation. Since all the calibration capacitances (C_{cm} in Fig. 7(a)) have equal size, the actual value of the attenuation capacitor can be modified changing the number of modules that are connected in parallel to the fixed contribution, $C_{att,nom}$. This operation can be easily accomplished through a serial register of 64 flip-flops, driven by an $UP/\overline{DOWN}$

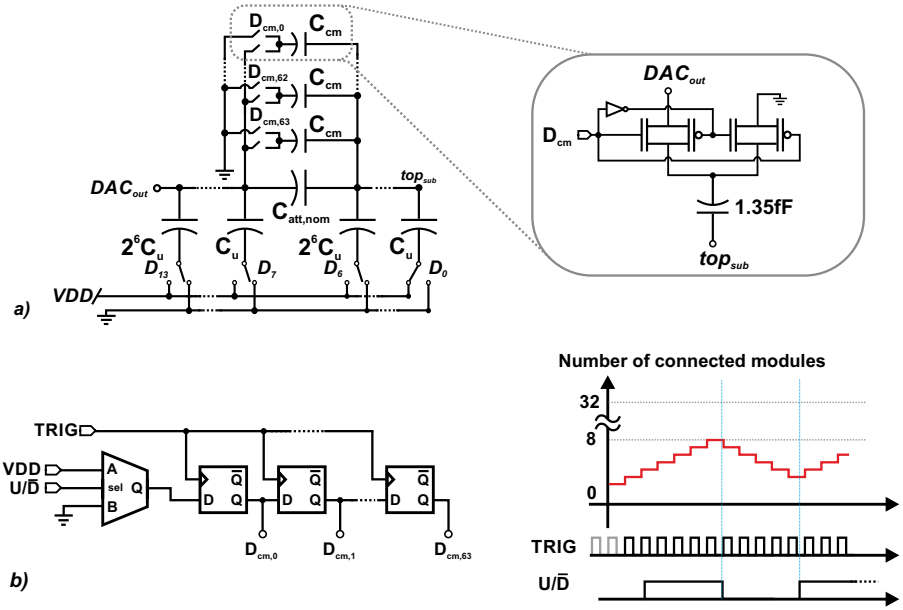

Fig. 7 Capacitive DAC with calibration of the attenuation capacitor (a). The number of unit calibration capacitors is controlled by a serial register (b).

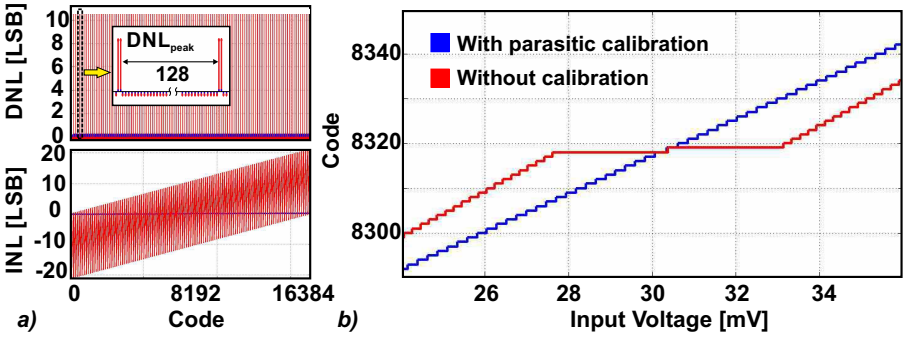

Fig. 8 Simulation results showing periodical DNL and INL patterns due to a parasitic capacitance $C_{par,sub}$=600 fF with and without calibration (a) and detail of the static characteristic highlighting the effect of the calibration (b).

signal and a clock ($TRIG$), as shown in Fig. 7(b).
The calibration is performed at the start-up and its working principle is briefly described in the following. When the calibration is enabled, the SAR logic circuit is disabled to directly control the bottom plates of the main- and sub-DAC capacitors through two auxiliary signals, B_C and $B_{C,N}$, as shown in Fig. 9. First, both the ADC inputs are short-circuited and connected to the common-mode voltage, $V_{DD}/2$, while the bottom plates are all connected to ground.

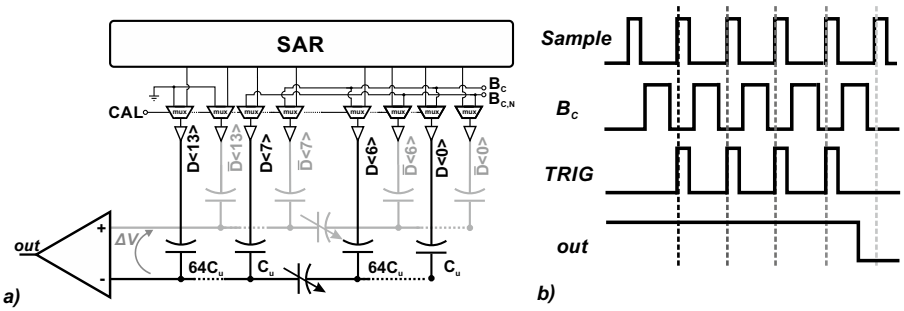

Fig. 9 Simplified schematic of the circuit enabling the calibration algorithm (a) and time diagram of the control signals (b).

Then, the input switches are turned off leaving the input of the comparator floating, and $\overline{D}_7$ in the positive DAC and all the bits connected to the sub-DAC of the negative array, $D_{0:6}$, are forced to V_{DD} setting $B_{C,N}$=1. It's easy to verify that this condition yields a differential voltage at the comparator input, $V_{in,p} - V_{in,n}$, equal to

$$\Delta V \cong \frac{V_{DD}}{C_{main} + C_{par,main}} \left[C_u - \frac{C_{att}}{1 + \frac{C_{par,sub}}{C_{sub}}} \right], \tag{5}$$

C_{main} and C_{sub} being the overall capacitance of the main- and sub-DAC, respectively, both equal to $2^{\frac{N}{2}} C_u$. This condition can be useful to detect the optimum value of the attenuation capacitance. In fact, Eq. 5 suggests that the comparator input voltage changes signs when C_{att} overcomes the optimum value given by Eq. 4. Therefore, in the calibration phase, the number of capacitances C_{cm} that are connected in parallel to the fixed attenuation capacitor is progressively increased until the comparator output toggles from 1 to 0. As soon as this condition is verified, the procedure is stopped and the number of calibration capacitances actually in use is stored. It's worth pointing out that the calibration capacitors have one terminal tied to the top-plate of the main-DAC and the other one connected either to ground or to the sub-DAC. Every time a capacitor C_{cm} is connected in parallel to the actual attenuation capacitor, the top-plates of the main DACs, i.e., the comparator inputs, are forced to the common mode voltage, $V_{DD}/2$ and then $B_{C,N}$ is pulled up. This procedure avoids the problem of the initial charge on the calibration units that can affect the charge balance altering the accuracy of the calibration algorithm.

Indeed, with this aforementioned procedure, the voltage difference at the comparator input is function of the capacitances C_{att} and $C_{par,sub}$ of the negative array. In order to cope with relative mismatch between the two arrays, the same procedure is repeated pulling up to V_{DD} the control signal B_C, thus forcing to 1 D_7 in the negative DAC and all the bits connected to the sub-DAC of the positive array, $\overline{D}_{0:6}$, after the sampling phase. This allows to

correctly calibrate also the attenuation capacitance of the positive array. However, the result of these calibrations is affected by the comparator offset, leading to an incorrect assessment of the optimum attenuation capacitance, i.e.,

$$C_{att} = \left[C_u + \frac{V_{os}}{V_{DD}} \left(C_{main} + C_{par,main} \right) \right] \cdot \left(1 + \frac{C_{par,sub}}{C_{sub}} \right). \tag{6}$$

For example, considering V_{DD}=1.8 V, a worst-case offset of -1 mV, and a capacitance of the main-DAC of 32 pF, the attenuation capacitance is underestimated by 17.8 fF with respect to the optimum value of 254.7 fF. This turns into DNL peaks of about 3 LSB. To avoid the effect of the comparator offset, the calibration procedure is repeated swapping the comparator inputs, i.e., the positive array is connected to the negative input and vice-versa. The values of C_{att} obtained in the two calibration steps are averaged and the effect of the comparator offset is completely canceled out, without any additional calibration [19].
It's worth pointing out that this calibration method, differently from the works in [19,18], acts directly on the attenuation capacitance, rather than trying to calibrate the parasitic capacitance, thus allowing to save a great amount of area. In fact, since the effect of a single capacitance in the sub-DAC is attenuated by a factor $C_{att}/C_{main} = 2^{(N/2)} = 128$, the same range of compensation would be obtained adding a capacitance at the top-plate of the sub-DAC variable from 0 to 11 pF, made of 64 capacitance of 173 fF, and sizing the attenuation capacitance as $1.2C_u$=300 fF.

2.5 Switching algorithm

The proposed converter adopts a modified version of the efficient monotonic switching algorithm, also known as set-and-down, presented in [14]. Differently from the original switching procedure proposed by [14], during the sampling phase the bottom plates of the two MSB capacitors are connected to ground instead of V_{DD} like all the others. According to the result of the first bit evaluation, one of the two capacitors is connected to V_{DD}. From the second bit onward the algorithm proceeds as the monotonic procedure until the LSB is assessed. The variation in the MSB evaluation step, shown in Fig. 10, implies an initial increase of the common-mode DAC output voltage by $V_{DD}/4$. Then, the common mode voltage drops monotonically to $V_{DD}/2$, instead than to ground as in the traditional monotonic algorithm, reducing the non-linear effects deriving from the offset variations at the comparator input along the conversion cycle [14]. Moreover, this allows the adoption of an NMOS differential pair (rather than a PMOS topology, mandatory adopting a monotonic algorithm), reducing the non-linear input capacitance for the same amount of power consumption and thermal noise.

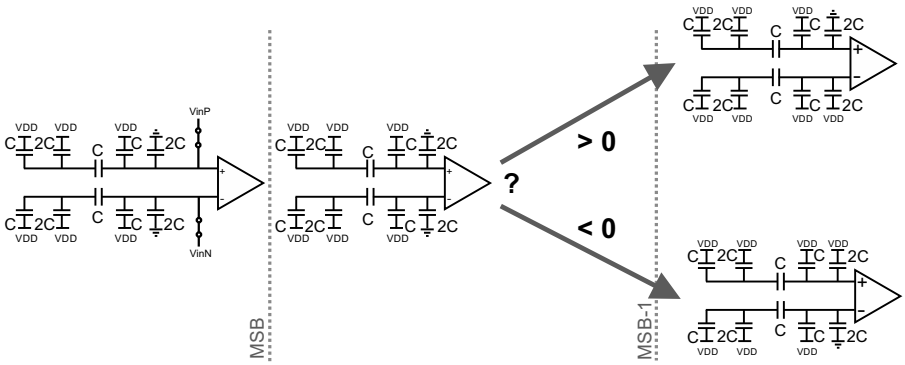

Fig. 10 Variation of MSB evaluation step of the proposed switching algorithm with respect to the original monotonic procedure in [14].

3 Active circuits design

The scheme of the proposed 14-bit converter is shown in Fig. 1. In order to achieve a better common-mode noise rejection and less distortion, a fully-differential topology is adopted. This section is devoted to describe the active circuits of the converter, namely the sampling switches, the comparator and the asynchronous logic circuit.

3.1 Sampling switches

The proposed converter adopts the top-plate sampling, which allows to resolve the first bit without redistributing any charge, thus saving energy and area. The differential input signal is directly sampled on the top of the two main-DACs by means of two bootstrapped switches [22], implemented as NMOS transistors. Their size has been chosen considering that, to achieve an accuracy of N bits and a settling error less than 0.5 LSB, the 3-dB frequency of a sampled circuit has to satisfy the following constraint [23]:

$$f_{3dB} = \frac{1}{2\pi R_{on} C_s} > \frac{(N+1)\,ln2}{\pi} f_s, \tag{7}$$

where R_{on} is the on-resistance of the switch, C_s=32 pF the sampling capacitance and f_s the sampling frequency. For the targeted 100 kSps sampling rate, a size of 3 μm/0.35 μm assures an on-resistance of 1.5 kΩ and a safety margin of 10 on the cut-off frequency. The small size of the switches, together with the large sampling capacitance and the large threshold voltage of the devices (600 mV), allows to greatly reduce two main sources of non-linearity due to top-plate sampling, i.e., the charge-injection that occurs at the end of the sampling phase and the signal-feedthrough during the conversion phase, being both signal-dependent. Simulations performed with an ideal converter

(capacitive arrays with no mismatch and no parasitic capacitances, and ideal comparator) yield an SNDR larger than 98 dB, corresponding to a resolution of 16 bits.

3.2 Comparator

A two-stage comparator, shown in Fig. 11, has been adopted in the proposed converter. It consists of a static preamplifier followed by a differential latch. Since the common-mode input voltage varies between $3V_{DD}/4$ and $V_{DD}/2$ with the proposed switching algorithm, the preamplifier features an NMOS differential pair. This is an advantage with respect to adopt the traditional monotonic switching algorithm, which implies the use of PMOS transistors at the comparator input. In fact, for the same bias current and input transconductance (thus also the same thermal noise and bandwidth), the NMOS pair features a lower input capacitance with a reduced effect on the converter linearity, while flicker noise is not an issue due to the switching operation, as explained in the following.
The preamplifier features a mirrored topology to reduce the impedance at the drain of the differential pair transistors, thus mitigating the kickback noise. The gain of the amplifier is set to 30 by means of two 60-kΩ poly resistors (R_G in Fig. 11), while the bandwidth (BW) is tailored to about to 10 MHz accurately sizing the capacitive load. This value is high enough to assure the amplification of the input signal and to toggle the latch in less than 30 ns, even when the signal is as small as 0.1 LSB, without impairing the comparator noise and power performance.
The bias current of the preamplifier has been sized to keep the overall input referred noise of the comparator well below the quantization noise. Assuming that the comparator noise is mainly determined by the preamplifier because of its high gain, the equivalent input referred noise results

$$V_{n,in,rms} = \sqrt{\frac{8k_bT\gamma}{g_m}(1+\alpha)\frac{\pi}{2}BW}, \tag{8}$$

where g_m is the transconductance of the input transistors and α is a coefficient that takes into account the remaining noise contributions (current mirror, load transistors and output resistors). Biasing the input MOS transistors in moderate inversion, Eq. 8 would turn into

$$V_{n,in,rms} = \sqrt{\frac{8k_bTn^2U_T}{I_B}(1+\alpha)\frac{\pi}{2}BW}, \tag{9}$$

where I_B is the bias current of the preamplifier and $n \cong 1.5$ the sub-threshold slope coefficient. For $\alpha \approx 1$, in order to achieve an input-referred noise lower than LSB/5 (corresponding to about 44 μV), a minimum first stage bias current I_B of 30 μA is required. Its final value has been set to 40 μA to take a safety margin, resulting in an overall preamplifier current of 80μA. To save

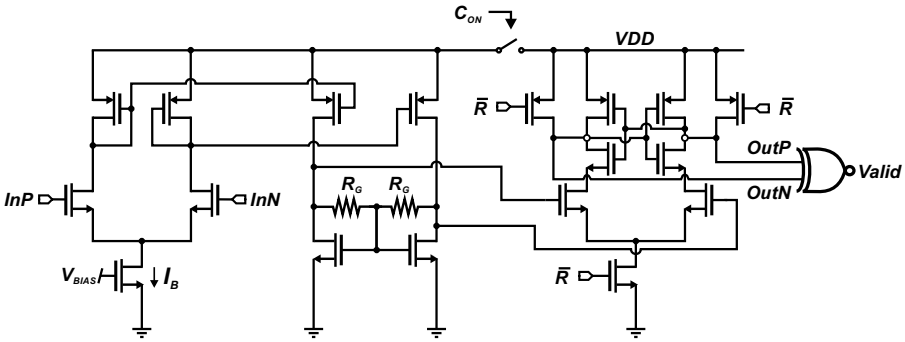

Fig. 11 Schematic of the two-stage comparator implemented cascading a preamplifier and a latch.

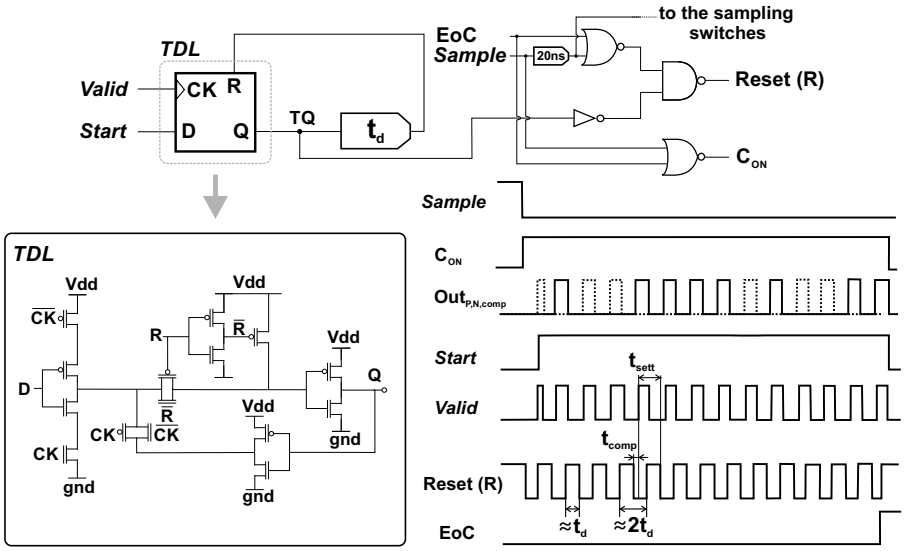

Fig. 12 Logic temporizer and time diagram.

power, the preamplifier operates in a power-switching regime being turned on only during the evaluation period of the 14 bits thanks to the control signal C_{ON} (see Fig. 11), corresponding to a duty cycle of 22.5% at 100 kSps. As additional effect, the power switching operation filters the flicker noise contribution up to approximately 500 kHz making its contribution negligible.

3.3 Asynchronous Logic

The SAR logic circuit generates the necessary commands to control the comparator and the capacitive DAC. In order to reduce its power consumption, an

asynchronous dynamic logic is adopted. By using a dynamic logic, less transistors are needed to implement the same function, while being asynchronous it requires only a low-speed sampling clock instead of an oversampled clock, thereby saving power. The core of this circuit is a logic temporizer (see Fig. 12), implemented using a dynamic latch (TDL) with a delayed feedback loop. Its function is to switch on the preamplifier, enable the comparator, wait for its decision and then reset it for a time large enough to assure the settling of the DAC voltage.
At the end of the sampling phase, i.e., at the falling edge of the *Sample* signal, the comparator is turned on (C_{ON}=1), starting the evaluation of the Most Significant Bit (MSB). It also enables the temporizer through the *Valid* signal (see Fig. 11), which marks the end of each successful comparison and acts as a clock for the TDL. However, only when the bottom plates of the MSB capacitors are completely switched after the first comparison, a *Start* signal (see Fig. 1) is pulled high till the end of the conversion phase, effectively starting the feedback mechanism that allows the reset and comparison phase to alternate. In fact, its rising edge triggers the first transition of the TDL output (TQ), causing the reset of the comparator latch (*Reset*=1) for a time $t_d \cong 90$ ns fixed by the delay unit (t_d in Fig. 12) and forcing *Valid* to zero. At the end of the reset phase, the comparator evaluates the MSB-1 bit and sets high the $Valid$ signal. However, the comparator is not reset till the falling edge of TQ has completed the feedback path, i.e., after a time t_d. Thus, *Reset* resembles a square wave with a period of $2t_d$. Since the comparator takes approximately $t_c \cong 30$ ns for a decision, a time of t_{sett}=$2t_d$-$t_{comp} \cong 150$ ns is left to the logic circuit and to the array to switch and settle, respectively, during the evaluation phase of each bit. When also the Least Significant Bit (LSB) has been evaluated, the End of Conversion (EoC) rises, the comparator preamplifier is turned off (C_{ON}=0), and the comparator latch is reset till the next sampling phase.

4 Measurement results

The ADC has been implemented using a 2P4M 0.35-μm CMOS technology adopting the aforementioned MiPiP "sandwich" capacitors of about 250 fF, corresponding to a sampling capacitance of approximately 64 pF (32 pF each array). The converter measures 1.35 mm^2, as shown in Fig. 13. The performance of the ADC have been measured at 1.8-V supply for 5 samples and compared to a second SAR converter (named test-ADC and shown in Fig. 14) implemented in the same CMOS process, with the same logic circuit and comparator but without optimized capacitive array and attenuation capacitance calibration.

4.1 Static performance

The static performance of the proposed converter are depicted in Fig. 15, which reports both DNL and INL as functions of the output code with and without the parasitics compensation. Due to the large parasitic capacitance at the comparator input (about 1.2 pF mainly due to the ground shield), the differential input range of the converter is about 3.4 V, instead of 3.6 V. Before foreground calibration, the DNL shows periodic peaks every 128 codes approximately equal to 9 LSB, very close to the simulated value (see Fig. 8). Consequently, the INL features a periodic pattern ranging from -18 to +18 LSB. Once the calibration is applied, the DNL and the INL range between -1/+1 LSB and-2.6/+2.1 LSB, respectively. The improved static performance before and after calibration of the attenuation capacitances demonstrate the validity of the proposed foreground calibration technique.

4.2 Dynamic performance

Fig. 16 shows the measured output spectrum for a low-frequency (a) and a close-to-Nyquist frequency (b) input sinewave at 100-kSps sampling rate with calibration enabled. The output spectrum at low-frequency before calibration is also shown in Fig. 16(a). Without calibration, the SFDR and SNDR are 72.2 and 55.64 dB, respectively. The corresponding ENoB is 8.95, limited by the spurious tones due to the DNL periodical pattern [24]. Enabling the calibration, the SFDR and SNDR are greatly improved, being 81.8 and 70.65 dB, respectively, corresponding to an ENoB of 11.45 for a low frequency input signal. Close to Nyquist frequency the SNDR is slightly reduced, being 68.1 dB, equivalent to an ENoB of 11.02.

4.3 Power consumption

The power consumption as function of the sampling rate is shown in Fig. 17. At 100-kSps sampling rate, the ADC draws an average current of 24.1 μA from the 1.8-V supply, resulting in a power consumption of 43.4 μW. According to post-layout simulations, most of the power is due to the comparator (75%), while DAC and SAR logic circuit account for 19% and 6%, respectively, of the overall power. The leakage current measured at 1.8-V supply is about 15 nA, thus becoming significant only at low sampling rates (less than 100 Sps) .

4.4 Test-ADC

A test-ADC has been implemented to assess the efficiency of the proposed techniques aiming to improve the linearity of the converter. The test-ADC adopts standard PiP capacitors available in the design-kit with approximately

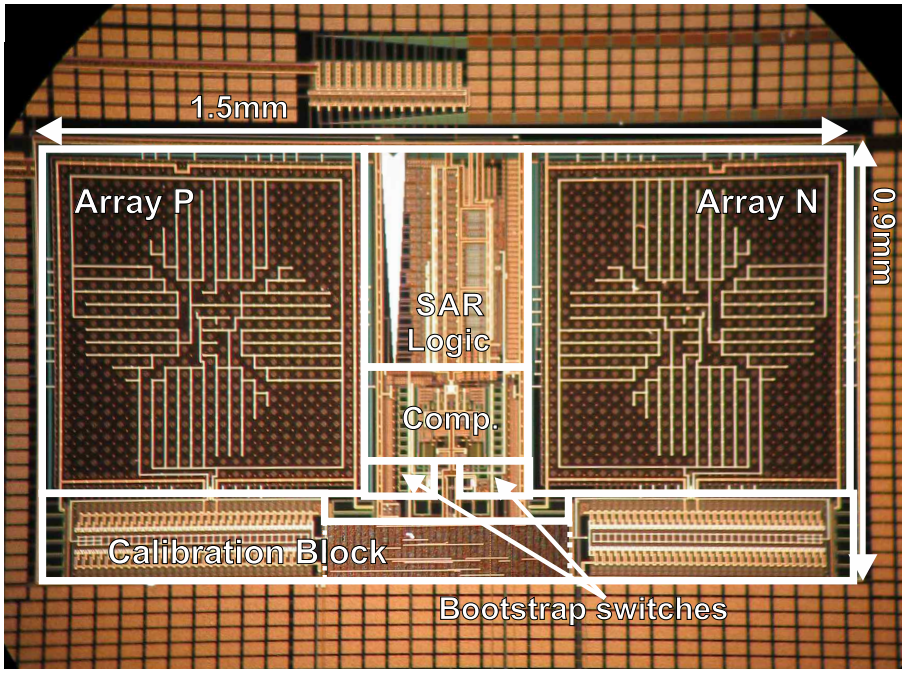

Fig. 13 Die photo of the proposed ADC.

the same value for the unit capacitance ($\cong 250\,\text{fF}$), thus expecting to have approximately the same linearity due to statistical mismatch. However, its array layout (see Fig. 14) is not optimized to be immune to oxide radial gradients. It has been designed to be rather insensitive to linear horizontal oxide gradients, while the vertical dimension has been kept small to reduce the effect of a vertical linear gradients. Moreover, the wiring parasitics were carefully tailored according to the extraction tool not to affect the converter linearity. This was accomplished thanks to a bank of *ad-hoc* parasitic capacitances, as shown in Fig. 14. Finally, the attenuation capacitor was sized to balance the parasitic capacitance of the sub-DAC [18], but without any calibration algorithm implementing a feedback control. This resulted in a simulated peak DNL (without mismatch contribution) of about 0.1 LSB.

Fig. 18 shows the measured INL of the test-ADC. It ranges between -32 and 31 LSB, corresponding to an SNDR of 44 dB and an ENoB of about 7. This poor linearity performance can be ascribed to the effect of an oxide radial gradient, as the one shown in Fig. 3, in the two differential arrays. In particular, the reconstructed INL curve in Fig. 18 (red line) is obtained assuming maximum variation of the oxide thickness of 20 % from the border to the center of the array in both vertical and horizontal direction. This results in a non-perfect compensation of the parasitic capacitance and in an increase of C_{13} and C_{12}, i.e., the capacitances corresponding to the MSB and MSB-1, with respect to

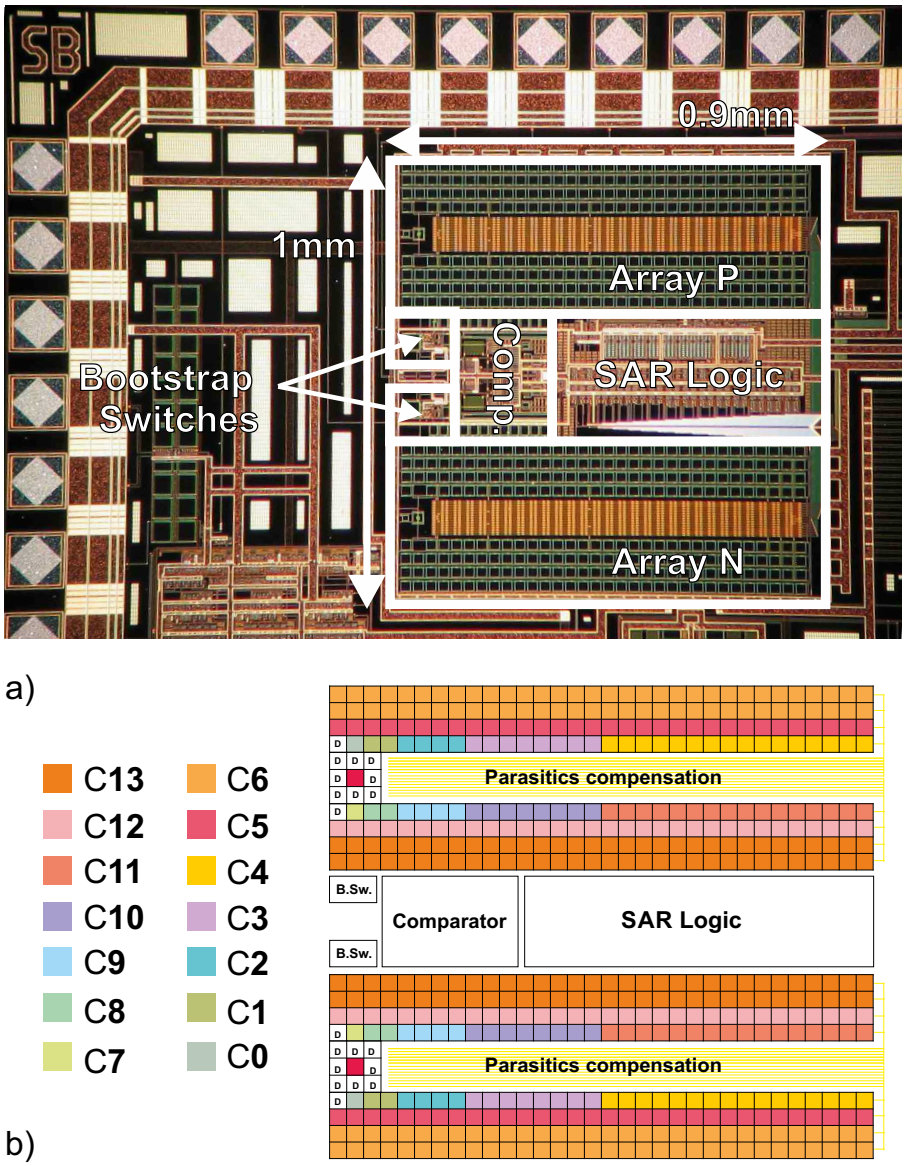

Fig. 14 Die photo of the test-ADC (a) and corresponding layout scheme of the capacitive arrays (b).

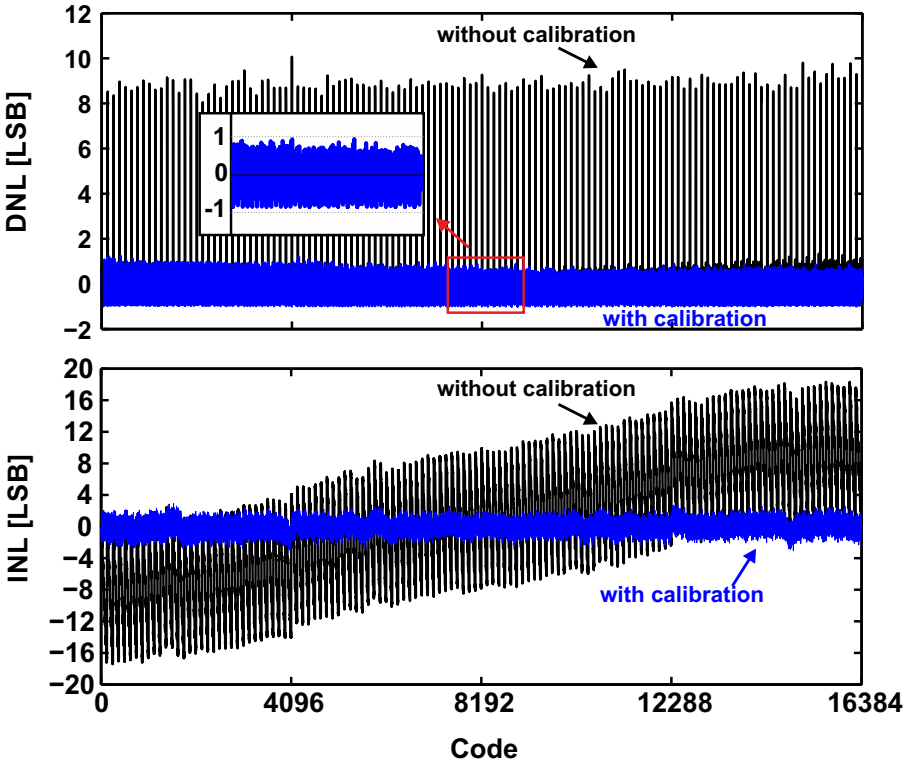

Fig. 15 Measured DNL and INL with and without calibration of the attenuation capacitance.

the nominal value. This explains the periodic behavior every 2^7=128 codes, and the large hops corresponding to the codes 2^{13} and 2^{12}.

4.5 Performance summary and comparison with state-of-the-art SAR converters

The performance of the implemented converter are summarized in Table 1 and compared with recent state-of-the art SAR ADCs featuring an SNDR larger than 70 dB. The proposed converter shows an efficiency in-line with the other high-resolution converters. However, this is the only converter that relies on an optimized array layout and a custom design of the unit capacitance to mitigate the effect of the capacitive mismatch and parasitics without resorting to complex calibration scheme, oversampling, dithering or a combination of these techniques. For example, the converter in [7] adopts a sub-radix-2 array design with a perturbation-based least-mean-squares (LMS) calibration and a non-subtractive dithering to achieve 13.5-bit resolution. In [10], noise-shaped-uniform dithering is proposed to improve the converter SNR, together with

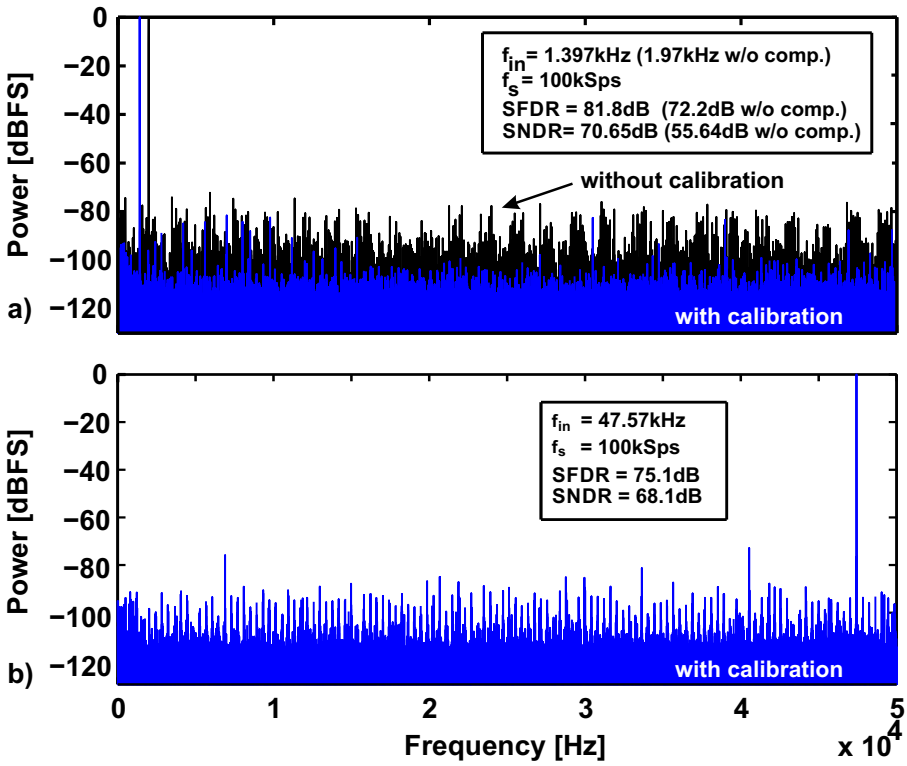

Fig. 16 Measured spectrum at 100-kSps sampling frequency with and without calibration for an input sine-wave at low-frequency (a) and close to Nyquist (b).

Table 1 Comparison with the-state-of-the-art medium-to-high resolution SAR converters

	[10]	[26]	[8]	[11]	[27]	[7]	this work
Res. (bit)	14	13	14	14†	14	14	14
Tech. (nm)	130	90	65	350 HV	65	130	350
Sampling Rate (MSps)	40	50	80	0.25	0.128	0.072	0.1
Power (μW)	66000	4200	31100	4.29	1.37	130	43.4
Supply (V)	1.5	1.2	1.2	3.3	0.8	1.2	1.8
Peak ENoB (bit)	13.5	11.5	11.6	13	12.8	13.5	11.45
Peak SNDR (dB)	83	71	71.6	82	78.81	83	70.7
Peak SFDR (dB)	-	84	88.6	97.8	87.1	96.8	81.2
Area (mm^2)	0.55	0.1	0.55	0.98	0.18	0.42	1.35
Capacitors	-	-	MoM	PiP	MoM	MiM	MiPiP
FoM (fJ/conv.step)	143	28.7	125	2050	5.4	156	155

† Two-step SAR architecture with 8-bit physical resolution DAC

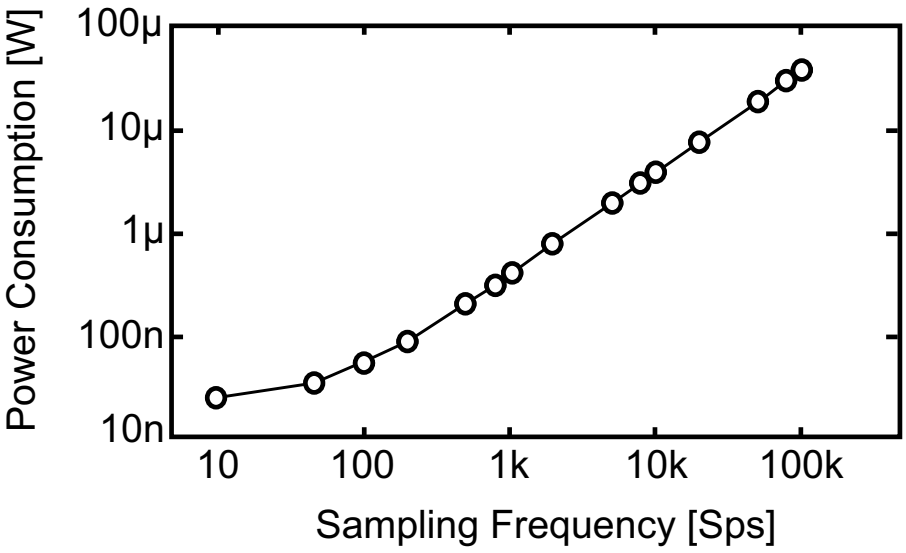

Fig. 17 Power consumption of the proposed ADC as function of the sampling frequency.

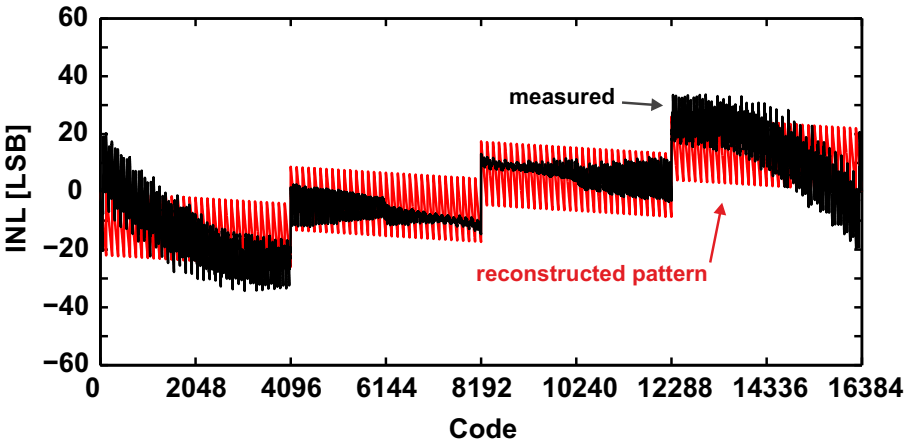

Fig. 18 Measured INL of the test-ADC. The red curve refers to the estimate once a radial gradient is supposed to affect the array capacitances.

multiple LSB decisions to enhance the noise performance of DAC and comparator. Finally, the outstanding result in [6] (12.8 ENoB, 5.4 fJ/conv.step) is obtained performing dynamically multiple comparisons for majority voting, combining oversampling and dithering, as well as exploiting chopping to cancel out comparator noise.

Fig. 19 compares the efficiency performance of the SAR converters published in the last 15 years at IEEE International Solid State Circuits Conference (ISSCC) and VLSI Circuits Symposium [25]. The proposed ADC shows the

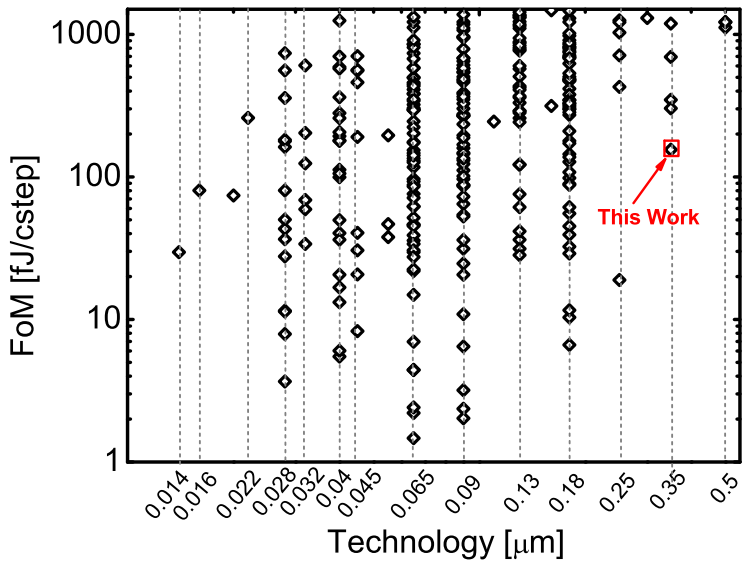

Fig. 19 Efficiency performance of the proposed ADC vs. technology among the state-of-the-art converters published in the last 15 years at the IEEE ISSCC and VLSI Circuits Symposium [25].

best FoM among converters implemented in 0.35-μm CMOS or less scaled technology.

5 Conclusions

This paper presents a high efficiency fully-differential SAR ADC in 350-nm CMOS technology adopting binary-weighted with attenuation capacitor arrays to limit the wiring complexity. The capacitive DACs exploit a semi-custom unit capacitance with a ground shield to avoid the effect of the parasitics on the converter linearity and are designed to be immune to linear and radial oxide gradients, which are a typical source of mismatch. Moreover, a calibration algorithm reduces the effect of the sub-DAC parasitics acting on the value of the attenuation capacitance. The converter features an SNDR of 70.7 dB, corresponding to a resolution of 11.45 bits, at 100-kSps with a power consumption of 43.4μW, resulting in an energy per conversion step of 155 fJ. This figure-of-merit makes the proposed converter the most efficient among SAR ADCs implemented in 0.35-μm or less scaled technology. Measurements performed on a test-ADC, where the capacitive array is implemented without custom unit elements, optimized layout and calibration technique, further demonstrate the effectiveness of the solutions adopted to improve the converter linearity. The

measured performance make the proposed ADC compatible with biomedical applications, 3-axis magnetic field sensing systems and most of the MEMS inertial sensors for consumer electronics [28].

Acknowledgment

This work was supported by the European Community through the European Nanoelectronics Initiative Advisory Council Nanoelectronics Framework Programme under Grant Lab4MEMS 325622-2. The authors would like to thank Dr. Luca Bettini for fruitful discussions.

References

1. S. Brenna, L. Bettini, A. Bonetti, A. Bonfanti, and A.L. Lacaita, Fundamental Power Limits of SAR and $\Delta\Sigma$ Analog-to-Digital Converters, *Proceedings of IEEE Nordic Circuits and Systems Conference (NORCAS)*, Oct. 2015, pp. 1–4.
2. S. Brenna, P. Minotti, A. Bonfanti, G. Laghi, G. Langfelder, A. Longoni, and A.L. Lacaita, A low-noise sub-500μW lorentz force based integrated magnetic field sensing system, *IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 932–935, Jan. 2015.
3. A. Bonfanti, M. Ceravolo, G. Zambra, R. Gusmeroli, T. Borghi, A.S. Spinelli, and A.L. Lacaita, A multi-channel low-power IC for neural spike recording with data compression and narrowband 400-MHz MC-FSK wireless transmission, *Proceedings of European Solid-State Circuits Conference (ESSCIRC)*, pp. 330–333, Sep. 2010.
4. M.S. Chae, W. Liu, Z. Yang, T. Chen, J. Kim, M. Sivaprakasam, and M. Yuce, A 128-Channel 6mW Wireless Neural Recording IC with On-the-Fly Spike Sorting and UWB Transmitter, *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp.146–148, Feb. 2008.
5. S. Brenna, A. Bonfanti, and A.L. Lacaita, A 6-fJ/Conversion-Step 200-kSps Asynchronous SAR ADC with Attenuation Capacitor in 130-nm CMOS, *Analog Integrated Circuits and Signal Processing*, vol. 81, 2014, pp. 181–194.
6. P. Harpe, C. Zhou, B. Yu, N.P. van der Meijs, W. Xiaoyan, K. Philips, G. Dolmans, and H. de Groot, A 26μW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios, *IEEE Journal of Solid State Circuits*, vol. 46, no. 7, pp. 1585–1595, July 2012.
7. S. Fateh, P. Schonle, L. Bettini, G. Rovere, L. Benini, and Q. Huang, A Reconfigurable 5-to-14 bit SAR ADC for Battery Powered Medical Instrumentation, *IEEE Transaction on Circuits and Systems I: Regular Paper*, vol. 62, no. 11, pp. 2685–2694, Nov. 2015.
8. R. Kapusta, J. Shen, S. Decker, H. Li, E. Ibaragi, and H. Zhu, A 14 b 80MS/s SAR ADC with 73.6dB SNDR in 65nm CMOS, *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 3059–3059, Feb. 2013.
9. S. Thirunakkarasu and B. Bakkaloglu, Built-in Self-Calibration and Digital-Trim Technique for 14-Bit SAR ADCs Achieving 1 LSB INL, *IEEE Transaction on VLSI systems*, vol. 23, no. 5, pp. 916–925, May. 2015.
10. M. Hesener, T. Heichler, A. Hanneberg, D. Herbison, F. Kuttner, and H. Wenske, A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13μm CMOS, *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2007, pp. 248–600.
11. I. Ozkaya, C. Gurleyuk, A. Ergul, A. Akkaya, and D.Y. Aksim, A 50 V Input Range 14bit 250kS/s ADC with 97.8dB SFDR and 80.2dB SNR, *Proceedings of European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2014, pp.71–74.
12. A. Abusleme, A. Dragone, G. Haller and B. Murmann, Mismatch of lateral field metal-oxide-metal capacitors in 180nm CMOS process, *IEEE Electronic Letters*, vol. 48, pp. 286–287, Mar. 2012.

13. B. Murmann, Energy Limits in A/D Converters, *Proceedings of the IEEE Tension Faible Consommation*, pp. 1–4, June 2013.
14. C.C. Liu, S.J. Chang, G.Y. Huang, and Y.Z. Lin, A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure, *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.
15. M. Saberi, R. Lotfi, K. Mafinezhad, and W. Serdjin, Analysis of Power Consumption and Linearity in Capacitive Digital-to-Analog Converters used in Successive Approximation ADCs, *IEEE Transaction on Circuits and Systems I: Regular Paper*, vol. 58, no. 7, Aug. 2011, pp. 1736–1747.
16. M.J.M. Pelgrom, A.C.J. Duinmaijer , and A.P.G. Welbers, Matching Properties of MOS Transistors, *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, June 1989.
17. S. Haenzsche, S. Henker, and R. Shcuffny, Modeling of capacitor mismatch and non-linearity effects in charge redistribution SAR ADC, *Proceedings of the IEEE Mixed Design of Integrated Circuits and Systems (MIXDES)*, pp. 300–305, June 2010.
18. Si-Seng Wong, Yan Zhu, Sai-Seng Sin, Seng-Pan U, and Rui Paulo Martins, A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC, *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1783–1794, Aug. 2013.
19. W. S. Liew, X. Zou, and Y. Lian, Split Capacitor DAC Mismatch in Successive Approximation ADC, *Proceedings of IEEE Custom Integrated Circuits Conference (CICC)*, pp. 279-282, Sept. 2009.
20. M. Yoshioka, K. Ishikawa, and S. Tsukamoto, A 10b 50MS/s 820μW SAR ADC with on-chip Digital Calibration, *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2010, pp. 384–386.
21. S. Brenna, A. Bonetti, A. Bonfanti, and A.L. Lacaita, A tool for the assisted design of charge redistribution SAR ADC, *Proceedings of Design, Automation and Test in Europe Conference (DATE)*, Mar. 2015, pp. 1265-1268.
22. A. Shikata, R. Sekimoto, and H. Ishikuro, A 0.5V 65nm-CMOS single phase clocked bootstrapped switch with rise time accelerator, *Proceedings of the IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS)*, 2010, pp. 1015–1018.
23. D. Zhang, A. Bhide, and A. Alvandpour, A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13 m CMOS for medical implant devices, *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1585–1593, July 2012.
24. A. Abidi and H. Pan, Spectral Spurs Due to Quantization in Nyquist ADCs, *IEEE Transaction on Circuits and Systems I: Regular Paper*, vol. 51, no. 8, Aug. 2004, pp. 1422–1439.
25. B. Murmann, ADC Performance Survey 1997-2015, Online - web.stanford.edu, 2015, *http://web.stanford.edu/∼murmann/adcsurvey.htm*.
26. T. Morie, T. Miki, K. Matsukawa, Y. Bando, T. Okumoto, K. Obata, S. Sakiyama, and S. Dosho, A 71 dB-SNDR 50 MS/s 4.2mW CMOS SAR ADC by SNR enhacement techniques utilizing noise, *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2013, pp. 272–273.
27. P. Harpe, E. Cantatore and A.V. Roermund, An Oversampled 12/14b SAR ADC with Noise Reduction and Linearity Enhancements achieving up to 79.1dB SNDR, *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2014, pp. 194–195.
28. S. Brenna, P. Minotti, A. Bonfanti, G. Laghi, G. Langfelder, A. Longoni, and A.L. Lacaita, A Sub-400-nT/sqrt(Hz), 775μW, Multi-Loop MEMS Magnetometer With Integrated Readout Electronics, *IEEE Journal of Microelectromechanical Systems*, vol. 24, Issue 6, pp. 1938–1950, Aug. 2015.