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REVIEW OF SCIENTIFIC INSTRUMENTS **86**, 113101 (2015)

Improving the counting efficiency in time-correlated single photon counting experiments by dead-time optimization

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Time-Correlated Single Photon Counting (TCSPC) has been long recognized as the most sensitive method for fluorescence lifetime measurements, but often requiring "long" data acquisition times. This drawback is related to the limited counting capability of the TCSPC technique, due to pile-up and counting loss effects. In recent years, multi-module TCSPC systems have been introduced to overcome this issue. Splitting the light into several detectors connected to independent TCSPC modules proportionally increases the counting capability. Of course, multi-module operation also increases the system cost and can cause space and power supply problems. In this paper, we propose an alternative approach based on a new detector and processing electronics designed to reduce the overall system dead time, thus enabling efficient photon collection at high excitation rate. We present a fast active quenching circuit for single-photon avalanche diodes which features a minimum dead time of 12.4 ns. We also introduce a new Time-to-Amplitude Converter (TAC) able to attain extra-short dead time thanks to the combination of a scalable array of monolithically integrated TACs and a sequential router. The fast TAC (F-TAC) makes it possible to operate the system towards the upper limit of detector count rate capability (~80 Mcps) with reduced pile-up losses, addressing one of the historic criticisms of TCSPC. Preliminary measurements on the F-TAC are presented and discussed. [http://dx.doi.org/10.1063/1.4934812]

I. INTRODUCTION

For many years, Time-Correlated Single Photon Counting (TCSPC) techniques have been playing a central role in a variety of applications characterized by a strong demand in terms of temporal resolution such as fluorescence lifetime spectroscopy and imaging, photon migration, optical time domain reflectometry, and time of flight measurements.[1] TCSPC techniques provide a much better timing resolution compared to the one attainable with analog techniques.[1] However, the main drawback of TCSPC is that the experiment must be repeated many times until the desired number of photons, which depends on the application, is recorded. Thus, the main limitation is the time needed to perform a complete measurement, which is a key parameter in applications like fluorescence lifetime imaging (FLIM) microscopy[2,3] and diffuse optical tomography.[4] In order to overcome this limit, many instruments able to manage a higher and higher count rate have been designed. Nevertheless, there are two fundamental limitations to the maximum achievable count rate: classic pile-up and counting loss.

Classic pile-up results from the fact that a single TCSPC device can record only one photon per excitation pulse: if two photons arrive in the same period, the second one will always be neglected. If the probability of having two photons per period is not negligible, the recorded histogram will be distorted. The power of the incident light and consequently the mean number of photons per excitation period can be set depending on the distortion that can be tolerated. Alternatively, one can increase the laser pulse frequency without changing its average output power, thus reducing the mean number of photons per excitation period. Pile-up is negligible for a count rate of 1% of the laser pulse frequency and remains tolerable up to a count rate of 5% of the laser pulse frequency. For the lasers currently used in lifetime spectroscopy, the pulse frequency is 80–90 MHz, corresponding to a pile-up limited count rate of 4 Mcps–5 Mcps.[1]

Counting loss is caused by the dead time of detector and TCSPC electronics. A detector registering a photon is unable to detect further photons for a dead time. Similarly, the signal processing of a recorded photon generates a dead time during which the TCSPC electronics is unable to process any further photon event. In current systems, the dead time of the TCSPC electronics is larger than that of the detector, being therefore the dominant contribution to the counting loss. As long as the photon detection rate is small compared to the reciprocal dead time of the TCSPC module, the counting efficiency, i.e., the ratio of the recorded count rate to the detector count rate,[1] is close to 100%. The recorded count rate at an efficiency of 50% is conventionally defined as the "maximum useful count rate."[1] For the fastest TCSPC modules, the dead time is about 100 ns, corresponding to a maximum useful count rate of 5 Mcps. An efficient yet expensive way to reduce pile-up distortion and counting loss is the multi-module technique.[1] In a multi-module system, the photons from several detectors are processed in parallel. Therefore, pile-up and counting loss are reduced in proportion to the number of TCSPC channels.[1] Of course, multi-module operation also increases the system cost and can cause space and power supply problems.

In this paper, we propose an alternative approach based on a new detector and processing electronics designed to reduce the overall system dead time, thus enabling efficient photon

collection at high excitation rate. In Sec. II, we will briefly discuss the impact of dead time on count rate and counting efficiency and its potential implications in TCSPC experiments based on single-beam and multi-beam optical excitation systems. In Sec. III, we will present a fast Active Quenching Circuit (AQC) designed to operate Single-Photon Avalanche Diodes (SPADs) with a minimum dead time of 12.4 ns, thus allowing saturated count rates up to about 80 Mcps. Sec. IV will then illustrate the structure of a new Time-to-Amplitude Converter (TAC) able to attain extra-short dead time, thanks to the combination of a scalable array of monolithically integrated TACs and a sequential router. Preliminary experimental results obtained with a prototype fast TAC (F-TAC) will be presented in Sec. V. We demonstrate that the F-TAC makes it possible to operate the system towards the upper limit of detector count rate capability, while maintaining good timing resolution and differential non-linearity (DNL) performance. Conclusions are drawn in Sec. VI.

II. IMPACT OF DEAD TIME ON COUNTING EFFICIENCY AND COUNT RATE

In conventional TCSPC instruments, the timing signals are processed by a TAC followed by an Analog to Digital Converter (ADC), which provides digital values used to assign photon counts to the corresponding histogram bins. Alternatively the tasks performed by TAC and ADC can be carried out by a single fully digital circuit, a so called Time-to-Digital Converter (TDC). TACs and TDCs largely set the dead time of TCSPC instruments, which is typically of the order of 100–400 ns.[1] From now on, we will consider only TACs as the timing electronics, although the same conclusions hold for TDC-based systems.

When using high-repetition-rate excitation sources, the TAC is typically operated in the "reversed" start-stop mode, i.e., it is started using the signal from the detector and stopped by the correlated signal from the excitation source. In this way, the TAC is only triggered by usable events, and not by laser trigger pulses that do not result in a detected photon. Therefore, this mode of operation suffers less from dead-time effects.

We consider here a real case scenario where the TAC is the rate-limiting component in the TCSPC system, being its dead time t_d much longer than that of the detector. Each recorded photon causes a dead time t_d. It must be noted that the dead time in typical TAC device is "non-paralyzable," i.e., a photon lost in the dead time of a previous one does not cause new dead time.[1] Under this condition, the TCSPC electronics is losing on average $r_{det} \times t_d$ photons during each conversion, where r_{det} is the average photon detection rate (detector count rate).

Thus, the average number of photons lost during the experiment is

$$N_{lost} = r_{rec} \times T \times r_{det} \times t_d, \tag{1}$$

where r_{rec} is the average rate at which photons are recorded (recorded count rate) and T is the measurement time. The counting efficiency can be defined as

$$\eta = 1 - \frac{N_{lost}}{N_{det}} = 1 - r_{rec} \times t_d, \tag{2}$$

where N_{det} is the average number of detected photons over the measurement time T.

Rearranging Eqs. (1) and (2), we obtain

$$r_{rec} = \frac{r_{det}}{1 + r_{det} \times t_d}. \tag{3}$$

Eqs. (2) and (3) apply with satisfactory accuracy to reversed start-stop measurements at high pulse repetition rate.[1] Although these equations have been derived considering the TAC as the rate-limiting component in the TCSPC system, they are still valid if the opposite scenario is considered, that is, when the detector has a longer dead time compared to that of the TAC, thus being the rate-limiting component.

Figure 1 illustrates the counting efficiency as a function of dead time for a constant recorded count rate (see Eq. (2)). This relationship would typically apply to single-beam/single-detector applications, where the user can set the excitation power in order to get the desired recorded count rate. A reduction in the dead time causes the collection efficiency η to proportionally increase, the recorded count rate being the proportionality factor. In practice, by decreasing the TAC dead time, one can decrease the excitation power while keeping the same recorded count rate. This strategy would be effective in mitigating adverse effects such as photodamage,[5,6] which is a serious issue for *in vivo* experiments, or photobleaching of the fluorescent marker.[7,8]

Figure 2 reports the recorded count rate as a function of the dead time for a constant detector count rate (see Eq. (3)). This relationship would apply to situations where either photodamage, photobleaching or limited excitation power budget sets the maximum detector count rate to around 10^6 counts per second. The latter case might be encountered in multifocal FLIM of bright samples.[9–11] The ultrafast excitation sources most commonly used in single and multiphoton microscopy typically provide an average output power that is far more than should be applied in conventional single-beam microscopy.

One way to make use of the excess is to utilize multiple excitation foci[12–14] and perform parallel analysis of the fluorescent emission using a detector array. If a multifocal

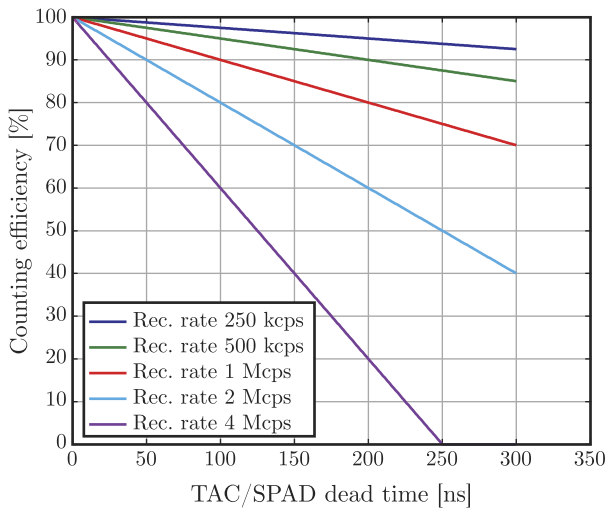

FIG. 1. Counting efficiency of a TCSPC system as a function of dead time for a constant recorded count rate.

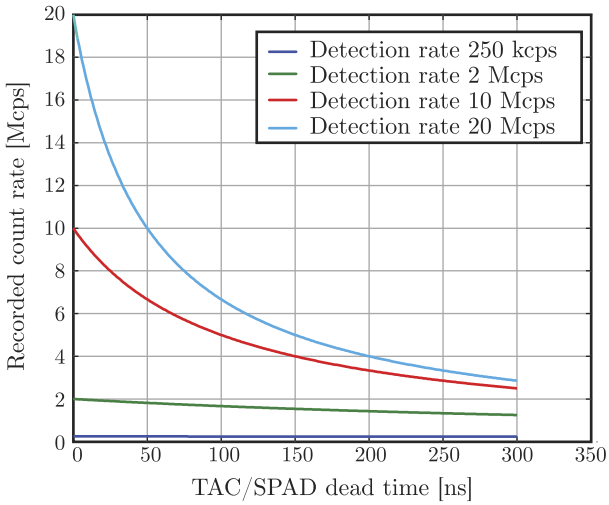

FIG. 2. Recorded count rate of a TCSPC system as a function of dead time for a constant detection rate.

microscope utilizes n beams each with the same average power as employed in a single beam system, then the total measurement time is decreased by a factor of n. According to Figure 2, a further improvement might be achieved in these systems by reducing the TAC dead time while keeping the same excitation power (i.e., the same detector count rate), thus leading to a higher recorded count rate and, in turn, to a lower measurement time.

It can be noticed that a real advantage in reducing the dead time is achieved at high detector count rates (i.e., $r_{det} \times t_d > 1$), when the curves shown in Figure 2 approach a $1/t_d$ law.

In order to better understand the above arguments, we can make two numerical examples. For the first scenario, we can assume that the user targets a recorded count rate of 4 Mcps. A TAC with a dead time in the order of 100 ns would provide a counting efficiency of about 60% (Eq. (2)). With a detector dead time equal to 12.4 ns and a TAC with negligible dead time (see Section IV), the efficiency would increase up to 95%, thus leading to the same recorded count rate while the power of the excitation source is decreased by a factor 1.6.

For the second scenario, we can consider a detector count rate of 4 Mcps and a TAC dead time of 100 ns. In this condition, the recorded count rate obtained from Eq. (3) is 2.86 MHz (71% of efficiency). Considering the low dead time detector and electronics as previously done, the recorded count rate could be increased up to 3.8 MHz (95% of efficiency), decreasing the measurement time by a factor of about 1.3.

III. FAST ACTIVE QUENCHING CIRCUIT

TCSPC techniques have been introduced and developed over four decades relying on photomultiplier tubes (PMTs), that is, vacuum tube devices. In more recent years, SPADs[15,16] have emerged as a solid state alternative to PMTs. Besides the well known advantages of solid state versus vacuum tube devices (small size, ruggedness, low power dissipation, low supply voltage, high reliability, etc.), SPADs provide inherently higher quantum efficiency, particularly in the red and near infrared spectral regions.

In order to exploit the intrinsic performance of SPAD devices, it is necessary to operate them in accurately controlled conditions, with short dead time.[15] To this purpose, an AQC is associated to the detector to (i) sense the onset of the avalanche current, (ii) force the bias voltage of the diode to drop below the breakdown voltage (active quenching) and, (iii) restore the initial bias after a well-controlled hold-off time (active reset) so that the diode is ready to detect a subsequent photon. The AQC generates a non-paralyzable, short, and well-defined dead time after each avalanche pulse, during which the detector is insensitive to absorbed photons.

A first step toward the increase of the conversion efficiency of a TCSPC system was to maximize the detector count rate capability. To this end, we completely revised the design of an integrated AQC (iAQC) previously developed by our group,[17,18] in order to reduce dead time to the least possible value. Nowadays, many AQC have been presented in the literature with even shorter dead times.[19–21] In all these solutions, both detector and quenching circuit are realized in CMOS technology and integrated on the same chip, therefore significantly decreasing the capacitance of the switching node of the SPAD. Our AQC is designed to work in conjunction with custom technology SPAD[16] which features better performance although being realized on a different chip. The increased performance of the proposed quenching circuit, with respect to those of the previous versions,[17] is mainly due to a better fabrication technology (0.18 μm CMOS instead of 0.8 μm CMOS) along with a careful optimization of the delays. In previous versions, the main goal was to keep the number of transistors as low as possible and so there was a trade-off between area occupation and performance.

Figure 3 shows the simplified block diagram of the optimized iAQC, derived from the structure reported in Ref. 17.

We manufactured different chips including either a single iAQC, to work in conjunction with an individual SPAD detector, or an array of up to 32 iAQCs able to operate several detectors in parallel, while reducing the overall space occupation.

The iAQC is directly connected to the cathode pin of the detector, which swings between VDD_{AQC} and GND_{AQC} during quench and reset operations. Depending on the application, those two voltages can have a difference of tens of volts and for that reason a high-voltage CMOS technology has been used (0.18 μm HV-CMOS by Austriamicrosystems), allowing to exploit nMOS and pMOS transistors with 50 V of maximum

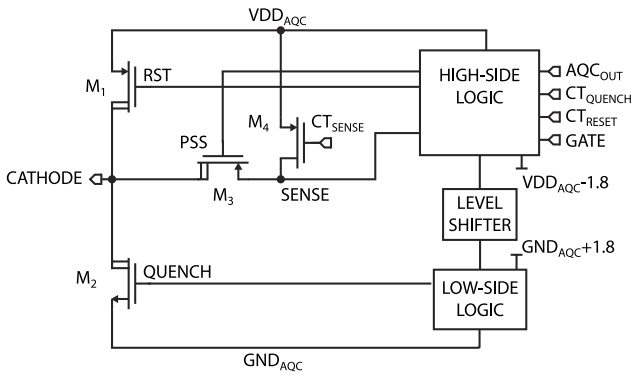

FIG. 3. Simplified block diagram of the integrated active quenching circuit.

V_{DS} (drain-source voltage). In Figure 3, transistors M_1, M_2, and M_3 are high-voltage MOS.

The cathode is connected to VDD_{AQC} through the series of M_3 and M_4, whereas M_1 and M_2 are turned off while the SPAD is awaiting a photon. The value of the series resistance of M_4 can be changed by the user changing the CT_{SENSE} voltage. A higher sense resistance leads not only to a fast avalanche sensing but also to a higher sense voltage and so to a higher electrical crosstalk between adjacent AQCs in the same array.

When the avalanche current is sensed, the control logic asserts the quenching signal, M_3 is turned off in order not to dissipate power between the two voltage rails, and M_2 drives the cathode low. After the quenching phase, the reset starts, so M_2 is turned off and M_1 drives the cathode high. At the end of the reset phase, M_1 and M_2 are turned off and M_3 is turned on. The duration of both the quenching and the reset phases is controlled through delay lines and it can be adjusted by the user through the CT_{QUENCH} and CT_{RESET} voltages. The iAQC provides an external AQC_{OUT} pulse upon the avalanche current sensing, which can be used in photon counting applications. This circuit can be operated also in gated mode: when the external GATE signal is driven, high M_2 is turned on, keeping the SPAD device quenched. Since the high-voltage transistors support a maximum GATE voltage of 1.8 V, the control logic has been divided into a high-side logic and a low-side logic separated by a voltage translator made up of high-voltage nMOS transistors.

Figure 4 shows a detail of the circuit that is used to control the duration of the quench and reset phases. The working principle is based on a RC transient: inverters are designed in order to have a not negligible load capacitance C_p, whereas the resistance is realized by means of MOS M_1 in pass-transistor configuration. The input signal is generated upon the sensing of an avalanche. The control signal (CT_{QUENCH} or CT_{RESET}) drives the gate of M_1, changing its series resistance and so the transient time. M_2 rapidly discharges the capacitance C_p after a falling edge of the input signal, resetting the delayer. The last inverters regenerate the signal edges.

Figure 5 shows the cathode voltage of the SPAD connected to the iAQC circuit. The CT_{QUENCH} and CT_{RESET} voltages have been chosen to obtain the minimum dead time, the SPAD has been kept in a dark environment, and the waveform has been acquired using the infinite persistence mode of the oscilloscope. As it can be noticed, the minimum distance between two subsequent pulses is 12.4 ns.

Since the quench phase duration strongly affects the afterpulsing probability, the latter was measured using the time-correlated carrier counting (TCCC) method,[22] at ambient temperature for a detector manufactured in custom technology,[23] changing the dead time from 300 ns to 12.4 ns. In these conditions, the probability changed from 0.8% to 2%. It is therefore possible to reduce the detector dead time without decreasing significantly the system performance.

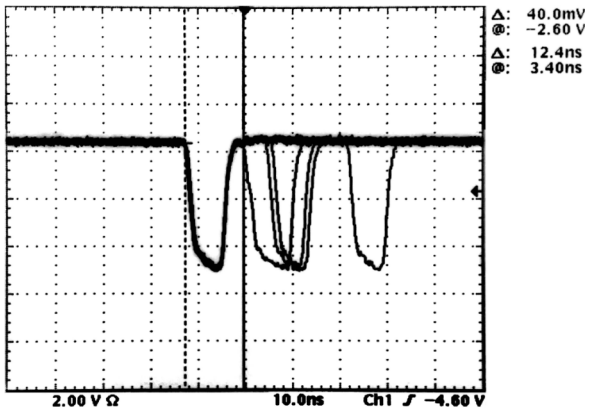

FIG. 5. Cathode voltage waveform obtained with the circuit of Fig. 3 by operating the SPAD detector at an average count rate of 10 kcps. A dead time of 12.4 ns is clearly observed. (Infinite persistence mode. Horizontal scale 10 ns/div; vertical scale 2 V/div.)

IV. FAST TAC STRUCTURE AND CALIBRATION

A. F-TAC structure

The second step toward the improvement of the conversion efficiency was to develop a TAC with a very short dead time, called F-TAC. It is worth noting that the dead time of a single converter cannot be shrunk indefinitely: to circumvent this limitation, we propose a solution based on "multiple" TAC exploitation. The idea of routing a signal coming from a single detector to multiple converters is known in the literature.[24]

The main idea of the F-TAC is presented in Figure 6. Several time-to-amplitude converters are put in parallel, sharing the same stop signal provided by the external sync source, e.g., the excitation laser. The circular shift register sequentially routes the start signal to the converters. The overall number of TACs is selected in such a way that each TAC element is addressed after having already performed the previous conversion. The maximum frequency of the start signal is the inverse ratio of the detector dead time, so the number of converters has to be chosen in order to manage such throughput. However, there are several aspects which have to be taken into account in order to properly exploit the idea of this fast TAC.

First of all, monolithically integrated time-to-amplitude converters with high performances are needed in order to make this idea feasible. Bulky TACs made up of discrete components cannot be highly parallelized in order to create a compact

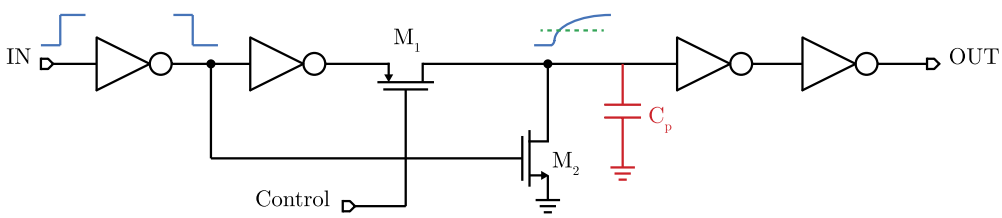

FIG. 4. Schematic of the circuit that is used to control the quench and reset duration.

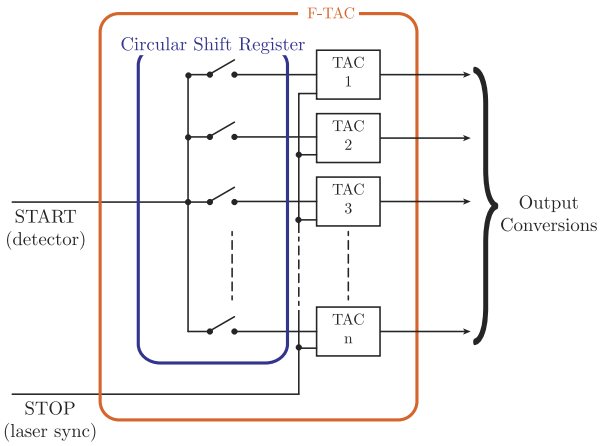

FIG. 6. Schematic block diagram of the F-TAC. A circular shift register is used to sequentially feed the start signal to the individual TAC converters. The overall TAC number n should be high enough to achieve a total dead time lower than that of the single photon detector.

system and the power dissipation would be an issue as well. An integrated array of four TACs with high performances and small area has been already designed by our group.[25] These converters have a total dead time of about 120 ns including the time needed by the Field Programmable Gate Array (FPGA) to sample the conversion of the ADC and to assert the reset signal (see Section V). At least ten of these TACs should be parallelized to build a F-TAC with an effective dead time shorter than that of the iAQC described in Sec. III.

A second concern arises from the fact that different time-to-amplitude converters, and accordingly different ADC channels, are used to record photons detected by the same detector. To address this issue, it is mandatory to calibrate differences among acquisition channels in order not to degrade the timing performance. In Subsection IV B, we will illustrate in detail the calibration algorithm that we developed in order to compensate for differences in the mean time bin-width and for offsets between channels.

B. F-TAC calibration

The start-stop delays measured with different acquisition channels have to be pooled together to obtain a single histogram. Therefore, it is mandatory to compensate all the mismatches between channels. There are two types of mismatch: mean bin-width and offset. The mean bin-width is given by the ratio of the full-scale range (FSR) of any individual TAC and the resolution of the subsequent ADC in channels. Since the full-scale range is inversely proportional to the conversion current,[25] small mismatches in the individual conversion currents result in TAC channels with mismatched time bin-width. Offset is due to the different paths that the signal follows, depending on which acquisition channel it has been routed to. A specific calibration algorithm has been developed for compensating both sources of mismatch. First of all, the mean bin-width of each individual channel has to be calculated. To this purpose, start and stop signals delayed by a fixed time interval, t_{d1}, are repeatedly fed to all channels, and the corresponding histograms made up of a single Gaussian peak are collected. The same procedure is then repeated setting a different time interval, t_{d2} between the two signals, in order to collect a second Gaussian peak in a different time position. The two fixed start-stop delays are selected such that the two resulting peaks in each acquisition channel are located close to the beginning and to the end of the full-scale range. The mean bin-width is then easily calculated for each channel as the ratio $(t_{d2}\text{-}t_{d1})$/#bins, where #bins is the distance between the two Gaussian peaks measured in number of bins.

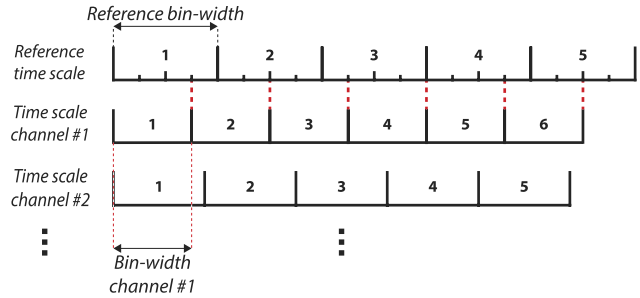

FIG. 7. Example of time scales of different selected channels. A reference bin-width slightly larger than the largest bin-width is set, defining a reference time scale.

Then, a discrete time scale having a bin-width slightly larger than the largest mean bin-width of the acquisition time scales is set, defining a reference time scale (see Fig. 7). The goal is to map each bin of the acquisition time scales into the corresponding bin in the reference time scale. In practice, each count occurred in a bin of any acquisition time scale must be properly assigned to the corresponding bin in the reference time scale. As a first step, a proper coefficient, called $A(n)$ *coefficient*, is calculated for each acquisition channel n (n = 1, 2, 3, ...) as the ratio between the mean bin-width of the acquisition time scale and the bin-width of the reference one.

For instance, let us consider the example reported in Figure 7, where the A coefficient for channel #1, $A(1)$ is 0.75. By definition, all counts occurring in bin #1 of channel #1 will be assigned to bin #1 of the reference time scale.

However, bin #2 of channel #1 is partially overlapped to bins #1 and #2 of the reference time scale. Namely, 66% of this bin falls in reference bin #2 and the remaining 34% falls in reference bin#1 (see Fig. 7). This means that counts occurring in bin #2 of channel #1 must be properly distributed amongst reference bins #1 and #2. The distribution is done according to the following procedure: the number of the bin where the count occurred is first multiplied by the factor $A(1)$. In our case, the result of the multiplication is $2 \cdot 0.75 = 1.5$, which can be split into an integer part, *int*, and a fractional part, *fra*. Then the fractional part is multiplied by the reciprocal of the $A(1)$ coefficient, which is called $C(1)$ *coefficient* (in this example, $0.5 \cdot C = 0.5 \cdot 1/0.75 = 0.66$). The obtained result represents the fraction of times, f, in which the occurring count has to be assigned to the reference bin #($int + 1$), whereas $(1 - f)$ is the fraction of times in which the occurring count has to be assigned to the reference bin #(int). The same procedure applies to each time bin of any acquisition channel.

Upon calculating coefficients $A(n)$ and $C(n)$ for all the TAC channels, the offset mismatches needs to be compensated. To this purpose, start and stop signals delayed by a fixed time interval are fed to the acquisition channels, but this time, the

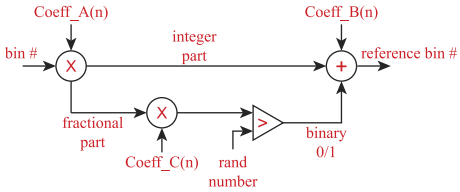

FIG. 8. Block diagram of the run time calibration firmware. A random number generator is used to determine the destination bin (see text for details).

calculated coefficients $A(n)$ and $C(n)$ are used to map the acquisition time bins into the reference time bins. Therefore, all the histograms are built on the reference time scale and they are made up of single Gaussian peaks. One acquisition channel is then chosen as reference, and the offset coefficient, $B(n)$, is calculated as the peak shift between the generic channel histogram and the reference channel histogram. Once the three sets of calibration coefficients $A(n)$, $B(n)$, and $C(n)$ are calculated and stored, mismatches between channels can be fully compensated using the run time calibration scheme reported in Figure 8.

To illustrate the operation of the run time calibration scheme, we can consider the counts occurring in bin #2 of channel #1. According to the above discussion, the reference bin for the occurred counts is bin #2 for the 66% of the times and bin #1 for the remaining times.

In order to determine the reference bin, a random number generator is exploited, whose output is uniformly distributed between 0 and 1. This number is then compared with the result of the multiplication between the fractional part and the $C(1)$ coefficient: if the random number is less than or equal to the multiplication result, the reference bin will be calculated by summing "1" to the integer part, otherwise it will be equal to the integer part. In the previous example, the random number is compared with 0.66, so 34% of the time will be higher than 0.66 and the reference bin will be #1. Eventually, the $B(1)$ coefficient is applied to account for the offset.

Preliminary results showing the efficacy of the presented calibration algorithm are shown in Section V.

V. PRELIMINARY EXPERIMENTAL RESULTS

A first prototype of the F-TAC was implemented by exploiting an 8-channel acquisition board,[26] previously developed in our lab. The board, whose schematic is reported in Figure 9, includes two four-channel integrated TAC chips whose outputs are fed to a commercial, eight-channel ADC (Analog Devices AD9252) featuring 14 bit resolution and a maximum conversion rate of 50 Msps. An onboard FPGA (Xilinx XC6SLX150T, Spartan-6 family) organizes the collected measurements and manages the F-TAC operations. Finally, a circular shift register made up of discrete components was added to the board in order to route the start signal to the converters.

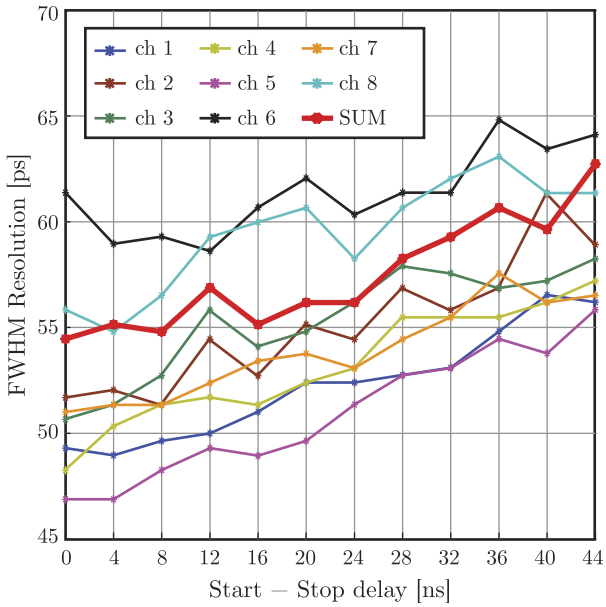

FIG. 10. Timing resolution of the eight individual timing channels compared with the one of the F-TACs, obtained by summing up the eight individual histograms.

We first tested the timing resolution of the F-TAC by using artificial signals. The output of a pulse generator was split into two signals: the first one was used as a start and the second one was used as a stop after having being delayed by means of a passive adjustable delayer. In this way, we fed the system with a fixed start-stop delay and negligible jitter.

The FWHM of the obtained Gaussian peak, which represents the timing resolution of the TCSPC system, was measured for different delays and FSRs after the application of the calibration routine. The timing resolution of the

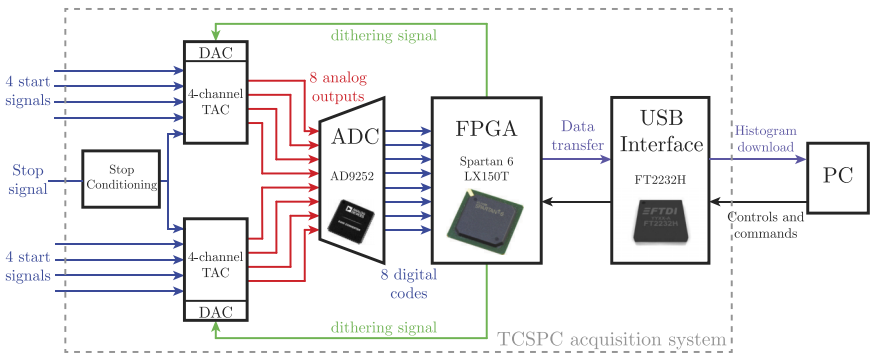

FIG. 9. Block diagram of the employed 8-channel TCSPC acquisition board. The time delay between eight start signals and the stop reference is measured by means of two TAC arrays and then digitized by an ADC. The digital codes are then sampled and recorded by an FPGA. Reproduced with permission from Antonioli *et al.*, Rev. Sci. Instrum. **84**, 064705 (2013). Copyright 2013 AIP Publishing LLC.

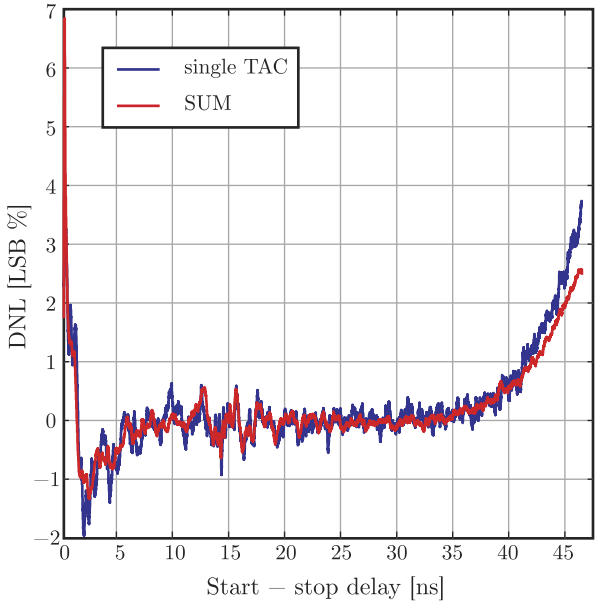

FIG. 11. Differential non linearity of one timing channel compared with the one of the F-TACs.

F-TAC was obtained by summing up the eight individual histograms.

Figure 10 reports the timing resolution of the F-TAC as a function of the start-stop delay, compared with the one of the eight individual timing channels. A remarkable timing resolution of about 55 ps FWHM is observed for the F-TAC, comparable with the one of each timing channel. Similar results were obtained with all the available FSRs, i.e., 11, 22, 45, and 88 ns.[26]

In order to measure the DNL of the F-TAC, the outputs of two pulsers working at different frequencies were used as start and stop signals, thus being these signals uncorrelated. Experimental results were quite similar for all the eight tested channels and the available full-scale ranges. As an example, Figure 11 shows the DNL of a single timing channel compared to the DNL of the F-TAC for a FSR of 45 ns. Also in this case, the performance of the single channels is comparable with the one of the F-TACs. The DNL increase in the first part of the plot, i.e., for short start-stop delays, is due to the current generator inside the converter, whose output undergoes an initial transient before approaching the nominal value causing the time bin-width to be slightly larger. The DNL increase in the last part of the plot, i.e., for long start-stop delays, is due to the amplifier inside the converter whose output starts to saturate. The ADC full-scale range is 2 V and therefore the Least Significant Bit (LSB) value is 122 μV. Finally, considering a useful 10%–90% full-scale range, the DNL is equal to 2% LSB peak-to-peak.

These results validated our idea and led us to start the integration of this low dead time time-to-amplitude converter.

VI. CONCLUSIONS

High count rate capability is becoming a key feature in a wide variety of advanced TCSPC applications.[27] A way to address this issue is to reduce the overall system dead time, thus enabling efficient photon collection at high excitation rate.

In this paper, we presented a fast active quenching circuit for single-photon avalanche diodes, which features a minimum dead time of 12.4 ns, thus allowing saturated count rates up to about 80 Mcps. This fast TAC makes it possible to operate the system towards the upper limit of detector count rate capability. A first prototype of the F-TAC was implemented by exploiting an 8-channel acquisition board previously developed in our lab. Preliminary experimental results show that the fast TAC provides a timing resolution FWHM of about 55 ps and a differential non linearity of 2% LSB peak-to-peak over a useful 10%–90% interval of the full-scale range. This result validates the basic idea of the new converter, thus opening the way to the development of high count rate TCSPC systems.

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