Cost-Effective High-Performance Single-Photon Detection System

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We pioneer a novel single-photon detection platform able to exploit the best performance out from state-of-the-art Single-Photon Avalanche Diodes (SPADs), fabricated in CMOS, custom Silicon and also InGaAs/InP technologies. The platform provides cost-effective, high-performance, fully programmable, time-resolved detection modules, all based on a common FPGA processing board and compact industry-standard 1-inch aluminum tube housing.

Two implementations exploit either a large area (up to 100 µm) CMOS SPAD [1] with Active Quenching Circuit [2] and a 10 ps resolution Time-to-Digital Converter (TDC) [3] or a 32x2 (50 µm) linear CMOS SPAD array with multiplexed TDC and readout. The modules effectively provide two stand-alone complete Time-Correlated Single-Photon Counting (TCSPC) systems, with either single-channel or 64-channels, with extremely reduced size (1" x 2"), low power consumption (self-powered through a standard USB 2.0 link), low cost and no need of expensive and bulky external TCSPC boards. The FPGA architecture and the 40 MB/s communication interface enable real-time data analysis and built-in histogram computation, with a high degree of data processing flexibility. A bidirectional wide-band SMA connector can be programmed as trigger output/input, for synchronization with external systems (e.g. laser) in TCSPC or 3D LIDAR setups.

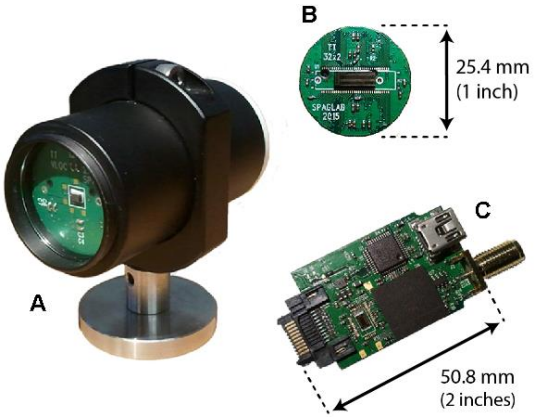

Fig. 1 : (A) Complete module with a single CMOS SPAD; (B) 32x2 CMOS SPAD array *Detection Board*; (C) *TDC+FPGA Board*, with micro USB link and input/output SMA connector.

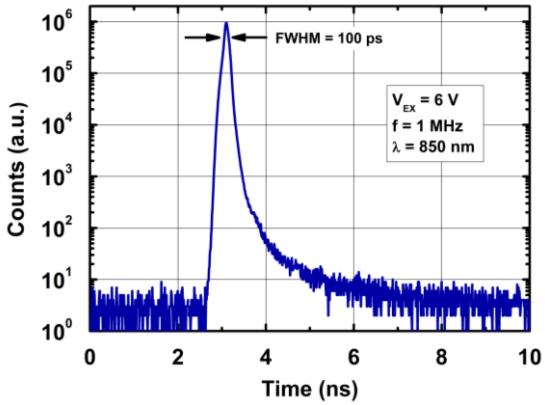

Fig. 2 : Temporal response of a single-pixel 50 µm SPAD *Detection Board* to an 850 nm laser pulse (40 ps FWHM), resulting in ~ 100 ps FWHM at 6 V excess bias.

Fig. 1 shows platform's hardware, based on a *Detection Board* and a *TDC+FPGA Board*, hosting the 10 ps TDC chip [3], a Xilinx Spartan-6 FPGA for data processing, an USB 2.0 high-speed controller and a wide-bandwidth connector, which provides all power supply and communication I/O lines to the *Detection Board*. Different *Detection Boards* have been developed, for hosting different home-made or third party SPADs: for example, Fig. 1A and Fig. 1B shows the ones with the single SPAD chip and the 32x2 CMOS SPAD array mounted, respectively. These boards directly provide digital "photon-out" signals to the *TDC+FPGA Board*, since the AQC can be either on-chip with the CMOS SPAD, or off-chip for custom SPADs. Excess bias, breakdown voltage and hold-off time are all user-programmable through a friendly graphical interface. Some *Detection Boards* host a CPLD (as for the 32x2 SPAD array implementation) for routing channel signals to TDC and for application-specific customizations (e.g. on-board counters, coincidence detection, correlation, etc.).

These implementations detect single-photons with 45 % detection efficiency at 550 nm (still > 15 % at 800 nm), a dark count rate less than 100 cps at room temperature and an afterpulsing probability less than 1 % with 60 ns hold-off time, giving a maximum saturated count rate of 16 MHz. The TDC performs time measurements over a range of 160 ns, with a maximum conversion rate of 3 Mconv/s. The whole system's single-shot precision is 100 ps FWHM (with the 50 µm CMOS SPAD, as in Fig. 2), and the differential nonlinearity is lower than 1.3% of LSB rms (i.e. < 130 fs).

References

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