Modeling resistance instabilities of set and reset states in phase change memory with Ge-rich GeSbTe

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Abstract—To satisfy the growing market demand for embedded non-volatile memory (eNVM), alternative solutions to Flash technology are currently under investigation. Among these, phase change memory (PCM) is attracting strong interest due to the low cost of integration with the CMOS front-end and good scalability. Embedded PCM (ePCM), however, must feature high reliability during both packaging and functional stages. This work studies reliability of PCM based on Ge-rich GeSbTe, providing evidence for resistance drift and decay in both the reset and set states. Set state instability is attributed to grain-boundary relaxation and grain growth. A unified model is presented, capable of predicting the reliability of set/reset states at elevated temperature.

Keywords: Phase change memory, embedded memory, set drift, soldering, reliability modeling
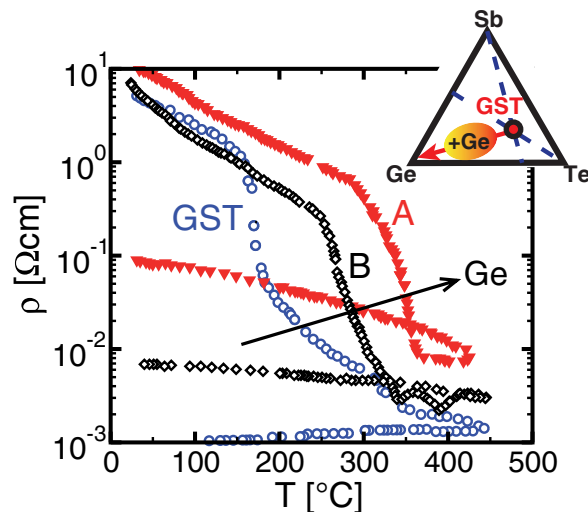
Fig. 1. Measured resistivity-temperature characteristic for different chalcogenide materials (T-ramp rate $10°C/min$). Note how the crystallization temperature T_X increases by increasing the Ge% from GST to alloy A.

I. INTRODUCTION

Phase change memory (PCM) is one of the main emerging memory technology, featuring nanosecond phase switching [1], low programming power [2] and good reliability and scalability. PCM properties can be tailored by material and cell engineering thus allowing for multiple applications, such as stand-alone nonvolatile memory [3], storage class memory (SCM) [4] and embedded memories in microcontrollers and smart cards [5]. Embedded phase change memory (ePCM) can be scaled to future lithographic nodes and is compatible with high-k metal gate logic, given its integration in the back-end of the line (BEOL) technology. On the other hand, ePCM should also feature data retention at high temperature, *e.g.*, $150°C$ in automotive applications, and during packaging, where the temperatures can rise above $250°C$ for few minutes. To satisfy these tough reliability constraints, new chalcogenide materials with improved crystallization temperature were proposed, namely Ge-rich GeSbTe [6]–[8], C-doped GeTe [9] and SiO_2-doped GeTe [10].

In this work, we address data retention in ePCM with Ge-rich GeSbTe, where we evidence a resistance drift and decay for both the set (poly-crystalline) and the reset (amorphous) states. These effects are modeled by structural relaxation and crystallization of amorphous chalcogenide phase, possibly residing at the grain boundaries in the set state [8]. We thus develop a unified model, capable of a physical description and accurate prediction of ePCM data retention for variable annealing conditions and programmed states. The present work extends the results of Ref. [8] by showing new experimental data and a more detailed explanation of the set/reset instabilities model. In particular, we added the comparison between PCM device with conventional active material and Ge-rich Ge-Sb-Te (Figs. 2-5) and we validated our physical interpretation by measuring the activation energy for conduction E_C in both the drift and decay regimes (Fig. 10). The onset of resistance decay after drift has been also modeled in detail in Fig. 15, allowing for an accurate prediction of resistance window as a function of operation temperature.

II. MATERIAL AND CELL ENGINEERING

Fig. 1 shows the measured resistivity as a function of temperature (T) during a ramped-T annealing experiment with heating rate of $10°C$ min^{-1}. The figure compares GST ($Ge_2Sb_2Te_5$) with two Ge-rich GeSbTe alloys, namely material B and A with increasing Ge content (see inset). The resistivity first decreases due to the temperature-activated conduction in the amorphous phase, then sharply drops as a
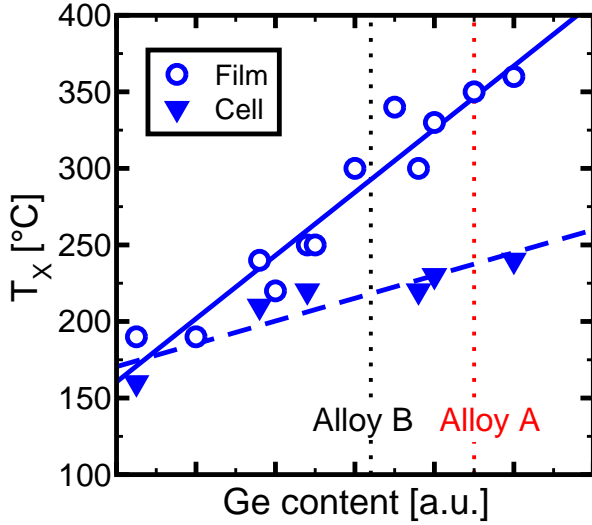
Fig. 2. Measured T_X as a function of Ge%. T_X is smaller after integration in the PCM cell, due both to the different experimental technique employed (T-ramp 10°C/min for the film and 1 hour bake for the cell) and possible local composition variation upon set/reset pulses on the PCM cell.

Fig. 4. IV characteristics of the ePCM with alloy A and GST as active layers. The higher V_T of alloy A allows better read-disturb immunity.
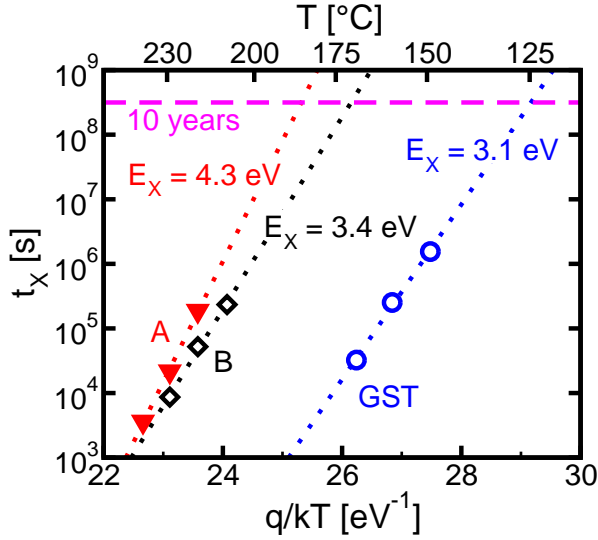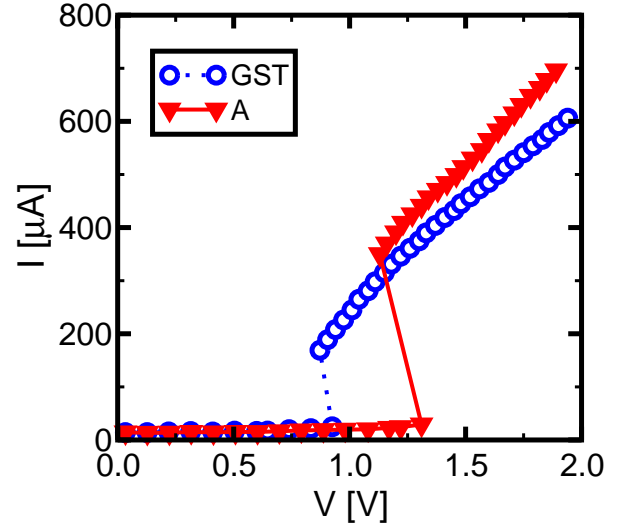

Fig. 3. Arrhenius plot of t_X for PCM with GST, alloy A and B. The activation energy increases and the stable T range at 10 years increases from GST to alloy A.
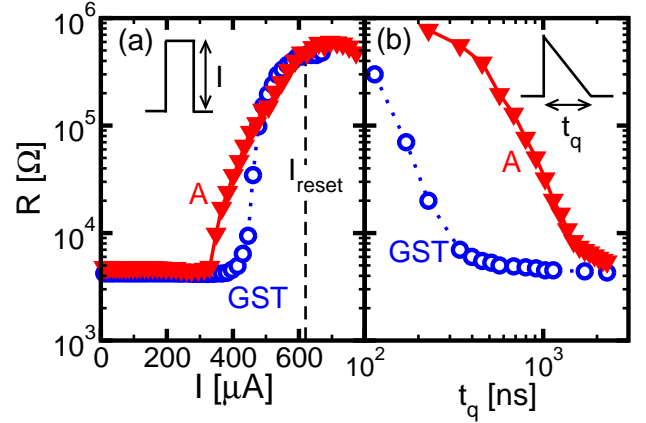

Fig. 5. Measured reset (a) and set (b) programming characteristics for alloy A and GST. In (a), resistance was measured for increasing current (inset), showing reset at about 600 μA for both materials. In (b), a triangular pulse with quenching time t_q was applied. Alloy A reaches set state in about 2 μs.

result of crystallization. The crystallization temperature T_X can be defined in correspondence of the maximum slope in the $R - T$ curves: T_X increases from about 150°C for GST to about 350°C for alloy A. The same measurement was repeated on many Ge-Sb-Te compositions with different Ge content. Experimental results in Fig. 2 clearly demonstrate the linear increase of T_X with Ge% in both thin film samples and PCM cells. The increase of T_X at higher Ge content can be attributed to the increase of tetrahedral Ge-Ge bonds [11], which stabilize the amorphous structure with respect to crystallization. PCM devices with 90 nm mushroom-type structure were fabricated using GST, alloy A or alloy B as active material [8]. Fig. 3 shows the Arrhenius plot of the crystallization time, defined by the drop of resistance below $R = 100$ kΩ of reset-state PCM devices during constant-T

annealing [8]. The data satisfy the Arrhenius law given by:

$$t_X = \tau_{0X} e^{\frac{E_X}{k_B T}} \tag{1}$$

where τ_{0X} is a time constant, k_B is the Boltzmann constant and E_X is the activation energy for crystallization. Using Eq. (1) to fit t_X in Fig. 3 we obtain $E_X = 3.1$ eV for GST, 3.4 eV for alloy B and 4.3 eV for alloy A. From these results, both t_X at a given T and E_X increase monotonically at increasing Ge content, in agreement with [6], [12]. This is a key guideline for the optimization of the PCM material for high temperature retention. In the following, we will restrict our attention to alloy A and to the reference GST material.

Fig. 4 shows the I-V characteristics of ePCM with alloy A and GST. Threshold voltage V_T for alloy A is higher than GST, which allows better stability over read disturb [13]. Fig. 5a shows the programming characteristics of PCM devices with GST and alloy A, namely the PCM resistance R as a function of the current of the applied square pulse. The reset transition appears as the rise of resistance in correspondence of a reset current I_{reset} of about 600 μA for both GST and alloy A. This
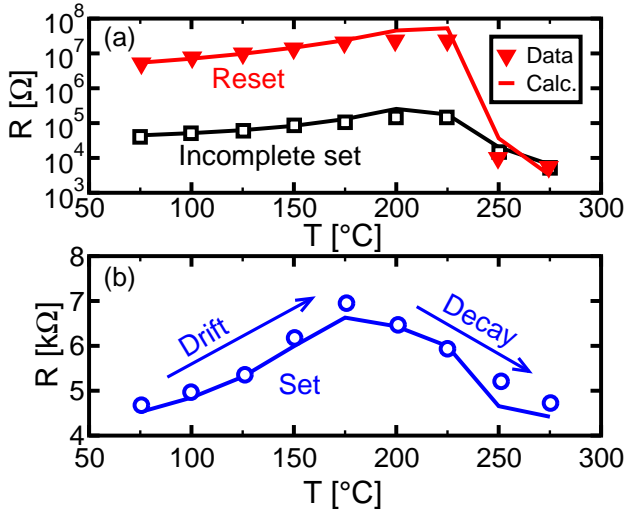
Fig. 6. Measured resistance for increasing annealing temperature for reset, incomplete set (a) and set state in (b). Each annealing step lasted 1 hour, while the resistance is measured at room temperature. All the states show an increase of R (drift regime) followed by a drop of R (decay regime).

indicates that I_{reset} is negligibly changed by increasing the Ge content, thus allowing for low power consumption in embedded memories. Fig. 5b shows the set transition characteristics, where R is monitored after the application of a triangular pulse with current I_{reset} and with increasing quenching time t_q (see inset). R decreases for increasing t_q, indicating the transition from the amorphous phase, obtained at fast quenching from the molten phase, to the poly-crystalline phase, originating from the regrowth of ordered grains at the boundary between the crystalline GST and the molten phase [14]. To achieve full crystallization, t_q is around 500 ns for GST and 2 μs for alloy A. Note that Fig. 5b seems in contradiction with Fig. 1, where the set-state resistance of GST and Ge-rich Ge-Sb-Te differs by an order of magnitude in Fig. 1, while they are almost equal in Fig. 5b. This difference might be attributed to the fact that the PCM device in Fig. 5b was programmed by electrical set/reset processes, which might induce local composition changes in the phase change region above the bottom electrode contact [15]. The longer set transition is the drawback of the increased Ge content, stabilizing the amorphous phase against crystallization as already seen in Figs. 1 and 3. Note, however, that a 2 μs set transition is much faster than the programming time of floating-gate memories, thus ePCM solution is advantageous in terms of speed for embedded applications.

III. RELIABILITY CHARACTERISTICS

To study R stability in PCM devices with alloy A, we performed annealing experiments for 1 h at constant annealing temperature T. Fig. 6 shows the PCM resistance measured at room temperature for reset, incomplete set states (a) and for the set state (b) as a function of T. The incomplete set and the set states were obtained with triangular crystallization pulses with $t_q = 1$ μs and 3 μs, respectively. All states in the figure display similar behavior, namely an increase of R in the drift regime, followed by a sharp decrease in the decay regime. GST-based PCM devices programmed in the reset state are
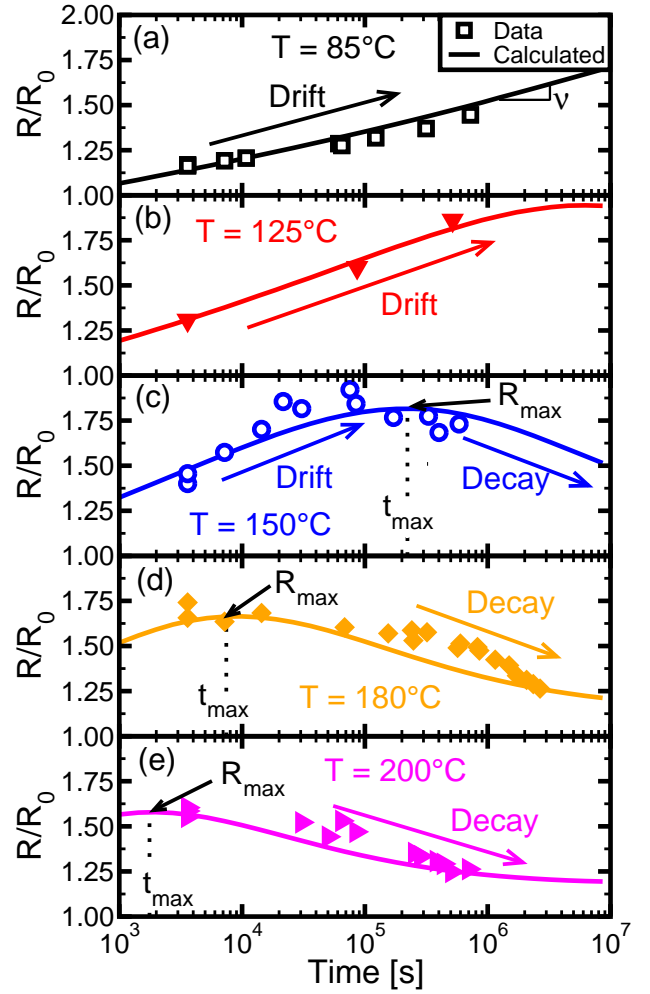

Fig. 7. Measured and calculated $R(t)$ for the set state at annealing temperature of 85°C (a), 125°C (b), 150°C (c), 180°C (d) and 200°C (e), indicating the T-acceleration of drift/decay. R_{max} and corresponding t_{max} are taken at the transition between the drift and decay regimes.

known to display drift [16], [17] and resistance decrease due to crystallization. Most recently, drift [5], [8], [10] and resistance decay [8] were reported for Ge-rich GeSbTe in the set state. Note that no set resistance drift was previously reported for conventional GST [18], which is the standard material for stand-alone PCM devices. This suggests a dominant role of Ge in the structural relaxation of chalcogenide materials [19]. Since the drift effect is detrimental on the set side of the reading window, a predictive model for extended reliability of ePCM based on Ge-rich GeSbTe is required. To further analyze the drift and decay regimes of the set-state resistance, Fig. 7 shows R measured at room temperature as a function of annealing time for isothermal conditions at increasing temperature $T = 85$°C (a), 125°C (b), 150°C (c), 180°C (d) and 200°C (e). The results clearly evidence the T-accelerated nature of drift and decay of resistance in the set state: For relatively-low T (Fig. 7a and b) the resistance evolution is dominated by drift, where the resistance drift slope ν in the log-log plot increases with T. For intermediate T (Fig. 7c and d), resistance drift is followed by decay, which takes place at increasingly short time for increasing T. Finally, at high T (Fig. 7e), only resistance decay is evidenced in the considered
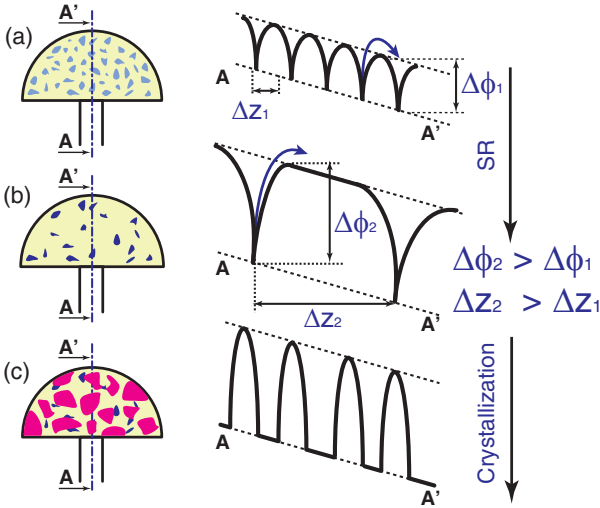
Fig. 8. Physical interpretation of the R drift/decay evolution in Fig. 6a for the reset state. Conduction in the amorphous phase is driven by hopping between energy barrier of height E_C (a). Structural relaxation (SR) consists of the annealing of defects, which leads to an increase of E_C (b), followed by the nucleation of crystalline grains (c), causing the drop of R.

range of experimental times.

IV. PHYSICAL INTERPRETATION OF RESISTANCE INSTABILITY

Fig. 8 describes the physical interpretation for resistance drift and decay in the amorphous reset state. Conduction in the amorphous phase is due to thermally-activated hopping among localized states in the mobility gap [20]. The resistance can thus be analytically described by a Poole-Frenkel (PF) equation given by:

$$R = R_0 e^{\frac{E_C}{k_B T}} \quad (2)$$

where R_0 is a pre-exponential constant and E_C is the effective (average) energy barrier for hopping (Fig. 8a). Drift is attributed to structural relaxation (SR) of the non-equilibrium amorphous state [21], resulting in an annealing of the localized states and in a consequent increase of the PF barrier height E_C (Fig. 8b). The barrier increase leads to an increase of R in Eq. (2), thus accounting for the observed resistance drift. Crystallization then follows by nucleation and growth of crystalline grains, resulting in a decrease of the number and heights of energy barriers and a consequent decrease of R (Fig. 8c).

Following the explanation of reset-state drift and crystallization in Fig. 8, we interpreted the set-state resistance instability by SR and crystallization of residual disordered phase in Ge-rich Ge-Sb-Te in Fig. 9. The residual disordered regions might be localized, for instance, at the grain boundary (GB) between crystalline grains, as indicated in Fig. 9a, or in some confined region along the conduction path. Previous literature works [22], [23] showed how conduction in poly-crystalline semiconductors appears limited by the GBs, acting as high-gap semiconductors due to the segregated defects and local disorder. Following this picture, the PF equation in our model was used to describe thermal emission over the barrier, rather than the PF conduction in the residual amorphous phase
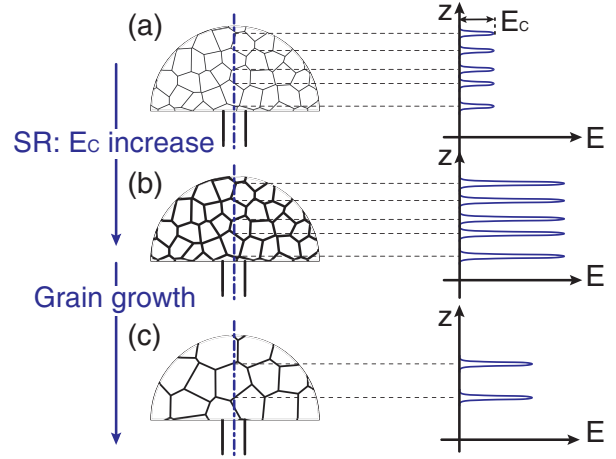

Fig. 9. Physical interpretation of the $R(t)$ behavior of the set state in Fig. 6b. Conduction is controlled by the residual amorphous phase at grain boundaries (GB). SR at GBs causes an increase of E_C (drift), while grain growth leads to E_C reduction and R decay.

itself. Thus, R in the set state can be expressed similar to Eq. (2) with proper choice of E_C. To support this conduction model, Fig. 10 shows the measured R and E_C for PCM with alloy A in the set state, before and after annealing at various temperature and time. For all states, E_C shows a value of few meV, thus consistent with the presence of a conduction barrier controlling the resistance, as shown in Fig. 9a. SR of the residual amorphous phase causes an increase of E_C (Fig. 9b) according to Eq. (2), thus leading to T-accelerated drift of the set state, evidenced in Fig. 7b. This physical interpretation is supported by results in Fig. 10, showing an increase of R and of E_C after moderate annealing of 1 h at 150°C in the set state. Further annealing results in grain growth and crystallization of the residual amorphous phase, resulting in a decrease of the height and number of energy barriers along the current flow (Fig. 9c) and to a consequent decay of R, as evidenced in Fig. 6b. This is demonstrated by the decay of R and E_C in Fig. 10 for extensive annealing, namely 1 day at 200°C and 230°C. Note the good correlation between R and E_C in both the drift and the decay regimes of the set state, which support the use of Eq. (2) for the set state and the physical interpretation of set-state resistance instability in Fig. 9. Our physical interpretation is also able to explain why set resistance drift/decay was not reported for conventional GST cells: The faster crystallization of GST would result in larger crystalline grains, with no or eventually few GBs along the conduction path.

V. SET-STATE RELIABILITY MODELING

The physical interpretation in Fig. 9 and the experimental results in Fig. 10 provide the basis for our model of the resistance instability in the set state. SR was described as T-accelerated annealing of defect, where each defect in the mobility gap displays a characteristic energy barrier E_{SR} for thermally-accelerated defect annealing [21]. The energy distribution $g_{SR}(E_{SR})$ of defect states thus evolves with time
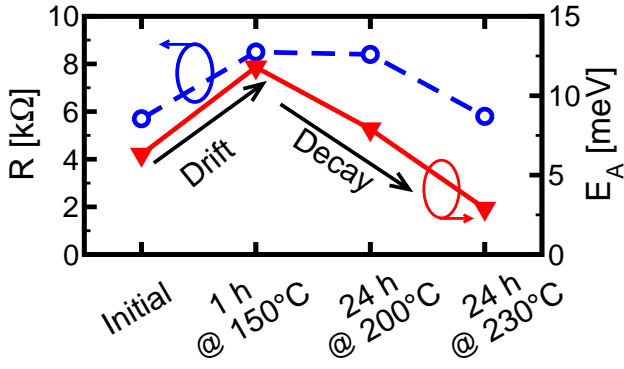
Fig. 10. Measured R and activation energy E_C for conduction of the set state at various annealing conditions. These results allow attributing the drift/decay effects to E_C, see Eq. (5).
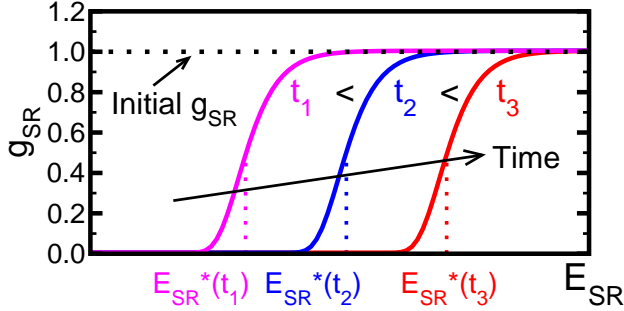

Fig. 11. Calculated defect distribution g as a function of E_{SR} at increasing time for $T = 150°C$. The initial distribution was assumed constant, then defects are annealed moving from low to high energy E_{SR}.

according to the rate equation [21]:

$$\frac{dg_{SR}}{dt} = -\frac{g_{SR}}{\tau_0} e^{-\frac{E_{SR}}{k_B T}} \quad (3)$$

where τ_0 depends on E_{SR} through the Meyer-Neldel (MN) rule [24]:

$$\tau_0 = \tau_{00SR} e^{-\frac{E_{SR}}{k_B T_{MN}}} \quad (4)$$

where $\tau_{00SR} = 8$ s and the Meyer-Neldel temperature $T_{MN} = 535$ K is the iso-kinetic T at which all defects show the same annealing time. Fig. 11 shows the calculated $g_{SR}(E_{SR})$ at an annealing temperature of $150°C$. First, states at low E_{SR} decay, since their corresponding transition time is shorter in Eq. (3). As time increases, states at larger E_{SR} decay, thus the density of defect states $g_{SR}(E_{SR})$ at any given time is virtually zero below a characteristics annealing front, defined by the energy E_{SR}^* for which $g_{SR} = 0.5$. Fig. 11 indicates that the annealing front energy E_{SR}^* increases for increasing time.

The SR kinetics in the set state can be furthered analyzed from Fig. 12a, showing the Arrhenius plot of the measured and calculated t_{SR}, defined as the time for R to reach a given resistance level, namely $1.3R_0$, $1.4R_0$ or $1.5R_0$ in the drift regime at constant T (see Fig. 7a). Since R identifies the annealed state, the activation energy obtained in the Arrhenius plot corresponds to the energy E_{SR}^* describing the same state in Fig. 11 [21]. The energy E_{SR}^* is reported in Fig. 12b as a function of R/R_0 describing the annealed state: E_{SR}^* increases for increasing R, since a larger R corresponds to stronger
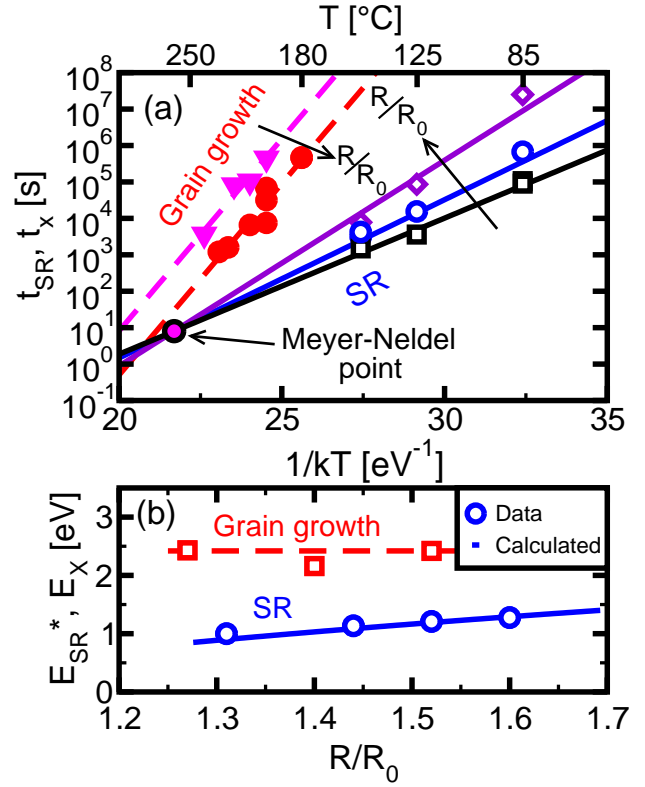

Fig. 12. (a) Measured and calculated Arrhenius plot of t_{SR} and t_X for variable threshold R/R_0 in Fig. 7 and (b) extracted activation energies for SR (E_{SR}) and grain growth (E_X) as a function of R/R_0. While E_{SR}^* increases during annealing, E_X is almost constant.

relaxation, namely more extensive annealing of defects in Fig. 11. Fig. 13a shows the calculated E_{SR}^* as a function of time for $T = 150°C$, evidencing the shift of the annealing front at increasing time.

Fig. 12a also reports the Arrhenius plot of t_X, defined as the time to reach a value R in the decay region (see Fig. 7d). The slope of t_X in the Arrhenius plot yields E_X, namely the energy barrier for crystallization of the residual amorphous phase in the poly-crystalline state. Fig. 12b shows that E_X remains almost constant for all values of R. To describe crystallization, a rate equation similar to Eq. (3) was thus adopted, where the activation energy for crystallization was kept constant at $E_X = 2.42$ eV and the pre-exponential time τ_0 is distributed in the amorphous material by a density function $g_X(\tau_0)$. In a similar way as before, it is possible to describe the crystallization front by τ_0^* taken at $g_X = 0.5$. Fig. 13a also shows the calculated τ_0^* as a function of time for $T = 150°C$: As τ_0^* becomes comparable to a critical value $\tau_{0X}^* = 3 \times 10^{-23}$ s, crystallization takes place. Tab. I summarizes the main parameters used in the model for various PCM states. Fig. 12a also shows calculation results for t_{SR} and t_X, while Fig. 12b shows the calculated E_{SR}^* as a function of R/R_0. The good agreement in both cases supports the accuracy of our model for SR and crystallization.

To describe the impact of SR and crystallization processes on R, the activation energy E_C of resistance is the modeled as:

$$E_C = \alpha E_{SR}^* \left(1 - \beta \tanh \frac{\log \tau_0^* - \log \tau_{0X}^*}{\eta}\right) \quad (5)$$
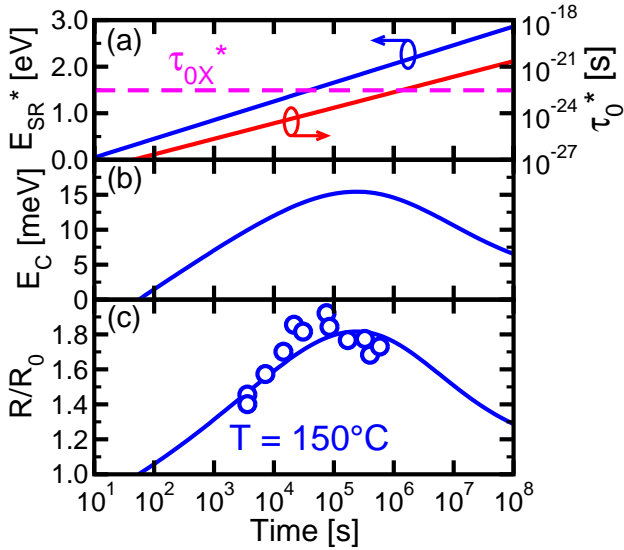
Fig. 13. (a) Calculated evolution of E_{SR}^* (left) and τ_0^* (right) by Eq. (3) (τ_{0X}^* is shown for reference) at $T = 150°C$, (b) calculated E_C for conduction by Eq. (5) and (c) measured/calculated R/R_0 by Eq. (2).

For $\tau_0^* \ll \tau_{0X}^*$ (drift regime), Eq. (5) predicts that E_C increases linearly with E_{SR}^* according to a parameter $\alpha = 0.014$, thus describing resistance drift through Eq. (2). As τ_0^* becomes comparable to τ_{0X}^* (crystallization, or grain growth regime), the second term in Eq. (5) results in a gradual decrease of E_C, where $\beta = 0.9$ controls the resistance decrease upon decay and $\eta = 4.3$ determines the slope of the decay, thus accounting for crystallization. Fig. 13b shows the calculated E_C, obtained by Eq. (5), evidencing the drift regime, where E_C increases linearly with E_{SR}^*, followed by the crystallization regime, where E_C decays as τ_0^* approaches the critical value τ_{0X}^*.

The resistance is then obtained from E_C through Eq. (2), as shown in Fig. 13c for $T = 150°C$. Calculations were repeated at different annealing temperatures under isothermal conditions, as shown in Fig. 7: In all cases, a very good agreement is obtained in both the drift and the decay regimes. The drift regime can be described by the slope ν in the log-log plot. The crossing from drift to crystallization is instead marked by the maximum of resistance R_{max}, occurring at a characteristic time t_{max} (see definition in Fig. 7c, d and e). These parameters determine the evolution of resistance window during memory operation, thus they play an essential role in reliability control and prediction of ePCM devices.

Fig. 14 shows the Arrhenius plot of measured and calculated R_{max} (a), t_{max} (b) and ν (c) for the set state during isothermal conditions. The transition time t_{max} decreases with T, as

TABLE I
ARRHENIUS AND MN PARAMETERS FOR SIMULATING THE KINETICS OF SR AND CRYSTALLIZATION/GRAIN GROWTH FOR THE SET, THE INCOMPLETE SET AND THE RESET STATES.

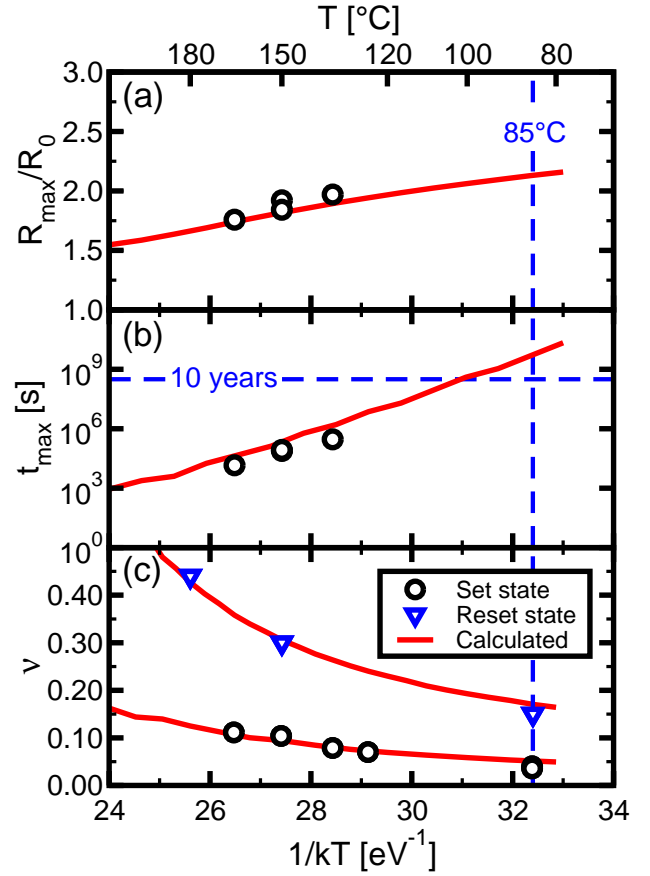|	$\tau_{00SR}[s]$	$\tau_{0X}^*[s]$	$E_X[eV]$	$T_{MN}[K]$
Set	8	$3\cdot10^{-23}$	2.42	535
Incomplete set	8	$3\cdot10^{-23}$	2.60	535
Reset	10	$3\cdot10^{-39}$	4.20	550

Fig. 14. Arrhenius plot of the measured and calculated maximum resistance R_{max} (a), the corresponding time t_{max}(b) and the drift exponent ν of set and reset states (c). The decrease of t_{max} (b) and the increase of ν (c) with T are due to the thermal activation of crystallization and SR respectively, while the decrease of R_{max} with T (a) is explained in Fig. 15.

a result of the temperature-acceleration of the crystallization processes. Similarly, the increase of ν with T can be explained by the T-acceleration of SR. The T-dependence of R_{max} can instead be understood by considering the Arrhenius plot of SR and crystallization processes in Fig. 12. To this purpose, Fig. 15 schematically shows the Arrhenius plot of t_{SR} and t_X, the latter evaluated at the onset of the decay regime at R_{max}. Two isothermal annealing are compared at temperatures T_1 and T_2 with $T_1 > T_2$. For $T = T_1$, the crystallization time t_X crosses t_{SR1}, corresponding to a resistance value R_{max1} which thus marks the transition between drift and decay. For $T = T_2 < T_1$, instead, t_X crosses a different SR time t_{SR2} with $E_{SR2}^* > E_{SR1}^*$, thus corresponding to a more relaxed state with larger resistance R_{max2}. Since $R_{max2} > R_{max1}$, the maximum resistance at the crossing between drift and decay increases for decreasing temperature in a isothermal annealing experiment. Note that this result is due to the crystallization time t_X passing below the isokinetic point where all t_{SR} line cross each other. This interpretation allows to explain the results in Fig. 14a, which highlights that low-temperature annealing, while causing less acceleration of drift, results in a larger reduction of the available read window at t_{max}, which should be taken into account for reliability prediction.
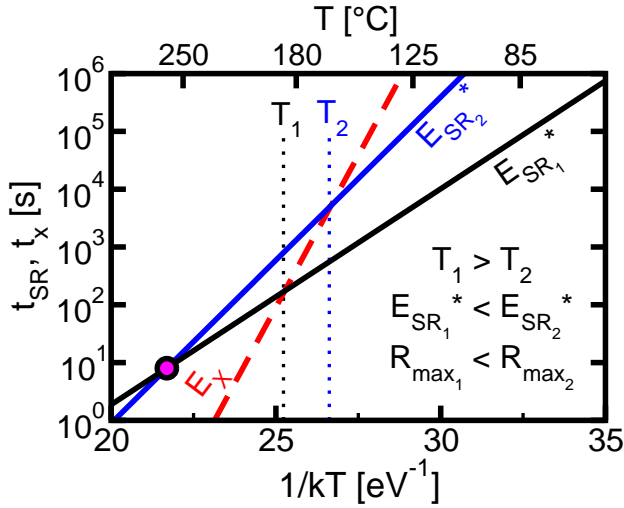
Fig. 15. Simplified sketch of the Arrhenius plot of SR and crystallization time in Fig. 12. The crystallization front at the transition between the drift and the decay regimes (dotted line) crosses two different SR fronts at T_1 and T_2 (with $T_1 > T_2$). Note that $E_{SR1}^* < E_{SR2}^*$. Since E_C increases with E_{SR}^* (Eq. (5)), this explains why R_{max} in Fig. 14a decreases at increasing T.

VI. UNIFIED MODEL

The experimental results in Fig. 6 demonstrates that set and reset states display similar annealing behavior with resistance drift followed by resistance decay. Therefore, the model for set-state resistance evolution was extended to the reset state and to intermediate states in PCM with alloy A as active chalcogenide material. The reset state is characterized by a larger activation energy $E_X = 4.3$ eV (Fig. 3): This is markedly larger than $E_X = 2.3$ eV in the set state, possibly because the amorphous region extends to the whole programmed dome in the reset state. On the other hand, the residual amorphous phase at GBs in the set state might suffer from easy crystallization due to the adjacent crystalline grains. The incomplete set state, obtained by a triangular set pulse with $t_q = 1$ μs, displayed activation energy $E_X = 2.6$ eV intermediate between the set and the reset states possibly due to the larger residual amorphous phase with thicker GBs and smaller grains [25]. Model parameters used in our calculations for the reset and intermediate states are reported in Tab. I. Calculation results by the unified model are shown in Fig. 6a (reset and intermediate states) and Fig. 6b (set state) for R measured after annealing at fixed time (1 h) and increasing T. The measured and calculated slope of resistance drift for the reset state is also shown in Fig. 14c to further support the accuracy of the unified model.

Fig. 16a shows the measured and calculated R as a function of time for the set and reset states at $T = 85°C$ and $150°C$, to describe possible worst cases in consumer and automotive applications, respectively. For the sake of clarity, Fig. 16b shows results for the set state on a smaller resistance scale. Calculation results closely reproduce data for experimental times below 10^6 s and allow prediction of the resistance evolution at longer times. According to the model, data retention is guaranteed up to 10 years, with a minimum resistance window in correspondence of t_{max} of more than 2 decades, assuming a minimum reset-state resistance of 1 MΩ for shorter times
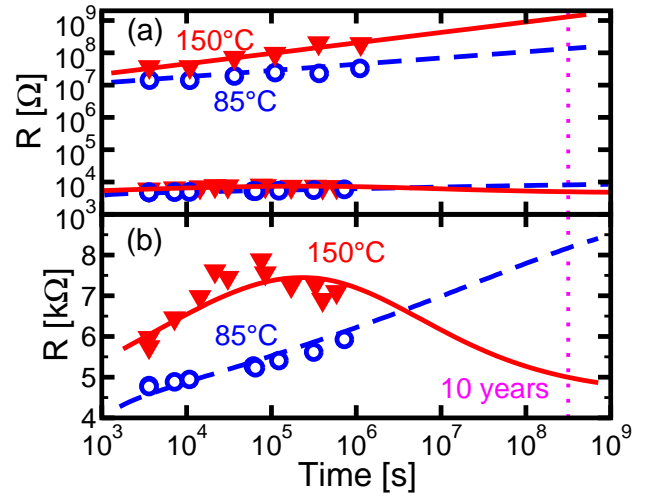

Fig. 16. (a) Measured and calculated R for set/reset states during isothermal annealing at $85°C$ and $150°C$. The evolution of the set state is highlighted in (b).
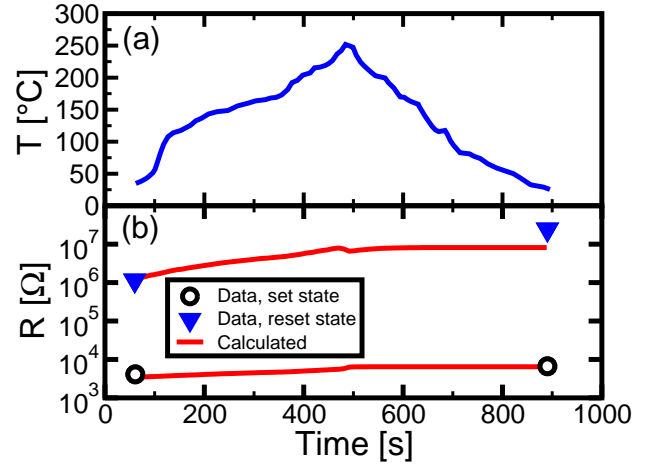

Fig. 17. Temperature evolution during soldering according to the JEDEC standard [26] (a) and corresponding calculated evolution of R for the set and reset states (b). Data and calculations confirm good data retention after soldering reflow process.

not shown in the figure. The set state displays pure drift at $85°C$, since t_{max} is larger than 10 years in this case. On the other hand, t_{max} is around 10^5 s for $150°C$, with a maximum resistance of about 8 kΩ. The anticipated decay has a beneficial impact on the resistance window, due to the T-dependence of R_{max} in Fig. 16a.

Finally, we investigated data retention upon soldering reflow process [12], [27]. Fig. 17a shows the soldering temperature profile according to the JEDEC standard [26], reaching a maximum temperature of $250°C$. Fig. 17b shows the measured and calculated resistance before/after soldering. Data were obtained from the median value within 100 cells, while the calculations were performed by Eq. (3) using the time evolution of T in Fig. 17a. The model is able to predict the resistance evolution for both set and reset states even in non-isothermal conditions. Experiments and calculations demonstrate data retention upon soldering reflow process.

VII. Conclusions

Embedded PCM offers several advantages in terms of cost and scalability compared to Flash memory, however the tight reliability requirements must be met through material engineering. The resistance instability has been analyzed in ePCM devices based on Ge-rich GeSbTe. Although Ge enrichment leads to higher crystallization point in the reset (amorphous) state, the set state displays drift and decay of resistance. These effects are interpreted by SR and crystallization of residual amorphous phase, possibly located at the GB of the poly-crystalline phase. A new model is developed to describe SR and crystallization in the set state, then extended to the reset and incomplete set states to achieve a unified model of resistance change with time. The model allows for physics-base extrapolation of resistance variation, allowing to demonstrate data retention at $85°C$ and $150°C$ for 10 years and after soldering reflow.

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