Multichannel low power time-to-digital converter card with 21 ps precision and full scale range up to 10 μs

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Multichannel low power time-to-digital converter card with 21 ps precision and full scale range up to 10 μs

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We present a Time-to-Digital Converter (TDC) card with a compact form factor, suitable for multichannel timing instruments or for integration into more complex systems. The TDC Card provides 10 ps timing resolution over the whole measurement range, which is selectable from 160 ns up to 10 μs, reaching 21 ps rms precision, 1.25% LSB rms differential nonlinearity, up to 3 Mconversion/s with 400 mW power consumption. The I/O edge card connector provides timing data readout through either a parallel bus or a 100 MHz serial interface and further measurement information like input signal rate and valid conversion rate (typically useful for time-correlated single-photon counting application) through an independent serial link. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4900863]

I. INTRODUCTION

Many applications require to accurately measure the time delay between a synchronization pulse and an event, with sub-nanosecond resolution and precision. For example, the Time-Correlated Single-Photon Counting (TCSPC) technique[1] allows to reconstruct fast, low intensity, and repetitive optical waveforms by means of high sensitivity photodetectors and high performance time measurement instrumentation, such as in fluorescence lifetime imaging (FLIM),[2] Förster resonance energy transfer (FRET),[3] fluorescence correlation spectroscopy (FCS),[4] and diffuse optical tomography (DOT),[5] just to mention a few. TCSPC is based on the detection of single photons of the optical signal under test and on the precise measurement of their arrival time; after many acquisitions of individual photons, the histogram of the arrival times allows to reconstruct the optical signal waveform, down to few picoseconds with no need to employ hundreds of GHz bandwidth electronics. Detectors employed in TCSPC-based optical applications are principally photomultipliers (PMTs), micro-channel plates (MCPs), or Single-Photon Avalanche Diodes (SPADs):[6] PMTs and MCPs are bulky, usually not very robust and require high voltages and power; SPADs are currently the most practical solid state, high performance photon counting detectors.

Advanced time measurement devices must provide both picosecond resolution and very low Differential Non-Linearity (DNL), really much better than the typical 50% LSB of standard and general purpose commercial instrumentation. For instance, state-of-the-art TCSPC boards provide 0.8 ps resolution with less than 0.8% LSB rms DNL,[7] and 4 ps resolution with less than 1% LSB rms DNL.[8] Time measurement devices can be either digital, like Time-to-Digital Converters (TDCs), able to perform direct conversion of a time interval into a digital code, or analog such as Time-to-Amplitude Converters (TACs), which perform an intermediate conversion into an analogue voltage prior to Analog-to-Digital Conversion (ADC). At the beginning, TACs were the preferred solution for TCSPC applications due to the better nonlinearity performance. Instead recent improvements in the DNL performance of TDCs make these devices a more valid alternative in TCSPC setups, also considering the other two key advantages in respect to TAC devices, i.e., intrinsic robustness to disturbances and much longer full scale range attainable at the same resolution (LSB).

Furthermore, many applications require multi-channel systems where each channel is fed by a separate detector, for instance, working at a different wavelength (e.g., as in time-resolved functional near-infrared spectroscopy[9] and in time-resolved fluorescence spectroscopy[10]), or imaging different spatial spots of the object under observation (in order to reduce the acquisition time of scanning based FLIM instrumentation[11]). In all those cases, the time measurement electronics must be duplicated or, at least, smart signal routing must be employed to minimize size and cost of electronics.[12,13]

In this paper, we present a stand-alone TDC Card able to measure time intervals up to 10 μs with a constant 10 ps resolution, 21 ps single-shot precision, and 1.25% LSB rms (i.e., 0.125 ps), DNL. The compact dimensions and the multi-function I/O edge-card connector allow easy integration of the Card into multichannel timing measurement systems or in other complex systems requiring precise time measurement.

The paper is organized as follows: the architecture of the developed TDC Card is described in Sec. II, while experimental characterization is presented in Sec. III; finally Sec. IV summarizes the work.

II. TDC CARD ARCHITECTURE

The TDC Card is shown in Fig. 1 and is 78 mm × 28 mm × 10 mm. The time interval to be measured is defined by the START and STOP input signals, which can be provided

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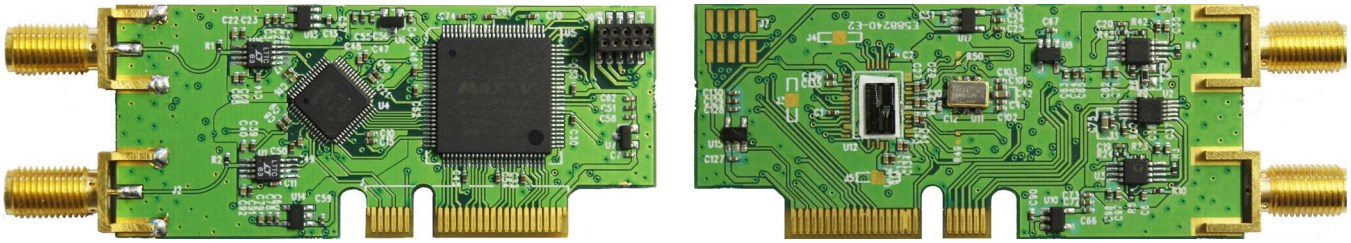

FIG. 1. Picture of both sides of the TDC Card, showing the two input SMA connector and the I/O edge card connector. The TDC chip, the 100 MHz reference clock, and the linear regulators are shown on the right, while the signal conditioning electronics and the data processing CPLD are on the left. Overall dimensions are 78 mm × 28 mm × 10 mm.

by two SMA connectors or through two dedicated edge card connector pins. The edge card connector also provides pins for data-bus readout, module configuration, and power supply. Compared to our previously developed TDC Module,[14] this TDC Card provides high performance in a more compact footprint and much reduced power consumption, thus enabling multichannel systems instrumentation.

The core of the Card is an application-specific integrated TDC circuit fabricated in a 0.35 μm CMOS technology,[15] which employs two independent START/STOP channels to measure the START/STOP arrival times in respect to an extremely stable and low jitter 100 MHz reference clock. An input signal front-end circuitry performs signal conditioning and a Complex Programmable Logic Device (CPLD) manages the TDC chip, data acquisition, and calibration.

A. TDC IC

The TDC chip,[15] shown in Fig. 2, is based on a "coarse" counter and two (START and STOP) interpolators. The counter accumulates the number of reference clock rising edges occurring between START and STOP, hence providing a maximum measurable time interval (Full Scale Range, FSR) of 160 ns. The interpolators are identical and resolve START and STOP occurrences within the reference clock period, reaching 10 ps resolution. This topology also inherently implements the sliding-scale technique, thus improving measurement linearity. Each interpolator consists of two cascaded interpolation stages: a multiphase-clock interpolator and a single-stage Vernier delay-loop interpolator. This is a good trade-off between low power consumption, high resolution, good DNL, and fast conversion time. The effective interpolators' resolution is affected by process mismatches, therefore calibration coefficients are needed to properly compute raw interpolator data.[16]

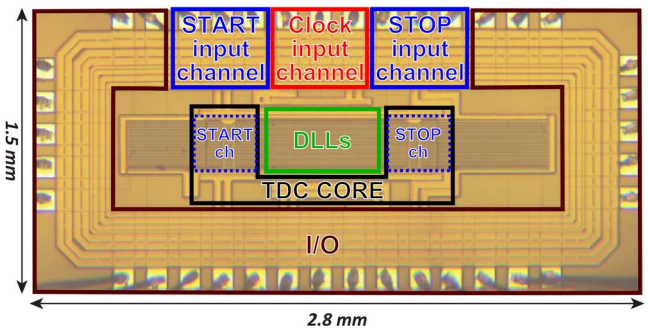

FIG. 2. Microphotograph of the TDC chip, containing the two independent START and STOP interpolators and the global electronics for synchronization and references.

The TDC operation principle is illustrated in Fig. 3. The counter output is proportional to time $T_{counter}$, which is given by the reference clock period multiplied by the number $N_{counter}$ of clock rising edges occurred between START and STOP pulses. The first interpolator stage is a multiphase-clock interpolator based on a Delay-locked loop (DLL) witch creates 16 signals, synchronous to the reference clock, and delayed by 16 different delays with 625 ps step, from 0 to the 10 ns reference clock period. When a START (or a STOP) pulse occurs, all multiphase clocks are sampled, and a decoder translates the clocks state into a code corresponding to the time elapsed between the first clock phase successive to the START (or STOP) pulse and the successive reference clock rising edge with a 625 ps resolution. Then the second interpolator stage measures the time-interval between a START (STOP) pulse and the first successive clock phase with a 10 ps resolution; it consists of a modified Vernier delay line, folded in two delay loops. The START (STOP) pulse and the clock phase pulse selected by the first interpolation stage cycle within two delay loops; the cycling is stopped when the clock pulse overtakes the START (STOP) one. The overall time interval result T is given by the number of clock rising edges ($N_{counter}$) counted by the counter, multiplied by the clock period (T_{CK}), plus the time measured by the START interpolator (T_{START}), minus the time measured by the STOP interpolator (T_{STOP}),

$$T = N_{counter} \times T_{CK} + T_{START} - T_{STOP}. \quad (1)$$

The counter provides a 4 bit output, while each interpolator provides an 11 bit output, namely, N_{START} and N_{STOP}. These raw data are then converted into T_{START} and T_{STOP} taking into account the effective resolution of the interpolators. When a time interval greater than 160 ns is measured, the TDC "coarse" counter folds, thus giving an incorrect data, while the interpolators provide valid N_{START} and N_{STOP} values. As described in the followings, proper external logic circuits is needed to sense the folding of the "coarse" counter and to extend the full scale range.

The TDC chip is designed to interface with 3.3 V LVCMOS signals. It also requires a 100 MHz reference clock as a time base for measurements, and accepts the first START and then the first STOP pulse following a RESET command; successive input pulses are rejected until the next

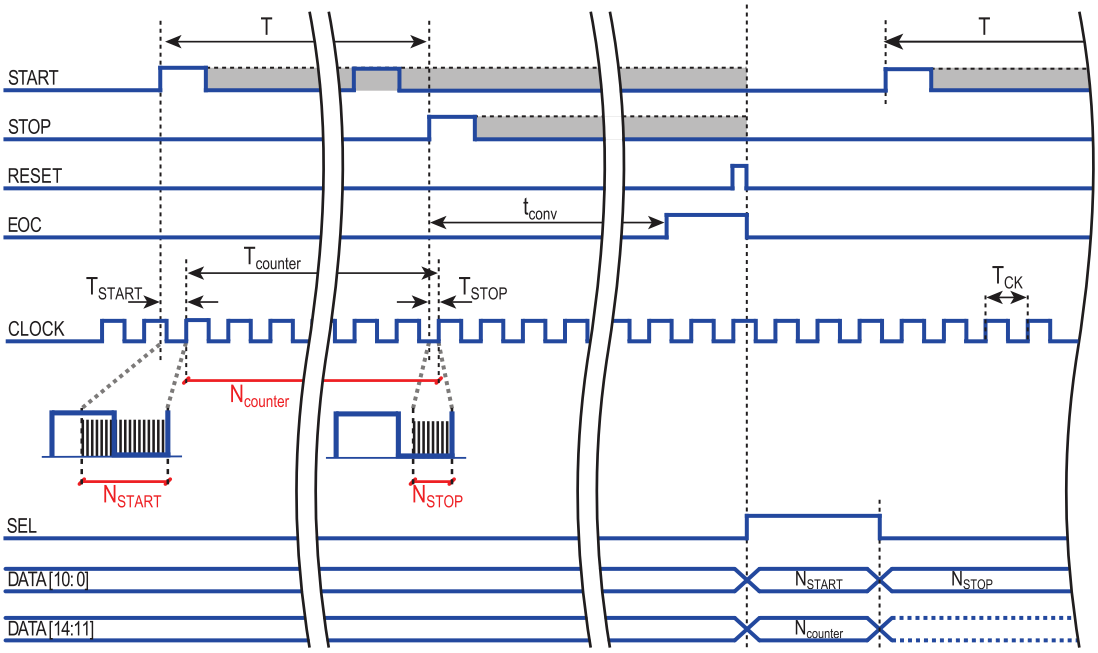

FIG. 3. Timing diagram of the TDC main signals. After the RESET falling edge the TDC is ready to perform a new conversion, while the previously conversion results are stored in a register and are available to be readout through the output bus by means of SEL control. The time interval T is measured using the interpolator principle: the counter accumulates the number of reference clock rising edges between START and STOP, while two identically interpolators resolve the occurrences of both START and STOP events within 10 ps resolution. Eventually, the End-Of-Conversion (EOC) signal marks the end of conversion.

RESET. After a valid START-STOP couple, the TDC is busy performing the conversion, which lasts until the End-Of-Conversion (EOC) signal is set. This occurs within a 150 ns maximum conversion time (conv); the ASIC then requires a RESET pulse for storing conversion results into the output registers and for resetting counter and interpolators for the next conversion. The result is readout by using the SEL signal, which selects the data the TDC has to output on the 15 bit bus: SEL = 1 for the 11 bits of N_{START}, 4 bits of $N_{counter}$; SEL = 0 for the 11 bits of N_{STOP} (the remaining 4 bits are left floating).

B. Input signal conditioning electronics

The TDC chip requires signals with 3.3 V CMOS levels and is rising-edge sensitive. The signal conditioning front-end shown in Fig. 4 allows to use any input level (NIM, ECL, TTL, CMOS, or non-standard signals), both positive and negative edge-triggered, as START and STOP signals. The first stage of the front-end electronics uses two fast comparators (LT1711 by Linear Technology), powered at ±3.3 V, having a very low propagation delay and dispersion. The START/STOP signals provided through SMA connectors feed the positive inputs of the respective comparator, while the negative inputs are connected to the outputs of a dual 12 bit DAC, which provides the user-selectable threshold level. The DAC is controlled via an I2C interface accessible through the edge-card connector. The START and STOP thresholds can be independently set within the ±2.5 V range, with 2.44 mV steps.

The 3.3 V standard CMOS comparator outputs trigger a 40 logic elements non-volatile CPLD (Altera MAX V family). Since START and STOP signals can be sourced from either the input comparators or the edge-card connector, the CPLD firmware implements a multiplexer, to select which signal must be fed to the TDC, and an XOR logic gate, for edge selection; this structure is replicated for both the START and STOP paths. In order to provide valid START-STOP inputs to the TDC chip, the CPLD firmware includes a D-type Flip-Flop (FF) on each path. When the TDC EOC signal is low, the first START input signal sets the START FF output high, masking any successive input pulses. When the START FF output is high, the STOP FF is enabled and only the first successive STOP pulse sets the FF output high. The flip-flop outputs are kept high as long as the TDC completes the conversion, guaranteeing no signal commutation, while the TDC is busy. This CPLD-based front-end provides a lower propagation delay, jitter degradation and better area optimization compared to using discrete digital logics.

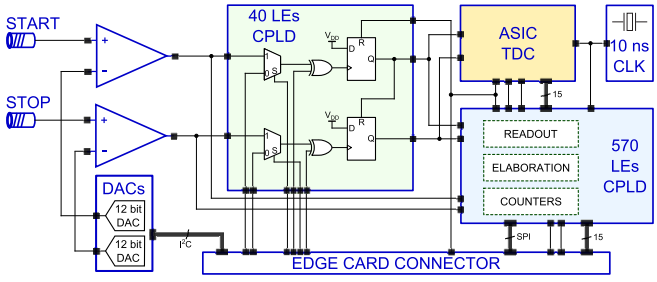

FIG. 4. TDC Card block diagram. The 100 MHz reference clock is provided by a crystal oscillator and a phase-locked loop circuit. The TDC chip valid START and valid STOP are signal-conditioned by means of a 40 Logic Elements CPLD with the task to select between SMA or edge card connector input for each input and the respective synchronization edge. The input comparators have adjustable thresholds in order to convert the SMA input pulses into CMOS signals. A 570 Logic Elements CPLD perform data readout and data processing.

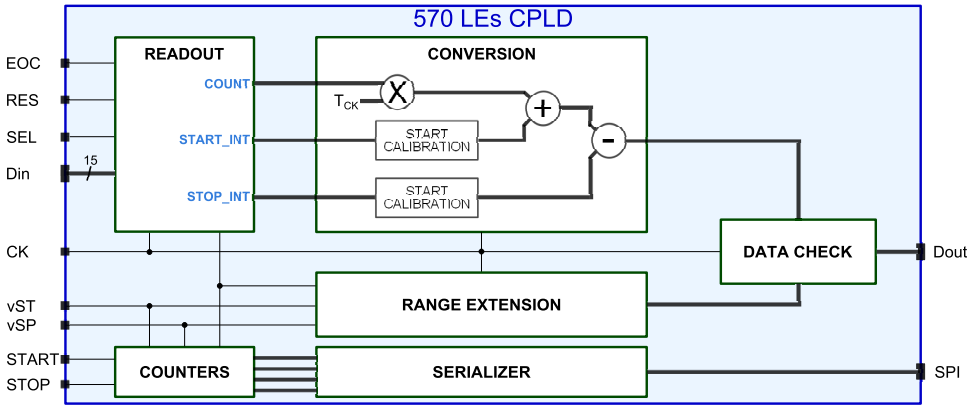

FIG. 5. Simplified block diagram of the data processing CPLD: TDC readout and signal management is the first task; then data conversion employs calibration coefficients to provide timing result. The output TDC bits are merged with those of the range extension circuitry, which works in parallel. The final time results are available on the 15 bit parallel output bus or on a serial interface. The counters are used in order to measure the START, STOP, conversion, and valid conversion rates. These information are serialized and available via SPI interface.

In order to minimize disturbances and crosstalk between START, STOP, and reference clock signals, each path uses components powered by separate supply rails. Also the CPLD START and STOP signals are located on different CPLD I/O banks; the core power supply however is the same. The use of two CPLDs would have guaranteed better isolation between START and STOP paths, reducing mutual disturbances, but it would have increased area occupation, power dissipation, and propagation delay between the START FF output and the STOP FF reset input, resulting in an increase of the shortest measurable time interval.

C. Data processing and range extension

The TDC chip output bus provides the raw data conversion result, composed by 4 bits for the global counter and, for each interpolator, 4 bits for the first stage and 7 bits for the second stage. A 570 logic elements non-volatile CPLD (Altera MAX V family) is used to perform chip management, data acquisition and calibration, and rates measurement, as shown in Fig. 5.

The counters are used to measure the START, STOP, Conversion, and Valid Conversion rates, since this information is very useful in most applications, such as in TCSPC: four counters are used to accumulate the number of events occurred since their last readout, thus they provide the user with the average event rate information. Their data can be accessed through an independent SPI (Serial Peripheral Interface) bus in order to update the rates value at least 800 times per second.

The first data processing function implemented in the firmware is the TDC chip readout, where a state machine handles the data acquisition. The default state waits for an EOC signal then feeds a RESET pulse to the TDC chip. The following state sets SEL = 1, so in the next state the counter and START interpolator data are stored while SEL is reset to 0. Finally in the last state, the STOP interpolator data are stored, a flag signals a valid data ready to be processed and the state machine returns at the default state. A second CPLD firmware function is data conversion: when the readout flag is set, a 5 stage pipeline structure converts the TDC raw data, applying the necessary interpolator calibration coefficients and performing Eq. (1).

Another function implemented in the data conversion CPLD firmware is the extension of the conversion range beyond the intrinsic 160 ns limit. This can be done because the TDC chip does not stop an ongoing conversion when its range is exceeded, and the CPLD has access to the same reference clock, valid START (vST) and valid STOP (vSP) signals that are used by the chip. The idea is to use the TDC interpolator results and to replace the "coarse" counter with a longer one. The implementation of this range extension function consist in a four bit "range counter," that emulates the TDC coarse counter, while a second "frame counter" keeps track of how many times the range counter overflows. Both TDC chip and CPLD make use of the same reference clock, START and STOP signals, but due to different signal propagation delay and circuit fabrication technology the coarse counter and the range counter can count different reference clock rising edge in the same time interval. Aim of the range counter is not to substitute the TDC coarse counter, instead to split the intrinsic TDC range into a safe zone, where the frame counter is certain to be correct, and an uncertain zone, where the frame counter might be lagging behind; this uncertainty is then solved by checking the TDC conversion result against the range extension information.

When the conversion result is ready, the firmware sends the final result to the output interface. In order to make the TDC Card versatile for different systems, the output interface can be a 16 bits parallel bus or a 100 MHz serial interface. In fact a simple microcontroller can read form the parallel bus the TDC results, while the 100 MHz serial interface can be supported by an external deserializer or a FPGA devices. In particular for FSR settings that require more than 16 bits the output interface is serial only.

III. CHARACTERIZATION

The main figures of merit for time measurement systems are timing precision, timing accuracy, and differential nonlinearity. In order to make this card suitable for multichannel systems, power consumption is also a key factor. The TDC chip consumes about 50 mW in idle state and up to 80 mW at

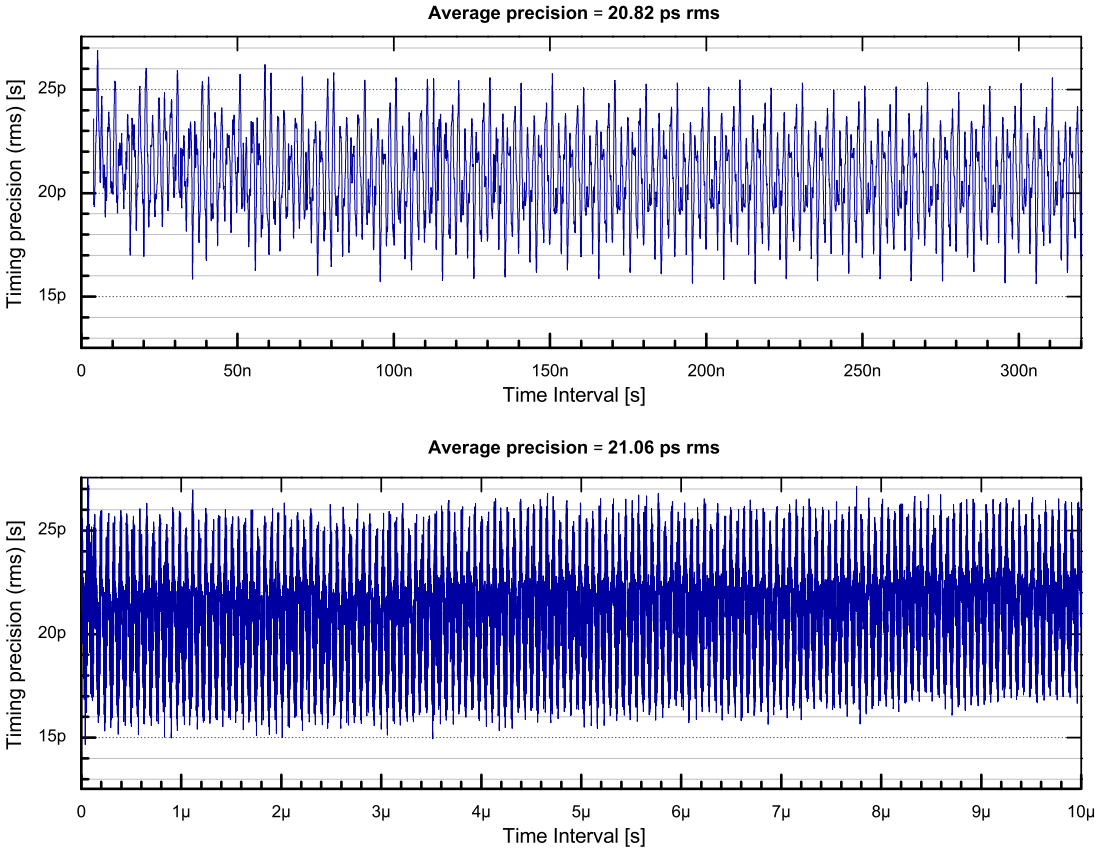

FIG. 6. Timing precision of the TDC Card, expressed as rms value of the distribution of measurement results around the mean value of a constant time-interval, swept across a 320 ns full scale range with 100 ps steps (top) and across a 10 μs full scale range with 1.5 ns steps (bottom).

the maximum conversion rate of 3 Mconversion/s. The overall Card consumption ranges from 350 mW to 400 mW. This represents a good low power consumption result in respect to the good timing measurement performance achieved by the TDC Card.

A. Timing precision

Timing precision, also called single-shot precision in TCSPC instruments, reveals the TDC card intrinsic timing jitter, i.e., the uncertainty in the conversion of a given time interval. This parameter is computed by repeatedly measuring a constant START-STOP delay, a large amount of times; the distribution of conversion results is then used to compute the standard deviation. This process is repeated multiple times, sweeping the START-STOP delay along the overall full scale range. Fig. 6 shows the measured precision at two different full scale ranges: a short 320 ns FSR tested at 100 ps delay steps; the longest FSR of 10 μs at 1.5 ns steps.

The TDC Card is capable of average precision of about 21 ps rms (i.e., about 49.5 ps FWHM, Full-Width at Half Maximum). These measurements also prove the correct operation of the CPLD range extension function, as the measured trend shows no errors or glitches at integer multiples of 160 ns.

B. Timing accuracy

Timing accuracy is the ability of a time interval meter to measure the exact time interval between START and STOP. Typically, most time measurement applications do not require the ability to measure the absolute START-STOP time difference; rather, what is usually needed is the exact time difference between START-STOP couples. We measured the accuracy of the TDC Card by exploiting a 10 ns reference clock split in two independent paths, each one gated by a random generator; the resulting couple of signals has a delay equal to a random integer multiple of 10 ns, which is fed as START and STOP to the TDC Card. After a large number of conversions, the obtained histogram is composed of independent peaks with 10 ns time difference. Fig. 7 shows such a measurement, with 320 ns full scale range, and proves the excellent accuracy: the average time difference between consecutive peaks is 9.9993 ns, with a sub ps variation due to the peak

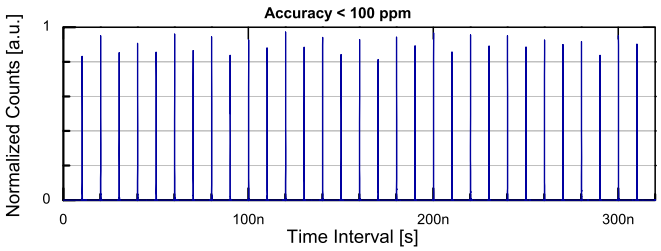

FIG. 7. TDC Card timing accuracy evaluated using a 10 ns reference clock and two random generators in order to obtain couples of START/STOP pulses having a delay equal to a random integer multiple of 10 ns. The resulting histogram shown peaks with an average distance of 9.9993 ns, resulting in a better than 100 ppm accuracy.

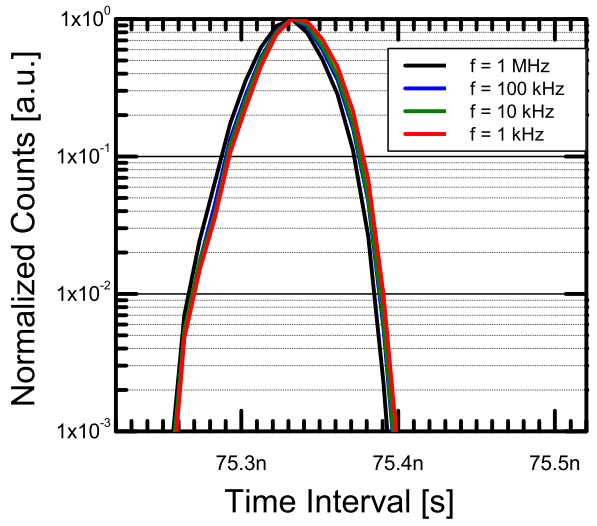

FIG. 8. Measurements of the same 75.33 ns time-interval, acquired after varying the START-STOP repetition rate from 1 kHz to 1 MHz. The mean distribution value changes by less than 1 LSB, from 75.33 to 75.336 ns, while the peak value remains always centered at 75.33 ns.

shapes, resulting in a better than 100 ppm accuracy. The same result was found when using the (longest) 10 μs full scale range.

In order to obtain an absolute START-STOP interval the intrinsic TDC Card time offset can be measured and subtracted. This is a deterministic value that arises from mismatches in the Card path layout and internal delays in the signal conditioning CPLD; in particular, these delays are dependent on the CPLD firmware. Typically, the TDC Card time offset is less than few ns.

We also investigated the impact of conversion rate on TDC performance. Fig. 8 shows the measurement of the same time interval when the START-STOP repetition rate changes by three decades, from 1 kHz to 1 MHz. The timing precision remains about 19 ps rms, the histogram peak value is 75.33 ns for each frequency, while the mean value varies from 75.33 ns to 75.336 ns, well less than 1 LSB.

C. Differential nonlinearity

Differential nonlinearity shows the bin value variation in respect to the nominal bin value. Good linearity performance is a fundamental requirement in advanced applications, such as TCSPC, which call for variations lower than few percent of the LSB in order to accurately reconstruct optical waveforms. We measured the DNL of the TDC Card by means of a code density test: a periodic STOP signal and an uniformly distributed random START signal (e.g., a single photon detector dark count) define randomly variable time intervals to be measured. Ideally, the histogram obtained by converting these time intervals is an uniform distribution; converter nonlinearity and non-uniform distribution of the random START signal result in deviations from such a flat histogram. In order to neglect the distribution non-uniformities and to see only converter nonlinearity, the measurement needs to accumulate a very large number of samples (at least 10 k conversion per histogram bin). The resulting histogram then reflects the TDC Card nonlinearity: Fig. 9 shows the measured DNL over the 320 ns full scale range, with a value of 9.5% LSB peak and 1.25% LSB rms. The higher nonlinearity in the first part of the converter range is due to crosstalk between START and STOP paths inside the signal conditioning CPLD, while the remaining portion reaches the same performance as the sole TDC chip. Also this measurement is free of glitches at integer multiples of 160 ns, confirming again the correct operation of the CPLD range extension function.

IV. CONCLUSIONS

We presented a very compact dimension (78 mm $\times$ 28 mm $\times$ 10 mm) TDC Card that provides high performance (less than 21 ps rms precision and DNL of 1.25% LSB rms, with a full scale range up to 10 μs) with low power consumption (less than 0.4 W). This card provides a simple I/O interface by means of an edge card connector for data readout and user selectable operation mode.

The TDC Card opens the way to easy integration of time measurements into many different systems and to develop multichannel timing instrumentation for many applications (including demanding TCSPC technique applications such as FLIM, FRET, FCS, and DOT) where very compact dimensions and many-channels working in parallel are needed.

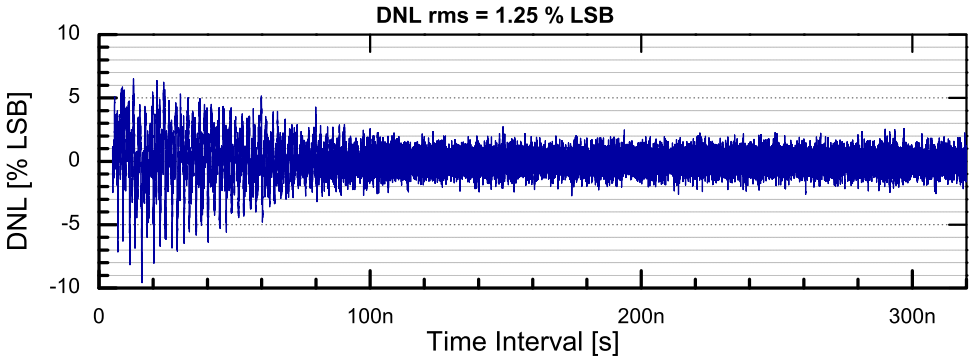

FIG. 9. TDC Card Differential Non-Linearity, measured through a code density test, by means of uncorrelated START and STOP pulses, resulting in uniformly distributed random time intervals. By accumulating a large number of samples for each bin, the resulting histogram reflects the TDC nonlinearity. As it can be seen, the DNL is always much better than 1.25.

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