New routing electronics for high performance TCSPC with SPAD arrays

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The analysis of very fast and faint light signals is increasingly widespread in many different fields, from chemistry to biology and from telemetry to communications. Among all the techniques, Time-Correlated Single Photon Counting (TCPSC) has been playing a central role for many years due to the achievable high temporal resolution. Nowadays many TCSPC applications, like Fluorescence Lifetime Imaging Microscopy (FLIM) or Förster Resonant Energy Transfer (FRET), are characterized by a strong demand in terms of number of acquisition channels in order to reduce the overall measurement time.

The recent developments of Single Photon Avalanche Diodes (SPAD) arrays are leading to the design of high density and high performance TCSPC systems. Nevertheless, there are several challenges that need to be faced during the design, like reduction of occupied area and power consumption.

For those reasons, state of the art TCSPC systems suffer from a trade-off between number of channels and performance: the higher the number of acquisition channels is, the poorer the performance are.

Considering the challenge of designing a TCSPC system with many channels, one strong limitation in increasing the number of detectors would be the maximum throughput affordable by the PC and therefore the maximum count rate would be fixed. In order to achieve low differential non linearity (few percent of LSB) and low jitter (less than 20 picoseconds), the best timing architecture is made up of a Time-to-Amplitude Converter (TAC) followed by an ADC. Considering a system with thousands of TACs, its throughput can reach several gigabytes per second, which are hard to be managed by an external PC. It's worth noting that in this case it's possible to reduce the number of TACs without impairing the detector count rate as long as the external PC is setting the main limitation. In this way, the area occupied and the power dissipated by the single TAC can be increased, thus helping the design of high performance converters.

We present the idea of new routing electronics enabling the realization of photon timing systems that can feature both a high number of acquisition channels (even thousands) and high performance.

The main feature of this router is that its logic can be dynamically reconfigured therefore each detector that has been hit by a photon can be fed to any of the TACs and low counting detectors are not masked by high counting ones. For this reason, each detector is assigned with a random read out priority and an arbitration mechanism draws the highest priority ones that will be routed to the TACs.

In order to have a scalable architecture, which allows future expansion of the detector array, each pixel has been coupled with an arbitration logic. In this way, each pixel do generate its own random read out probability and compare it with the other ones.

Finally, in order to understand which SPAD has to be routed, a shared decoder computes the detector positions from their read out priority and fed the TACs with their timing signals.

In conclusion, we present the first results of the design of new routing electronics. The development of these chips can lead to the design of innovative architectures for TCSPC measurement, featuring both a large number of channels and very high performances on each channel.