An Integrated Testbed with Single DC Source for Delivering Symmetrical Square-Wave Excitation Voltage in the Triple Pulse Test

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***Abstract*— While the conventional methods are based on sinusoidal excitations to parameterize the loss of magnetic components, recent studies have justified the characterization directly through large-signal, rectangular excitations, as are experienced in typical power electronics converters. The Triple Pulse Test (TPT) has been proposed previously for this purpose as a discontinuous procedure to characterize the high-frequency loss of magnetics. The excitation circuit used to deliver the TPT is advanced in this paper by removing the need for two external power supplies. Instead, a single power supply is connected to a voltage-offsetting input stage which uses a novel implementation of a half-bridge circuit to deliver a controllable offset between two capacitor banks. This dc-link offsetting circuit can compensate the asymmetric voltage drops on the power devices and delivers rectangular voltages with symmetric amplitude to form closed BH loops on the device under test. The aim is for the integrated testbed is to deliver the TPT autonomously, iterating over several operating points, to generate a loss map of one magnetic component. This testbed could subsequently aid the manufacturer of magnetics to shift from material-based datasheet to component-based, which will enable the end users to model high-frequency magnetics more easily and accurately.**

Keywords—triple pulse test, core loss, loss map, integrated testbed, voltage offset

I. Introduction

Due to the rapid rise in the use of switched power electronics devices, there has been increasing academic and industry interest in how to accurately model the efficiency of these systems. The active devices used in switched converters, such as MOSFETs and IGBTs, are well understood and parameterizable, e.g. through the Double Pulse Test [1]. However, the loss characteristics of magnetic devices (e.g. filter inductors) remain poorly parameterised under high-frequencies and rectangular excitation voltages used in power-converters.

Conventional practice for modelling the loss characteristics of magnetic components is to employ the Steinmetz's equation. The coefficients for this equation are provided by manufacturers, which are frequency dependant and based on sinusoidal excitations. There has been extensive research into how the currently employed Steinmetz equation can be adapted and improved to cater for arbitrary waveforms [2] [3] [4]. There remains however a fundamental limiting factor in that these coefficients are gathered by applying sinusoidal excitation to the magnetic components. In switched power-converters, magnetic components are exposed to square wave excitation with spectral content across a wide band of frequencies. As such, it is difficult to predict the characteristics of components under square wave excitation using the manufacturer provided frequency specific parameters.

More recently the academic community has turned to parameterising the loss characteristics of magnetic components empirically through applying square wave excitation as would be experienced in power electronics applications. One proposed method for generating a user-friendly loss map for magnetics components is the Triple Pulse Test (TPT) [5] [6]. This test is analogous to the Double Pulse Test (DPT) for parameterising switching devices. To deliver the TPT, a short burst of square wave pulses is applied to the magnetic component under test. The test only delivers enough pulses to allow the response of the magnetic device to stabilise, reducing the power supply demand for even very high-power operating points. By testing the component over a range of operating conditions, a complete, empirically measured, dataset for the loss characteristics of a given component can be obtained. The ultimate aim of the TPT is to change the way manufacturers provide characteristics for their magnetic components, allowing power-electronics engineers to design more efficient high-power switched converters.

As demonstrated in [5], it is vital in a TPT to deliver a symmetrical square-wave excitation voltage onto the device under test to retrieve meaningful results. However, the asymmetrical voltage drops on the excitation power devices poses a challenge to this objective. Extended from the nonideal solution in [5] and [6] utilizing two dc sources in series, this paper proposes and implements the addition of a digitally controllable voltage-offsetting stage at the input of the TPT excitation circuit to compensate the asymmetrical voltage drops. This circuit uses a novel implementation of a half-bridge configuration to create a voltage offset between two supply capacitor banks without interfering with measurements on the test side of the excitation circuit. The addition of this input stage aims to solve the voltage offset issue in the TPT excitation circuit without having to employ the use of external power supplies, hence creating a more integrated test platform. The newly implemented input stage is integrated with the existing TPT excitation circuit on a PCB mounted integrated testbed. This work aims to move the TPT closer to being adopted by manufacturers as an alternative, user-friendly way of collecting empirical magnetic component loss data, more applicable to the work of modern power-electronics engineers. A reference design is built and experimentally tested as proof of concept.

II. Triple Pulse Test and Voltage Drop Compensation Problem

A diagram of the TPT excitation circuit used in the paper proposing the practical TPT is shown in Fig. 1. Switches T_1 and T_2 are actuated to deliver the excitation voltage waveform. Where the TPT is being run with a DC bias in the

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inductor under test, only one of the switches is actuated. During the pulse where both switches are closed, the current in the inductor flows through the diode in parallel with each of the switches. This is preferable for the TPT as the effects of introducing deadtime between switches operating in complement with each other would degrade the accuracy of the test results. It is only possible to operate the excitation circuit in this fashion at operating points where the current in the inductor is completely unidirectional. Where the current in the inductor is bi-directional, both T_1 and T_2 have to be operated in a complementary fashion to provide a continuous current path.

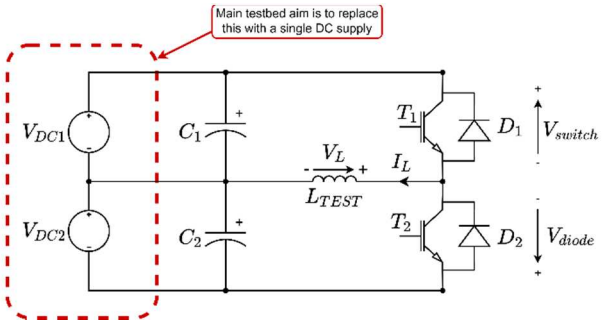

Fig. 1. Triple Pulse Test excitation circuit as used in [5] and [6]

To run a TPT, the excitation circuit needs to deliver a series of square wave voltage pulses that are symmetric around zero volts (i.e., have an average value of zero volts). To set up a DC bias in the inductor, an extended pulse is added to the start of the TPT pulse-train. An example of the shape of the TPT excitation waveform is shown in Fig. 2.

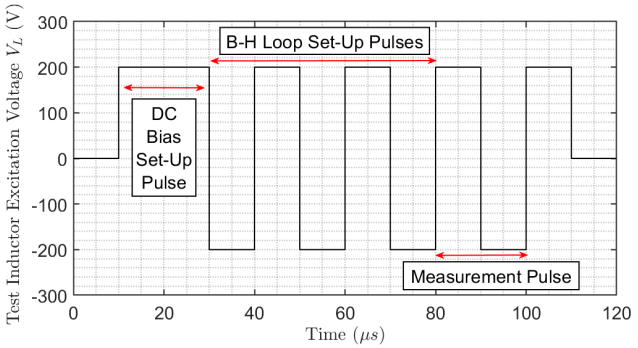

Fig. 2. Example TPT excitation waveform

Under the DC bias case, the problem of voltage asymmetry across the pulse train becomes apparent. Assuming the case where the inductor current is always positive, only T_1 in Fig. 1 would be actuating. During the positive pulse, the current path would be through the upper closed switch. During the negative pulse however, the current would be conducted through the lower diode D_2. This leads to an asymmetrical voltage drop between the positive and negative conduction paths. (1) and (2) describe the difference between the two voltage paths where V_{L+} and V_{L-} are the inductor voltage during the positive and negative pulses respectively.

$$V_{L+} = V_{DC2} - V_{switch} \quad (1)$$

$$V_{L-} = -(V_{DC1} + V_{diode}) \quad (2)$$

The issue with asymmetrical pulses is that the voltage driving current into the inductor under test would not be the same as the voltage driving the current back down again. The TPT finds the loss in the inductor by analysing the loop formed by plotting flux density B and magnetic field strength H against each other. When the voltage pulses for the TPT excitation are asymmetrical, the BH loop does not return to its starting point at the end of the measurement pulse as either energy still remains in the magnetic field of the inductor, or the energy in the magnetic field is lower than at the start of the test pulse. This energy difference is unaccounted for and hence read as part of the loss characteristic by TPT data analysis.

The temporary solution applied in the proposed TPT excitation circuit was to use two bench power supplies (V_{DC1} and V_{DC2} in Fig. 1) as shown in [6]. The voltage delivered by these supplies was manually adjusted until the pulses of the TPT were symmetrical around zero volts. The purpose of the voltage-offsetting circuit proposed in this paper is to negate the need for two external supplies, instead allowing the use of a single supply to the test circuit, with a voltage-offsetting stage to offset the voltages across the two input capacitors (C_1 and C_2 in Fig. 1).

III. The Input Voltage-Offsetting Circuit

A. Voltage-Offsetting Circuit Layout

The voltage-offsetting circuit uses two MOSFETs in a half bridge configuration. A choke inductor connects the midpoint of the two MOSFETs to the midpoint of the input capacitors for the TPT excitation circuit. A circuit diagram of the proposed input stage is shown in Fig. 3.

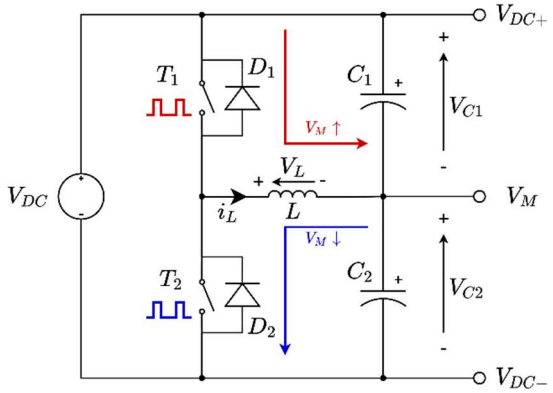

Fig. 3. Voltage-offsetting circuit layout

Without either of the switched being actuated, the voltage at the midpoint of the two capacitors holds at half the DC supply voltage, assuming the upper and lower capacitors are identical. The voltage across each of the capacitors can then be offset by actuating the voltage-offsetting switches with pulse width modulated (PWM) gate drive signals. How quicky the voltage transitions depend on the duty ratio of the PWM signal. Unlike in most switched power-electronics devices, the switching of these devices is not continuous. This is because once the voltage at the midpoint has reached the desired level, the output current of the half-bridge circuit becomes zero amps. The switches of the voltage-offsetting circuit are only actuated when the midpoint voltage needs to transition, otherwise they act as open circuits. This has numerous advantages. Firstly, assuming ideal components, the steady state power consumption of the circuit is zero watts, even if the voltage between the two capacitors is being held at an offset. In practice this is not quite the case at the voltage measurement circuit for closed loop control requires a small continuous current, and the capacitors and MOSFETs will

have a small leakage. Secondly, it means the voltage-offsetting circuit can be dissabled completely while the TPT is being run. This means the addition of the voltage-offsetting stage to the TPT excitation circuit has minimal impact on the TPT measurements.

Because the switching in the voltage-offsetting circuit is discontinuous, there is little purpose in actuating the switches in a complementary fashion. Instead, only one switch is actuated at a time with the reverse-conducting diode of the other switch providing the current path for the inductor during the PWM off time. This is in contrast to other power-electronics devices which actuate the switches in complement to reduce losses from conduction though a reverse diode as opposed to a closed switch. Actuating only one switch at a time simplifies the control requirements of the circuit and nullifies the possibility of shoot-though failure.

B. Voltage-Offsetting Circuit Control Scheme

The controller in this circuit changes the capacitor midpoint voltage by actuating one of the two MOSFETs using a PWM gate signal. To raise the capacitor midpoint voltage, the upper switch is actuated, allowing current to flow from the upper supply rail to the midpoint. This lowers the charge on the upper capacitor and increases the charge on the lower capacitor. To lower the capacitor voltage, the lower switch is actuated, allowing current to flow from the midpoint to the lower supply rail. This raises the charge on the upper capacitor and lowers the charge on the lower capacitor.

For the implementation in this paper, the voltage-offsetting circuit is controlled with the use of a closed control loop via a digital microcontroller. Voltage measurement transducers are connected across each of the capacitors to provide a feedback path for the control loop. The output from the microcontroller is the PWM gate driving signals for each of the MOSFETs. The control loop uses a single control output value with a maximum value saturating at the maximum duty ratio for the PWM gate signals, and a minimum value of minus the maximum duty as summarised in (3).

$$-\delta_{MAX} < Controller\ Output < \delta_{MAX} \tag{3}$$

When the controller output is positive, the magnitude of the output becomes the PWM duty ratio of the upper switch. Likewise, when the controller output is negative its magnitude becomes the PWM duty ratio of the lower switch. In this paper, only proportional control is used, though it could be beneficial to include integral control to reduce steady state error of the system.

C. Controlling Current in the Choke Inductor

Special care must be taken in the control of the voltage-offsetting circuit to ensure the current in the choke inductor does not build to dangerous levels. If the current in the inductor were to reach saturation point, its effective inductance would drop significantly leading to a current spike and possible damage to the conducting MOSFET. The most certain way to ensure the current in the inductor stays at safe levels is to have the current return to zero between PWM cycles. In switched power-electronics circuits this is often referred to as discontinuous conduction mode (or DCCM).

Current build-up in the choke inductor is manageable through restricting the maximum duty ratio for the gate signals of each of the MOSFETs. While the PWM signal is being applied, the current increase during the switching on-time, t_{on}, must be less than or equal to the current decrease during the switching off-time, t_{off}. Assuming the voltage is constant during one switching cycle, the change in current of the inductor over one on-cycle of the upper switch is given by (4). In this equation, V_M refers to the midpoint voltage relative to the DC supply and is synonymous with V_{C2}. The change in current over one off-cycle is given in (5).

$$\Delta i_{L+} = \delta T_{PWM} \cdot \frac{V_{DC} - V_M}{L} \tag{4}$$

$$\Delta i_{L-} = (1-\delta) T_{PWM} \cdot \frac{-V_M}{L} \tag{5}$$

To find an expression for the maximum duty ratio at which DCCM is maintained, Δi_{L+} must be equal to, or less than, $-\Delta i_{L-}$. The equation that results from combining (4) and (5) is shown in (6).

$$\delta_{MAX} = \frac{V_M}{V_{DC}} \tag{6}$$

This presents a limiting condition for the safe operation of the voltage-offsetting circuit. If the midpoint voltage drops to zero, the maximum allowable duty ratio becomes zero too, hence the circuit cannot operate. The issue is that the voltage over the inductor during t_{on} is the full DC supply voltage, but during t_{off} it becomes zero volts and hence the current in the choke inductor remains unchanged. To avoid this situation, the voltage-offsetting circuit must only operate within a range of midpoint voltages. With this condition in place, the maximum duty ratio for the voltage transition is given by (7), where ΔV_{MAX} is the maximum range of voltages the midpoint can take, centred around half the DC supply voltage.

$$\delta_{MAX} = \frac{V_{DC} - \Delta V_{MAX}}{2 \cdot V_{DC}} \tag{7}$$

Further to this, the maximum duty ratio must be limited so the current in the inductor does not rise too high within a single on cycle of the PWM gate signal. This limiting condition is summarised in (8) where i_{Lpk} is the maximum allowable current in the inductor.

$$\delta_{MAX} = \frac{2 \cdot i_{Lpk} \cdot L}{(V_{DC} + \Delta V_{MAX}) \cdot T_{PWM}} \tag{8}$$

To operate safely, without risking saturation of the choke inductor, the maximum duty ratio for the PWM gate drive signals for each of the MOSFETs must be limited to the minimum value of δ_{MAX} from both (7) and (8). This is summarised in (9). Fig. 4 shows the closed control loop.

$$\delta_{MAX} = \min\left(\frac{V_{DC} - \Delta V_{MAX}}{2 \cdot V_{DC}}, \frac{2 \cdot i_{Lpk} \cdot L}{(V_{DC} + \Delta V_{MAX}) \cdot T_{PWM}}\right) \tag{9}$$

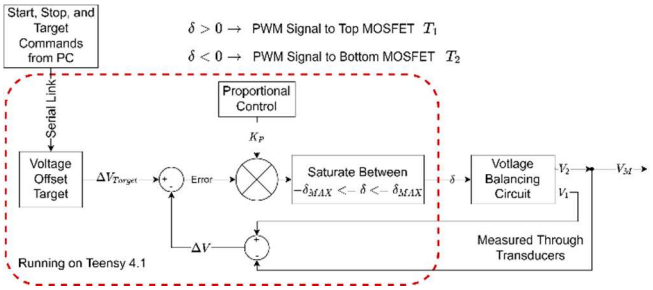

Fig. 4. Closed control loop implemented on the digital microcontroller

This diagram shows how proportional control is implemented in the voltage-offsetting circuit's closed control loop. A single controller is used for both upper and lower switches where a positive output indicates the upper switch should be actuated, and a negative output indicated the lower should be actuated. The red dashed area indicated the portion of the control loop running on a digital microcontroller. In the case of this testbed, a Teensy 4.1 controller was used.

IV. Practical Demonstaration of the Voltage-Offsetting Circuit

A. Midpoint Voltage Offsetting

This voltage-offsetting circuit has been integrated into a single, PCB mounted testbed for delivering the TPT. Fig. 5 shows this integrated testbed with the voltage-offsetting circuit highlighted. The instruments and control parameters used to gather the following data are shown in Table 1.

TABLE 1 INSTRUMENTS AND CONTROL PARAMETERS USED FOR VOLTAGE-OFFSETTING DEMONSTRATION

Power Supply	Rohde & Schwarz NGE100
Voltage Probe	Keysight N2140A
Digital Oscilloscope	Keysight DSOX1202G
Maximum Duty Ratio (δ_{MAX})	0.2
Proportional Control Factor	0.5

Fig. 5. TPT integrated testbed with new voltage-offsetting circuit included

To demonstrate the voltage-offsetting circuit's ability to offset the voltage across the testbed capacitor banks, the transition of the midpoint voltage-offsetting circuit was recorded as the controller target changed from three volts above half the supply voltage, to three volts below. The transition was also measured in the opposite direction to demonstrate the voltage-offsetting circuit's ability to both raise and lower the midpoint voltage. For the duration of this test the TPT excitation side of the circuit remained disabled. The resulting voltage traces are shown in Fig. 6 where V_1 and V_2 refer to the upper and lower capacitor bank voltages respectively. The midpoint voltage is the voltage across the lower capacitor bank, V_2.

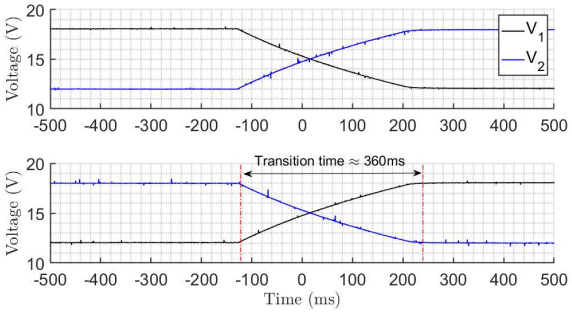

Fig. 6. Experimental demonstration of the voltage-offsetting circuit adjusting the capacitor voltages

The results from this demonstration show the voltage-offsetting circuits ability to transition the voltage midpoint of the testbed's capacitor banks quickly and accurately in both directions. They also show the voltage offset holding steady after the transition has taken place, with only minor noise from the switches intermittently adjusting the voltage which will slowly drift back towards half of the DC supply voltage.

While this confirms the testbed's ability to operate at low voltages, it also needs to cater for high voltage operation, as the TPT will often be run with supply voltages exceeding $200V$. In further experimentation, the testbed was observed operating with a supply voltage of $100V$ and $200V$. For these experiments, alternative measurement instrumentation was used. This instrumentation is listed in Table 2. The control parameters for the high voltage tests remained the same.

TABLE 2 INSTRUMENTS AND CONTROL PARAMETERS USED FOR VOLTAGE-OFFSETTING DEMONSTRATION AT HIGH VOLTAGE

Digital Electronics Power Supply	ISO Tech IPS2302A
High Voltage Power Supply	Elektro-Automatik 11 EA-PS 8360-15 T
Voltage Probe	Keysight N2862B
Digital Oscilloscope	Keysight DSOX1202G

For high voltage testing, the transition of the lower capacitor voltage (the midpoint voltage) was captured. The target was adjusted from six volts below half the DC supply voltage to six volts above it. The results from the high voltage test are shown in Fig. 7.

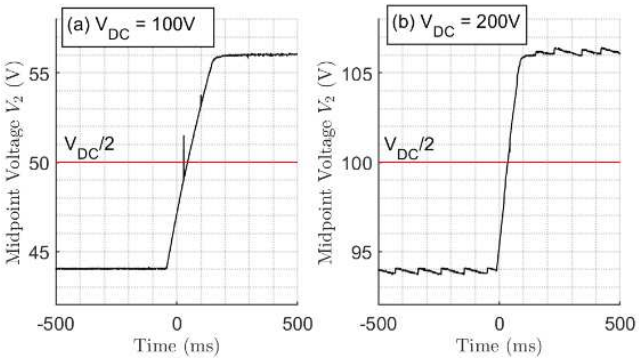

Fig. 7. Experimental demonstration of the voltage-offsetting circuit adjusting the low capacitor voltage with a $100V$ (a) and $200V$ (b) supply

The results in Fig. 7 show how the voltage-offsetting circuit is capable of accurately adjusting the testbed capacitor midpoint voltage up to at least $200V$. The transition take place marginally faster for the higher voltage supply as, with the same control parameters in use, the current in the inductor is allowed to build up higher. At the highest tested supply voltage of $200V$ a sawtooth shaped waveform appears over the non-transitional sections of the voltage trace. This is believed to be primarily caused by the switching of the high-voltage power supply, though the lower ADC resolution of the voltage-offsetting circuit's control loop at high supply voltage could also be a contributing factor.

B. Utilizing the Voltage-Offsetting Circuit to Compensate for Voltage Asymmetry in the Triple Pulse Test

The voltage-offsetting circuit was evaluated in conjunction with the TPT excitation circuit by running a TPT using the integrated testbed. As previously mentioned, the operating point under which the voltage asymmetry problem is most severe is where the inductor under test has a DC bias

current, and only one of the MOSFETs in the excitation circuit is actuated. Hence, to clearly demonstrate the efficacy of the voltage-offsetting circuit, a TPT was run with the parameters shown in Table 3. The inductor under test was a wound toroid of the material 3C90 from Ferroxcube with seven primary, and seven secondary windings. The theoretical inductance of this component was approximately 184µH. Fig. 8 shows how the scope was connected to the testbed to collect the data from this experiment.

TABLE 3 TEST PARAMETERS USED FOR THE TPT

DC Supply Voltage	$30V$
TPT Pulse Width	$6\mu s$
TPT DC bias setup pulse width	$16\mu s$

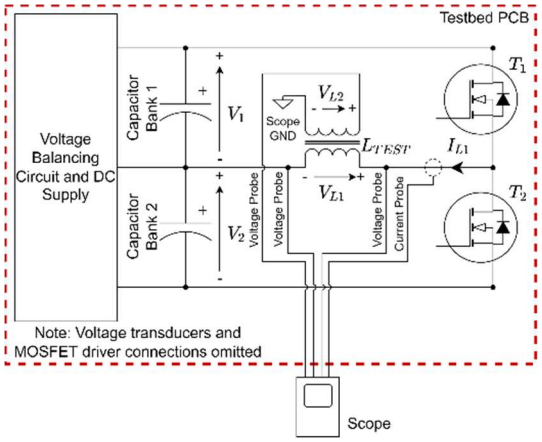

Fig. 8. Test probe layout for TPT experiments

Fig. 9 shows the results of the TPT without the voltage-offsetting circuit enabled (with the midpoint voltage half the DC supply voltage).

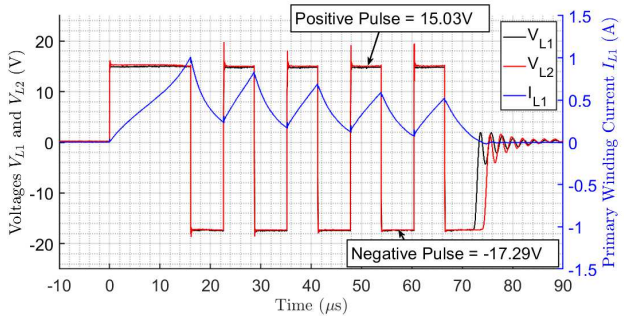

Fig. 9. TPT results from integrated testbed with voltage-offsetting disabled

As is indicated in Fig. 9, the voltage of the positive pulse is just over 2V lower in magnitude than the negative pulse. This is as expected, with the extra voltage on the negative pulse coming from the required forward voltage of the reverse conducting diode. The results also show how the average current in the inductor degrades significantly over the course of the TPT due to the voltage lowering the current being greater than the voltage driving the current up.

To apply compensation for this asymmetry using the voltage-offsetting circuit, the controller of the circuit is enabled and a target is found, by trial and improvement, to provide the most symmetrical TPT excitation waveform possible. To prevent the voltage-offsetting circuit interfering with the TPT measurements, the controller is dissabled, and both MOSFETs are set to open, 1µs ahead of the first TPT rising edge. The results of the TPT with the voltage-offsetting circuit compensation is shown in Fig. 10.

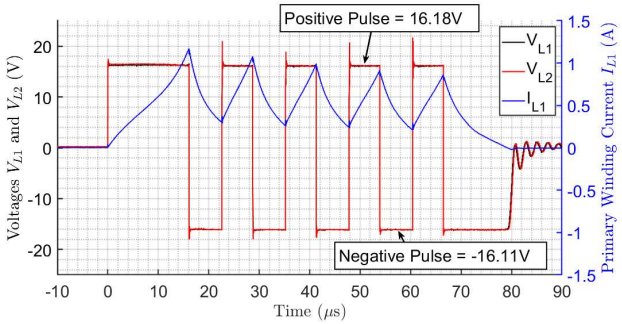

Fig. 10. TPT results from integrated testbed with voltage-offsetting enabled prior to test

The results clearly show the vast improvement in the symmetry of the TPT excitation waveform. The difference in magnitude between the positive and negative pulses is reduced from 2.26V down to 0.07V. The average current in the inductor also does not degrade as dramatically in the compensated test results. The marginal degradation is now mainly down to losses in the inductor itself.

To put the results of these two TPT experiments into context, the data collected was processed using TPT analysis software kindly provided by the authors of [5] and [6]. This analysis implements the calculations used in [5] to extract loss data from the captured waveforms. The output from the analysis software is a plot of the BH loop formed by the changing magnetic field strength and flux density over the course of the TPT measurement pulse (the third positive-negative cycle of the excitation waveform). The resulting plot from analysis of the TPT data is shown in Fig. 11.

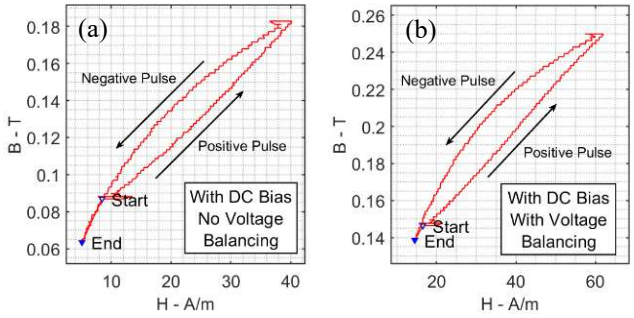

Fig. 11. TPT data output for (a) uncompensated and (b) compensated cases

The results show how with the uncompensated, non-symmetric TPT excitation, the resulting BH loop does not have the same start and finish point. Instead, the end point overshoots the start point during the discharging of the inductor (the negative part of the excitation waveform). The loss in the inductor is calculated from the area enclosed by the BH loop, hence in this case, the calculated loss would be lower than the true value due to the decreased enclosed are. By contrast, the BH loop from the compensated TPT excitation has the start and end points much closer together, providing vastly improved accuracy in the resulting loss calculations. It is also worth noting that the uncompensated BH loop occurs at lower values for both magnetic field strength and flux density, despite both tests having the same bias current set up in the first positive pulse of the TPT excitation. This is due to the increased average inductor current degradation for the

uncompensated case. Effectively, the uncompensated BH loop is at a lower inductor DC bias operating point than the compensated case.

V. Conclusion

This work has proposed an improved testbed for delivering the Triple Pulse Test (TPT) for characterising the losses in magnetic components. The key feature of the improved testbed is the addition of the input stage voltage-offsetting circuit. This circuit aims to solve the problem of asymmetry in the square wave excitation used in the TPT caused by the different current paths under DC biased conditions. The voltage-offsetting circuit archives a controllable offset between two capacitor banks in series by using a half-bridge configuration with a novel control scheme. The voltage-offsetting circuit can be fully disabled just before the TPT waveform is generated, hence removing the potential for interference with the TPT measurements.

A practical implementation of the integrated testbed was created in this work to demonstrate the voltage-offsetting circuit's ability to transition the voltage midpoint of two capacitor banks at varying supply voltages. The testbed was also used to deliver a TPT both with and without compensation from the input voltage-offsetting circuit. Finally, to put the gathered data into context, the measurements from the TPT's were processed using TPT analysis software to generate BH loops. The difference between the BH loops with and without compensation show how the voltage-offsetting circuit can be used to dramatically increase the accuracy of the TPT measurement by forming closed BH loops as a result of removing the asymmetry in the excitation voltage.

Further work on this integrated solution could see the TPT delivered iteratively in an automated manner. Instead of manually delivering the test, compensating by trial and error for the voltage asymmetry issue, the testbed could be issued instructions digitally to run the test repetitively at varying operating points. For each operating point the testbed could tune out any asymmetry though automated repetition and adjustment of the voltage-offsetting circuit to achieve the most accurate results possible. It is anticipated that this testbed can subsequently aid the manufacturer of magnetics to shift from material-based datasheet to component-based, which will enable the end users, e.g. power electronics engineers, to model high-frequency magnetics more easily and accurately.

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References

[1] Semikron, "Determining switching losses of SEMIKRON IGBT modules," 2014. [Online]. Available: https://www.semikron.com/dl/service-support/downloads/download/semikron-application-note-determining-switching-losses-of-semikron-igbt-modules-en-2014-08-19-rev-00/

[2] M. Albach, T. Durbaum and A. Brockmeyer, "Calculating core losses in transformers for arbitrary magnetizing currents a comparison of different approaches," PESC Record. 27th Annual IEEE Power Electronics Specialists Conference, 1996, pp. 1463-1468 vol.2

[3] Jieli Li, T. Abdallah and C. R. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248), 2001, pp. 2203-2210 vol.4

[4] K. Venkatachalam, C. R. Sullivan, T. Abdallah and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," 2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings., 2002, pp. 36-41

[5] J. Wang, K. J. Dagan, X. Yuan, W. Wang and P. H. Mellor, "A practical approach for core loss estimation of a high-current gapped inductor in PWM converters with a user-friendly loss map," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5697-5710, June 2019

[6] J. Wang, X. Yuan and N. Rasekh, "Triple Pulse Test (TPT) for characterizing power loss in magnetic components in analogous to Double Pulse Test (DPT) for power electronics devices," IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, 2020, pp. 4717-4724