Hysteresis-Free Nanosecond Pulsed Electrical Characterization of Top-Gated Graphene Transistors

Enrique A. Carrion, Andrey Y. Serov, Sharnali Islam, Ashkan Behnam, Akshay Malik, Feng Xiong, Massimiliano Bianchi, Roman Sordan and Eric Pop

***Abstract*— We measure top-gated graphene field-effect transistors (GFETs) with nanosecond-range pulsed gate and drain voltages. Due to high-κ dielectric or graphene imperfections, the drain current decreases by ∼10% over timescales of ∼10 μs, consistent with charge trapping mechanisms. The pulsed operation leads to hysteresis-free *I–V* characteristics that are studied with pulses as short as 75 and 150 ns at the drain and gate, respectively. The pulsed operation enables reliable extraction of GFET intrinsic transconductance and mobility values independent of sweep direction, which are up to a factor of two higher than those obtained from simple dc characterization. We also observe drain-bias-induced charge trapping effects at lateral fields greater than 0.1 V/μm. In addition, using modeling and capacitance–voltage measurements, we extract trap densities up to 10^{12} cm^{-2} in the top-gate dielectric (here Al_2O_3). This study illustrates important time- and field-dependent imperfections of top-gated GFETs with high-κ dielectrics, which must be carefully considered for future developments of this technology.**

***Index Terms*— Charge trapping, field-effect transistors (FETs), graphene, high-κ dielectric, hysteresis, mobility, nanosecond pulsed measurements.**

I. Introduction

GRAPHENE devices are promising candidates for nanoelectronics [1], [2] due to good electrical properties, such as high mobility [3] and high saturation velocity [4]. Other than carbon nanotubes (CNTs), graphene is the only material with intrinsic electron and hole mobilities that are both high (10 000 cm^{2}V^{-1}s^{-1} or higher) at room temperature *and equal*, due to symmetric conduction and valence energy bands. In contrast, transistor materials from Si and Ge to III–V compounds have a reasonably good electron mobility (up to 800 cm^{2}V^{-1}s^{-1} for Si electron inversion layers and 30 000 cm^{2}V^{-1}s^{-1} for InAs and InSb quantum wells), but hole mobility two to twenty times lower (200 cm^{2}V^{-1}s^{-1} for Si hole inversion layers and up to 1000 cm^{2}V^{-1}s^{-1} for strained InSb) [5].

In the past few years, practical circuits have been demonstrated using graphene field-effect transistors (GFETs), including amplifiers [6], [7], inverters [8], ring oscillators [9], radio-frequency mixers [10]–[12], and wafer-scale circuits [13]. However, depending on the high-permittivity (high-κ) top-gate dielectric used, the graphene–dielectric interface, and the testing conditions (e.g., air ambient versus vacuum), GFETs often exhibit characteristics that depend on the voltage sweep direction, i.e., hysteresis. The hysteresis shift can be defined as the difference in Dirac voltage (V_0) between forward (FWD) and reverse (REV) gate voltage sweeps ($\Delta V_0 = V_{0,\mathrm{FWD}} - V_{0,\mathrm{REV}}$), where V_0 is the gate voltage of minimum conductivity in the graphene channel, and can be considered analogous to the threshold voltage in traditional MOSFETs.

Hysteresis is primarily caused by charge trapping [14]–[16] at the graphene–dielectric interfaces and by ambient molecules (i.e., water and oxygen) in contact with the graphene surface [17]. The latter effect can be reduced or eliminated by measurements under vacuum conditions (∼10^{-5} torr) [15], [18] after an annealing step [18], [19]. However, trapping at the interfaces or within the bulk of the dielectrics surrounding the graphene channel is an inherent and challenging problem. Ultimately, such trapping causes device reliability and operation issues that translate to changes in carrier concentrations, and thus introduce uncertainties when extracting parameters of interest, including mobility, contact resistance, and transconductance. Similar threshold voltage instabilities had also been observed in the early years of silicon technology [20] and as recently as the last decade with the introduction of high-κ dielectrics and metal gate-stacks [21], [22]. Addressing such trapping and voltage instability issues is crucial for the continued development and accurate metrology of GFETs.

In this paper, we investigate the effect of pulsed current–voltage (*I–V*) measurements on the hysteresis and extracted parameters (such as mobility) of top-gated GFETs.

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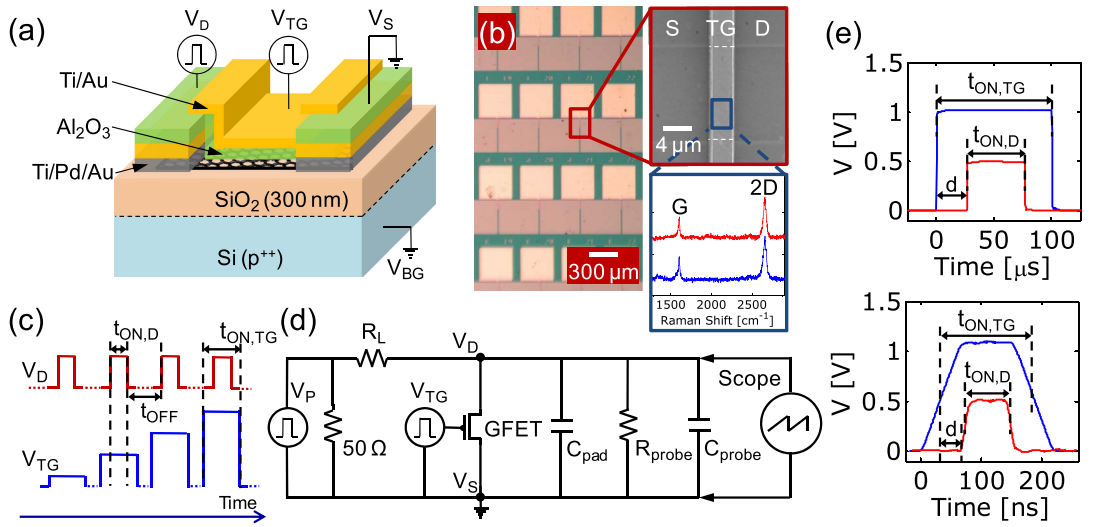

Fig. 1. (a) Schematic diagram of top-gated GFETs fabricated in this paper. (b) Optical and SEM images as well as Raman spectra of typical devices. (c) Schematic diagram of pulses and biases applied at top-gate (V_{TG}) and drain (V_D) terminals. The amplitude of V_{TG} is increased when performing a gate sweep of the voltage. (d) Diagram of a circuit used to apply voltage pulses at drain and gate terminals. Current is calculated from the voltage drops across the load resistor ($R_L = 0.5 - 1.5$ kΩ), GFET, probe resistance ($R_{probe} = 100$ kΩ), and pad ($C_{pad} = 8.3$ pF) and probe capacitances ($C_{probe} = 0.8$ pF). (e) Measured drain and top-gate pulses—top gate scope connection not shown in (d)—with $t_{ON,TG} = 100$ μs and $t_{ON,D} = 50$ μs (top) and $t_{ON,TG} = 150$ ns and $t_{ON,D} = 75$ ns (bottom). In both cases, V_D has a delay $d = t_{ON,D}/2$ relative to V_{TG}. In addition, $V_{TG} = 1$ V and $V_D = 0.5$ V.

Submicrosecond pulsed output characteristics of top-gated exfoliated graphene FETs [23] and micro- to millisecond pulsed transfer characteristics of back-gated FETs were reported in [14], [15] and [17] (sweep rates used in [17] range from 0.19 to 4.18 V/s), the latter only probing trapping at the graphene–SiO_2 interface. Here, we use graphene grown by large-scale chemical vapor deposition (CVD) and examine the gate and drain effects of reducing drain and gate pulse widths down to 75 and 150 ns, respectively (over 5× smaller than the shortest pulses investigated in [23]). We uncover two apparent trapping time constants of approximately 0.3 and 4.2 μs, ostensibly due to imperfections in the top-gate high-κ dielectric (Al_2O_3), its interface (oxidized Al seeding layer), or the graphene itself. Hysteresis is greatly reduced when using nanosecond voltage pulses at the drain and gate terminals, effectively limiting the time over which charge trapping can occur. The extracted mobility is independent of sweep direction and up to a factor of two higher than if dc measurements were simply employed. The approach described here leads to reliable characterization of GFETs, even in the face of imperfect dielectrics and interfaces.

II. Device Fabrication and Measurement Setup

Graphene is grown on copper foils similarly to [8], [24], using CVD with a methane/hydrogen mixture as precursor gases. It is then transferred onto SiO_2(300 nm)/Si substrates using a dual stack of poly(methyl methacrylate) (PMMA) for support and protection (60 nm of 495 A2 and 250 nm of 950 A4). PMMA is removed using a 1:1 solution of methane dichloride and methanol, followed by a H_2/Ar anneal (2 h at 400 °C) [25]. Next, Ti/Pd/Au (0.7/20/20 nm) source/drain electrodes are fabricated using UV lithography and e-beam evaporation, followed by O_2-plasma channel definition and atomic layer deposition (ALD) of $t_{ox} \approx 20$ nm of Al_2O_3 (seeded by 1.5 nm of evaporated and oxidized Al). Finally, a Ti/Au (0.7/20 nm) top gate with a gate–source/drain overlap of ∼150 nm is fabricated using e-beam lithography. Channel dimensions (L and W) range from 2 to 10 μm.

Figs. 1(a) and (b) show the schematic, optical, and scanning electron microscope (SEM) images of completed devices. Raman spectra taken after transfer [inset of Fig. 1(b)] indicate that graphene is monolayer (2D-peak to G-peak integrated intensity ratio $I_{2D}/I_G \approx 2$) and with D-peak to G-peak integrated intensity ratio $I_D/I_G \approx 0.25 \pm 0.15$ [26]. From the I_D/I_G ratio, we estimate [27] an average distance between Raman-active defects to be $L_a \approx 250 \pm 150$ nm. Considering micrometer-scale device dimensions used here, we expect the presence of defects and grain boundaries within the channel [28], and thus lower mobilities than those of exfoliated (single crystal) graphene devices [4].

During measurements, we apply voltage pulses (V_P) at the drain while increasing the amplitude of voltage pulses at the top gate (V_{TG}), as shown in Fig. 1(c) and (d). The V_D pulse is applied after the rising (t_R) edge and removed before the falling (t_F) edges of V_{TG}, since gate pulse edges cause a small resonance on V_D, especially at larger amplitudes (i.e., $V_{TG} > 2$ V) and shorter edges ($t_R = t_F < 500$ ns). Hence, the full-width at half-maximum of V_{TG} is twice that of V_D ($t_{ON,TG} = 2 \cdot t_{ON,D}$), and a delay relative to V_{TG} ($d = t_{ON,D}/2$) is half the width of V_D [Fig. 1(e)]. We find that these two constraints maximize signal integrity. The rise (t_R) and fall (t_F) times of gate or drain pulses vary depending on their width (i.e., $t_R = t_F = 10$ ns for $t_{ON,D} = 75$ ns and $t_R = t_F = 20 - 50$ ns for $t_{ON,TG} = 150$ ns).

The OFF-state relaxation time between drain pulses (t_{OFF}) ranges between 0.1 and 1 ms, which is 3–4 orders of magnitude larger than the shortest $t_{ON,D}$ applied (75 ns). These OFF-times were found to be sufficiently long to relax all

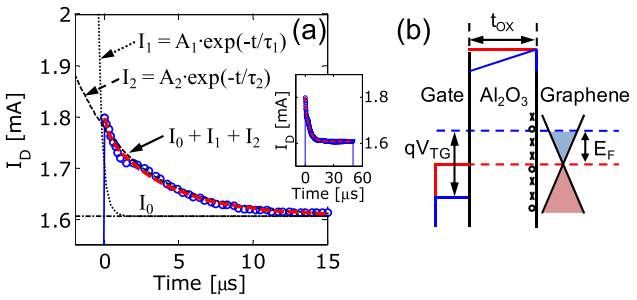

Fig. 2. (a) Measured drain current I_D (blue circles) during the first 15 μs of a typical 50-μs pulse (V_D = 1.9 V, V_{TG} = 0.5 V). Inset shows the same data set, zoomed out for the entire 50 μs. Device measured in air ambient ($L \times W = 2 \times 10$ μm). Transient behavior is due to the population of interface and bulk oxide charge traps. Current is fitted (red dashed lines) with $I_D(t) = I_0 + A_1 \cdot \exp(-t/\tau_1) + A_2 \cdot \exp(-t/\tau_2)$. Exponential terms are shifted by I_0 and shown by black dashed and dotted lines. Fitting parameters are I_0 = 1.6 mA, A_1 = 0.03 mA, and A_2 = 0.16 mA, with two time constants τ_1 = 0.3 μs and τ_2 = 4.2 μs. (b) Schematic band diagram of the metal–oxide–graphene device showing population of interface traps as the graphene Fermi level (dashed) changes. Interface states could act as either hole (circles) or electron (x-symbols) traps.

measurable effects of charge trapping from our short pulses. Larger relaxation times (up to the range of seconds) have been used while studying trapping at the graphene/SiO_2 [14]–[17] and CNT/SiO_2 [29] interfaces. In contrast, our analysis attempts to study and control trapping using nanosecond-range top-gate pulses ($t_{ON,TG}$), effectively limiting the amount of carriers than can become trapped instead of increasing detrapping via longer OFF-state relaxation.

To measure pulsed I–V characteristics, we employ a pulse generator, a 1.5-GHz oscilloscope, an active probe, and a simple voltage divider circuit in our setup [Fig. 1(d)]. For each top-gate pulse (V_{TG}), a corresponding voltage pulse is applied to a load resistor (R_L), such that after subtracting its voltage drop (V_{RL}), a pulse of amplitude V_D is applied to the GFET ($V_D = V_P - V_{RL}$). For I_D–V_{TG} measurements, the amplitude of V_D is kept the same throughout the measurement by adjusting the amplitude of the pulse V_P at each V_{TG} bias through a feedback loop (since V_{RL} changes with the bias-dependent resistance of the device). Every recorded V_D waveform (at a given V_{TG}) is an average over 200 applied pulses. The time dependence of the drain current $I_D(t)$ is obtained from the voltage drops across the load resistor (R_L) and a 50-Ω matching resistor (in parallel with the 50-Ω output impedance of the pulse generator), the GFET, the active probe resistance (R_{probe}), and pad (C_{pad}) and probe capacitances (C_{probe}), such that

$$I_D(t) = \frac{V_P(t) - V_D(t)}{R_L + 25\ \Omega} - \frac{V_D(t)}{R_{probe}} - (C_{pad} + C_{probe}) \times \frac{dV_D(t)}{dt}. \quad (1)$$

III. Results of Pulsed Measurements

With this setup, we first look at the typical transient behavior of current [Fig. 2(a)] when $t_{ON,D}$ = 50 μs pulses are applied at the drain terminal. I_D reaches the steady state with ~10% degradation after ~10 μs due to the effect of charge traps at this particular bias condition. This drop-off is faster than those mentioned in [14] and [17], which studied charge trapping at back gates with much thicker amorphous SiO_2 layers. The best fit of $I_D(t)$ is obtained using two decaying exponentials of the form $A \cdot \exp(-t/\tau)$ (black dashed lines), yielding time constants τ_1 = 0.3 μs and τ_2 = 4.2 μs. These suggest the presence of at least two trapping mechanisms, such as interface and bulk trapping [23], [30], [31]. Interface trap response times scale exponentially with their energy difference from either the valence or the conduction bands of a typical channel material [30]. Since graphene does not have a band gap and trap states can be located across a wide range of energies [Fig. 2(b)], interface traps can be rapidly filled when the energy of carriers is higher than that of electron (x-symbols) or hole traps (circles). On the other hand, bulk trap response times depend on tunneling through the oxide, and thus they are expected to be slower. In our case, the oxidized Al seeding layer (AlO_x) and graphene imperfections (i.e., grain boundaries) could be responsible for contributions to interface trapping, while the ALD-grown Al_2O_3 contributes to bulk trapping. Nevertheless, a simple tunneling front model [29] analysis reveals that such traps are likely less than ~1 nm apart in the Al_2O_3, making it challenging to ascertain their exact physical origin, which could be the topic of a future investigation.

We note that the time constants identified here (0.3 and 4.2 μs) are not originated from circuit transients, as circuit RC time constants due to R_L, R_{GFET}, R_{probe}, C_{pad}, and C_{probe} are ~10 ns. However, thermal time constants of top-gated GFETs with similar geometry are of the order ~100 ns [32]; thus, it is possible that the shorter time constant found here (τ_1 = 0.3 μs) can include a small thermal self-heating transient, which can also influence current degradation (although we note that our pulsed measurements were done at relatively low current density, ~0.1 mA/μm, except those in Section VI).

The effect of trap filling on electrical measurements can also be observed in Fig. 3(a), where the dc transfer characteristics of a typical top-gated GFET ($L \times W = 2 \times 10$ μm) show Dirac voltage shift and hysteresis (ΔV_0) in air and vacuum measurements. Charge trapping (or detrapping) is less likely to occur at the bottom graphene/SiO_2 interface when we vary V_{TG}, as the voltage drop between the graphene and back gate is small (V_{BG} = 0 V). The presence of hysteresis in both air and vacuum suggests that ambient adsorbates (i.e., O_2 and H_2O) and the top dielectric trapping (interface and bulk) contribute to the change in carrier density in the channel, while the dc top-gate voltage is swept [14], [15]. Thus, to minimize such V_0 instabilities, we perform pulsed measurements as described above. For each V_{TG} bias, I_D is calculated as a function of time using (1) and its amplitude is averaged over the duration ($t_{ON,D}$) of each drain pulse. Fig. 3(b) shows the in-air transfer characteristics for different V_{TG} ON-times ($t_{ON,TG}$) and compares them with simple dc I–Vs using the same bias conditions (V_D = 0.5 V and V_{BG} = 0 V). As $t_{ON,TG}$ is decreased from 100 μs to 400 ns, FWD and REV sweeps collapse onto one another and hysteresis ΔV_0

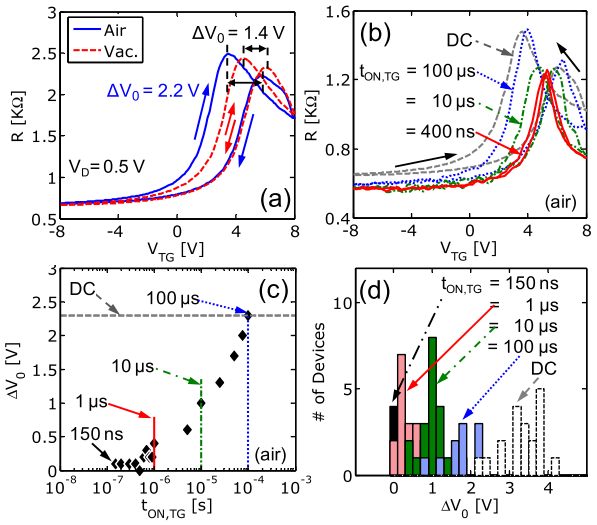

Fig. 3. (a) Hysteresis in dc measurement of resistance (R) versus top-gate voltage (V_{TG}) of a typical device ($L \times W = 4 \times 8$ μm) in air (blue-solid) and in vacuum (red-dashed). Arrows indicate sweep directions (from -8 to $+8$ V and back). Hysteresis is $\Delta V_0 = 2.2$ and 1.4 V in air and vacuum, respectively ($V_D = 0.5$ V). (b) Typical $R - V_{\mathrm{TG}}$ characteristics of another device measured in air under dc (dashed lines) and pulsed conditions. Note the suppression of hysteresis between FWD and REV sweeps as $t_{\mathrm{ON,TG}}$ decreases to 400 ns ($L \times W = 2 \times 10$ μm). (c) Measured shift in Dirac voltage (ΔV_0) from (b) as a function of $t_{\mathrm{ON,TG}}$. ΔV_0 is marked (lines and arrows) at five selected testing conditions: $t_{\mathrm{ON,TG}} = 0.15$, 1, 10, 100 μs, and dc. (d) Histogram of ΔV_0 for 20 devices measured at same five testing conditions: $t_{\mathrm{ON,TG}} = 0.15$, 1, 10, 100 μs, and dc. Note that not all devices were tested for each case.

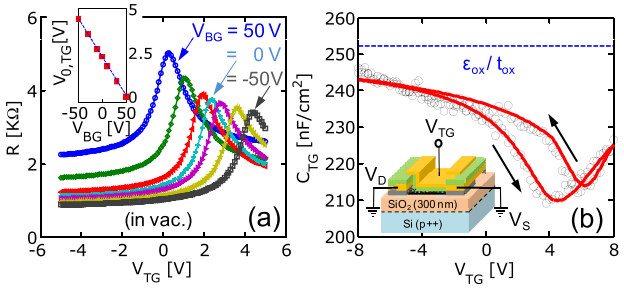

Fig. 4. (a) DC $R - V_{\mathrm{TG}}$ for different V_{BG} values ($L \times W = 5 \times 5$ μm, $V_D = 0.1$ V for only FWD sweep is shown). Inset: $V_{0,TG}$ versus V_{BG}. The slope represents the ratio between top and back-gate oxide capacitances ($C_{\mathrm{ox}}/C_{\mathrm{BG}} \approx 22$). (b) Measured top-gate capacitance at 100 kHz (C_{TG}, circles) and calculated (red solid line) using model described in the text. Expected value from simpler extraction in (a) is also shown (dashed line). Inset shows schematic diagram of measurement. V_{TG} is applied to top gate, source/drain are grounded, and back gate is left disconnected. Side-wall and overlap capacitances that appear in parallel with C_{TG} were measured in similar FET structures without graphene, and subtracted from the result.

disappears. In Fig. 3(c), the corresponding ΔV_0 is shown as a function of $t_{\mathrm{ON,TG}}$ down to 150 ns; we note that for dc I–Vs, $\Delta V_0 = 2.3$ V, while for $t_{\mathrm{ON,TG}} < 500$ ns hysteresis ΔV_0 approaches 0 V. This ΔV_0 reduction was observed across 20 devices ($L, W = 2$–10 μm) [Fig. 3(d)] for five testing conditions: $t_{\mathrm{ON,TG}} = 0.15$, 1, 10, 100 μs, and dc. We attribute the broadening of each distribution (corresponding to each $t_{\mathrm{ON,TG}}$ case) to device-to-device variations, i.e., graphene or dielectric interface quality and contact resistance.

The transfer characteristics shown in Fig. 3(b) are consistent with the presence of negative charges in the oxide. The fixed negative charges can be present in Al_2O_3 imperfections [33], and are apparent since $V_0 > 0$ V for all measurements (dc and pulsed) and sweep directions (FWD and REV). The occupied trapped states, responsible for Dirac voltage shift (ΔV_0) and hysteresis, depend on pulse duration; shorter pulses limit the electrical stress time over which carriers can become trapped. We also observe that the (unified) Dirac voltage of the 400-ns pulsed sweep falls between that of the FWD and REV dc sweeps. These differences in V_0 are consistent with hole traps charging up in the oxide (making it less negative) when V_{TG} is swept FWD starting in the hole region ($V_{\mathrm{TG}} < V_0$), and with electron traps accumulating during the REV sweep in the electron region ($V_{\mathrm{TG}} > V_0$) (making the oxide more negative). These additional trapped states in the oxide also contribute to the apparent variation of the channel resistance at V_0 in dc sweeps by increasing the charge puddle density (i.e., increasing impurity or minimum carrier densities in the channel) [4]. In contrast, when using short pulses (< 1 μs), less trapped states are disturbed, and V_0 and $R(V_{\mathrm{TG}} = V_0)$ remain constant independent of sweep direction.

IV. Gate Capacitance and Trap Charging Effects

To estimate quantitatively oxide trapped charge densities responsible for hysteresis, we examine capacitance through measurements and modeling. First, we estimate the top dielectric capacitance, as suggested in [34], by measuring the top-gate Dirac voltage ($V_{0,\ \mathrm{TG}}$) shift as a function of V_{BG}, in vacuum. As shown in Fig. 4(a), this yields the ratio between the top- and back-gate oxide capacitance, $C_{\mathrm{ox}}/C_{\mathrm{BG}} \approx 22$, which gives $C_{\mathrm{ox}} \approx 250$ nF/cm^2 and $\varepsilon_{\mathrm{ox}} \approx 5.7$ for our top Al_2O_3 dielectric with oxidized Al seeding layer. Next, we measure C–V characteristics [Fig. 4(b)] by applying dc and ac voltages to the top-gate terminal with an *LCR* meter. Away from the Dirac voltage, C_{TG} approaches the previously estimated top-layer capacitance ($C_{\mathrm{ox}} = \varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}}$), while near V_0, it decreases and exhibits hysteresis similar to that observed in the I–V measurements (Fig. 3; C–V and I–V measurements used similar voltage sweep rates, $\sim$1.6 V/s.)

To estimate trapped charge densities in the top-gate dielectric quantitatively, we fit a C-V model by applying Gauss' law to our structure

$$V_{\mathrm{TG}} - \left[V_0 + \frac{Q_{\mathrm{it}}\,(E_F = 0)}{C_{\mathrm{TG}}}\right] = -\frac{[Q_n\,(E_F) + Q_{\mathrm{it}}\,(E_F)]}{C_{\mathrm{TG}}} + \frac{E_F}{q} \tag{2}$$

where E_F is the Fermi level in graphene [Fig. 2(b)], Q_n is the charge density in graphene, and Q_{it} is the sum of trapped charge accumulated at the AlO_x/graphene interface and Al_2O_3 bulk. Quantum capacitance (C_q) is included in our model explicitly in the carrier density [$Q_n(E_F)$] calculation by integrating over the density of states. The total capacitance (C_{TG}) is calculated [Fig. 4(b)] as a derivative of the total charge ($Q_{\mathrm{TG}} = Q_n + Q_{\mathrm{it}}$) to the gate voltage by varying

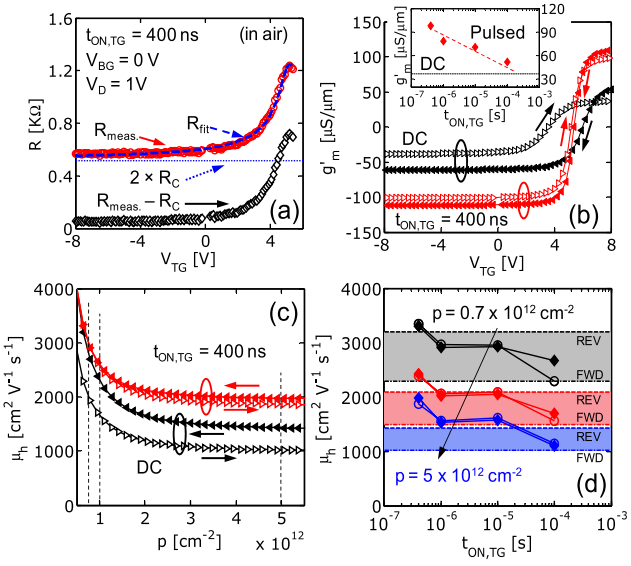

Fig. 5. (a) Hole R–$V_{\rm TG}$ measured ($R_{\rm meas}$), fitted ($R_{\rm fit}$) as in [35], and with contact resistance (R_C) subtracted ($R_{\rm meas} - R_C$). (b) Intrinsic transconductance (g_m') from Fig. 3(b), as a function of $V_{\rm TG}$ from pulsed (red) ($t_{\rm ON,TG} = 400$ ns) and dc (black) measurements. Arrows indicate direction (FWD or REV) of sweep. Inset shows maximum $|g_m{}'|$ (from FWD sweeps) as a function of gate ON-times. (c) Extracted hole mobility as a function of carrier density (p) from Fig. 5(b). (d) Hole mobility versus $t_{\rm ON,TG}$ for different $p = 0.7$ (black), 1 (red), and 5×10^{12} cm^{-2} (blue). Values extracted from Fig. 5(c) at the marked (vertical dashed lines) concentrations. Open circles and solid diamonds are from FWD and REV pulsed sweeps, respectively. Values extracted from dc FWD and REV sweeps mark limits of shaded regions. Note large mobility uncertainty of dc sweeps (up to ~1000 cm^{2}V^{-1}s^{-1} or ~30%) compared with pulsed sweeps (~50 cm^{2}V^{1}s^1 or ~2 %).

E_F, such that

$$C_{\rm TG} = \left(\frac{\partial Q_{\rm TG}}{\partial E_F}\right)\left(\frac{\partial V_{\rm TG}}{\partial E_F}\right)^{-1}. \qquad (3)$$

From this model, we estimate (negatively charged) trap densities of 7.2×10^{11} and 10^{12} cm^{-2} for the FWD and REV sweeps, respectively, at $E_F = 0$ eV (Dirac point).

V. Pulsed Mobility Extraction

Next, we extract device transconductance (g_m) and effective hole mobilities (μ_h) from pulsed and dc measurements [Fig. 3(b)]. We do so by first fitting a transport model ($R_{\rm fit}$) [4], [35], which includes contact resistance ($R_C \approx 2-3$ kΩ · μm), to the measured I_D–$V_{\rm TG}$ characteristics ($R_{\rm meas}$), as shown in Fig. 5(a). Fig. 5(b) then shows the intrinsic transconductance $g_m{}'$ (calculated after R_C is subtracted) derived from 400-ns pulsed measurements (red) and dc measurements (black) for FWD and REV sweep directions. We note that $g_m{}'$ changes sign as $V_{\rm TG}$ is swept past the Dirac point (i.e., threshold voltage) and carrier transport changes from holes to electrons. In addition, hysteresis is greatly reduced with 400-ns pulses compared with the dc measurement. Furthermore, the maximum value of $g_m{}'$ for pulsed measurements (~100 μS/μm) is approximately twice as high as the one obtained from dc measurements (~50 μS/μm). This trend is evident from the inset of Fig. 5(b),

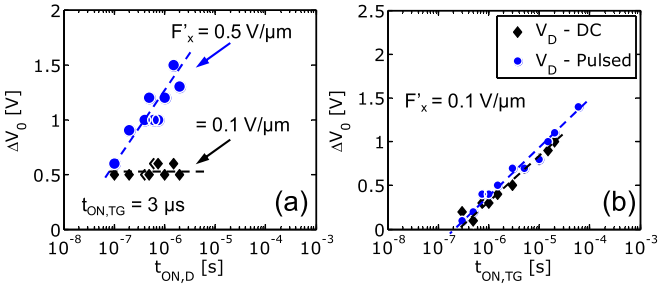

Fig. 6. (a) Dirac voltage shift (ΔV_0) as a function of drain ON-time ($t_{\rm ON,D} = 100$ ns–2 μs and $t_{\rm ON,TG} = 3$ μs). The $V_{\rm TG}$ sweeps (not shown) are from −8 to 8 V and back to −8 V, while V_D is increased from 1 (black diamonds) to 3 V (blue circles). V_D values correspond to intrinsic lateral fields $F_x' \approx 0.1$ and 0.5 V/μm, respectively, after contact resistance is subtracted ($L \times W = 3 \times 9$ μm). (b) ΔV_0 versus $t_{\rm ON,TG}$ (300 ns–80 μs). The drain terminal is biased using a dc (diamonds) and pulsed bias (circles) ($F_x' = 0.1$ V/μm and $t_{\rm ON,D} = 0.5 \cdot t_{\rm ON,TG}$).

which shows the maximum $g_m{}'$ (from FWD sweep) as a function of gate ON-time.

In Fig. 5(c), we show the effective mobility calculated as in [4] and [35]. We note that mobility values are approximate since R_C is fitted and not directly measured, and a constant $C_{\rm ox}$ was used to simplify the extraction procedure. Nevertheless, this exercise illustrates the consistency and reliability of pulsed characterization versus dc measurements. We show hole mobility (μ_h) versus carrier density for 400-ns pulses (red) and dc measurements (black), from FWD and REV sweeps. Pulsed measurements generate higher and consistent mobility values, due to reduced charge trapping. Conversely, mobility appears to be a function of sweep direction (marked with arrows) when obtained from dc I–V measurements. We note that self-heating effects do not play a role because the mobility estimates are all done at low lateral field and low current levels, ~0.06 mA/μm, where the maximum temperature rise is at most 5 K for our GFETs [4], [32], even for the dc measurements.

Subsequently, we examine mobility dependence on $t_{\rm ON,TG}$. Fig. 5(d) shows μ_h at three carrier densities: 0.7, 1, and 5×10^{12} cm^{-2}; open circles and solid diamonds represent values from FWD and REV sweeps. The mobility range from dc measurements (top and bottom lines of shaded regions) has an uncertainty up to 1000 cm^{2}V^{-1}s^{-1} (or ~30%), while for pulsed characterization, this uncertainty is significantly smaller (~50 cm^{2}V^{-1}s^{-1} or ~2%). Once again, we note that mobility is higher at shorter pulses, due to the minimized trapped charge.

VI. High Field Effects

We also briefly examine the effects of high lateral intrinsic fields $F_x{}'$ (after subtracting R_C) on ΔV_0 using our nanosecond pulsed technique. First, we find that for $F_x' \sim 0.1$ V/μm and a constant $t_{\rm ON,TG}$ (3 μs), ΔV_0 remains constant as we decrease $t_{\rm ON,D}$ from 2 μs down to 100 ns [Fig. 6(a)]. Conversely, when we raise $F_x{}'$ to 0.5 V/μm, ΔV_0 drastically increases as well. This increased ΔV_0 caused by higher F_x' occurs when hot carriers in the channel begin to fill interface or bulk trap states of the dielectric [23]. Finally, we examine ΔV_0 as we decrease

$t_{ON,TG}$ and replace the pulse generator at the drain terminal with a regular dc supply. We find that, at low $F_x{}'$, ΔV_0 is equally suppressed using a pulsed or a dc voltage at the drain terminal [Fig. 6(b)].

In general, GFET hysteresis is a function of the amount of trapped charge at the interface and bulk of the dielectric (Q_{it}), which in turn affects the overall charge in the channel, capacitance, and ultimately I–V results. In addition, Q_{it} is a function of frequency, gate voltage (V_{TG} or V_{BG}), and intrinsic lateral field (F_x'). Thus, to eliminate hysteresis and Dirac voltage instabilities during measurements, one should consider these dependencies and bias devices accordingly.

VII. Conclusion

In conclusion, intrinsic properties of GFETs can be probed with pulsed operation and pulses shorter than the trapping time constants of interface and bulk trapping. We also report transfer characteristics, transconductance, and mobility values that do not depend on voltage sweep direction (FWD or REV) or rate. Such results correctly represent the intrinsic properties of the GFET channel, as detrimental effects from oxide and interface traps (hysteresis and I_D degradation) can be greatly reduced. Finally, we show that high lateral fields can affect hysteresis and charge trapping through hot-carrier injection, a situation that can also be mitigated using short drain ON-times. All of these findings shed light on careful ways to characterize graphene devices and reduce detrimental effects using pulsed measurements, which is important for future advancement of graphene device technology.

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