Working Principles of a DRAM Cell Based on Gated-Thyristor Bistability

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I. Introduction

THE possibility to exploit thyristor action to achieve high-performance next-generation DRAM cells has been recently investigated with many device proposals, considering both physical [1], [2] and virtual [3]–[5] thyristor structures either with one [1], [2], [4] or two gates [3]. Key benefits of all of the proposed solutions appear to be a simple process and fast write and read operations with low voltage requirements. However, for a solid assessment of both the performance and the prospects of these new device structures, a comprehensive and clear understanding of their operation is needed, starting from their basic-physics.

In this letter, we provide a detailed discussion of the basic physics and the working principles of the T-RAM cell [1], [2], representing a volatile memory device exploiting the bistability of a physical single-gate nanoscale thyristor to target DRAM applications. Device operation requires very simple anode (V_A) and gate (V_G) voltage waveforms, with grounded cathode, and relies on the possibility to lead the thyristor either to its high-current ("1") or to its low-current ("0") state by a fast low-to-high V_G switch, depending on the amount of holes in the gated p-base. To this regard, note that, despite the role of holes in the gated p-base on data storage has been clearly highlighted in previous works, the extreme importance of the speed at which the gate voltage is switched for cell state sensing is here discussed for the first time. Results show, moreover, that by proper selection of the low and high V_G levels during read, state-1 can be reached with the stationary hole concentration in the p-base, while hole depletion is needed to lead the device to state-0. This represents the starting point to analyze device performance and reliability.

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II. Experimental Results

A. Working Principles

Fig. 1 shows (a) the structure of the T-RAM cell (details can be found in [6] and [7]) along with the experimental parameters for its electrical characterization and (b) the *static* anode current vs. anode voltage (I_A-V_A) characteristics of the cell for different V_G. The curves have been measured directly sensing I_A during a slow V_A sweep in presence of a protection resistance $R_P = 5.5\ \text{M}\Omega \gg R_L$ and allow the definition of the static forward-breakover (V_{FB}) and hold (V_H) voltages as depicted in the figure [6]. Note that the static V_{FB} has only a very small reduction moving from $V_G = -2$ V to 0 V, allowing the exploitation of the maximum bistability window of the thyristor in this V_G range.

Although Fig. 1b shows that in quasi-stationary conditions $V_A \simeq 2.75$ V is required at $V_G = 0$ V to lead the thyristor to its high-current state, Fig. 2 reveals that early device turn-on occurs when V_G reaches 0 V through a fast low-to-high transition [6]. The voltage scheme of the experimental test adopted to investigate this point is shown in Fig. 2a and consists first in raising V_A from $V_{AL} = 0$ V to V_{AH} and then in raising V_G from $V_{GL} = -2$ V to $V_{GH} = 0$ V in a time t_r, monitoring I_A after this transition. As shown in Fig. 2b, this *dynamic* sensing of I_A results in thyristor turn-on at the static V_{FB} corresponding to $V_G = 0$ V only for t_r longer than 10 μs,

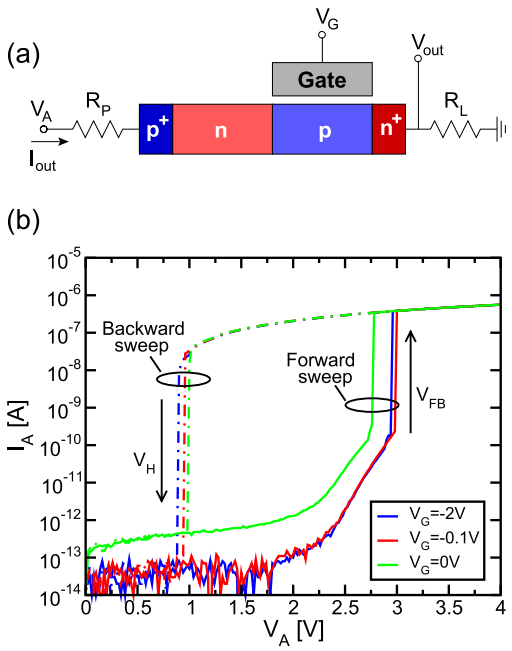

Fig. 1. (a) Schematics for the T-RAM cell investigated in this work and main experimental parameters: I_A is directly sensed at the anode by a semiconductor parameter analyzer in static measurements ($I_A = I_{out}$), while is obtained from the V_{out} sensed by an oscilloscope in dynamic measurements ($I_A = V_{out}/R_L$). The n- and p-base are nearly 100 nm long, the silicon thickness is 30×30 nm^2 and the gate oxide thickness is 5 nm. (b) T-RAM I_A-V_A curves from a slow forward and backward sweep of V_A at different V_G. ON current is limited by R_P.

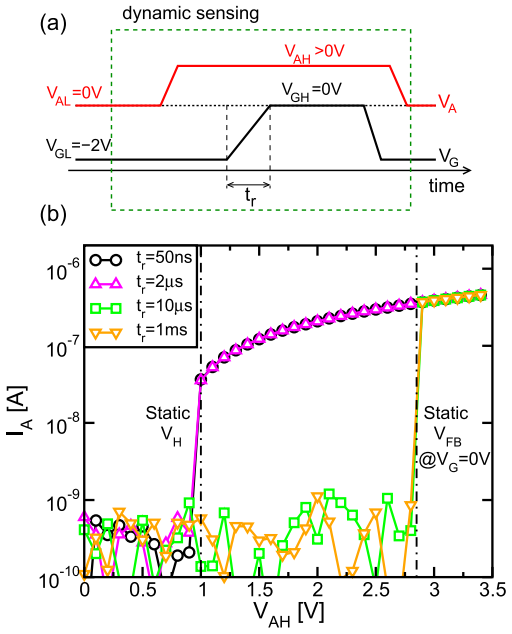

Fig. 2. (a) V_A and V_G waveforms for dynamic sensing of the T-RAM cell and (b) resulting I_A-V_{AH} characteristics for different t_r. ON current is limited by R_P.

while device turn-on happens at the static V_H for t_r shorter than 2 μs. This has been explained in [6] considering that a high amount of holes exists in the thyristor p-base at V_{GL} and that if t_r is short enough to prevent their escape while V_G

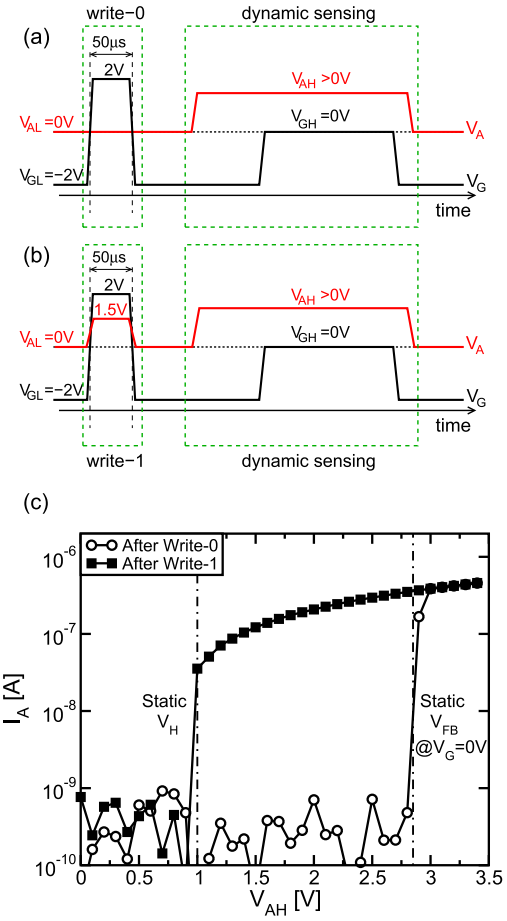

Fig. 3. V_A and V_G waveforms for (a) write-0 and (b) write-1 prior to dynamic sensing of the T-RAM cell and (c) resulting I_A-V_{AH} characteristics. All the pulse fronts are of 50 ns. ON current is limited by R_P.

is being raised, their charge contributes to the increase of the p-base potential and, in turn, of the electron current flowing from the cathode to the n-base triggering thyristor turn-on. As a result, a lower V_A is required to lead the device to its high-current state in its bistability window when V_G equals 0.

Results in Fig. 2 pave the way for the exploitation of the bistability of the gated-thyristor to achieve DRAM operation. Note, in fact, that early device turn-on resulting from dynamic sensing of I_A with short t_r comes from the presence of a hole concentration in the p-base during the V_G ramp that is higher than that corresponding to stationary conditions. This means that removing holes from the p-base prior to dynamic sensing prevents early turn-on, leading the thyristor to its low-current state for V_{AH} below the static V_{FB} at $V_G = 0$ V. This is accomplished with the voltage scheme of Fig. 3a, where a highly positive V_G pulse with grounded anode acts as a write-0 operation prior to dynamic sensing, whose resulting I_A-V_{AH} curve is reported in Fig. 3c (open symbols). To restore a high hole concentration in the p-base and lead the thyristor again to its high-current state during dynamic sensing, the voltage scheme of Fig. 3b can be adopted. Here a write-1 operation is performed by raising not only V_G to the same high level of the write-0 operation but also V_A to a positive value above the static V_H (1.5 V was used in the experiment). This makes the

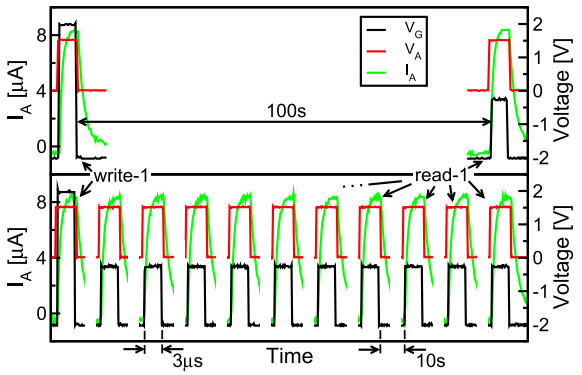

Fig. 4. Voltage and current waveforms during write-1 ($V_A = 1.5$ V, $V_G = +2$ V, duration of 3 μs) and (a) a single read operation after 100 s or (b) 10 read operations spaced by 10 s (read duration is 3 μs). In both cases, $V_{AL} = 0$ V, $V_{AH} = 1.5$ V, $V_{GL} = -2$ V and $V_{GH} = -0.25$ V. All the pulse fronts are of 50 ns, no R_P was used and $R_L = 2$ kΩ.

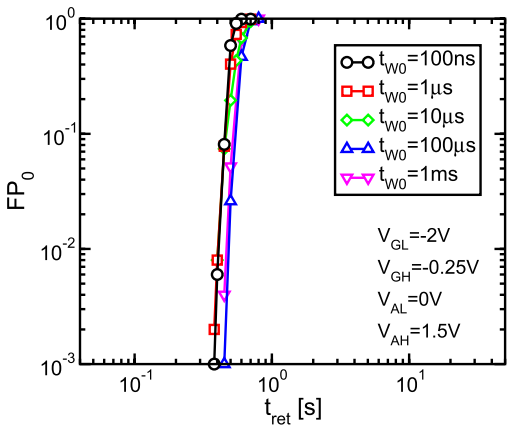

Fig. 5. FP0 as a function of t_{ret}, for different durations t_{W0} of the write-0 pulse. The same voltage levels of Fig. 4 were used, representing just unoptimized test conditions, see [7].

gated-thyristor turn on during this operation, rapidly restoring a high hole concentration in the p-base and leading the device to state-1 during the next dynamic sensing, as shown in Fig. 3c (filled symbols).

B. First Analysis of Cell Performance

In light of the previous discussion on the working principles of the T-RAM cell, no retention issue is expected on state-1 when V_{GL} and V_{GH} are properly selected to lead early device turn-on with the stationary hole concentration in the p-base at V_{GL}. This clearly appears from Fig. 4, where cell read by dynamic sensing with $t_r = 50$ ns (limited by our experimental setup), $V_{GL} = -2$ V and $V_{GH} = -0.25$ V leads to cell turn-on even after 100 s from the write-1 operation ($V_A = 1.5$ V, $V_G = +2$ V, duration of 3 μs), both (a) without and (b) with intermediate read operations.

Due to hole generation in the p-base, instead, state-0 can be preserved only for finite time stretches. Fig. 5 shows the probability to find the cell on state-1 after a write-0 operation (fail probability for state-0, FP0) as a function of the time separation between this operation and dynamic sensing (t_{ret}). A steep curve close to 1 s appears, irrespective of the duration of the write-0 pulse. This reveals negligible variability effects and represents a promising starting point for the optimization of the voltage waveforms used for device operation [7] and, more generally, of the device operating conditions. Finally, note that the voltage waveforms required for cell operation allow successful array functionality with easily manageable disturbs on unselected cells [8].

III. Conclusions

In this letter, we have presented the first comprehensive analysis of the basic physics and the working principles of the T-RAM cell, highlighting the role of dynamic sensing and hole concentration in the p-base and the related impact on data retention on state-1 and state-0.

Acknowledgments

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