3D Chip-level Broadband Measurement Technique for Radiated EM Emission

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***Abstract*—This paper proposes a novel broadband 3D chip-level radiated EM emission measurement technique. Two different test carriers with the embedded CPW and coil conductors respectively are designed and realized by the integrated passive device (IPD) process, which allow collecting the EM emission via near-field coupling. Using an in-house designed 0.18-µm CMOS VCO as the DUT, the emission spectrum obtained using the CPW conductor demonstrates a broadband characteristic up to above 20 GHz with an excellent agreement of the direct measurements. Compared to the traditional IEC standard approaches typically limited below 3 GHz, the proposed high sensitivity and broadband technique is suitable for evaluating EM interference of high-frequency ICs in advanced 3D packaging.**

***Keywords*—3D, Broadband, chip-level, EMI, EMC, IPD, voltage-controlled oscillator (VCO).**

I. Introduction

As Moore's law approaches the physical limit, one future direction that has attracted much attention recently is "More than Moore." In this scenario, different functional blocks including the high-frequency ICs will be stacked using advanced 3D packaging technologies. It can be envisioned that the electromagnetic compatibility (EMC) among the ICs due to the radiated emission inside the package becomes a very critical issue. Regarding the radiated emission test, the IEC (International Electrotechnical Commission) standard 61967-2 [1] adopts the transverse electromagnetic (TEM) cell to evaluate the EM emission of ICs, which is a closed rectangular stripline with the tapered region at each end, and the septum in the TEM cell is used to receive the radiated emission as shown in Fig. 1(a). The IEC 61967-8 IC stripline method [2] is also developed for characterizing radiated emission of ICs as shown in Fig. 1(b). Compared with the TEM cell, the IC stripline method become more popular [3]-[5] for IC-EMC tests owing to the building cost, occupied space, and sensitivity. However, these currently available methods cannot fulfill the above-mentioned requirement for the radiated EM emission from high speed ICs in the 3D stacked package. The IEC test methods could only be utilized to characterize radiated emission for packaged ICs without the capability for chip-level testing. Also, the TEM cell and IC stripline methods only support the frequency below 1 GHz and 3 GHz, respectively.

In this paper, we propose using the IPD testing carriers for 3D chip-level broadband radiated EM emission measurements

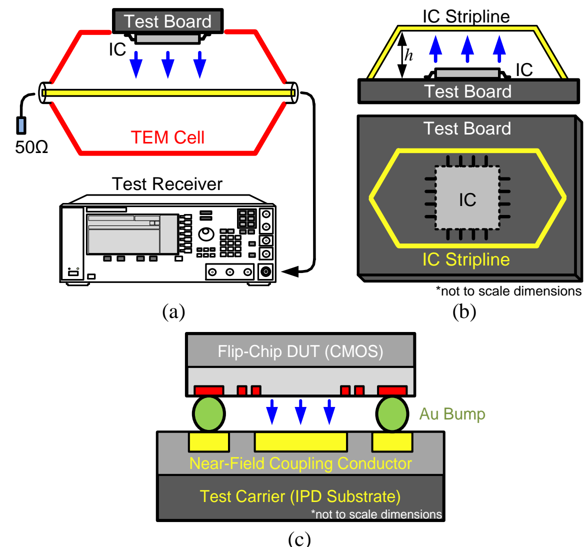

Fig. 1. Radiated EM interference measurement for ICs: (a) TEM cell method, (b) IC stripline method, and (c) proposed chip-level near-field coupling method.

as illustrated in Fig. 1(c), which can overcome the issues for the current IEC standard methods and has not been reported before. Two different conductors as the EM emission receiver inside the test carriers are designed. Using the in-house developed CMOS VCO (f_0 ~ 6 GHz) as the DUT, the spectrums are measured using both direct contact (conduction) and via the test carrier (radiation) up to tens of GHz. The measured results indicate that the IPD carrier with the CPW conductor is capable of high sensitivity and broadband radiated emission test at the chip level.

II. Chip-level Near-field Coupling Method

A. Coupling Conductor Design

According to the IEC, one important guideline for the radiated EM emission test structure design is to have a fixed distance between the IC and the septum for obtaining reliable measurement results, as illustrated in Fig. 1(a). Similarly, the height between the stripline and the DUT was set to a fixed value (6.7 mm as the example in the standard [2]) to control the measurement variation and maintain the characteristic impedance of the stripline, as shown in Fig. 1(b). In the proposed IPD test carriers, a fixed distance of only 30 µm can

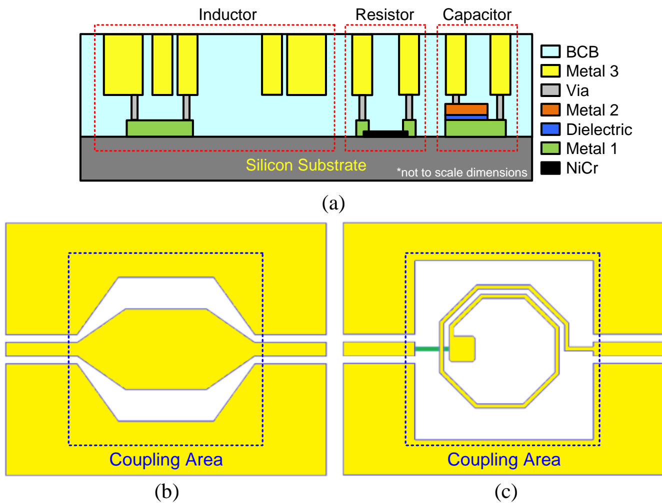

Fig. 2. Test carrier design: (a) cross section of IPD process, (b) coupling CPW line, and (c) coupling coil.

be achieved by the height of gold bumps as illustrated in Fig.1(c), which takes the advantage of IPD microfabrication and flip-chip technology. As a result, the DUT can be in proximity to the test carrier for near-field coupling and is very suitable for testing the bare die chips for 3D package, which cannot be performed using the conventional IEC standard methods. Another key point is to design a coupling conductor as the receiver for the radiated emission from the DUT. The IPD technology is a passive device-only process developed for RF applications. Using a high-resistivity silicon substrate, the IPD technology has three metal layers with a low-loss tangent dielectric material of benzocyclobutene (BCB), as shown in Fig. 2(a). The thick top metal layer (M3) of Cu is 10 μm for low loss interconnects.

Two different conductors in the test carrier are designed for comparison, as shown in Fig. 2(b) and 2(c), respectively. A 50-ohm CPW line with a width of 170 μm and ground spacing of 65 μm is implemented as shown in Fig. 2(b). The length of CPW line within the coupling area is 170 μm using two 100 μm tapered transitions connected to a finer CPW line with a width of 30 μm, ground spacing of 15 μm, and length of 1400 μm for probing. The simulated result of the CPW line shows an insertion loss of 0.16 dB at the 6 GHz band. In addition, the proposed CPW coupling line could cover a frequency range up to 46.5 GHz, according to the IEC standard of the IC stripline defined based on VSWR < 1.25. The other design of the test carrier uses a coil coupling conductor, where a coil using the 1.5-turn spiral inductor is considered an effective manner to receive the radiated signal. The coil is with a width of 10 μm, a spacing of 10 μm, and a radius of 55 μm. The simulated quality factor (Q) and inductance are 33 and 1.29 nH at the 6 GHz band, respectively.

B. Device Under Test of CMOS VCO

To demonstrate the proposed test method for evaluating the radiated EM emission from the unpackaged ICs, an LC-tank voltage-controlled oscillator (VCO) is designed using a standard 1P6M 0.18-μm CMOS process as the DUT, as shown in Fig. 3(a). From the viewpoint of EM radiation as shown in

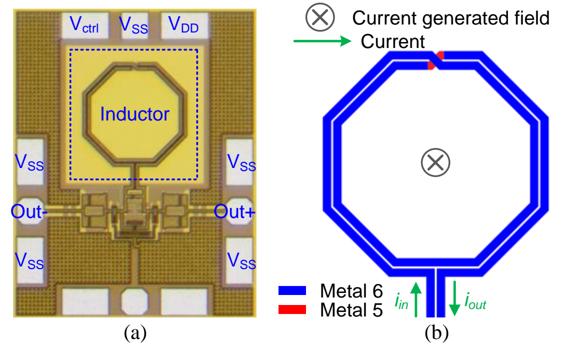

Fig. 3. Device under test: (a) CMOS LC-tank VCO, (b) spiral inductor in the LC tank.

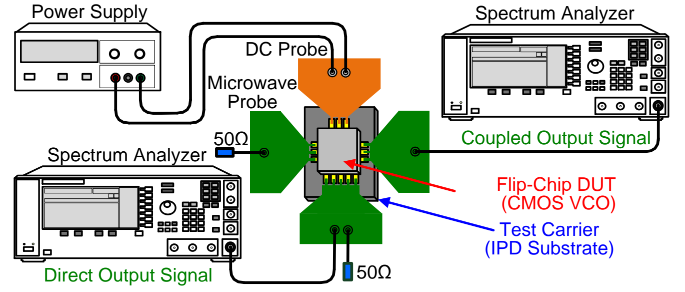

Fig. 4. Proposed setup of chip-level radiated EM interference measurement.

Fig. 3(b), assuming the current flows into the right port of the spiral inductor and flows out to the left port. The current will generate an out-of-plane magnetic field. This can emulate the noise generators in a large-scale IC, which acts like the undesired aggressor that could affect the normal operation of either analog or digital circuits.

The VCO was operated under a supply voltage of 1.8 V with a frequency of around 6 GHz. The cross-coupled pair topology is adopted with a 2-turn spiral inductor, as shown in Fig. 3(b). The inductor is with a width of 9 μm, a spacing of 2 μm, and a radius of 56 μm. The inductance and Q are 2.2 nH and 9.2 at 6 GHz, respectively. The varactor is implemented by the accumulation-mode MOS with a gate length of 0.5 μm and finger number of 10. Under a 1.8 V supply voltage, the dc current of the core circuit is 6.9 mA. The measured output power with buffer is −3.7 dBm (cable loss included). The tuning sensitivity and phase noise are 6.24−5.75 GHz and −113.1 dBc/Hz at a 1-MHz offset. The chip size is 0.6 mm × 0.7 mm including the RF and dc bias pads.

III. Measured Results and Discussion

The coupling conductor is set face-to-face the DUT as illustrated in Fig. 1(c) for the radiated EM emission measurements. The area of the coupling conductor is designed to have a similar size to the inductor in VCO for effective coupling of the EM emission generated by the inductor of LC-tank VCO. With flip-chip technology, the DUT was flipped and bonded on the IPD substrate as a test carrier. The gold bumps with a diameter of 70 μm and height of 30 μm can support the DUT above the test carrier and serve as the interconnects to supply dc voltage to VCO and carry out the signal to the test receiver.

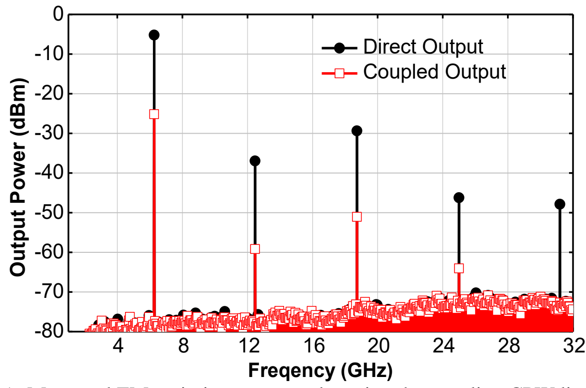

Fig. 5. Measured EM emission spectrum by using the coupling CPW line.

The proposed chip-level coupling method could sense a more uniform and stronger magnetic field. The sensitivity issue in the conventional TEM cell and IC stripline methods can be solved. Note that an additional post-amplifier which is essential in the IEC standard approaches can be avoided here.

The detailed measurement setup is illustrated in Fig. 4. The signal generated from the VCO was carried out by both direct output and coupled output measurements simultaneously by on-wafer probing. The direct output measures the conducted signal from the VCO through the gold bumps and IPD traces directly, which show a larger signal level in the test receiver. On the other hand, the coupled output receives the signal coupled from the VCO to the coupling conductor in the IPD test carrier. Eventually, both signals pass through the microwave probes and the cable harness to the test receiver.

Fig. 5 shows the measured emission spectrum of the VCO by utilizing the coupling CPW line. As expected, the coupled output signal level is lower than the direct output one. It is worth pointing out that the measured power difference between direct output and coupled output is very consistent, about 20 dB over the entire frequency range up to the 5th harmonic, as shown in Table I. The reduced signal level can be attributed to the path loss in the air between DUT and the coupling CPW line. The results indicate that using the CPW line as the coupling conductor exhibits a flat and broadband response.

In contrast, Fig. 6 shows the measured spectrum of the VCO by using the coupling coil to collect the EM emission. As can be seen, the odd harmonics of VCO show much higher levels than the even harmonics. Note that the coupling mechanism between the IPD coil and the spiral inductor of CMOS VCO is similar to a transformer. The odd harmonics can be effectively transferred from the primary winding (inductor on CMOS VCO) to the secondary winding (coil on IPD carrier). However, the even harmonics are suppressed because of the half-wave symmetry, as summarized in Table I. The results highlight the importance of the coupling conductor design. Although the coil could enhance the coupling efficiency, the CPW design presents a more reliable and wideband response, which can detect more precisely the original EM emission levels at various harmonics for the unpackaged ICs in an advanced 3D package.

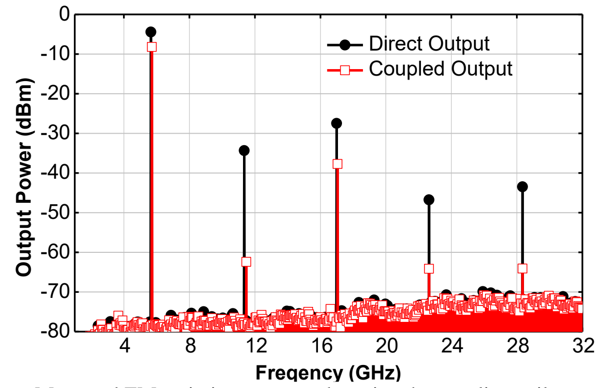

Fig. 6. Measured EM emission spectrum by using the coupling coil.

TABLE I
MEASURED POWER LEVEL DIFFERENCE BETWEEN DIRECT AND COUPLED OUTPUTS

Coupling Conductor	Harmonics				
	1st	2nd	3rd	4th	5th
CPW Line	-20.0 dB	-22.2 dB	-21.7 dB	-17.9 dB	-24.8 dB
Coil	-3.8 dB	-28.1 dB	-10.3 dB	-17.4 dB	-20.6 dB

IV. CONCLUSION

This paper proposed a novel broadband 3D chip-level radiated EM emission measurement technique using the IPD test carriers, which can overcome the issues for the current IEC standard methods such as a limited frequency range and only for unpackaged ICs. Two different coupling conductors were designed to measure the radiated emission from a CMOS VCO. The results indicated that using the CPW conductor in the test carrier can obtain a reliable and wideband response, compared with the coupling coil. The proposed radiated EM emission test approach is suitable for evaluating EM interference of high-frequency ICs in advanced 3D packaging.

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