Performance and Robustness

Characterisation of SiC Power MOSFETs

Asad Fayyaz, *M.Eng (Hons.)*

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Abstract

Over the last few years, significant advancements in the SiC power MOSFET fabrication technology has led to their wide commercial availability from various manufacturers. As a result, they have now transitioned from being a research activity to becoming an industrial reality. SiC power MOSFET technology offers great benefits in the electrical energy conversion domain which have been widely discussed and partially demonstrated. Superior material properties of SiC and the consequent advantages are both later discussed here. For any new device technology to be widely implemented in power electronics applications, it's crucial to thoroughly investigate and then validate for robustness, reliability and electrical parameter stability requirements set by the industry.

This thesis focuses on device characterisation of state-of-the-art SiC power MOSFETs from different manufacturers during short circuit and avalanche breakdown operation modes under a wide range of operating conditions. The functional characterisation of packaged DUTs was thoroughly performed outside of the safe operating area up until failure test conditions to obtain absolute device limitations. For structural characterisation, Infrared thermography on bare die DUTs was also performed with an aim to observe hotspots and/or degradation of the structural features of the device. The experimental results are also complemented by 2D TCAD simulation results in order to get a further insight into the underlying physical mechanisms behind failure during such operation regimes. Moreover, the DUTs were also tested for body diode characterisation with an aim to observe degradation and instability of electrical device parameters which may adversely affect the performance of the overall system. Such investigations are really important and act as a feedback to device manufacturers for further technological improvements in order to overcome the highlighted issues with an aim to bring about advancements in device design to meet the ever-increasing demands of power electronics.

Acknowledgement

List of Definitions, Symbols, and Terms

AC – Alternate current

α_T – Current temperature coefficient

BPD – Basal plane dislocation

BJT – Bipolar junction transistor

C – Carbon

CAD – Computer-aided design

C_{DS} – Drain-source capacitance

C_{GS} – Gate-source capacitance

d – Device thickness

DC – Direct current

D_{it} – Density of interface states

D_n, D_p – Diffusion coefficients

D_{FW} – Freewheeling diode

DUT – Device under test

E – Electric Field

E_{BRK} – Breakdown Field

E_{max} – Maximum electric field

E_C, E_V – Conduction, Valence band energy

E_{AV} – Avalanche energy

E_{SC} – Short circuit energy

E_g – Energy bandgap

E_{SW} – Switching energy losses

ε_s – Dielectric constant

FOM – Figure of merit

FPGA – Field programmable gate array

GaN – Gallium Nitride

I_1, I_2, I_3 – Phase currents

I_{AV} – Avalanche current

I_D – Drain current

I_F – Body diode forward current

I_{GS} – Gate source current

I_{GSS} – Gate leakage current

I_{LEAK} – Drain leakage current

I_L – Load current

$I_{PH(pk)}$ - Inverter peak input current

I_{SC} – Short circuit current

IR – Infrared

J – Total current density

J_n, J_p – Electron, Hole current density

k – Boltzmann's constant

L_{LOAD} – Load inductance

L_{STRAY} – Stray inductance

λ_{th} – Thermal Conductivity

m – Modulation index

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

n, p – Electron, Hole density

n_i – Intrinsic carrier concentration

N_C, N_V – Conduction, Valence density of states

OLTO – Overload turn-off

$P_{D(max)}$ – Maximum allowed power dissipation

$P_{SC(pk)}$ – Peak short circuit power

PV – Photovoltaic

PWM – Pulse width modulation

q – Electronic charge

R_{Drift} – Drift Resistance

$R_{DS(ON)}$ – Drain to source on-state resistance

R_G – Gate resistance

$R_{G(INT)}$ – Internal gate resistance

R_{GS} – Gate-source resistance

R_{ON} – On-state resistance

$R_{ON,sp}$ – Specific on-state resistance

R_S – Specific electrical resistance

R_{th} – Thermal Resistance

SF – Stacking fault

Si – Silicon

SiC – Silicon Carbide

SCSOA – Short circuit safe operating area

SOA – Safe operating area

t_{AV} – Time in avalanche

T_A – Ambient temperature

T_{CASE} – Case temperature

t_d – Dead time

T_J – Junction temperature

$T_{J(max)}$ – Maximum junction temperature

t_{ON} – ON time

t_{PULSE} – Pulse width time

t_{SC} – Short circuit withstand time

TCAD – Technology computer-aided design

μ - Carrier mobility

μ_n – Electron mobility

μ_p – Hole mobility

UIS – Unclamped Inductive Switching

V – Electrostatic potential

V_{BD} – Breakdown Voltage

$V_{BR(DSS)}$ – Manufacturer's rated breakdown voltage

$V_{BR(eff)}$ – Actual breakdown voltage

V_{BE} – Base-emitter voltage

v_D – Average drift velocity

v_{sat} – Saturation drift velocity

V_{DD} – Input voltage

V_{DS} – Drain-source voltage

$V_{DS(max)}$ – Rated nominal blocking voltage

$V_{GS(th)}$, V_{th} – Threshold voltage

V_{GS} – Gate-source voltage

V_F – Body diode forward voltage drop

V_m – Amplitude of modulating signal

V_{SW} – Amplitude of carrier signal

WBG – Wide bandgap

ZTC – Zero temperature coefficient

List of Publications

The work carried out during the course of this PhD project resulted in the following publications:

Journal:

Fayyaz, Asad, Gianpaolo Romano, Jesus Urresti, Michele Riccio, Alberto Castellazzi, Andrea Irace, and Nick Wright. "A Comprehensive Study on the Avalanche Breakdown Robustness of Silicon Carbide Power MOSFETs." *Energies* 10, no. 4 (2017): 452.

Fayyaz, Asad, Gianpaolo Romano, and Alberto Castellazzi. "Body diode reliability investigation of SiC power MOSFETs." *Microelectronics Reliability* 64 (2016): 530-534.

Romano, Gianpaolo, **Asad Fayyaz**, Michele Riccio, Luca Maresca, Giovanni Breglio, Alberto Castellazzi, and Andrea Irace. "A comprehensive study of short-circuit ruggedness of silicon carbide power MOSFETs." *IEEE Journal of Emerging and Selected Topics in Power Electronics* 4, no. 3 (2016): 978-987.

Castellazzi, Alberto, **Asad Fayyaz**, Gianpaolo Romano, Li Yang, Michele Riccio, and Andrea Irace. "SiC power MOSFETs performance, robustness and technology maturity." *Microelectronics Reliability* 58 (2016): 164-176.

Fayyaz, Asad, and Alberto Castellazzi. "High temperature pulsed-gate robustness testing of SiC power MOSFETs." *Microelectronics Reliability* 55, no. 9 (2015): 1724-1728.

Fayyaz, Asad, Li Yang, Michele Riccio, Alberto Castellazzi, and Andrea Irace. "Single pulse avalanche robustness and repetitive stress ageing of SiC power MOSFETs." *Microelectronics Reliability* 54, no. 9 (2014): 2185-2190.

Conference:

Fayyaz, Asad, Alberto Castellazzi, Gianpaolo Romano, Michele Riccio, Andrea Irace, Jesus Urresti and Nick Wright. "Influence of gate bias on the avalanche ruggedness of SiC power MOSFETs." In *Power Semiconductor Devices and ICs (ISPSD), 2017 29th International Symposium on*, pp. 391-394. IEEE, 2017.

Castellazzi, Alberto, **Asad Fayyaz**, Gianpaolo Romano, Michele Riccio, Andrea Irace, Jesus Urresti-Ibanez, and Nick Wright. "Transient out-of-SOA robustness of SiC power MOSFETs." In *Reliability Physics Symposium (IRPS), 2017 IEEE International*, pp. 2A-3. IEEE, 2017.

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Fayyaz, Asad, Gianpaolo Romano, Alberto Castellazzi, and Andrea Irace. "Robustness investigation of SiC power MOSFETs under negative temperature." In *Power Electronics and Applications (EPE'16 ECCE Europe), 2016 18th European Conference on*, pp. 1-8. IEEE, 2016.

Romano, Gianpaolo, Michele Riccio, Luca Maresca, Giovanni Breglio, Andrea Irace, **Asad Fayyaz**, and Alberto Castellazzi. "Influence of design parameters on the short-circuit ruggedness of SiC power MOSFETs." In *Power Semiconductor Devices and ICs (ISPSD), 2016 28th International Symposium on*, pp. 47-50. IEEE, 2016.

Romano, Gianpaolo, Luca Maresca, Michele Riccio, Vincenzo d'Alessandro, Giovanni Breglio, Andrea Irace, **Asad Fayyaz**, and Alberto Castellazzi. "Short-circuit failure mechanism of SiC power MOSFETs." In *Power Semiconductor Devices & IC's (ISPSD), 2015 IEEE 27th International Symposium on*, pp. 345-348. IEEE, 2015.

Castellazzi, Alberto, **Asad Fayyaz**, Li Yang, Michele Riccio, and Andrea Irace. "Short-circuit robustness of SiC power MOSFETs: Experimental analysis." In *Power Semiconductor Devices & IC's (ISPSD), 2014 IEEE 26th International Symposium on*, pp. 71-74. IEEE, 2014.

Yang, L., **A. Fayyaz**, and A. Castellazzi. "Characterization of high-voltage SiC MOSFETs under UIS avalanche stress." In *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference On*, pp. 1-5. IET, 2014.

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1. Background and motivation

Nowadays, energy efficiency is central to every system due to limited non-renewable fuel resources and an increased awareness regarding climate change. Furthermore, as the energy demand of the world is continuously increasing with time due to increased urbanization and electrification, more efficient and reliable renewable energy generation solutions such as wind and photovoltaic (PV) are required. In order to meet the ever-increasing energy demands around the globe, it is foreseen that the trend towards more electrical systems will continue and accelerate over the next years. In particular, increased attention is given to advancements in power electronics which will eventually result in a much more efficient generation as well as management of electrical energy. Of course, it is only possible subject to the robustness and reliability assessment of semiconductor power devices (also known as switches) which are the most fundamental components within power conversion system, known as power converters. A power converter is an electronic circuit which performs conversion of electrical characteristics (i.e. current and voltage) in order to transfer energy from source to the load [1]. Moreover, newer device technologies with higher voltage, higher current, and higher switching frequency are also much needed to accommodate the growing needs of energy storage technologies and smart grid technologies [2].

Ideally, it is expected that energy conversion is as efficient as possible by minimising energy losses within the process. Definition of an ideal switch features the ability to conduct infinite current with zero on-state voltage drop (i.e. conductor like behaviour) and block infinite voltage with zero off-state current flow (i.e. insulator like behaviour) along with instantaneous switching without energy loss between ON and OFF states. The semiconductor devices offer an approximation of these features to a reasonable extent. Nevertheless, in practice, power device design is usually characterised by trade-offs between on-state, switching, and off-state performance. The ability of a power device to closely approximate an ideal switch is an

important figure of merit, therefore, it plays an important role as competition amongst manufacturers and is one of the key parameters when it comes to device selection [3].

Currently, the power semiconductor industry is majorly served by silicon (Si) semiconductor material as Si device fabrication technology has evolved over the years to provide mature, reliable and robust technologies in abundant volumes at remarkably low costs. Even though state-of-the-art Si device technologies are always improving, the material itself possess performance limitations due to its intrinsic physical properties. However, as mentioned earlier, increasing demands for energy generation and efficiency require device solutions that outperform Si-based devices to more closely resemble an ideal switch. Moreover, some demanding power electronics domains such as automotive, railway traction, aerospace, and military applications also require power devices to operate under really harsh conditions. In order for Si-based devices to meet these stringent requirements, expensive cooling systems with a large number of devices connected in series and parallel are needed along with active or passive snubbers. This will lead to an increase in the size and weight of power converter which is highly undesired. Therefore, to fulfil such requirements is only possible due to wide bandgap (WBG) materials, thanks to their superior material properties. Power devices made from WBG materials outperform Si devices allowing them to penetrate newer and advanced power conversion domains not possible to be served previously by Si technology as well as improve existing conversion processes within which Si is widely used. Most commonly used WBG materials are silicon carbide (SiC), gallium nitride (GaN) and Diamond. The work carried out within this thesis focuses on SiC power MOSFETs. Power MOSFETs are particularly of interest since they are normally OFF transistors with non-dissipative gate control. They have bi-directional current conduction capability which makes them really attractive for advanced power conversion applications allowing to minimise the number of devices. The superior material properties enable devices made out of SiC to have higher switching frequencies, operational temperatures, power density levels and breakdown voltages as well as lower

switching and conduction losses to offer improved efficiency. These features also enable to significantly decrease size, weight, and volume of power converters due to a reduction in the size of heatsinks and passive components which are of strategic importance in certain power electronics applications. The higher bandgap, higher breakdown field, higher thermal conductivity and significantly lower intrinsic carrier concentrations are the some of the key superior properties of SiC semiconductor material due to which, the above-mentioned benefits could be brought into realization in power converters [4]. These properties are discussed in further detail in section 2.1 of the thesis.

SiC power MOSFET technology had been severely plagued by huge densities of defects in the crystal and oxide-semiconductor interface. However, after substantial and continued research efforts and consequent developments in device fabrication technology, SiC power MOSFETs have started to gain popularity over the recent years within the power electronics community and as a result, they are now a commercial reality readily available to be purchased (as a discrete device and in modules) from different manufacturers [5]. Not only that, research activities are also well underway to manufacture power electronics circuitry entirely using SiC devices and several studies have demonstrated all SiC-based converters. As also mentioned in [6], SiC power devices may also be found implemented in some commercial power systems which is a great step towards achieving a wide scale deployment of these devices in future commercial systems. Converter efficiencies as high as > 99% for SiC have been reported in various literature materials. Some of these investigations could be found in [7-9].

1.1. Research Motivation, Aims, and Objectives

Alongside technological advancements in the SiC device fabrication technology also comes the need to assess the performance, robustness and reliability characterisation of those devices. Extensive characterisation of any new device technology is an important industrial requirement prior to their wide-scale deployment in commercial electronics circuitry. In general, it is expected for a device to be able to operate at a voltage, current, and/or temperature well above the nominal continuous ratings given in the datasheet. Dynamic transient characterisation such as short circuit (SC) and unclamped inductive switching (UIS) are two of the widely considered operation modes. These operating conditions are really stressful for the device and devices could possibly be frequently subjected to such operating condition in power converters. Such assessments are crucial to investigate device operation and determine absolute device limitations outside of the safe operating area (SOA). SOA determines the voltage and current boundaries (usually set in the datasheet by the manufacturer) within which the device should be operated to avoid any destructive failure.

❖ SC is a key withstand capability test procedure for semiconductor devices within the power electronics industry. It is, in particular, relevant to drives application (80% of the power electronic applications) and aims to assess their robustness i.e. short circuit withstand time (t_{SC}), the usual industrial requirement of $t_{SC} \geq 10$ µs to allow for the intervention of protection circuitry, under various different operational conditions. It is crucial to perform extensive characterization of SiC devices in order to assess the absolute device limitations to feedback the semiconductor manufacturing industry for aiding future development with SiC device manufacturing technology. The SC experimental results consisting of both single pulse and aging tests are presented here. The tests were performed on start-of-the-art commercial 1.2 kV rated SiC power MOSFETs from various manufacturers. The experimental results are then further complemented by electro-thermal simulation to understand the failure mechanism.

❖ Power MOSFETs are widely used in high switching frequency power electronics applications driving inductive loads such as motor drive applications. At turn-off, the sudden interruption of current in inductive load and/or parasitic elements results in back EMF (electromagnetic force) being produced which could force the device into a drain-to-source avalanche. Avalanche rugged power MOSFETs are expected to withstand time in avalanche (t_{AV}) and be able to also dissipate energy during avalanche (E_{AV}) outside of the SOA under a range of operating conditions. E_{AV} is an important figure of merit for all applications requiring load dumping and/or to benefit from snubber-less converter design. Failure of the device may occur as a result of this harsh switching transient. Here, both single pulse capability and aging tests are of interest. Therefore, extensive characterisation during avalanche breakdown operation comprising of experimental and simulation results are presented here in this chapter. The tests were performed on state-of-the-art commercial 1.2 kV rated SiC power MOSFETs from various manufacturers. To better understanding the failure mechanism, electro-thermal simulations were also performed.

❖ Another important feature of a power MOSFET is its intrinsic body diode which could be used for current freewheeling in inverters subject to their stable operation. Moreover, making use of the body diode also eliminates the need for an anti-parallel diode resulting in a reduction of cost and number of components. It is therefore important to assess the stability of relevant electrical parameters prior to be benefiting from this feature. Therefore, body diode reliability of 1.2 kV SiC power MOSFETs were investigated within an inverter operation and relevant electrical parameters were monitored at regular intervals. Moreover, devices were also subjected to static stress in order to reassure the results obtained.

1.2. Thesis Outline

This thesis consists of seven chapters. A brief overview of the chapters to follow is included here:

Chapter 2: This chapter starts with a comparison of relevant material properties of Si and SiC semiconductor material followed by a brief overview of power MOSFET operation and recent SiC developments. The last section includes a brief description of some of the device qualification methodologies widely used for device characterisation within power electronics community.

Chapter 3: This chapter discusses different experimental methodologies which were implemented for device characterisation investigation. More specifically, double pulse test circuit operation is described which was used for SC and UIS tests with slight modifications. Furthermore, 2-level 3-phase inverter setup is also explained which was used for body diode characterisation. The second section of this chapter talks about fast transient infrared thermography technique used on bare dies for structural characterisation. Moreover, simulation technique for electro-thermal mixed mode simulations is also discussed here to finish off this chapter.

Chapter 4: A range of functional and structural experimental results for SC at different test conditions on packaged and bare die devices are presented. Aging test results are also included. In the second section, simulation results showing physical mechanism responsible for the failure of the device are discussed. Finally, the chapter ends with a discussion on experimental and simulation results highlighting the possible failure mechanisms during SC.

Chapter 5: This chapter presents experimental results during UIS test condition to investigate the avalanche breakdown operation of SiC power MOSFETs. Again, a range of results on packaged and bare die devices are presented here along with aging tests. The experimental results are followed by simulation results discussing failure mechanism are presented. Lastly,

a discussion section is included to discuss experimental and simulation results as well as highlighting the possible failure mechanism.

Chapter 6: This chapter discusses the body diode reliability investigation of SiC power MOSFETs. The body diode of the MOSFET was stressed within an inverter operation and stability of relevant electrical parameters i.e. body diode forward voltage drop (V_F) and drain leakage current (I_{LEAK}) were monitored which are included here. Devices were also stressed under static conditions to reconfirm the findings obtained.

Chapter 7: This is the last chapter of the thesis. Here, conclusions and future works are discussed.

2. Review of Power Semiconductor devices

Silicon (Si) is the most popular base material for manufacturing power semiconductor devices. A broad range of applications is currently being successfully served by unipolar and bipolar devices developed from Si since the 1950s. Silicon carbide (SiC) semiconductor material, a wide bandgap (WBG) material, has superior physical properties as compared to Si and therefore, power devices made from SiC are much more promising in various aspects as will be discussed here in the next section. Efforts have been made in the past to develop semiconductor devices using SiC but the manufacturing technology has been highly plagued with high densities of defects in the crystal and gate oxide. However, relatively recently from 2000 onwards, significant advancements have been made in SiC power device manufacturing technology which has resulted in their wide commercial availability. Undoubtedly, Si-based device technology is mature but its intrinsic material properties restrict their performance in higher switching frequency, higher temperature, higher voltage and higher power applications. Nevertheless, Si device technology is also consistently improving even at the time of writing this thesis but due to its inherent material properties, its overall benefits could never be anywhere near to what SiC has to offer. For this reason, WBG materials especially SiC are heavily researched upon with the aim of further improving device technology to utilize the benefits of the inherent material properties to take power electronic conversion technology to the next level [10, 11]. The superior physical properties (discussed in later sections) on offer from SiC material will provide cutting-edge technology development, leading to weight and volume reduction of the future electrical energy handling equipment (such as power converters, inverters, switch mode power supplies etc.). In order to explore new power electronics application areas (e.g. more electric aircraft, avionics, military applications, railway traction etc.) where silicon cannot be used due to its physical limitations, it is paramount that new WBG device technologies are explored to be able to develop power electronics circuitry for high power and switching frequency applications [4, 12, 13].

This chapter contains three section. Section 2.1 includes a brief comparison and summary of fundamental material properties of Si and SiC. The overview of a power MOSFET and the recent advancements for SiC devices are discussed in section 2.2. Lastly, section 2.3 gives a brief description of various different characterisation techniques used for power devices.

2.1. Comparison of Si and SiC material properties

Different crystal structures of SiC known as polytypes are produced which are chemically identical to contain the same amount of Si and Carbon (C) atoms covalently bonded to each other but differ in electrical properties even though their chemical formula is the same. The three major polytypes of SiC are 3C, 4H, and 6H.

Table 2.1: Fundamental material properties of Si and SiC [10, 11, 14-16]

Property	Units	Silicon (Si)	Silicon Carbide (SiC)		
			4H	6H	3C
Band gap Energy (E_g) [14]	eV	1.1	3.23	3.20	2.36
Breakdown Field (E_{BRK}) [14]	MV/cm	0.3	2.0	2.4	1.2
Electron Mobility	cm^2/V·s	1400	1000	400	800
Hole Mobility	cm^2/V·s	471	115	101	40
Relative Dielectric Constant (ε_r)	-	11.8	9.7	9.7	9.7
Thermal Conductivity (λ_{th})	W/cm·K	1.5	4.9	4.9	3.2
Melting Point	°C	1412	3103	3103	3103
Intrinsic Carrier Concentration (n_i)	cm^{-3}	1×10^{10}	5.0×10^{-9}	1.6×10^{-6}	1.5×10^{-1}
Saturation Drift Velocity (v_{sat})	cm/s	1×10^7	2×10^7	2×10^7	-

The carrier mobilities in 4H polytype of SiC are superior to those of its other polytypes. Moreover, 4H polytype is preferred over 6H due to it having identical mobilities along both

planes of the semiconductor crystal. Fundamental material properties of Si and SiC relevant to power semiconductor devices are presented in Table 2.1 [10]. The material properties mentioned here are discussed in detail in the next subsections.

2.1.1. Breakdown Field (E_BRK)

The breakdown field for 4H-SiC is 2.0 MV/cm which is approximately seven times bigger than the breakdown field of Si, 0.3 MV/cm, as given in Table 2.1. Even though the breakdown field of 6H-SiC is slightly bigger than 4H-SiC polytype, 4H-SiC is favoured over 6H-SiC in these high power vertical devices due to its higher mobility along the c-axis, which refers to the direction in which growth of the most epitaxial layers takes place. Here, epitaxial layer/region, also known as drift layer/region, is a lightly doped structure within a power device which helps to withstand high drain-source voltage by containing the depletion region in the OFF state. The breakdown voltage (V_{BD}) for non-fully N- depletion region structures, which is inversely proportional to the drift doping concentration, i.e. *pn* diodes could be expressed as [17]:

$$V_{BD} = \frac{\varepsilon_s E_C{}^2}{2qN_{DRIFT}}$$

(2.1)

As also clear from equation 2.1, the higher breakdown field of SiC can allow achieving much higher doping levels for the same breakdown voltage level. Moreover, for a given V_{BD}, SiC power devices could be made thinner than the Si devices. The minimum width of the N-Drift (W_m) region is in general limited by the need to contain the entire depletion region which extends with the applied blocking voltage. In SiC, higher critical electric field (E_C) implies thinner devices as W_m is inversely proportional to E_C. The critical electric field is the maximum field that the device can sustain prior to the onset of avalanche breakdown mechanism. Equation 2.2 approximates the required width of the drift region [18].

$$W_m \approx \frac{2V_{BD}}{E_C}$$

(2.2)
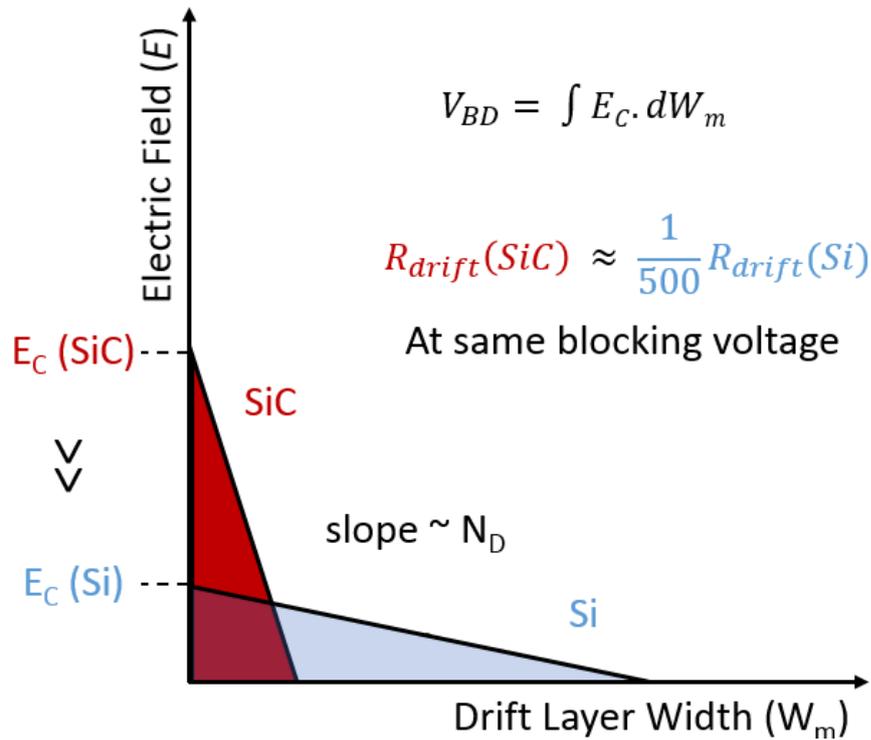
Figure 2.1: *Distribution of electric field within SiC and Si structures (Comparison) [19]*

Thinner devices due to higher E_C and doping also means that for the same breakdown voltage, SiC devices can have relatively lower on-state resistances as illustrated using Figure 2.1. The specific electrical resistance (R_S) for n-type drift layer could be expressed using equation 2.3. The R_S for SiC power devices is approximately five hundred times lower than the Si devices due to the higher density of electrons (due to higher doping concentration). For higher breakdown voltages, higher doping levels in WBG semiconductors are used than in Si which further increases the specific on-state resistance ratio between the Si and SiC power devices.

Furthermore, thinner devices also reduce the storage of the minority charge carriers in diodes. It then allows a decrease in the reverse recovery losses and thus high frequency operation could also be achieved which also implies lower switching losses [18].

$$R_S = W_m \cdot \frac{1}{q\mu_n n} \tag{2.3}$$

2.1.2. Band-gap Energy (E$_G$)

SiC is a WBG semiconductor since its band-gap energy (E$_G$) is much larger than Si. Any semiconductor material with E$_G$ higher than 2 eV is classed as a WBG material e.g. SiC, GaN and diamond are some of the most popular ones. The E$_G$ of 4H-SiC is 3.23 eV which is three times that of Si as shown in Table 2.1. The valence electrons of the semiconductor material are required for the complete pairs of covalent bonds with neighbouring atoms. Hence, a certain amount of energy defined as band-gap energy (E$_G$) is required to break the electrons out of the bonds and into the conduction band, where they move freely and can contribute towards conduction of current. This is illustrated by the simplified band-gap energy diagram in Figure 2.2. The importance of higher band-gap is that it allows high temperature operation for the device. The wider the bandgap of the material, the higher the temperature at which it could operate. The intrinsic carrier concentration, dependent on E$_G$ and temperature, is an important parameter which governs high temperature operation of SiC power devices as discussed in detail in the next section.
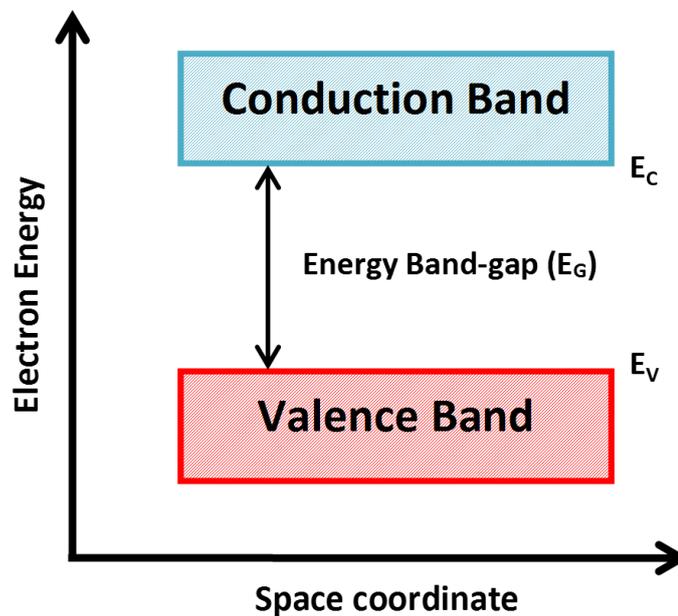
Figure 2.2: *Energy band-gap diagram*

2.1.3. Intrinsic Carrier Concentration (n_i)

The thermal generation of electron-hole pairs across the energy band-gap of a semiconductor determines the intrinsic carrier concentration. In order to calculate its value, energy band-gap (E_G), as well as the density of states in the valence (NV) and conduction (NC) bands, are required. The intrinsic carrier concentration is given by:

$$n_i = \sqrt{np} = \sqrt{N_C N_V}\, e^{-E_G/2kT}$$ (2.4)

where k is Boltzmann's constant (1.83 x 10^{-23} JK^{-1}) and T is the absolute temperature.

The intrinsic carrier concentration for Si can be calculated to give:

$$n_i = 3.87 \times 10^{16} T^{3/2} e^{-(7.02 \times 10^3)/T}$$ (2.5)

whereas for 4H-SiC, it can be written as:

$$n_i = 1.70 \times 10^{16} T^{3/2} e^{-(2.08 \times 10^4)/T}$$ (2.6)

The intrinsic carrier concentration is a function of E_G and temperature. Figure 2.3 shows a plot comparison of the intrinsic carrier concentration for Si and SiC over a range of temperature from 300 K to 700 K which represent usual operating temperature ranges for power devices. It is evident from Figure 2.3 that SiC has an extremely lower intrinsic carrier concentration than Si, even at high temperatures. It is also worth noting that the intrinsic carrier concentration for Si at room temperature (300 K) is 1.4 x 10^{10} cm^{-3} whereas it is just 6.7 x 10^{-11} cm^{-3} for SiC [10]. The maximum temperature limit imposed by a power device is defined as the temperature at which the n_i reaches a comparable value to the doping concentration of the drift region. In that case, the junctions inside the device level out, thus the intended operation and control of the device (i.e. electrical characteristics) is lost which could even result in destructive failure of the device.
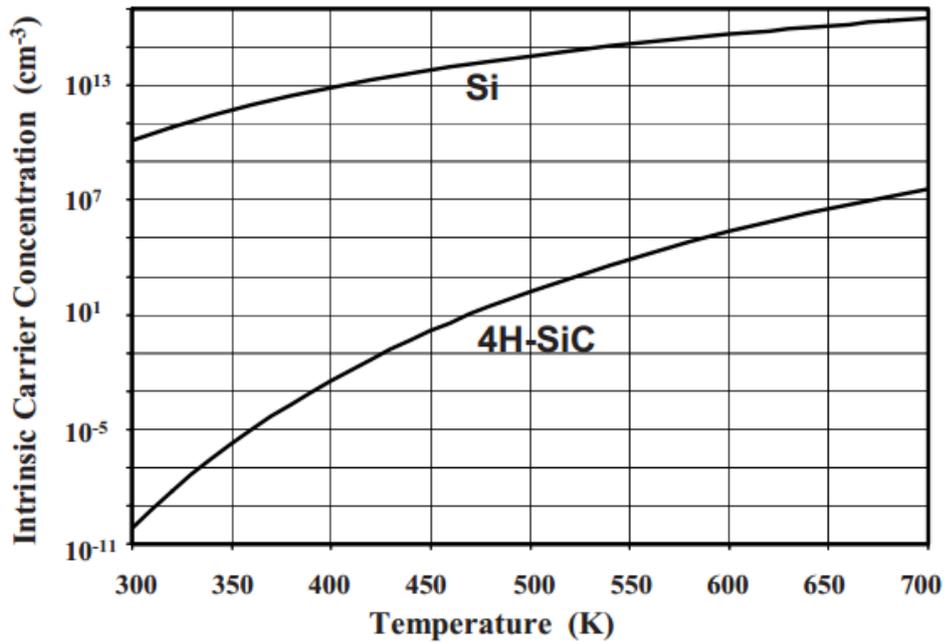
Figure 2.3: Comparison of Intrinsic Carrier Concentration for Si and 4H-SiC versus

temperature [10]

In the case of Si, at a relatively low temperature of 540 K, the intrinsic carrier concentration becomes equal to the typical drift doping concentration of 1 x 10^{15} cm^{-3}. On the other hand for 4H-SiC, even at 700 K, the intrinsic carrier concentration is only 3.9 x 10^7 cm^{-3}, much lower than the normal drift doping levels. The intrinsic carrier concentration becoming comparable to the doping concentration results in the development of mesoplasmas. The destructive failure in semiconductors occurs due to mesoplasmas which generate current filaments with very high current density. Such mechanism is much likely to take place in SiC at much higher temperature than in Si. SiC power devices could easily withstand temperature even as high as 1000 K. However, the maximum operating temperature for a device is rather limited by the packaging materials and interconnect technology [1]. Operation at such high temperatures also means a significant reduction in cooling system requirements i.e. reduction in size and weight of the overall power system.

2.1.4. Thermal Conductivity (λ_{th})

The thermal conductivity for 4H-SiC is 4.9 W/cmK which is approximately three times higher than the thermal conductivity of Si, 1.5 W/cmK, as given in Table 2.1. The ability of a material to conduct heat is defined as thermal conductivity [20]. The higher the thermal conductivity of a material, the faster the rate of transfer of heat generated. The operation of a power device is fundamentally characterised by heat generation and self-heating phenomena. During steady-state operation of a power device, equation 2.7 defines the maximum allowed power dissipation which is as follows:

$$P_{D(\max)} = \frac{T_{J(\max)} - T_A}{R_{th}} = \frac{\Delta T}{R_{th}}$$

(2.7)

where $T_{J(max)}$ is the maximum junction temperature, T_A is the ambient temperature ($T_{J(max)} >$ T_A) and R_{th} is the thermal resistance of the device

The thermal resistance of the device is dependent on the thermal conductivity as given by equation 2.8:

$$R_{th} \propto \frac{1}{\lambda_{th}} \cdot d$$

(2.8)

where d is device thickness

A higher thermal conductivity value enables a reduction of the thermal resistance of the semiconductor device as also expressed in equation 2.8. As a result of R_{th} reduction, in principle, the achievable power density can be increased for a given ΔT. On the other hand, a reduction in ΔT could also be achieved for a given power dissipation. The reduction of R_{th} of the semiconductor device itself is clearly advantageous. However, the extent to which this feature can be taken advantage of is clearly dependent on the overall thermal resistance value of the packaged device [3].

2.1.5. Saturation Drift Velocity (v_{sat})

In semiconductors, the presence of electric field results in the acceleration of the carriers. The average velocity for carriers (v_D) is dependent on the mobility (μ) and electric field (E) as expressed using equation 2.9. This linear relationship is only valid for low electric fields up to the values of 10^4 V/cm.

$$v_D = \mu E \tag{2.9}$$

However, electric fields above this value are usually encountered in power devices. In that case, the carrier drift velocity no longer increases proportionally to the electric field. The velocity approaches a constant value which is known as the saturated drift velocity (v_{sat}). The saturation drift velocity in 4H-SiC is 2.0 x 10^7 cm/s, twice the saturation drift velocity in Si (1.0 x 10^7 cm/s). The v_{sat} can be written as:

$$v_{sat} = \mu E_C \tag{2.10}$$

where E_C is the critical electric field above which, carrier velocity does not increase further

The higher saturation drift velocity of SiC allows achieving higher operating frequencies for power devices making them suitable for applications requiring high switching frequencies. High frequency operation is directly proportional to the E_C and v_{sat}, dictated by Johnson's figure of merit equation as discussed in section 2.1.7. Therefore, SiC power devices have much higher switching speeds than Si devices [18].

2.1.6. Electron and hole mobility (μ_n and μ_p)

Amongst all the material properties discussed here, electron carrier mobility is the only property which is not superior to SiC. The electron mobility for SiC is 1000 cm^2/Vs as compared to 1400 cm^2/Vs for Si. Figure 2.4 illustrates the electron mobility comparison between SiC and Si versus temperature range of 300 K – 500 K (usual operating temperature range for power devices). Such mobility levels are achievable in the drift region (also referred to bulk mobility)

however, the mobility in the channel region is still in the range of 15 – 20 cm^2/Vs due to large

density of traps at the SiC/SiO$_2$ interface [21]. Mobility plays an important role in the on-state

performance of the device i.e. current density. The overall on-state current density is defined

as:

$$\vec{J} = q\mu_n n \cdot \vec{\nabla}V + qD_n \cdot \vec{\nabla}n + q\mu_p p \cdot \vec{\nabla}V - qD_p \cdot \vec{\nabla}p \qquad (2.11)$$
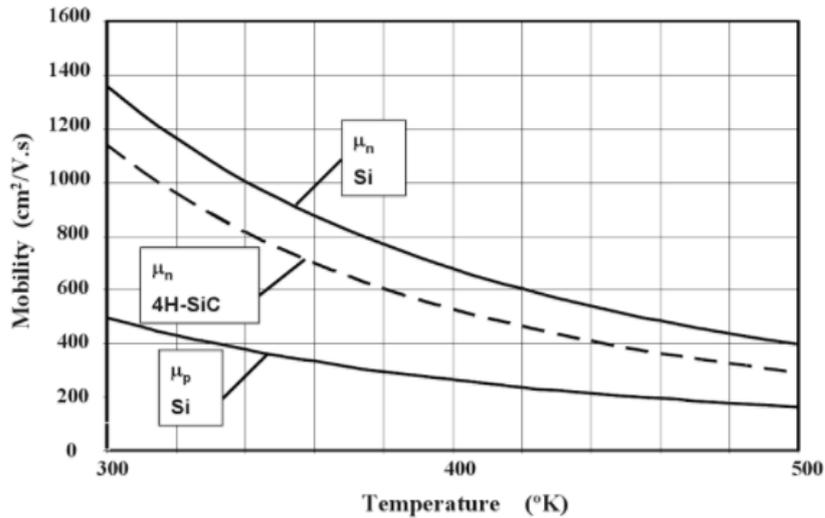
Figure 2.4: *Comparison of SiC and Si mobility as a function of lattice temperature [10]*

The overall current density consists of two components: drift and diffusion current. The total

current is due to the flow of both electrons and holes which are driven by the gradients of

electrostatic potential and charge carriers' density within the semiconductor device. It is

advantageous to design devices which primarily make use of drift current component of only

one type of charge carrier (desirably electrons since $\mu_n > \mu_p$) and use the other type of charge

carrier for diffusion. Due to the superior properties of SiC discussed earlier, it is possible to

fabricate thinner and high blocking voltage SiC MOSFET chips with on-state resistance

comparable (or maybe even lower) to Si IGBTs. Another advantage of SiC MOSFETs, unlike Si

IGBTs, is that they don't make use of large diffusion current components to achieve the

acceptable on-state performance which in turn means a significant reduction in charge

storage effects in the space charge region which contributes towards higher switching

performance [3]. Even though the carriers' mobility is lower in 4H-SiC material as compared to Si, all the other benefits achieved due to higher E_{BRK} and larger E_G as discussed earlier over weigh this constraint, therefore, making SiC so special.

2.1.7. Figure of Merit (FOM)

The performance of a power device and semiconductor materials are usually evaluated using a value determined from various Figure of Merit (FOM) equation(s) [22]. The higher the value is, the better the performance of the semiconductor material. The aim of the proposed FOMs is to allow comparison of different theoretical performance which arises from the differences in the physical properties of various materials. Some of the well-known and widely used FOMs are briefly mentioned below.

- **Baliga's figure of merit (BFOM)**

Baliga's FOM is defined using equation 2.10. Its value indicates how the resistance of the drift region would be affected due to the material properties of the semiconductor. BFOM is inversely proportional to the specific on-state resistance of the drift region [10].

$$BFOM = \varepsilon_s \mu_n E_C{}^3 \qquad (2.10)$$

Moreover, Baliga also defined a figure of merit (known as Baliga's high frequency figure of merit (BHFFOM)) which evaluated the capability of devices to operate at high switching frequency. It is described using equation 2.11 [22].

$$BHFFOM = \mu_n E_C{}^2 \sqrt{\frac{V_G}{4V_{BD}{}^3}} \qquad (2.11)$$

- **Johnson's figure of merit (JFOM)**

This figure of merit describes how the material parameters of semiconductor devices have an impact on the high frequency and high power operation of the devices. JFOM is evaluated using equation 2.12 [23].

$$JFOM = \frac{E_C{}^2 v_{sat}{}^2}{4\pi^2}$$
(2.12)

- **Keyes' figure of merit (KFOM)**

The figure of merit derived by Keyes provided a thermal limitation on the switching behaviour of the transistors. KFOM can be calculated using equation 2.13 [24].

$$KFOM = \lambda \left(\frac{cv_{sat}}{4\pi\varepsilon_s} \right)^{1/2}$$
(2.13)

Comparison of the above mentioned FOMs is given in Table 2.2. The values presented in Table 2.2 are normalised with respect to Si. Referring to table 2.2, in principle, SiC outperforms Si for all FOMs discussed here.

Table 2.2: Comparison of normalized figures of merit for Si and 4H-SiC [25]

Material	BFOM	BHFFOM	JFOM	KFOM
Si	1.0	1.0	1.0	1.0
4H-SiC	560	69	400	5.1

2.2. Overview of Power MOSFET

The MOSFET (**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor) is a semiconductor device widely used for high power switching applications. It is a normally OFF and voltage controlled unipolar device. Nowadays, MOSFET switches are almost present in the majority of the mainstream power conversion applications e.g. switch mode power supplies (SMPS) and motor drives. The development of the vertical power MOSFET structure in the 1970s proved to be a big achievement and a milestone in power electronics at that time as it allowed improved performance as compared to the existing power bipolar transistors [26]. Power MOSFETs rapidly gained popularity over BJTs within the power electronics community due to their simple, efficient and non-dissipative voltage controlled gate drive because of having high input impedance. For a long time, Si MOSFETs have been hindered with relatively higher conduction losses due to their high on-state resistance (R_{ON}). As a result, power MOSFETs made out of Si are widely used for applications below 600 V as R_{ON} significantly increases at higher blocking voltages [4]. As also discussed in section 2.1.3., using SiC as a base material to manufacture power MOSFETs allows a significant reduction of R_{ON} at a given blocking voltage. Engineering samples of SiC power MOSFETs up to 10 kV have been demonstrated within power conversion applications in recent publications [27-30].

2.2.1. SiC Power MOSFET structure and recent developments

The planar MOSFET structure is currently the most common structure used for developing SiC power MOSFETs. The first planar SiC power MOSFET was made commercially available by CREE in 2011 in a TO-247 package [31]. The cross-section of SiC planar MOSFET structure along with its schematic symbol is shown in Figure 2.5. It consists of three terminals: gate, drain, and source. The MOSFET structure presented here is of a typical n-channel enhancement mode device. Since they have lower on-state resistances as compared to p-channel enhancement mode devices, therefore, they are the most commonly used devices for power switching applications. This structure is also known as vertical-diffused (VD) MOSFET

structure. These structures can withstand high voltages mainly due to the thick lightly doped N-Drift region. The fabrication process for these structures starts with an N- epitaxial layer grown on a heavily doped N+ substrate.
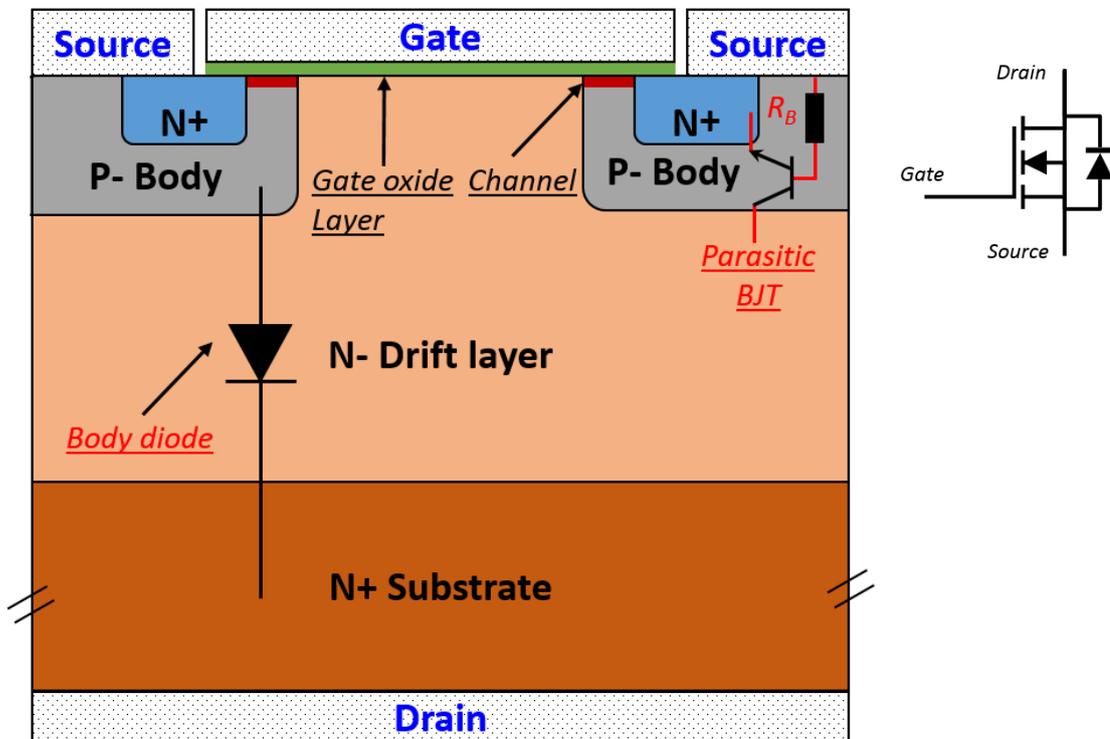
Figure 2.5: *Structure of SiC Power D-MOSFET*

The SiC power device technology has been significantly improved over the last 10 to 15 years. Some of the main issues had been the size, cost, and quality of SiC crystals being produced. Most importantly, the quality and size of the wafers need to be improved significantly with really low densities of defects (i.e. density of micropipes (MP) and basal plane dislocations (BPDs)) as these epitaxial wafers form the basis of any power devices. Nowadays, 6" (150 mm) diameter SiC wafers with MP density $\leq 1/cm^3$ are widely available to be purchased from the market. Recent claims have been made where SiC wafers with densities of MP and BPDs $\leq 1/cm^3$ and $5000/cm^3$ respectively have been demonstrated [32]. Relatively recently in 2015, research samples of 8" (200 mm) SiC wafers have also started to emerge onto the market [33]. However, 8" SiC wafers are still in the development phase and thus not available to be

purchased commercially. The development and growth of larger sizes of SiC crystals (diameter ≥ 8") are mainly hindered due to large densities of defects [34].

Another critical issue faced within fabrication of power MOSFETs has been the growth of gate oxide (SiO_2) for the formation of SiC/SiO_2 layer. As the oxide grows during oxidation, carbon (C) atoms present in SiC crystal need to be removed by transport through the oxide in the form of CO or CO_2. The removal of carbon atoms results in a much slower oxide growth rate for SiC even though the oxidation process is relatively the same for both Si and SiC. It has not been possible to fully remove the carbon atoms and hence unreacted carbon atoms result in the formation of clusters which consequently lead to traps (defects) at the SiO_2-SiC interface [35]. Currently, the density of interface states (D_{it}) at the SiC/SiO_2 interface has been around 10^{12} $eV^{-1}cm^{-2}$ which is about two to three orders of magnitude higher than the comparatively matured Si/SiO_2 interface (10^{10} $eV^{-1}cm^{-2}$). However, recent studies presented in [36, 37] have shown to have approximately achieved an order of magnitude reduction in D_{it} to around 1.5 x 10^{11} $eV^{-1}cm^{-2}$. Large D_{it} severely reduces interface mobility in the channel due to Coulomb scattering phenomenon when the traps are occupied with electrons. Moreover, high D_{it} has also been primarily the cause of V_{th} instability in SiC power MOSFETs due to trapping/de-trapping of electrons in these interface states as a result of applied bias between gate and source terminals. Instability in V_{th} is undesirable as it tends to shift operating characteristics of the MOSFET and thus may adversely affect their performance within converters.

SiC power MOSFETs are being developed for blocking voltages well above 600 V due to their significantly lower on-state resistance when compared to Si counterparts. Discrete devices and modules are now widely manufactured and therefore readily available to purchase from various suppliers. Devices with voltage ratings of 650 V, 900 V, 1000 V, 1200 V and 1700 V are commercially available within the market. However, 3.3 kV and 6.5 kV SiC power MOSFETs are in the development pipeline and are expected to become commercially available in the near

future. As a result, SiC power MOSFETs are considered for applications where Si IGBTs were previously used (and beyond) to block high voltages and conduct high currents.

Trench gate structures have also been developed over the last few years. The first trench structure was made commercially available by ROHM in 2015. The new SiC trench structure outperforms the D-MOSFET structure since it offers 50% lower on-state resistance and 35% reduction in input capacitance. The reduction in input capacitance is another benefit that leads to a reduction of switching losses by up to 77% as compared to the planar D-MOSFET structures. This comparison was performed by ROHM on their 1200 V / 180 A rated planar and trench modules [38]. Undoubtedly, switching faster reduces switching losses and helps improve system efficiency. The careful power plane and gate driver circuit designs are crucial to keeping parasitic inductances to the minimal to avoid voltage overshoot at the drain and ringing at the gate terminals as later discussed in chapter 3 of the thesis. Lastly, a complete timeline has been presented in Figure 2.6, summarising all the recent developments for SiC power devices.
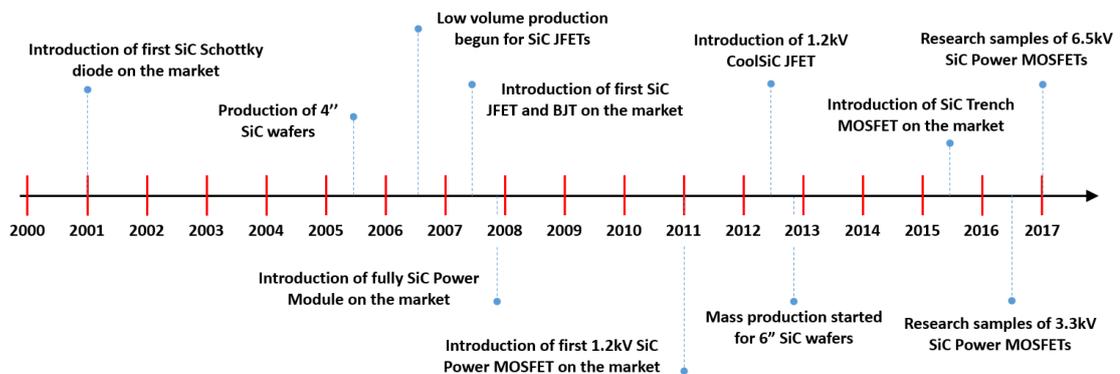
Figure 2.6: Timeline of developments for SiC power devices [5]

2.2.2. Operation and characteristics of a SiC Power MOSFET

The basic operation of a MOSFET switch involves the formation of a conductive channel when the applied V_{GS} exceeds the threshold voltage ($V_{GS(th)}$). The V_{th} of SiC power MOSFETs is in the range of 2 V to 4 V. The drain current (I_D) then starts to flow when a positive voltage is applied to the drain terminal. The application of positive bias at the gate terminal attracts n-type carriers (electrons) in the P-well underneath the gate oxide thus forming a thin layer of conduction electrons (majority carriers). The formation of a channel (also known as inversion layer) provides a path for the current to flow from the drain to the source terminal. However, the flow of current is facilitated by the high electric field inside the structure as a result of the applied V_{DS} at the drain terminal. When the device conducts current, it is defined to be in the ON-state. On the other hand, no channel is formed underneath the gate in the P-well if V_{GS} is lower than $V_{GS(th)}$ i.e. V_{GS} is either zero or negative. In this case, the conduction of drain current is blocked. As a result, the device supports high voltage applied at the drain terminal. Here, the device blocks voltage and does not conduct current, therefore, it is said to be in the OFF-state. However, drain leakage current always flow. This explains the basic analogy of a MOSFET switch as to how it conducts current and blocks voltage [10, 39]. Depending on the device design, there is always an absolute maximum blocking voltage that the device could withstand. If the voltage between drain and source terminals ever reaches a critical value also known as breakdown voltage, the reverse biased body diode breaks down which results in significant current flow. This mechanism of current flow between drain and source is termed as avalanche breakdown as discussed in detail in the later sections of the thesis.

Power MOSFET is a bidirectional current switch and therefore, drain current during ON-state can also flow in the reverse direction (from source to drain via the channel) if the potential applied at the drain is lower than the source terminal. The pn junction of P-Body and N-Drift region forms an intrinsic body diode within the MOSFET. Due to the N+ substrate region, the intrinsic body diode is essentially a PiN diode. The diode becomes forward biased if the

MOSFET is in the OFF-state and positive voltage exceeding the on-state forward voltage drop of the body diode (V_F) is applied at the source terminal with respect to the drain terminal. The V_F of the body diode is around 2.5 V to 2.7 V. The presence of intrinsic body diode in the MOSFET structure eliminates the need of anti-parallel diode for current freewheeling in inverter applications. At the same time, the presence of intrinsic body diode and the ability of a power MOSFET to conduct reverse current allows synchronous rectification within inverters. Synchronous rectification within inverters is desirable as it helps reduce the overall losses associated with semiconductor devices as also discussed in section 3.1.4 [4]. However, reliability assessment of the intrinsic body diode is crucial prior to making use of this feature. The change in electrical parameters such as V_F and I_{LEAK} over a relatively short amount of time is undesirable as it can adversely affect the inverter's performance.

The total drain to source on-state resistance $R_{DS(on)}$ of a MOSFET device could be divided into various different parts such as the channel, JFET region (and drift region along with the resistance of the packaging i.e. electrode contacts etc. A MOSFET structure showing different resistance components which make up $R_{DS(on)}$ is shown in Figure 2.7. The $R_{DS(on)}$ is the sum of all these components and can be calculated using equation 2.13. In the case of Si power devices, $R_{DS(on)}$ is mainly dominated by the N-Drift layer resistance (R_D) within high voltage power devices. However, this doesn't apply to SiC power devices as SiC power devices for the same breakdown voltage are relatively much thinner than the Si counterparts.

$$R_{DS(ON)} = R_{SOURCE} + R_{CH} + R_{ACC} + R_{JFET} + R_D + R_{SUB} + R_{MISC} \qquad (2.13)$$

where R_{SOURCE} = Source diffusion resistance; R_{CH} = Channel resistance; R_{ACC} = Accumulation resistance; R_{JFET} = JFET region resistance; R_D = Drain region resistance; R_{SUB} = Substrate resistance and R_{MISC} = Package related resistance
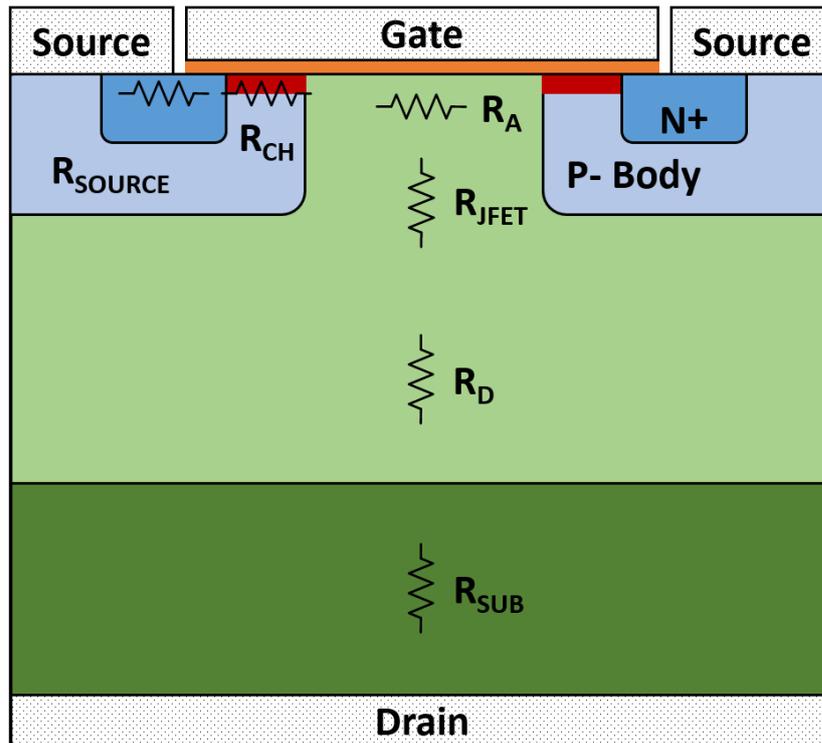
Figure 2.7: Internal resistances within a Power MOSFET

Transfer and output characteristics form the basic form of understanding about the operation of a MOSFET as a switch. It is essentially a V_{GS} controlled electronic switch. So, for an applied V_{DS} voltage, the amount of drain current (I_D) which would flow through the switch is determined by the applied V_{GS}. This relationship is best described by the I_D-V_{GS} transfer characteristics. The typical representation of transfer characteristics of a SiC power MOSFET at two different T_{CASE} and a given V_{DS} are presented in Figure 2.8. SiC power MOSFET is a thermally unstable device since I_D during on-state has both a positive and negative temperature coefficient (α_T) which is dependent on the value of V_{GS} and V_{DS}. The I_D-V_{GS} curves for two different T_{CASE} ($T_2 > T_1$) also have an intersection point (also known as zero temperature coefficient ZTC) which helps to identify the range of V_{GS} for both operation modes. To the left of the intersection point, the device exhibits unstable electro-thermal operation mode as α_T is positive. Here, higher temperature gives higher I_D (i.e. V_{th} plays an important role as it decreases with the increase of temperature to give more current at a fixed V_{GS}). To the right

of the intersection point is the stable mode of operation for the device as α_T is negative. When α_T is negative, I_D decreases as temperature is increased (i.e. $R_{DS,ON}$ plays its role as it increases with the increase of temperature to give a decrease in I_D).
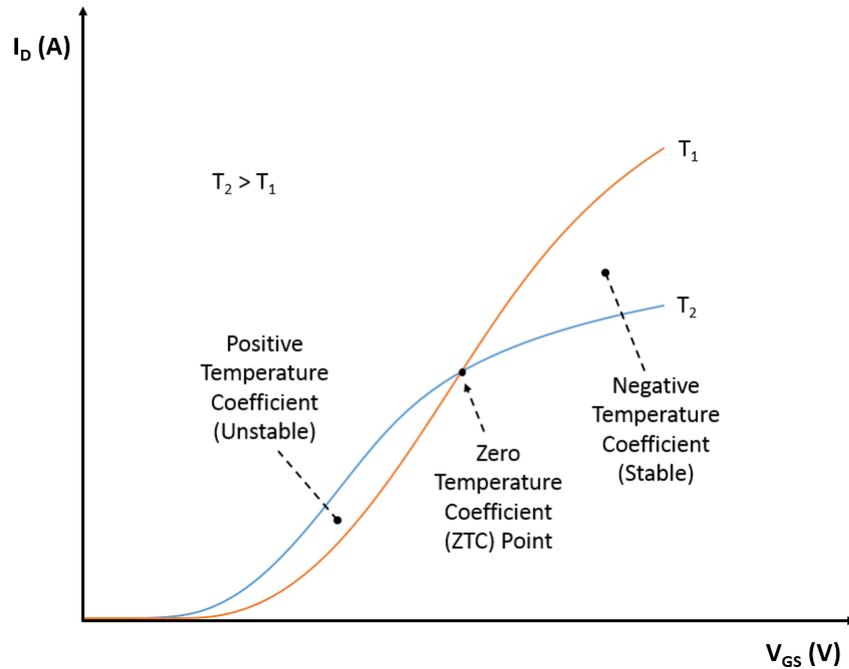
Figure 2.8: Typical transfer characteristics of a SiC power MOSFET

If the dependence of drain current on temperature is considered to be linear, it could then be described using equation 2.14 as follows:

$$I_D(T_J) = I_D(T_0) + \alpha_T(T_J - T_0) \tag{2.14}$$

In the above equation, T_J is the junction temperature, T_0 is the case temperature and α_T is the drain current temperature coefficient. Rearranging the above equation for the temperature coefficient (α_T) for the drain current gives equation 2.15:

$$\alpha_T = \left.\frac{\partial I_D}{\partial T}\right|_{V_{GS}, V_{DS}} \tag{2.15}$$

The increase in T_J as a result of constant power dissipation can be approximated using equation 2.16 as follows:

$$T_J(T) - T_0 = Z_{th,JA}(t) V_{DS} I_D(t, T_J) \qquad (2.16)$$

Rearranging 2.16 gives an equation for thermal impedance as described using equation 2.17 as follows:

$$Z_{th,JA}(t) = \frac{T_J(t) - T_0}{V_{DS} I_D} \qquad (2.17)$$

Substituting Equation 2.14 in equation 2.16 gives an important equation which is labelled 2.18:

$$T_J(t) = T_0 + \frac{Z_{th,JA} V_{DS} I_D(T_0)}{1 - V_{DS} \alpha_T Z_{th,JA}} \qquad (2.18)$$

The numerator term defines the increase in temperature as a result of the constant power dissipation ($V_{DS}I_D$). The denominator of the above equation determines the condition for thermal instability as described by parameter S for constant applied V_{DS} as follows in equation 2.19:

$$S = V_{DS} \alpha_T Z_{th,JA} \qquad (2.19)$$

The value of S helps to distinguish between stability and instability. If S < 1, the device is in stable operation mode and S ≥ 1 implies unstable operation mode. Using equation 2.19, the condition for instability can be rewritten as equation 2.20. From equation 2.20, it is obvious that $\alpha_T > 0$ to obtain thermal instability condition.

$$\alpha_T \geq \frac{1}{V_{DS} Z_{th,JA}(t)} \qquad (2.20)$$

In Figure 2.9, α_T as a function of I_D for a given temperature is plotted for illustration purposes. For a given device chip (i.e. given value of $Z_{th,JA}$), the condition presented in equation 2.20 identifies two operation regions dependant on the value of V_{DS}. Indeed, the device exhibits electro-thermal unstable behaviour for a range of I_D values (between I_1 and I_2) when the

condition in equation 2.20 is met. As V_{DS} is increased, the range of I_D (I_1-I_2) for which the device exhibits unstable behaviour is also increased. However, once I_D increases above the higher current limit of unstable behaviour I_2, the device regains thermally stable behaviour. Moreover, as I_D increases further, α_T becomes negative therefore implying that the thermal instability condition is removed. Furthermore, the device is highly susceptible to thermal runaway leading to hot-spot formation due to uneven current distribution inside the chip during unstable operation [40, 41].
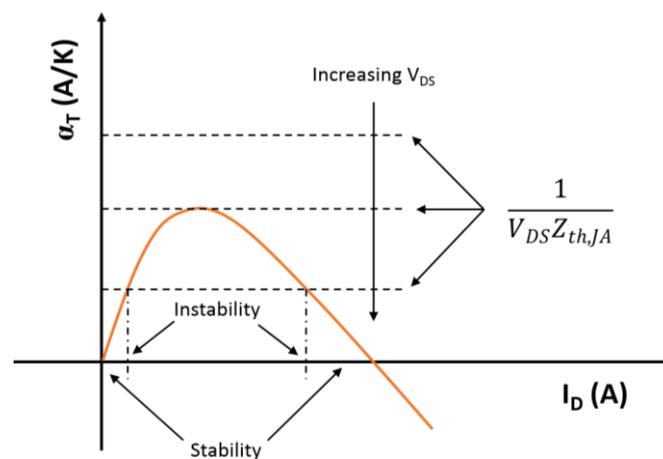
Figure 2.9: *Illustration of thermally stable and unstable operation of a Power MOSFET [40]*

The I_D-V_{DS} output characteristics help to identify how the on-state voltage drop (V_{DS}) changes for the range of I_D at a given V_{GS}. The typical output characteristic for a power MOSFET are presented in Figure 2.10. As expected, higher V_{GS} results in higher I_D flow at a given V_{DS}. For lower values of V_{DS}, I_D increases as the average drift velocity (v_D) of mobile carriers is proportional to the applied electric field as also discussed earlier in section 2.1.4. However, for higher V_{DS} values, the I_D curves start to saturate when the mobile carriers reach v_{sat} (i.e. it is no longer proportional to electric field) and further increase in V_{DS} doesn't affect I_D as also discussed later in section 3.3.
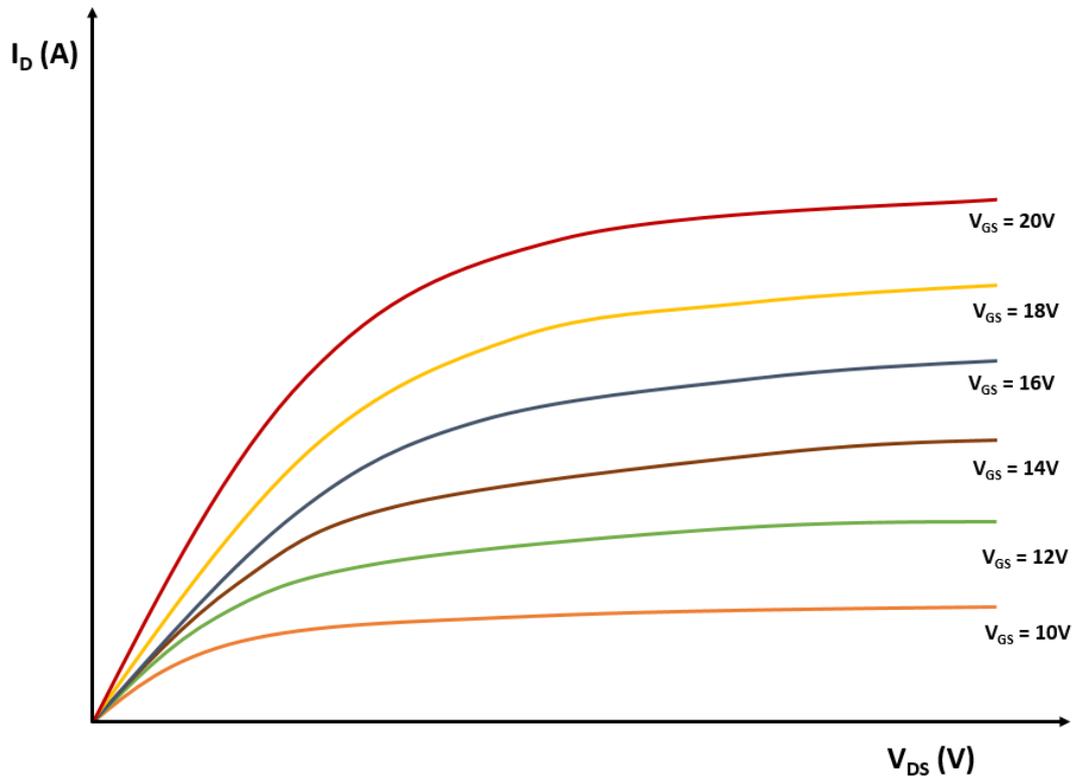
Figure 2.10: *Typical output characteristics of a SiC power MOSFET*

SiC power MOSFET internally exhibit some intrinsic capacitances which also play an important role in switching transients as included in the equivalent circuit of a MOSFET shown in Figure 2.11. Three different capacitances exist namely gate-drain capacitance (C_{GD}), gate-source capacitance (C_{GS}) and drain-source capacitance (C_{DS}). These quantities are really important for designing an optimum gate driver circuit. The rise of V_{GS} is usually determined by the value of the time constant due to R_G and C_{GS}. C_{GS} needs to be charged before the gate-source terminals can withstand voltage during on-state. C_{GD} is also known as the Miller capacitance and this capacitance is important where more than two switches are operated in series (i.e. during an inverter operation). During commutation of switches with sharp dV/dt, a small current flows through C_{GD} which moves the potential at the gate node up and down. As a result, V_{GS} sees overshoot and undershoot. This effect needs to be considered during circuit design to avoid accidental turn-on of both switches resulting in shoot-though as also mentioned in section

3.1.4. The V_{DS} switching transient is affected by the C_{DS}. All these capacitances are a function of V_{DS} and thus affect the switching characteristics of the MOSFET.
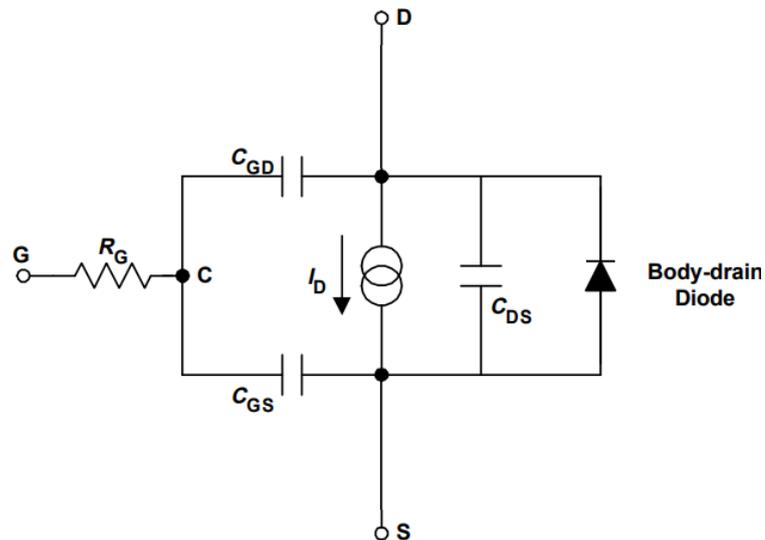
Figure 2.11: MOSFET equivalent structure showing intrinsic components

Lastly, all power devices have limitations as to what is the maximum power (i.e. voltage and current) that it could withstand safely before it would fail destructively. Therefore, power devices have various current-voltage graphs which illustrate the maximum safe operating boundaries (usually defined as a safe operating area (SOA)) within which, they should be operated to avoid unexpected device failure. The SOA is usually determined by five different limitations as shown in SOA graph presented in Figure 2.12. In the grey area, the device operation is limited by $R_{DS(on)}$. The topmost horizontal current boundary imposes the absolute maximum current that a MOSFET can conduct. The vertical line on the far right of the boundary represents the limitations due to the manufacturer's rated breakdown voltage ($V_{BR(DSS)}$). Another important limitation is imposed by the maximum power dissipation during DC operation. Last but not least, towards the right of the DC operation curve, limitations are imposed by the thermal instability of the MOSFET as explained earlier in this section and later on in section 5.3. However, during DC operation, the separation between the limitations due to maximum power dissipation and thermal instability operation should be obtained

experimentally. Nevertheless, in realistic operating conditions, several different outside of SOA transient events such as short circuit (SC) and unclamped inductive switching (UIS) also occur. Even though such events fall outside of SOA, the devices are still expected to safely withstand such events to a certain extent. The robustness assessment of SiC power MOSFETs under outside of SOA was the key aim of this study and the findings have been presented in section 4 and 5 of this thesis.
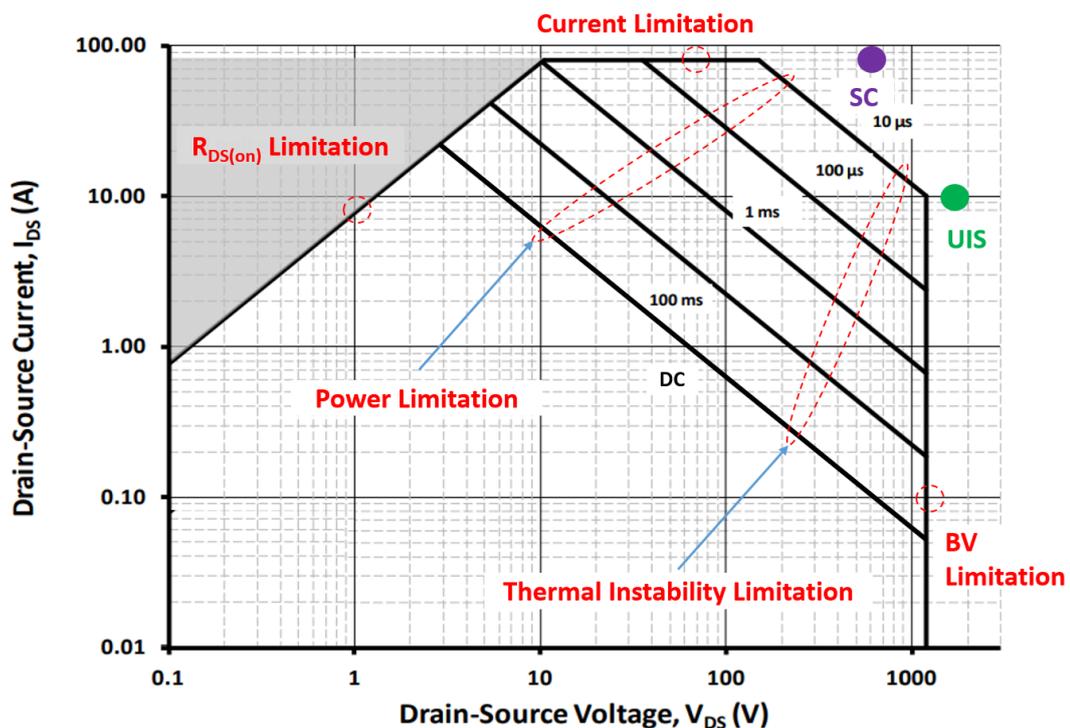
Figure 2.12: Typical safe operating area (SOA) for a power MOSFET

2.3. Device Qualification methodology

As also mentioned earlier in section 2.2.1, SiC fabrication technology has seen challenges with the growth of gate oxide with large density of interface traps as well as the quality of SiC wafers plagued with huge densities of MP and BPDs. However, over the recent years many technological advancements have happened which has resulted in significant improvement in the SiC MOSFET device fabrication procedures which has also led to wide commercial availability of these devices. Along with that also comes the growing interest from industry to

thoroughly investigate these devices in terms of their technology maturity, performance, and robustness. Always whenever a new device hits the market, it is really important that those devices are rigorously tested as per the industry's defined qualification methodologies and test standards in order to assess the technology maturity. Such efforts are nevertheless crucial for better understanding of the device's reliability and the underlying failure mechanisms during operation modes discussed here [42]. The aim of such investigations is to also feedback the device manufacturers to help them rectify the identified issues in order to improve future generations of these devices. A brief overview of some of the most important test standards and qualification methodologies for assessment of device performance, robustness and technology maturity are presented here. The test procedures briefly discussed here are usually imposed by regulatory bodies such as the Joint Electron Device Engineering Council (JEDEC) and British Standards Institution (BSI) and these requirements depending on the application should be met prior to deployment of devices in power electronics circuits. These procedures could be classed into two categories: static and dynamic characterisation.

2.3.1. Static Characterisation

This type of characterisation consists of tests where a device is stressed under constant parameters such as current and voltage. The test methodologies discussed here are part of the JESD22-A108C test standard from JEDEC [43].

High temperature gate bias (HTGB) test

This test has been designed to study the defects in the gate oxide technology which may lead to instability in the threshold voltage (V_{th}) of the device. In this test, the devices are stressed between gate and source with applied static bias equal to or near the maximum rated V_{GS} both positive and negative given in the datasheet for a total of at least 1000 hours. The test is stopped at regular intervals and variations in critical parameters such as gate leakage current (I_{GSS}) and V_{th} are monitored.

High temperature reverse bias (HTRB) test

The aim of this test is to study the quality of the wafer, junctions and device terminations which may lead to an increase in the drain leakage current (I_{LEAK}). In this test, the devices are stressed with positive bias at the drain terminal (i.e. in order to reverse bias the body diode pn junction). The devices are usually stressed between drain and source at or near (at least at 80%) the maximum rated blocking voltage of the device for a total of 1000 hours. Here, the test is stopped at regular intervals and variations in critical parameters such as gate leakage current (I_{GSS}) and the on-state body diode forward voltage drop (V_F) are monitored.

High temperature forward bias (HTFB) test

This test aims to study the defects in the wafer and the junction which may result in a shift of the on-state voltage drop for the pn junction. In this test, the body diode of the device is forward biased (i.e. the device is biased between the source and drain with $V_{GS} \leq 0$). The devices are stressed at or near the maximum current rating levels for also a total of 1000 hours. Such tests are usually carried out on diodes but is particularly of interest for MOSFETs as they have an intrinsic body diode. Variation in parameters such as V_F is monitored at regular intervals.

2.3.2. Dynamic Characterisation

Dynamic characterisation of power devices looks at various different switching transient events which posses stress in a completely different way (i.e. sharp dV/dt and dI/dt which also result in sharp dT_J/dt) as opposed to the static stress applied in the tests discussed earlier in 2.3.1.

Double Pulse Switching Performance

Double pulse switching test is the typical type of test which is performed to study the turn-on and turn-off switching transients of power devices. Furthermore, these tests are quite popular

and widely used to perform switching loss analysis due to non-instantaneous dV_{DS}/dt and dI_D/dt switching transients. It is explained in further detail later in section 3.1 of the thesis.

Overload turn-off Robustness

Such tests are performed where devices are switched off at either overload current or voltage conditions. For overload current, it is expected that the devices are able to withstand at least twice the rated nominal steady-state current at the maximum temperature rating of the device. For overload voltage test conditions, the devices are expected to switch at above 50% of rated nominal blocking voltage. The overvoltage criteria differ from the overcurrent criteria as these devices are usually de-rated as low as 50% for many applications (i.e. 3.3 kV devices are indicatively used at up to 1.8 kV nominal V_{DD}).

Short Circuit Robustness

This type of test stresses the device during short circuit operation where there is no load connected in series with the device to limit device current. In here, I_D is limited by the physics of the device. For this criteria, certain standards have been published by JEDEC such as JESD77-D [44] and JESD24-9 [45] which define the short circuit withstand time (t_{SC}) and short circuit safe operating area (SCSOA). Typically, it is expected that the devices would be able to withstand t_{SC} of at least 10 µs to allow enough time for the intervention of the protection circuitry. Any additional time that a device could withstand at rated voltage and temperature implies an important consideration when competition takes part among manufacturers. SC testing and experimental results are discussed further in section 3 and 4 of the thesis.

Avalanche Breakdown Robustness

Avalanche breakdown robustness of power devices is tested using unclamped inductive switching test. In this test, the device is forced to enter avalanche breakdown operation and their ability to withstand time and dissipate energy in avalanche is studied. Various different

standards from JEDEC exist (such as JESD210A [46], JESD88E [47], and JESD77-D [44]) which tends to define terms and definitions about the avalanche breakdown testing of power devices. UIS testing is discussed further in more detail in section 3 and 5 of the thesis.

3. Experimental Methodologies and Electro-thermal Simulations

In order to obtain a comprehensive and in-depth transient characterisation of SiC power MOSFETs, various different experimental methodologies were developed to perform tests followed by the use of electro-thermal simulations which are explained and discussed in this chapter of the thesis. The overall analysis implemented as part of this study consisted of three stages (discussed in more detail in the next sections) which were functional characterisation, structural characterisation followed by the electro-thermal simulations. Functional tests, usually performed on packaged devices, were designed to study the evolution of electrical behaviour (i.e. voltage and current waveforms) as well the stability of electrical device parameter (i.e. threshold voltage (V_{th})). Once the electrical behaviour and critical limits of the DUT were well-studied through functional tests, structural tests were then carried out. Structural tests were performed on bare die devices using fast transient infrared (IR) thermography. Such test technique is crucial to analyse the current distribution (i.e. surface temperature distribution) within the DUTs leading up to failure test conditions. These tests are performed with an aim to detect formation of hot-spot and/or degradation of the device's surface. Information obtained here helps to distinguish if the failure is either related to the physics of the semiconductor itself or due to degradation of the structural features of the device (i.e. changes in contact metallization etc.). The proposed hypothesis concluded with the help of functional and structural tests were further investigated using 2D technology computer-aided design (TCAD) simulations. A schematic representation of the adapted overall methodology, has been included in Figure 3.1. Moreover, these three stages act within a cycle as they were repeated several times to obtain a wide variety of experimental and simulation results to broaden the understanding of the device's failure mechanism during operating conditions such as short circuit (SC) and avalanche breakdown as later discussed.
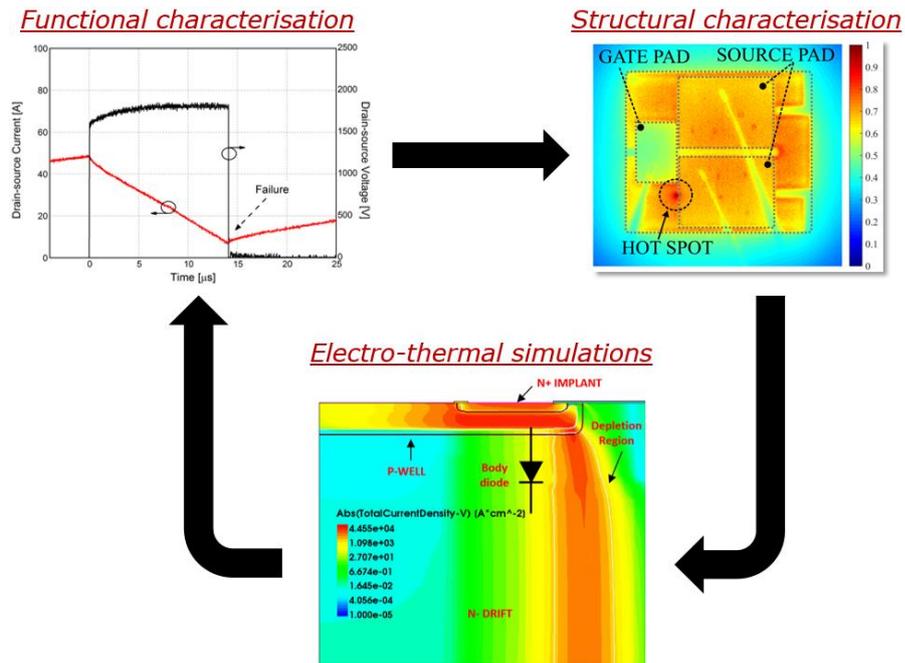
Figure 3.1: Schematic representation of the adapted methodology

3.1. Functional Characterisation

3.1.1. Double-Pulse Tester (DPT) Circuit

In order to investigate the hard switching transient characteristics of power devices, a so-called double-pulse tester (DPT) circuit, a well-established solution, is widely used. A double pulse is sent to the DUT using a signal generator. The pulse width (t_{PULSE}) of each pulse and time between pulses is adjustable via the signal generator. During the first pulse, the inductor current (I_L) is charged up to the desired value (i.e. required loading conditions). The diode (D_{FW}) in parallel with the L_{LOAD} is used for current freewheeling to satisfy the current continuity requirement of L_{LOAD} while the DUT does not conduct between pulses. The circuit schematic of a DPT circuit is presented in Figure 3.2. The circuit contains a device under test (DUT), load inductor (L_{LOAD}), a freewheeling diode (D_{FW}) and a capacitor bank (C_{BANK}). Here, L_{LOAD} used were air wound inductors to allow achieving high current levels without having issues with core saturation.
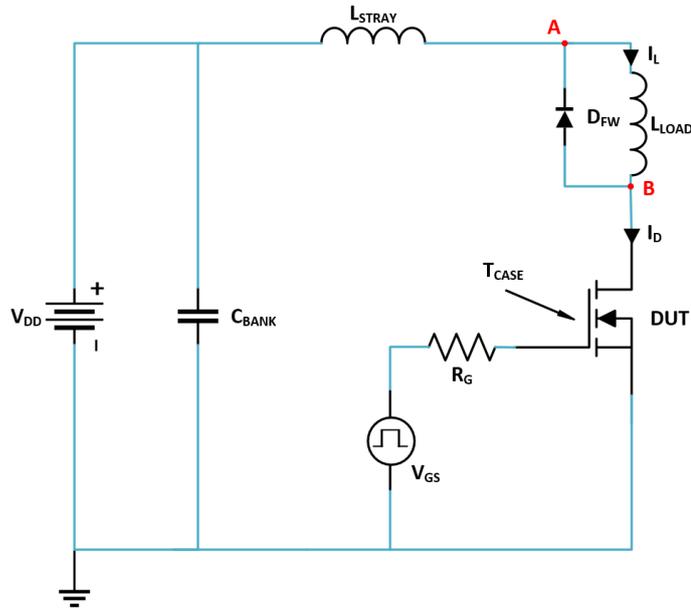
Figure 3.2: *Circuit Schematic for DPT circuit*

The implemented hardware test setup is shown in Figure 3.3. The overall C_{BANK} has a total value of 1 mF with a rating of 1.8 kV to allow input voltage (V_{DD}) characterisation up to around 1.5 kV. Both the DUT and D_{FW} are mounted horizontally with an independent thermal connection onto a hotplate to allow characterisation at different case temperatures (T_{CASE}) up to 200 $^\circ$C. A high precision digital programmable signal generator is used to ensure fine control of the gate signal, with a resolution of 10 ns. In order to minimise stray inductance (L_{STRAY}) to avoid voltage overshoot, a double-sided printed circuit board (PCB) was used (as a power plane) and the use of wires was minimised by vertically mounting the gate driver directly. L_{STRAY} is also used as one of the important test parameters since it has an influence on the switching performance of the device. Indeed, theoretically, SiC as a material offers faster switching speeds than its Si counterparts. However, in practicality, parasitic elements impose limitations on the actual possible switching speeds as well as give rise to switching losses.
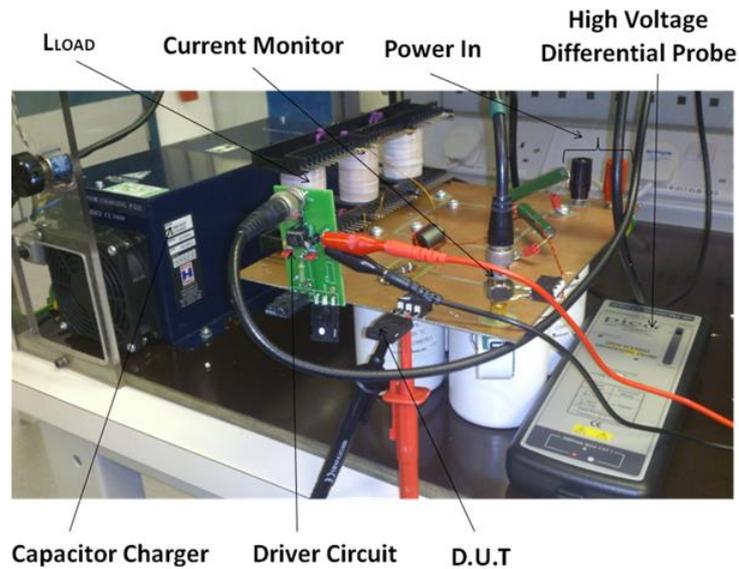
Figure 3.3: Implemented DPT circuit

The DPT circuit developed here is a unified test setup which could be used to perform different kinds of tests to characterise SiC power MOSFETs with simple modifications between node A and B labelled in Figure 3.2. The tests are as follows:

- ✓ Performance Characterisation:

  - Nominal double pulse switching – No modifications to DPT circuit

- ✓ Robustness Characterisation:

  - Overload turn-off (OLTO) switching – No modifications to DPT circuit

  - Short circuit (SC) withstand capability – Create short between node A and B

  - Unclamped inductive switching (UIS) – Remove D_{FW} between node A and B

Nominal double pulse switching test helps to extract all the required information about turn-on and turn-off transitions of an active switch and freewheeling diode at the same time under variable electrical and thermal conditions. Hence, making this test setup quite popular within the industry. They are also used to accurately estimate the switching losses for a given loading condition within an inverter. On the other hand, the robustness tests mentioned here reproduce unintended, nevertheless stressful and potentially frequent operating conditions

which DUTs may experience within a power converter. Such tests are part of standard technology assessment and validation campaigns prior to deployment of new switches within power converters.

The typical voltage and current waveforms for double pulse switching are presented in Figure 3.4. It can be divided into five time durations from t_0 to t_4. Time t_0 represents when the DUT is blocking V_{DD} and therefore $V_{GS} = 0$ V and $I_L = I_D = 0$ A. During time t_1, the DUT receives the first pulse so it turns ON (when $V_{GS} > V_{GS(th)}$) and V_{DD} drops across L_{LOAD}. At the same time, I_D and I_L increase linearly as dictated by L_{LOAD}. The DUT turns off (when $V_{GS} < V_{GS(th)}$) at the start of time t_2 (short delay between pulses) and again goes into blocking state ($V_{DS} = V_{DD}$). Here, I_D goes to 0 but I_L freewheels through D_{FW}. The DUT turns ON again during the second pulse (time t_3) and I_D continues to flow approximately from the same value left at the end of the first pulse. Again when the device turns OFF at the end of the second pulse, time t_4, the device once again goes back to blocking V_{DD} and I_D goes to zero. However, once again, I_L does not immediately go to zero due to the energy stored in L_{LOAD}. The I_L freewheels through D_{FW} and eventually decreases to zero as a result of the series resistances of D_{FW} and L_{LOAD}.
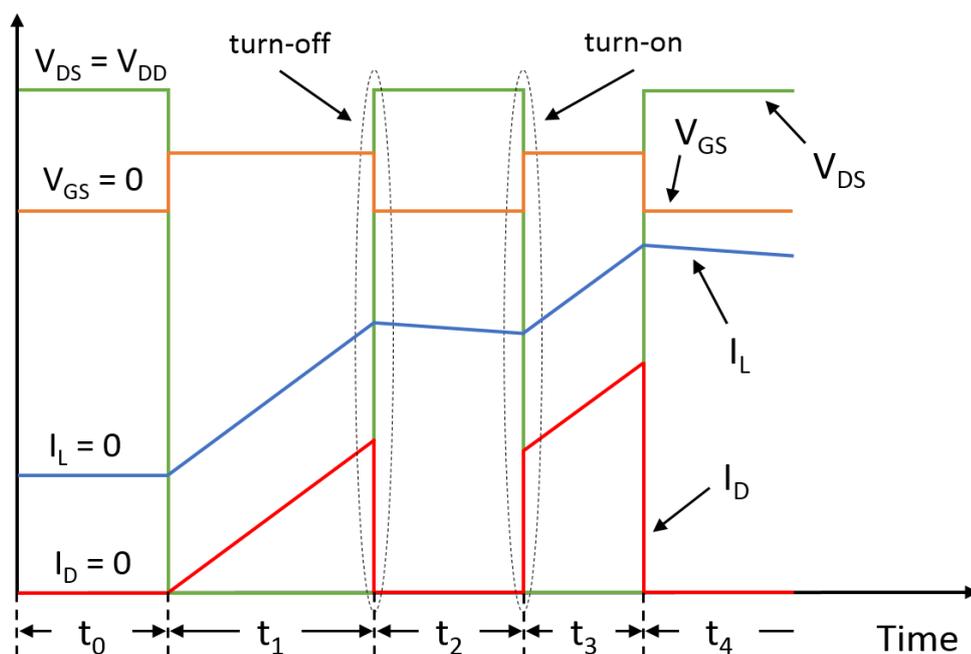
Figure 3.4: *Typical double pulse switching – V_{DS}, V_{GS}, I_D and I_L waveforms*

The falling edge of the first pulse and the rising edge of the second pulse correspond to the turn-off and turn-on current and voltage transients of the DUT. Figure 3.5 shows the zoom in of the turn-on and turn-off switching transients. As expected, the switching transients are not instantaneous which results in switching energy losses (E_{SW}). These losses vary on parameters such as the level of current and voltage being switched as well as T_{CASE}. The self-heating during double pulse switching test was considered to be negligible due to relatively lower power dissipation levels as compared to SC and UIS. Here, the voltage (ΔV) and current (ΔI) overshoot demonstrate the presence of parasitic elements in the circuit. The V_{DS} overshoot during turn-off is as a result of L_{STRAY}. On the other hand, during turn-on, there also exists I_D overshoot which occurs due to the charging of the drain-source capacitance (C_{DS}). The pulse width is suitably adjusted to switch the desired current levels.
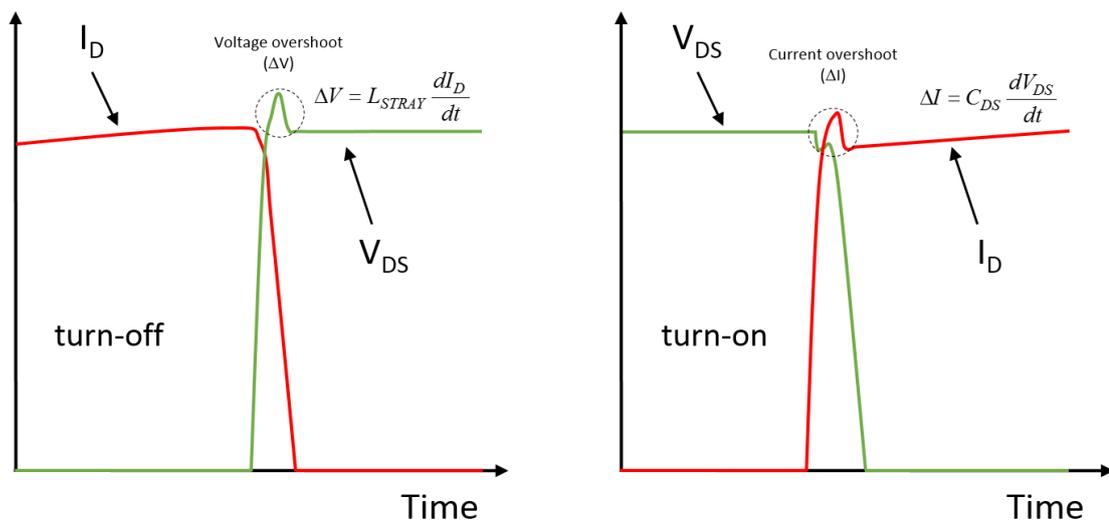
Figure 3.5: *Turn-on and turn-off switching transients (zoomed in) – V_{DS} and I_D waveforms*

Furthermore, power devices are usually expected to withstand current and voltage exceeding the nominal continuous ratings. OLTO test is used to demonstrate safe turn-off of the device under overload conditions. In this test, only a single pulse is sent to DUT and I_L increases and then when DUT is switched off, I_D drops to zero and I_L freewheels in the diode which finally drops to zero. OLTO test is usually carried out for both overcurrent and overvoltage test conditions at different T_{CASE}. For overcurrent turn-off, the device should withstand at least

twice the rated continuous drain current given in the datasheet. The value for L_{LOAD} and t_{PULSE} are the usual parameters to obtain the desired I_D current levels. Moreover, these devices always have a margin of de-rating that needs to be considered for the maximum OFF-state voltage peak transient during the design of a power converter. In many applications, a de-rating of 50% is implemented (i.e. devices rated at 1.2 kV are used up to indicatively 600 V nominal input voltage). Overvoltage tests are usually performed at switching voltage levels higher than 50% of the voltage rating. The typical voltage and current waveforms for OLTO test are presented in Figure 3.6.
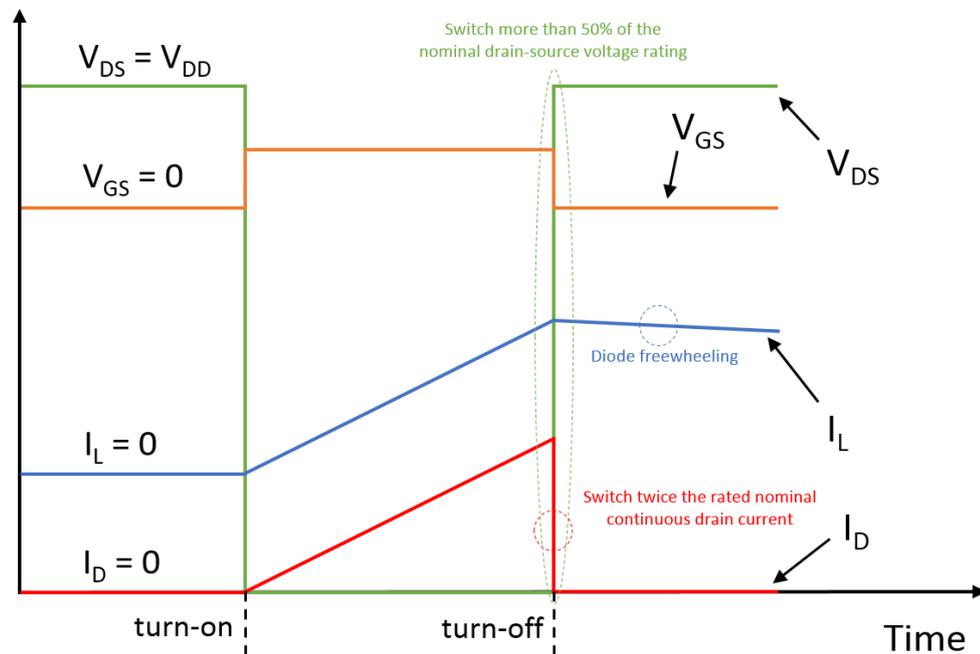
Figure 3.6: *Typical OLTO switching – V_{DS}, V_{GS}, I_D and I_L waveforms*

Lastly, to finish off section 3.1.1 on DPT setup, some experimental results are also included here to complement the quality of the thesis. Experimental turn-off and turn-on double pulse switching waveforms for test conditions: V_{DD} = 400 V, V_{GS} = 18 V, L_{LOAD} = 500 µH and T_{CASE} = 150 °C are included in Figure 3.7 (a) and (b) respectively. The t_{PULSE} and L_{LOAD} are usually adjusted to obtain the desired switching current levels. Moreover, OLTO's experimental switching waveforms for test conditions: V_{DD} = 400 V, V_{GS} = 18 V, L_{LOAD} = 1 mH and T_{CASE} = 150 °C are presented in Figure 3.8. It is worth noting that the device is able to turn off without any

problem even at current levels significantly higher than the rated nominal current. This shows

great device performance without any current tails.
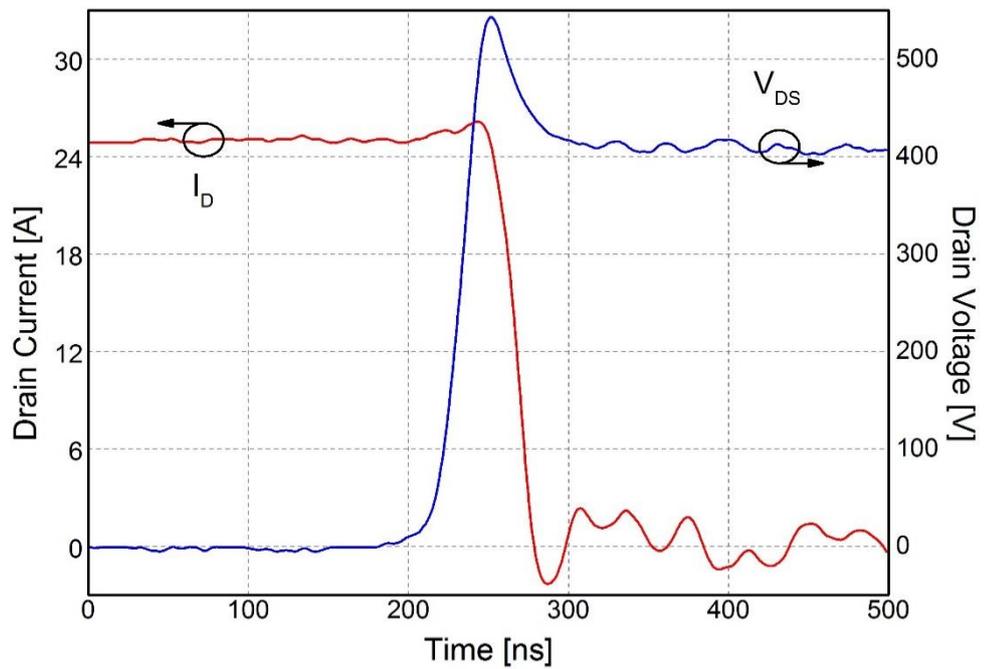
(a)
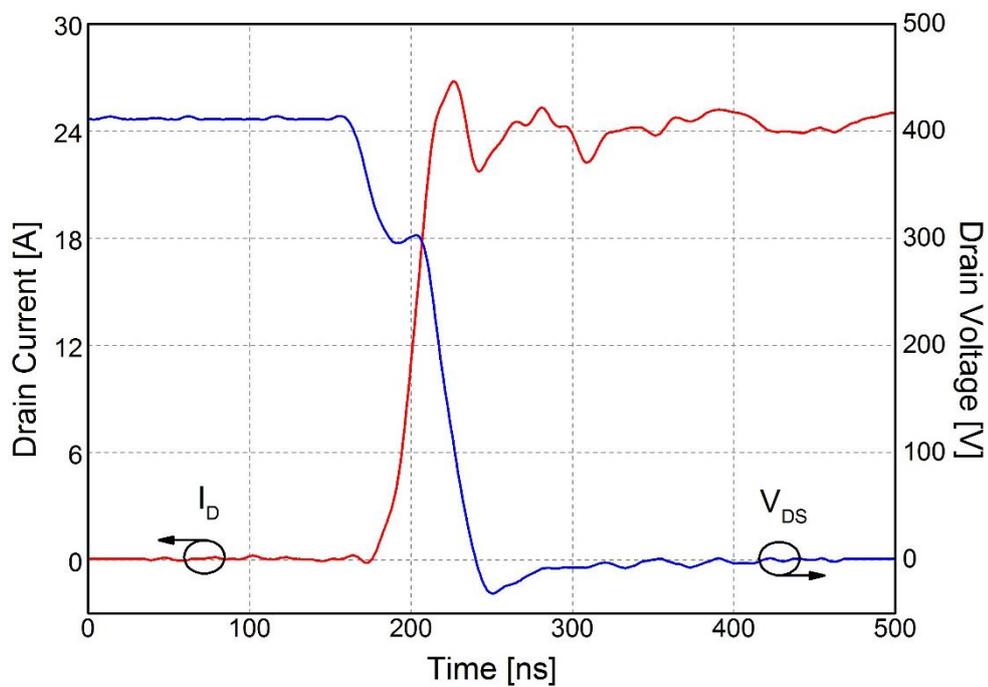
(b)

Figure 3.7: *MOSFET's switching transient – V_{DS} and I_D waveforms; (a) – turn-off; (b) – turn-on*
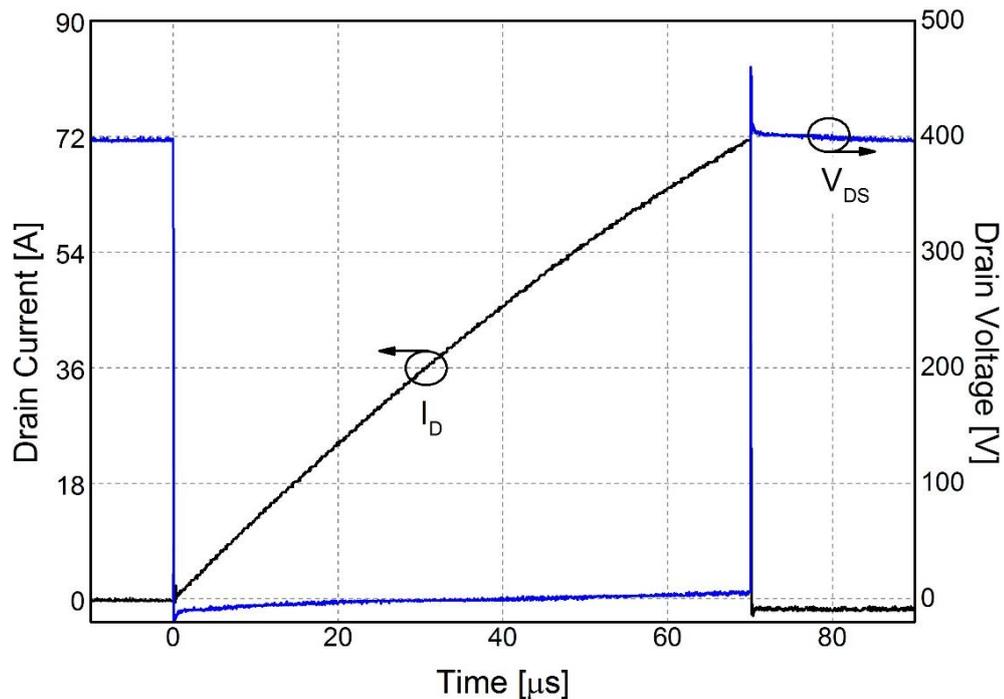
Figure 3.8: *Experimental OLTO current switching – V_{DS} and I_D waveforms*

The current measurements for the DUT, D_{FW}, and L_{LOAD} were measured with the help of current transformer and Rogowski current transducer depending on suitability and ease of measurements. A current transformer produces current in the secondary winding which is proportional to the current flowing in the primary. The 13W0100 current transformer from LILCO [48] was used which had a high sensitivity of 0.1 V/A, a very high frequency bandwidth (BW) of 25 MHz and BNC output socket. The CWT 1B Rogowski current transducer from PEM [49] was used. It consists of a coil, an integrator circuit along with a BNC socket output. The clip around coil is thin and flexible enough to place it around the leg of the device in a TO-247 package. The integrated circuit converts the measured current signal into a voltage signal (proportional to each other). It also features a high sensitivity of 20 mV/A with a very high frequency bandwidth of 30 MHz. High BW of both measurements techniques makes them a suitable option for measuring sharp dI/dt.

The voltage measurements were made using a differential voltage probe. The TESTEC TT-SI 9110 voltage probe [50] was used which a high BW of 100 MHz.

3.1.2. Short circuit (SC) Operation

The circuit schematic for testing a device during SC is shown in Figure 3.9. In order to create the SC condition, D_{FW} is removed and the inductive load, L_{Load}, is permanently shorted between node A and B from the circuit schematic shown in 3.1.1. SC represents an unintended and undesirable operating condition, which is extremely stressful for the device. However, it can be a frequently occurring event in many industrial settings e.g. motor drive applications. Typical applications require devices to be capable of withstanding short circuit duration (t_{SC}) of at least 10 µs at usually 80% of their rated nominal blocking voltage ($V_{DS(max)}$) dictated on the datasheet [51]. A t_{SC} value of 10 µs is associated with the usual intervention time requirement for the action of the protection circuitry.
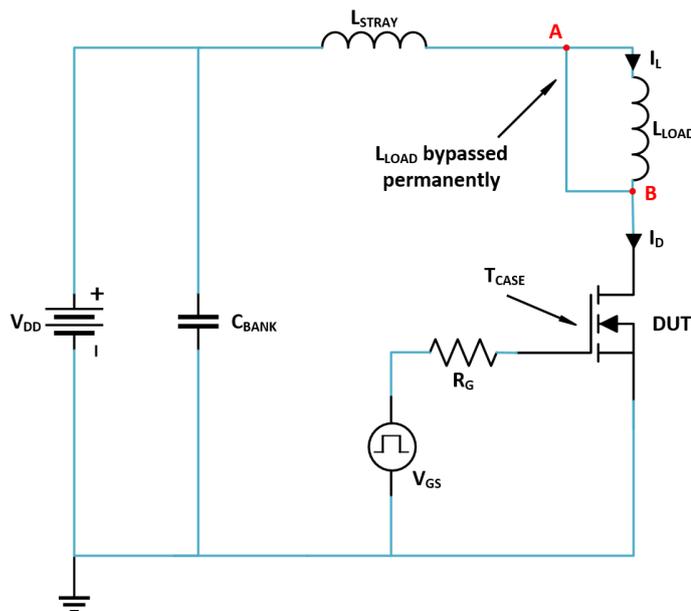
Figure 3.9: *Circuit schematic representing SC test*

SC events could be classified into two different types. The Hard Switch Fault (HSL) – Type I takes place when the device is subjected to the desired dc link input voltage (V_{DD}) in the OFF state and it is later switched ON with a single gate pulse (t_{PULSE}) without any load connected between the source and ground. Fault Under Load (FUL) – Type II occurs when the device is already in conduction carrying load current (ON state and V_{DS} is low) and a sudden fault

condition bypasses the load being driven resulting in shoot-through. In Type II, as the device experiences SC, a sharp dV/dt will result in an increase of V_{DS} which will also result in the flow of current through the Miller capacitance. As a consequence, gate potential will shift higher, therefore, resulting in a relatively higher SC current [52, 53]. For this project, all the SC tests were performed using Type I – Hard Switch Fault (HSL) condition. Here, for SC, a single gate pulse with a given duration (t_{ON}) is sent to the gate of the DUT.

The typical current and voltage waveforms during non-destructive SC test are presented in Figure 3.10. When the DUT is switched ON, the drain current (I_D) rises immediately according to the gate resistance (R_G) of the gate driver, DUT's internal gate resistance ($R_{G(INT)}$) and gate capacitance (C_{GS}). Afterwards, I_D reaches a peak value, $I_{SC(pk)}$, followed by a decrease and then it eventually settles at a certain value with relatively small variation for the remaining of t_{SC}. The decrease in the SC current is associated with the self-heating of the device which causes the on-state resistance (R_{ON}) to increase thus causing lowering of the current. The specific on-state resistance ($R_{ON,sp}$) could be calculated using equation 3.1 [10]. R_{ON} of a SiC MOSFET has a positive temperature coefficient which explains lowering of I_{SC} during the pulse [54]. Moreover, The V_{DS} also experiences voltage undershoot and overshoot at device turn-on and turn-off respectively, as a result of the inevitable presence of the L_{STRAY} in the circuit and the sharp change in current (dI_D/dt). At DUT turn-on, I_D starts to flow through the circuit. The quick change of current (dI_D/dt) through the parasitic element (L_{STRAY}) results in a fixed value of back emf being produced across them, as expressed by equation 3.2. The back emf (V_{STRAY}) produced across the parasitic element will act against V_{DD} which results in the V_{DS} undershoot. At the same time, at DUT turn-off, the current would decrease rapidly. This sudden change of current (dI_D/dt) across L_{STRAY} is undesirable. L_{STRAY} tries to maintain the flow of current by inducing a voltage (V_{STRAY}) in the opposite direction thus causing V_{DS} overshoot at turn-off.
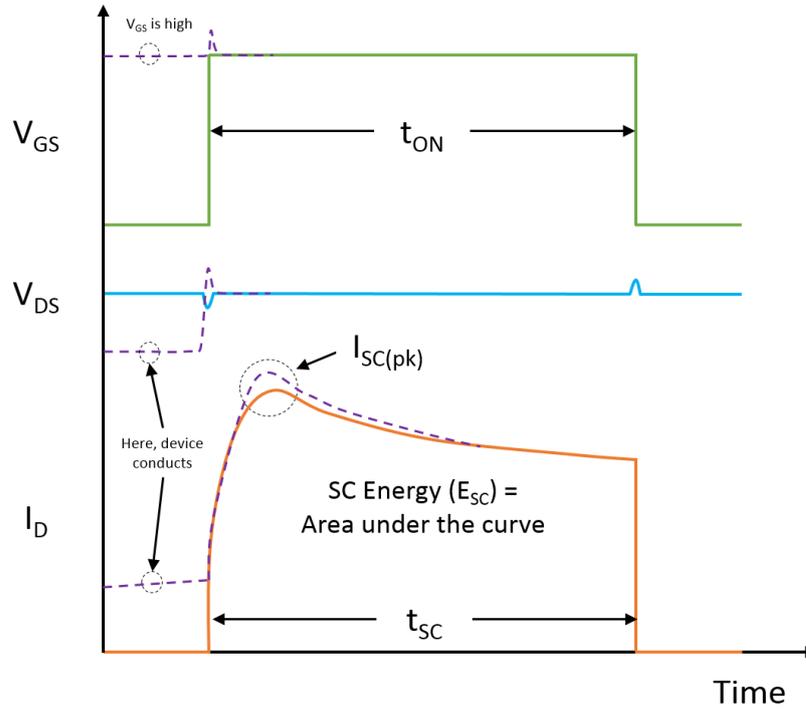
Figure 3.10: Typical experimental current and voltage waveforms for non-destructive SC test

– Solid: HSF and dashed: FUL

$$R_{ON,sp} = \frac{W_{DRIFT}}{q\mu_n N_{DRIFT}} \qquad (3.1)$$

$$V_{STRAY} = L_{STRAY} \frac{dI_D}{dt} \qquad (3.2)$$

The instantaneous power dissipation during SC test (P_{SC}) can be calculated using equation 3.3. Since energy is the integral of voltage and current (power) therefore, equation 3.3 could be integrated to give equation 3.4 which can be used to calculate the SC energy dissipation (E_{SC}).

$$P_{SC}(t) = V_{DS}(t) \cdot I_D(t)dt \qquad (3.3)$$

$$E_{SC} = \int_0^{t_{SC}} V_{DS}(t) \cdot I_D(t)dt \qquad (3.4)$$

In the beginning of any test, for a given V_{DD} and $P_{SC(pk)}$, t_{ON} was chosen carefully to have small E_{SC} in order not to unnecessarily destroy the DUT straight away. Afterwards, the approach was to gradually increase t_{ON} (also increasing E_{SC}) until DUT was destroyed or degraded with an

aim to identify the operating limitations of DUT and identify precursors leading to failure. The R_G value used for all the tests was 4.7 Ω. The SC results presented here were carried out for a range of input voltage (V_{DD}), case temperature (T_{CASE}) and gate voltage (V_{GS}).
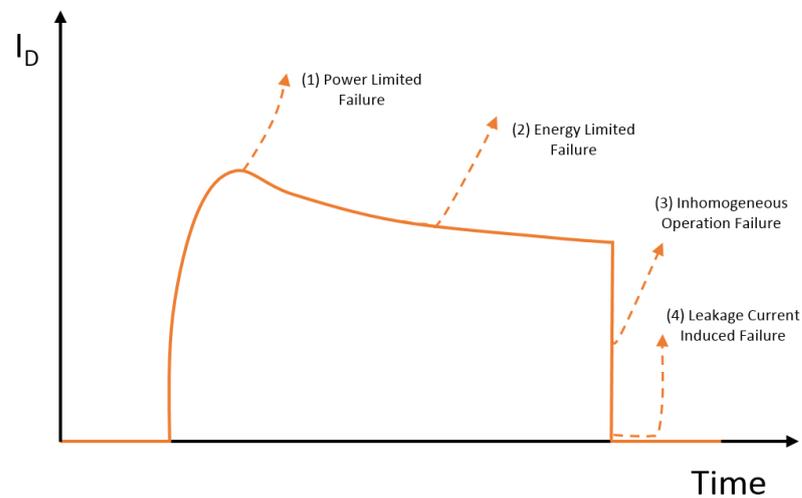
Figure 3.11: *Illustration of SC failure modes within power devices*

Lastly, a brief overview of the known SC failure modes for power devices is also discussed here along with the aid of Figure 3.11. The failure modes are as follows [55, 56]:

1) **Power Limited Failure:** This failure mode occurs near $I_{SC(pk)}$ after device turn-on due to really high power (i.e. High V_{DD}). It is also known as an electrical failure mode.

2) **Energy Limited Failure:** In this case, the device fails while in steady state as a result of high energy dissipation exceeds the critical failure energy that the device can withstand. This is also known as a thermal failure mode.

3) **Inhomogeneous Operation Failure:** It is also known as turn-off failure mode. It occurs at device turn-off caused by the excessive surge in power due to voltage overshoot caused by sharp dI/dt.

4) **Leakage Current Induced Failure:** This failure occurs a few microseconds after the device returns to the blocking state. It happens as a result of a localised current conduction causing a really high leakage current to flow eventually leading to thermal runaway.

3.1.3. Unclamped Inductive Switching (UIS) Operation

Unclamped inductive switching (UIS) test is the typical test carried out to assess the avalanche ruggedness of a power MOSFET within the industry. It represents a stressful event for the power MOSFET which could rather be a more frequent event in high switching frequency application driving inductive loads (e.g. motor drive applications). Avalanche ruggedness of a power MOSFET is defined as its ability to sustain avalanche current (I_{AV}) under unclamped switching load conditions [57]. Avalanche ruggedness is an important device feature which enables snubber-less converter design which would potentially result in cost reduction, weight reduction, and smaller volumes. At the same time, certain automotive applications such as engine control units (ECUs) and anti-locking braking systems also make use of this feature [58]. These applications require devices to consistently (i.e. repetitive) dissipate overload transient energy released from inductive loads namely motors and actuator controlled solenoids. Switches in such applications are required to dissipate energy (E_{AV}) while in avalanche breakdown regime (i.e. withstand a certain time in avalanche (t_{AV})). As such, there is no fixed requirement for E_{AV} dissipation or I_{AV} and vary depending on the application.
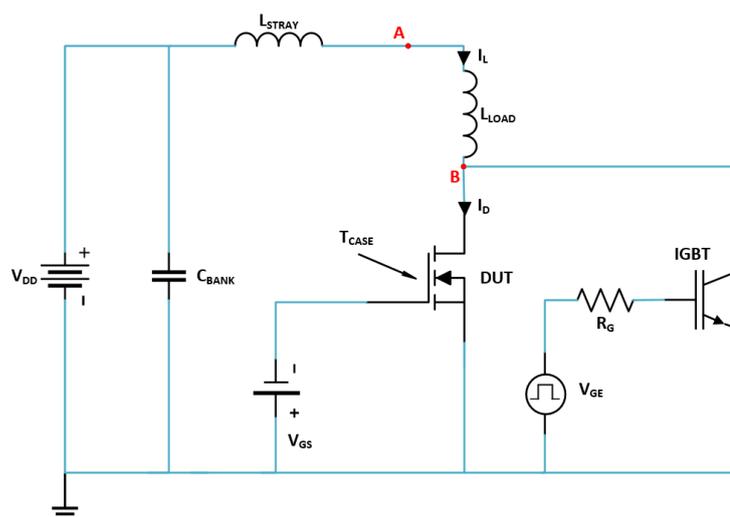
Figure 3.12: *Circuit schematic representing UIS test*

The circuit schematic for assessing avalanche ruggedness of devices is given in Figure 3.12. For UIS test, D_{FW} between node A and B from the DPT circuit referred in section 3.1.1 is removed.

An additional auxiliary IGBT with a breakdown voltage higher than the DUT (3 kV IGBT) is connected in parallel to the DUT. The IGBT is used to ramp up the inductor current (I_L) to the desired value in order to avoid self-heating of the DUT prior to its avalanche breakdown. Here, the IGBT (IXBH12N300) used was provided from IXYS [59].

The typical voltage and current waveforms during non-destructive UIS transient are shown in Figure 3.13. During the UIS test, the DUT is kept biased with $V_{GS} \leq 0$ V to keep it off. The t_{ON} of the IGBT is selected to obtain the desired peak avalanche current (I_{AV}). The linear rise of I_L during t_{ON} of the IGBT is dictated by the L_{LOAD} value and can be expressed using equation 3.5. After the IGBT turn-off, the DUT enters avalanche breakdown since L_{LOAD} generates back emf as I_L cannot immediately go to zero due to the current continuity condition of an inductor. In other words, the energy stored in L_{LOAD} during unclamped load dumping is dissipated into the device while in avalanche breakdown. After t_{AV} during safe UIS event, V_{DS} goes back to blocking state ($V_{DS} = V_{DD}$). The avalanche energy (E_{AV}) dissipation can be expressed using Equation 3.6. As already mentioned in earlier sections, L_{STRAY} refers to the parasitic elements in the circuit. Here, they are considered as negligible when compared to L_{LOAD}.
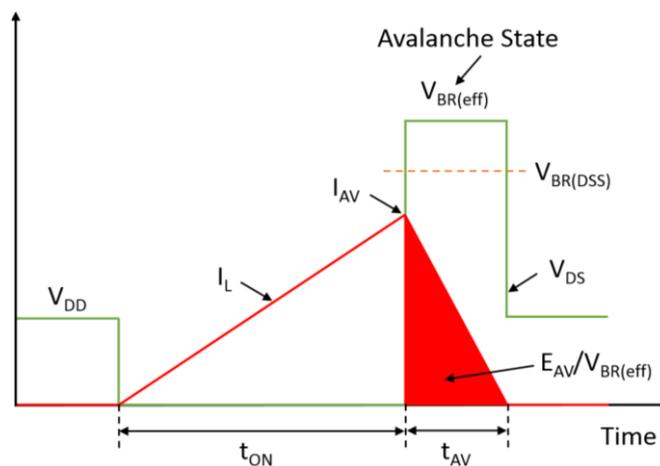
Figure 3.13: *Typical experimental current and voltage waveforms for non-destructive UIS transient*

$$V_{DD} = L_{LOAD} \frac{dI_{AV}}{dt_{ON}} \tag{3.5}$$

$$E_{AV} = \frac{1}{2} L_{LOAD} I_{AV}{}^2 \frac{V_{BR(eff)}}{V_{BR(eff)} - V_{DD}} \tag{3.6}$$

For all test condition, t_{ON} of the IGBT was gradually increased (increasing E_{AV}) until the DUT failed, with an aim to identify the operating limitations of the device and identify precursors of failure and interpret the failure mechanism.

The failure mechanism of N-MOS Si power MOSFETs during avalanche breakdown is well-understood. It is mainly attributed to the activation of the intrinsic parasitic npn BJT. Over time, various different Si power MOSFET structures evolved, which significantly targeted the parasitic BJT element to delay its activation and therefore enhance robustness [60]. Activation of parasitic BJT in Si power MOSFETs also becomes more likely as the temperature is increased. The base-emitter voltage (V_{BE}) required for BJT activation in Si is 0.6 V – 0.7 V at ambient temperature (T_A) and decreases at a rate of ~ 2 mV/K. On the other hand, it is expected that the wider bandgap of SiC suppresses the activation of the parasitic BJT during typical UIS events (i.e. with typical values of switched currents and ensuing temperature evolution). In SiC, the intrinsic carrier concentration (n_i) remains several orders of magnitude lower than in Si even at very high temperatures and the activation V_{BE} voltage of the intrinsic BJT is much higher (indicatively 2.5 V – 3 V at room temperature) and does not decrease as much with temperature [17].

3.1.4. Three-Phase Inverter Circuit

In order to assess the body diode reliability of SiC power MOSFETs, an inverter test setup was designed and constructed. An inverter circuit converts a DC input voltage to an AC output voltage. They are widely used in applications such as ac motor drives and uninterruptible ac power supplies to synthesize a sinusoidal AC output with controlled frequency and magnitude.

The DC voltage for inverter input can be provided either from a diode rectifier or a DC voltage supply [61].

Power MOSFET is a normally OFF voltage controlled transistor switch with bi-directional current flow capability. On top of that, it also offers an intrinsic body diode which eliminates the need for using an anti-parallel diode for current freewheeling in an inverter. These features make them a popular choice for synchronous rectification within inverters [4]. It is therefore really important to investigate the stability of electrical parameters (i.e. body diode on-state voltage drop (V_F) and drain leakage current (I_{LEAK})) associated to the body diode structure of SiC power MOSFETs. The experiment was designed to allow the inverter to operate for 1000 hours for a given set of test conditions. During that time, the inverter was stopped at regular intervals in between to monitor if any degradation of the body diode had occurred by measuring electrical parameters of the DUTs mentioned earlier. Such characterisation of SiC power MOSFETs under realistic operating conditions is a necessary requirement prior to their implementation within industrial and commercial applications.
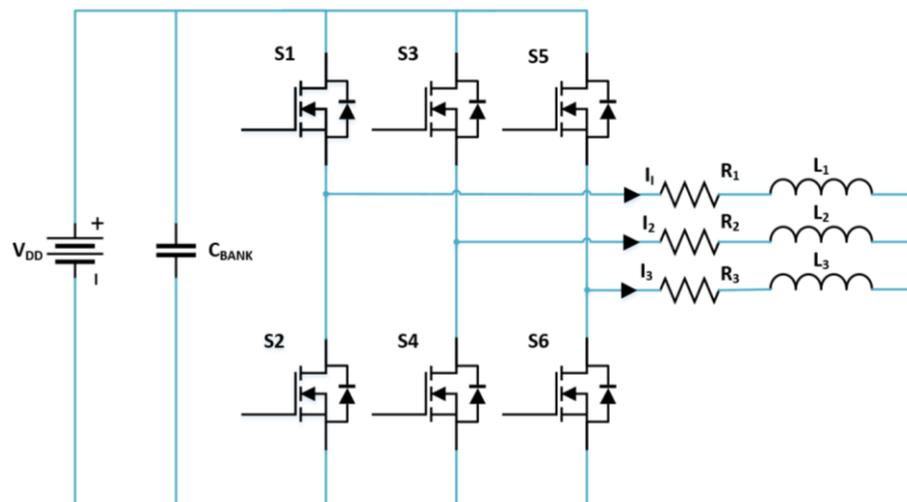
Figure 3.14: Circuit schematic representing an Inverter

The three-phase two-level inverter test setup designed for body diode characterisation was connected using star connected inductive load ($L_1 = L_2 = L_3$ = 20 mH). Here, in the designed

setup, no resistive load was considered in order to avoid unnecessary dissipation of active power over the long running time of the experiments. The schematic of the implemented inverter is shown in Figure 3.14. The series resistances R_1, R_2, and R_3 represent the series equivalent resistance for each inductor L_1, L_2, and L_3 respectively. The circuit consists of three legs, one for each phase and each leg has two switches with a total of six active switches. The diodes in parallel to the switches represent the body diode. The implemented circuit hardware test circuit based on the circuit schematic presented in Figure 3.14 is included in Figure 3.15. The designed power plane was a double sided PCB with 4 oz. of copper thickness and the gate drivers were mounted vertically onto the power plane PCB directly without using wires in order to avoid voltage overshoot by minimising L_{STRAY}. The overall C_{BANK} has a total value of 3 mF with a voltage rating of 900 V to allow V_{DD} characterisation up to ca. 600 V. The DUTs were horizontally screwed onto a heatsink to allow characterisation of different T_{CASE} of up to 150 °C. A dedicated heat sink, as seen in Figure 3.15, was designed using power resistors and fans for heating up and cooling down respectively in order to be able to maintain the desired T_{CASE} for DUTs during operation as well as for measurements of parameters. The spring type connectors were used for connecting the DUTs which allowed easy disconnecting of DUTs from the power PCB during parameter measurements.
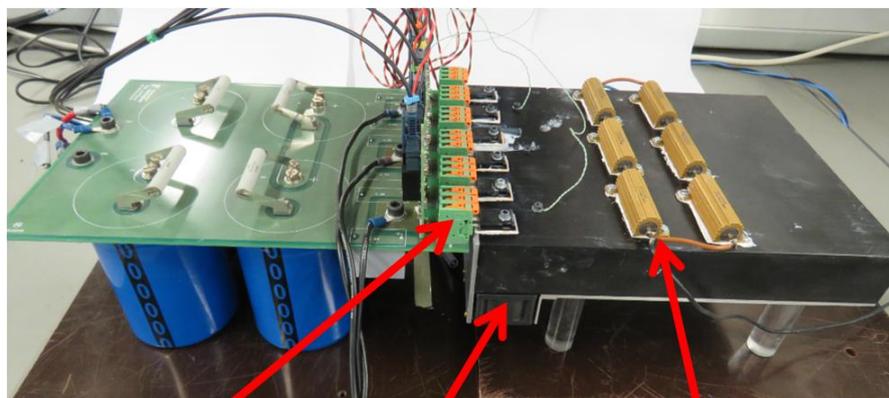
Connectors   **_Fans_**   **_Power Resistors_**

Figure 3.15: Implemented Inverter hardware test setup

An open-loop control using pulse width modulation (PWM) scheme was implemented for the six switches using an Altera DE0-Nano FPGA development board [62]. The illustrative representation of PWM scheme is included in Figure 3.16. The switching carrier signal (triangular wave) and modulating signal (sine wave) with desired frequencies are both input to a comparator to generate a PWM signal. In other words, the digital signal pulses generated at the output of the comparator modulate with the amplitude of the input modulating signal. The generated PWM signal has a fixed frequency (same as the switching frequency (f_{SW})) but the duty cycle of the pulses vary to effectively control the amount of power delivered to the load. Here, the term modulation index (m – usually varies between 0 and 1) is defined as the ratio of the amplitude of the modulating signal (V_m) to that of the carrier signal (V_{SW}) as also expressed using equation 3.7.

$$m = \frac{V_m}{V_{SW}}$$ (3.7)
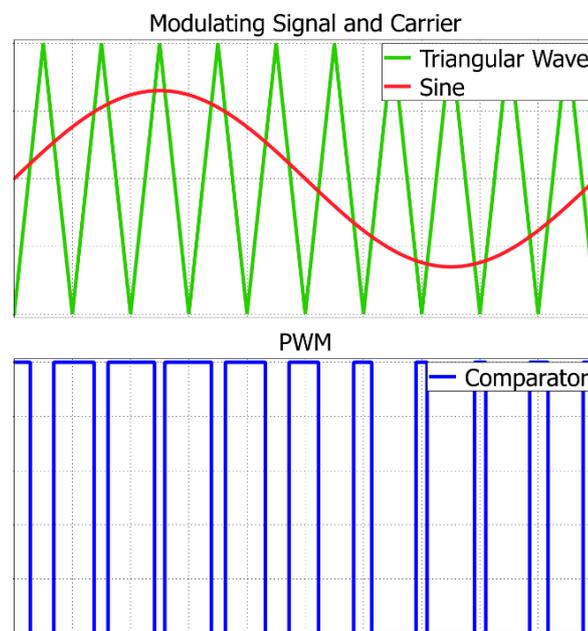
Figure 3.16: *Illustration of PWM scheme*

Moreover, in an ordinary three-phase inverter, the gate signals of the two switches in one leg should be complementary with an insertion of dead time between the commutations to avoid

any shoot-through as illustrated in Figure 3.17. During the dead time ($V_{GS} < V_{GS(th)}$), the body diode of the MOSFET is used for current conduction. After the dead time, the MOSFET is turned ON (i.e. $V_{GS} > V_{GS(th)}$) and then, the device current is diverted from the body diode through to the channel and hence the technique synchronous rectification as also shown in Figure 3.18. This technique is used to benefit from the lower on-state drain-source resistance ($R_{DS(ON)}$) during reverse current conduction to reduce conduction losses and increase the inverter efficiency. The low $R_{DS(ON)}$ results in on-state voltage drop across drain-source which is lower than V_F thus a reduction in device losses. It is not usually always the case for higher current I_D levels at which the body diode conduction may outperform the on-state reverse conduction. Hence, it is important to optimise the operation of an inverter in reference to the static characteristics provided in the datasheet. Furthermore, it is also required that the switching commutation in each leg has to be phase shifted by 120° and therefore phase currents (I_1, I_2, and I_3) are also phase shifted by 120° among them.
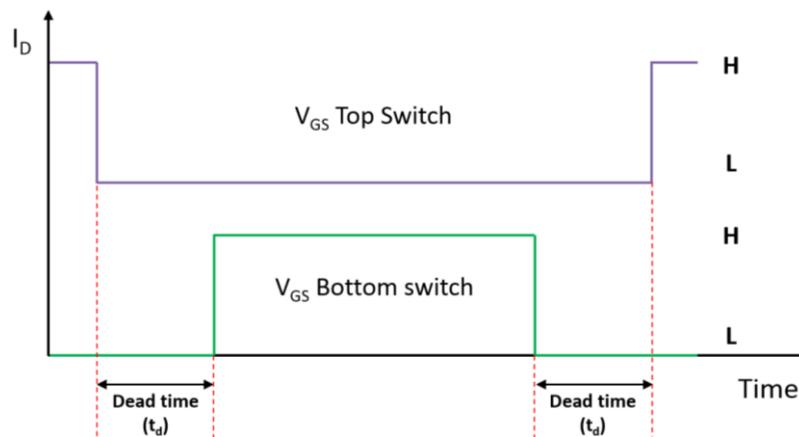
Figure 3.17: *Illustration of dead time*

Reverse Current Conduction in Inverter
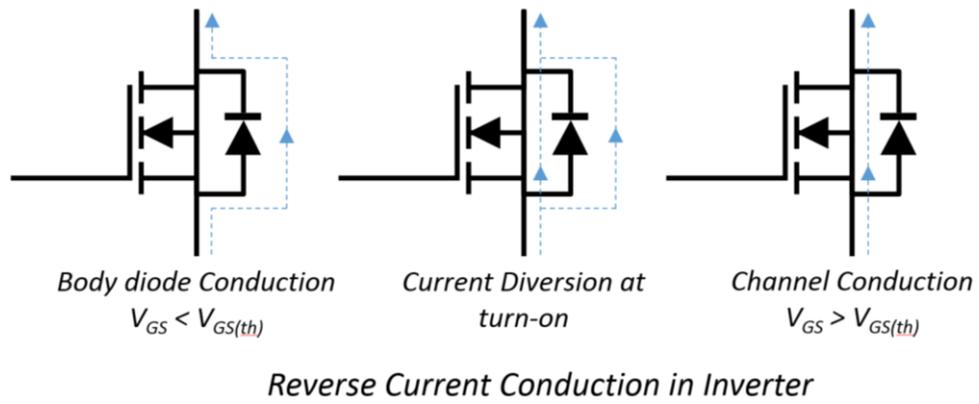
Figure 3.18: Reverse current conduction in an inverter [63]

3.1.5. MOSFET Gate Drive

A gate driver circuit plays an important role in power electronics circuits as they involve control of switching devices. A gate driver chip has an integrated circuit (IC) usually consisting of a push-pull stage which amplifies a low power input signal from the signal generator to produce a high current drive signal at the output which is used to drive the gate of the power MOSFET. SiC Power MOSFETs are voltage controlled devices with really high input impedance and therefore require very small gate-source current (I_{GS}) during conduction. However, respectively at turn-on and turn-off (switching transients), in-rush and out-rush current is required to charge and discharge the gate-source capacitance (C_{GS}) within the MOSFET. The gate driver IC used was from IXYS [64] which had a maximum output current capability of 9 A to allow fast switching transients. Moreover, the gate driver used had the capability to provide maximum voltage swing of -5 V / 20 V.

3.2. Structural Characterisation

3.2.1. Infrared (IR) Thermography

An advanced infrared (IR) thermography technique, custom design as elaborated in [65], was used on bare die SiC power MOSFETs in order to obtain the device's surface temperature during SC and UIS test transients. IR thermography technique was used as it can provide additional information about the chip that could not be extracted from functional characterization using packaged devices. Information obtained from IR analysis such as the formation of the hotspot and/or degradation of the chip surface eventually helps to predict failure mechanisms under the investigated test operating conditions.

The IR test setup features equivalent time sampling method with a frame rate capability of up to 1 MHz which allows acquisition of fast transient dynamics. It is also possible to capture the temperature distribution and thus the current distribution of the device at any time instance during the test using a single shot as well as multiple shots. The IR camera trigger and gate drive signals were provided using an FPGA board. The point of capture is chosen carefully to obtain the maximum DUT's surface temperature. The integration time for the IR camera was set to 1 μs and two-point calibration procedure was carried out to compensate for the emissivity contrast effect [66]. The surface temperature of the device reached (well above 500 °C) during the test which surpassed the calibration range of the camera. So, the thermal images were post-processed within MATLAB to represent a normalized temperature (T_n) distribution (using equation 3.8).

$$T_n = \frac{T - T_0}{T_{max} - T_0}$$

(3.8)

Figure 3.19 presents an illustrative description of the IR experimental test setup which was used for structural characterization of the DUTs. The picture of the actual IR experimental test setup hardware is also included here as shown in Figure 3.20.
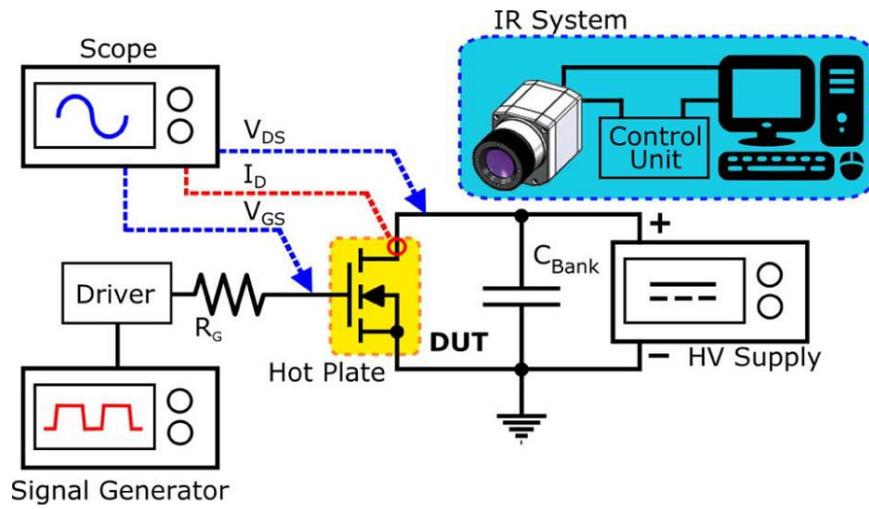
Figure 3.19: *Illustrative description of the IR experimental test setup*
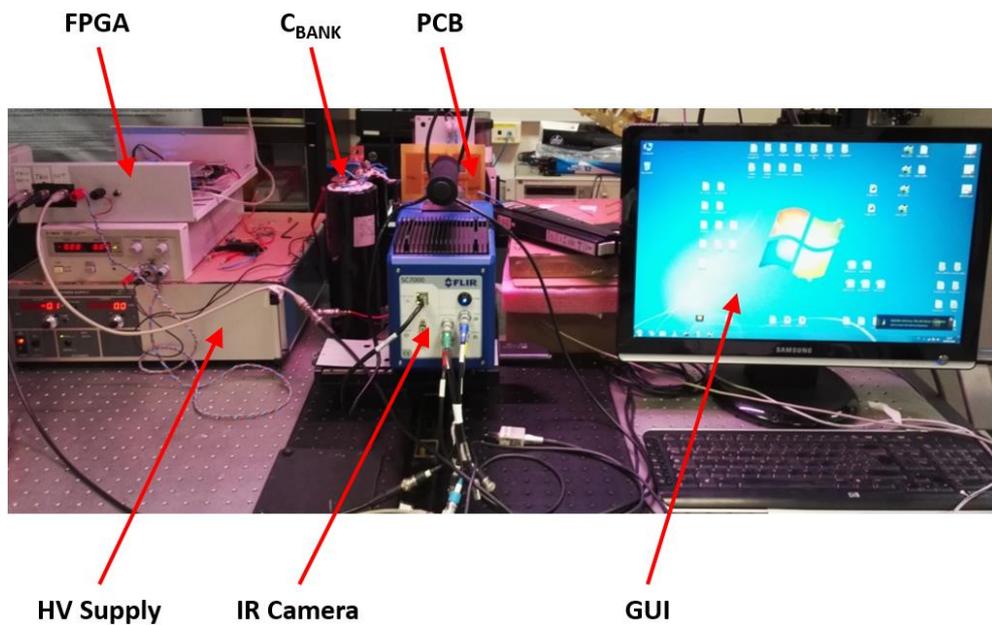
Figure 3.20: *Implemented IR Experimental test setup*

3.3.   Electro-thermal Simulations

Computer-aided design (CAD) is a well-established tool for the design of semiconductor power devices. Within these CAD tools exist a special tool known as technology computer-aided design (TCAD) which is used for semiconductor process and device design. Research organizations and industry widely use TCAD tools to simulate process and device technologies prior to the manufacturing of semiconductors. Such platforms also include various other specialised set of tools which could also be used to investigate the electrical, thermal and optical properties of semiconductor devices. Furthermore, these tools are also used to simulate structures under different operating conditions and hence their simulation results can be used to get a deeper insight into the failure mechanisms of devices under those test conditions. A complete and deep understanding of such failure mechanisms is necessary to feedback semiconductor industry for future design improvements in order to enhance their performance, robustness, and reliability [67].

Power semiconductor devices experience a sharp increase in T_J due to heat generation when subjected to conditions such as SC and UIS (avalanche breakdown). A sharp increase in T_J can be critical given that such devices usually already operate in high temperature environments. In other words, huge ΔT_J has a major effect on their performance and robustness [68]. For appropriate electro-thermal modelling of power semiconductor devices, the temperature dependence of physical parameters (i.e. implementation of accurate physics-based models) within the simulations must be duly incorporated [69, 70]. The T_J increase has a strong effect on the electrical characteristics of a device. Electro-thermal simulations are performed using compact physics-based models incorporated in TCAD simulators [71, 72]. These simulations form a crucial part of device characterisation which helps to investigate the underlying physical mechanisms responsible for device failure [60, 73, 74]. For the investigation of SiC power MOSFETs, here, Sentaurus TCAD software from Synopsys® was used [75].

3.3.1. Overview of Sentaurus TCAD software

This section aims to provide a brief overview of the TCAD software used for the analysis of SiC power MOSFETs. TCAD, a branch of electronic design automation, platforms are used to simulate semiconductor fabrication process technologies and device operation. TCAD tools can be further divided into two categories: process and device TCAD. Process TCAD deals with the semiconductor fabrication processes up until the physical device structure whereas device TCAD is used to simulate the performance of the fabricated structure. Such tools are crucial for simulating novel device structures prior to actual device fabrication as well as improve and optimize the existing device structures. These tools work by solving a set of essential and fundamental, physical and partial differential equations (PDEs) for the discretized device geometry in order to compute the device's behaviour [76]. Process simulations always begin with the mesh definition and grid initialization to define a new device structure. Subsequently, process simulations involve simulating device fabrication steps such as ion implantation, deposition, oxidation, etching, and diffusion [77]. A re-mesh strategy may also be required following the process steps if the geometry of the device changes since a finer mesh is required at the SiC/SiO$_2$ interface and pn junctions. A more detailed analysis of the different process simulations and steps could be found in various different literatures (e.g. [78]). Those steps have not been discussed here as they are beyond the scope of this study.
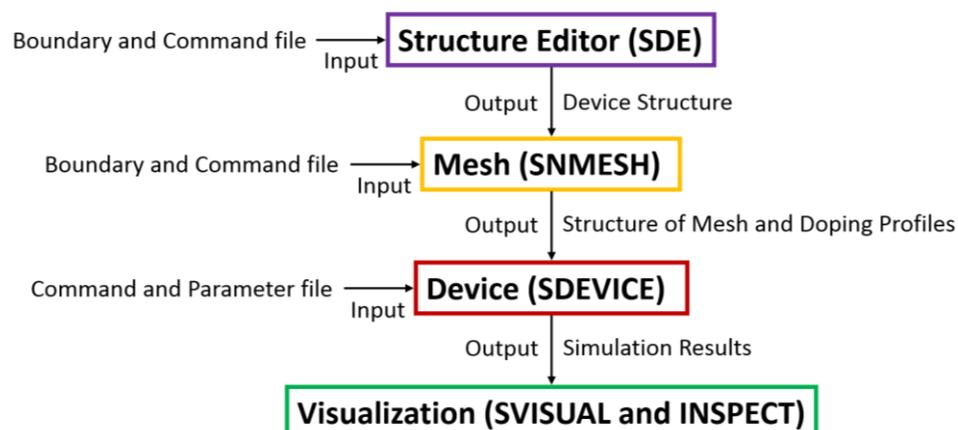
Figure 3.21: *Illustration of a simplified simulation flowchart within Sentaurus TCAD*

A simplified simulation flowchart for Sentaurus TCAD is presented in Figure 3.21. The dimensions of the cell are defined (using SDE) followed by the definition of doping profiles, materials and mesh (using SNMESH). A suitable mesh is important to optimise the simulation running time without compromising the accuracy of the results. The usual practice is to define a coarse mesh for the entire device. Afterwards, a refined mesh is applied in critical areas such as the channel, SiC/SiO$_2$ interface and *pn* junctions. It helps to take into account the high current densities and physical mechanisms occurring inside the device. An appropriate mesh is also important in order to define the accurate geometry of the device structure. The process of discretization divides the device geometry into various small elements which also leads to the formation of device mesh. A non-uniform mesh was defined throughout the device geometry for more accurate solution although the device simulator allows the possibility of both uniform and non-uniform mesh. Discretization helps to obtain solution over all nodes. The final structure is saved which is then used for further device simulations [76]. Following the mesh stage, the device structure is then used to perform electrical simulations (using SDEVICE). The input command file for SDEVICE has six different sections: *File, Electrode, Physics, Plot, Math and Solve*. The *File* section specifies the input and output files for simulation. The electrical boundary conditions setting all the initial voltages for each contact are included in the *Electrode* section. In *Physics* section, appropriate physics-based device models (accounting for mobility, recombination, and impact ionization etc.) are taken into account. The variables to be saved for visualising (on device structure) later on are specified using *Plot* section. PDEs are self consistently solved by SDEVICE. In the *Math* section, only a few settings relating to iterations and error calculations could be defined. Lastly, *Solve* section defines the instructions for the solver in order to obtain a sequence of solutions (i.e. initial guess and ramping up the contact voltages as required). An input parameter file also exists which includes all the values defined for model parameters [79]. An initial guess of the solution is used to compute charge. The calculated charge is then used to iteratively solve PDEs

(Poisson's and continuity equations) defining the electrostatic potential and carrier distribution locally for each element until the solution converges. Finally, any simulation results produced as a result of those simulations could be plotted for visualization and further analysis (either using SVISUAL or INSPECT).

3.3.2. Basic Device Equations

The simulator uses various fundamental physics equations in order to simulate semiconductor devices. The simulator makes use of these physical device equations in order to compute terminal voltages, currents, and charges that describe the carrier distribution and conduction mechanisms.

Electrostatic Potential and Quasi-Fermi Potentials

Mobile charges (electrons and holes) and immobile charges (traps and fixed charges) are crucial in all semiconductor devices. These charges possess electrostatic potential and, in turn, are themselves affected by the applied electrostatic potential. Hence, at least, electrostatic potential should be computed for all electrical device simulations. The Poisson equation, included as equation 3.9, is solved to obtain the electrostatic potential [75].

$$\nabla \cdot \left(\varepsilon \nabla \phi + \vec{P} \right) = -q(p - n + N_D - N_A) - \rho_{trap} \tag{3.9}$$

where ε is the electrical permittivity, $\vec{P}$ is the ferroelectric polarization, q is the elementary electric charge, n and p are electron and hole densities, N_D is the concentration of ionized donors, N_A is the concentration of ionized acceptors and ρ_{trap} is the charge density due to the traps and fixed charges [75]. The electron and hole quasi-Fermi potentials can be used to compute the electron and hole densities and vice versa. If the assumption is made for Boltzmann statistics, the electron and hole density equations (equations 3.10 and 3.11) are as follows:

$$n = N_C \exp\left(\frac{E_{F,n} - E_C}{kT}\right) \qquad (3.10)$$

$$p = N_V \exp\left(\frac{E_V - E_{F,p}}{kT}\right) \qquad (3.11)$$

where N_C and N_V are the effective density of states, $E_{F,n} = -q\phi_n$ and $E_{F,p} = -q\phi_p$ are the quasi-Fermi energies for electrons and holes, ϕ_n and ϕ_p are electron and hole quasi-Fermi potentials and lastly, E_C and E_V are conduction and valence band edges [75].

Carrier Transport in Semiconductors

The simulator supports different models for carrier transport within semiconductors. These could be described as continuity equations (3.12 and 3.13):

$$\nabla \cdot \vec{J}_n = qR_{net} + q\frac{\partial n}{\partial t} \qquad (3.12)$$

$$\nabla \cdot \vec{J}_p = -qR_{net} - q\frac{\partial p}{\partial t} \qquad (3.13)$$

where $\vec{J_n}$ and $\vec{J_p}$ are the electron and hole current density, q is the elementary electric charge, R_{net} is the net recombination rate, and lastly, n and p are electron and hole density.

The continuity equations presented in 3.12 and 3.13 could be used to express different transport models. Drift-Diffusion and thermodynamic transport models were used within simulations which are briefly discussed here [75].

- Drift-Diffusion Model (Isothermal Simulation)

It is the default model for carrier transport within Sentaurus Device. For this model, the electron and hole current densities are given by equations 3.14 and 3.15 respectively.

$$\vec{J}_n = q\mu_n n\vec{E} + qD_n\vec{\nabla}n \qquad (3.14)$$

$$\vec{J}_p = q\mu_p p\vec{E} - qD_p\vec{\nabla}p \qquad (3.15)$$

The contributions due to the spatial variations of electrostatic potential, electron affinity, and band gap are accounted for by the first term. The remaining terms correspond to the contributions due to the spatial variation of the effective masses m_n and m_p, and the gradient of concentration. $\gamma_n = \gamma_p = 1$ for Boltzmann statistics. The Einstein relation describes the diffusivities D_n and D_p (function of mobilities) as: $D_n = kT\mu_n$ and $D_p = kT\mu_p$. Furthermore, current equations, $\vec{J_n}$ and $\vec{J_p}$, can be simplified (labelled as 3.16 and 3.17) to give:

$$\vec{J}_n = -nq\mu_n\nabla\phi_n \tag{3.16}$$

$$\vec{J}_p = -pq\mu_p\nabla\phi_p \tag{3.17}$$

where ϕ_n and ϕ_p are the electron and hole quasi-Fermi potentials.

- Thermodynamic Model (Including Self-Heating)

Equations 3.16 and 3.17 can be rewritten (given as equations 3.18 and 3.19) in the thermodynamic model to include the temperature gradient as a driving term.

$$\vec{J}_n = -nq\mu_n\left(\nabla\phi_n + P_n\nabla T\right) \tag{3.18}$$

$$\vec{J}_p = -pq\mu_p\left(\nabla\phi_p + P_p\nabla T\right) \tag{3.19}$$

where P_n and P_p are the absolute thermoelectric powers and T is the lattice temperature.

3.3.3. Simulated Device Structure

In order to allow better understanding and interpretation of the experimental results, it was paramount to perform advanced TCAD simulations. Advanced TCAD aided numerical electro-thermal simulations helped to identify the physical mechanisms taking place inside the device during SC and avalanche breakdown, which led to device failure as presented in later sections. For TCAD analysis, a full 2D cell structure of a planar MOSFET was constructed, along with device symmetry, within TCAD software and the experimental results were reproduced. The simulated cell structure along with important annotations is included in Figure 3.22. Table 3.1

includes important doping concentration and physical dimension values associated with the implemented cell structure.

Table 3.1: *Implemented values for important parameters*

Parameter	Value	Parameter	Value
N_{DRAIN}	5.0×10^{18} cm^{-3}	Cell Width	17.4 µm
N_{DRIFT}	1.0×10^{16} cm^{-3}	t_{OXIDE}	50 nm
$N_{CHANNEL}$	2.0×10^{17} cm^{-3}	$L_{CHANNEL}$	~ 350 nm
$N_{SHIELDING}$	1.0×10^{19} cm^{-3}	L_{DRIFT}	17 µm
N_{SOURCE}	6.0×10^{19} cm^{-3}	L_{DRAIN}	1 µm
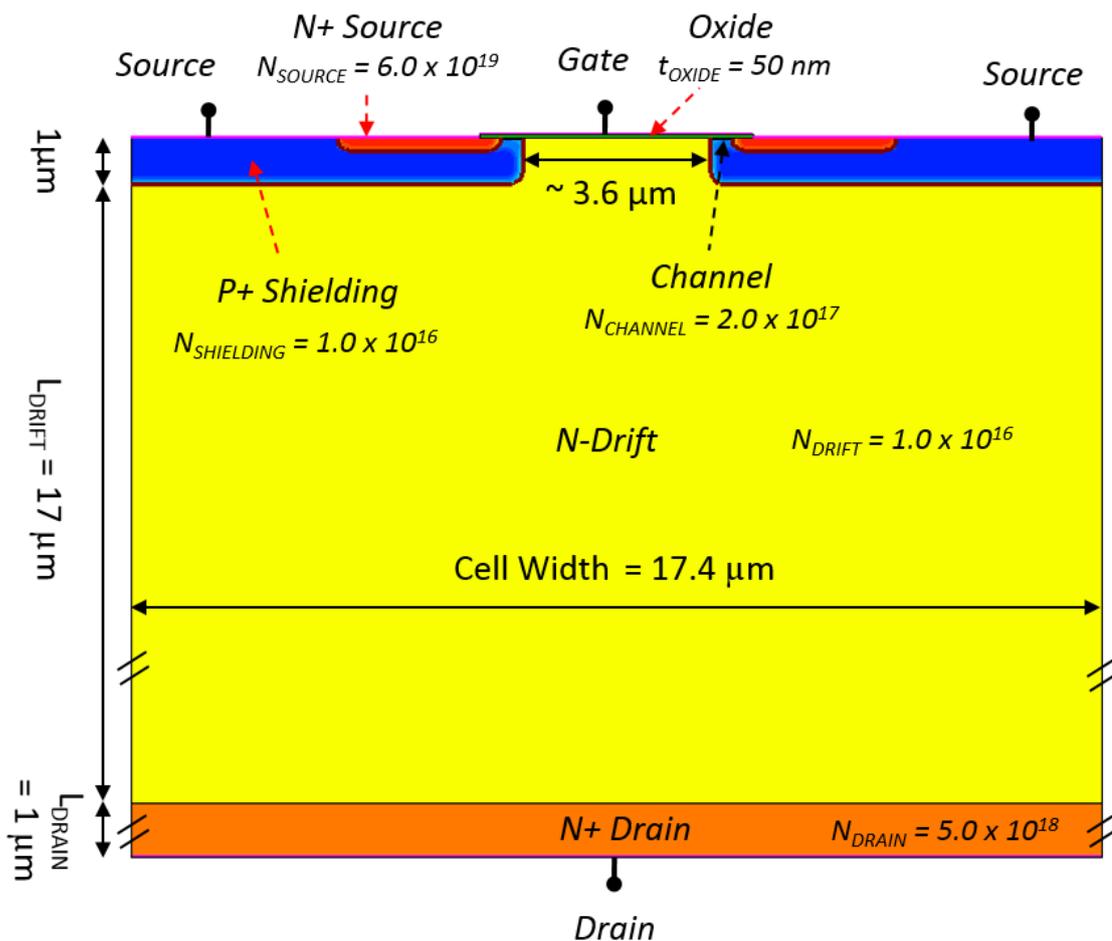
Figure 3.22: *Simulated cell structure (Not to scale)*

The doping concentrations and physical dimensions presented in Table 3.1 were defined with the help of literature data and previously published articles [15, 17, 80]. Principal models accounting for mobility dependence as well as degeneration and their corresponding parameters are briefly discussed and included in later section 3.2.4. The temperature dependence of semiconductor devices is well known, therefore, the temperature dependence of parameters was also accordingly included. Hence, the heat generation and transport equations were solved along with the semiconductor equations. For the purpose of simulations, source and body contacts were physically separated but both connected to the same bias voltage.
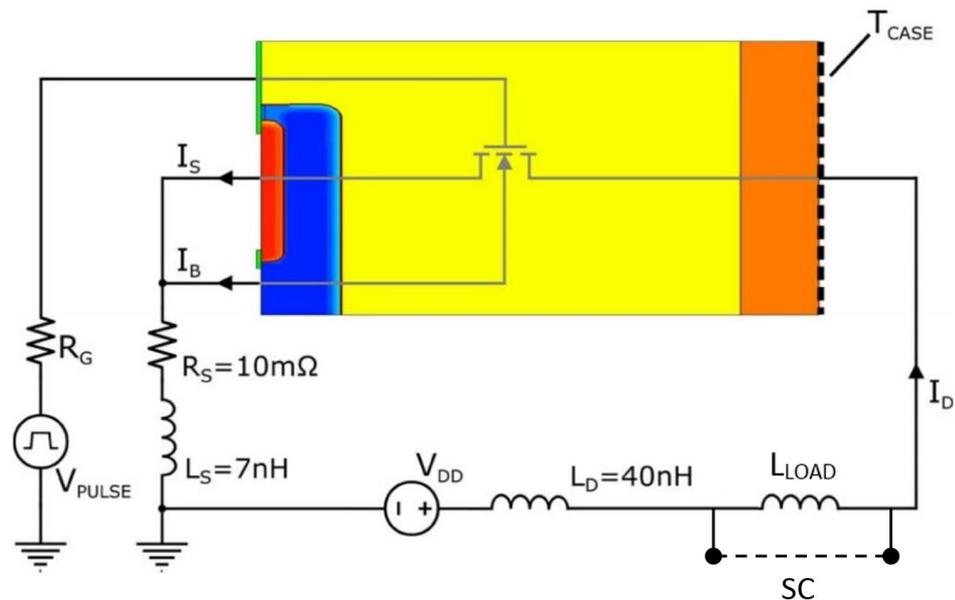
Figure 3.23: *Mixed-mode circuit schematic for SC and UIS*

The implemented device structure was used to create a circuit description in order to perform mixed-mode simulations as shown in Figure 3.23. In order to account for the inevitable presence of parasitic elements (also discussed earlier in section 3.1.1) arising from wires and connections, additional components were included. In specific, parasitic inductance and resistance at source (L_S and R_S) affecting the dI_D/dt at device turn-on as well as the parasitic inductance (L_D) on drain which gives rise to voltage spikes at turn-on/turn-off. The cell

structure was calibrated in order to appropriately match the isothermal transfer characteristics (I_D versus V_{GS}) and output characteristics (I_D versus V_{DS}) of Dev-A. However, by any means, it is not an actual representation of actual device structure. Therefore, these simulations act as generic analysis in order to have a qualitative analysis of physical mechanisms responsible for device failure. The measured transfer characteristics were obtained using a curve tracer at V_{DS} = 20 V for T_{CASE} of 300 K and 410 K. Figure 3.24 includes the measured (squares) and simulated (solid) transfer characteristics. The experimental and simulation results both verify the unstable behaviour for a typical SiC MOSFET as also illustrated in Figure 2.8. The measured output characteristics also obtained using a curve tracer for V_{GS} sweep starting from 10 V up until 20 V in steps of 2 V at V_{DS} = 20 V and T_{CASE} = 300 K. Figure 3.25 includes the measured (squares) and simulated (solid) output characteristics.
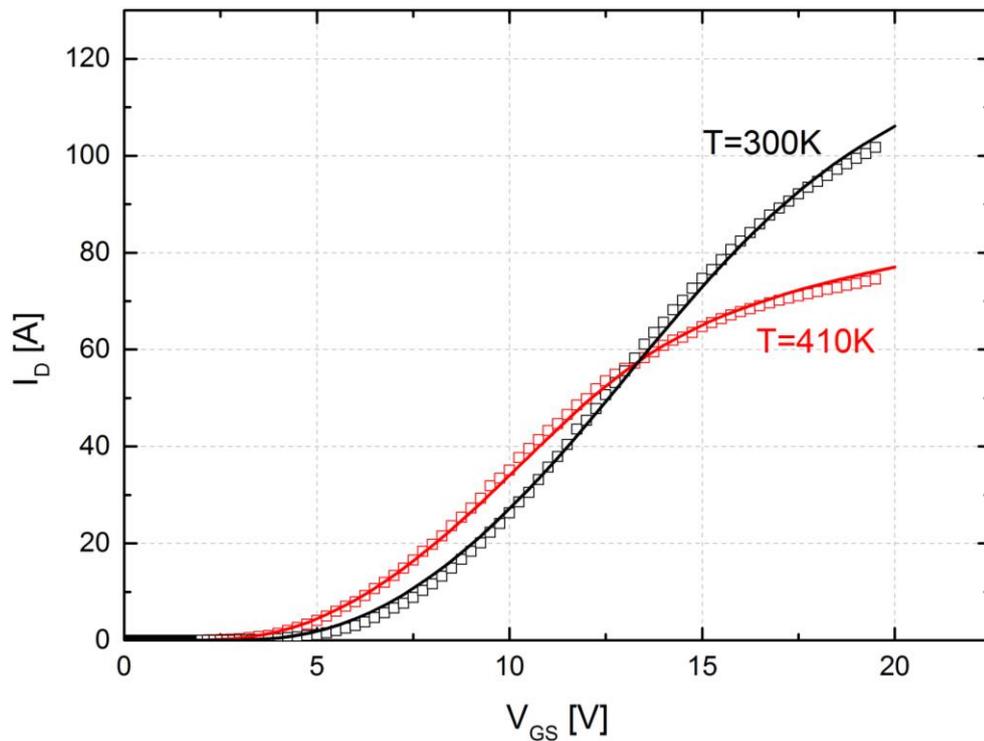
Figure 3.24: *Isothermal simulated (solid) and measured (squares) transfer (I_D vs. V_{GS})*

characteristics
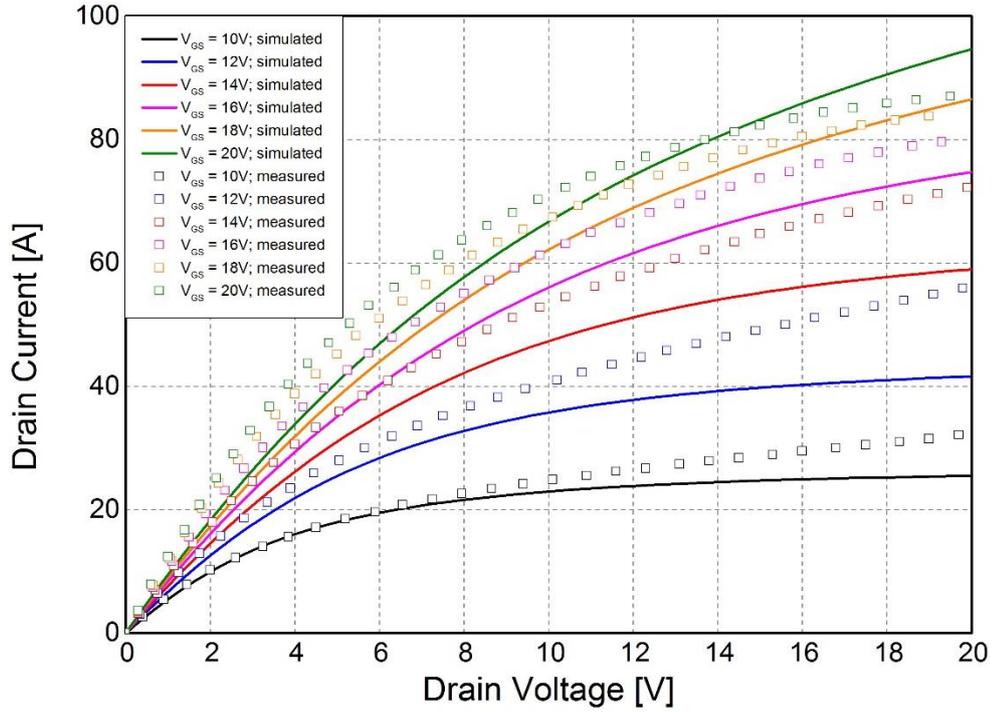
Figure 3.25: *Isothermal simulated (solid) and measured (squares) output (I$_D$ vs. V$_{DS}$)*

characteristics

The defects (traps) at the semiconductor/oxide (SiC/SiO$_2$) interface also play an important role in device's behaviour as they lead to trapping of electrons which then has a concurrent effect on electron mobility due to Coulomb scattering phenomena. It is therefore really important to consider the inclusion of density of fixed charge (Q$_F$) and interface states (D$_{it}$) at the interface. Several studies have reported about the behaviour of interface levels/states on MOSFET devices [35, 81, 82]. These trap levels, when occupied by electrons, act as acceptor-like (negatively charged) above mid-gap energy (E$_i$). One effect due to this is threshold voltage (V$_{th}$) instability (in this case, positive shift). The analytical expression for V$_{th}$ is included in equation 3.20 [83].

$$V_{th} = V_{fb} + \phi_s + V_{ox} = V_{fb} + 2\phi_F + \frac{1}{C_{ox}}\left(\sqrt{2\varepsilon_s q N_A(2\phi_B)} + q\int_{E_i}^{E_i+q\phi_B} D_{it}(E)dE\right) \qquad (3.20)$$

Semiconductor devices have the ability to support high voltages in the OFF-state, without having a significant drain leakage current (I$_{DSS}$). The avalanche breakdown mechanism is

dependent on the distribution of electric field (*E*) inside the structure [15]. During device design, N_{DRIFT} is carefully chosen to obtain the desired breakdown voltage (V_{BD}) of approximately 1900 V. At the same time, the depth of the N-Drift layer should be appropriately selected as it should contain the full depletion layer width (W_m) corresponding to V_{BD} of the device being designed. It is crucial to avoid the depletion region reaching the N+ substrate region as it causes punch through. The analytical device design equations defining the V_{BD} and W_M for non-fully N- depleted region structures are included here as equation 3.21 and 3.22 respectively [17].

$$V_{BD} = \frac{\varepsilon_s E_C{}^2}{2qN_{DRIFT}}$$ (3.21)

$$W_m = \sqrt{\frac{2\varepsilon_s V_{BD}}{qN_{DRIFT}}}$$ (3.22)

where E_C is the critical electric field which is defined (equation 3.23 for 4H-SiC) as:

$$E_C = 3.3 \times 10^4 N_D{}^{1/8}$$ (3.23)

For 4H-SiC, equation 3.21 and 3.22 could be written as a function of N_{DRIFT} only as presented in equation 3.24 and 3.25 below [17]:

$$V_{BD} = 3.0 \times 10^{15} N_{DRIFT}{}^{-3/4}$$ (3.23)

$$W_m = 1.82 \times 10^{11} N_{DRIFT}{}^{-7/8}$$ (3.24)

In the presence of the high electric field, the collision of mobile carriers possessing sufficient energy with the lattice atoms results in the creation of electron-hole pairs. This is known as impact ionization. Subsequently, electron-hole pairs generated due to impact ionization result in the generation of further electrons and holes pairs. In other words, impact ionization is an augmented process producing a continuous flow of electrons through the depletion region which results in a significant flow of current between drain and source during avalanche

breakdown. Therefore, appropriate impact ionization model needs to be selected within simulations. The maximum operating voltage for a power device is therefore limited by avalanche breakdown mechanism [17].

3.3.4. Physical Models

Appropriate use of physical device models is essential in order to account for mechanisms such as degradation of carrier mobility, carrier recombination, the definition of the band gap and impact ionization (avalanche breakdown). The parameters of the physical models used were changed until an appropriate calibration of the device characteristics was achieved. The selection of mobility models and avalanche generation implemented here were selected with the help of various different literature materials [75, 84-86].

Carrier Mobility (μ) Models

A modular approach is used within Sentaurus to define the carrier mobilities. At the least, the carrier mobility is a function of lattice temperature (T). The carrier mobility can degrade further due to doping concentration, interface traps, and high electric fields. Usually, more than one mobility model is activated and all the mobility contributions (such as bulk and channel etc.) are combined using Matthiessen's rule as expressed in equation 3.26:

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \dots\dots\dots$$

(3.26)

- Phonon Scattering – Constant Mobility Model

This mobility model is defined by default. The constant mobility model [87], calibrated up to 460 K, accounts for the phenomena of phonon scattering and is only dependant on T. Here, it is defined in equation 3.27 as:

$$\mu_{const} = \mu_L \left(\frac{T}{300K} \right)^{-\zeta}$$

(3.27)

- Doping Dependence – Arora Mobility Model

The mobility degradation occurs due to scattering caused by impurity atoms which should also be taken into account. The Arora mobility model [88], calibrated up to 500 K, was used to account for the mobility degradation due to doping in the channel. The model (equations 3.28 - 3.32) is defined as:

$$\mu_{arora} = \mu_{min} + \frac{\mu_d}{1 + \left(\dfrac{(N_{A,0} + N_{D,0})}{N_0}\right)^{A^*}}$$

(3.28)

where

$$\mu_{min} = A_{min}\left(\frac{T}{300K}\right)^{\alpha_m}$$

(3.29)

$$\mu_d = A_d\left(\frac{T}{300K}\right)^{\alpha_d}$$

(3.30)

$$N_0 = A_N\left(\frac{T}{300K}\right)^{\alpha_N}$$

(3.31)

$$A^* = A_a\left(\frac{T}{300K}\right)^{\alpha_a}$$

(3.32)

- Interface Degradation – Lombardi Mobility Model

The presence of a high transverse electric field in the channel region of a MOSFET leads to a strong interaction of the carrier to the SiC/SiO$_2$ interface. The carriers experience scattering due to acoustic surface phonons and surface roughness. The degradation of mobility due to these phenomena needs to be taken into account. Here, to take into account these mechanisms, Lombardi model [87] was used. This model has been calibrated up to lattice temperature of 460 K. The terms accounting for acoustic phonon scattering and surface roughness are given in equation 3.33 and 3.34 respectively:

$$\mu_{ac} = \frac{B}{F_{\perp}} + \frac{C((N_{A,0} + N_{D,0} + N_2)/N_0)^{\lambda}}{F_{\perp}^{1/3}(T/300K)^k} \tag{3.33}$$

$$\mu_{sr} = \left(\frac{(F_{\perp}/F_{ref})^{A^*}}{\delta} + \frac{F_{\perp}^{3}}{\eta} \right)^{-1} \tag{3.34}$$

The contributions due to μ_{ac} and μ_{sr} are then combined with the bulk mobility using Matthiessen's rule (equation 3.35 – 3.37):

$$\frac{1}{\mu_{lombardi}} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} \tag{3.35}$$

where

$$A^* = A + \frac{(\alpha_{\perp,n}n + \alpha_{\perp,p}p)N_{ref}^{\nu}}{(N_{A,0} + N_{D,0} + N_1)^{\nu}} \tag{3.36}$$

$$D = \exp(-x/l_{crit}) \tag{3.37}$$

- Density of Interface traps – NegInterfaceCharge Mobility Model

The implementation of a mobility model which accounts for the mobility degradation due to such high density of interface traps (D_{it}) in SiC is really important. SiC/SiO$_2$ interface technology is highly plagued by high D_{it} which tends to not only affect the mobility in the channel but also lead to V_{th} instability. NegInterfaceCharge model [75] accounts for mobility contributions due to phenomena of Coulomb scattering. It is defined as (equation 3.38 – 3.40):

$$\mu_{coulomb} = \frac{\mu_1 \left(\dfrac{T}{300K} \right)^k \left\{ 1 + \left[c \Big/ \left(c_{trans} \left(\dfrac{N_{A,D} + N_1}{10^{18}cm^{-3}} \right)^{\gamma_1} \left(\dfrac{N_C}{N_0} \right)^{\eta_1} \right) \right]^{\nu} \right\}}{\left(\dfrac{N_{A,D} + N_2}{10^{18}cm^{-3}} \right)^{\gamma_2} \left(\dfrac{N_C}{N_0} \right)^{\eta_2} D \cdot f(F_{\perp})} \tag{3.38}$$

Where

$$f(F_\perp) = 1 - \exp\left[-(F_\perp/E_0)^\gamma\right]$$ (3.39)

$$D = \exp(-x/l_{crit})$$ (3.40)

- Carrier Saturation velocity – High-Field Saturation Model

At high electric fields, the carrier drift velocity saturates to a certain speed defined as saturation velocity (v_{sat}) and hence it is no more proportional to the electric field. To take into account this effect, Canali mobility model [89] was used. Canali model has been calibrated up to 430 K. It is defined as (equation 3.41 – 3.43):

$$\mu(F) = \frac{(\alpha+1)\mu_{low}}{\alpha + \left[1 + \left(\frac{(\alpha+1)\mu_{low}F_{hfs}}{v_{sat}}\right)^\beta\right]^{1/\beta}}$$ (3.41)

where

$$\beta = \beta_0\left(\frac{T}{300K}\right)^{\beta_{\exp}}$$ (3.42)

$$v_{sat} = v_{sat,0}\left(\frac{300K}{T}\right)^{v_{sat,\exp}}$$ (3.43)

Avalanche Generation Model

The generation of electron-hole pairs occurs as a result of Impact ionization (avalanche generation). The process of avalanche generation requires a certain threshold for electric field strength. This electric field strength eventually results in the acceleration of the carriers through the space charge regions. Avalanche generation is important to assess the avalanche breakdown performance of SiC power devices. The generation rate is expressed using equation 3.44 as:

$$G_{ii} = \alpha_n n v_n + \alpha_p p v_p \tag{3.44}$$

where α_n and α_p are the ionization coefficients for electrons and holes respectively.

Various different models exist for the behaviour of the ionization coefficients. Okuto-Crowell model [90] was implemented as expressed in equation 3.45 below:

$$\alpha(F_{ava}) = a \cdot (1 + c(T - T_0)) F_{ava}^{\gamma} \exp\left[-\left(\frac{b[1 + d(T - T_0)]}{F_{ava}}\right)^{\delta}\right] \tag{3.45}$$

where T is the lattice temperature and T_0 = 300 K.

Lastly, all the parameter values for the models used have been included separately in Appendix A at the end of the thesis.

4. Short Circuit Robustness

4.1. Experimental Testing and Results

4.1.1. Experimental Results – Functional Characterisation

This section represents all the experimental results obtained on packaged SiC power MOSFETs during SC. Tests were carried out parametrically over: T_{CASE}, V_{DD}, V_{GS} and $P_{SC(pk)}$. The test results presented in chapter 4 are on three different DUTs from different manufacturers. Some of the important features of these devices are summarised here in Table 4.1.

Table 4.1: Summary of relevant device parameters

DUT	$V_{DS(max)}$ (V)	$R_{DS(on)}$ @ 25 °C (mΩ)	I_D @ 25 °C (A)	C_{ISS} (pF)	Package
Dev-A [91]			36	950	TO-247
Dev-B [92]	1200	80	40	2080	
Dev-C [93]			45	1700	HiP247^{TM}

Case Temperature (T_{CASE}) Sweep

First set of tests presented here demonstrate the effect of different T_{CASE} (−25 °C, 25 °C and 75 °C) on the SC performance while keeping all the other parameters (V_{DD} = 600 V and V_{GS} = 18 V) unchanged. Figure 4.1 and 4.2 present I_D and V_{DS} waveforms during SC for T_{CASE} = −25 °C. Figure 4.3 present SC I_D waveforms at failure for three different T_{CASE} on three separate Dev-A devices and all the relevant test conditions are also summarised in Table 4.2. The SC pulse was gradually increased to move out of the short circuit safe operating area (SCSOA) until failure was observed in order to determine the absolute SC limits of the DUT for the applied test conditions. SC energies for failure t_{SC} were also calculated using equation 3.4 and included in the table. Trapezoidal numerical integration (*trapz*) function within MATLAB was used to calculate energy and the code is included in Appendix B.
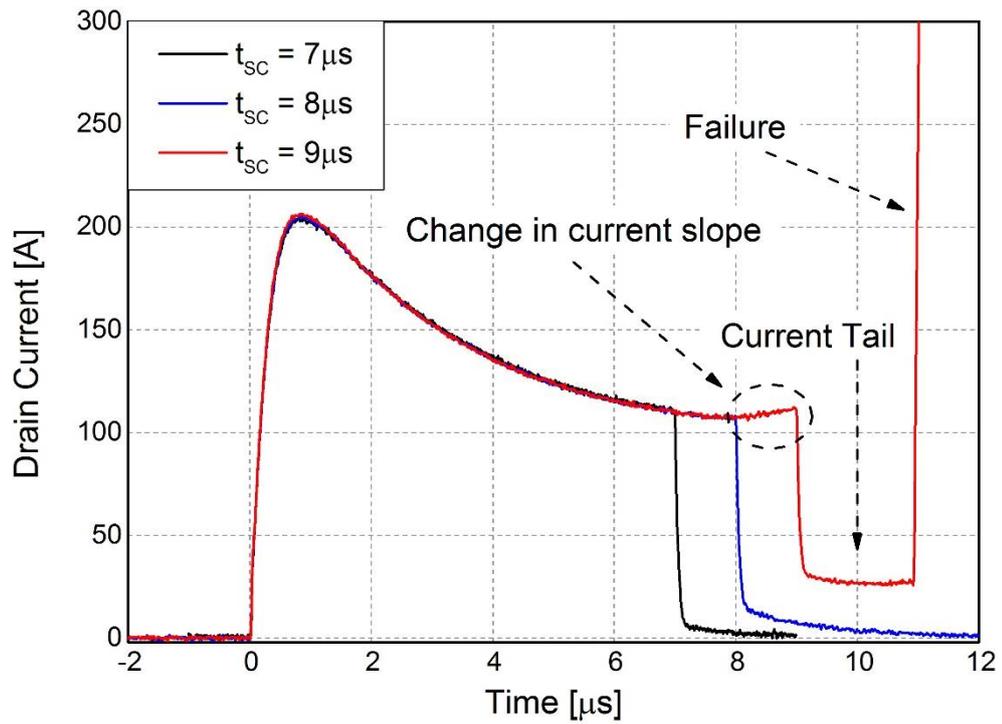
Figure 4.1: *Experimental SC drain current (I_D) waveforms; <u>Dev-A</u>; V_{DD} = 600 V; V_{GS} = 18 V; T_{CASE}*

= −25 °C; t_{sc} = 7 μs, 8 μs and <u>9 μs (Failure)</u>
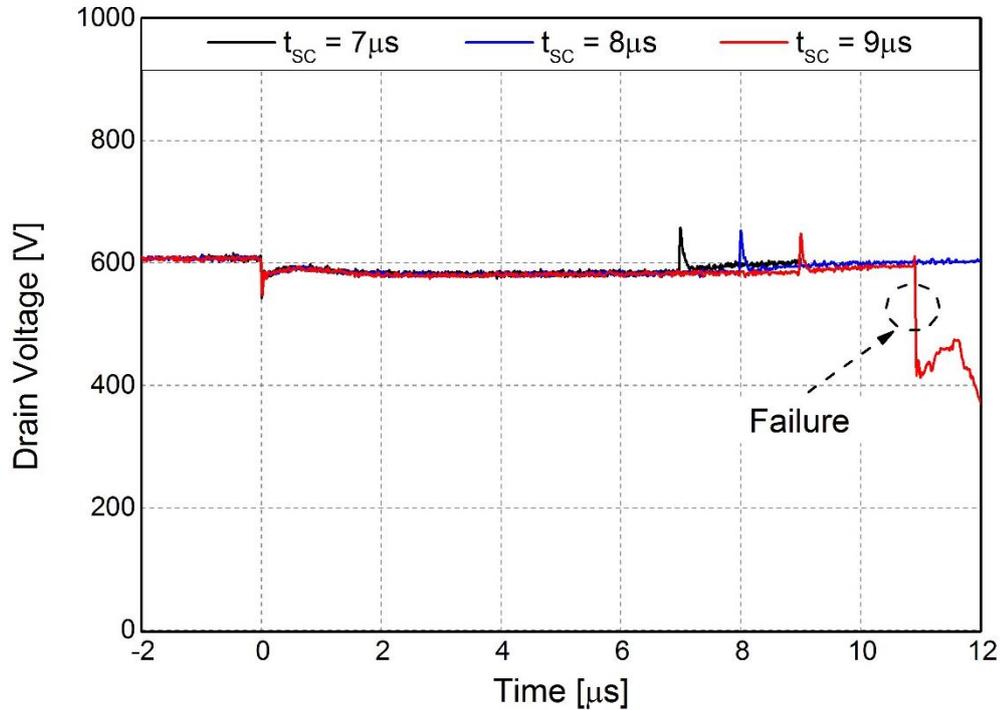
Figure 4.2: *Experimental SC drain voltage (V_{DS}) waveforms; <u>Dev-A</u>; V_{DD} = 600 V; V_{GS} = 18 V;*

T_{CASE} = −25 °C; t_{sc} = 7 μs, 8 μs and <u>9 μs (Failure)</u>
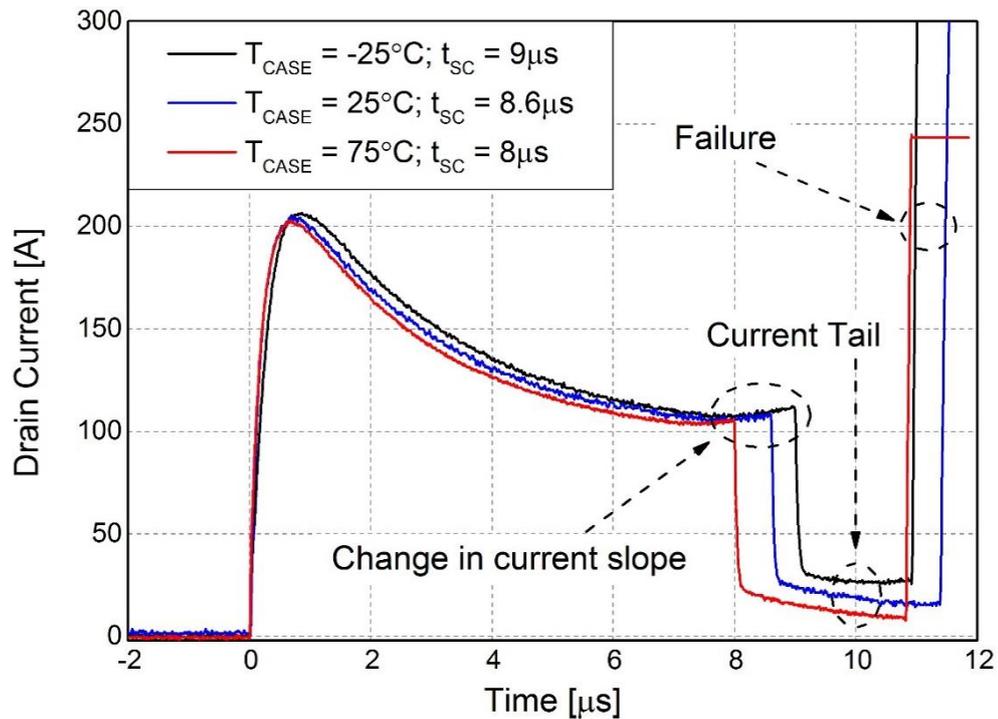
Figure 4.3: *Experimental SC drain current (I_D) waveforms; <u>Dev-A</u>; V_{DD} = 600 V; V_{GS} = 18 V; T_{CASE}*

= −25 °C, 25 °C and 75 °C; <u>Comparison</u>

As the critical t_{SC} is progressively approached, few important observations can be made, which are also quite apparent from Figure 4.1. A significant appearance of the current tail after device turn-off started to occur followed by the predominant change in sign of the current derivative prior to device turn-off. Eventually, at critical t_{SC}, I_D increased rapidly and uncontrollably which led to the destruction of the device as also pointed out in Figure 4.1. The DUTs in SC failed catastrophically at t_{SC} of 9 μs, 8.6 μs and 8 μs for T_{CASE} of −25 °C, 25 °C and 75 °C respectively as shown in Figure 4.3. E_{SC} at failure for each critical t_{SC} were also plotted versus T_{CASE} and included in Figure 4.4. As the T_{CASE} was increased, the SC withstand capability of the DUT deteriorated suggesting that the failure is T_{CASE} dependent and in some way associated to reaching critical junction temperature (T_J) which results in irreversible damage to the device.

Table 4.2: *Summary of test conditions (<u>Dev-A</u>; Different T_{CASE})*

T$_{CASE}$ (°C)	V$_{DD}$ (V)	V$_{GS}$ (V)	t$_{SC}$ (μs) at Failure	E$_{SC}$ (J) at Failure
-25			9	0.76
25	600	18	8.6	0.73
75			8	0.67
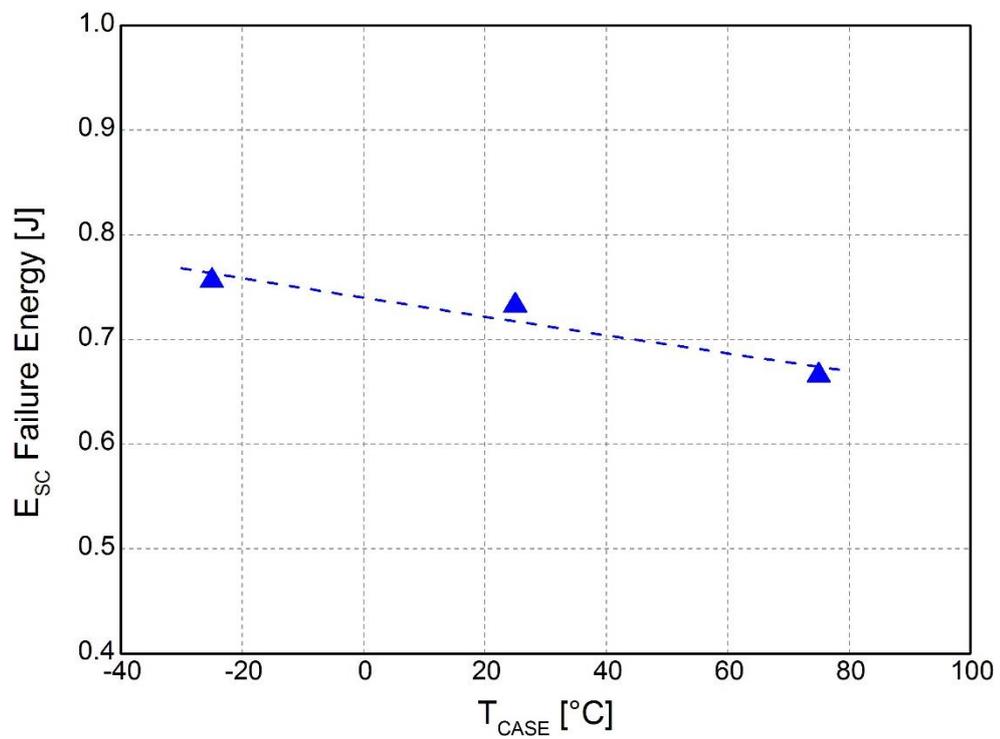
Figure 4.4: *Relationship between E$_{SC}$ at failure versus T$_{CASE}$; <u>Dev-A</u>*

Input Voltage (V$_{DD}$) Sweep

The second set of tests presented here are at three different V$_{DD}$ (400 V, 600 V, and 800 V) while keeping all the other test parameters (T$_{CASE}$ = 150 °C and V$_{GS}$ = 16 V) unaltered. Figure 4.5 present I$_D$ waveforms during SC for V$_{DD}$ = 600 V. Some of the selective results for three different V$_{DD}$ on three separate Dev-A DUTs are presented in Figure 4.6 and summary of all the relevant test conditions is given in Table 4.3. These tests were carried out with an aim to demonstrate the SC robustness at different P$_{SC(pk)}$ as well as also point out the approximate V$_{DD}$ at which the DUT could sustain t$_{SC}$ ≥ 10 μs. The P$_{SC(pk)}$ calculations were also carried out using equation 3.3 and included in the table. Here at V$_{DD}$ = 400 V, Dev-A can withstand SC of t$_{SC}$ ≥ 10 μs and therefore t$_{SC}$ was increased well above 10 μs up to 15 μs with a small current tail. On the other hand, the substantial current tail could be seen as early as t$_{SC}$ of 9.4 μs and 6.6 μs for V$_{DD}$ of 600 V and 800 V respectively. Since T$_J$ rise is directly proportional to the power dissipation inside the device, t$_{SC}$ at which current tail starts to appear is brought forward with increasing P$_{SC(pk)}$.
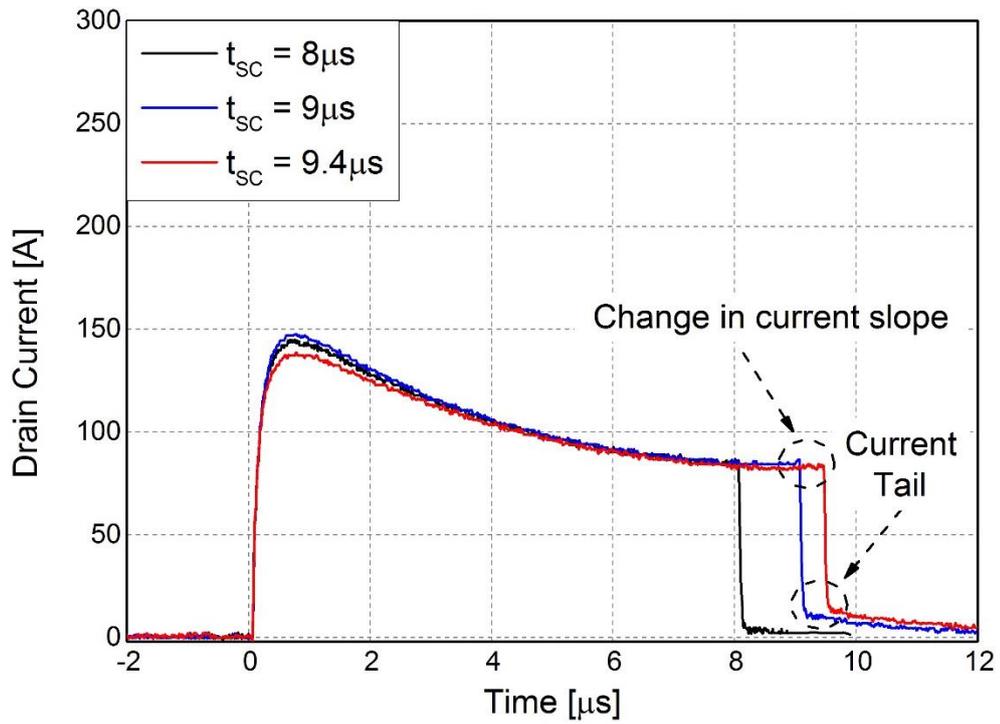
Figure 4.5: *Experimental SC drain current (I_D) waveforms; <u>Dev-A</u>; <u>V_{DD} = 600 V</u>; V_{GS} = 16 V; T_{CASE}*

= 150 °C; t_{sc} = 8 µs, 9 µs and 9.4 µs
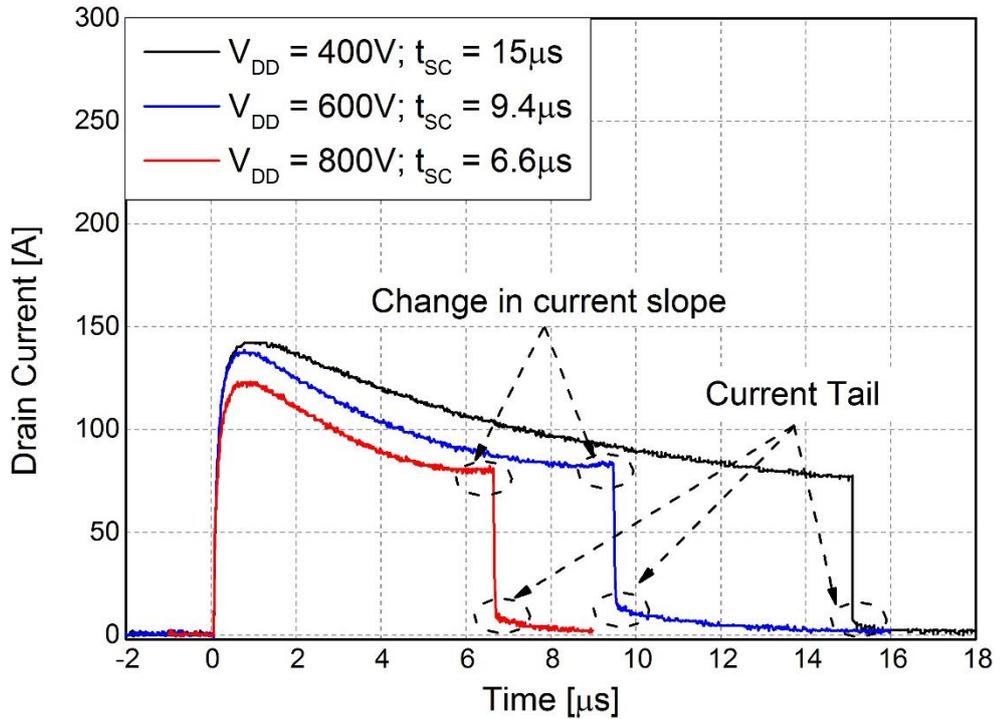
Figure 4.6: *Experimental SC drain current (I_D) waveforms; <u>Dev-A</u>; V_{GS} = 16 V; T_{CASE} = 150 °C;*

V_{DD} = 400 V, 600 V and 800 V; <u>Comparison</u>

Table 4.3: *Summary of test conditions (<u>Dev-A</u>; Different V_{DD} – High Power)*

V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	t_{SC} (µs)	$P_{SC(pk)}$ (kW)
400			15	57.60
600	150	16	9.4	88.20
800			6.6	100.80

During the course of SC characterisation, two distinctive SC results were observed which also helped to lead to the conclusion that there could be two different modes of failure during SC as discussed in further detail later on in section 4.2. Figure 4.7 and 4.8 present SC results at V_{DD} of 400 V (T_{CASE} = 90 °C) and 800 V (T_{CASE} = 150 °C) on previous generation Dev-A* DUTs for a fixed V_{GS} of 18 V and the test conditions are summarised in Table 4.4. For V_{DD} = 800 V, Figure 4.7, t_{ON} of 10 µs was sent to the DUT and it failed catastrophically without even turning off. Above certain high voltage value (mainly above V_{DD} = 400 V), as failure was approached, it was not possible to turn-off the device safely even if t_{ON} was increased carefully in steps of (ns) and hence all tests resulted in catastrophic DUT failure. Another important observation to be noted here is that the DUT actually failed slightly before completing 10 µs. On the other hand, for V_{DD} = 400 V, Figure 4.8, t_{SC} was increased progressively. Instead, a different failure observation was made where the I_D of DUT significantly decreased for t_{SC} = 32.2 µs (dashed line) without catastrophic failure indicating that the DUT had become partially nonoperative. The decrease in the I_D current was observed immediately as the t_{SC} was increased from 32.1 µs to 32.2 µs. For tests at V_{DD} = 400 V, for t_{SC} of 32.2 µs, the gate voltage also decreased from 18 V to 13 V when the I_D decreased due to increased gate leakage current (I_{GSS}) [94]. Alongside, a decrease in gate-source impedance was also measured. Therefore, the DUT was classed as being degraded and not fit for purpose anymore.
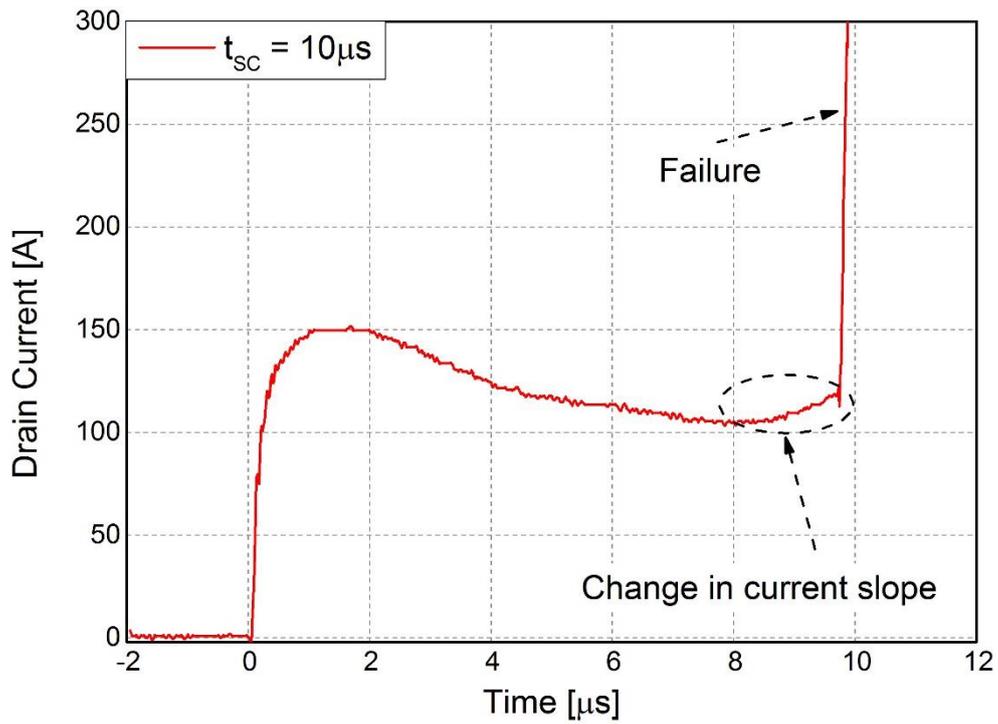
Figure 4.7: *Experimental SC drain current (I_D) waveform; <u>Dev-A*</u>; V_{DS} = 800 V; V_{GS} = 18 V; T_{CASE}*

= 150 °C; t_{SC} = <u>10 μs (Failure)</u>
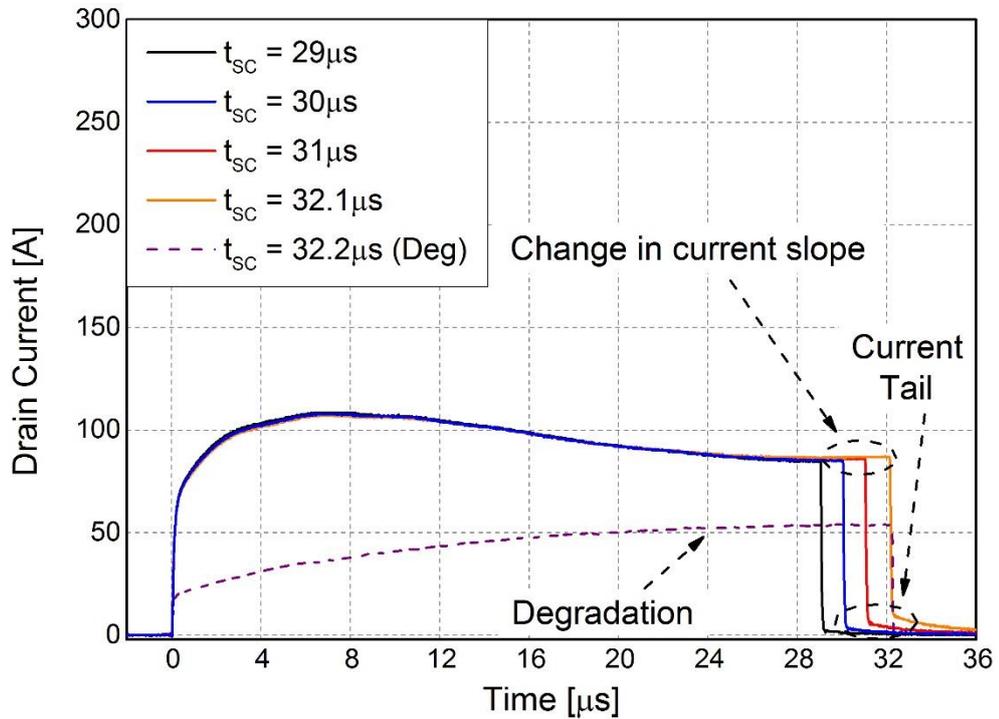
Figure 4.8: *Experimental SC drain current (I_D) waveform; <u>Dev-A*</u>; V_{DS} = 400 V; V_{GS} = 18 V; T_{CASE}*

= 90 °C; t_{SC} = 29 μs, 30 μs, 31 μs, 32.1 μs and <u>32.2 μs (Degradation)</u>

V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	t_{SC} (µs)
400	90	18	29, 30, 31, 32.1 and 32.2
800	150		10

* Previous generation SiC MOSFET of Dev-A

In order to verify that two different failure mechanisms exist during SC, the third set of tests were performed at low V_{DD} (and $P_{SC(pk)}$) with long t_{ON} pulse duration where t_{ON} of the gate signal was kept constant to 100 µs. Here, V_{DD} was increased starting from 100 V until failure was observed. This set of tests were designed in order to study the DUT behaviour for slower temperature dynamics and hence longer thermal stress as opposed to the tests presented earlier for a range of higher V_{DD} resulting in faster temperature dynamics and shorter thermal stress (shorter t_{ON} until failure). Figure 4.9 – 4.11 show selective results on Dev-A for three different V_{DD} at low power and summary of all the relevant test conditions are also included in Table 4.5.

Figure 4.9 shows the I_D waveforms for the three V_{DD}. The DUT survived the whole t_{ON} duration for V_{DD} = 100 V and 150 V. When the V_{DD} was increased to 175 V, the DUT was not able to sustain the whole t_{ON} duration and it failed at approximately 85 µs as also seen in Figure 4.9 when I_D drops to zero. Moreover, important observations are highlighted and presented in Figure 4.10 and 4.11. V_{GS} dropped down to zero and I_{GSS} suddenly increased corresponding to the time instant when I_D dropped to zero. It clearly indicates that the gate-source impedance decreased significantly to a point where there is a short between gate and source resulting in device turn-off at 85 µs. Furthermore, this was also confirmed by physical measurement of resistance between gate and source (R_{GS}) which was found to be less than 1 Ω. In this case, the DUT did not fail catastrophically and hence could be classed as degraded due to loss of its

intended operation resulting from damage to the gate/source structure. Failure of some constituent features such as the metallization layer and/or passivation layer could possibly have resulted in device degradation.

Table 4.5: *Summary of test conditions (Dev-A; Different V_{DD} – Low Power; fixed t_{ON})*

V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	t_{ON} (μs)	$P_{SC(pk)}$ (kW)
100				16.70
150	25	18	100	26.85
175				32.73
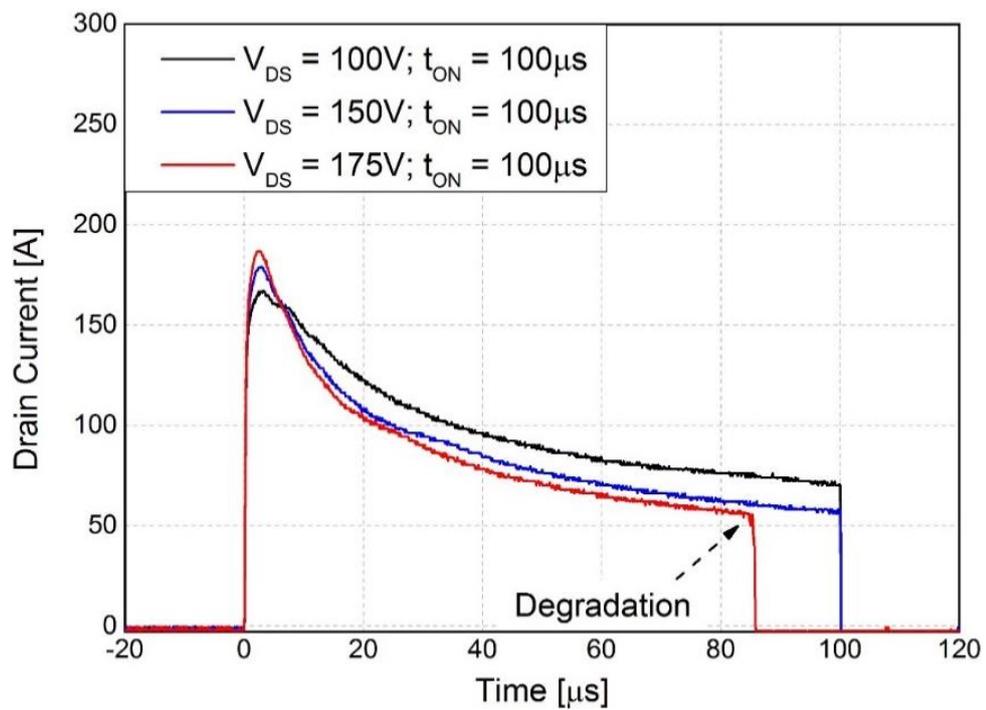
Figure 4.9: *Experimental SC drain current (I_D) waveforms; t_{ON} = 100 μs; V_{GS} = 18 V; T_{CASE} = 25 °C; Dev-A; V_{DD} = 100 V, 150 V and 175 V (Degradation)*
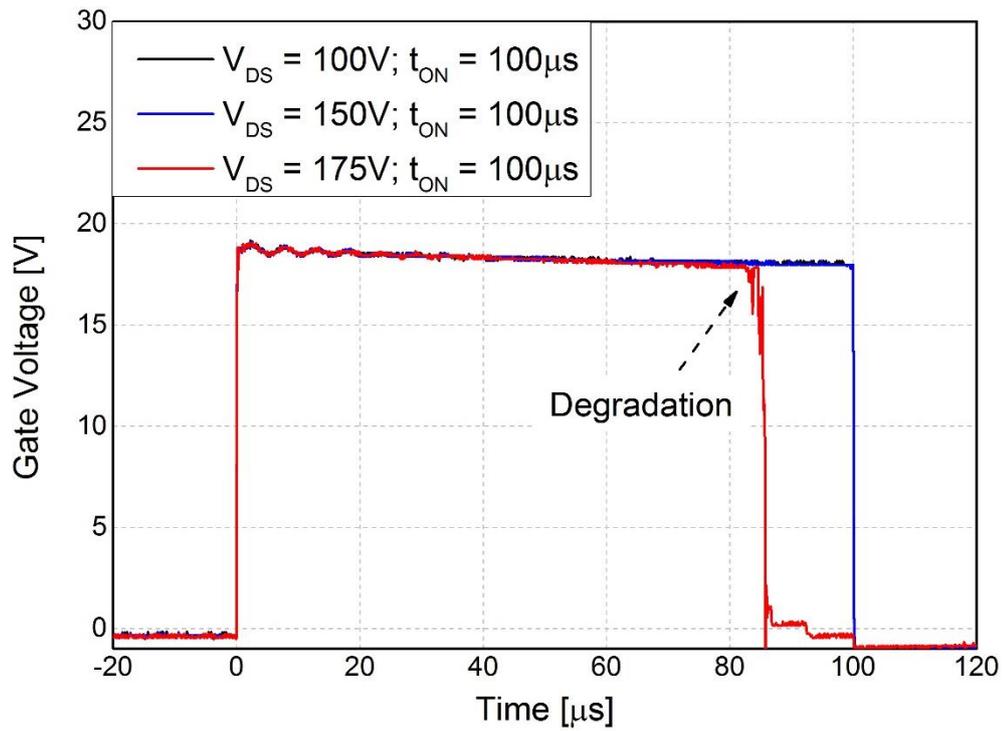
Figure 4.10: *Experimental Gate voltage (V_{GS}) waveforms; <u>Dev-A</u>; t_{ON} = 100 µs; V_{GS} = 18 V; T_{CASE}*

= 25 °C; V_{DD} = 100 V, 150 V and <u>175 V (Degradation)</u>
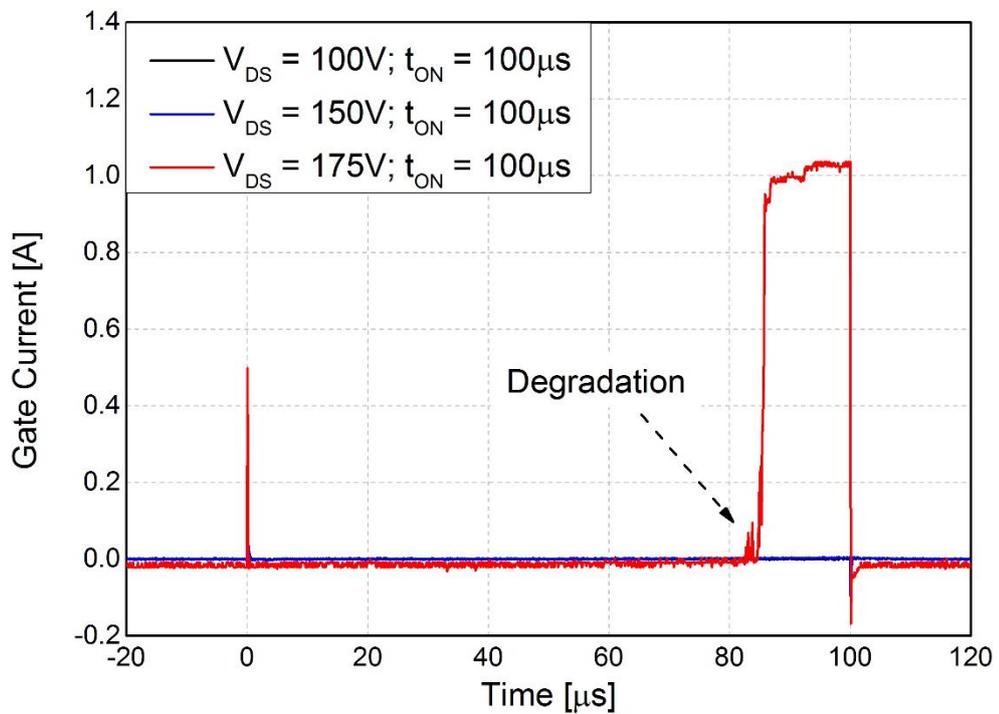
Figure 4.11: *Experimental Gate current (I_{GSS}) waveforms; <u>Dev-A</u>; t_{ON} = 100 µs; V_{GS} = 18 V; T_{CASE}*

= 25 °C; V_{DD} = 100 V, 150 V and <u>175 V (Degradation)</u>

Gate Voltage (V_{GS}) Sweep

The last set of results were carried out to study device behaviour at different V_{GS} without failure. Here, the test was performed at fixed t_{SC} of 6 μs for two different V_{GS} of 16 V and 19 V. The resulting I_D waveforms are shown in Figure 4.12. The test conditions are also summarised in Table 4.6. For comparison, lower V_{GS} implies lower $I_{SC(pk)}$ which results in lower $P_{SC(pk)}$. Obviously, as suggested earlier, the SC robustness is temperature dependent, thus, the DUTs during SC would be more robust at lower V_{GS} since lower $P_{SC(pk)}$ would result in lower T_J rise inside the device. However, it is desirable to operate at higher V_{GS} to benefit from better device performance as dictated by the device's transfer and output characteristics.

Table 4.6: *Summary of test conditions (<u>Dev-A</u>; Different V_{GS})*

V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	t_{SC} (μs)	$P_{SC(pk)}$ (kW)
600	75	16	6	85.20
		19		108.24
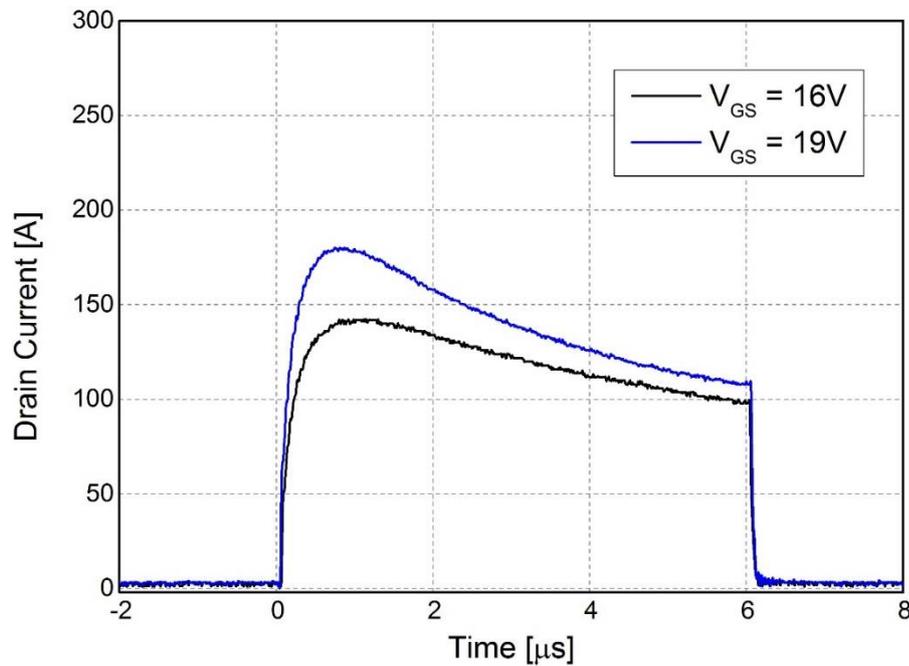
Figure 4.12: *Experimental SC drain current (I_D) waveforms; <u>Dev-A</u>; V_{DD} = 600 V; t_{SC} = 6 μs; T_{CASE}*

= 75 °C; <u>V_{GS} = 16 V and 19 V</u>

4.1.2. Experimental Results – Structural Characterisation

This section represents the experimental results carried out on bare dies. The tests presented here are on Dev-A at V_{DD} of 400 V and 600 V. Table 4.7 includes a summary of all test condition. Bespoke Infrared (IR) thermography, as explained in section 3.2.1 [65], was used to investigate the surface temperature distribution of the DUT under different test conditions with an aim to observe what the device undergoes close to and/or at failure. Figure 4.13 shows I_D waveforms resulting from a gradual increase in t_{ON} for V_{DD} = 400 V.

Table 4.7: Summary of test conditions (Dev-A)

| V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	t_{SC} (µs)
400	25	18	10, 13, 14, 15, 15.5, 16 and 17
600	25	18	5, 6, 7 and 8
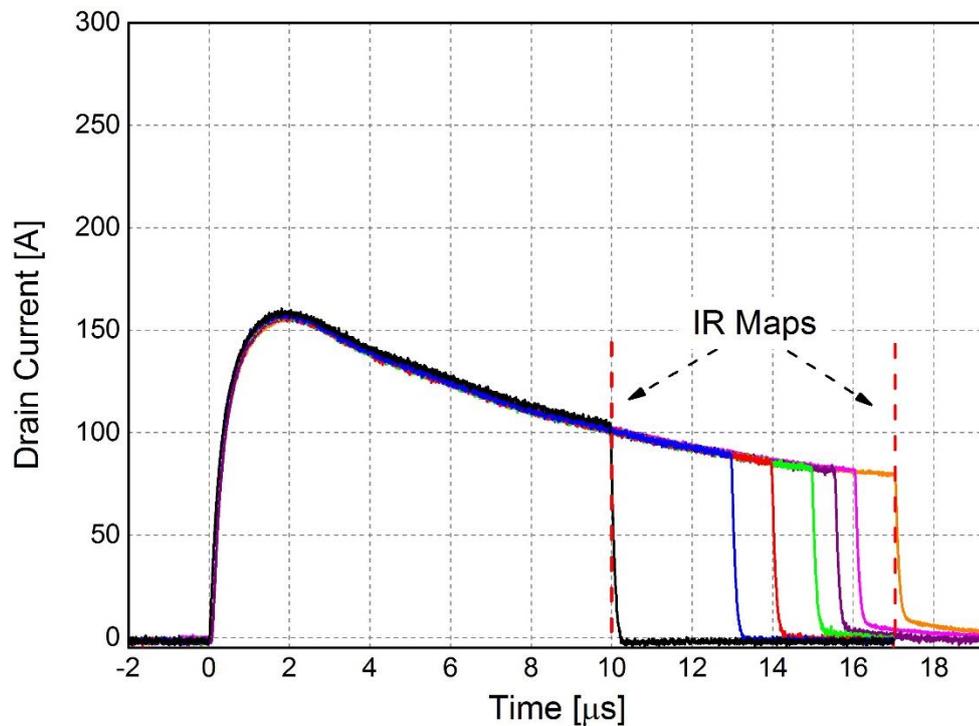
Figure 4.13: Experimental SC drain current (I_D) waveforms; Dev-A; V_{DD} = 400 V; V_{GS} = 18 V; T_{CASE} = 25 °C; t_{sc} = 10 µs, 13 µs, 14 µs, 15 µs, 15.5 µs, 16 µs and 17 µs

IR system was configured to capture a thermal image at end of each t_{ON} pulse. Two different thermal maps showing normalized surface temperature distribution (measured temperatures were well in excess of 500 °C and outside of the camera's calibration range as also discussed in section 3.2.1) are presented in Figure 4.14 (a) and (b) corresponding to t_{SC} of 10 µs and 17 µs respectively. The Figure 4.14 (a) shows a uniform temperature distribution (t_{SC} = 10 µs) over the entire device's active area due to having uniform current conduction throughout the entire device. However, when t_{ON} reached 17 µs, the surface temperature distribution was non-uniform (encircled portion) as could be seen in Figure 4.14 (b). It shows that an essential feature(s) of the device in the encircled portion was somehow degraded. Thus, cells in that portion carry less current and finally become inoperative (residual R_{GS} measured in few ohms).

(a) – t_{SC} = 10 µs

(b) – t_{SC} = 17 µs
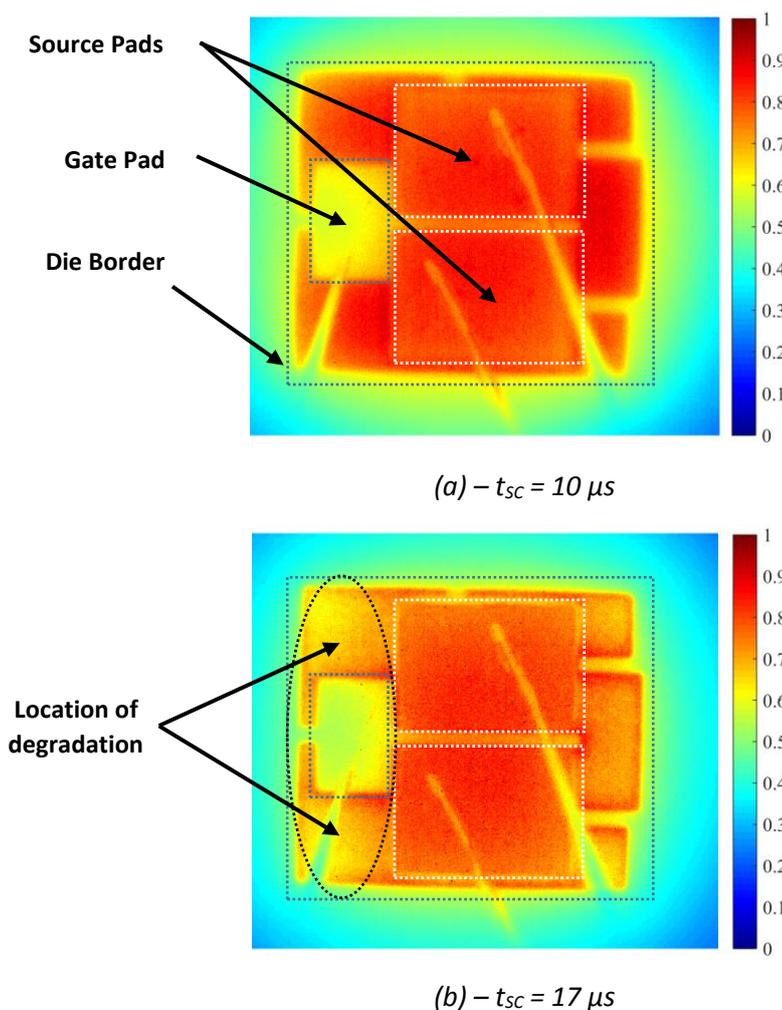
Figure 4.14: *Normalized temperature distribution; <u>Dev-A</u>; <u>V_{DD} = 400 V</u>; V_{GS} = 18 V; T_{CASE} = 25 °C*

The I_D waveforms for the test at V_{DD} = 600 V are included in Figure 4.15. Here, the IR map corresponding to turn-off of t_{SC} = 8 μs at failure is presented in Figure 4.16. The thermal map discovered phenomena of current crowding in a small confined area leading to the formation of a hot-spot (encircled; positive feedback phenomena) prior to failure as can be seen in Figure 4.16. Such phenomena occur when the temperature within a small cluster of cells keeps on increasing when makes those cells draw more and more current leading to thermal runaway.
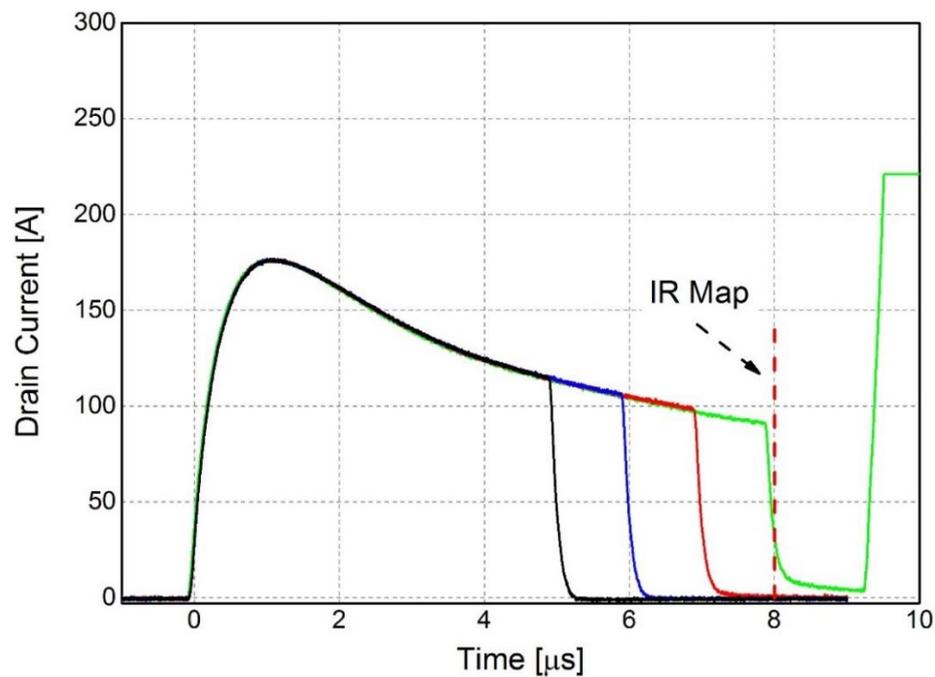
Figure 4.15: *Experimental SC drain current (I_D) waveforms; <u>Dev-A</u>; <u>V_{DD} = 600 V</u>; V_{GS} = 18 V;*

T_{CASE} = 25 °C; t_{SC} = 5 μs, 6 μs, 7 μs and <u>8 μs (Failure)</u>
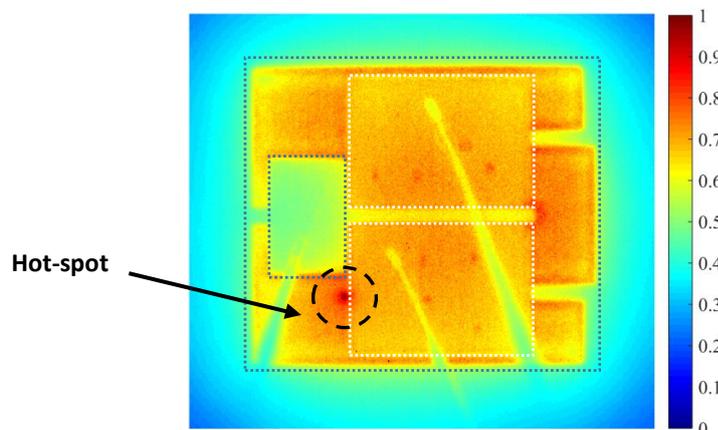
Figure 4.16: *Normalized temperature distribution; <u>Dev-A</u>; <u>V_{DD} = 600 V</u>; V_{GS} = 18 V; T_{CASE} = 25 °C*

4.1.3. Aging Test Results

Another important aspect to be investigated was the SC robustness of SiC power MOSFETs when subjected to repetitive SC stress and hence aging tests were carried out. It is important since SC events could occur quite frequently during power systems. Here, the packaged Dev-A DUT was subjected to repetitive pulses of t_{SC} with an aim to detect variations, if any, in electrical waveforms. Therefore, t_{SC} value of 10 µs corresponding to usual nominal requirement (far away from failure critical t_{SC} duration) was chosen for a given set of test conditions also summarised in Table 4.8. The aging test was carried out at V_{DD} = 400 V, V_{GS} = 19 V and T_{CASE} = 150 °C and the resulting I_D waveforms for up to 1000 SC pulses are presented in Figure 4.17. An obvious change in the device characteristics was manifested as the aging stress accumulated. The I_D current during SC decreased significantly (but later on stabilized) as the number of pulses increased. The V_{GS} along with voltage drop across (R_G) were also measured. The voltage drop across R_G was then used to calculate I_{GS} given the R_G value. The evolution of V_{GS} and I_{GS} waveforms during the aging test are depicted in Figure 4.18 and 4.19 respectively. The decrease in V_{GS} could be better understood by making a reference to increasing I_{GS} shown in Figure 4.19. Increase in I_{GS} possibly indicates degradation of structural features (such as gate oxide and/or metallization layer) which resulted in a decrease of the overall resistance within the gate-to-source loop. As a result of that, a concurrent increase in the device's R_{ON} was observed therefore explaining the observed I_D decrease [95].

Table 4.8: *Summary of aging test conditions (Dev-A)*

V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	t_{SC} (µs)
400	150	19	10
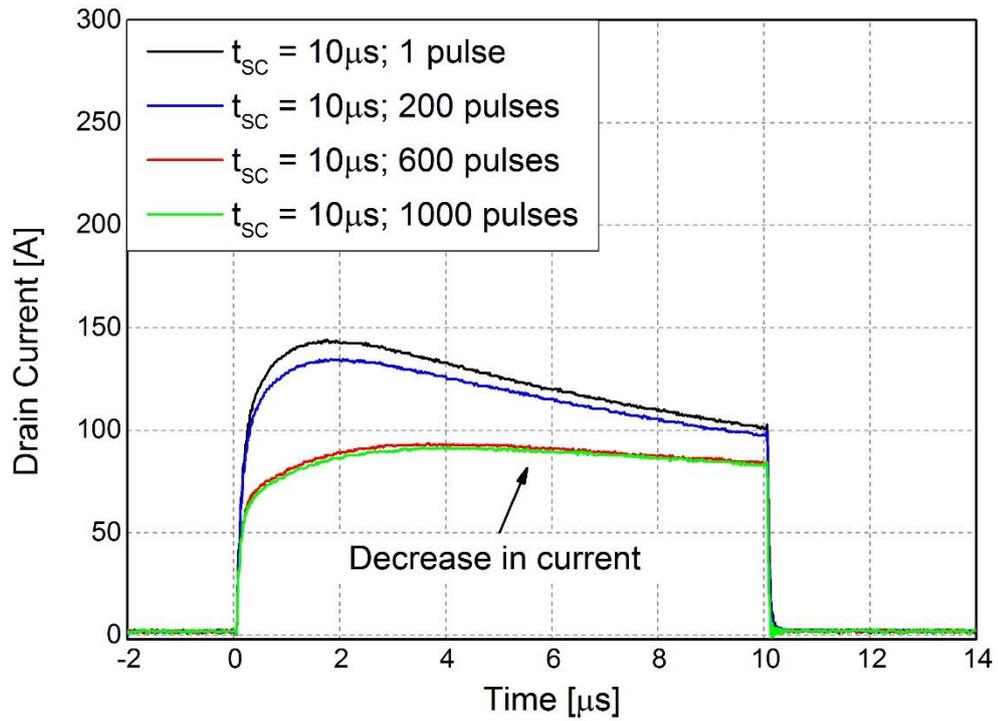
Figure 4.17: *Experimental SC drain current (I_D) waveforms; V_{DD} = 400 V; V_{GS} = 19 V; T_{CASE} = 150 °C; <u>Dev-A</u>; <u>t_{SC} = 10 µs (1000 pulses)</u>*
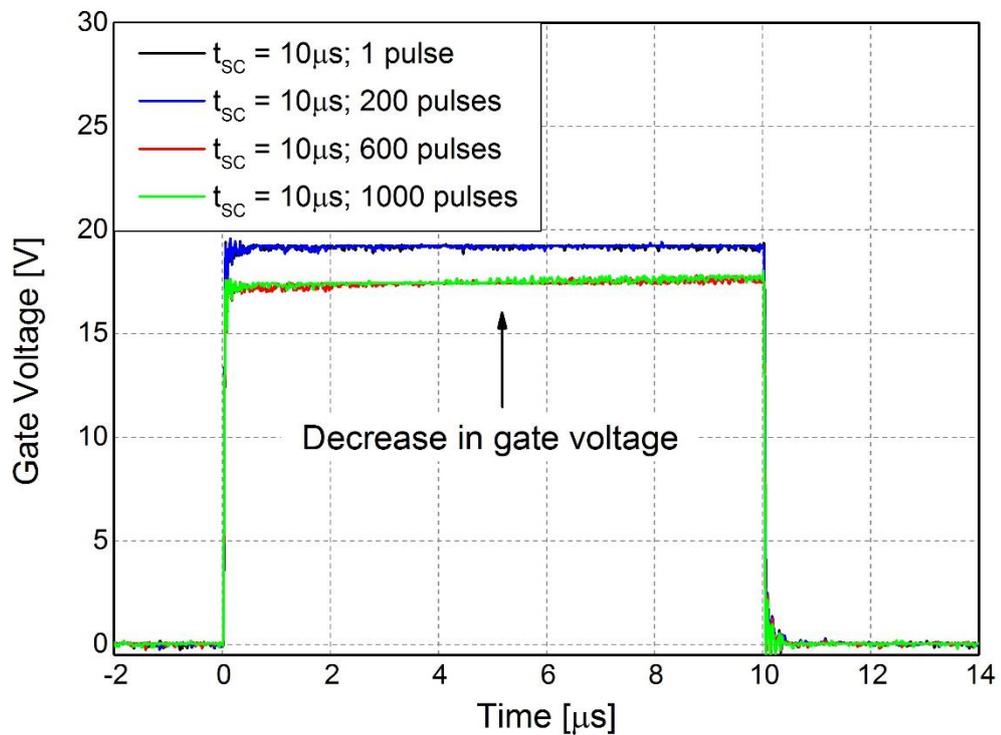
Figure 4.18: *Experimental Gate voltage (V_{GS}) waveforms; V_{DD} = 400 V; V_{GS} = 19 V; T_{CASE} = 150 °C; <u>Dev-A</u>; <u>t_{SC} = 10 µs (1000 pulses)</u>*
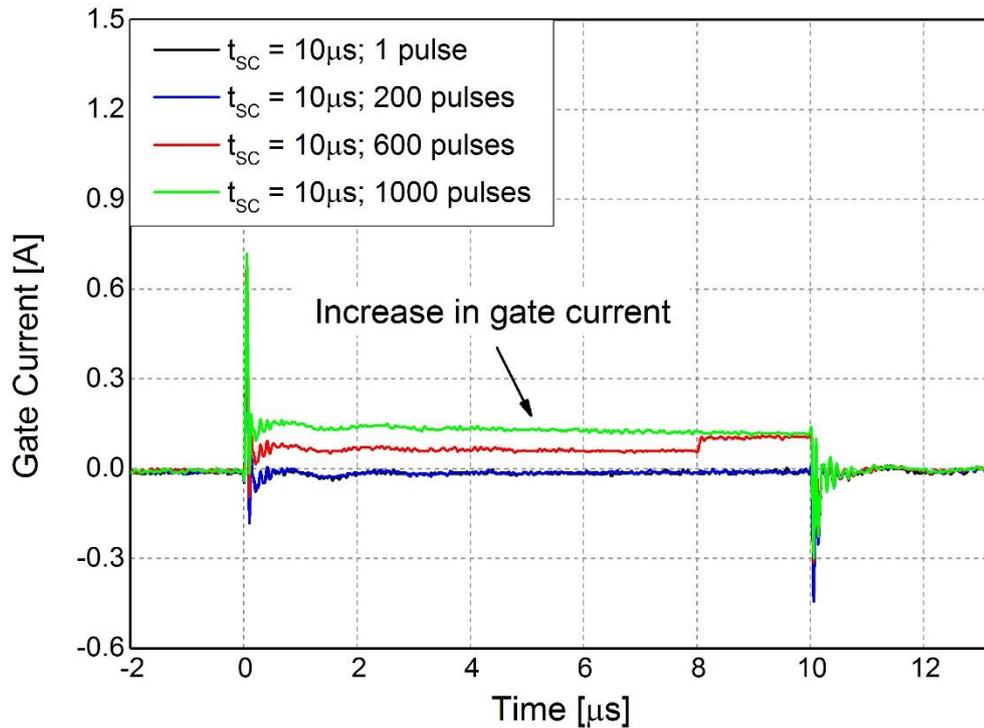
Figure 4.19: *Experimental Gate current (I_{GS}) waveforms; V_{DD} = 400 V; V_{GS} = 19 V; T_{CASE} = 150*

°C; Dev-A; t_{SC} = 10 µs (1000 pulses)

4.1.4. Experimental Results – On other DUTs

Dev-B: Some tests were also performed on Dev-B DUT and the corresponding I_D waveforms

are included in Figure 4.20 and the test conditions are summarised in Table 4.9. The tests were

performed at V_{DD} = 600 V, V_{GS} = 18 V and T_{CASE} = 25 °C. Here, the t_{ON} of the DUT was increased

with an aim to discover precursors of failures, if any, similar to the ones observed above for

Dev-A. As the t_{ON} was increased, the appearance of prominent current tails started to appear

(as also observed earlier) at approximately t_{SC} = 13 µs onwards.

Table 4.9: *Summary of test conditions (Dev-B)*

| V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	t_{SC} (µs)
600	25	18	12, 13, 14, 14.5, 15 and 15.5
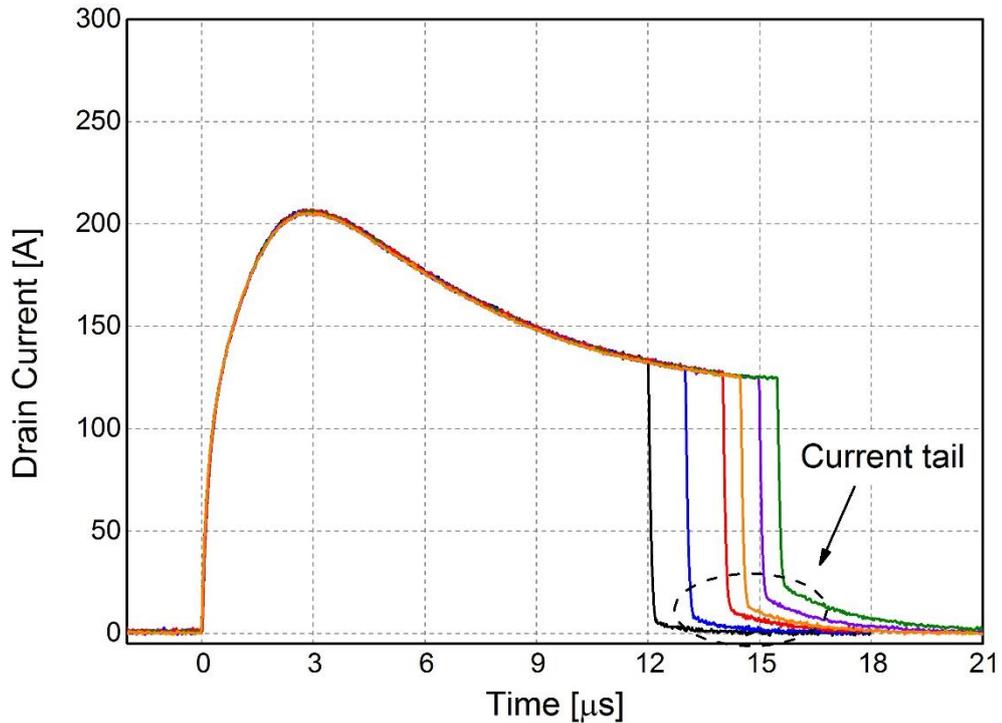
Figure 4.20: *Experimental SC drain current (I_D) waveforms; <u>Dev-B</u>; V_{DD} = 600 V; V_{GS} = 18 V;*

T_{CASE} = 25 °C; t_{SC} = 12 μs, 13 μs, 14 μs, 14.5 μs, 15 μs and 15.5 μs

Dev-C: A few tests performed on Dev-C DUT are also presented here. Figure 4.21 shows I_D waveforms for tests performed at V_{DD} = 400 V, V_{GS} = 20 V and T_{CASE} = 25 °C. The test conditions are included in Table 4.10. Here, again, similar precursors leading to failure were identified as already observed for previous DUT types. The current tails started to appear at approximately t_{SC} = 8 μs which became prominent as the t_{ON} was increased further. Dev-C DUT also exhibited similar signs prior to failure indicating possibly that the physical mechanism responsible for different SiC power MOSFETs tested during SC are probably similar to each other.

Table 4.10: *Summary of test conditions (<u>Dev-C</u>)*

| V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	t_{SC} (μs)
400	25	20	7, 8, 8.5, 9 and 9.5
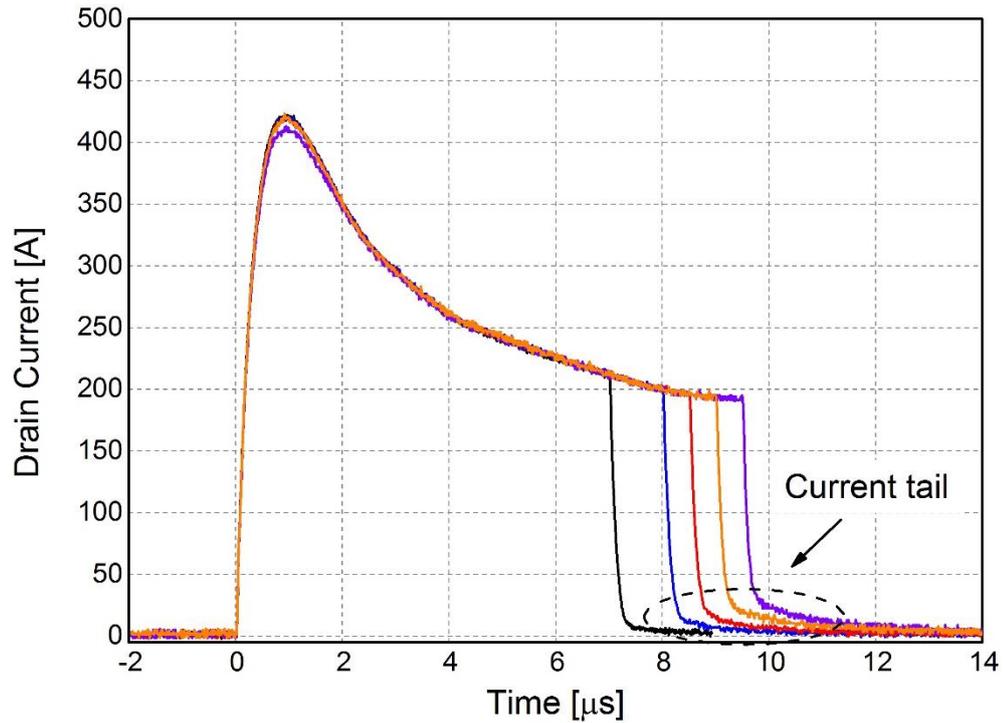
Figure 4.21: *Experimental SC drain current (I_D) waveforms; <u>Dev-C</u>; V_{DD} = 400 V; V_{GS} = 20 V;*

T_{CASE} = 25 °C; t_{sc} = 7 μs, 8 μs, 8.5 μs, 9 μs, and 9.5 μs

4.2.   Simulation Results

The simulations were carried out at: V_{DD} = 400 V; V_{GS} = 18 V; T_{CASE} = 25 °C. The simulated I_D waveforms showing current tail and change in current derivative at device turn-off along with corresponding average surface temperature (t_{sc} = 17 μs, 18 μs, and 18.5 μs) are included in Figure 4.22. In order to better understand the underlying mechanism responsible for the formation of the current tail, the hole current component flowing out of the P-Body terminal (separated from the N+ Source terminal; two separate terminals for P-Body and N+ Source were used) was plotted as shown in Figure 4.23. From Figure 4.23, the significant hole current component flow could be observed which would also be responsible for the change of current slope just before turn-off. Another aspect to be noted in Figure 4.22 is the extremely high average surface temperatures at around 1000 K.
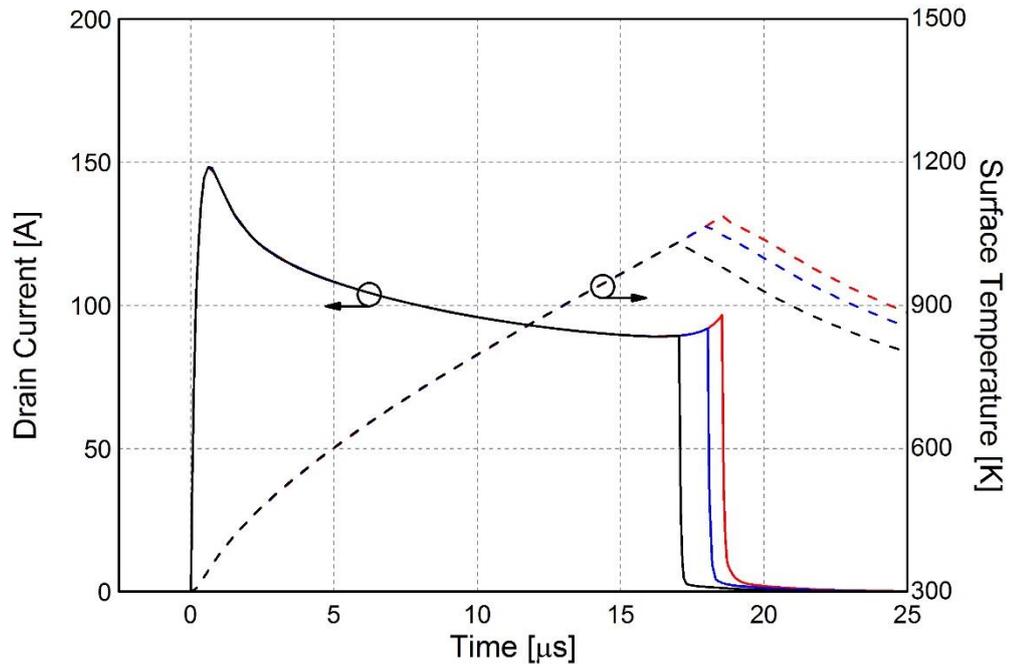
Figure 4.22: *Simulated SC drain current (I_D) waveforms (solid); Average surface temperature*

(dashed) $\underline{V_{DD} = 400\ V}$; $V_{GS} = 18\ V$; $T_{CASE} = 25\ °C$; $t_{sc} = 17\ μs$, $18\ μs$, and $18.5\ μs$
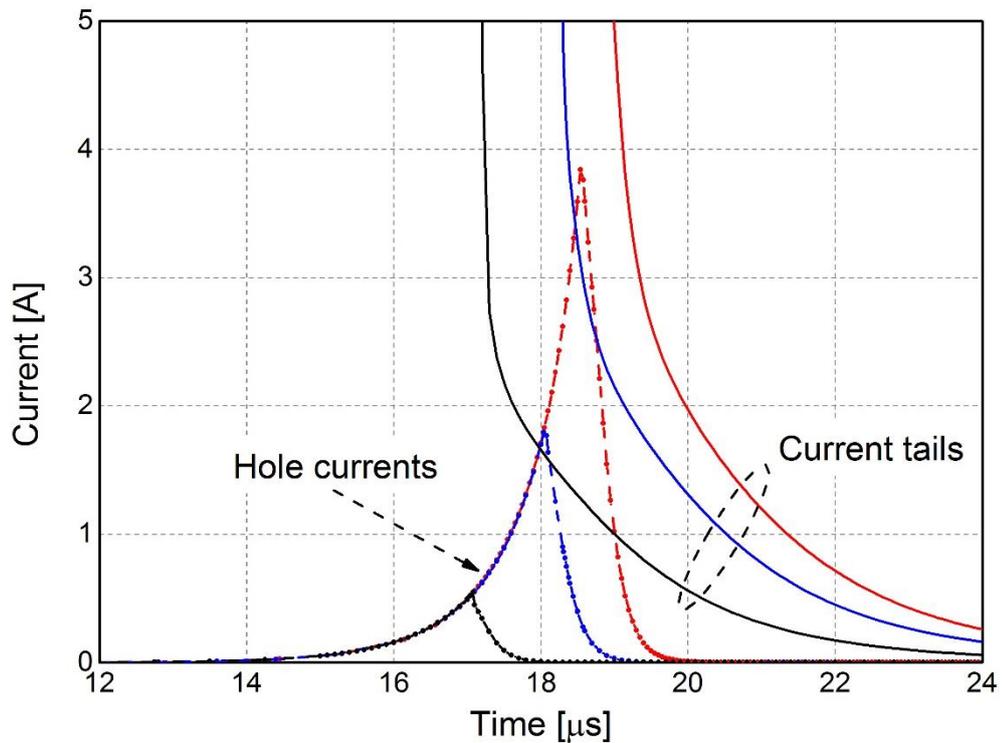
Figure 4.23: *Simulated SC drain current (I_D) waveforms (solid); Hole current component*

(dash/dot) $\underline{V_{DD} = 400\ V}$; $V_{GS} = 18\ V$; $T_{CASE} = 25\ °C$; $t_{sc} = 17\ μs$, $18\ μs$, and $18.5\ μs$

The hole current density within the cell structure was also plotted at different time instances for t_{SC} = 18.5 µs as illustrated in Figure 4.24. At the start (t = 16 µs), hole concentration value is insignificant and therefore, the leakage current between the P-Body / N-Drift junction is negligible. However, as the temperature increased further (t = 16.5 µs – t = 18.5 µs), hole concentration level increased giving rise to a gradual increase in the leakage current, thus concurrently also resulting in hole current component flowing out of the P-Body terminal. The presence of high electric field (E) in the N-Drift region generated hole carriers which move towards the top of the device. Once the hole carrier concentration is high enough, they eventually punch through the P-Body / N-Drift region resulting in significant hole current density. At the same time, however much smaller in magnitude, leakage current due to the generation of electrons from source to drain also takes place when V_{GS} = 0 V. Indeed, the current tail consists of both hole and electron current components responsible for leakage current. The current tail eventually goes to zero once all the generated carriers are removed (t = 19 µs – t = 20 µs).
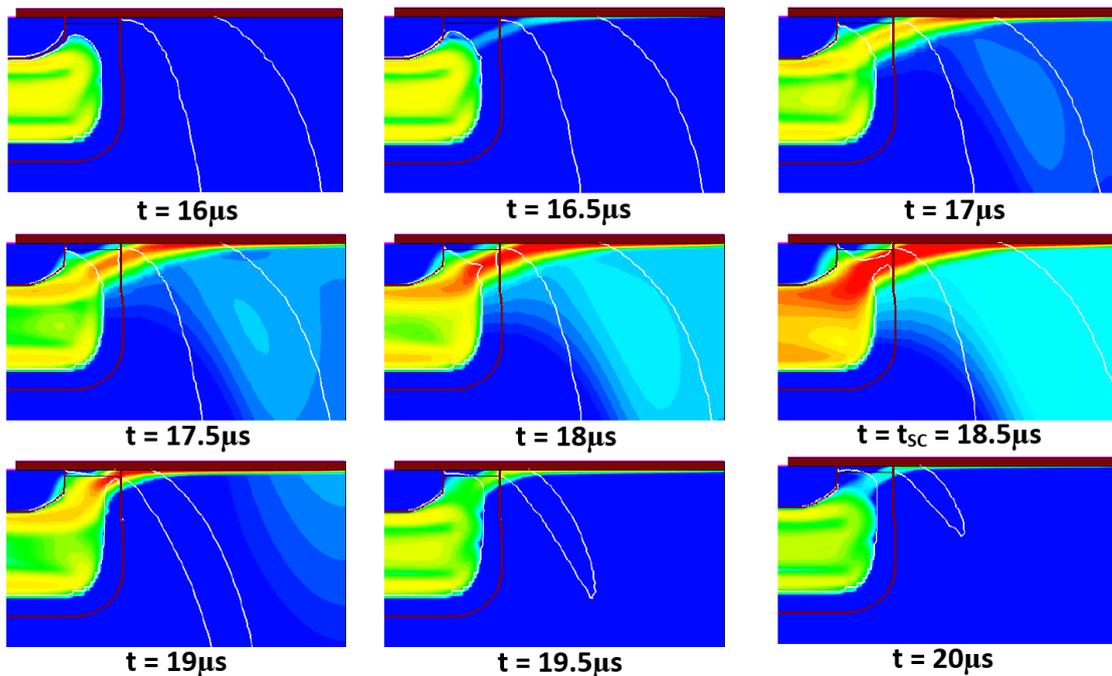
Figure 4.24: *Simulated hole current density; V_{DD} = 400 V; V_{GS} = 18 V; T_{CASE} = 25 °C*

Moreover, leakage current could also reach critical level resulting in device failure due to thermal runaway. Simulated I_D waveforms (t_{sc} = 5 µs, 5.5 µs, and 6.2 µs) along with corresponding average surface temperature waveforms carried out at V_{DD} = 600 V; V_{GS} = 18 V; T_{CASE} = 25 °C are included in Figure 4.25. At failure after DUT turn-off, the I_D increases uncontrollably after turn-off due to this positive feedback phenomena of thermal runaway. Furthermore, SC withstand capability is deteriorated as the T_{CASE} is increased since it requires a shorter time to reach the critical temperature to trigger thermal runaway as clearly depicted by the experimental results in Figure 4.3 and 4.4. Since the starting temperature is higher, it takes less time to thermally generate carriers responsible for leakage current value corresponding to the critical T_J causing failure. The increase in current slope at DUT turn-off is much more significant in simulations as compared to the experimental results presented earlier. It is due to the reason that the simulations were carried out with single cell whereas a real device consists of many cells which will have some differences introduced alongside the process. Thus, the electro-thermal interactions with surrounding cells are not taken into account. Lastly, all the test conditions at which the simulations were performed are also summarised in Table 4.11.

Table 4.11: *Summary of simulation test conditions*

V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	t_{SC} (µs)
400	25	18	17, 18 and 18.5
600			5, 5.5 and 6.2
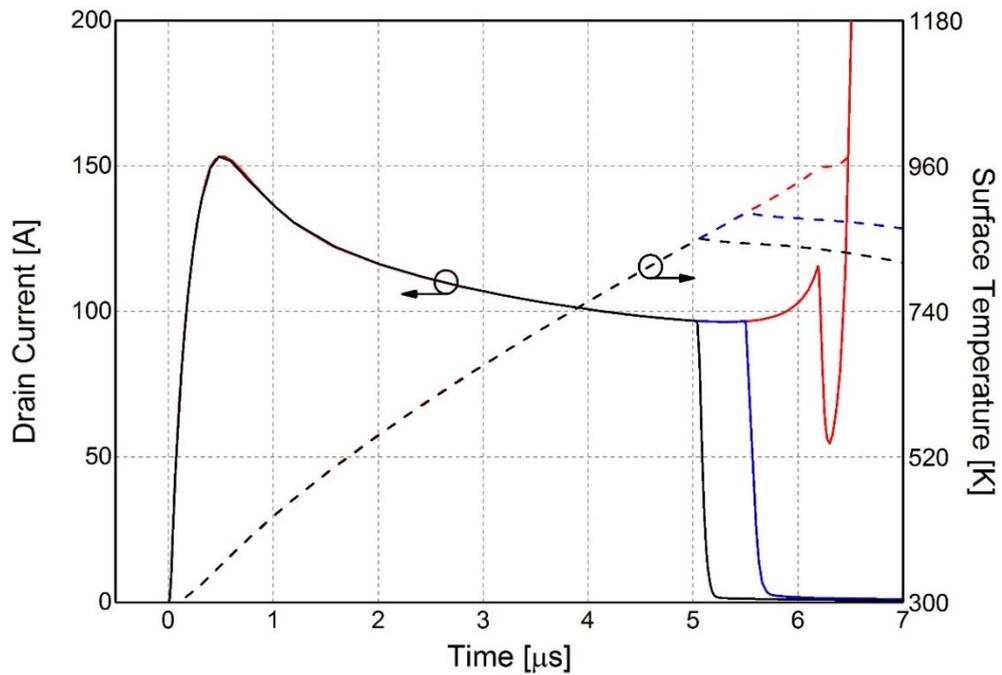
Figure 4.25: *Simulated SC drain current (I$_D$) waveforms (solid); Average surface temperature (dashed) V$_{DD}$ = 600 V; V$_{GS}$ = 18 V; T$_{CASE}$ = 25 °C; t$_{sc}$ = 5 µs, 5.5 µs, and 6.2 µs (Failure)*

4.3. Discussion

The overall aim of this chapter is to present a pool of experimental results in order to extensively characterise SiC power MOSFETs as well as identify device limitations under SC operation at various different test conditions. In order to achieve this, functional and structural characterisation was performed followed by TCAD simulations in order to interpret experimental results as well as understand the corresponding underlying physical mechanisms responsible for failure when subjected to SC condition. Tests have been presented here on three different device types of similar ratings from different manufacturers. The appearance of current tails and change of current slope at device turn-off associated to reaching critical T$_J$ temperature within the device have been identified as signs leading to device failure. Also, it is apparent that these devices are unable to attain the SC withstand capability requirement of t$_{SC}$ = 10 µs at two-thirds of the rated V$_{DS(max)}$ [51]. From

the experimental and simulation results presented above, following statements about SC robustness of SiC power MOSFETs could be said:

➤ Dependence on T_{CASE}. Higher T_{CASE} deteriorates t_{SC} capability. As T_{CASE} is increased, the margin required to reach critical temperature for failure shrinks as also supported by Figure 4.3 and 4.4.

➤ Dependence on V_{DD}. Higher V_{DD} worsens t_{SC} capability. As V_{DD} is increased, $P_{SC(pk)}$ also increases. Higher $P_{SC(pk)}$ results in sharper temperature rise and hence reaching critical T_J faster showing precursors of failures as also demonstrated in Figure 4.6.

➤ Dependence on V_{GS}. Higher V_{GS} results in higher $I_{SC(pk)}$ (dictated by the transfer characteristics) while keeping other test conditions unaltered as shown in Figure 4.12. Higher $I_{SC(pk)}$ would result in higher $P_{SC(pk)}$ thus SC robustness worsens for higher V_{GS}. Devices can be operated at lower V_{GS} to give longer SC withstanding but at an expense of poorer on-state performance.

➤ Two different failure mechanisms as illustrated with aid of Figure 4.26. Type I: Uncontrollable increase in I_D (thermal runaway) for higher V_{DD} (See Figure 4.3, 4.7, 4.15, 4.16 and 4.25). Type II: Degradation due to a permanent change in device features such as metallization layer and/or passivation layer for lower V_{DD} (Demonstrated in Figure 4.8 – 4.11 and 4.14).

➤ The $I_{SC(pk)}$ decreases as the DUT ages subjected to repetitive SC pulses as also illustrated in Figure 4.17 – 4.19. It is due to an irreversible increase in contact resistivity of source metal resulting in an increase of R_{ON} as also discussed in [95].

Finally, to conclude this chapter, different failure mechanism for SiC power MOSFETs during SC are discussed here. As briefly mentioned earlier, two possible phenomena occur giving rise to two different failure mechanisms. They have been labelled as Type I and Type II failure modes. During Type I failure mode, DUT at failure experiences a sharp increase in I_D resulting

in thermal runaway. Whereas, Type II failure mode occurs due to degradation of essential device features (such as gate oxide, metallization layer and/or passivation layer) and hence resulting in device eventually becoming inoperative. Both modes are temperature driven but are distinguished by the change in junction temperature over time (dT_J/dt) as demonstrated in Figure 4.26. It is due to the fact that temperature rise is directly proportional to power dissipation and hence to V_{DD}. The temperature required to trigger thermal runaway ($T_{T\_RUNAWAY}$) would obviously be higher than the temperature required to cause degradation ($T_{DEGRADATION}$) of device features. For the case when power dissipation is lower, device temperature would have slower dynamics high enough to surpass the degradation threshold ($T_{DEGRADATION}$) but not enough to reach thermal runaway threshold ($T_{T\_RUNAWAY}$). If the device is subjected to $T_{DEGRADTAION}$ for long enough duration, it results in irreversible damage to device features (Type II failure). As a result of this, the device loses partial or full ability to conduct current. On the contrary, higher power dissipation results in a faster temperature rise such that it reaches $T_{T\_RUNAWAY}$. At this point, a large number of hole carriers are generated which is responsible for high leakage current resulting in a thermal runaway (results in uncontrollable I_D increase and device destruction – Type I failure). In this case, the duration DUT stays at $T_{DEGRADATION}$ is not long enough to cause substantial damage to the device surface. For intermediate power levels, the failure type is distinguished by the time required to degrade the device and time needed to trigger thermal runaway point. In a certain case, where both occur, Type I failure mechanism always prevails.
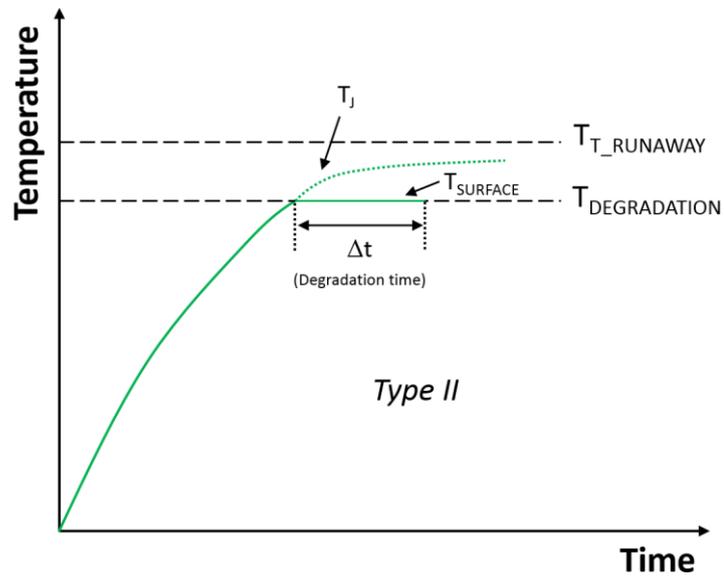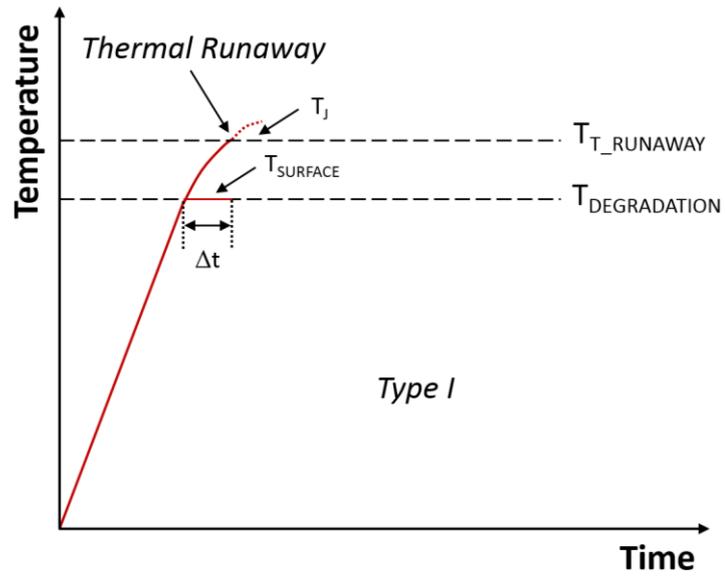
Figure 4.26: *Proposed types of failure (Type I and Type II)*

5. Avalanche Breakdown Robustness

5.1. Experimental Testing and Results

5.1.1. Experimental Results – Functional Characterisation

This section represents all the experimental results obtained on packaged SiC power MOSFETs during UIS. Tests were carried out parametrically over: T_{CASE}, V_{DD}, V_{GS}, and L_{LOAD}. The test results presented in chapter 5 are on three different DUTs from different manufacturers. Some of the important features of these devices are summarised here in Table 5.1.

***Table 5.1:** Summary of relevant device parameters*

DUT	$V_{DS(max)}$ (V)	$R_{DS(on)}$ @ 25 °C (mΩ)	I_D @ 25 °C (A)	C_{OSS} (pF)	Package
Dev-A [91]			36	80	TO-247
Dev-B [92]	1200	80	40	77	
Dev-C [93]			45	130	HiP247^{TM}

T_{CASE} Sweep

The first set of UIS results for three different T_{CASE} values (–25 °C, 25 °C and 75 °C) are presented here in order to assess the avalanche robustness of Dev-A DUTs while keeping all the other parameters (V_{DD} = 400 V, L_{LOAD} = 500 µH and V_{GS} = 0 V) unaltered. Figure 5.1 present V_{DS} and I_L waveforms for a safe UIS event at T_{CASE} of –25 °C. A safe UIS test is characterized by the return of I_L and V_{DS} to zero and V_{DD} (blocking state) respectively. The V_{DS} and I_L waveforms at failure for T_{CASE} of –25 °C are also included in Figure 5.2. For a UIS transient at failure, illustrated in Figure 5.2, the DUT loses its blocking ability resulting in a sharp collapse of V_{DS} and the current starts to increase again (as dictated by V_{DD} and L_{LOAD}) due to an internal short amongst all the DUT terminals followed by a catastrophic failure.
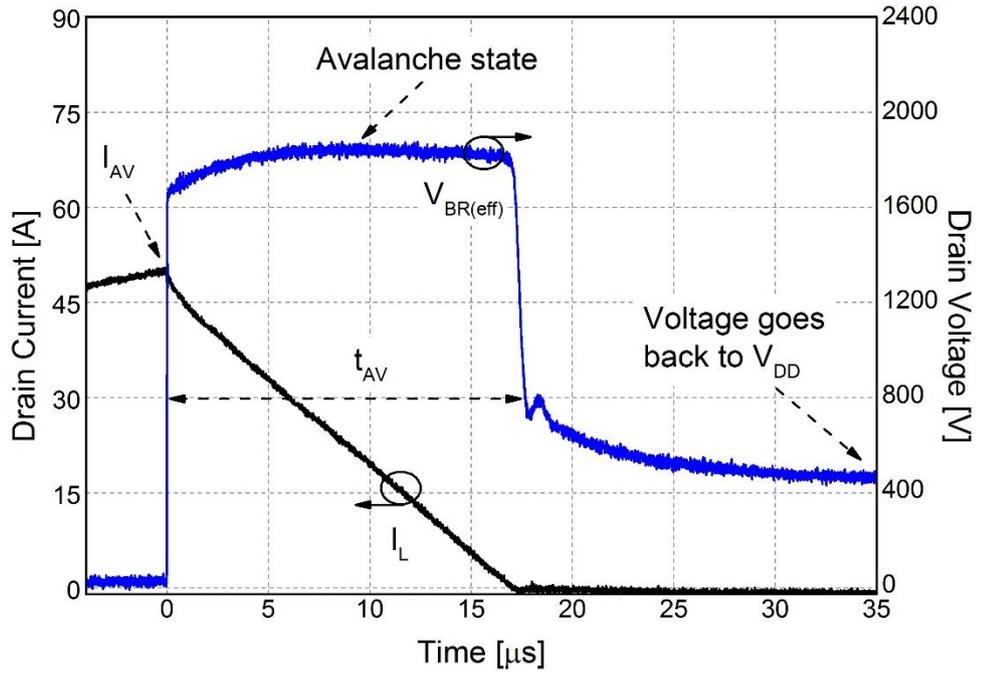
Figure 5.1: *Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 400 V; V_{GS} = 0 V; T_{CASE} = −25 °C; L_{Load} = 500 μH; <u>Dev-A</u>; <u>Safe UIS</u>*
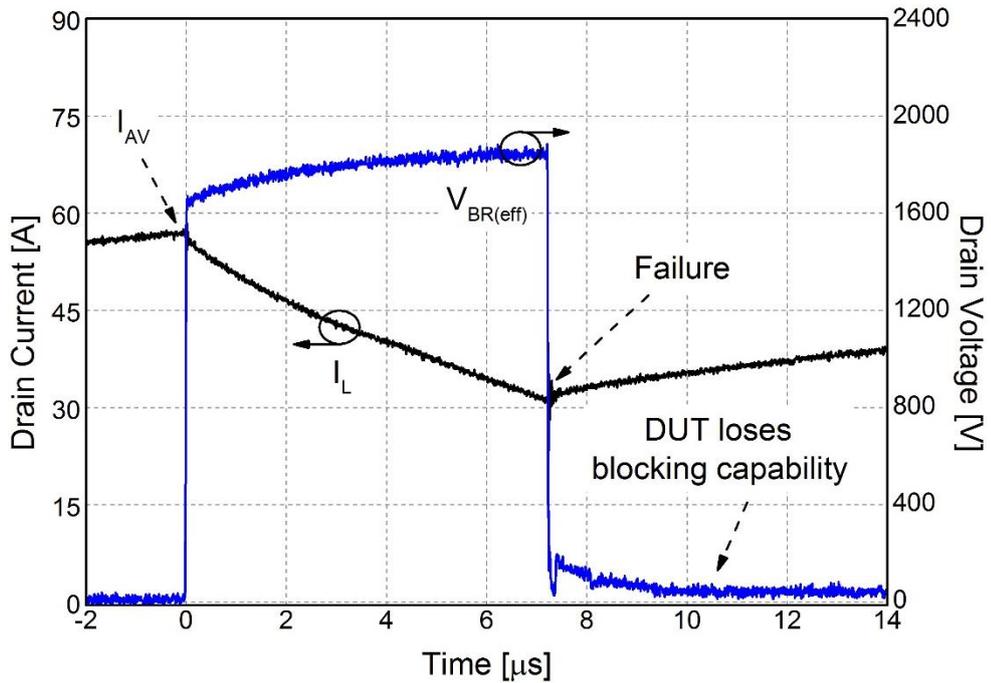
Figure 5.2: *Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 400 V; V_{GS} = 0 V; T_{CASE} = −25 °C; L_{Load} = 500 μH; <u>Dev-A</u>; <u>Failure UIS</u>*

T_{CASE} (°C)	V_{DD} (V)	V_{GS} (V)	L_{LOAD} (µH)	I_{AV} (A) at Failure	E_{AV} (J)** at Failure
-25				57	0.99
25	400	0	500	49	0.77
75				43	0.68

In order to study the behaviour of T_{CASE} on DUTs, L_{LOAD} was kept same while t_{ON} was increased to get higher I_{AV} value until failure was observed for each T_{CASE}. The failure I_L waveforms for three T_{CASE} are included in Figure 5.3. At failure, an important observation about I_{AV} in Figure 5.3 is that its value decreases as the T_{CASE} is increased. At the same time, decreasing I_{AV} value with increasing T_{CASE} also results in a lower E_{AV}. The corresponding V_{DS} waveforms at failure are also shown in Figure 5.4.

** Failure: I_L and V_{DS} were extrapolated to 0 A and V_{DD} respectively in order to obtain E_{AV}
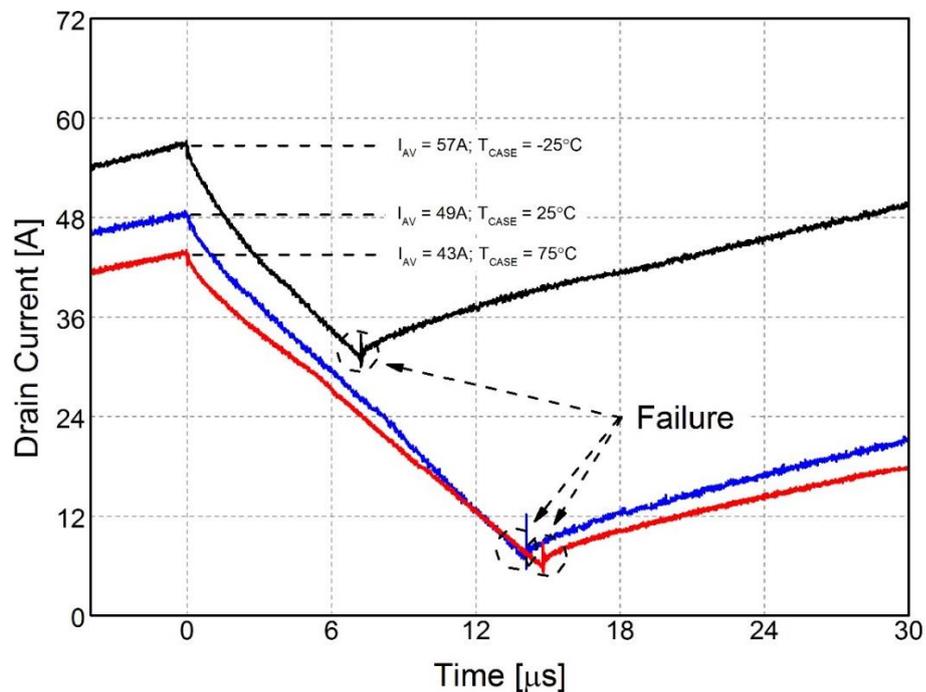
Figure 5.3: *Experimental UIS inductor current (I_L) waveforms; Dev-A; V_{DD} = 400 V; L_{Load} = 500 µH; V_{GS} = 0 V; T_{CASE} = −25 °C, 25 °C and 75 °C; Comparison*
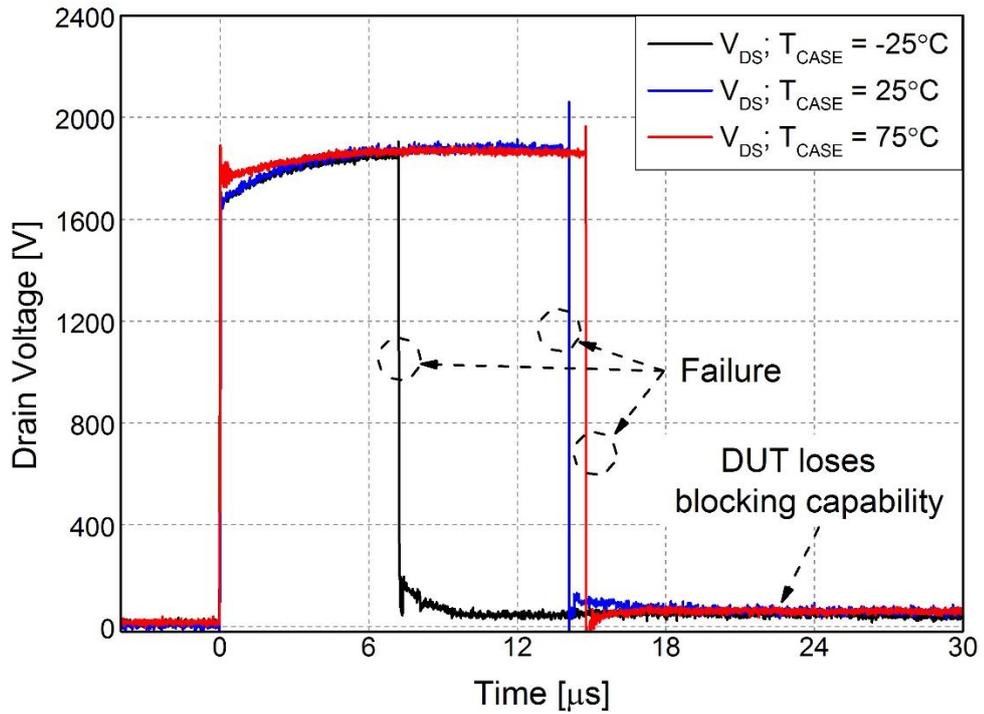
Figure 5.4: *Experimental UIS drain voltage (V_{DS}) waveforms; <u>Dev-A</u>; V_{DD} = 400 V; L_{Load} = 500*

μH; V_{GS} = 0 V; T_{CASE} = −25 °C, 25 °C and 75 °C; <u>Comparison</u>
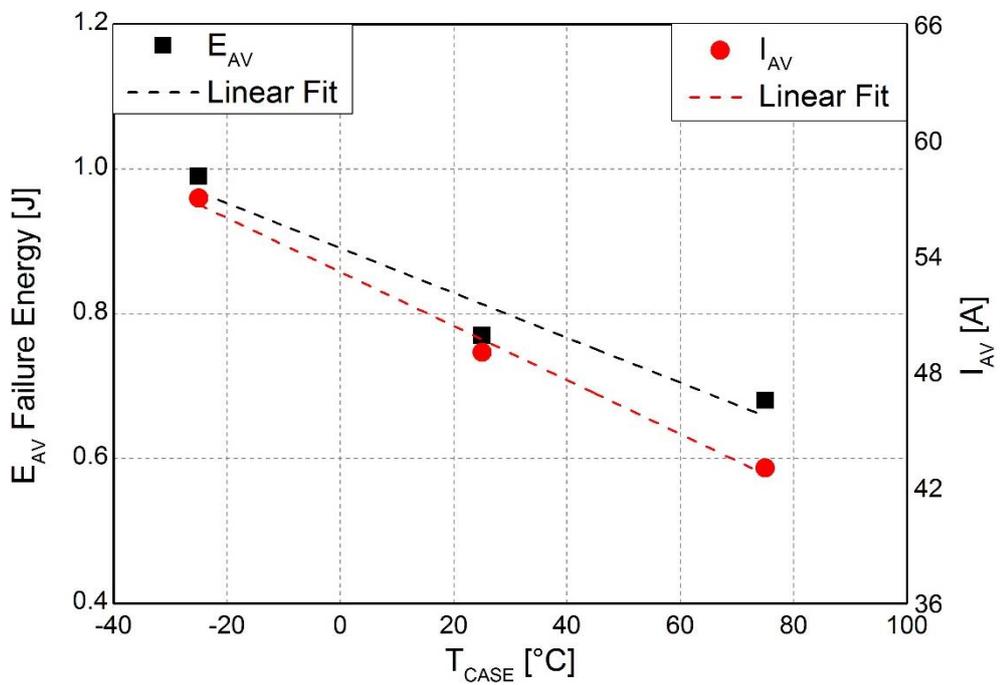
Figure 5.5: *Relationship for E_{AV} and I_{AV} at failure versus T_{CASE}; <u>Dev-A</u>*

Figure 5.5 plots E_{AV} and I_{AV} for failure conditions versus T_{CASE}. The summary of all relevant test conditions is included in Table 5.2 along with corresponding E_{AV} values (defined using equation 3.6) which were calculated using *trapz* function within MATLAB. The avalanche energy at failure is defined as critical E_{AV}. The avalanche capability of Dev-A DUT deteriorates as the T_{CASE} is increased as the switched current I_{AV} and energy being dissipated in avalanche (E_{AV}) is reduced before the destructive failure onsets. The results above give a clear indication that the avalanche breakdown capability and the associated failure of these devices are temperature dependent.

L_{LOAD} Sweep

The second set of UIS results included here are for different L_{LOAD} values (2430 µH, 2010 µH, and 1690 µH) while keeping all the remaining test conditions (V_{DD} = 400 V, T_{CASE} = 150 °C, and V_{GS} = 0 V) unchanged. Some of the selective I_{AV} and V_{DS} waveforms are presented in Figure 5.6 and 5.7 respectively. The test conditions are also summarised in Table 5.3. The tests on Dev-A were carried out at different L_{LOAD} in order to obtain different energy dissipation rates (i.e. different current slopes) during avalanche phase while keeping E_{AV} approximately constant at 1 J. The tests were started with the biggest available value of L_{LOAD} and decreasing its value until failure was obtained. As the L_{LOAD} value is decreased, the I_{AV} value becomes bigger and the resultant t_{AV} duration becomes smaller to give the same amount of E_{AV} dissipation as can be seen from Figure 5.6. As I_{AV} is increased, the peak power dissipation during avalanche ($P_{AV(pk)}$) also increases which results in a faster T_J rise within DUT. Therefore, for the case of L_{LOAD} = 1690 µH, the failure was obtained due to higher I_{AV} resulting in higher T_J even though E_{AV} was kept same. These results clearly indicate the dependence of E_{AV} dissipation on the L_{LOAD} value. The avalanche capability of Dev-A DUTs deteriorates as the L_{LOAD} is increased.
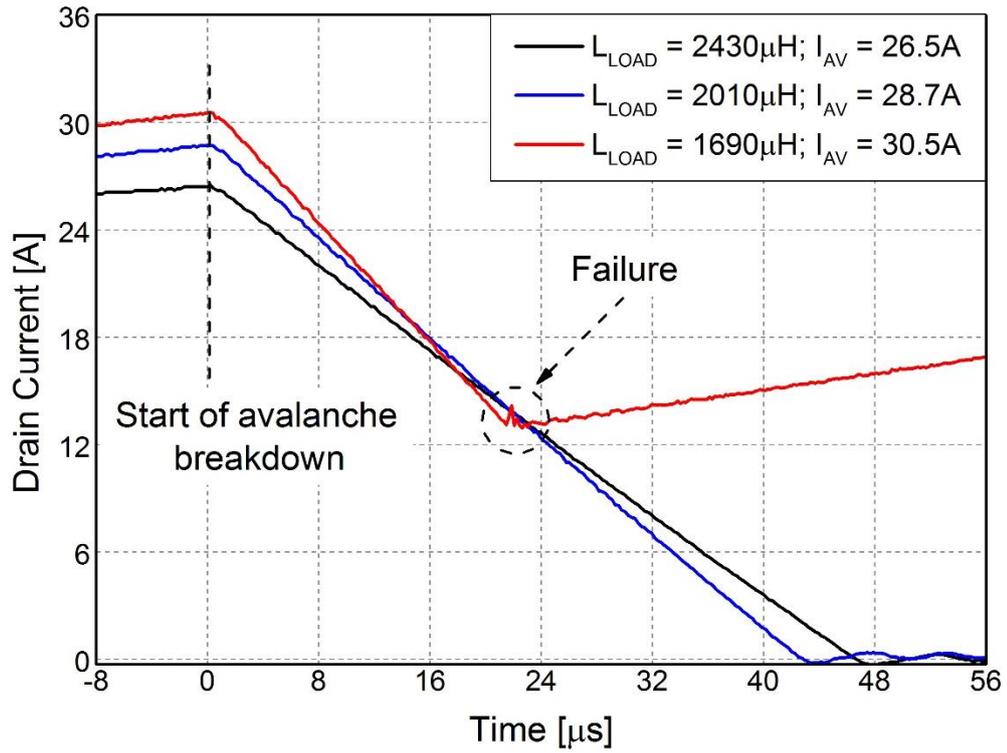
Figure 5.6: *Experimental UIS inductor current (I_L) waveforms; <u>Dev-A</u>; V_{DD} = 400 V; V_{GS} = 0 V;*

T_{CASE} = 150 °C; L_{Load} = 2430 μH, 2010 μH and 1690 μH; <u>Same E_{AV}</u>
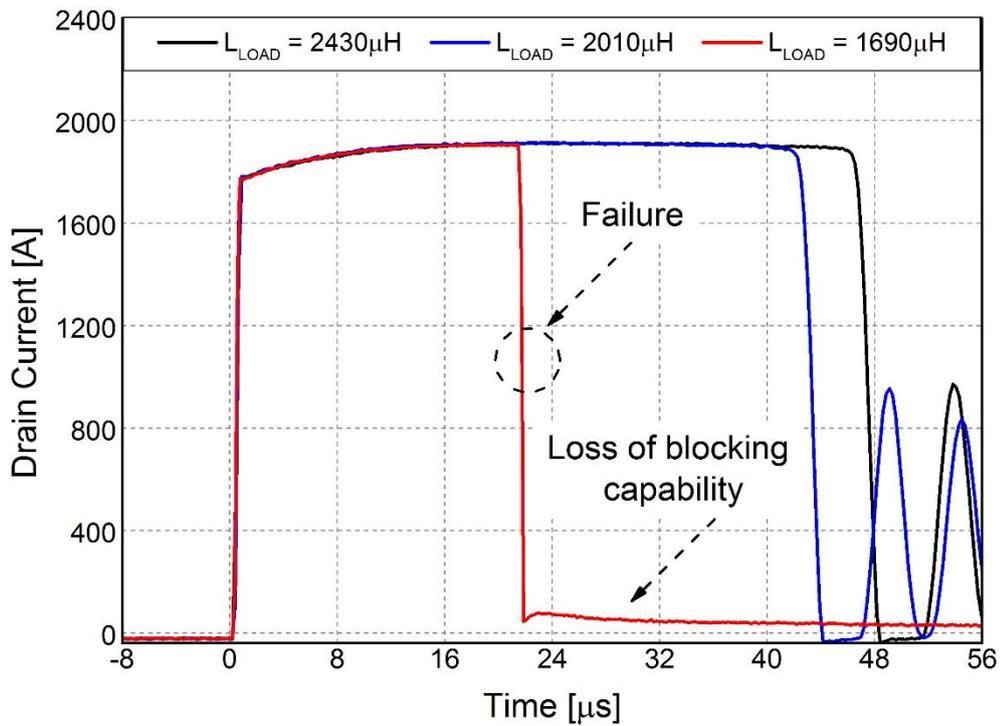
Figure 5.7: *Experimental UIS drain voltage (V_{DS}) waveforms; <u>Dev-A</u>; V_{DD} = 400 V; V_{GS} = 0 V;*

T_{CASE} = 150 °C; L_{Load} = 2430 μH, 2010 μH and 1690 μH; <u>Same E_{AV}</u>

Table 5.3: Summary of test conditions (Dev-A; Different L$_{LOAD}$)

T$_{CASE}$ (°C)	V$_{DD}$ (V)	V$_{GS}$ (V)	L$_{LOAD}$ (µH)	I$_{AV}$ (A)	E$_{AV}$ (J)
150	400	0	2430	26.5	1.12
			2010	28.7	1.11
			1690	30.5	1.08**

V$_{GS}$ Sweep

Furthermore, the third set of test results presented here investigate the dependence of avalanche breakdown robustness on gate bias voltage (V$_{GS}$) used for DUT turn-off. The results included here are at two different V$_{GS}$ (0 V and -5 V) while keeping all the other test conditions (V$_{DD}$ = 400 V, L$_{LOAD}$ = 500 µH and T$_{CASE}$ = 25 °C) unchanged. Figure 5.8 shows the I$_L$ and V$_{DS}$ waveforms at V$_{GS}$ = 0 V for safe UIS transient. For comparison, Figure 5.9 plots V$_{DS}$ and I$_L$ waveforms for both V$_{GS}$ = 0 V and -5 V at same I$_{AV}$. For V$_{GS}$ = 0 V, the DUT failed at I$_{AV}$ = 47 A. On the other hand, for V$_{GS}$ = -5 V, the DUT doesn't fail at I$_{AV}$ = 47 A which corresponds to the value at which the DUT failed when V$_{GS}$ was 0 V. For DUT tested at V$_{GS}$ = -5 V, higher I$_{AV}$ = 50 A i.e. higher E$_{AV}$ was needed before failure was observed as illustrated in Figure 5.10. Table 5.4 includes a summary of all the test conditions along with calculated E$_{AV}$ values. The results show the dependence of avalanche ruggedness on turn-off V$_{GS}$. In order to interpret these results and failure, TCAD tools are important. Therefore, the simulation results are included in section 5.2 giving insights into the proposed failure mechanism during avalanche breakdown phase.
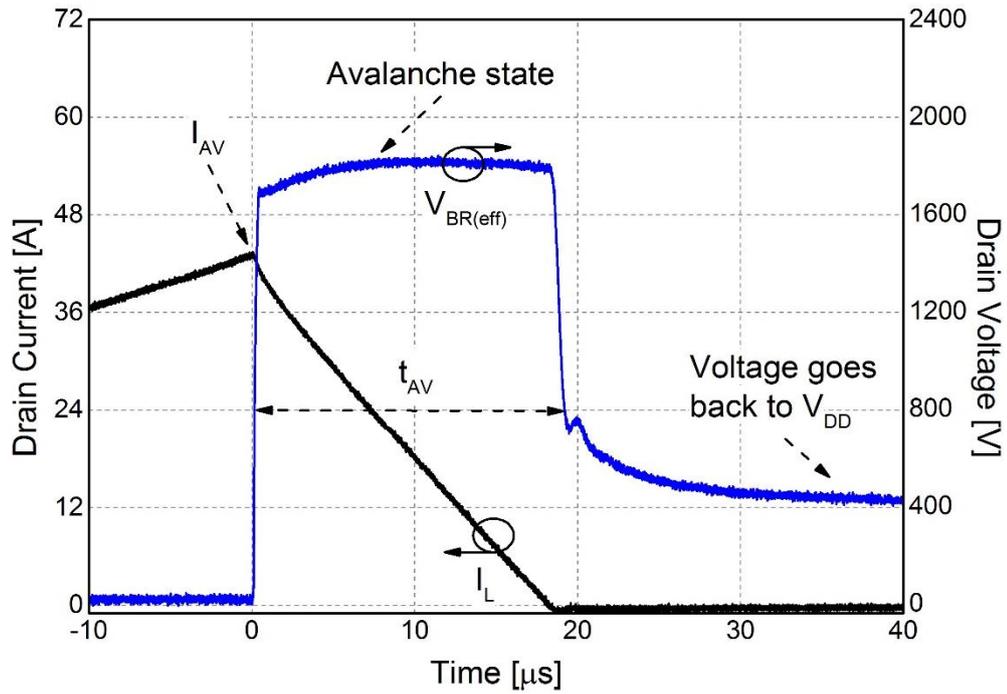
**Figure 5.8:** *Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 400 V; $V_{GS} = 0\ V$; T_{CASE} = 25 °C; L_{Load} = 500 µH; Dev-A; Safe UIS*
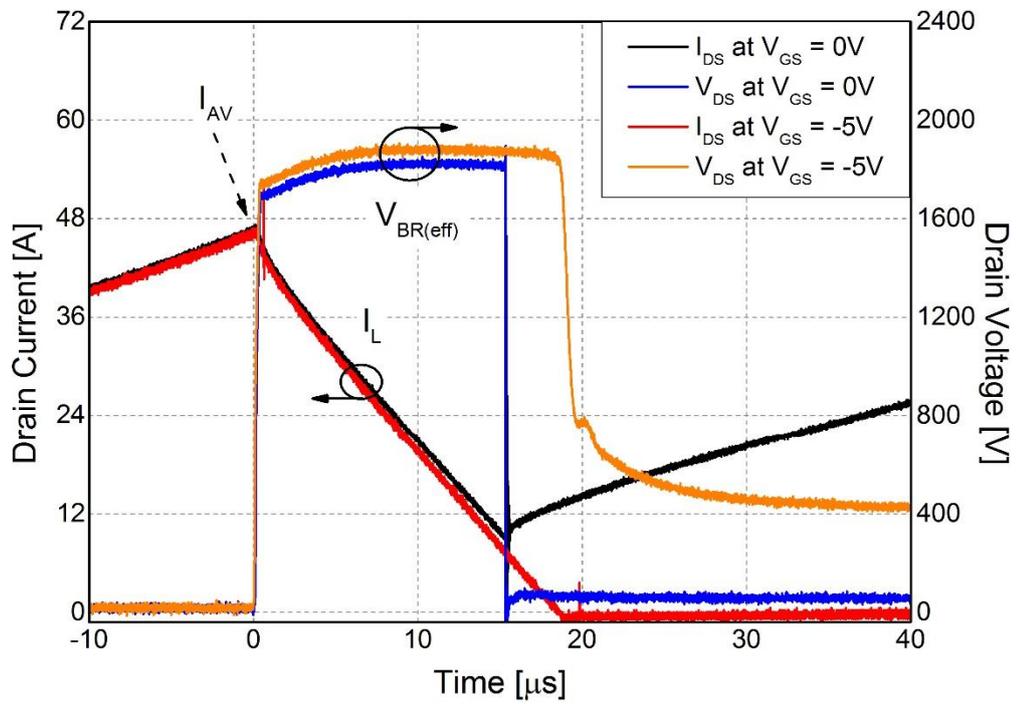
Figure 5.9: *Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 400 V; $V_{GS} = 0\ V\ and\ -5\ V$; T_{CASE} = 25 °C; L_{Load} = 500 µH; Dev-A; Comparison*
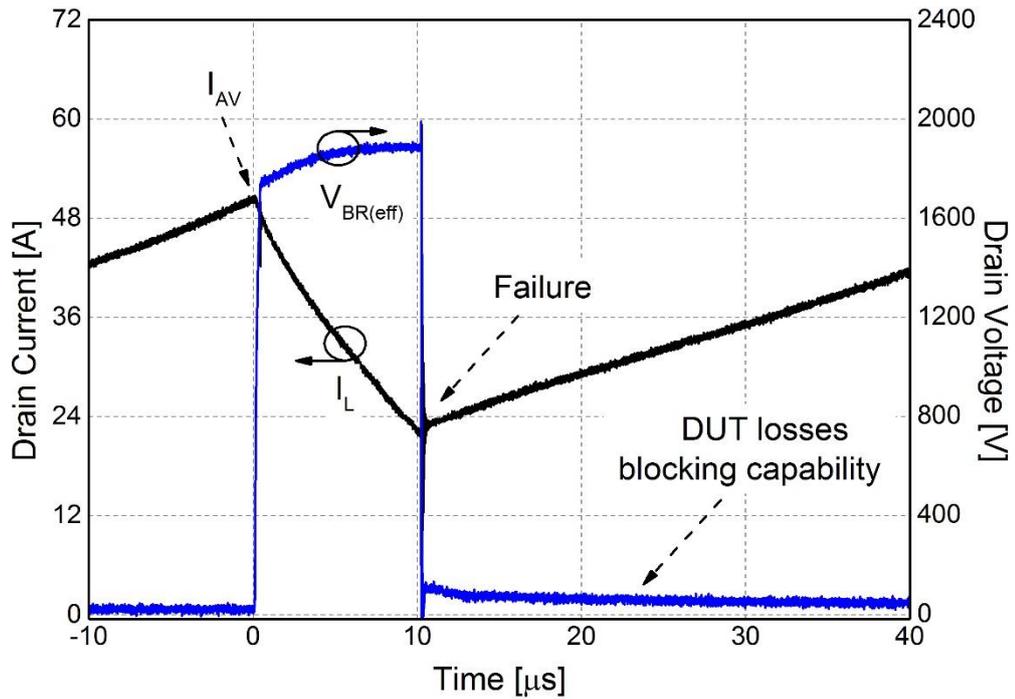
Figure 5.10: *Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} =*

400 V; $\underline{V_{GS} = -5\ V}$; T_{CASE} = 25 °C; L_{Load} = 500 µH; $\underline{Dev\text{-}A}$; $\underline{Failure\ UIS}$

Table 5.4: *Summary of test conditions ($\underline{Dev\text{-}A}$; Different V_{GS})*

T_{CASE} (°C)	V_{DD} (V)	V_{GS} (V)	L_{LOAD} (µH)	I_{AV} (A)	E_{AV} (J)
25	400	0	500	43	0.75
				47	0.84
		-5		47	0.88
				50	0.96

5.1.2. Experimental Results – Structural Characterisation

This section represents the experimental results carried out on bare dies. The tests presented

here are on Dev-A at V_{DD} = 400 V, L_{LOAD} = 4600 µH, V_{GS} = 0 V and T_{CASE} = 75 °C. Table 5.5

summarises all the test condition. Bespoke Infrared (IR) thermography, as earlier explained in

section 3.2.1 [65], was used to investigate DUT's surface temperature distribution with an aim

to observe what the device undergoes close to and/or at failure. Figure 5.11 shows V_{DS} and I_L waveforms for safe UIS transient before failure.
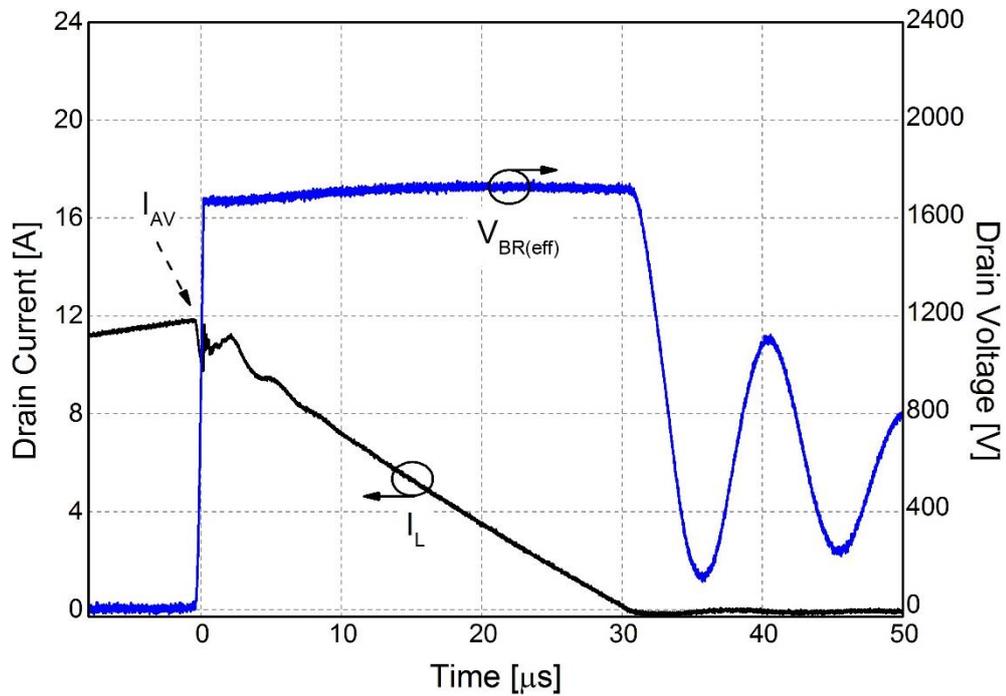
Figure 5.11: *Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 400 V; V_{GS} = 0 V; T_{CASE} = 75 °C; L_{Load} = 4600 µH; Dev-A; Before Failure*
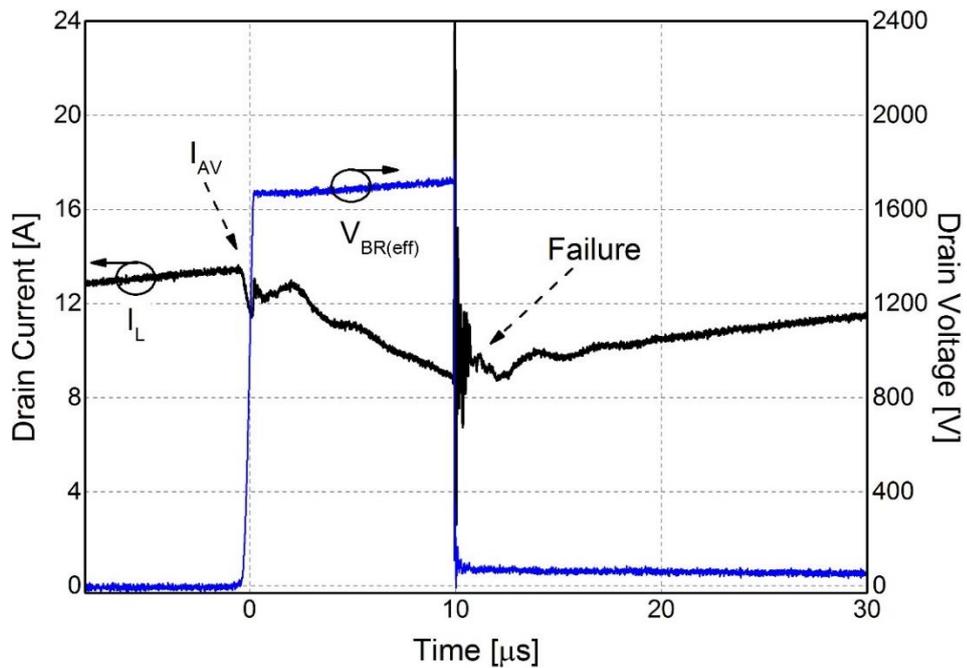
Figure 5.12: *Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 400 V; V_{GS} = 0 V; T_{CASE} = 75 °C; L_{Load} = 4600 µH; Dev-A; At Failure*

Figure 5.12 presents the V_{DS} and I_L waveforms at failure. The current is almost uniformly distributed for the safe avalanche transient as depicted in Figure 5.13 (a). The I_{AV} was increased until failure was obtained. The thermal map corresponding to failure is included in Figure 5.13 (b). An interesting observation to be made here is the phenomena of localized current crowding taking place inside the device where most of the total current is drawn by a small number of cells in a small locality within the entire active device area. Due to current crowding phenomenon, the formation of hot-spot takes place at the edge of the source pad (and the die border), eventually leading to failure. Formation of hot-spots has also been previously reported on Si devices [96]. The formation of a hot-spot is usually associated with a positive feedback mechanism involving bipolar current flow.

Table 5.5: Summary of test conditions (Dev-A)

T_{CASE} (°C)	V_{DD} (V)	V_{GS} (V)	L_{LOAD} (µH)	I_{AV} (A)
75	400	0	4600	11.9
				13.5
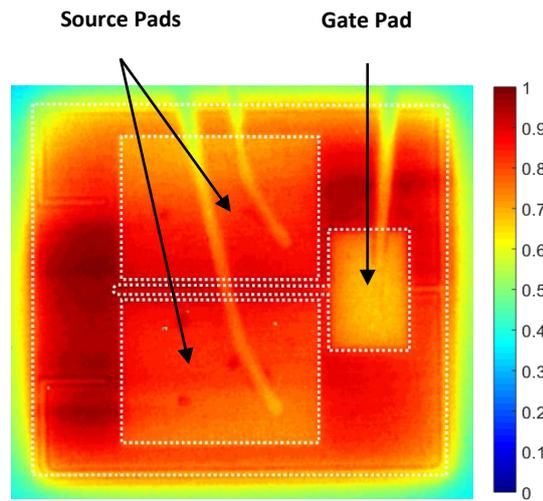
(a) – Before failure
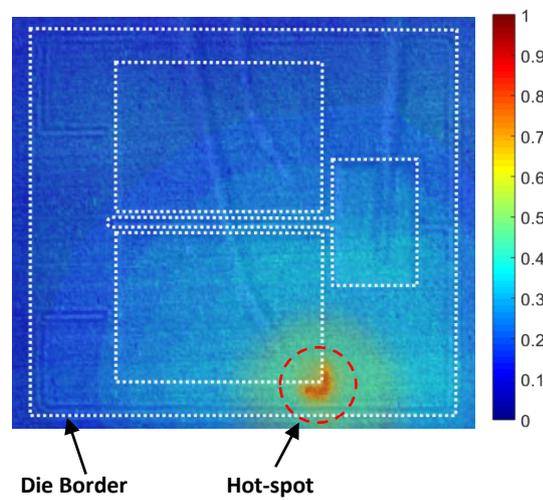
(b) – At failure

Figure 5.13: *Normalized temperature distribution; Dev-A; V_{DD} = 400 V; V_{GS} = 0 V; T_{CASE} = 75 °C*

5.1.3. Aging Test Results

Avalanche breakdown transients could be a frequent event for power devices since certain applications purposely make use of the avalanche ruggedness feature of devices. It is therefore important to assess the avalanche breakdown robustness of SiC power MOSFETs during repetitive UIS stress and therefore aging tests were performed. Here, the packaged Dev-A DUT was subjected to the repetitive dissipation of constant E_{AV} value well below the critical E_{AV} for the undertaken test conditions. The test conditions are summarised in Table 5.6. In order to monitor the changes in device characteristics, threshold voltage (V_{th}) parameter was measured at regular intervals (see Appendix C for measurement circuit schematics). This parameter shows a marked deviation from the initial value, already after few thousand pulses. A total of 669,000 pulses were sent to the device and all the measurements obtained for V_{th} differ from the previous ones which demonstrates continuous degradation taking place inside the device.

Table 5.6: *Summary of test conditions (<u>Dev-A; Aging Test</u>)*

T_{CASE} (°C)	V_{DD} (V)	V_{GS} (V)	t_{AV} (µs)	I_{AV} (A)	E_{AV} (J)
150	400	0	22	35	0.7
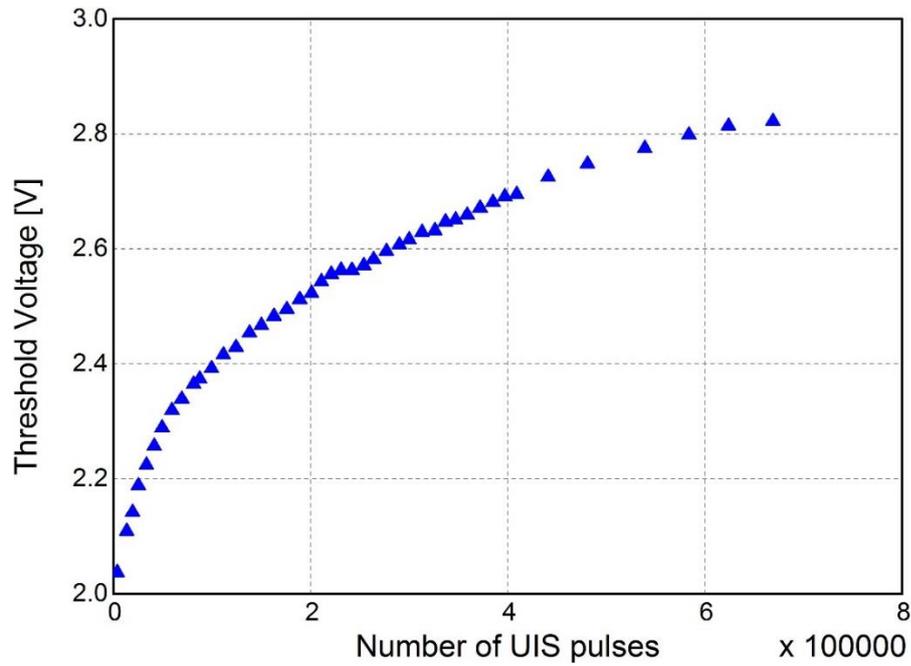
Figure 5.14: *Evolution of threshold voltage (V_{th}) due to repetitive UIS stress*

Here, V_{th} is defined as the gate-source voltage when the drain current equals to 5 mA. Figure 5.14 illustrates a positive shift in V_{th} as the UIS stress accumulated on DUT. The shift of V_{th} is usually associated to the interfacial charges (electrons for n-channel) trapped at and near the SiO_2-SiC interface which also leads to a significant degradation of the device performance due to a considerable reduction in the effective channel mobility. The V_{th} instability of SiC power MOSFETs is an ongoing area of research and previous studies show that V_{th} instability can be reduced by applying a nitric oxide (NO) or nitrous oxide (N_2O) post-oxidation anneal during the device manufacturing stage. Improvement of V_{th} stability is a major requirement in the development of technologically matured SiC power MOSFETs to allow power electronics circuitry solely based on SiC device [97-99].

5.1.4.   Experimental Results – On other DUTs

Dev-B: Experimental tests on Dev-B DUT were also performed and selective V_{DS} and I_L waveforms are included in Figure 5.15 along with the test conditions summarised in Table 5.7. The tests were performed at V_{GS} = 0 V, L_{LOAD} = 2430 µH and T_{CASE} = 75 °C while increasing V_{DD} until avalanche was achieved which resulted in the failure of the device straight away. Here, as could be seen in Figure 5.16 that the device possess no or little avalanche capability. As soon as Dev-B DUT entered avalanche breakdown, it failed due to such high breakdown voltage of the device. Even though the device's $V_{BR(DSS)}$ is 1200 V, the actual breakdown of the device is almost twice (approximately 2300 V) of the rated value. Such difference is entirely down to the device design and due to relatively lower doping of the drift layer which results in such high $V_{BR(eff)}$. Such high $V_{BR(eff)}$ implies that the maximum electric field (E_{max}) inside the structure during avalanche is extremely high which results in immediate DUT's failure.

On the other hand, Dev-B DUTs have relatively better SC performance as could be seen in Figure 4.20 in section 4. DUTs from Dev-B can sustain t_{SC} ≥ 10 µs at V_{DD} = 600 V whereas Dev-A couldn't safely sustain t_{SC} = 10 µs as illustrated in Figure 4.3. For nominal operating V_{DD} in power converters, the electric field (E) values inside the structure, in particular close to the gate oxide, would be relatively lower for Dev-B DUTs. It is believed that the manufacturer has compromised on avalanche ruggedness in order to offer better performance elsewhere e.g. better SC robustness and V_{th} stability.

***Table 5.7:** Summary of test conditions (<u>Dev-B</u>)*

V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	L_{LOAD} (µH)	E_{AV} (J)
210	75	0	2430	N/A
220				
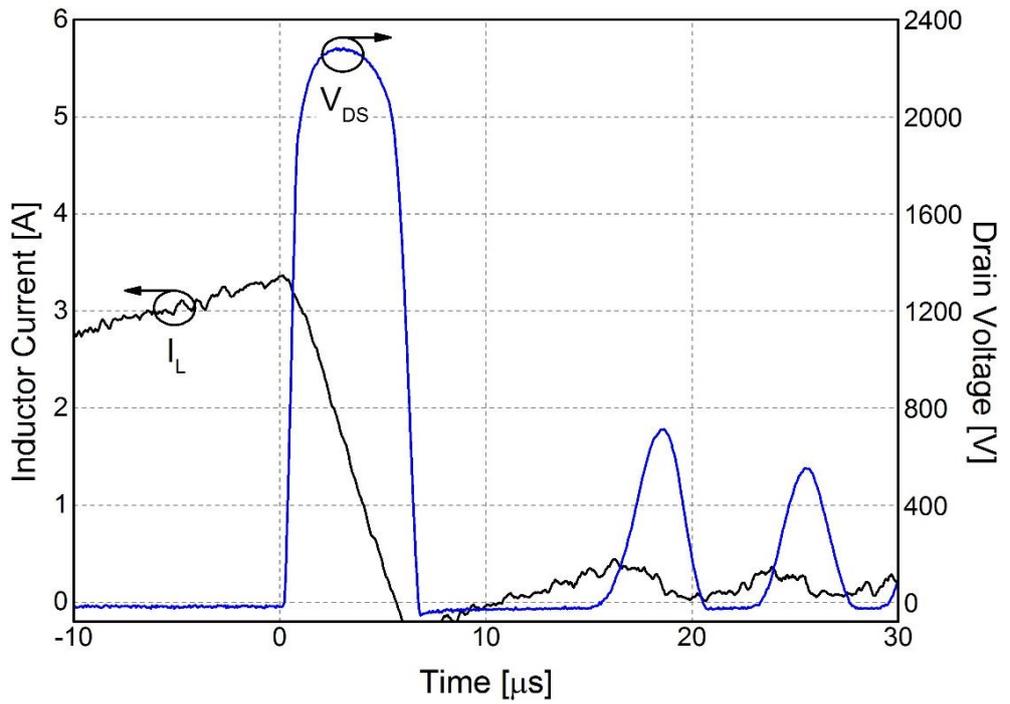
Figure 5.15: *Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 210 V; V_{GS} = 0 V; T_{CASE} = 75 °C; L_{Load} = 2430 µH; <u>Dev-B</u>; <u>Before Failure</u>*
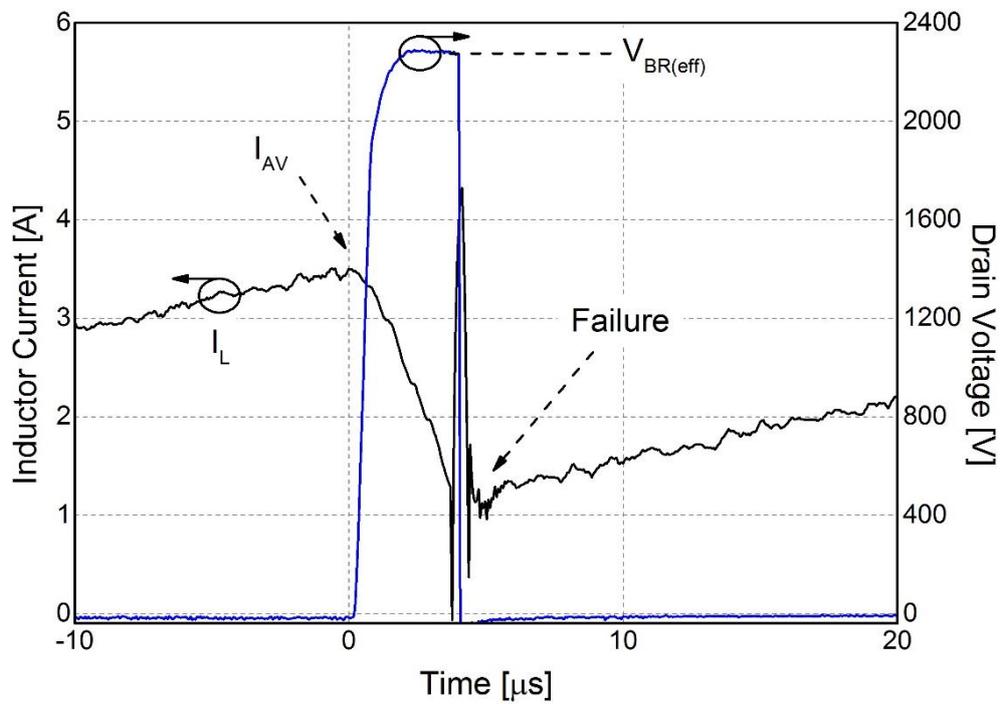

Figure 5.16: *Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 210 V; V_{GS} = 0 V; T_{CASE} = 75 °C; L_{Load} = 2430 µH; <u>Dev-B</u>; <u>At Failure</u>*

Dev-C: A few tests performed on Dev-C DUT are also presented here. Figure 5.17 shows V_{DS} and I_L waveforms before failure for test performed at V_{DD} = 400 V, V_{GS} = 0 V and T_{CASE} = 75 °C. The test conditions are included in Table 5.8. The V_{DS} and I_L waveforms at failure are included in Figure 5.18. Here, for Dev-C, it is interesting to note that the $V_{BR(eff)}$ is approximately 1400 V which is quite close to $V_{BR(DSS)}$ = 1200 V. These devices also possess avalanche ruggedness, therefore, have the ability to sustain avalanche breakdown and thus dissipate E_{AV}.

Table 5.8: Summary of test conditions (_Dev-C_)

V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	L_{LOAD} (µH)	I_{AV} (A)
400	75	0	1270	29.8
			1000	34.5
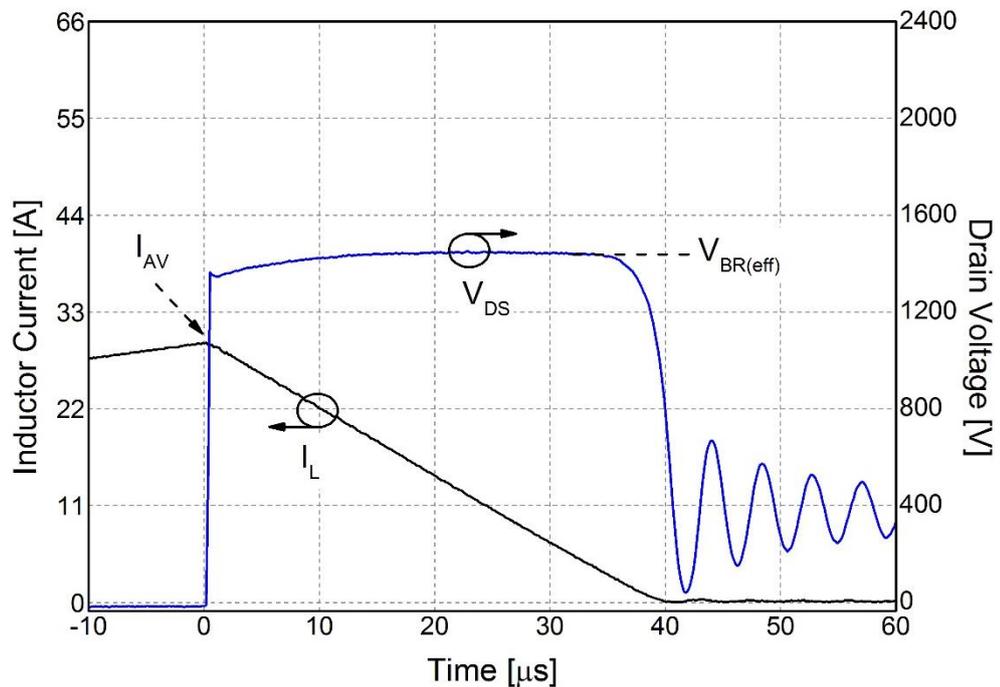
Figure 5.17: Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 400 V; V_{GS} = 0 V; T_{CASE} = 75 °C; L_{Load} = 1270 µH; _Dev-C_; _Before Failure_
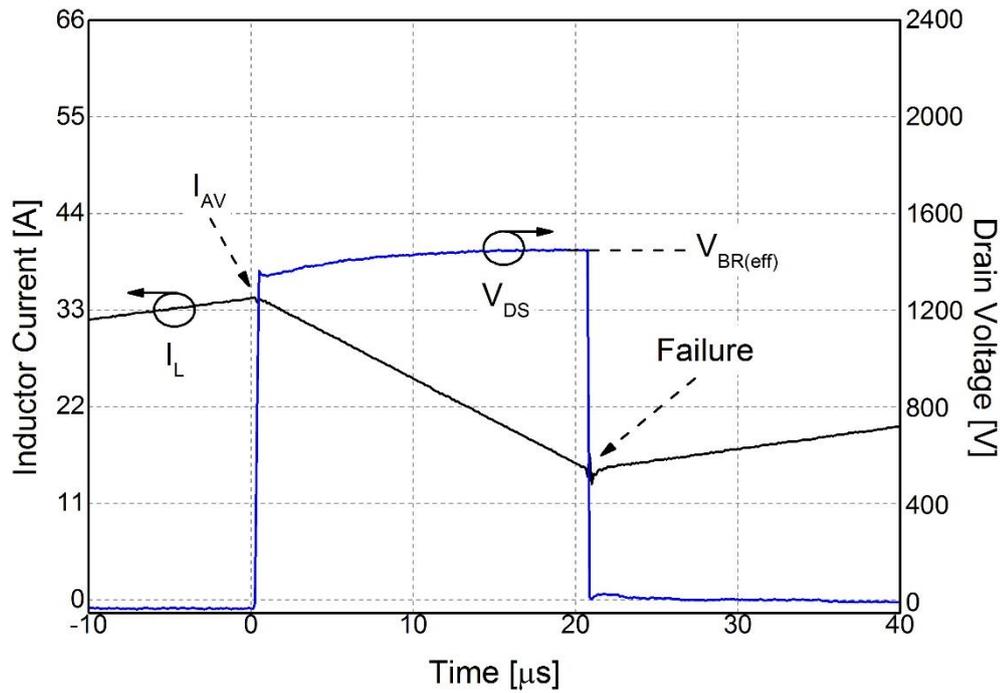
Figure 5.18: *Experimental UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 400 V; V_{GS} = 0 V; T_{CASE} = 75 °C; L_{Load} = 1000 µH; Dev-C; At Failure*

5.2. Simulation Results

The simulations were carried out at: V_{DD} = 400 V; V_{GS} = 20 V (turn-on) and 0 V (turn-off); L_{LOAD} = 500 µH and T_{CASE} = 25 °C. The simulated V_{DS} and I_L waveforms at failure are shown in Figure 5.19. In order to better understand the underlying mechanism responsible for the failure, the electron and hole current component flowing out of the N+ Source and P-Body terminals were plotted as shown in Figure 5.20. From Figure 5.20, significant electron current component flowing into the N+ Source region could be observed as the t_{AV} lapsed until failure occurred.
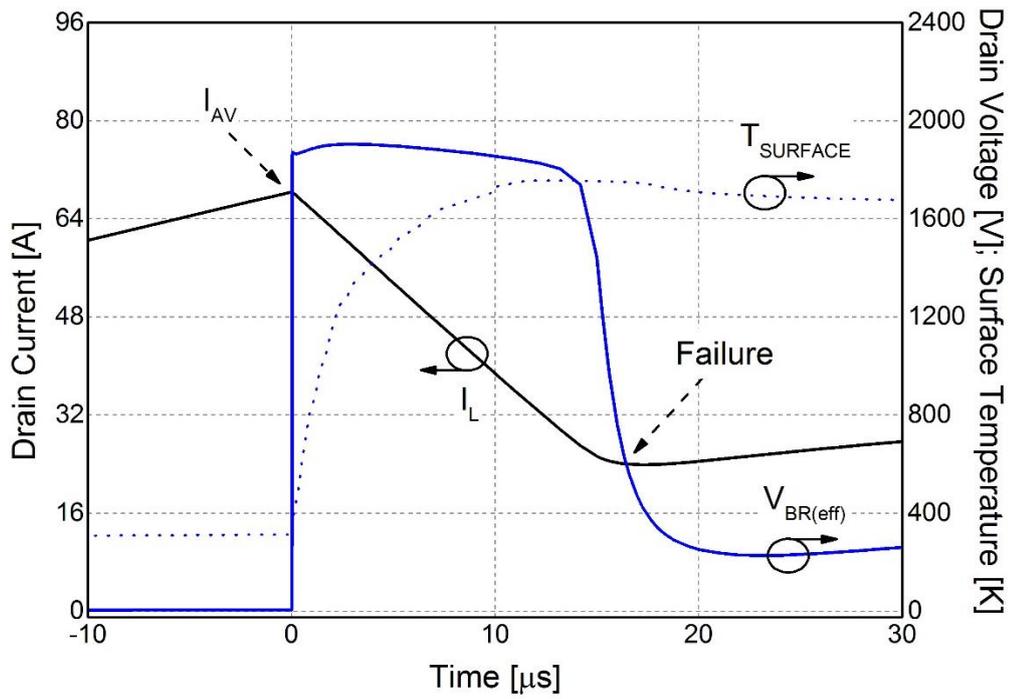
Figure 5.19: *Simulated UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 400 V; V_{GS} = 20 V (turn-on) and 0 V (turn-off); T_{CASE} = 25 °C; L_{Load} = 500 µH; At Failure*
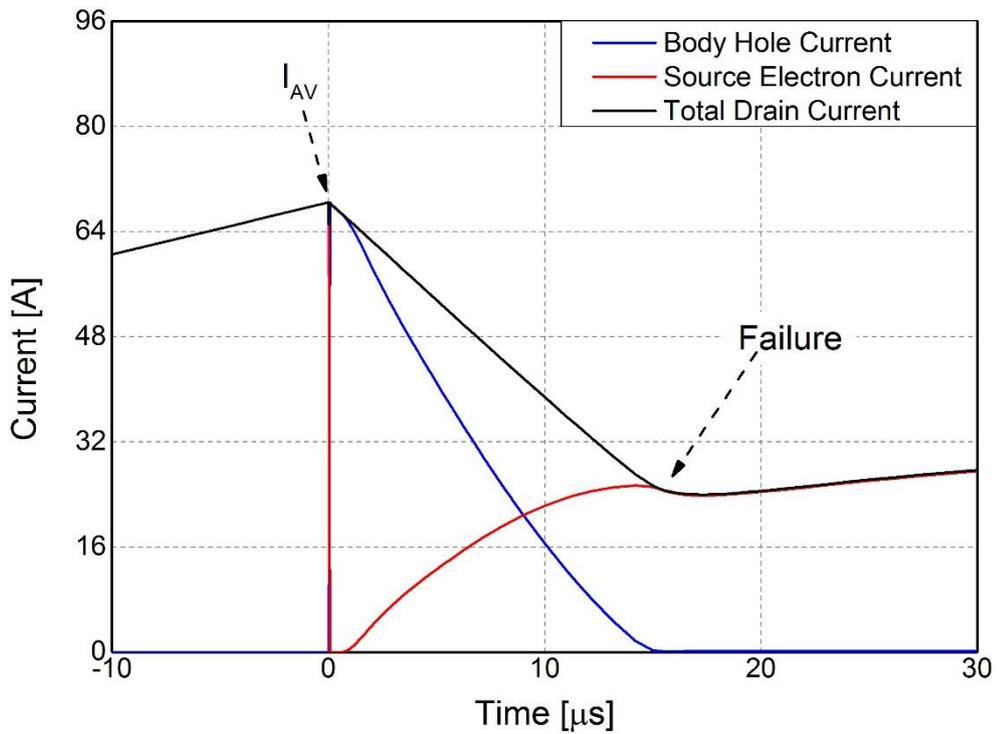
Figure 5.20: *Hole and electron current components along with total current at failure*

The total current density within the cell structure was also plotted at different time instances. The current distribution within the complete cell during t_{ON} when the DUT's channel is conducting is shown in Figure 5.21. Figure 5.22 presents the total current density within the entire cell structure immediately after the device enters avalanche breakdown. As expected, during avalanche breakdown, the maximum impact ionization takes place at the curvature of the P-Body / N-Drift *pn* junction, where the electric field reaches the highest value. As a result of this, the current density during avalanche breakdown usually flows through the corner of the P-Body / N-Drift region (i.e. DUT's body diode) of the MOSFET.

N+ Source   **N+ Source**

P-Body

Depletion Region

N-Drift

Abs(TotalCurrentDensity-V) (A*cm^-2)

3.895e+06
4.557e+04
5.333e+02
6.241e+00
7.303e-02
8.546e-04
1.000e-05

N+ Drain
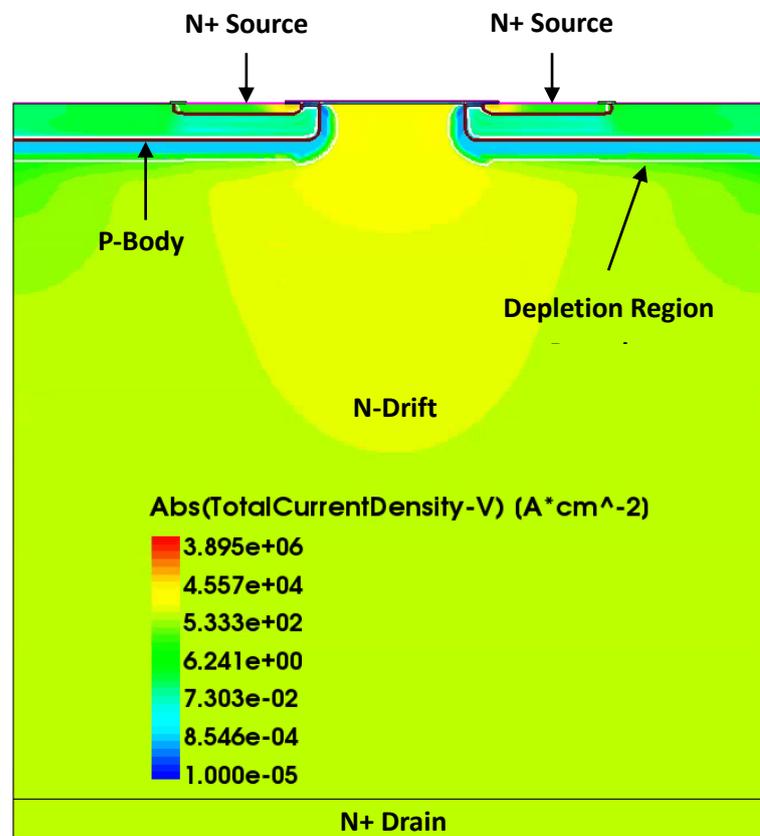
Figure 5.21: *Total current distribution during ON state before device enters avalanche*
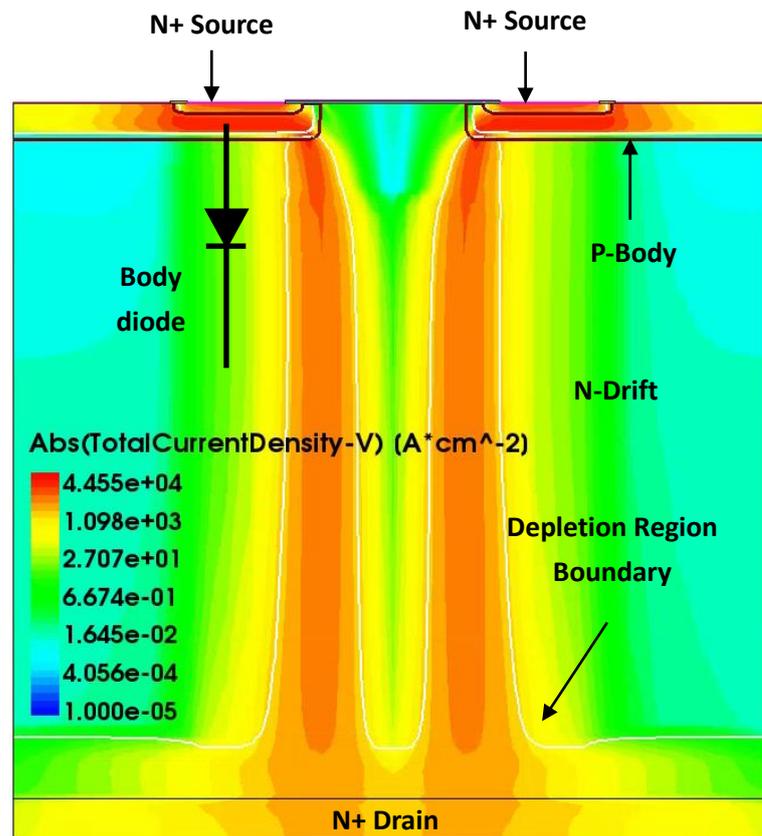
breakdown

Figure 5.22: Total current distribution immediately after device enters avalanche breakdown state

A zoom-in of the current distribution near the corner of the *pn* region during avalanche breakdown up until failure at four different t_{AV} instances of increasing order from (1) to (4) is also presented in Figure 5.23. A progressive shift of current from reverse diode towards channel is observed. During the first phase of breakdown phenomena, Figure 5.23(1), current mainly flows through the corner of the P-Body / N-Drift region corresponding to the location where highest electric field density and maximum impact ionization occurs inside the cell. However, as the lattice temperature (T) increases during t_{AV}, the current partially also starts to flow in and below the channel region, Figure 5.23(2) and (3), aided by the reduction of V_{th} due to consistent temperature increase near P-Body leading to channel activation. At failure, Figure 5.23(4), only electron current flows in and below the channel region. The cell temperature was simulated to be well above 1000 K at failure. T_J due to really high power

density in such a small device (die size: 3.10 x 3.36 mm) during such short UIS transients could easily rise significantly to really high values well above 1000 K.
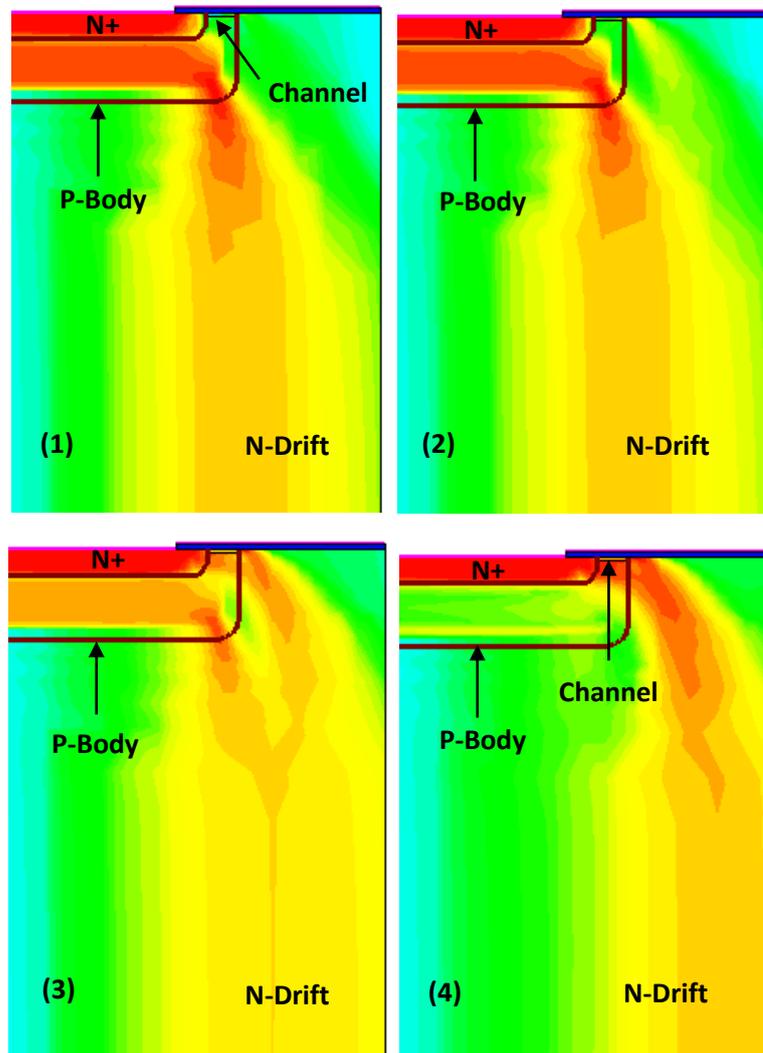
Figure 5.23: *Current distribution during avalanche breakdown and failure; Zoomed in; (1) to (4) with increasing t_{AV}*

Mixed-mode simulation results for V_{GS} = 20 V (turn-on) and -5 V (turn-off) at failure while keeping all the other test conditions constant are included in Figure 5.24. Here, slightly higher I_{AV} was required before failure was obtained. Simulations have shown that by using a negative V_{GS} to keep the device turned-off helps to better close the channel. Therefore, it takes longer (i.e. higher temperature) before the onset of source electron current flowing in and underneath the channel. Hence, channel activation is slightly delayed when negative V_{GS} is

applied allowing the device to sustain a slightly higher I_{AV} and E_{AV} before encountering failure. Effect of temperature on V_{th} has also been investigated experimentally in [100] which also partially supports the presented interpretation of V_{th} lowering which results in current flow in and underneath channel at failure as the T_J of DUT increases. Furthermore, choosing a lower T_{CASE} will result in higher power dissipation i.e. higher I_{AV} before the device failure takes place since longer time would be required to reach the critical lattice temperature responsible for the failure. Lastly, all the test conditions at which the simulations were performed are also summarised in Table 5.9.

Table 5.9: *Summary of simulation test conditions*

V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	L_{LOAD} (µH)
400	25	20V / 0V	500
400		20V / -5V	
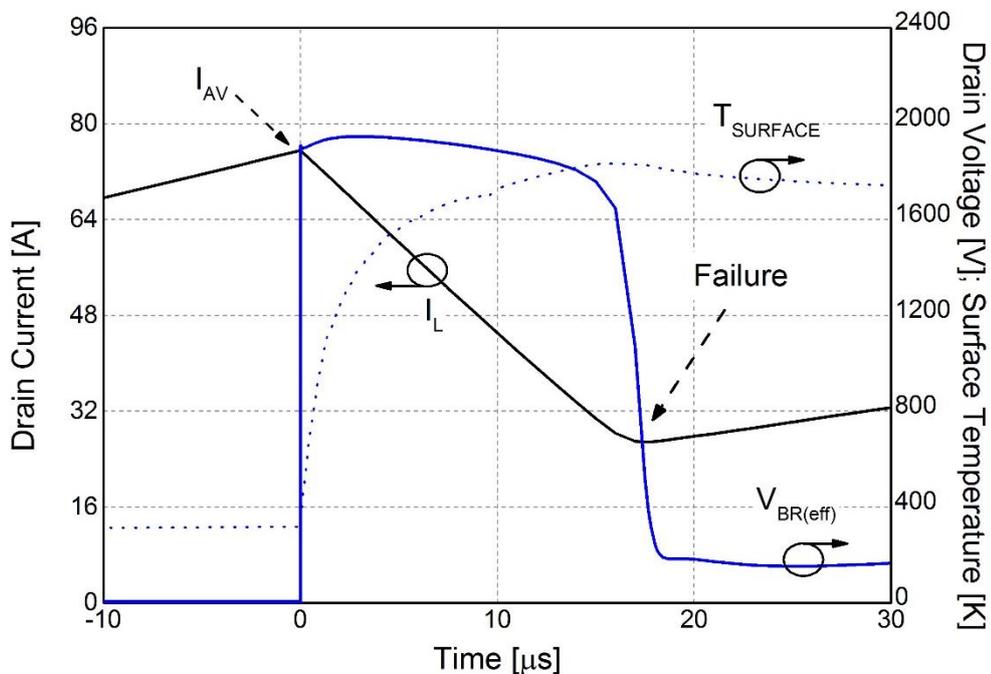
**Figure 5.24:** *Simulated UIS drain voltage (V_{DS}) and inductor current (I_L) waveforms; V_{DD} = 400 V; V_{GS} = 20 V (turn-on) and -5 V (turn-off); T_{CASE} = 25 °C; L_{Load} = 500 µH; <u>At Failure</u>*

5.3. Discussion

The overall aim of this chapter was to present a series of experimental results in order to extensively characterise SiC power MOSFETs as well as identify device limitations under UIS conditions at various different test conditions. In order to achieve this, functional and structural characterisation was performed followed by TCAD simulations in order to interpret experimental results as well as understand the corresponding underlying physical mechanisms responsible for failure when subjected to UIS condition. Tests have been presented here on three different device types of similar ratings from different manufacturers. Out of the three devices tested, Dev-A and Dev-C possess avalanche ruggedness while Dev-B lacks the ability to dissipate energy during avalanche. Also, it is apparent that Dev-A DUTs can dissipate E_{AV} up to around 1J depending on test conditions. From the experimental and simulation results presented above, following statements about avalanche breakdown robustness of SiC power MOSFETs could be said:

➢ Dependence on T_{CASE}. Higher T_{CASE} decreases critical I_{AV} value and E_{AV} dissipation at failure. As T_{CASE} is increased, the margin required to reach critical T_J during avalanche breakdown phase for failure shrinks as also supported by Figure 5.3 and 5.5.

➢ Dependence on L_{LOAD}. Decreasing L_{LOAD} worsens E_{AV} capability. As L_{LOAD} is decreased while keeping E_{AV} approximately constant, I_{AV} becomes higher and t_{AV} shrinks which results in faster T_J rise during avalanche breakdown. Therefore, E_{AV} capability can be improved for larger L_{LOAD} values i.e. E_{AV} dissipation rate has an effect on avalanche robustness of SiC devices as also demonstrated in Figure 5.6.

➢ Dependence on V_{GS}. Lower turn-off V_{GS} results in higher E_{AV} dissipation. Using a negative V_{GS} to turn-off the devices slightly improves the avalanche robustness of SiC devices allowing relatively higher I_{AV} and E_{AV} before encountering failure as also shown in Figure 5.8 – 5.10, 5.19 and 5.24.

- The failure mechanism is linked to the lowering of V_{th} due to really high T_J increase because of really high power dissipation within such short durations during avalanche breakdown. As a result of this, a progressive shift of current density from the body diode to the channel region (flowing into the source) was observed which eventually led to failure. After failure, all the current density was flowing in and underneath the channel as also shown in Figure 5.20 and 5.23.

- During the aging test, the DUT degraded when subjected to repetitive UIS pulses as interpreted by an increase in V_{th}, as also illustrated in Figure 5.14. V_{th} instability in SiC power MOSFETs is an ongoing area of research which is plagued by poor SiC/SiO$_2$ interface and high density of interface traps (D_{it}).
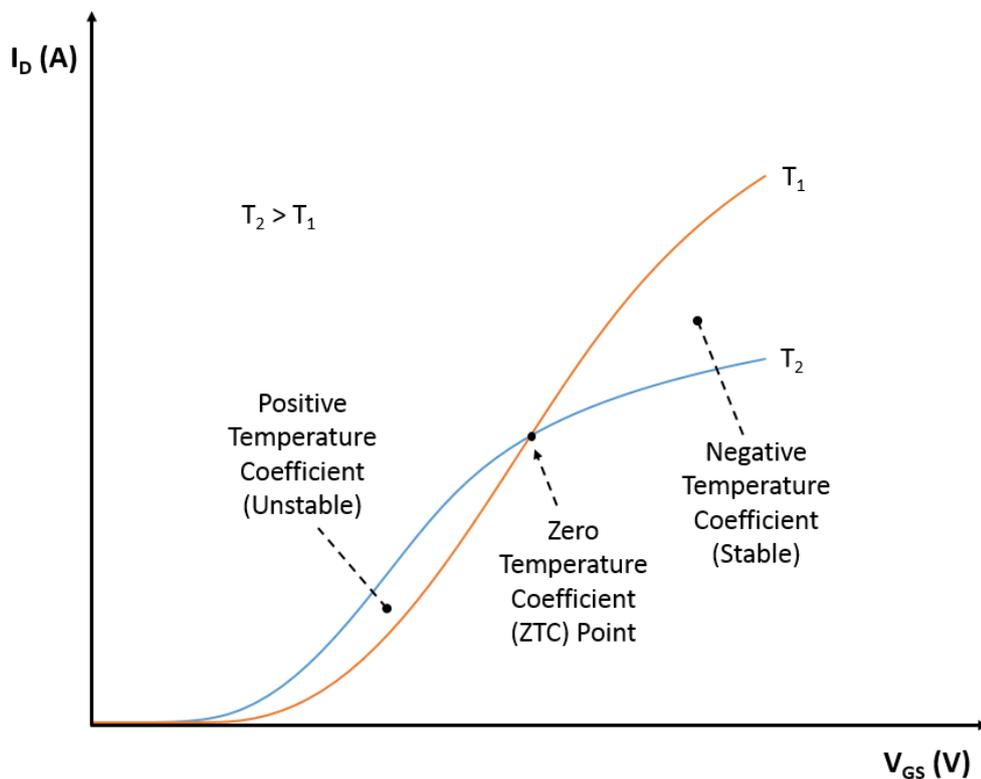
Figure 5.25: *Representation of the drain current temperature coefficient (α_T) and electro-thermal stability in terms of the transfer characteristics*
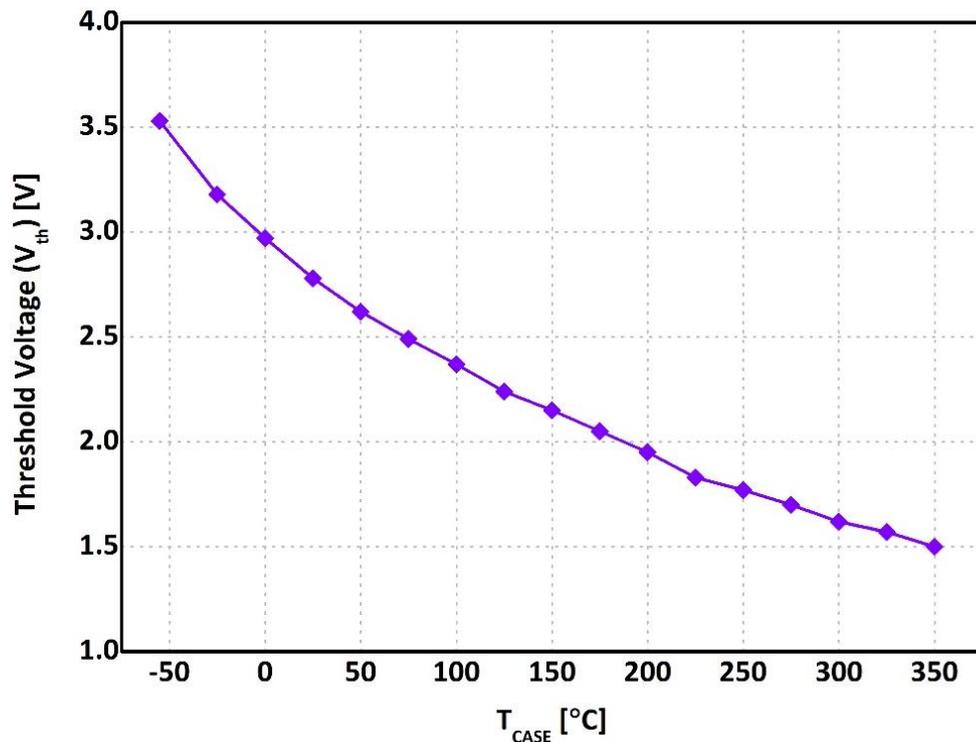
Figure 5.26: *Threshold Voltage versus T$_{CASE}$*

Finally, to conclude this chapter, the failure mechanism of SiC power MOSFETs during avalanche breakdown is discussed here. As briefly mentioned earlier, the failure mechanism is linked to the lowering of V$_{th}$ due to really high T$_J$ increase during avalanche breakdown. Unlike Si, SiC Power MOSFETs have a large range of operating V$_{GS}$ values (up until the zero temperature coefficient (ZTC) point) under which it exhibits an unstable electro-thermal behaviour. Figure 5.25 shows the typical transfer characteristics of SiC power MOSFETs as well as also illustrating the unstable electro-thermal operating region. The electro-thermal stability is determined by the drain current temperature coefficient (α_T). For the SiC power MOSFET to be electro-thermally stable, it should be operated above the ZTC point where α_T is positive. This instability can result in the formation of hot-spot leading to destructive failure as experimentally shown in [41]. Since during avalanche, the device is in the off-state therefore, it is in a highly unstable electro-thermal operating region which also explains the formation of hot-spot presented in Figure 5.13. During such unstable operation, the temperature distribution (i.e. current distribution) within the device could easily become non-uniform

resulting in a higher temperature in a small locality than the rest of the device. As a result of that, the cells which become hotter in principal should carry more current (i.e. due to V_{th} decrease and an increase of mobility). This process keeps on going until the temperature in those small number of cells becomes critical eventually leading to the hot-spot formation and going into thermal runaway. Moreover, experimental measurement for V_{th} versus temperature has been included in Figure 5.26 which clearly demonstrate its significant decrease as the temperature is increased which is also helpful to understand the flow of current in and around channel as observed in simulations.

6. Body diode Reliability

6.1. Experimental Testing and Results

This section represents all the experimental results on packaged devices in relation to the body diode reliability characterisation within an inverter operation stress and static stress regime. The test results presented in chapter 6 are on two different DUTs from different manufacturers. Some of the important parameters of these devices are summarised in Table 6.1.

Table 6.1: Summary of relevant device parameters

DUT	$V_{DS(max)}$ (V)	$R_{DS(on)}$ @ 25 °C (mΩ)	I_D @ 100 °C (A)	V_F @ I_F = 10A (V)	Package
Dev-A [91]	1200	80	24	3.3	TO-247
Dev-B [92]			28	4.6	

T_{CASE} Dependence

The dependence of case temperature (T_{CASE}) and the applied gate-source voltage (V_{GS}) to turn-off the device plays a crucial role in the performance of the SiC body diode which is essentially a PiN diode. The body diode forward voltage drop (V_F) decreases with an increase in case temperature (T_{CASE}) since the diode current (I_F) has temperature dependence. In other words, for a given V_F, I_F increases with an increase in T_{CASE}. The I_F versus V_F characteristics at different T_{CASE} for Dev-A and Dev-B are presented in Figure 6.1 and 6.2 respectively. These characteristics were measured experimentally over five different T_{CASE} = 50 °C, 75 °C, 100 °C, 125 °C and 150 °C with V_{GS} = -5 V using a Tektronix 371A curve tracer. The apparent shift of I_F versus V_F curve to the left as T_{CASE} is increased clearly demonstrates the dependence on T_{CASE}.
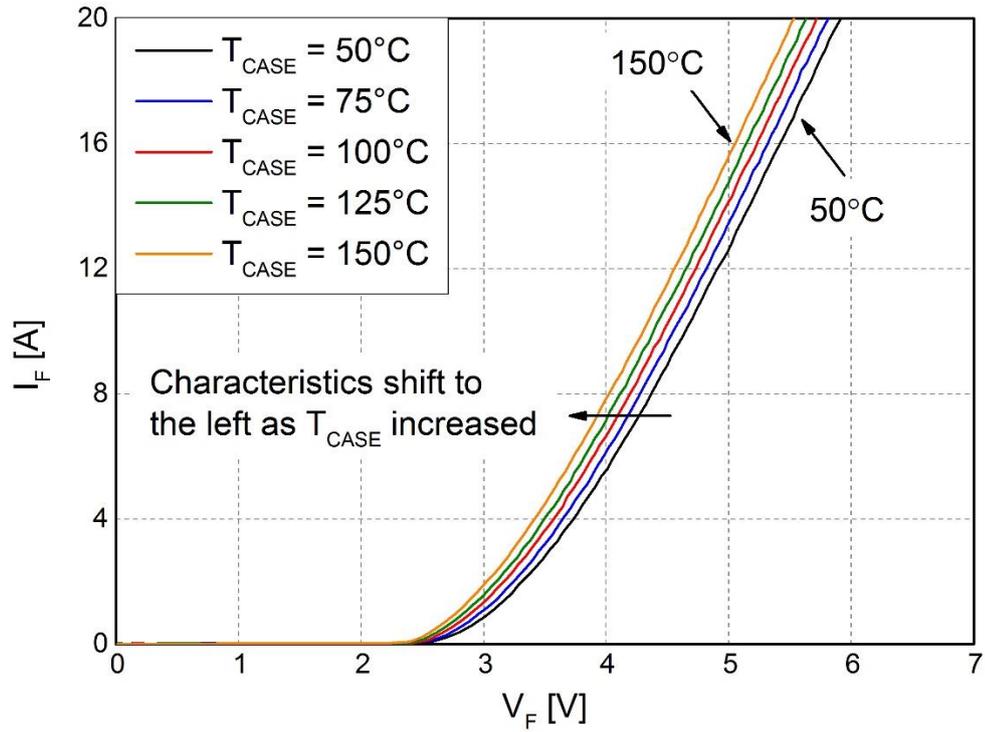
Figure 6.1: *Illustration of T_{CASE} dependence on I_F versus V_F characteristics; <u>Dev-A</u>*
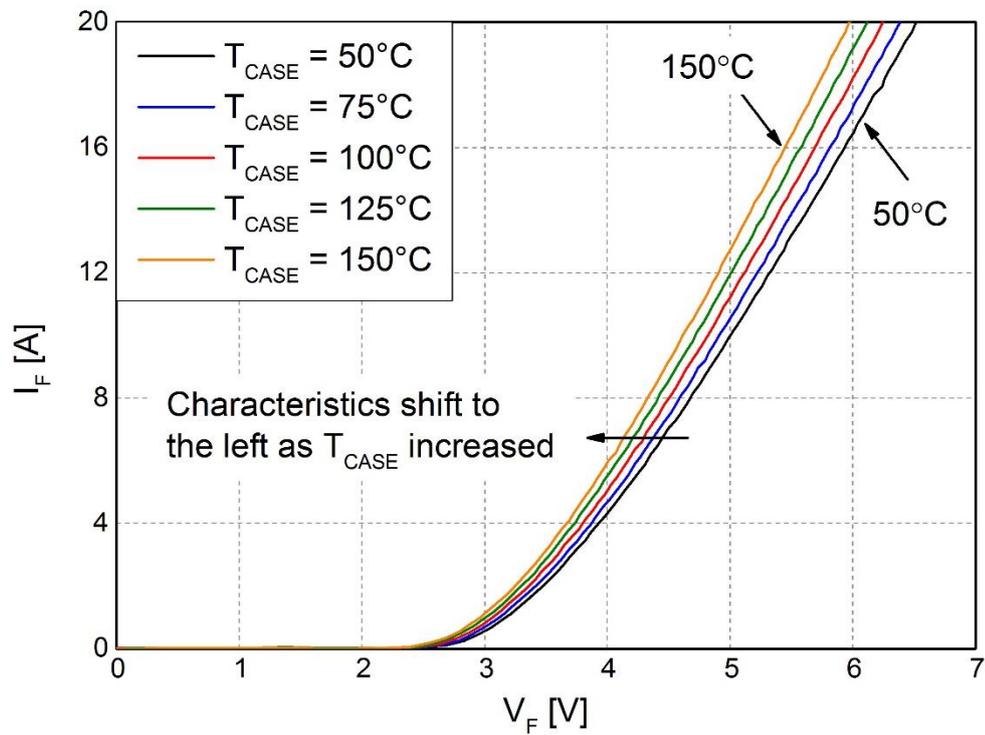
Figure 6.2: *Illustration of T_{CASE} dependence on I_F versus V_F characteristics; <u>Dev-B</u>*

V_{GS} Dependence

Moreover, SiC body diode performance was found to be dependent on the applied V_{GS} to turn-off the MOSFET channel. If V_{GS} = 0 V is used to turn-off the MOSFET channel, the diode current (I_F) flowing through the P-Body still flows over the channel region. Therefore, it is required to apply a negative V_{GS} voltage to ensure that no current flows over the channel region during the diode conduction. The reason primarily is the fact that SiC/SiO$_2$ interface is highly plagued with interface traps as also discussed earlier in section 2. As a result of this, the I_F/V_F characteristics would shift due to the degradation of the interface which is not desirable. The V_{GS} of around -4 V / -5 V is required to ensure channel is completely turned-off and no diode current flows over it.

The I_F versus V_F characteristics of Dev-A and Dev-B DUTs at five different V_{GS} voltages are presented in Figure 6.3 and 6.4 respectively. These characteristics were measured experimentally over five different V_{GS} = 0 V, -2 V, -4 V, -6 V and -8 V with T_{CASE} = 100 °C. The apparent shift of I_F/V_F characteristics to the right as more and more negative V_{GS} is used clearly demonstrates the flow of current over the channel. However, it is also clear that after V_{GS} = -4 V, no apparent change in the characteristics could be observed. Therefore, V_{GS} = -5 V was chosen to be the breakoff value after which, even a higher negative V_{GS} didn't have any further effect on I_F/V_F characteristics.

The measurements during stress analysis presented later on in this section were also carried out with V_{GS} = -5 V. This was necessary to distinguish that the shift of I_F/V_F characteristics observed during the device stress regimes (inverter and static stress) if any is entirely due to the degradation of the body diode feature and is not due to the degradation of the SiC/SiO$_2$ interface.
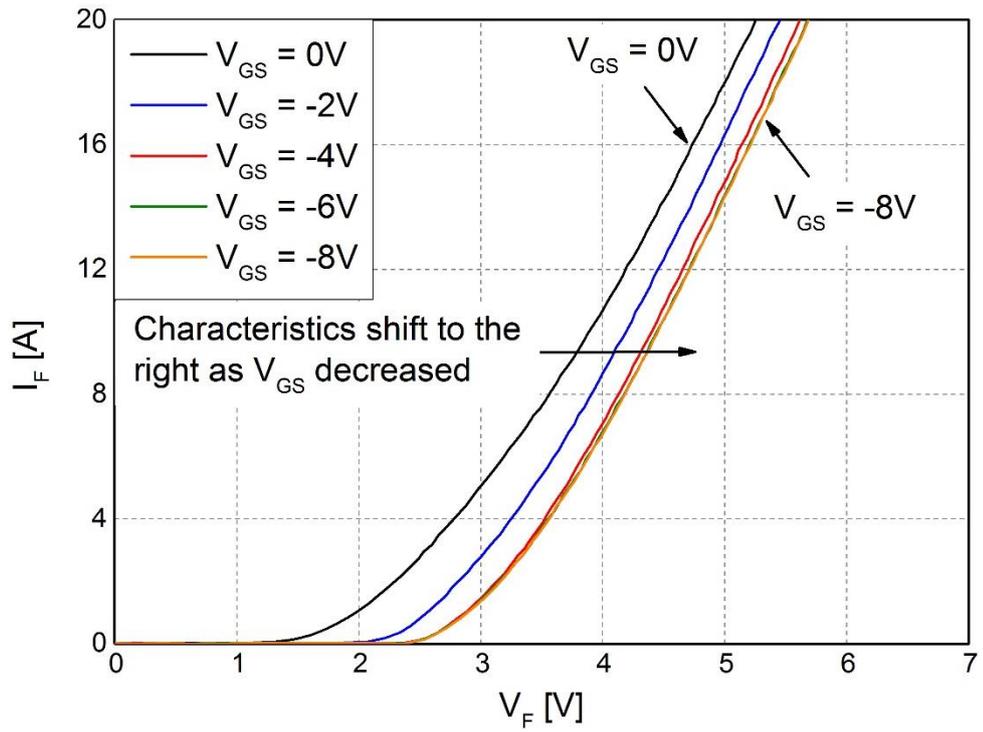
Figure 6.3: *Illustration of V_GS dependence on I_F versus V_F characteristics; Dev-A*
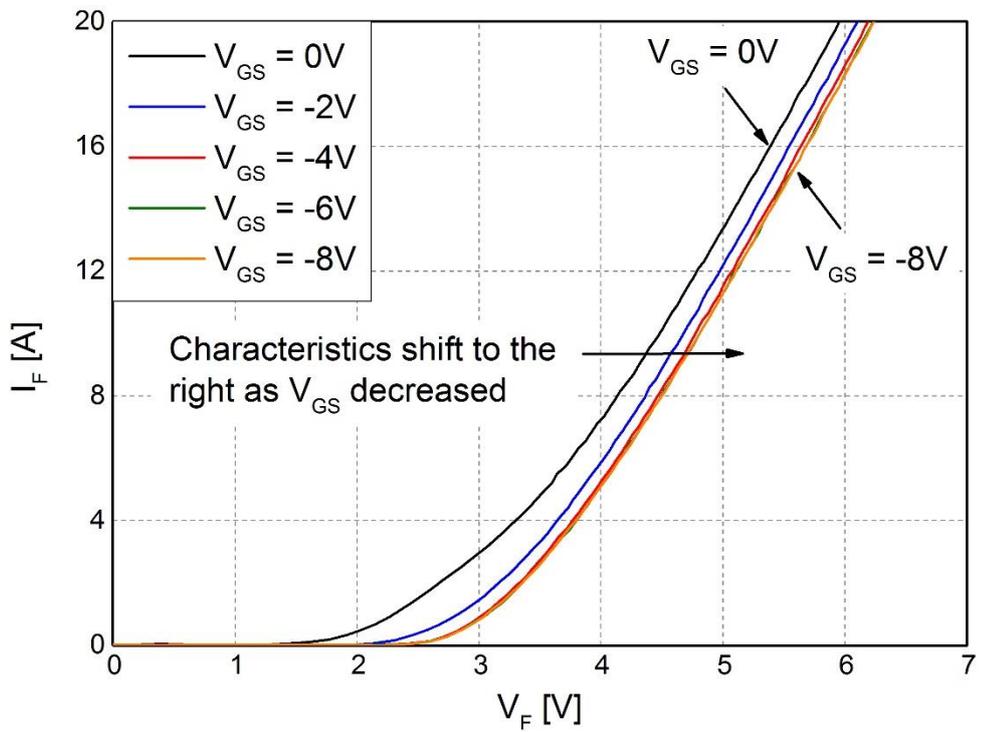
Figure 6.4: *Illustration of V_GS dependence on I_F versus V_F characteristics; Dev-A*

Inverter Stress

For stressing the DUTs during an inverter operation, the V_{DD} was chosen to be equal to 600 V (half of the rated nominal blocking voltage $V_{DS(max)}$). The V_{GS} was set to +20 V and -5 V. The inverter peak input current $I_{PH(pk)}$ was chosen to be app. 21 A (close to the rated continuous current at T_{CASE} = 100 °C). The PWM signals were generated using carrier signal frequency (f_{SW}) of 10 kHz and modulating signal frequency of 50 Hz. The amplitude of both these signals was selected to obtain a modulation index (M) of 0.6. The dead time between the top and bottom switch to avoid shoot-through was selected to be 400 ns as illustrated in Figure 6.5. The sinusoidal three-phase output current of the inverter having 50 Hz frequency has been included in Figure 6.6. The summary of all the test conditions is included in Table 6.2.

Table 6.2: Summary of test conditions (Inverter stress)

V_{DD} (V)	T_{CASE} (°C)	V_{GS} (V)	t_d (ns)	$I_{PH(pk)}$ (A)	f_{SW} (kHz)	M
600	100	+20/-5	400	21	10	0.6
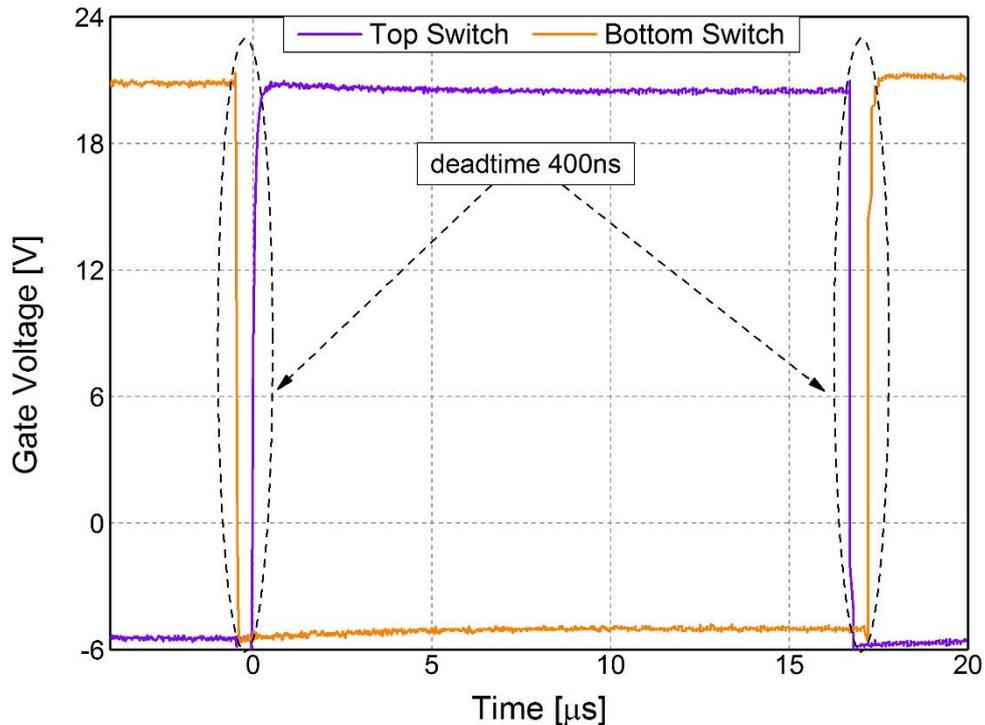
Figure 6.5: Gate signal waveforms for top and bottom switch – (S1 and S2)
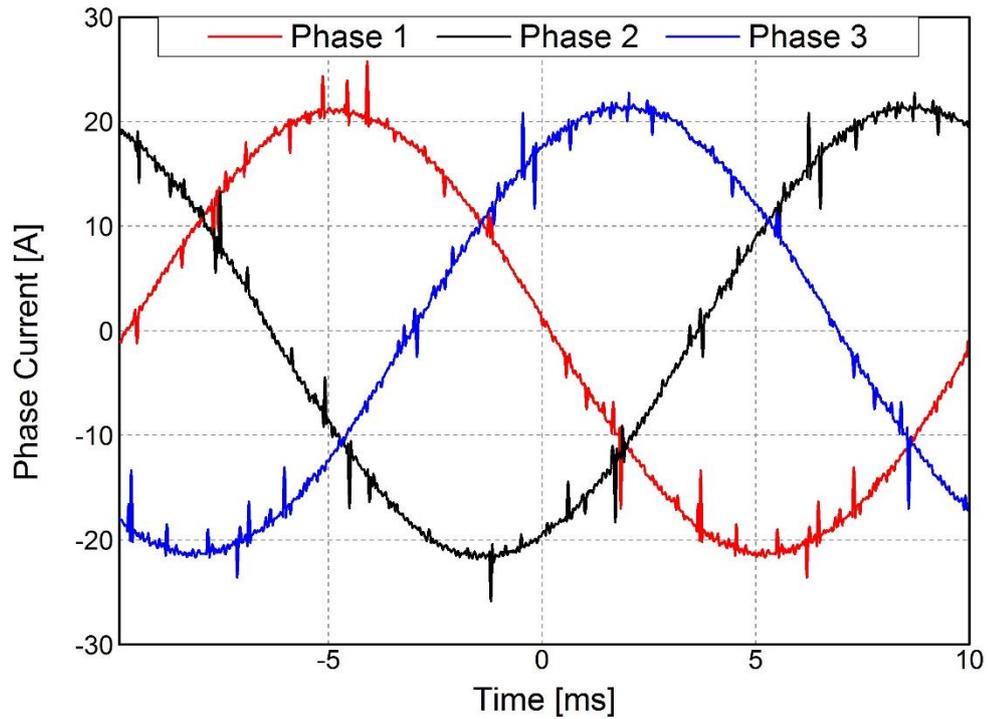
Figure 6.6: *Three-phase inverter sinusoidal output current at 50 Hz*

Evolution of body diode forward voltage (V_F) and drain leakage current (I_{LEAK}) of Dev-A DUTs have been plotted in Figure 6.7 and 6.8 respectively. The definition of V_F and I_{LEAK} measurements are included in Appendix C. Overall, it has been observed that V_F increases slightly by about 0.03 V for all the six DUTs as the stress accumulated on the devices within the 1000 hours. Moreover, I_{LEAK} showed a slight increase of around 0.2 nA for five out of six DUTs tested towards the end, however, no massive shift in this parameter was observed during the inverter operation stress testing during the 1000 hours. Similar tests were also performed on Dev-B DUTs where no change was observed for these parameters indicating no degradation of the body diode feature. Moreover, Dev-A DUTs have also shown great body diode performance and manifested no substantial degradation of the features during the 1000 hours of stress.
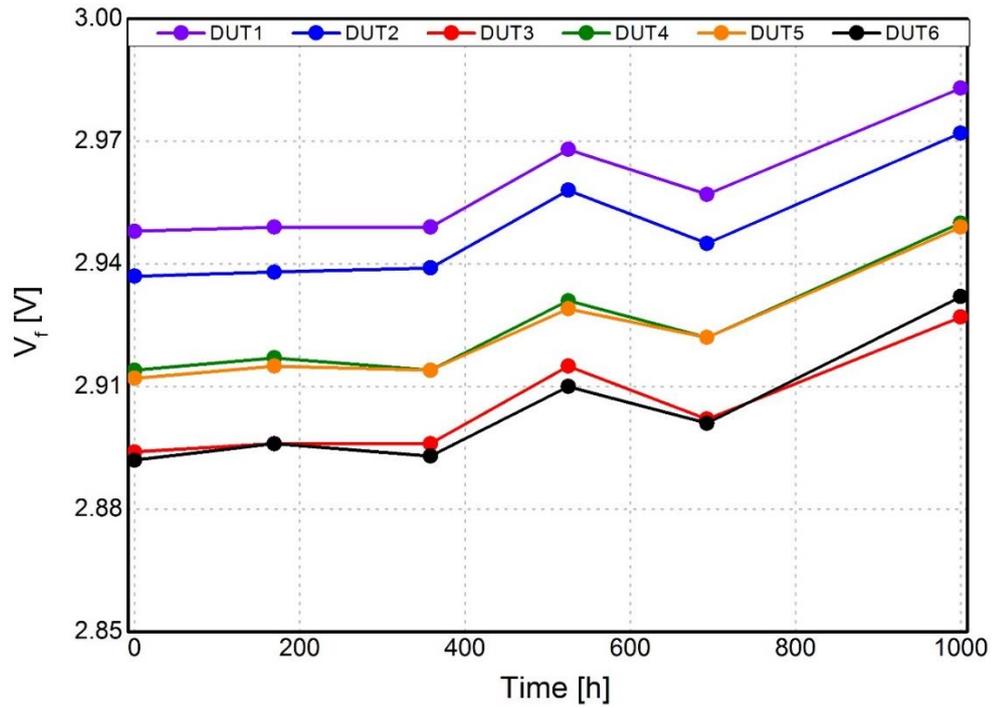
Figure 6.7: *Evolution of body diode forward voltage drop (V_F) within inverter stress;* <u>*Dev-A*</u>
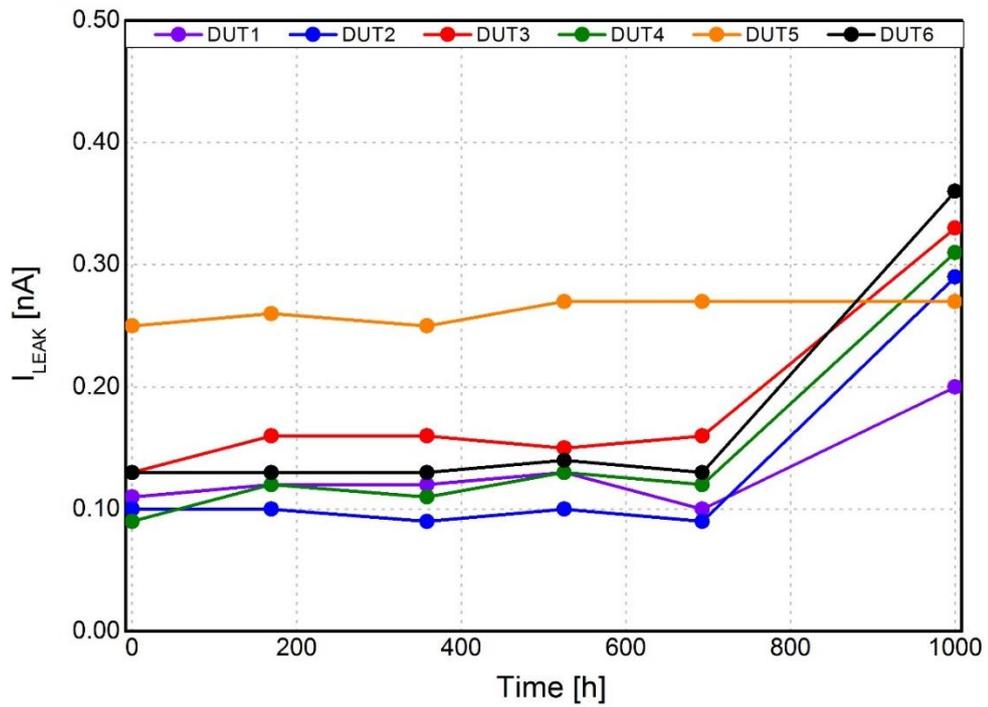
Figure 6.8: *Evolution of drain leakage current (I_{LEAK}) within inverter stress;* <u>*Dev-A*</u>

Static Forward Conduction Stress

This results presented here are on Dev-A and Dev-B DUTs when subjected to static bias stress. Here, the body diode of the MOSFET was forward biased with continuous DC forward current (I_F) of 10 A supplied using a current source at T_{CASE} = 100 °C. In order to maintain consistency in results, a total of 4 different devices were tested in series for each DUT type for a total of 100 stress hours. The test conditions are summarised in Table 6.3. During the stress, the test was stopped at regular intervals and the body diode forward characteristics (I_F versus V_F) were plotted at regular intervals using curve tracer and compared to the characteristics prior to stress. The body diode I_F/V_F forward characteristics for one Dev-A DUT are presented in Figure 6.9. The other three devices also showed a similar shift in the characteristics and therefore are not included here. Initially, V_F shifts to the right as can be seen from the measurement at 24 hours. However, after 72 hours of stress, the curve shifts back to the left overlapping the curve at 0 hours demonstrating a relaxation effect. After that, the I_F versus V_F characteristics become stable as can be seen from the measurement at 100 stress hours.
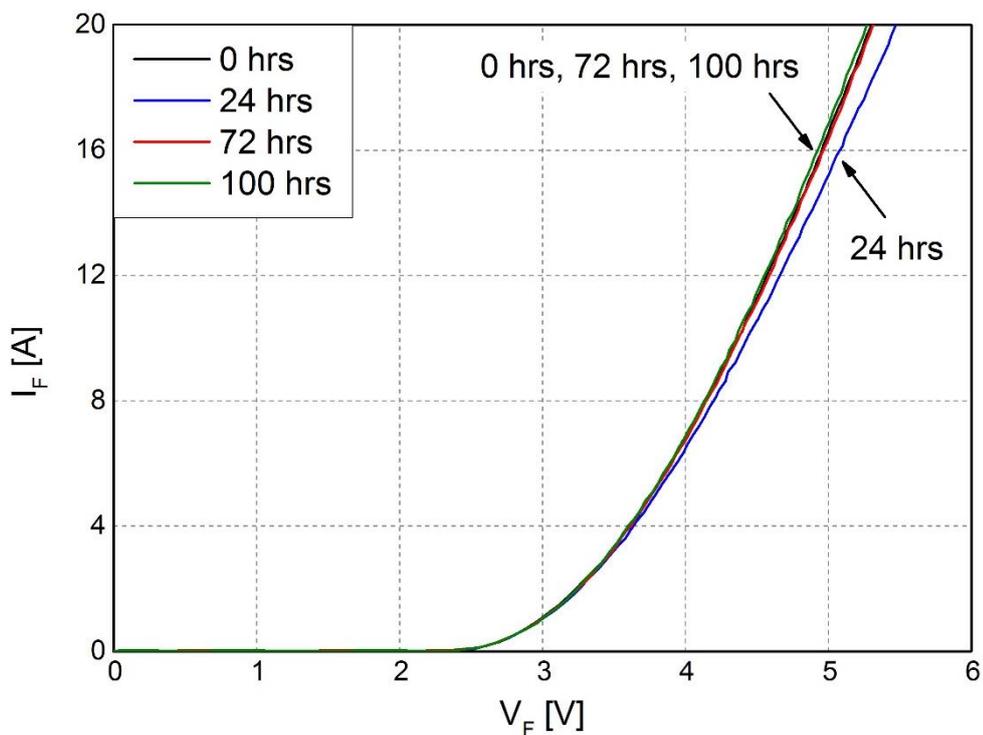
Figure 6.9: Evolution of body diode forward voltage drop (V_F) within static stress; Dev-A

Table 6.3: *Summary of test conditions (Static stress)*

T$_{CASE}$ (°C)	V$_{GS}$ (V)	Stress Duration (hours)	I$_F$ (A) - Continuous
100	-5	100	10

The body diode forward characteristics for Dev-B DUT is shown in Figure 6.10. Once again, results are included for only one device and the remaining DUTs showed a similar trend as shown in Figure 6.10 and thus not presented here. The I$_F$ versus V$_F$ curve shifted to the right as the stress accumulated on the device as can be seen from the curve at 24 hours stress duration. However, the characteristics shift back slightly to the left after further stress as could be seen at 72 hours as a result of relaxation effect. The characteristics then became stable as could be seen from the measurement at 100 hours. The shift in characteristics towards the right implies an increase in forward voltage drop (V$_F$) for the same forward current level (I$_F$).
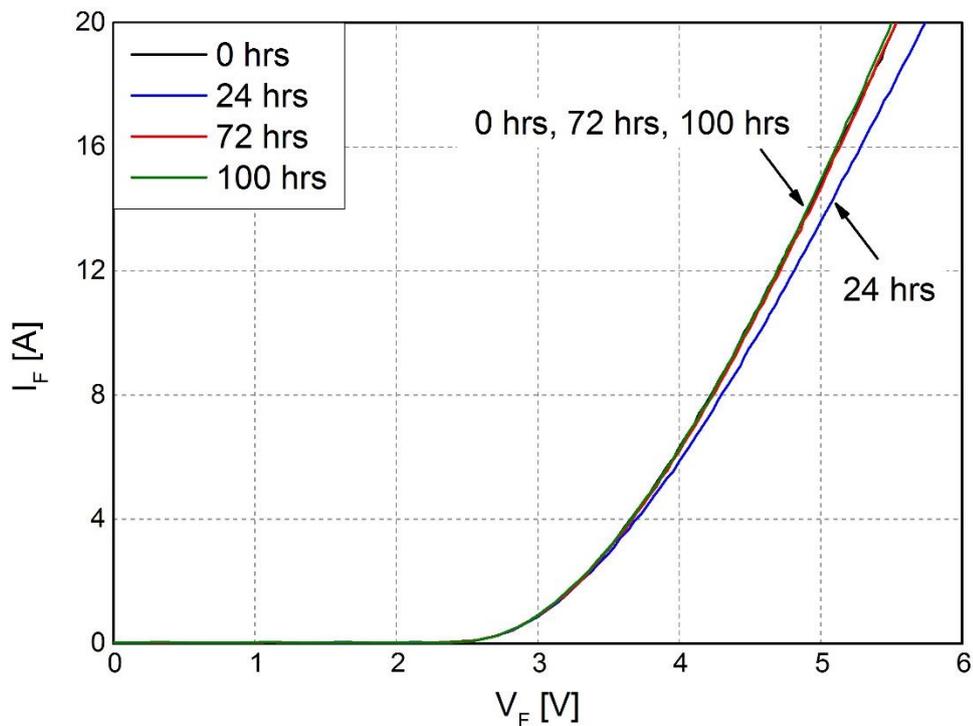
Figure 6.10: *Evolution of body diode forward voltage drop (V$_F$) within static stress; Dev-B*

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6.2. Discussion

During the operation of an inverter, four different types of stresses that the DUTs undergo could be identified. High $\frac{dV}{dt}$ when the devices are switching is one of them. The other two being the body diode forward current conduction and reverse blocking periods. Last but not least, is the stress when the body diode forward current has to be diverted when the device is turned ON (upon formation of the channel) since this is the case in synchronous rectification. Figure 6.11 presents how the typical drain source current flow lines within the MOSFET at 3 different time instances would look like within inverter operation. The 3 different time instances are as follows: a) forward current conduction of the body diode; b) body diode forward current diversion to the channel and c) current conduction through channel when device is fully ON and diode completely OFF. For the second case, though small in the case of SiC, reverse-recovery current still flows internally in the device. Such current forms a loop through the channel and hence, device sees high current spike at that instance.

An increasing V_F is attributed in various literature to the basal plane dislocations (BPDs) in the epitaxial layer, which results in the formation of stacking faults (SF) upon forward biasing of SiC PiN diode [101-103]. Positive change in V_F is undesirable as it can adversely affect the inverter's performance and efficiency i.e. higher body diode forward voltage drop for the same current level.

The slight increase in I_{LEAK} for Dev-A, Figure 6.8, is contributed not only by the stress of the body diode structure but also by the stress imposed when the device undergoes the reverse-recovery and the reverse bias stress during the MOSFET's forward voltage blocking periods. One possible physical mechanism for increased drain leakage current is the recombination-induced SFs. The SFs are caused as a result of forward biasing of the body diode which then act as recombination centers. These recombination centers introduce electronic states in the middle of the bandgap, which, in turn, behave as generation centers when the body diode is

reverse biased, causing a higher leakage current [102]. In [104], another possible mechanism is discussed for MOSFETs with thin gate oxide layer: is gate-induced I_{LEAK} due to band-to-band tunnelling taking place within the depletion region in the gate / drain overlap region when the MOSFET is in the blocking state. However, an in-depth physical interpretation of the above-mentioned mechanisms is beyond the scope of this project study.
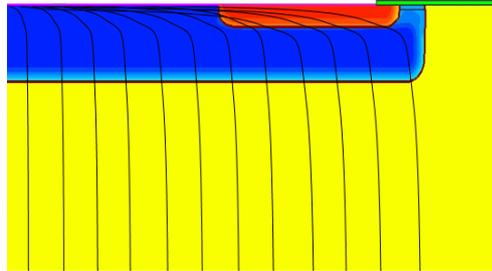
(a) – Body diode forward current conduction
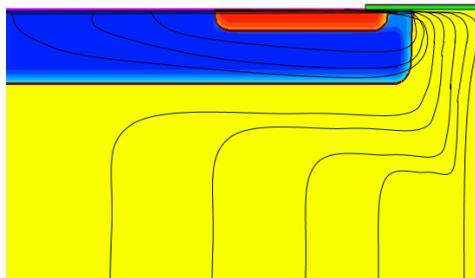
(b) – Current diversion from body diode to channel
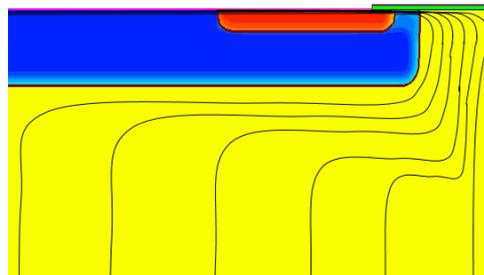
(c) – Current conduction through the channel

Figure 6.11: *Current flow lines for a MOSFET within inverter*

Results for Dev-A and Dev-B, presented in Figure 6.9 and 6.10, are in line with the interpretations formulated in [101, 102]. It is of interest to note that the body diode degradation becomes significant for higher current values as depicted in Figure 6.9 and 6.10 for static bias stress. It is really important to take this into account since the body diode of a MOSFET deployed in an inverter is forward biased under a wide spectrum of current values. Since all the V_F measurements for DUTs stressed within the inverter were carried out for $I_F =$ 500 mA (see definition of V_F in Appendix C), which is quite close to the knee voltage of the body diode, therefore, it might be that the real impact of the stresses on DUTs may be somewhat underestimated. Going forward, it would be beneficial to plot I_D vs. V_F characteristics at timely intervals for the devices stressed within the inverter instead to have a much better understanding of the V_F degradation due to the stresses applied.

The results presented for the chosen stress conditions on both DUT types demonstrated a good performance of the body diode feature in both inverter and static stress operation. The static stress results showed a temporary shift in the forward characteristics but then the characteristics starting from 72 hours shifted back to 0 hours indicating no substantial degradation over the 100 hours of stress. Moreover, as seen in Figure 6.7 and 6.8, that a small shift was observed in V_F and I_{LEAK} towards the end of the 1000 hours in the inverter stress conditions. Therefore, it has to be anticipated that newer test standards need to be developed where different stress regimes could be applied unlike for the case of Si. The inverter stress was only applied for 1000 hours due to time constraints since tests had to be repeated many times. Furthermore, it is required that more tests are carried out with higher T_{CASE}, $I_{PH(PK)}$ and V_{DD} to accelerate degradation.

Lastly, the measurements in Figures 6.1 to 6.4 were performed to demonstrate that the shift observed in the parameters is purely due to stress and not due to an error in T_{CASE} and/or V_{GS}. As demonstrated by these figures, a significant discrepancy in the value of T_{CASE} and V_{GS} is

required in order to observe such shifts which is not possible. Extra care was taken to ensure

consistency in the applied T_{CASE} and V_{GS} at the time of each measurement to minimise any

occurrence of errors.

7. Conclusion and Future Work

7.1.   Conclusion

The robustness and reliability investigation of SiC power MOSFETs mainly during short circuit and avalanche breakdown operations have been presented here in this project. Such transient events are really stressful for the device and may occur on a frequent basis in a given power system. Power devices are expected to have a certain degree of robustness to sustain such events, sufficient enough to allow the protection circuitry to remove such events. However, if such transients are not removed quickly upon occurring, they can also result in destructive failure of the device. This project dealt with various different experimental methodologies and simulation techniques in order to perform comprehensive electro-thermal device characterisation. The project aims to figure out the absolute device limitations using functional characterisation followed by structural characterisation in order to try to understand the failure mechanism during such events with the help of analysing temperature distribution inside the device. Moreover, to complement the experimental results on packaged devices and bare die devices, simulations were also carried out to further understand the physical mechanism taking place inside the device at failure.

The short circuit tests show that SiC power MOSFETs have considerable intrinsic robustness. Dev-A devices can safely do $t_{SC} \geq 10$ µs at low voltages up to around $V_{DD} \sim 500$ V. Above this V_{DD}, devices are not capable of withstanding the minimum short circuit duration requirement of 10 µs. The usual industrial requirement for a power device is to at least do 10 µs at two-thirds of the rated $V_{DS(max)}$. None of the device types tested are able to meet this requirement, however, SC robustness of Dev-B DUT is slightly better than the other 2 devices.

Two prominent precursors of failure were identified for SC operation i.e. change in current slope before device turn-off and appearance of current tails after device turn-off. However, if the t_{SC} during the tests was increased further, the device eventually failed or degraded. Here,

two different failure modes were identified which were distinguished by the power levels during SC. For lower power levels during SC, the device experiences slower temperature dynamics hence allowing enough time for the constituent features of the device's surface (i.e. metallization and/or passivation layer) to degrade resulting in a significant decrease in the resistance/impedance between gate and source terminals. Here, it is important to note that limitations due to packaging-related issues are responsible for device degradation and it is not due to the semiconductor material itself. In this case, gate leakage current significantly increased and the current during SC pulse also decreased. The decrease in the SC current could be understood better when reference is made to the thermal maps showing a decrease in temperature for a cluster of cells indicating that those cells cease to conduct current. Here, upon a decrease in SC current, the device was regarded as being degraded and not fit for purpose anymore. This failure was defined as a soft failure. In the other case, for higher power levels, the device failed destructively with an uncontrollable sharp increase in the drain current after device turn-off. For higher power levels, the temperature increase inside the device is faster such that it reaches the critical temperature to give significant drain leakage current eventually resulting in thermal runaway. For tests at high power levels, thermal maps showed the formation of the hotspot in a really small localized number of cells. Those cells drain more current than the remaining cells and hence temperature in those small number of cells increases further and eventually, the critical temperature is reached and the device undergoes thermal runaway. This failure was termed as a hard failure.

Aging tests for short circuit also showed signs of degradation for the device. Upon consistent dissipation of power during SC, the SC current decreased in value as the stress accumulated on the device and it eventually stabilized after few hundreds of pulses. Once again, the decrease in the SC current was found to be linked to an increase of the gate leakage current and the overall on-state resistance. Repetitive stress on the device also resulted in a decrease

of the gate-source voltage indicating a severe degradation of the gate structure i.e. increase in the total gate to source resistance.

Simulation results have shown that the hole current flowing between N-Drift and P-Body is responsible for the current tail at turn-off. The high electric field present in the N-Drift region generates hole carrier which moves upwards to the top of the device. The hole carriers eventually punch through the P-Body / N-Drift region resulting in the flow of hole current. Once the generated hole carriers are removed, the current tail disappears and goes to zero. However, when the magnitude of hole current becomes critical, the device enters thermal runaway as identified by the sharp increase of the drain current after device turn-off.

Avalanche robustness of power devices is usually tested using an unclamped inductive switching test setup. Out of the three type of SiC power MOSFETs tested, two of them (Dev-A and Dev-C) possess substantial avalanche ruggedness. However, Dev-B lacked avalanche ruggedness and it failed immediately after it entered breakdown. Dev-A DUTs are capable of dissipating avalanche energy of up to 1 J demonstrating an acceptable good performance of the body diode. Similarly, Dev-C DUTs also demonstrate a good degree of avalanche robustness. An important thing to be noted here is the big difference in the actual breakdown of all three devices. The breakdown voltages of Dev-A, Dev-B, and Dev-C are approximately 1800 V, 2300 V, and 1400 V respectively. It is due to different N-Drift doping concentrations and their thicknesses used in all three devices which tends to define this feature of a power device.

The failure of SiC power MOSFETs during avalanche breakdown is characterised when the device loses its ability to block voltage. As a result, when failure happens, the breakdown voltage goes down to zero indicating a short between all three terminals. When this happens, the current starts to increase again (i.e. current slope changes sign and its value) as dictated by the inductor value. Moreover, tests performed on bare dies showed a formation of hotspot

close to the source pad. Two possible mechanisms behind hot-spot formation could either be thermal runaway or activation of the parasitic BJT and the latter case being highly unlikely to occur in SiC transistors due to its wide energy bandgap. Moreover, as also discussed in chapter 2, during avalanche breakdown, the devices operate within a highly electro-thermally unstable region where the occurrence of hot-spots i.e. thermal runaway is very highly likely. The simulations have demonstrated that during failure, the electron current begins to flow in and underneath the channel as a consequence of really high lattice temperature inside the device which resulted in a decrease of the threshold voltage. This has been supported by the experimental analysis of devices during avalanche breakdown under different V_{GS} values along with measurement of V_{th} versus temperature. Moreover, no signs of parasitic BJT activation were observed during simulations. Low gain of the parasitic BJT and the superior properties of SiC suppresses the BJT activation for the ensuing power and temperature levels in this study. Therefore, the failure is as a result of electron leakage current flowing between the N-Drift and N+ Source region.

As such, aging tests didn't show any change in the current and voltage waveforms during operation. However, to monitor the device degradation, V_{th} was regularly monitored which showed a positive increase in its value as the stress accumulated on the DUT. The shift in V_{th} is usually attributed to the high density of interface traps at the SiC/SiO$_2$ interface.

Body diode reliability study carried out on Dev-A and Dev-B DUTs showed great performance of the body diode feature with no substantial degradation of the monitored electrical parameter. The I_F/V_F curve initially shifted to the right but eventually returned back to its original curve prior to stress at 0 hours as a result of stress relaxation effect.

Overall, the SiC MOSFETs types tested here showed a considerable amount of robustness during these transient events. However, there is still clearly an area for improvement as these devices do not meet the SC withstand criteria of the industry. Moreover, many potential

features of SiC MOSFETs are still limited due to packing related issues. Indeed, newer packaging technologies are also needed to fully exploit the benefits of SiC transistors.

7.2. Contribution

An innovative approach was implemented to develop a methodology in order to perform a detailed device characterisation consisting of experimental measurements (functional characterisation), IR measurements (structural characterisation) and electro-thermal simulations. The developed methodology was used to determine the absolute device limitations within SC and avalanche breakdown operation for SiC power MOSFETs as well as to better understand the underlying failure mechanisms within these modes of operation. The IR measurements provided a lot of useful information about the evolution of temperature distribution inside the device (non-uniform temperature distribution and formation of hotspots at failure) leading up to failure. Moreover, electro-thermal simulations gave an in-depth insight into the physical mechanisms responsible for the failure. In this thesis, 2 different temperature related failure mechanisms (Type I – Thermal Runaway and Type II – Increased gate leakage current (Degradation)) have been proposed for SC operation which can be distinguished by the input voltage (V_{DD}). For avalanche breakdown operation, failure has been associated with increased leakage current in and around the channel region which is dependent on the gate-source (V_{GS}) voltage used to keep the device turned off. An investigation into the stability of the body diode feature of SiC power MOSFETs has also been presented in the thesis. Body diode feature demonstrated great performance with no substantial degradation in the monitored electrical parameters.

7.3. Future Work

Device characterisation is a critical area of research as newer SiC device technologies are expected to emerge onto the market over the next few years as device manufacturing technology is advancing rapidly. SiC power MOSFETs with a voltage rating of 3.3 kV and 6.5 kV

are already on the market and such investigations also need to be extended for those devices to point out their absolute device operational limitations as well as the stability of electrical device parameters. Moreover, as the densities of defects in the wafer reduce with time, the trend continues towards manufacturing devices with higher voltage and current rating i.e. bigger die sizes. It is also expected that 10 kV SiC power MOSFETs are also not far away from becoming a commercial reality in the next few years. Furthermore, GaN transistors have also started to make their way onto the market, therefore, similar studies are also needed for their robustness investigation and technology maturity.

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A. Appendix A

Parameters used for Arora mobility model:

Electrons:

A_{min} = 22.83; α_m = -0.536; A_d = 53.92; α_d = -2.2

A_N = 2 x 10^{17}; α_n = 0.72; A_a = 0.76; α_a = 0.722

Holes:

A_{min} = 0; α_m = -0.57; A_d = 113.5; α_d = -2.6

A_N = 2.4 x 10^{18}; α_n = 2.9; A_a = 0.69; α_a = -0.2

Parameters for fixed charges and interface traps:

Positive fixed charges Q_F = 2.68 x 10^{12} cm^{-2};

Acceptor like traps Q_A = 7 x 10^{11} cm^{-2};

E_0 = 0.18 eV; E_S = 0.1 eV;

A uniform energetic distribution of traps was implemented as presented below:

$E_0 - 0.5E_S < E < E_0 + 0.5E_S$

where E_0 is the central energy for the trap distribution from the conduction band E_C

Parameters for OkutoCrowell Model

Electrons:

a = 0.1; b = 6.346 x 10^6; c = 0; d = 0; gamma = 1; delta = 2

Holes:

a = 4.828 x 10^6; b = 1.334 x 10^7; c = 0; d = 0; gamma = 0; delta = 1

B. Appendix B

MATLAB code for energy calculations for SC and UIS tests:

% Trapezoidal numerical integration

% Power calculation
% Supposing V and I (and hence P) are column vectors

P=V.*I;

% Energy calculation
% ending_value corresponds to index of the last element
% Vector I before current start to rise vertically for SC
% Vector I until current goes to zero for UIS

E=trapz(t(1:ending_value,1),P(1:ending_value,1))

C. Appendix C

For the body diode forward voltage drop measurement, the measurement was done with V_{GS} = -5V and I_F = 500mA. The voltage applied between source and drain was increased until the ammeter read 500mA.
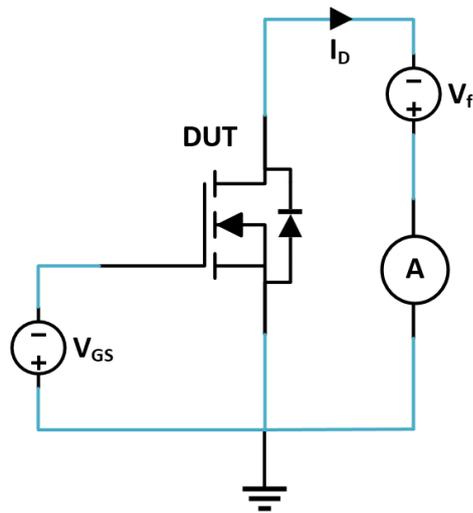

Figure C.1: *Measurement circuit for body diode forward voltage drop (V$_F$)*

The I_{LEAK} measurement was carried out at V_{DS} = 960V with gate and source shorted. At that applied voltage, the current value read from the ammeter was the drain leakage current.
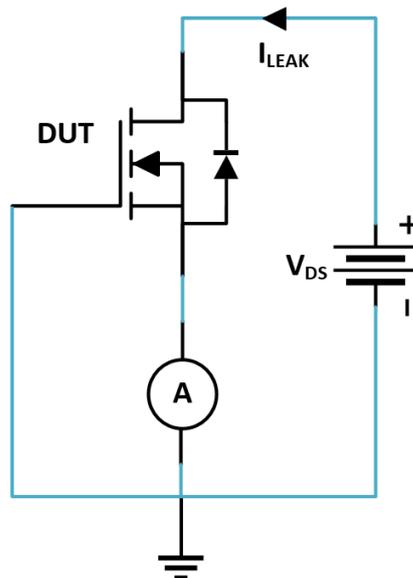

Figure C.2: *Measurement circuit for drain leakage current (I$_{LEAK}$)*