The University of Nottingham, Malaysia Campus
Department of Electrical and Electronic Engineering

INVESTIGATING AGEING BEHAVIOURS IN SUPERCAPACITOR (CELLS AND MODULES) USING EEC (ELECTRICAL EQUIVALENT CIRCUIT) MODELS

HADIZA AHMAD ABUBAKAR

Thesis submitted to the University of Nottingham for the degree of Doctor of Philosophy

May 2016

To Farhan (Chukwudi)

“You are a breath of fresh air and a source of light”

ABSTRACT

This thesis contributes to the reliability and ageing studies of supercapacitors for more efficient use in EV/HEV applications. This thesis demonstrates the effect of ageing/failure in supercapacitor cells and module cells using accelerated tests employed to expedite the ageing process. The tests, as explained below were categorised based on operational and environmental ageing factors associated with supercapacitor failure in EV/HEV applications to;

- Investigate supercapacitor cell performance at high temperature and constant voltage individual conditions, and also simultaneously (known as calendar test)
- Investigate the effect of voltage balancing/equalisation circuits on supercapacitor module cells' performance during constant current cycling tests under certain environmental and electrical factors
- Investigate supercapacitor module cells' cycling performance in a lab-scale designed electrical DC programmable motor load system that emulates supercapacitor operational conditions in an EV/HEV application.

The ageing behaviours characterised by the three factors mentioned above are quantified in this thesis through the periodic monitoring of their electrical and electrochemical state of health with Electrochemical Impedance Spectroscopy, Cyclic Voltammetry and Constant Current characterization tests. These tests help identity ageing modes in supercapacitors, and it was observed that regardless of their ageing factors; an increase in ESR and decrease of capacitance was determined. Although this

information is required, the results from Electrochemical Impedance Spectroscopy (EIS) tests revealed more details distinctive to each ageing factor. From this distinction, the ageing mechanisms in relation to the ageing factors, which causes the deterioration in the supercapacitor electrical performance, are identified and summarized as the following:

1. Loss of contact within supercapacitor electrode, given rise to the contact resistance due to the presence of high temperature as the main ageing factor
2. Change of supercapacitor porous electrode emulating a charge transfer reaction thereby increasing its distributed resistance, caused by the effect of high voltage or cycling

Mathematical models in the form of electrical equivalent circuits (EECs) distinctive of their ageing factors are generated from EIS electrochemical behaviours to easily describe ageing behaviours in supercapacitors. The EEC models developed using impedance modelling, generated an initial model from dormant cells, which transitioned to ageing models distinctive of their ageing factors as soon as a 100% increase in ESR and/or an 80% decrease in capacitance is observed. The proposed EEC models were validated to show the dynamic interaction between ageing of the supercapacitor cells on their electrical performance in both frequency and time domains.

In summary, the EEC models encompasses this thesis objective and as such considered the main contribution of this research work.

ACKNOWLEDGEMENTS

First and foremost, the greatest thanks go to Allah (S.W.T) for making this Ph.D. experience possible. You are indeed the Greatest, The Most Gracious, The Most Merciful.

It is with immense gratitude that I acknowledge the support of my supervisor Professor Dino Isa. Professor, thank you for being patient throughout this process. You are indeed blessed with humility and kindness. Even with the delays and disappointments you remained patient with me and uttered nothing less than encouragements. I remember always leaving our meetings uplifted than when I came in. Thank you.

Dr. Nur Nafisah Naim, I am proud to have seen the successful completion of your Ph.D. I would have to say I share the credit of this work with you; you have been instrumental in the completion of this thesis. Your notes, insights, support in the Lab and general assistance is greatly appreciated. Thank you Dr. Goh Chia Chieh and Nik Ahmad Akram, with your knowledge on circuitry design and coding, and your ability to render assistance whenever asked. Thank you Mr. K. Parthipann for always available to assist with the oven and compressor.

I would like to thank my parents for providing the financial, emotional and spiritual support needed to complete this thesis. Thank you for pushing me to realise my potential in the pursuit of this Ph.D. YOU ARE SIMPLY THE BEST.

Of course, I could not have endured these few years of my life without the unconditional support and love of my siblings. I love you guys. Zahrah, Nazir, and Bashir, thank you for your companionship on campus, you might not have noticed but it was greatly needed and fully appreciated.

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GLOSSARY

AEC - Asymmetric Electrochemical Capacitor

AC - Activated Carbon

AN – Acetonitrile

ANN – Artificial Neural Networks

C – Capacitance

CC – Constant Current

CMOS - complementary metal oxide semiconductor

CNLS - complex least-squares

CNTs - carbon nanotubes

CV – Cyclic Voltammetry

C-V – Constant Voltage

DAQ – Data Acquisition system

DL - Dielectric

DOE - The United states Department of Energy

EC – Electrochemical Capacitors

EEC – Electrical Equivalent Circuit

EDL – Electrical Double Layer

EDLCs – Electrical Double Layer Capacitors

EIS - Electrochemical Impedance Spectroscopy

EOL – End of Life

EPR – Equivalent Parallel Resistance

ESR – Equivalent Series Resistance

ESS – Energy Storage System

EV – Electrical Vehicles

DP – Drive Pulses

FC – Fuel cells

FCHEV – Fuel cell hybrid electric vehicle

GBL - γ-butyrolactone

H – HIGHWAY drive cycle

HEV – Hybrid Electric Vehicles

IL – Ionic Liquid

IHP – Inner Helmholtz plane

NFN - Neo-Fuzzy Neuron

OHP – Outer Helmholtz plane

PC - propylene carbonate

PSD - Pore Size distribution

R – RURAL drive cycle

SC – Supercapacitor

SEC - Symmetric Electrochemical Capacitor

SnG – STOP N GO drive cycle

SOHIO - Standard Oil Company of Ohio

SOH - State of Health

SU – SUBURBAN drive cycle

U – URBAN drive cycle

DEFINATION OF TERMS

A few terms used in this thesis and their definitions are presented below;

Accelerated ageing test – A set of test which is used to expedite ageing process in supercapacitors. It is performed at stressful conditions usually involving temperature and voltage to aggravate chemical reactions in supercapacitors.

Ageing behaviour – The behaviour exhibited during accelerated ageing test

Ageing duration – The time it takes the supercapacitor to fail, after concluding the accelerated tests.

Ageing effect – the influence of ageing on supercapacitor during accelerated tests.

Ageing factor/Stress factor – the cause of stress or pressure in a device which eventually causes the device to fail. The ageing factor can be from mechanical stress, environmental stress or operational stress.

Ageing mechanism/Failure mechanism– a detail description of an ageing process usually ignited by mechanical, electrical or environmental stress on a device which that contributes to a failure event.

Ageing mode/Failure mode – the manner in which a failure occur in a device either in a total lost in functionality to perform its intended function or unable to meet its requirement.

Ageing monogram – a signature that represents ageing effects in supercapacitor behaviour.

Ageing model/Failure model - an electric equivalent circuit model based on the aged response of supercapacitor behaviour.

Ageing rate – ageing rate is related to the chemical reactions in supercapacitor. Chemical reactions in supercapacitors is speeded up usually either by voltage or temperature. When the rate of the chemical reactions are increased, ageing happens quicker.

Balancing circuit /Equalization circuit – An electrical circuit used in balancing voltage/ current between supercapacitor cells in a 'module'.

Calendar life – Is a test used to sustain supercapacitor stored energy at a time by maintain the voltage at a constant value. This method of ageing test helps in measuring leakage current in supercapacitors.

Cell opening – swelling on the casing of the supercapacitor due to build-up of pressure which leads the cell to open up.

Cycle life – the number of complete charge and discharge cycle in supercapacitors, cycled from the minimum voltage of the supercapacitor to the its rated voltage, before the supercapacitor lost 20% of its initial capacitance or its resistance increased by 100%.

Cycling – a repeated charge and discharge cycle between two voltages using a set current on supercapacitor.

End-of-life – refers to the end of the useful life of supercapacitors. The criteria for the end-of-life is usually set by the manufacturers.

Leakage current - meaning the minimum current needed to charge a SC from 0V.

Open circuit/Short circuit – no current source or voltage source is attached to the supercapacitor, therefore no charge flows between the supercapacitor terminals.

Pre-conditioning – Discharging and storage of a capacitor under specified ambient conditions (temperature, humidity, and pressure) until its inner temperature attains thermal equilibrium with the surrounding temperature before testing.

Reference temperature – Is in between the ranges of 25°C ± 2°C by the IEC standard 60068-1

SC degradation/failure - This occurs when a supercapacitor exhibits a 20% decrease of its initial capacitance or its resistance increased by 100%, or in some extreme cases becomes an open or a short circuit

SC model – an electric equivalent circuit model based on the response of supercapacitor behaviour.

SC module – the arrangement of more than one supercapacitor, the arrangement is either done in series with the positive electrode terminal of one supercapacitor connected to the negative electrode terminal of another supercapacitor and so on, or arranged in parallel with the positive electrode terminal of one supercapacitor connected to the positive electrode terminal of another supercapacitor and so on

State of health – the condition of the supercapacitor usually referred to the cell capacitance.

Stress levels – the rate at which the stress factor is applied

Voltage Imbalance – is the uneven dispersion of voltage rating between supercapacitor cells in a 'module' during charging operations.

Lab-scale test bench (load based cycling system) – is a lab scale circuitry design for a programmable charge-discharge load, used in some of the ageing accelerated tests.

Note: The words; failure, ageing and degrading were used interchangeable throughout this thesis, so also was equalization and balancing.

CHAPTER 1- INTRODUCTION

1 Introduction

This research work deals with the study of supercapacitor ageing with regards to life expectancy and reliability. This work presents a unique approach to addressing the research problem and as a result, improve supercapacitor performance.

The main aim of this research work is to study the individual aspects of ageing in supercapacitors observed in Hybrid-Electric Vehicles (HEV/EV) applications.

1.1 Research Background

Supercapacitors are considered necessary energy efficient devices for rapid energy storage and delivery (Delhi, 2014). In recent years, supercapacitors have attracted significant attention, mainly due to their high power density, long life cycle, and bridging function for the power/energy gap between traditional dielectric capacitors

(which have high power output) and batteries/fuel cells (which have high energy storage) (Wang, Zhang, & Zhang, 2012) (Chmiola et al., 2006). Among the advantages of supercapacitors are high power density, a long lifecycle of charge/discharge with high currents, high efficiency, a wide range of operating temperatures, environmental friendliness with low maintenance, and high safety. These characteristics have made supercapacitors very competitive in various applications (Ban et al., 2013) (Francois Beguin, 2009). Unfortunately, even with all its advantages, supercapacitors still pose some challenges such as low energy density high cost, and high self-discharge rate, which limits specific applications (Wang et al., 2012) (Ricketts & Ton-That, 2000).

These challenges may cause some major concerns especially in supercapacitor cycle and shell life such as;

1) High cell voltage i.e. operating voltage higher than rated voltage, as a result of electrochemical decomposition of solvent due to the limited electrode material stability and/or solvent's thermodynamic decomposition windows which could produce gaseous products, leading to the pressure build-up inside the cell, causing safety concerns and self-discharge (Abdallah, Lemordant, & Claude-Montigny, 2012; Bittner et al., 2012; Chiba et al., 2011; Yang & Zhang, 2011)

2) Supercapacitor parallel leakage causing fast self-discharge and decrease in supercapacitor shell life. The factors that contribute to this particular limitation observed in supercapacitors are as follows (B. Conway, 2009): (a)

Faradaic reaction of electrolyte impurities; (b) parasitic redox reactions involving impurities; c) non-uniformity of charge acceptance along the surface of electrode material pores; and d) possible short-circuit of the anode and cathode from improperly sealed bipolar electrodes.

However, researchers have found ways to minimise some of these challenges by increasing energy density using two approaches that are expressed by;

$$E = \frac{1}{2}CV^2 \tag{1.1}$$

Where, E is energy storage, C is the specific capacitance and V is the cell voltage:

(1) The first approach is to increase the capacitance (C) of the electrode material while the. (2) The second method is to increase the cell voltage (V) using solvents such as non-aqueous and ionic liquid solutions which have a wider electrode potential window (Lewandowski & Galinski, 2007; Lewandowski, Olejniczak, Galinski, & Stepniak, 2010). It is understood that increasing the cell voltage is more efficient than increasing the capacitance as voltage is squared in the energy storage formula expressed above. Although research literature so far has documented supercapacitor voltage rating to be in the ranges of 1V-5V, this voltage levels is still not high enough to satisfy most applications such as; mobile phones, digital cameras, and hybrid/electrical vehicles, etc. (Ban et al., 2013). Hence the need to increase the voltage of the system by connecting individual SC cells to meet applications requirement (Al Sakka, Gualous, Van Mierlo, & Culcu, 2009).

Apart from the challenges mentioned above, which could be improved by refining certain material aspect of the supercapacitors during the development phase to

increase energy density (Li & Wei, 2013) (Farma et al., 2013). Supercapacitors tend to be reliable and require low maintenance during operations when used under the boundary conditions as (prescribed by manufacturers). Unlike batteries they have long cycle life and are rarely interrupted or replaced during continued operations. Despite having met all the conditions, some issues associated with the use of supercapacitors have been reported by many researchers with an agreement that, after some years of operation, supercapacitors develops capacitance fading and increase in resistance (El Brouji, Briat, Vinassa, Henry, & Woirgard, 2009). Supercapacitor lifecycle as predicted by various researchers are in the range of 10-20 years (Bohlen, Kowal, & Sauer, 2007), this is presumably true when operating under the boundary conditions defined by the manufacturer. However, supercapacitors used in a system especially in EV applications may not perform under these nominal conditions; Hence, the life expectancy of a supercapacitor has to be revised to include the factors affecting the ageing behaviour as a result of the system operation modes coupled with the supercapacitor manufacturers' datasheet.

Given these concerns, the need to improve SC reliability is crucial and therefore this research work focuses on testing the boundary conditions in supercapacitors, so as to analyse and mitigate supercapacitor failure/ageing modes. The research methodology proposed in this thesis is categorised into three sections to investigate ageing test methods, which includes; (a) Degradation mechanism based on supercapacitor parameter failure modes, (b) Life-expectancy timeline based on parameter deterioration, (c) supercapacitor Equivalent Electrical Circuit (EEC) model representing the degradation process.

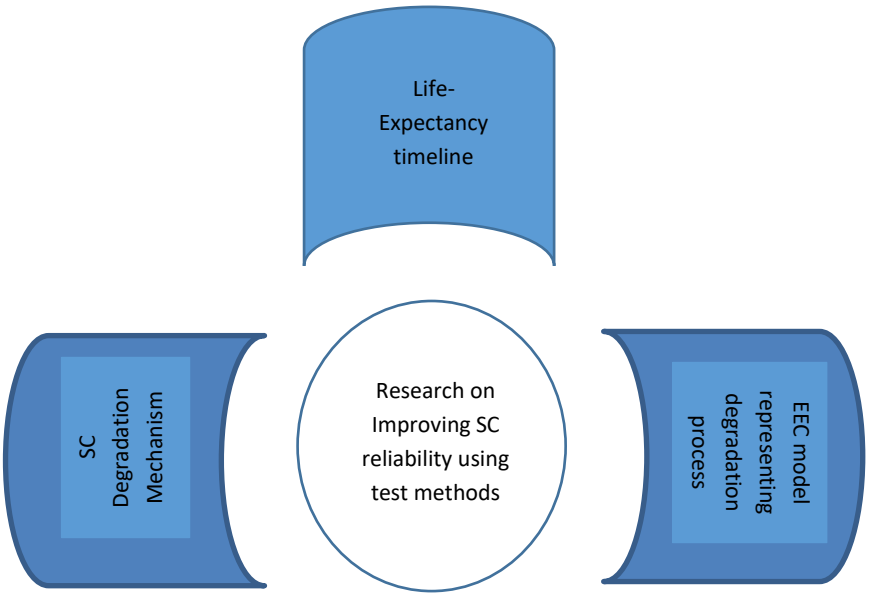


Figure 1-1: Research on improving SC reliability classified into three area of study

During the last decade, a significant number of investigations have been dedicated to testing these boundaries to maximise the capability of supercapacitors and also to understand their ageing behaviour under certain conditions. Depending on the conditions under which they are operated, supercapacitor performance can be affected in many ways, thus calling for more research on the study of degradation mechanism in supercapacitors; (M. Ayadi et al., 2013; Mohamed Ayadi, Briat, Lallemand, Coquery, & Vinassa, 2014; Chaari, Briat, Delétage, Woirgard, & Vinassa, 2011b; d'Entremont & Pilon, 2014; German et al., 2013)(M. Ayadi et al., 2013; Mohamed Ayadi et al., 2014; Chaari et al., 2011b; d'Entremont & Pilon, 2014; German et al., 2013).

Likewise, there is also growing interest in the development of supercapacitor model to understand their behaviour and the implication of the product design on the electrical performance (Ban et al., 2013; Fletcher, Black, & Kirkpatrick, 2014; Ike, Sigalas, Iyuke, & Ozoemena, 2015). Modelling is used to simulate system response to

give a better understanding of system applications in real time. In this case, the modelling of a supercapacitor is a good approach to understanding the actual outcome of using supercapacitors in an electrical system.

A large number of proposed models are in the form of equivalent electrical circuits (EECs) (Ban et al., 2013; Diab, Venet, Gualous, & Rojat, 2009; Faranda, 2010; Tironi & Musolino, 2009; Ying Zhang & Yang, 2011). The EECs are usually fit for specific applications. The problem though lies in the time scale of the EECs operation. First, they are built for short-term operation. Thus, their response only covers the short range of dynamic effects of supercapacitors. Second, they do not take into account the degradation in the state of health of supercapacitors. In reality, supercapacitors will be exposed to prolonged operation, whereby in due time, ageing will become inevitable. Therefore, efforts have been invested in searching for an approach that does not only look at the behaviour of the supercapacitor within a short operation period but is also interested at how supercapacitors will behave if it is used for the whole lifetime of the system. This need has fueled the emergence of complex models which are built to resemble the long-term behaviour of supercapacitors (e.g. (Bertrand, Briat, Vinassa, et al., 2010; Bohlen et al., 2007; Lajnef, Vinassa, Briat, Azzopardi, & Woirgard, 2007; Martin, Quintana, Ramos, & De La Nuez, 2008; Mitkowski & Skruch, 2013)).

1.2 Research Course

To steer this research on the right course; the research issue, questions, objectives, contribution and methodology is addressed.

1.2.1 Research Issue

Supercapacitors (SC) as a result of their high power density (Ko & Carlen, 2000)(Gualous et al., 2012)(Mohamed Ayadi et al., 2014) have been recently adopted as a preferred device for power storage especially in automotive applications (Bohlen et al., 2007) where they provide interesting solutions when it comes to the peak power requirements needed to operate HEV and EVs, such as the stop-start, boost and regenerative operation modes (Chaari, Briat, Delétage, Woirgard, & Vinassa, 2011a). Even with the SC's low energy density compared to batteries, as a result of their large capacitance (C) and low internal resistance (ESR), SC's are suitable options for applications where fast charging or discharging with high current rates are needed (Yu Zhang & Jiang, 2009).

Although SCs have long cycle life and could potentially live as long as the applications they are applied in and, B. E. Conway, (1999), their life span (ageing influence) is a major conundrum within literature: (Eggert & Heitbaum, 1986)(Kurzweil, Frenzel, & Gallay, 2005)(Kötz, Hahn, & Gallay, 2006), especially for EV applications.

After prolonged operations, SCs demonstrate parasitic electrochemical reactions such as the decomposition of the electrolyte under certain conditions, which

drastically reduce the life expectancy of the SC device, (Bohlen et al., 2007) characterized by failure modes which includes; increase in resistance and decrease in capacitance, short circuit or open circuit (for SC module operation) (Kötz, Ruch, & Cericola, 2010a), microscopic phenomena such as gas evolution, increase in electrode mass, and local separation of the coating layer from the metallic collector.(Azaïs et al., 2007)

SC's performance have significantly improved especially in the areas of material development (M. Ayadi et al., 2013). However, the issue of SC degradation/failure, especially SC ageing mechanism concerning its stress factor remains a challenge in the industry with limited documentation. According to some investigators (R.Gallay, A.Oukaour, B. Tala-Ighil, H.Gualous, B.Boudart, 2013), "improvement of supercapacitor reliability is fundamental and the follow-up and the detection of the ageing state remains a priority to avoid breakdowns and thus to intervene at the convenient moment". This suggests why, it is just not enough to know the stress factors as already established and agreed upon by various researchers (A. Schneuwly, M. Bartschi, V. Hermann, G. Sartorelli, R. Gallay, 2002), rather it is also important to go further and understand the signature behaviour exhibited by each stress factor and its overall contribution to SC electrical performance deterioration.

The increase in voltage and temperature exponentially accelerate electrochemical reactions (Global Industry Analysis, 2010) which eventually degrades the SC device, where the ageing effects exhibited by each stress factor have a distinctive pattern as characterised by impedance data (Kötz et al., 2010a). Therefore, a better understanding of the degradation pattern or 'ageing signature' and how it relates to

SC failure (with relations to electrical performance) is mandatory, in other to predict the time and mode of SC failure from performance data, so as to improve product design and material.

The standard approach used in testing SC lifetime and performance are based mostly on cycle-life and calendar-life testing (FreedomCAR, 2004). In respect to SC lifetime and performance test methods, this research work is focused on accelerating ageing testing methods with elevated voltage and temperature conditions under various cycling profiles. And these accelerated tests are not limited to single cell SC as the power demands in most applications surpasses a single cell, hence the need for a "SC module". In testing, SC module have been documented to exhibit a unique mode of failure (Kötz et al., 2010a) different from a SC cell as its major issue is balancing the voltages between the cells with a voltage equalization/balancing circuit, (Kötz et al., 2007)(Yi Zhang, Wei, Shen, & Liang, 2009) (Daowd, Omar, van den Bossche, & van Mierlo, 2011) without which might lead to SC failure characterized by either an open or short circuit.

The standard method to study the behaviour of SC is through modelling the current-voltage characteristics of the device using electrical equivalent circuits (EECs). EECs are usually made up of components that are chosen based on a phenomenological basis (Barsali, Ceraolo, Marracci, & Tellini, 2010), in which the components are selected to match what is observed during SC operations. However, this method does little to help uncover the cause of the deterioration in SC performance, (Bertrand, Briat, El Brouji, & Vinassa, 2010) which needs a deeper investigation at the cell level. The electrochemical processes during ageing degrade SC internal

components, either by physical structural changes or by alteration of the chemical characteristic, either way, both affecting SC overall performance.

In summary, this research work focuses on analysing SC ageing modes, through operational testing conditions in relation to EV applications. These testing methods, starts with standard power cycling and calendar test, to establish a baseline for SC ageing behaviour, and then expands further to investigate SC stress levels under conditions that emulate EV operation modes such as; the stop-start, boost and regenerative modes, this is done by introducing a load profile to emulate these conditions. In doing so, voltage equalisation/balancing circuit was introduced to the system to improve performance reliability. The act of SC balancing is crucial to the system when it comes to SC degradation. In fact, SC ageing caused by the lack of voltage balancing between cells due to open circuit is more detrimental to the whole system than any form of failure (Kötz et al., 2010a)(Fu, 2014)(Group, n.d.).

The experimental data gathered from SC accelerated tests is later used to create a model electrical equivalent circuit to explain easily the ageing evolution of SC dynamic electrical behaviour. This approach contributes to the underlying physics of SCs and also increase the efficiency of the SCs

1.2.2 Research Question

The issues presented above have generated a few questions that this research work seeks to answer. These issues are:

1. **How reliable are supercapacitors in EV applications: Supercapacitor lifecycle prediction on to EV applications**

Earlier, in EV applications, batteries were employed as the primary form of energy storage but after rigorous test, it was discovered that the battery life significantly decreases due to cycling at high power causing an increase in joule heating along the internal resistance of the battery. These degradation parameters have been researched extensively and have successfully projected battery life expectancy with precision.

Recently manufacturers have introduced supercapacitors, which are used in parallel with batteries (load levelling) to form an ESS (energy-storage-system) capable of meeting both power and energy requirements (Jeong, Lee, Kim, Choi, & Cho, 2002) thereby increasing the system efficiency. This arrangement brings about uncertainty in the system as a result of insufficient knowledge on the part of the SC performance and its life expectancy, and as to how deeply the battery performance is affected by the SC.

As a result of this uncertainty, studies have been carried out to address these situations, and researchers have still not been able to estimate lifecycle with precision.

The life expectancy of SCs under normal conditions as predicted by Bohlen et al.,(2007) to be in the range of 10-20 years for voltages below the rated maximum voltage and temperatures at room temperature. Although SCs used in a system especially in EV application does not operate under these nominal conditions, therefore, the life expectancy of a SC has to be revised to include

the factors affecting the ageing behaviour as a result of the system operation modes and conditions in relation the SC manufacturer's datasheet. According to a rule of thumb, the ageing rate doubles if either the SC voltage is increased by 100mV or the temperature is increased by 10K (Bohlen et al., 2007).

2. Supercapacitor applications: SC module in contrast to a single SC cell?

The power demands when dealing with EV is usually high, so when combining supercapacitors and batteries to form an energy system, the supercapacitors have to be sized up to meet up the power demands of the battery. A single supercapacitor voltage has the maximum rated value of 5V and because of the voltage limitation in SC, SCs are required to be connected in series and/or parallel to form a "module" in other for the application to operate at high voltage and high current levels.

In EV applications, SC module sizing and arrangement is a crucial factor especially in defining the power required to work these applications; factors like; voltage, current, capacitance and internal resistance have to be put under consideration when choosing the best method of SC arrangement. Each arrangement, that is to say serial, parallel or matrix connections are selected to favour either low or high power requirements of a particular application.

This problem is resolved by a better understanding of the EV application with regards to the SC testing methods that are employed.

3. **How to make SC more robust by integrating the system with a balancing circuit?**

In applications that require high power, the SC are connected either in series or/and parallel to form a module to meet system demands. A serial connection can produce a SC module with a high voltage during charging operations, although, these voltage boost does not guarantee that each SC cell charges at the same rate and that it would not exceed its individual rated voltage. In the event the rated voltage of any one of the SC cell in the module is exceeded, the life expectancy decreases as a result of over-voltage coupled with the possibility of uneven temperature distribution across the module (Kötz et al., 2007)(Al Sakka et al., 2009). Dispersion of SC parameters also leads to different ageing rates of each SC cell. The location of each of the SC cell contributes to the different ageing rate, whereby the cell that is closest to the terminal will be exposed to higher stress and thus experiences a stronger degradation as compared to the rest of the cells (Bohlen et al., 2007). This SC mode of failure is characterised by either a short or an open circuit. The instance this failure mode is met in any single SC, that component must be replaced or the whole system is jeopardised.

A voltage equalisation circuit is introduced to balance the voltage across the module evenly in the system, thereby increasing the life expectancy of the system.

4. **Supercapacitor failure and method of quantifying the failure evolution**

SC is stressed mostly by two predominant factors i.e. voltage and temperature which are the primary influence of ageing in SCs. SC performance during EV operation such as charge-discharge cycles deteriorates the life of SCs with time. This time frame under normal conditions could last up to tens of years, EV applications, however, do not operate under normal conditions and therefore, the test procedure needs to be accelerated within standards and manufacturers recommendations to study the degradation process under a reasonable time frame. The knowledge about the effect of temperature, voltage and charge-discharge cycle on SC performance and lifetime is vital for a successful utilisation of this device in an EV application. The consensus for SC EOL criteria is 20% loss of capacitance and/or more than 100% increase of the ESR (Gualous et al., 2012). These ageing phenomena are quantified and analysed by conducting characterization tests which include; constant current charge-discharge test, Cyclic Voltammetry test and Electrochemical Impedance Spectroscopy tests to determine the most precise method of parameter identification and also to model the electrical ageing behaviour of SCs.

5. **Study SC ageing mechanism for EV operations: By employing a lab-scale test bench (load based cycling system) to emulate EV drive cycle profiles, so as to analyse supercapacitor degradation process.**

A single failed cell can jeopardise an entire SC module and so, understanding the performance behaviour of a single SC operating on its own or in a module

is vital. The failure mechanism in a SC module exhibits failure modes that cannot be recognised from a single cell. Therefore, it is necessary that failure modes realised in a SC module be investigated in addition to failures of a single SC.

SC failure is investigated by determining the mechanism of failure which is caused as a result of electrical, mechanical or environmental stress. In this research, a lab scale test bench (is designed to accelerate SC failure by inducing environmental stress in the form temperature and voltage) is employed to identify and evaluate different ageing processes encountered in an EV.

6. **Supercapacitor model: Model that best describes SC electrical and electrochemical behaviour, through different ageing stages thereby capturing the complete ageing mechanism?**

   This research work goes further to explore possible SC models that describe its electrical behaviour and also represents the ageing evolution from life inception to potential EOL. The model, in the form of an electrical equivalent circuit (EEC), should be able to represent the physicochemical process in a SC and simulate current-voltage characteristics of a SC. It should also be able to cover a broad range of frequency and time constants, as the ageing effect in SC is usually observed after prolong operational period of months or sometimes even years. By representing all these properties, the model stands a chance in explain SC ageing mechanism during test operations and eventually optimising SC cell design for additional robustness.

1.2.3 Research Objectives and Delivrables

The main aim of this research is to envelop SC ageing process from inception to SC EOL. This process encompasses identifying and analysing failure mechanisms observed during operation by means of conventional characterization tests and also modelling the electrical behaviour of the SC. The knowledge acquired from this research is useful for the improvement needed in product development and reliability assessments. to achieve this goal, a few objectives have been drawn up and followed precisely;

- To analyse the effect of SC ageing factors one at a time before combining them together, so as to understand and distinguish between the ageing mechanisms of each ageing factor, thereby creating a baseline to explain the mechanism of SC failure in operation whereby more than one ageing factor is present. Prognosis of the interaction between the ageing factors is mandatory so as to understand the risk on SCs under operating conditions, thereby improving the design and safety of the SC cell.

- To distinguish and analyse the ageing mechanism between a single SC cell and 'SC module'. According to previous studies, results have shown a difference of ageing modes between single cells and module (Kötz, Ruch, & Cericola, 2010b). The failure pattern seen in SC modules is so abrupt that the mechanism of failure is mostly linked to the voltage imbalance between cells coupled with uneven temperature dispersion (Kötz et al., 2007)(Al Sakka et

al., 2009). Therefore, a suitable equalisation/balancing circuit was proposed and introduced to improve SC module performance. The failure mechanism is to be understood, analysed and compared between SC module with a balancing circuit and SC module without a balancing circuit within the span of this research work.

The deliverables below were provided to achieve the objectives presented in this research work

- A lab scale test bench (load based cycling system) is designed to carry out tests so as to investigate the degradation process of a supercapacitor by emulating a few operational modes with electrical motor load profiles.

- SC electrical performance is modelled with electrical equivalent circuits (EECs) which interpret the dynamic behaviour of SC and at the same time is also able to model the degradation process in the aged SCs. It is also able to relate the ageing mechanism due to electrochemical and structural changes in an aged SC to the EEC to understand how the ageing mechanism contributes to the failure in SCs.

1.2.4 Research Contribution

Study of SC lifespan with respect to the ageing mechanism is highlighted during this thesis as a preventive method of failure, and in so doing improves real product maintenance. This thesis emphasises a method of analysing ageing mechanism of SCs during operation conditions. If the ageing mechanism is analysed during operation conditions, it will be easier to identify the failure cause and mode in SCs, thus preventing impending failure, the moment it begins to show traces of degradation. During the span of this research ageing mechanisms are categorised under various operating conditions and are evaluated and cross-referenced against EV applications. Thereby, providing an added advantage of understanding SC's influence in EV applications. In addition to explaining the degradation process exhibited in each operating condition, a model developed using EEC aids in evaluating the ageing process through parameter regression (or in other words through the change in electrical parameters) from its precursor parameters.

1.2.5 Research Methodology

This research work was carried out by putting forward an approach to understanding the phenomena in SC EOL (or situations leading up to it) under strict operating conditions disclosed during this thesis. The study was aimed at (1) Understanding the causes and modes of SC ageing not only under standard testing conditions but also conditions that emulate specific modes in EV application. (2) Understanding and relating each cause of failure to the mode of failure and its failure effect on SC. (3)

Understanding voltage irregularity in SC module by embracing a balancing circuit as a course of action to improve/rectify ageing effects levied by voltage imbalance. (4) This research work can only be achieved, by resolving on a suitable method of identifying SC ageing effect by periodically monitoring the degradation process using a befitting tool to ensure the success of this research.

An experimental methodology was drawn up to satisfy the research questions presented in section 1.2.2, which have a few guidelines to follow: (1) this approach recommends an accelerated test to expedite SC ageing process under a suitable time frame for laboratory testing. (2) It also provides a platform whereby more than one ageing factor is tested at a time to study and understand SC ageing effect in EV applications (3) this methodology gives room for improvement by introducing an equalisation circuit to reduce SC ageing effect to some degree in a “module”. In as much as the balancing circuit was used to reduce the voltage imbalance in a module, a study on the effect with and without the circuit is eminent in order to determine ageing mechanisms and distinguish failure pattern in both scenarios.

This research work has collected a few techniques of measuring characteristic properties in SC behaviour from series of methods used in various literature for measuring SC behaviour. The few measurement technique adopted in this research were used periodically between calculated accelerated tests to monitor or observe SC behaviour (or in this case health) as particular SC characteristic properties degrade. The method of observation known as SC characterization collects data showing the gradual regression of SC parameter within a failure timeline.

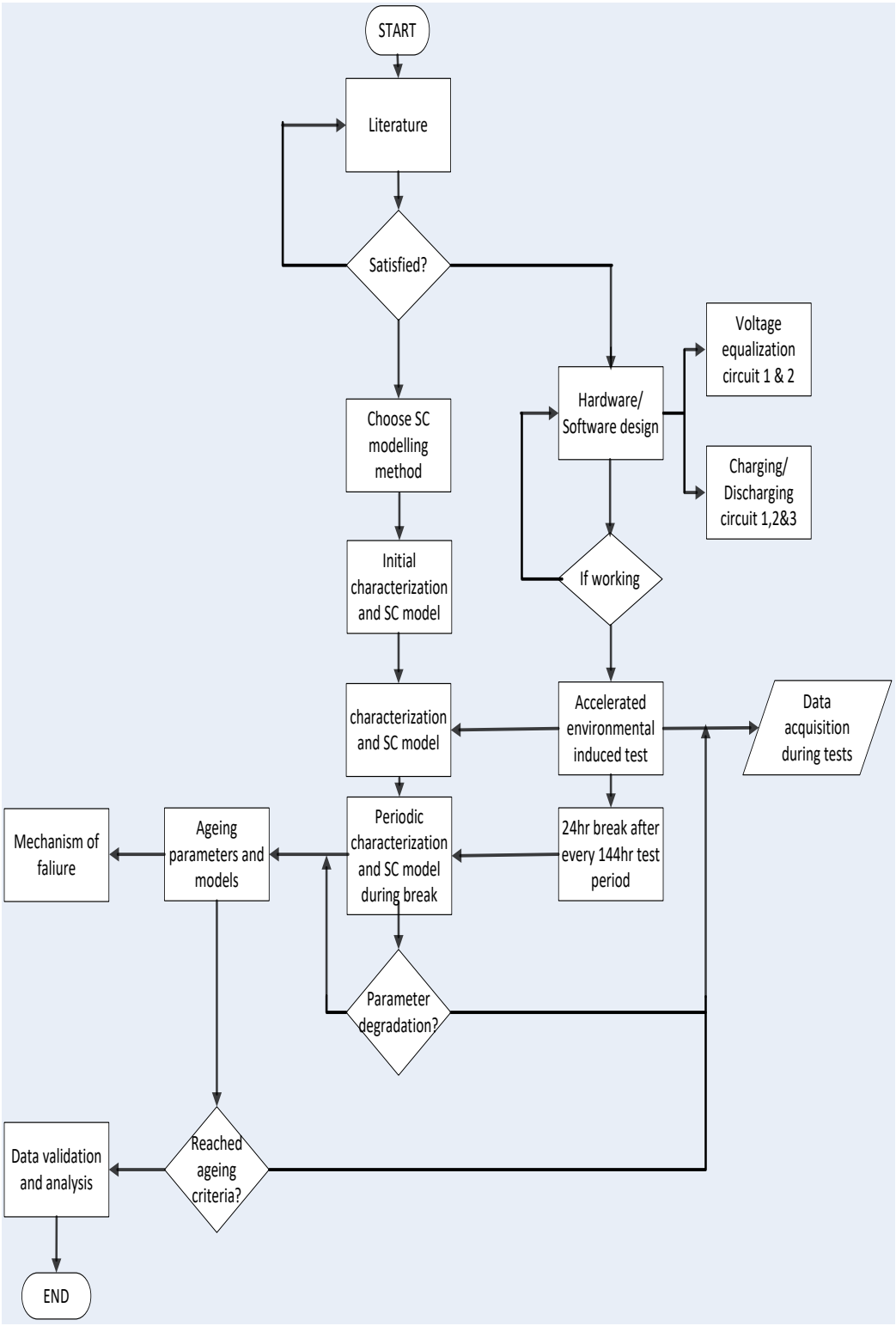


Figure 1-2: Research Methodology Flowchart

1.3 Scope of Thesis

This thesis investigates the ageing behaviour in both single SC cell and SC module. A commercial cell with a capacitance rating of 25F and a voltage rating of 2.7V was used throughout the experimental process. The commercial cell was limited to a single product developed by Maxwell Technology, the USA using carbon electrodes and acetonitrile organic electrolyte and packed in cylindrical packages. The SC was limited to only one product to minimise the difference in characteristic properties when more than one cell is combined in a module and also to provide a straight forward process in analysing SC life degradation with certainty.

Furthermore, this study only covers the wear out failures and ageing behaviour induced by external factors such as environmental stress and operational stress. Therefore, any ageing behaviour caused by internal faults related to the cell design and materials are not covered in this thesis.

The ageing behaviour explored in this thesis, are focused on thermal environmental and electrical operation. The temperature employed ranges between 75^{o}C-85^{o}C and this range was chosen based on the SC operating conditions and also the electrolyte boiling point temperature. This temperature range is believed to be a sufficient and practical enough to accelerate SC ageing process in a laboratory setting.

Ageing behaviour due to cycling test in concurrence with thermal stress described above was studied. Different cycling tests were carried out using different current profiles which were classified into experimental set-ups explained in chapter 3.

1.4 Thesis Outline

This thesis is made up of seven chapters in total, and brief introductions to the remaining six chapters are presented below:

- **CHAPTER 2**

  Chapter 2 is a compilation of literature research from previous work that relates to this research problem statement. This chapter starts with a background study on the main research material supercapacitor, from history, market predictions and trends, fundamental principle operational principle, the structural description, types of SC available in the market and the advantages/disadvantages of the supercapacitor technology. The chapter goes on to explain the theoretical principles behind supercapacitor modelling, types of models, supercapacitor sizing in a module and the advantages of introducing a voltage equalisation/balancing circuit to a supercapacitor module; with illustration recovered from various literature papers from previous research works. Finally, the chapter describes types of SC ageing test, ageing factors and failure quantification is extensively reviewed from different research methodological point of view.

  All the literature put together helped to envision the research focus and eventually draw up a methodology in chapter 3 to tackle the research issue. The chapter is concluded by ascertaining the research limitations observed in the literature reviews.

- **CHAPTER 3**

This chapter starts by explaining the importance of SC performance and reliability in EV operations, and why it is crucial to study SC End-of-life (EOL) with the purpose of identifying ageing mechanisms. This chapter proposes a step by step methodology of assessing SC failure as shown in the block diagram (Figure 3-2), which is divided into three stages. The first stage starts by characterizing parameters of the SC cells to establish an initial state of health, the second stage develops an initial model is developed using parameters found during characterization, and in the final stage the SC cells are subjected to accelerated tests (comprising of SC failure causes with respect to environmental and operation factors). These stages are repeated over and over again on a periodic basis to analyse SC degradation till the point where failure modes are established. Finally, SC life is predicted with the aid of developed failed models using parameters collected during characterization. The chapter explains in detail the accelerated tests, experimental set-up and the duration in which the tests are carried out. It also describes the equipment, materials, instruments, hardware and software used during the experiments. The chapter concludes with a brief explanation of the electrochemical characteristics and measurement techniques used throughout this research.

- **CHAPTER 4**

Chapter 4 of this thesis is on research design and testing. In this section electronic hardware supported with software (written codes) are employed to enforce proposed accelerated tests based on the working principle assigned to the experimental set-ups discussed in chapter 3. The chapter consists of designs on proposed equalisation circuits and three types of charge-discharge circuits; these circuit designs consist of both hardware and software. After design completion, the chapter goes further to implement testing protocols using the research methodology and also document test profiles representing the accelerated tests categorised by their experimental set-up in chapter 3.

- **CHAPTER 5**

Chapter 5 is divided into two parts;

In the first part, different techniques of measuring SCs were presented, and the alarming dissimilarities reported by the results from these techniques prompted an investigation to identify the most suitable measuring method for this research work. Identifying the measurement technique started with a survey on methods developed by SC manufacturers, and then, those methods were tested and their results compared to choose the appropriate measuring method and test setting best suited for this research.

The second part of this chapter deals with modelling SC electrical properties. Methods of modelling using under time and frequency domains were explored in this chapter and a suitable choice using a reliable method of parameter characterization and collection was selected. At this chapter, an initial EEC model was developed to represent SC electrical properties, which is later improved in the subsequent chapter to envelop SC ageing behaviour.

- **CHAPTER 6**

In this chapter results gathered from the accelerated ageing tests on the SCs are presented and discussed in details, it also goes a step further to develop models representing those ageing factors.

At first, the chapter studies the effect of environmental and operational stresses on the SCs ageing behaviour. That is, the effect caused by high temperature, constant voltage, constant current cycling with and without equalisation/balancing circuit, various charge-discharge profile with and without a motor load were studied individually to distinguish the ageing mechanism in relation to these ageing factors. The changes to the state of health and properties of the SCs are monitored periodically in the periodic characterization tests. The results from electrochemical measurements are compared to the SC electrical performance to find the correlation between the ageing processes to the decline performance in SC. From the isolation of the ageing factors, this chapter identifies the ageing signature of each factor and hence, identifies the primary contributor to the deterioration performance.

In addition to the results gathered in this chapter, models representing each ageing factor are developed based on their ageing mechanisms. Model evolution from the initial model developed in chapter 5 to the aged model is illustrated in this chapter, thus representing the changes in the state of health of the SCs. Since the initial model and the aged models are in the form of electrical equivalent circuit model, which makes simulations of the current-voltage characteristic of these models in time domain is possible.

- **CHAPTER 7**

The concluding chapter of the thesis, it summarises the research work presented in the whole thesis and reiterates the research questions to confirm that appropriate answers were provided and understood to some certainty. It also discusses this research works limitations and provides ideas for future improvement.

CHAPTER 2 - LITERATURE REVIEW AND THEORY

2 Outline

Chapter 2 is a compilation of literature research from previous work that relates to this research problem statement. This chapter starts with a background study on supercapacitor SC, from history to future predictions, structural description and the advantages/disadvantages of the SC technology.

The chapter goes on to explain the theoretical principles behind supercapacitor modelling, sizing of supercapacitor module and the benefits of introducing a voltage equalization/balancing circuit to a supercapacitor module; with illustration recovered from various literature papers from previous research work

Finally, Supercapacitor ageing causes and effect, accelerated test methods with ageing factors, failure quantification, and ageing models are extensively reviewed from different research methodological points of view.

All the literature put together helped to recognize the research focus which eventually assisted in drawing up a methodology (in chapter 3) to tackle the research problem.

2.1 Supercapacitor: Generation

Electrostatic and Electrolytic capacitors are known as the first and second generation capacitors. These conventional capacitors were developed centuries ago primarily for low power applications such as memory backup supplies or analogue circuits due to their low capacitance charge ranging from microfarads to Pico farads (Cingoz, 2012). Conventional capacitors have been in existence since a philosopher called Thales of Miletus discovered electric charges when he rubbed amber with a cloth and observed magnetic particle attraction. That event led to the triboelectric effect which demonstrated the effect of rubbing two non-conducting materials (Yu, Chabot, & Zhang, 2013). In 1745, a better understanding of electrostatic and electrochemistry led to the invention of a condenser which evolved into better structural capacitors in the twentieth century when they were redesigned to a more practical and economical means of storing electrostatic charges that are now used in electrical systems.

With Rapid development in materials featuring high surface area and low resistance, a third generation capacitor with the capability to store relatively higher energy in the form of electric charge was produced. The third generation capacitor trade name has been known by many manufacturers to vary from; Dynacaps, gold capacitors,

electrochemical double layer capacitors (ELDC), Ultra-capacitor, to Supercapacitor (SC) (Atcitty, 2006), (Namisnyk, 2003). However throughout this thesis, the term supercapacitor SC which is a widely used trade name (verified by Nippon Electric Company (NEC)) is easier to identify with and therefore used.

2.2 Energy Storage System

Energy consumption is one of the biggest challenges that our society face today, and with the increasing depletion of fossil fuel coupled with its harmful effect on the environment when consumed; researchers are focusing their attention on greener solutions such as renewable and clean energy sources to replace fossil fuel (Trust, 2006). Various devices are under development for storing energy, such as batteries, conventional capacitors, fuel cells, supercapacitors, etc. Supercapacitors have aroused more interest in recent days, and so this research will focus on this subject. An ideal energy storage device should provide high energy in a short time i.e. high power density, and should also store and deliver large amount of energy i.e. high energy density.

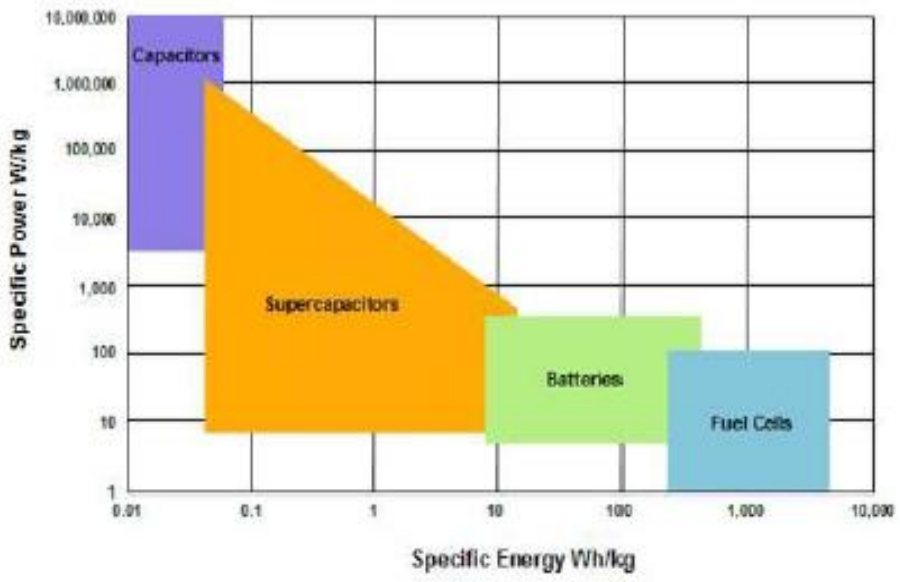


Figure 2-1: The Ragone plot of different energy devices (Ko & Carlen 2000)

The Ragone plot in Figure 2-1, which represents a device's energy and power capabilities places SCs in a position with an added advantage to storing a larger amount of energy than conventional capacitors, while preserving higher power densities than batteries and fuel cells. SCs among its pairs, have shown a lot of potential in applications such as memory backup, quick charge, battery life improvement, and uninterrupted power supplies (Y. Kim, 2003), and as a result, this has drawn significant attention from researchers, especially in transportation, i.e., HEVs, buses and power-trains and electric utility applications (Smith, Ieee, Sen, & Ieee, 2008).

2.2.1 Advantages and Disadvantages of Supercapacitors in Energy Storage Systems

A. ADVANTAGES

Supercapacitor as an energy storage device possesses favourable advantages when compared to the other devices, as categorized below:

- **Energy and Power Density**: Regarding energy density, existing commercial SCs have ranged from 1 to $10Wh/Kg$ (Gao, Dougal, Member, & Liu, 2005). The average power density of SC ranges from 1000 to $5000\ W/kg$, while the energy density is limited to about $30Wh/kg$ (University, 2003) which is $1/10$ to $1/100$ less than the energy of batteries and fuel cells respectively.
- **High Efficiency**: The Columbic efficiency (is defined as the ratio of the number of electrons discharge to the number of electrons that need to be recharged to bring an energy storage device back to its original state of charge) (Y. Wang, 2008). SCs have high columbic efficiency of about 99% (Technologies, 2006) as well as high trip efficiency. (Trip efficiency is defined as the ratio of electrical energy produced after charging and discharging the storage system to the electrical energy required from the charging source.) The trip efficiency implies that SCs use less cooling system since it dissipates less energy heat.
- **Low ESR**: SCs can be charged with a very high pulsed current as a result of its low ESR. In addition to that, no chemical reaction is involved in energy storage and charge/discharge of SCs. This means that charging and discharging can be

done with the same high rated current, an advantage that supports regenerative braking application.

- **Temperature**: SCs operate over a wide range of temperatures from -40° to 85° (Company, 2014). The operating temperature of a SC is determined by the electrolyte. If the temperature is low, the mobility of the ions in the electrolyte is also low, except for cases whereby the temperature reaches freezing point which deteriorates the ions' kinesis in the electrolyte. Moreover, when the temperature is high, the mobility of the ions also increase.
- **Cycle life**: Standard specification for the end-of-life (EOL) of SCs is explained by a 20% decrease in capacitance and an increase in ESR by 100%. During operations, SC performance gradually degrades, and its life ends when its performance no longer satisfies the application. A typical SC is good for several hundred thousand charging/discharging cycles.
- **Environmental friendly**: SC operation involves no chemical reaction; therefore it produces no environmental pollution. The use of SCs in electric vehicles EVs improves the fuel economy and decrease vehicle emissions throughout the lifecycle of the vehicle.
- **Safety**: In the case of a short of the SC terminals during operations, the SC will not be damaged. However, immense heat will be created along the short, as enormous amounts of current are quickly dissipated. This rapid increase in temperature within the SC could be considered a limitation regarding life span and is obvious by, the burning sensation observed by the user (EngineeringShock).

The advantages mentioned above makes the SC a unique fit for applications that require pulse power, such as a bust-mode communication for wireless systems, writing to disk and LCD operation for digital cameras, and starting vehicles (Y. Wang, 2008).

B. DISADVANTAGES

- **High Self-discharge**: The self-discharge of a SC is substantially higher than that of an electrostatic capacitor and somewhat higher than the electrochemical battery. The organic electrolyte contributes to this. The stored energy of a SC decreases from 100 to 50 percent in 30 to 40 days.(University, 2003)
- **Low voltage rating**: The main disadvantage of SCs is their inability to withstand high rated voltage. The maximum voltage of a SC is by far lower than the required voltage in most SC related applications especially automation systems. To achieve such energy, SC single cells must be connected in series to form a 'module'.
- **Over-Voltage**: However, a SC module is not without limitations, as the variations in any individual SC cell in terms of manufacturing tolerance causes a major system failure (Technologies, 2006). In a module, SC cells with smaller capacitances generate larger terminal voltage, which causes some cells to go beyond the rated voltage more quickly than others when charging the module. Similarly, when discharging a module, different SCs develop different terminal voltages, and some may even have potentially negative terminal

voltages. It is dangerous to operate cells at negative terminal voltages or terminal voltages higher than their rated maximum; accordingly, care must be taken in the control of series-connected SC module (Yi Zhang, Wei, Shen, & Liang, 2009). Over-voltage is a major disadvantage in SC applications. Therefore, this research will apply particular interest in this area. This limitation is later addressed and discussed in further in this chapter.

- **Cost**: SCs are expensive in terms of cost per watt. Some design engineers argue that the money on SCs should rather be spent on a larger battery. However, it important to recognize SCs and chemical batteries are not in competition with each other; rather they are different products serving unique applications (University, 2003).

2.3 Capacitor Classification

Capacitors are divided into three classes as shown in figure 2-2 namely; Electrostatic, Electrolytic and Electrochemical capacitors.

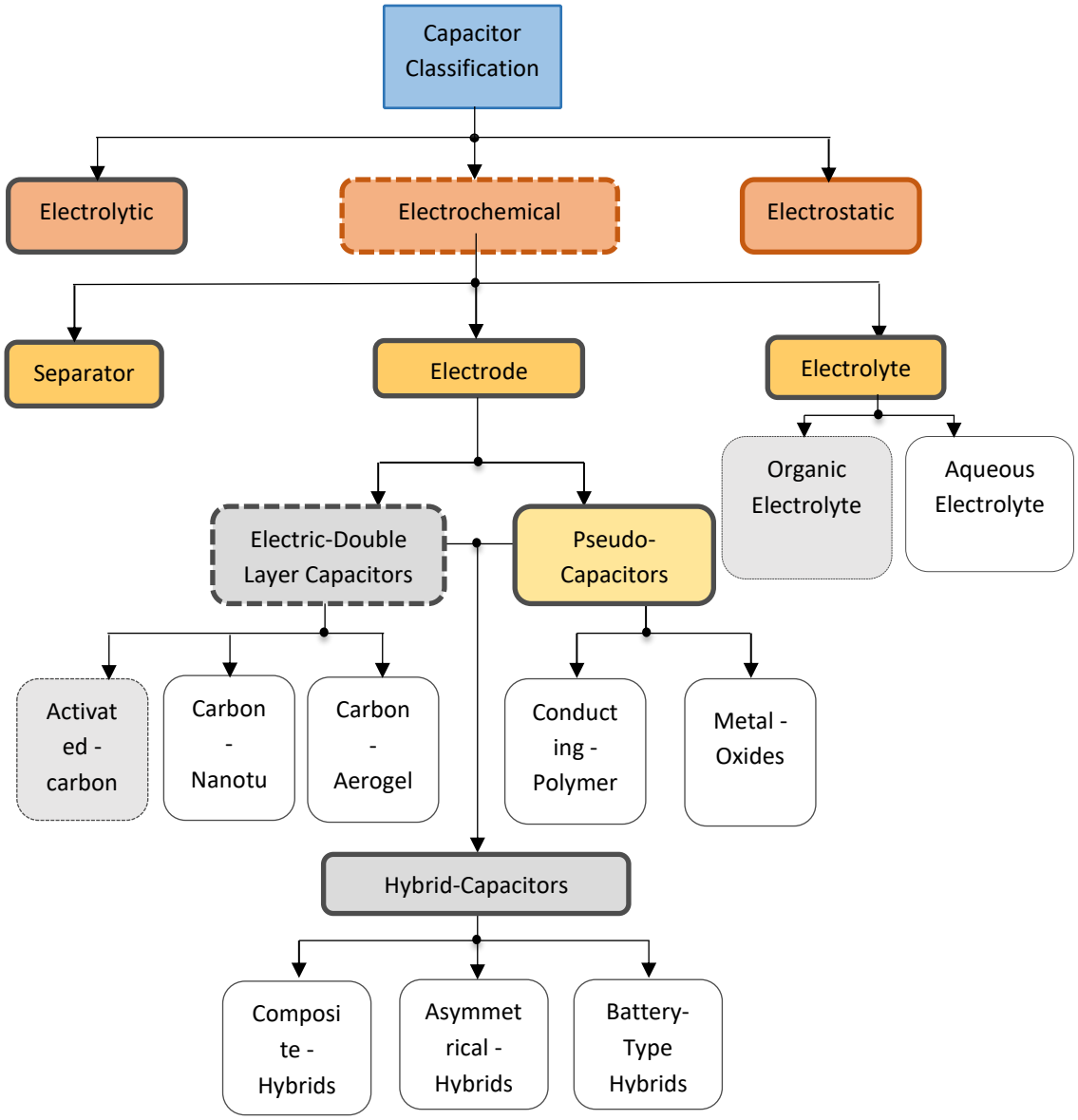


Figure 2-2: Classification of capacitors grouped into capacitor structure gathered from (Sharma & Bhatti, 2010) (Peng, Zhang, Jewell, & Chen, 2008) (GRBOVIC, 2010) (Atcitty, 2006)

A. Electrostatic Capacitors

Electrostatic capacitor is the first generation fundamental electric circuit elements that store electrical energy in the order of microfarads and assist in filtering. They are made up of two metal electrodes (parallel plates) separated by a dielectric as shown in Figure 2-3a. The dielectric is nothing but a non-conducting material that is inserted between the parallel plates of the metal electrode material (Sharma & Bhatti, 2010). This class of capacitor has two main applications; it is mostly used to charge or discharge electricity, and secondly, as a function to block the flow of DC current especially in circuits where excellent frequency characteristics are required (Jayalakshmi & Balasubramanian, 2008).

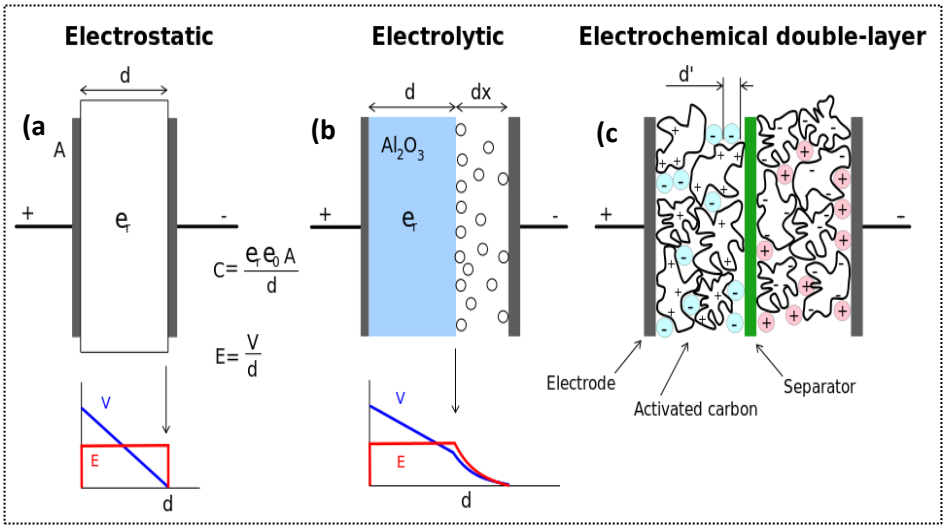


Figure 2-3: Cell construction diagram of the three classes of capacitors; (a) Electrostatic Capacitors, (b) Electrolytic Capacitors and (c) Electrochemical double-layer Capacitors, adopted from (Zurek 2006)

B. Electrolytic Capacitors

Electrolytic capacitors are the next generation capacitors with similar cell construction to electrostatic capacitors but have a conductive electrolyte salt in

direct contact with the metal electrodes(Sharma & Bhatti, 2010). The polarized capacitor is classified into three metallic families; Aluminium, Tantalum, and niobium capacitors. The cell structure is made up of an anode metallic electrode in which an insulating oxide dielectric layer is created by anodization (forming), and a solid/liquid electrolyte which covers the surface of the oxide dielectric layer in principle serves as the second cathode electrode of the capacitor. (Hillman & Helmold, 2004)

C. Electrochemical Capacitors

Electrochemical capacitors (EC) are third generation capacitors with higher energy density than electrostatic and electrolytic capacitors, due to their porous electrode structure. At the macroscopic level, electrochemical capacitors have very high electrode surface area as large as $1000-2000\ m^2/cm^3$ (Bakhoum & Member, 2009) (Bard & Faulkner, 2001) (Ko & Carlen, 2000) due to the porous electrodes and very small separation between the electronic and ionic charge at the electrode surface. EC are grouped into two major categories, namely symmetric and asymmetric based on their electrode material. Symmetric Electrochemical capacitors (referred to as SECs) use the same electrode material for both the positive and negative electrodes, while Asymmetric Electrochemical capacitor (referred to as AECs) use two different materials for the positive and negative electrodes. SECs as illustrated in Figure 2-2 are further divided into two classes; namely electric-double layer capacitors (EDLC) and Psuedo-capacitors, while AECs is a hybrid combination of EDLC and pseudo-capacitors to help increase energy density by increasing the capacitance beyond that of SEC through

redox reaction (Jayalakshmi & Balasubramanian, 2008) of the electrode materials such as composite-hybrids, asymmetric-hybrids and battery-type hybrids to name a few as illustrated in Figure 2-2. However, SECs is the main area of focus in this project, and their electrostatic charge is formed from the accumulation and separation of ions at the interface between the electrolyte and electrodes. The electrolyte solution comprises of either aqueous substances (such as potassium hydroxide or sulphuric acid) or organic substances (such as acetonitrile or propylene carbonate).

2.3.1 Structure of Supercapacitor (EDLCs)

SC device consists of two electrodes enveloping an electrolyte solution so as to allow a potential to be applied across the cell, which forms a double layer structure, one at each electrode/electrolyte interface as shown in Figure 2-3c (Electrochemical double layer structure). An ion-permeable separator is placed between the electrodes to prevent electrical contact, but this still allows ions from the electrolyte to pass through. High energy densities are therefore achievable in SCs due to their high specific capacitance, attained because of a high electrode/electrolyte interface surface area and a small charge layer separation of atomic dimensions (Namisnyk, 2003).

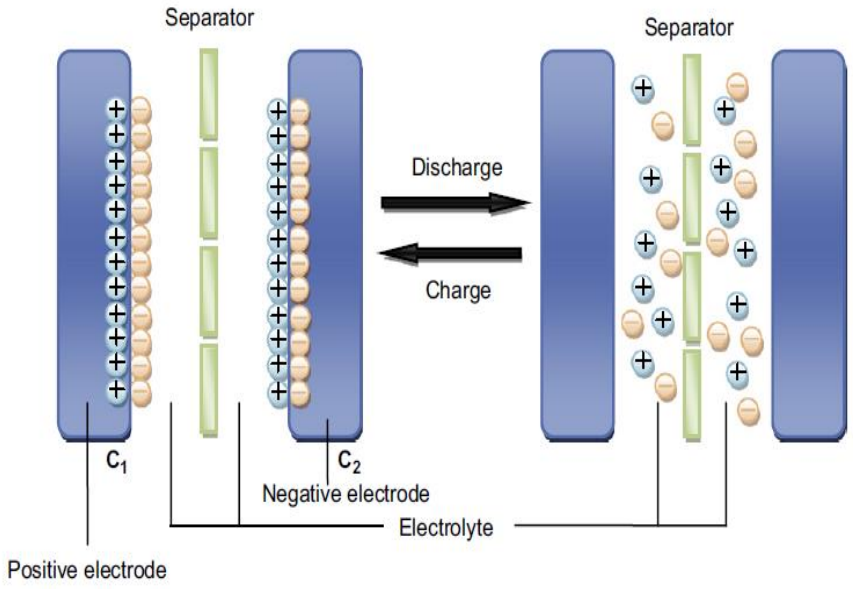


Figure 2-4: Representation of an electrochemical double layer capacitor (in its charged and discharged state) adopted from (Xin Li & Wei, 2013)

2.3.1.1 Electrode Material

The most common electrode material is carbon, due to its low cost, large surface area, excellent electrical conductivity, high power density easy production technology and high electrochemical stability (H. Gualous, Bouquain, Berthon, & Kauffmann, 2003) (Cingoz, 2012) (Bai, Du, Chang, Sun, & Gao, 2014). Carbon materials are produced through carbonization and activation procedure, and they exist in different forms, which include the most widely used activated carbon (AC), carbon black, carbon aerogels, carbon nanotubes (CNTs), and graphene (Lipka, 1996) (Pandolfo & Hollenkamp, 2006) (Volfkovich, Bograchev, Mikhalin, & Bagotsky, 2013). Activated carbons are made from very small carbon-rich natural particles, for example, coconut shells, wood or coal, or synthetic materials like polymers, which in bulk forms a low-density volume of particles with pores between them that resemble a sponge (Do, 2004) (Simon & Gogotsi, 2008).

It is well known that the performance of carbon materials as EDLCs is strongly dependent on factors such as the specific surface area, pore size distribution (PSD), particle size, electrical conductivity, and surface chemistry (Sun, Wang, Zhou, Zhang, & Qiu, 2013). Among these factors, the surface area of electrode plays an essential role on SCs, and empirical evidence suggests that not all of the high surface area contributes to specific capacitance, though it is directly proportional to its surface area. Therefore capacitance is not only influenced by surface area, but also, the ability for electrolyte ions to interact with the electrode plates. Activated carbons are produced by thermal or chemical treatment of carbonaceous materials to increase their surface area.

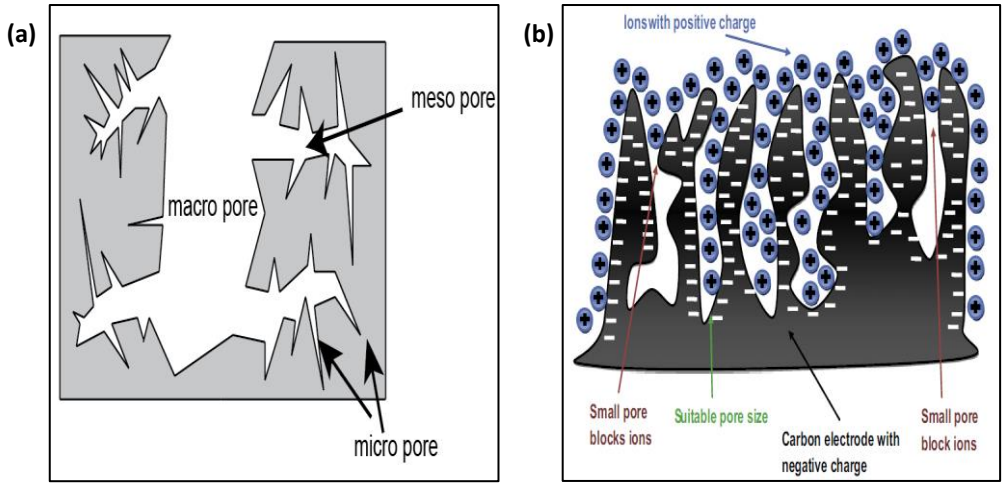


Figure 2-5: SC Electrode material; (a) Conceptual scheme of pore of activated carbon. Adapted from (Itagaki et al., 2007) and (b) Schematic of the ion size and pore size effect on nanoporous carbon electrode. Small pore blocks the ion from penetrating inside the pore to fully utilize all the surface area, while a suitable pore size facilitates the ion migration to form EDLCs adopted from (Xin Li & Wei, 2013)

The mobility of electrolyte ions in electrode material depends on the porosity of the electrode material. The porous structure of the activated carbon consists of micropores (diameter < 2 nm), mesopores (diameter from 2 – 50 nm) and macropores (diameter > 50 nm) as represented in the Figure 2-5a (Pandolfo &

Hollenkamp, 2006) (Cingoz, 2012). As seen in Figure 2-5b, electrolyte ions that find it difficult to penetrate smaller micropores (although increasing the electrode surface area), minimize the mobility of the ions to other pores, hence limits the capacitance charge value. As a result, when fabricating a SC, it is important to select a pore structure that compliments the electrolyte solution in such a way, it increases ion mobility while maintaining a large surface area electrode (Glavin & Hurley, 2007).

The size of electrode pore also has some form of influence on the energy and power density of the SC. The conductivity of the electrode material has a direct influence on power density, but inversely proportional to particle size. Although the small particles are desirable for higher capacitance, they increase the internal resistance, which limits the power density. Power density can be increased with activated carbon electrodes possessing larger pores. On the other hand, it will decrease available charge storage due to reduced surface area (Namisnyk, 2003) (Cingoz, 2012).

2.3.1.2 Electrolyte

SC operating voltage window is limited by the type of electrolyte used. There are two most widely used electrolytes in SCs; i.e. aqueous and organic electrolytes. The third type of electrolyte is the Ionic liquid (IL), which is not discussed in this thesis. The pie chart in Figure 2-6 shows the percentage of manufacturers using organic, aqueous and IL in their SCs.

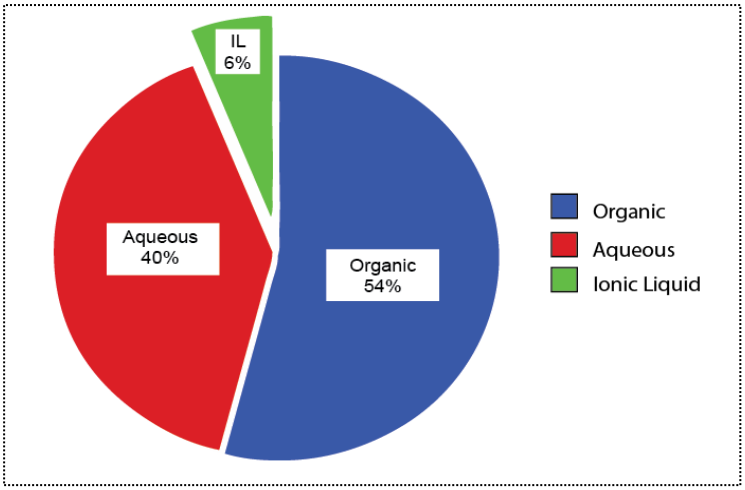


Figure 2-6: The percentage of supercapacitor manufacturer using organic, aqueous and IL electrolytes. Adapted from (Harrop et al., 2013), (Naim, 2015)

Listed under the aqueous group electrolyte are H_2SO_4, KOH, Na_2SO_4 and NH_4Cl. The aqueous electrolyte has high ionic concentration and low resistance. SCs utilizing this type of electrolyte have higher specific capacitance and higher specific power than SCs utilizing non-aqueous electrolytes. Moreover, aqueous electrolyte is low in cost (Béguin & Frąckowiak, 2013). However, aqueous electrolyte has a small voltage window due to its low decomposition voltage which can be as low as 1.2V. Recently, Ratajczak et al. have demonstrated that SC using Li_2SO_4 aqueous electrolyte can operate up to 1.5V, higher than 1V, that is typically attained by KOH and H_2SO_4 aqueous electrolyte (Ratajczak, Jurewicz, & Béguin, 2013).

Organic electrolyte, on the other hand, has higher decomposition voltage, as high as 3.5V (G. Wang, Zhang, & Zhang, 2012). Aqueous low decomposition voltage makes it harder to improve SC energy and power densities because a higher operational voltage will generate a greater specific energy; this is why organic electrolyte is preferred in commercial SCs and high-energy applications. The only drawback is that organic electrolyte has a higher resistance than the aqueous electrolyte. Under the

organic electrolyte group, there are propylene carbonate (PC) and acetonitrile (AN) solvents. PC-based electrolytes are environmentally friendly but suffer at low temperature. Whereas, AN-based electrolytes can dissolve larger amount of salt (G. Wang et al., 2012), but are toxic to the environment. Nevertheless, AN-based electrolytes have excellent low-temperature performance than PC-based electrolytes (Liu, Verbrugge, & Soukiazian, 2006).

In organic electrolytes, salts are dissolved in PC or AN solvents. The most common salts are tetraethylammonium tetrafluoroborate ($TEABF_4$) and triethyl methylammonium tetrafluoroborate ($TEMABF_4$). Nevertheless, Ionica-Bousquet et al. (2010) have demonstrated that polyfluorododecarborate-based salts, usually used for Li-ion batteries, can be used in SC to reduce solvent degradation under harsh conditions, thus extending cell life. (Ionica-Bousquet et al., 2010)

2.3.1.3 Separator

A separator is used in the fabrication of SCs to prevent electrical contact between the two electrodes. Separators are porous membrane that is ion-permeable to allow ionic flow across the separator and into the electrode (Ko & Carlen, 2000). SC Separators utilizing organic electrolytes are usually cellulosic papers. Glass fibre separators are also used, often with aqueous electrolytes (Sharma & Bhatti, 2010).

The separator does not participate in the cell reactions, but its properties can affect SC performance. Presently, there is not much discussion on SC separators that can be found in literature. Nevertheless, the effect of separator thickness on SC resistance

has been studied by Stoller and Ruoff (2010) (Stoller & Ruoff, 2010a). A thicker separator yields higher resistance because it increases electrode spacing. Therefore, a thinner separator is preferred; however, it must have adequate strength to withstand the pressure of being wound up, in particular, during the construction of cylinder-typed SCs.

2.3.2 Supercapacitor Models

The interaction that occurs at the boundaries between the electrodes, electrolyte and separator in a SC system exhibits a dynamic behaviour that needs to be understood. Various models over the years have been developed to understand the fundamental processes underlying SC system and explain the phenomena between the structural interactions at the boundary parts. Not only that, the scientific community has exploited this mode of research to predict the performance characteristic of SCs, which has entirely reduced the time and costs for fabrication and physical experimentation.

The early works of Helmholtz (Sharma & Bhatti, 2010)(Simon & Gogotsi, 2008), Gouy-Chapman (Hossain & Adamiak, 2013), Stern- Graham models (Grahame, 1947) (Mitsugi Senda, Takashi Kakiuchi, Toshiyuki Osakai, 1987)(Kazarinov, 1987) have contributed a great deal to the emergence of block models built either analytically, experimentally or numerically. These block models were usually modelled on a macro-scale and studied in frequency and/or time domains (Dănilă, Luchache, & Livint, 2011), which could be grouped as: electrical model (Ban et al., 2013), thermal

model (Hamid Gualous, Louahlia-Gualous, Gallay, & Miraoui, 2009) (Al Sakka, Gualous, Van Mierlo, & Culcu, 2009a), electrochemical model (Martín, Quintana, Ramos, & de la Nuez, 2008), black box model (A. Eddahech, Ayadi, Briat, & Vinassa, 2013), mathematical model (Srinivasan & Weidner, 1999) (Lin, Ritter, Popov, & White, 1999) and Artificial Neural Networks model (ANN) (Zhao, Li, Zhang, & Liu, 2010) etc. Nonetheless, modelling the SC by means of deriving its equivalent circuit is still a preferable choice, not only does it represents SC conceptually through the arrangement of circuit elements, it can also be implemented in hardware which could replicate the actual behaviour and produce the same impedance response as the system under study.

In SC applications, a developed equivalent model which reflects and predicts the electrical and performance behaviour of SCs is important to characterize the SC based power system such as Zhang et al. (2009); Y. Y. Yao, D. L. Zhang, Member, IEEE, and D. G. Xu, Member (2006). A capacitor is often modelled with a single ideal capacitor connected in series with an ideal resistor (RC circuit); the ideal resistor represents an ESR that prevents the modelled capacitor from behaving like an ideal capacitor. RC model could also be used to model the electrical response of a SC. However, this model is too simplified and has proven to be insufficient when modelling SC long-term behaviour. This is attributable to the nature of the porous electrode itself. As the surface area of the porous electrodes consists of pores of various sizes, it is only rational that the SC is modelled by a lumped parameter model (theoretical representation of equivalent circuit) consisting of an infinite number of non-linear RC branches represented in Figure 2-7 (Belhachemi, Rael, & Davat, 2000). With the capacitance (voltage dependent) representing the negative and the positive

electrodes in the activated carbon fibres, the resistance (charge diffusion) corresponds to the electrode material, the electrolyte material, the membrane material and the various sizes of pores.

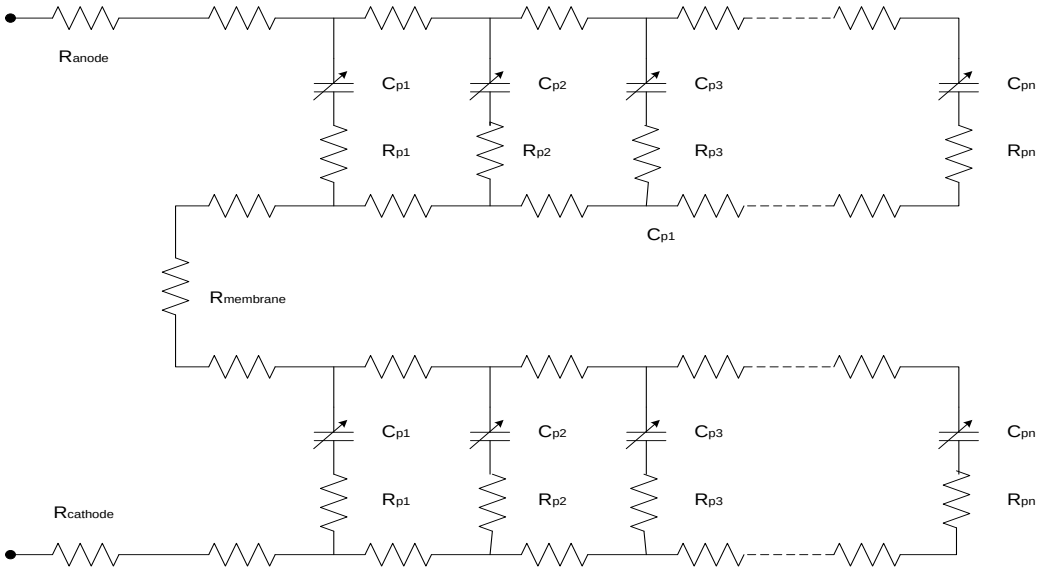


Figure 2-7: Supercapacitor theoretical model which comprises of infinite non-linear capacitors and resistors. Figure adapted from (Belhachemi et al., 2000)(Faranda, Gallina, & Son, 2007)

Although this model represents the physical structure and demonstrates the physical phenomena of SCs, it is rather impossible to implement it in practice because of its complexity.

More simplified models proposed by researchers are developed using a temporal approach (Belhachemi et al., 2000) (Yang, Carletta, Hartley, & Veillette, 2008) or a frequency approach (Itagaki, Suzuki, Shitanda, Watanabe, & Nakazawa, 2007)(Du & Province, 2009) or a combination of both temporal and frequency approach like in W. Lajnef, J. M. Vinassa, et al. (2007), Rizoug et al. (2010) of parameter identification. Temporal approach simulates SC behaviour during charge/discharge cycle using a constant current to determine the model parameters, whereas the frequency

approach uses Electrochemical Impedance Spectroscopy (EIS) to identify the model parameters. Existing SC models can be categorized into four basic classes: RC parallel branch models, RC series-parallel branch models, RC transmission line models and RC ladder network models (horizontal and vertical). Each model category can be further extended to include both linear model (constant resistor and capacitor components) and non-linear models (nonlinear resistors and capacitors which may also be the functions of SC electrolyte temperature and terminal voltage) (Shi & Crow, 2008).

Figure 2-8 represents RC branch models, with both serial and parallel connections. Model Figure 2-8a and Figure 2-8b illustrates an ideal SC model, which gives a weak description of SC behaviour under various operating conditions. More efficient models, i.e. Figure 2-8c and Figure 2-8d were later proposed by researchers to describe the SC behaviour better (with one RC branch representing SC short-term behaviour and three to five RC branches representing SC long-term behaviour depending on the specific application). Faranda and Zuibeta later, proposed a non-linear RC parallel model with two branches (Faranda, 2010) and three branches as shown in Figure 2-8e (Zubieta & Bonert, 2000) to account for the temperature effect in SC under operating conditions, or four-branch (Lajnef, Vinassa, Azzopardi, & Zardini, 2004) equivalent circuit model. These models represent the SC's short-term, medium-term and long-term behaviour.

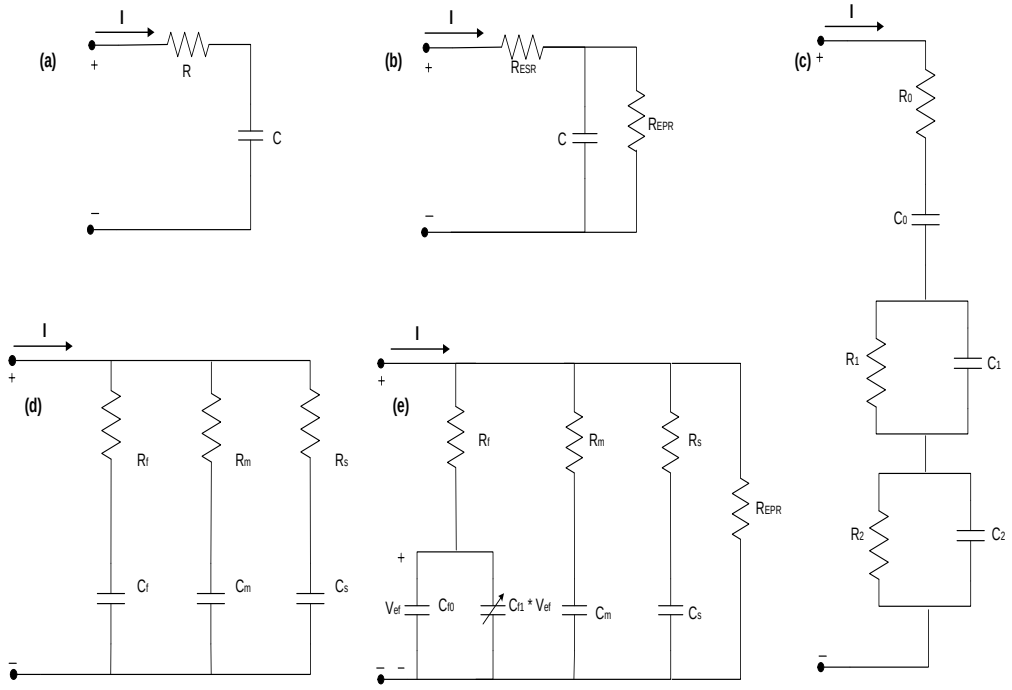


Figure 2-8: Electrical equivalent models of a supercapacitor: (a) RC simple SC model (b) RC series equivalent circuit (c) Three RC series-parallel branch model (d) Three RC parallel branch model (e) Three RC parallel branch model (Zubieta and Bonert model) (Zubieta & Bonert, 2000), appeared in (Dănilă et al., 2011; Shah, Kundu, & Maheshwari, 2012)

The transmission line model (Figure 2-9a) based on De Levie's porous theory can be rather challenging as it often requires between 4 to 20 RC orders to achieve a satisfactory accuracy (Lajnef, Vinassa, Briat, Azzopardi, et al., 2007). Although this equivalent circuit model is developed based on the assumptions that the pores are cylindrical, it is still commonly used to describe SC distributed characteristic and charge propagation along the electrode surface and its complex internal geometries (H et al. Song, 1999). In literature papers, transmission line models have been successfully applied to charge/discharge behaviour of a range of SC materials. However Fletcher et al. in (Fletcher, Black, & Kirkpatrick, 2013) argued that the transmission line model is only viable with SC materials containing pores whose diameters are uniform; such as conducting polymers (Fletcher, 1993), metal oxides

in dye-sensitized solar cells (Juan Bisquert, 2002), and corrosion films (Macdonald, 2009), but not so accurately with SC materials whose pores are neither identical nor uniform, such as activated carbons used in EDLCs.

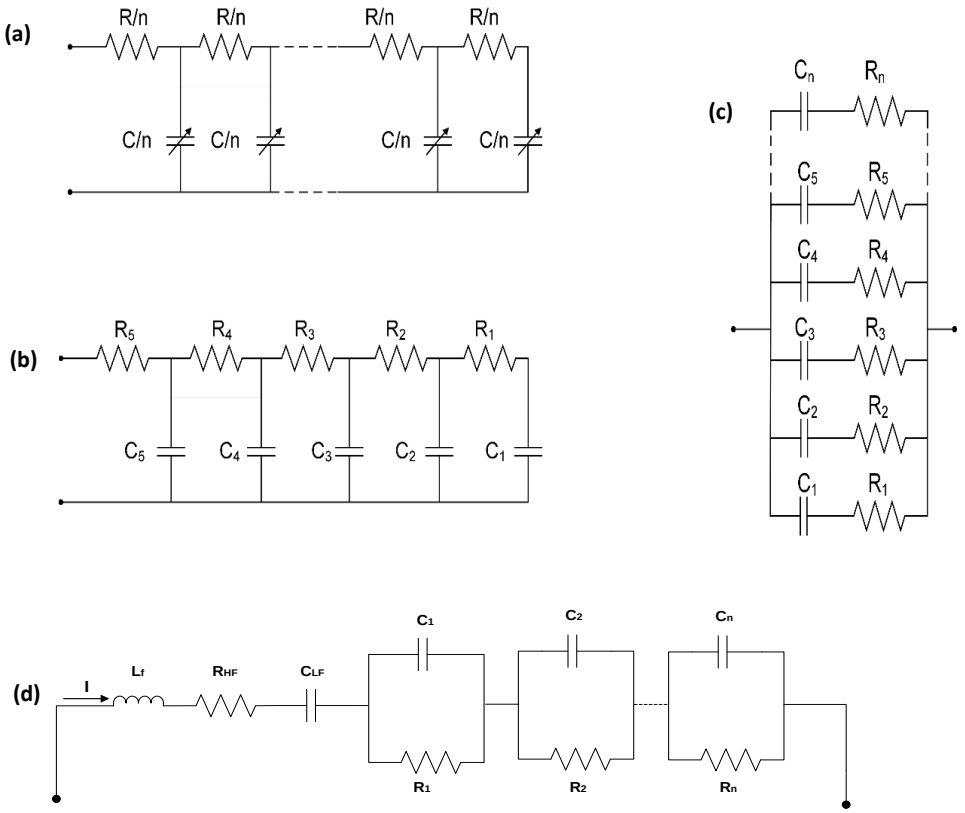


Figure 2-9: (a) A transmission line model as appeared in (Nassim Rizoug et al., 2012)(Lajnef, Vinassa, Azzopardi, Briat, et al., 2004); (b) a horizontal ladder network model as appeared in (Dougal et al., 2004); (c) a vertical ladder network as appeared in (Fletcher et al., 2013); and (d) a multi R-C branch model in Voigt topology (A dynamic model developed by (N Devillers et al., 2014)).

RC ladder network model is another type of SC model studied in papers by Nelms et al. (2003), Dougal et al. (2004), Li & Crow (n.d.) and most recently by Fletcher et al. (2013), to mimic the distributed nature of the resistance and capacitance in a porous electrode. Ladder network models are formed by resistances and capacitances that are connected in series and parallels; they can take either a horizontal form (Figure 2-9b) or a vertical form (Figure 2-9c). A higher order circuit, between 3 to 4 orders

(Nelms et al., 2003), fits SC transient behaviour better. In addition to that, five-stage ladder model has been recommended by Dougal et al. (2004) for most applications that require frequency range up to 10kHz.

The idea behind ladder network models lies on the different time constant of SCs dynamic behaviour. Some researchers have shown that the frequency model of the transmission line can be simplified by a multi R-C branch Figure 2-9d. This method was explored by Buller et al. (2002), Moss et al. (2007), Riu & Retière (2004), N Devillers et al. (2014**),** Tironi & Musolino (2009) and Kulsangcharoen et al. (2010), to provide an accurate model on the dynamic behaviour of the SCs. The time domain representation of this circuit can be obtained by taking the inverse transformation of the impedance spectra in frequency domain. The transformation of this model to the time domain model is shown extensively in Buller et al. (2002).

Building a model that can simulate SC behaviour at wide frequencies often requires the extension of circuit branches until a good accuracy is achieved, which leads to many parameters to be identified. Some researchers have explored a method based on separating the model according to the frequency range or the time constant at interest. For instance, Du & Province (2009) and El Brouji, Briat, J. M. Vinassa, et al. (2009) proposed both high frequency range models and low frequency range models, while Musolino et al. (2013) experimented with a model that represented SC behaviour at both low and high frequency for better model accuracy.

Nathalie Devillers et al. (2014) reviews showed that a dynamic model is more accurate than other types of model in representing the transient behaviour of SCs. The dynamic model was aimed at modelling at a microscopic scale over a very wide

frequency range. Unlike those equivalent circuit model mentioned previously, which do not necessarily represent the physical phenomena in the SC, the dynamic model is built in a way that it should be able to represent the internal phenomena with precision. The dynamic behaviour of SCs takes place in a wide frequency range, and it is influenced both by internal and by external parameters. This wide range is caused by different electrochemical effects, such as mass transport, the electrochemical double layer, and simple electrical effects. The duration for this dynamic behaviour is illustrated in Figure 2-14 (W. Lajnef, J. M. Vinassa, et al. 2007) with the help of a general electric model, comprising of SC simple electrical model, transmission line model and a parallel branch model with leakage resistance, describing the SC dynamic effect over a large charge/discharge duration (from milliseconds to hours).

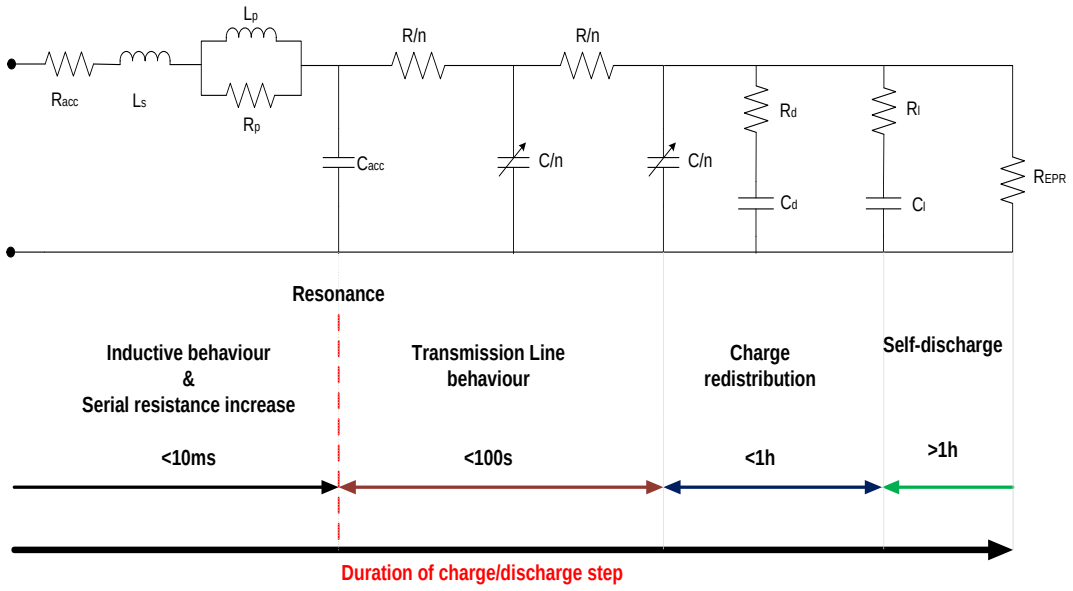


Figure 2-10: General electric model of supercapacitors, illustrating the time ranges of its dynamic effects, adapted from (Lajnef et al. 2007)

SC dynamic behaviour is strongly related to the effects of the porous electrodes. The charging process of SCs shows some non-linearity to the capacitance and voltage

relationship, as mentioned in Zubieta & Bonert (2000). The charging/discharging processes do not occur with the same time constant throughout the electrode material, as shown in Figure 2-10. The termination of the charging process leads to a drop in voltage, due to the finite conductance of the electrolyte (Kaus, Kowal, & Sauer, 2010a). Double-layer charge distribution that extends throughout the pore takes place following the removal of the current source.

Another aspect to SC dynamic behaviour is its nonlinear voltage response due to increasing state-of-charge, which has led the emergence of nonlinear models. The nonlinearity of SCs behaviour to the applied voltage is addressed by introducing nonlinear component, often a capacitor, which varies with voltage (observed in time domain when the charging process is stopped). This method is used in Niu & Yang (2011), Zhu et al. (2007), Zubieta & Bonert (2000), Funaki (2010), Zhang & Yang (2011). In 2007, Lajnef et al. proposed an equivalent circuit made of a nonlinear transmission line with voltage dependent capacitors for a peak-powered SC where they investigated the relationships among OCV, temperature and charging frequency (Lajnef, Vinassa, Briat, Azzopardi, et al., 2007). Rafik et al., also in 2007, proposed a 14 RLC equivalent circuit to describe the influences of operating frequency, voltage, and thermal effects on SCs (Rafik, Gualous, Gallay, Crausaz, & Berthon, 2007). Besides that, nonlinear models have been built by following the evolution of the model parameters as a function of voltage to obtain polynomial expressions that contained the voltage dependency terms of these parameters as demonstrated in (Nicolas Bertrand, Sabatier, Briat, & Vinassa, 2010). Recently, Torregrossa et al. (2013) attempted to model the long-term redistribution phenomenon in SC by the inclusion of two ‘virtual’ current sources and nonlinear capacitors, to take into account the

short and long duration of SC redistribution phenomenon. Wu et al. (2012) used artificial neural networks (ANNs) to determine the parameters of their nonlinear circuit model (Wu, Hung, & Hong, 2012a).

The dynamic characteristic of SC is observable in the frequency domain. SC exhibits a $45°$ impedance at low frequencies. According to Kötz and Carlen (2000) (Ko & Carlen, 2000), the $45°$ region, known as the Warburg region, which have the nature of the distributed resistance/capacitance in a porous electrode (Ko & Carlen, 2000).

The diffusion phenomena cause a 'fractional behaviour' at the middle and low frequencies area, which can be mathematically described by fractional differential equations (García, Roncero-sánchez, Parreño, & Feliu, 2010) (Dzieliński, Sarwas, & Sierociuk, 2010)(Martín et al., 2008). It has been shown in Dzieliński et al. (2011) and N Bertrand et al. (2010) that this type of modelling gave accurate results over a wider range of frequencies. In the time domain, El Brouji, Vinassa, et al. (2009) have shown that the fractional term was able to simulate satisfactorily the voltage evolution upon the cessation of the charging process. In 2013, Mitkowski and Skruch (2013) (Mitkowski & Skruch, 2013) proposed fractional-order models in the form of RC ladder networks. Fractional models have been proved able to minimize the number of parameters in the development of SC equivalent circuit models (Martin, Quintana, Ramos, & De La Nuez, 2008).

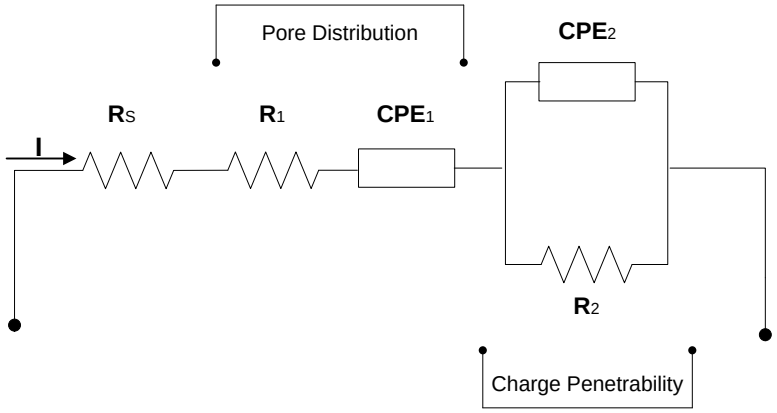


Figure 2-11: SC Impedance model proposed by N Bertrand et al. 2010 describing pore size dispersion and accessibility (N Bertrand et al., 2010)

Apart from the traditional equivalent circuits, SC's 'fractionality' has been modelled by the electrochemical equivalent circuit. In 2000, Kötz and Carlen (Ko & Carlen, 2000) proposed that the non-vertical line at the low frequency can be modelled by replacing the capacitance expression with a constant phase element (CPE) expression. CPE is a unique circuit component in Electrochemistry that is used to represent the frequency dispersion of capacitance (in pore size dispersion and accessibility)—one of the SC dynamic characteristics, caused by surface roughness or non-uniformly distributed properties of an inhomogeneous electrode surface (Martín et al., 2008). Similarly, the use of CPE in SC equivalent circuit modelling can also be found in García et al. (2010), Dzieliński et al. (2011), Quintana et al. (2006), Mahon et al. (2000), Nicolas Bertrand et al. (2010), El Brouji, Briat, J.-M. Vinassa, et al. (2009) and Dhirde et al. (2010). The CPE can be represented in a finite ladder network as shown in Fletcher et al. (2013). Biswas et al. (2006) (Biswas, Sen, & Dutta, 2006) have attempted to realise CPE to a form that can be used as a circuit device (Naim, 2015).

2.3.3 Supercapacitor 'Module'

SCs are low power devices with a maximum voltage of $2.7V$. Therefore, to meet the power requirements on certain applications such as Thounthong et al. (2005), N et al. (n.d.), Ariyanayagam (2012) and Embrandiri (2013), they must be merged together in series and/or parallel arrangements to form a 'module' with a specific voltage and capacitance rating. The most critical parameter for all capacitors, including SCs, are; voltage rating, capacitance, ESR (equivalent series resistance) and EPR (equivalent parallel resistance).

Subjecting any capacitor to a substantially higher voltage than it is designed to withstand, usually results in an irreparably damaged capacitor, and is particularly the case for SCs, so they must be protected from overvoltage conditions. Capacitors typically have two voltage ratings. Whatever voltage the capacitor can sustain indefinitely, without damage or performance degradation, is called the continuous working voltage, while the voltage that a capacitor can handle for just a short period, like a few hundred milliseconds, is the momentary peak or surge rating (Design, 2002).

When a SC is subjected to more than its tolerable voltage, the organic electrolyte within the cell begins to decompose, producing a gaseous by-product. If the overvoltage condition stays long enough, the pressure may build up until the safety vent, and the SC package opens. The electrolyte then decomposes and vaporizes until the SC's effective internal resistance increases and becomes an open circuit.

To achieve optimum "SC module" energy capacity, sizing the module is necessary to match application power and energy requirements. It is common when sizing SC module, to make the mistake of choosing a specific voltage and then calculating the capacitance required, which often results in over sizing of the SCs. The main aim when sizing any string of SCs is to minimize the mass, which implies using the least amount of SCs. It is important to note that the module overall voltage and capacitance are in fact related by the number of cells in the module n given the assumption that the SCs wouldn't be charged above the combined maximum voltage rating of all the cells. SC module voltage and capacitance in a parallel or series arrangement can be calculated using Equations (2.1) and (2.2).

$$V_{SC\ module} = n \times V_{max} \tag{2.1}$$

$$C_{SC\ module} = \frac{C_{cell}}{n} \tag{2.2}$$

Where, $C_{SC\ module}$ is the capacitance value of SC module; $V_{SC\ module}$ is the voltage rating of the module; C_{cell} is the capacitance value of the individual cell; n is the number of cells in a module; and V_{max} is the maximum SC cell voltage .

Theoretically, energy capacity in a SC module can be calculated using Equation (2.3) (Sirmelis & Grigans, 2011)

$$W_{SC\ module} = \sum_{n=1}^{n} \frac{C_{SC\ module} {V_{max}}^2}{2} \tag{2.3}$$

Where, $W_{SC\ module}$ is Energy of SC module; $C_{SC\ module}$ is the capacitance value of nth SC; V_{max} is the maximum SC cell voltage.

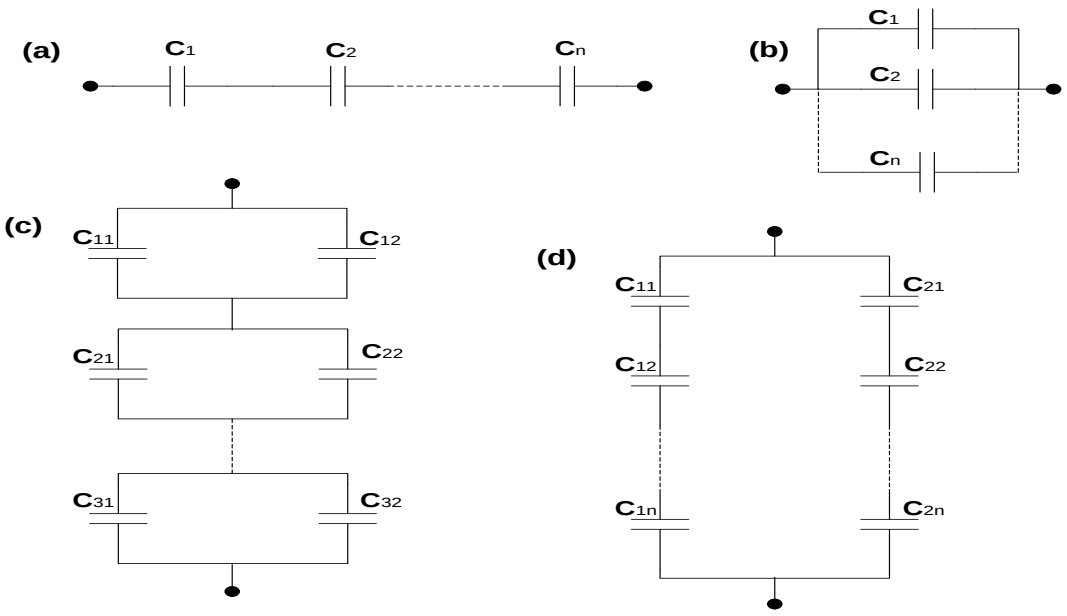


Figure 2-12: SC Module balancing arrangements in: (a) series (Barrade, 2002) , (b) parallel, (c) Matrix (parallel/series) (Sirmelis & Grigans, 2011) (E. Zhang, Qi, & Wei, 2010) and (d) Matrix (series/parallel) (Sakka, Gualous, & Van Mierlo, 2010; Sirmelis & Grigans, 2011) (E. Zhang et al., 2010)

2.4 Supercapacitor Voltage Equalization/Balancing Techniques

When connecting many capacitors in series, the issue of voltage balancing inevitably comes into play (N Rizoug, Bartholomeus, Vulturescu, Le Moigne, & Pierre, 2004). Basically, there are two reasons for an imbalance of voltages in a string of SCs: (1) deviations from the nominal capacitance of the SCs and (2) deviations in self discharge performance. While the first reason is mainly important during the dynamic performance of the SC string, the latter dominates for static SC performance during constant voltage phases. A cell management circuit maximizes the performance, and life of SCs installed in series (Linzen, Buller, Karden, & De Doncker, 2005)(R. Kötz, J-C. Sauter, P. Ruch, P. Dietrich, F.N. Büchi, P.A. Magne*, 2007)(Yi Zhang et al., 2009).

There has been a few research in the area of SC cell balancing with different design techniques to complement application requirements (Chang, Yang, Li, & Zhu, 2010)(Barrade, 2002)(Diab, Venet, Rojat, Umr-cnrs, & Lyon, 2006)(Cheimonidis, 2009)(Xuewen & Guo-zheng, 2014). SC balancing techniques are usually designed to the user's specification, which reflects its cost, flexibility, efficiency, and packaging implications.

Voltage equalization circuit have already been described, for applications with batteries (Juan Zhao, Jiuchun Jiang, & Liyong Niu, 2003; Kutkut & Divan, 1996; Lu, Qian, & Peng, 2012)(Cao, Schofield, & Emadi, 2008). However, In SC applications, the principle behind the equalization circuits differs from battery applications, given that the time constants during charge/discharge cycles are reduced to a few seconds, compared to battery cycles (Barrade, 2002).

The principle of voltage initialization during equalization is that all SCs are balanced at the upper voltage limit of the SC module (as shown in Figure 2-13). As a consequence, when the module is discharged, the individual SCs will adopt different voltages on a lower level. When recharged to the upper voltage, all the SCs will be balanced again, provided that the capacitances of individual SCs change slowly with time (Yi Zhang et al., 2009). This method is much more feasible and less expensive. R. Kötz, J-C. Sauter, P. Ruch, P. Dietrich, F.N. Büchi, P.A. Magne* (2007) has implemented it with an occasional initialization of all SCs, which has achieved a nice result.

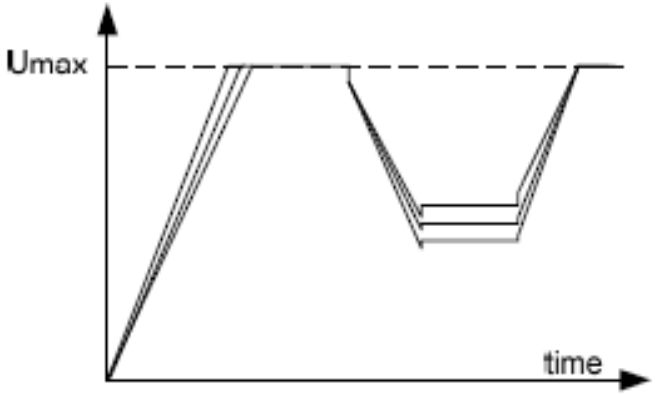


Figure 2-13: Principle of voltage initialization (Yi Zhang et al., 2009)

To redistribute and balance SC cells-voltage, various voltage equalization/balancing circuits are employed, which are based on two main concepts: dissipative and non-dissipative, also known as passive and active balancing method respectively (Diab et al., 2006) (Linzen et al., 2005).

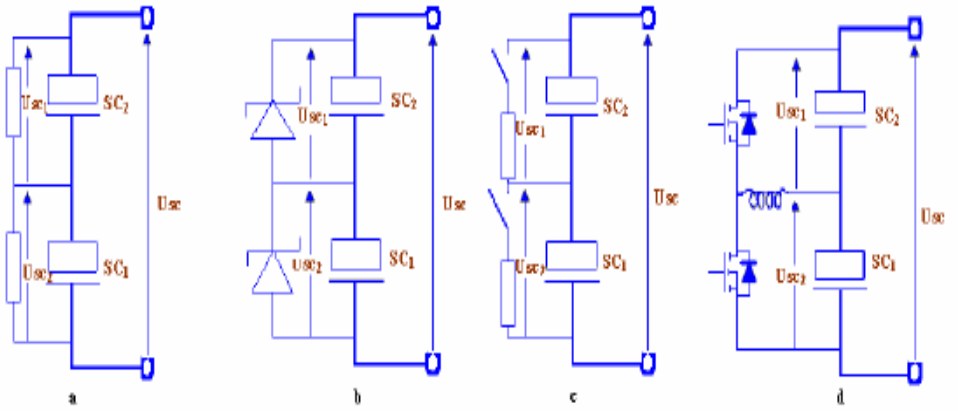


Figure 2-14: SC cell balancing circuits using; (a) Passive resistors; (b) Zener diodes; (c) Switched-resistors (d) DC-DC converter (Diab et al. 2006) (Linzen et al. 2005)

2.4.1 Dissipative Equalization/Balancing Circuit

This type of balancing method uses electrical components such as resistors to dissipate energy by converting it from the SC module to heat, hence balancing the cells in the module. This method is considered cheap and simple, though less efficient. The dissipative method employs passive resistors (Figure 2-14a), Zener diodes (Figure 2-14b) and switched-resistors (Figure 2-14c) to balance SC cells.

The cheapest and the simplest way to balance cells is to place resistors of equal resistances in parallel to each SC cell as shown in Figure 2-14a. This balancing method allows balancing cell voltage by dissipating energy manifested as overvoltage on the first SC (SC1) to the second SC (SC2) through thermal effect (Diab et al., 2006). The resistors in the balancing circuit are chosen so that the leakage current is two to ten times bigger than the leakage current through the SC cells depending on the desired accuracy. The big drawback of this method is that the SCs will constantly discharge over the resistors, but if the current drawn from the SCs is big compared to the current through the resistors, it might be a considerable option (Ershag, 2008).

Another type of dissipative balancing circuit uses Zener diodes as shown in Figure 2-14b, to equalize SC cells-voltage according to Zener voltage by dissipating the extra energy in thermal effect. In this method, the cell voltage is held constant as soon as the Zener voltage is reached. The diode operates as a by-pass for the main current. The disadvantages of this method are the high power losses in the diode and the

strong temperature dependency of the Zener voltage itself, which is less tolerable in most applications (Diab et al., 2006).

Switched resistor balancing circuit (Figure 2-14) is an extension to the passive resistor balancing method in which the SC voltage is monitored. The general concept depends on adding a controlled switch to an equalization resistor to limit the energy dissipation. The switch turns on when cell voltage goes beyond operating voltage and turns off when the level is lower than the operating voltage (Diab et al., 2006).

2.4.2 Non-Dissipative Equalization/Balancing Circuit

In contrast to dissipative circuits, non-dissipative balancing circuit (also known as active balancing circuit) behaves nonlinearly to force the SC cells to have an equal voltage, resulting in the most efficient use of the SC string. This method of voltage balancing employs active structures such as comparators (Yi Zhang et al., 2009), and converter topologies with or without a transformer (Linzen et al., 2005). These circuits transfer the excessive energy of cell overvoltage to other cells instantaneously to equalize cells voltage.

Figure 2-14d is an example of non-dissipative balancing circuit, which equalizes the cells voltage locally by two consecutive SCs, using a structure of buck-boost converter for each pair of SC. The balancing begins as soon as a difference of cells-voltage appears, the extra energy of SC2 is stored firstly in the inductor, then transferred indirectly to SC1 using a switch. The instantaneous transfer of energy related to overvoltage from SC2 to SC1 leads to higher efficiency and life expectancy. The main

disadvantage of these balancing circuits resides in the indirect energy transmission especially for applications with a huge number of SCs in series (Diab et al., 2006).

The active balancing circuit is required in high duty-cycle applications and where low parasitic losses are necessary. Some schemes are used to achieve active balancing and many are patented (a few of this literature is studied below).

In 2004, Guy C.Thrap, Del Mar, CA(US) invented a patent for Maxwell Technologies to charge and balance SC cells in a module. The balancing circuit consists of a voltage divider, operational amplifier and a resistor which is connected to each of the SC cells through a feedback loop. The circuit balances the cells by transferring energy from high charge SC to the low charge SC until they reach a balance charge. The patent provided an option to optimize the circuit by including a current limiting resistor to prevent system failure, and a gain stage to increase output current of the operational amplifier for high power demand applications (Guy C.Thrap, Del Mar, CA(US), 2004).

In 2007, Technologies (2007) published a document on Cell Voltage Management. The circuit developed by Maxwell was a sinking topology capable of sinking current in between 300mA to 400mA from every cell when the voltage of the cell was bigger or equal to 2.73V. Every cell voltage was monitored against a nominal reference voltage. The voltage management circuit was used to lower the voltage of the cell below the trip level when the reference cell voltage was exceeded. During the balancing stage, the management circuit would go into a quiescent state whenever the cell went below the critical voltage, which prevented failure and assured long lifetime of the cells (Technologies, 2007).

In 2009, Johnson (2009) overcame the overcharge problem by balancing the voltage across a string of SCs with a voltage limiting circuit across each cell. Three 310F SC cells were connected in series with each having its individual balancing circuit, to form an energy bank. The balancing circuit proposed by Johnson was connected to a Seiko voltage regulator, to charge the storage bank from a $3W$ solar panel, with $300mA$ short circuit current, to achieve a total of $7.95V$ of the module with each SC rated at $2.65V$ when fully charged. When the charge reached $2.65V$ at each of the SC cells, the PMV30UN switch would turn on, causing the output voltage of the amplifier to flow to the Seiko voltage regulator (Johnson, 2009).

In 2010, Chang et al. (2010) investigated SC active voltage equalizers on Rubber-Tyred Gantry Crane Energy Saving System. Chang investigated a series of active circuits using switch resistors, inductors, forward and flyback converters, before proposing an active voltage equalization method using a buck-boost converter. The paper proved that the switch resistor method consumed large amounts of energy to utilize the system because of its lower efficiency and poor reliability. While the forward and flyback converter method provided higher system efficiency than the switched resistors, but still wasn't effective enough, due to the complicated magnetic circuit, large voltage equalization error, big volume, and difficulties in the extended winding. The proposed buck-boost converter on the other hand transfers energy rapidly from high voltage SCs to the low voltage SCs with low energy loss (Chang et al., 2010).

In 2013, Chieh et al. (2013) proposed a novel SC cell power management system to balance SC cell voltage while monitoring the currents during charge and discharge

cycle. The SC cells were connected in series to form a multi-cell stack for practical applications due to the low operating voltage of SCs (Chieh et al., 2013).

2.5 Supercapacitor Ageing and Lifetime

2.5.1 Cause and Effect of Supercapacitor Ageing

Although SCs have been around for decades (Ko & Carlen, 2000), not much research on SC reliability is available, as opposed to lithium-ion battery, in which the investigations are more advanced. The scarcity of study in SC reliability is probably because the electrical energy generated in SCs is not by a redox reaction. Thus, SCs can loosely be regarded as a 'safer' energy storage than batteries and fuel cells (Winter & Brodd, 2004).

In SC applications such as electric vehicles (EVs) and hybrid electric vehicles (HEVs), researchers Burke, (2010b), Hu, Tseng, & Srinivasan, (2011), M. Embrandiri, Isa, & Arehli, (2011) investigated SC's improvement to battery powered systems. The addition of SCs to energy storage systems for EVs and HEVs has resulted in a more detailed assessment on SC ageing, to better understand the outcome that can be expected after long-term use, as well as, to create strategies which will alleviate any risk. Given that, SCs are seen as the solution to all the weak points in batteries (low power capability and limited cycle life) (Burke, 2007)(G. Wang et al., 2012)), SC reliability study is more urgently required. Although SCs are known for their fast charging/discharging (cycling) properties, because they experience very little chemical reactions during charging and discharging (G. Wang et al., 2012), Hahn et al.

(2006) observed a reversible expansion of the electrode material in activated carbon (AC) SCs utilizing organic electrolyte $TEABF_4$ in acetonitrile (AN) during charge/discharge cycle that is due to intercalation/insertion processes. This dimensional change that is often observed in batteries is believed to contribute to degradation and cycle life limitation in batteries. Therefore, considering that similar observation is also observed in SCs, this suggests that the process might also be a possible cause of limited cycle life in SC (Hahn, Barbieri, Campana, K??tz, & Gallay, 2006).

SCs have high power density but suffer low energy density. This characteristic is ascribed to their small voltage window. Therefore, Hahn, Wursig, Gallay, Novák, & Kötz, 2005, considered increasing the voltage window to improve SC energy density and power density, but it was proved that such a move could cause faradaic reactions, ion insertion and gassing resulting from electrolyte decomposition, which could in turn affect the SC's lifetime, Hahn et al. (2006) found a significant pressure increase in SCs based on $TEABF_4$ in propylene carbonate (PC) aqueous electrolyte when cycling between 0 and 2.5V, as well as when constant voltages up to 3V are applied to the cell (Hahn, Kotz, et al. 2006).

Kötz et al. (2008) investigated the pressure evolution in cylindrical-type SC based on three different solvents: propylene carbonate (PC), acetonitrile (AN) and γ-butyrolactone (GBL) (Kötz, Hahn, Ruch, & Gallay, 2008). At 3V constant voltage, GBL has the highest leakage current, followed by AN, while PC shows the lowest leakage current (half as much as the leakage current in AN). Despite the twofold higher leakage in AN, PC is found to produce a higher gas evolution rate, by a factor of 5,

than in AN, while GBL marks the highest figures both in terms of leakage current and gas evolution rate. In an attempt by Ruch et al. (2010) to draw distinctions between the ageing of electrode from two different types of solvent i.e. AN and PC (Ruch, Cericola, Foelske, K??tz, & Wokaun, 2010), they identified that in AN, the ageing is more profound at the positive electrode, while in PC, ageing is dominant at the negative electrode. The degree of ageing is reflected in the increase of resistance and the loss in capacitance in both types of electrolytes. Kötz et al. (2008) and Ruch et al. (2010) both concluded that the different faradaic processes occur in the negative and positive electrodes and this is directly dependent on the type of electrolyte used. This finding suggests that SC construction need to be optimized according to the type of electrolyte used.

In 2007, Azaïs et al. (2007) showed that after a long-term operation of 2.5V constant voltage, SCs based on AC and organic electrolytes AN experience a capacitance loss and a resistance increase that could be further enhanced by microscopic phenomena. These microscopic phenomena are gas evolution, raising electrode mass and local separation of the coating layer from the metallic collector (Azaïs et al., 2007). The main gases identified are methane, ethane, di-oxygen, carbon monoxide and carbon dioxide. The decomposition of electrolyte blocks electrodes pores in the gaseous products, and shows a reduction in the aged positive electrode in its specific surface area more substantial than that of the aged negative electrode, which in turn results in the loss of capacitance. These findings show that SCs undergo redox processes, most probably due to the traces of water in the organic electrolyte, which are accountable for SCs ageing. This finding was also backed up in (M. Zhu et al., 2008).

Kurzweil and Chwistek (2006) found a brownish salt residue on a burst SC, which had been long-term exposed long-term to 90℃ and 2.3V constant voltage, and updated their findings by reproducing the brownish salt residue through electrolysis to identify the components of the salt residue (P. Kurzweil & Chwistek, 2008). They detected that the AN electrolyte decomposed to form acetamide, acetic and fluoroacetic acid. They also found that after a thermal ageing experiment at $70℃$ for $550h$, white spots appeared on the aluminium foil which was immersed in AN, while, the aluminium which was in contact with air showed a greyish colour (P. Kurzweil & Chwistek, 2006a).

Aside from the electrolyte-based ageing, the ageing phenomenon in SCs is also caused by the carbon materials used in the electrodes. The carbon electrodes should be inert and be able to guarantee the reversibility of charge transfer reactions. However, this was not the case; the presence of heteroatoms identified in carbon materials (Ruiz, Blanco, Granda, & Santamar??a, 2008) caused faradaic reactions in SCs. Zhu et al. (2008) studied the chemical and electrochemical ageing of carbon materials in SC electrodes. To make the case simpler to analyse, the role of the binder was not taken into account (M. Zhu et al., 2008).

The ageing effects in SCs are expected to cause a change in their structural (physical) and chemical characteristics of their electrodes, the chemistry of their electrolyte (Chiba et al., 2011)(Ishimoto, Asakawa, Shinya, & Naoi, 2009), and, in extreme cases, even other components. In this way, the capacitance decreases, and the equivalent series resistance (ESR) increases. These two values can be employed to detect ageing quantitatively, even during use (Bittner et al., 2012).

Gualous et al. (2010) was able to identify three SC failure modes: (1) cell container opening caused by pressure build up in the cell, (2) more than 20% capacitance loss due to the reduced accessibility for the ions following electrochemical cycling, and (3) more than 100% increase of ESR from the weakening adhesion between electrode and collector with time and temperature (H. Gualous et al., 2010).

2.5.2 Supercapacitor Ageing Tests

The most common SC ageing factors are high temperature and high voltage (Bohlen, Kowal, & Sauer, 2007a). Besides temperature and voltage, SCs are also aged by applying constant current charge/discharge cycles, undergoing power and drive cycles on SC module (Jeon, Lee, Jeong, & Lim, n.d.). Like many electrochemical devices, the chemical reactions in SCs follow the Arrhenius law which states that higher temperature causes more rapid chemical reactions—for every 10°C increase or each 100mV, the chemical reaction rates double and the life is halved (Uno & Tanaka, 2012)(Schiffer, Linzen, & Sauer, 2006)(Bohlen et al., 2007a). Researchers have found ways to speed up the ageing process in laboratories, which if tested in a normal condition, would take longer than ten years (Uno & Tanaka, 2011a).

Accelerated testing that quickens failure has been practised widely. The accelerated tests are carried out by applying stress levels that are near the maximum tolerated limit or, beyond the conditions that the SC would be exposed to in its normal service. The manufacturers typically set the operation temperature for SCs either based on acetonitrile (AN) or propylene carbonate (PC), at -40°C to +70°C (Kötz, Hahn, & Gallay,

2006); despite the fact that SC based on PC suffers performance reduction at temperatures below 0℃ (Liu et al., 2006).

2.5.3 Supercapacitor Ageing Factors: Temperature and Voltage

In 2003, Gualous et al. investigated temperature influences on the lifetime and performance of SCs (H. Gualous et al., 2003). The authors studied the ESR variation with temperature on commercial SCs based on organic electrolyte and they found out that the ESR decreased as the temperature increased, consequently causing a reduction in the voltage. Additionally, capacitance decreased with temperature. This examination is in line with (Michel, 2006). In addition to that, Gualous et al. (2003) observed that the charging and discharging process raised the SC surface temperature by about $2℃$ when $140A$ current was applied to the device. Therefore, they recommended that the thermal behaviour of SC to be characterised, especially in the case of SC module in transportation applications.

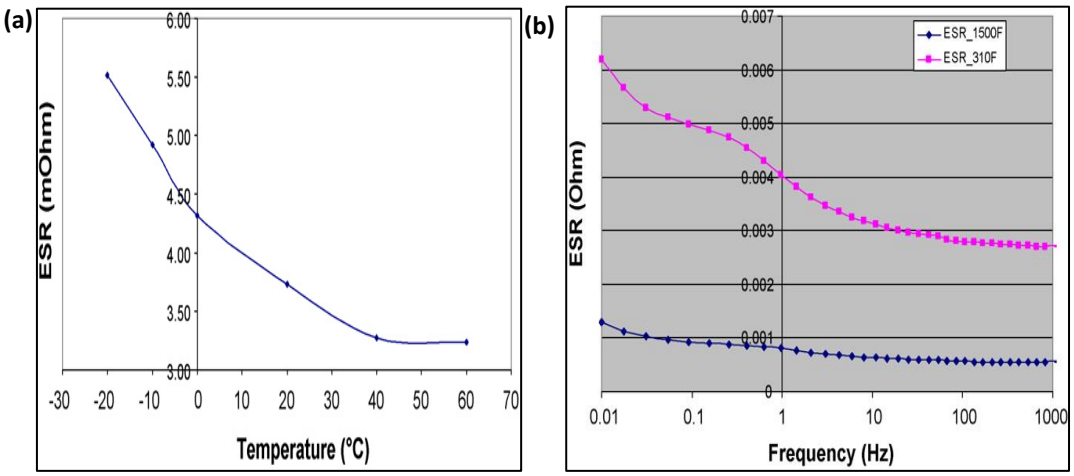


Figure 2-15: Demonstrating the influence of temperature on ESR and capacitance: (a) BCAP310F equivalent series resistance as function of temperature., (b) BCAP1500F and BCAP310F series resistance as function of frequency with a bias voltage respectively of 2.7V and 2.5V and a temperature of 20 ◦C. Adopted from (Al Sakka et al., 2009b)

Another test often mentioned in literature is the calendar life test. The calendar test is a mode of testing that studies the effect of temperature by storing the SCs at a constant temperature with a fixed voltage applied to the SCs at the same time (the voltage applied is usually specified at the maximum potential according to the decomposition point of the electrolyte system). Bohlen et al. (2007) in Part I of their work (Bohlen et al., 2007a), increased the ageing rate by a factor of 64 so that the end of life criteria cause be achieved in 3 months; this factor was attained by either increasing the temperature by 40K above the nominal temperature $25℃$ —which resulted in test temperature of $64.85℃$ —or by increasing the voltage by $200mV$ above the rated voltage (or increment of $20K$ and $400mV$).

Internal resistance (ESR) and capacitance are usually monitored to quantify ageing. The increase in ESR and the decrease in capacitance are usually due to two phenomena (Alcicek, Gualous, Venet, Gallay, & Miraoui, 2007): (1) degradation of the electrolyte; (2) degradation of the activated carbon. At high temperature, the electrolyte decomposes, leaving by-products that block the pores of the electrode, which in turn reduces the surface area and restrict the accessibility of ions in the activated carbon pores (Alcicek et al., 2007). The reaction of the chemical components is accelerated at a higher temperature, whereas the high voltage speeds up the decomposition of the electrolyte and the impurities cause redox reaction in SCs (Alcicek et al., 2007). Umemura et al. (2003), noted that the change in capacitance was different in the positive electrode and the negative electrode, after $1{,}000\ hours$ of ageing under floating voltage $2.5V$ at $70℃$ (Umemura et al., 2003).

In a test done by Kurzweil et al. (2005) on commercial SC based on the organic electrolyte, they found that the increase of resistance after 1000hours of constant voltage test at 2.5V and 70℃ is more pronounced than the capacitance loss. The leakage current also increases significantly by a factor of 8 after the test had stopped (P. Kurzweil, Frenzel, & Gallay, 2005).

Kötz et al. (2006) used a procedure that is based on aluminium electrolytic capacitors to monitor SC ageing. The procedure involved measuring the leakage current under various temperature and voltage conditions and then deriving the activation energy. The activation energy was higher for a temperature range of 0℃ to 60 ℃ than the activation energy for a temperature range of -40℃ to 0℃. The authors, however, were unsure if the SC's measurement history affects the results (Kötz et al., 2006).

In a test done by Bittner et al. (2012), SCs based on $TEABF_4$ in AN, organic electrolytes were aged at various voltages (between $2.3V$ to $2.5V$) and temperatures (50℃ to 80℃), it was found that the effect of voltage increase is more significant than the effect of temperature increase; for instance, SCs which are stressed with $2.5V$, 70℃ age faster than the SCs at $2.3V$, 80℃ (Bittner et al., 2012). A structural change in anodes caused by oxidation of the carbon was also observed. In addition to that, the separator of aged SCs, particularly on the side exposed to anode, also changed colour from white to yellow/brownish with a dark residue—potentially from carbon. The findings were in concordance to the results in (P. Kurzweil & Chwistek, 2008).

The evolution of the SC's declining performance under several voltages and temperature conditions were studied in El Brouji, Briat, J. M. Vinassa, et al. (2009).

The temperatures were varied in the range of $55℃$ to $65℃$, and the voltages were varied between $2.5V$ to $2.9V$. This ageing evolution was observed by monitoring the shape of the Nyquist plots. Although there was no visible change in the Nyquist shape, the effect of voltage and temperature was translated to the shifts of the Nyquist along the real axis and corresponds to the increasing ESR as shown in Figure 2-16. The higher the voltage, the more significant the ageing. The authors suggested that these distortions could be attributed to a reduction of the pseudo-capacitive charge storage mechanism.

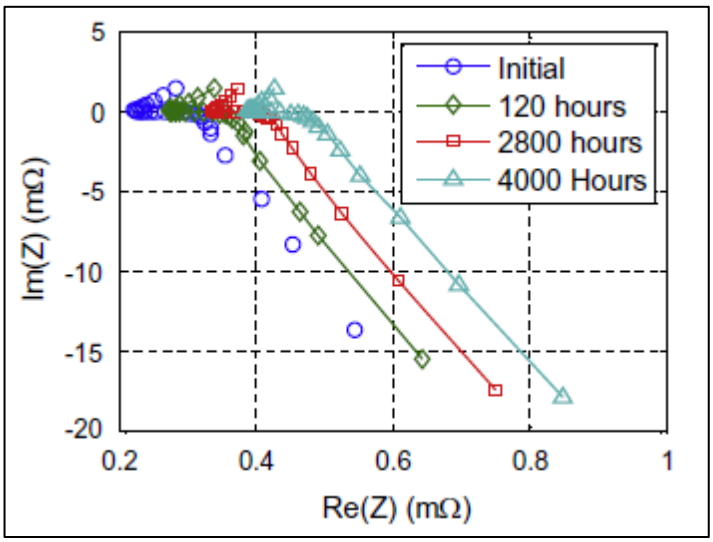


Figure 2-16: Impedance spectrum (Nyquist plot) changes during calendar life tests. Adopted from (El Brouji, Briat, Vinassa, Henry, et al., 2009)

Gualous et al. (2010) and Ayadi et al. (2013) on the other hand, were interested in the effect of thermal shock on SC. In Gualous et al. (2010) the thermal shock test was performed on a stack of SCs (no voltage was applied to the module) between two extreme climate chamber (using a profile shown in Figure 2-17). The stack was first placed in climatic chamber one at $80℃$ for 2 hours and then transferred to climatic chamber two at a regulated temperature of $20℃$. After 20 temperature shock cycles,

an increase in the ESR value is detected at about $+12\%$ by EIS measurement, while the capacitance variation is around 3%. Ayadi et al. (2013) later updated their findings to include the effect of vibration on SC ageing between $40℃$ and $50℃$ temperature change in H. Gualous, Camara, Boudrat, Gallay, & Dakyo, (2013). The results from the thermal cycling are compared to the results from calendar test held at fixed temperature of $50℃$. They found out that changing temperature had certainly caused SCs to age more than that exposed to calendar test (Figure 2-18).

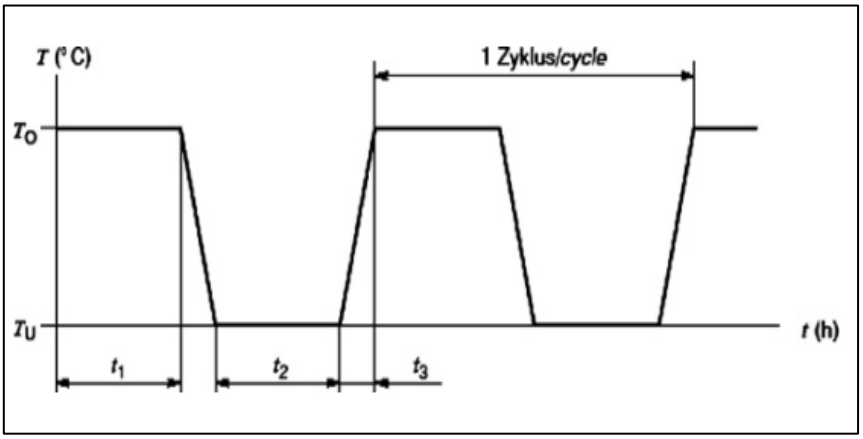


Figure 2-17: Thermal shock test in (H. Gualous et al., 2010) appeared in (Naim, 2015)

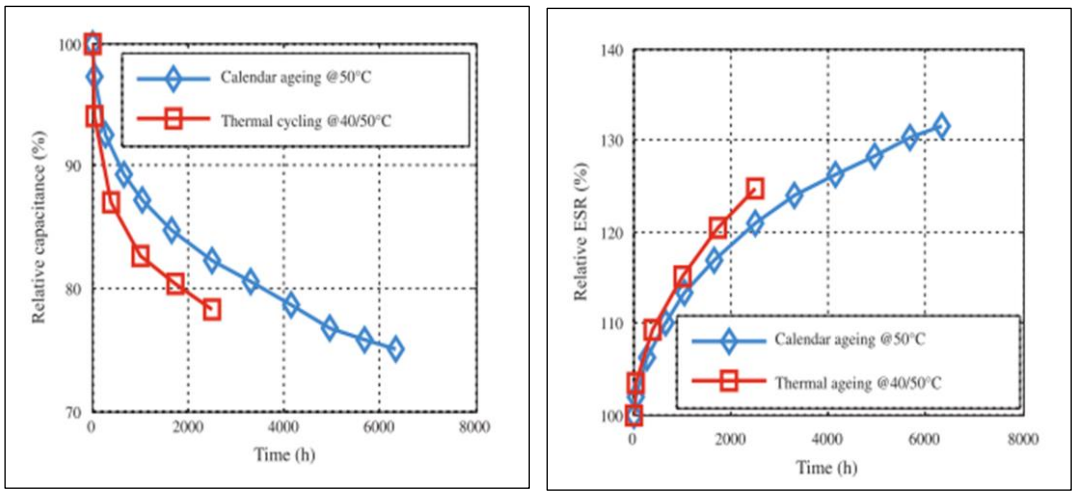


Figure 2-18: The effect from thermal cycling on capacitance (left) and resistance (right) were more pronounced than calendar ageing test. (Ayadi et al., 2013) appeared in (Naim, 2015)

Ageing tests that are based on temperature and voltage as the ageing factors do not exceed the maximum voltage (determined by the decomposition voltage of the electrolyte system), and the maximum temperature (determined by the electrolyte boiling point of 81.6^0C (H. Gualous et al., 2012) (Alcicek et al., 2005)). We have seen a growing interest in understanding SC behaviour beyond this range. This type of test is usually destructive and is meant to study the robustness of SC and its response to undesirable conditions. An example of an 'abusive' testing was done by Ruch, Cericola, Foelske-Schmitz, Kötz, & Wokaun, (2010) and Kurzweil & Chwistek, (2006). Constant voltages up to $6V$ and temperatures up to $90℃$ were used in their experimentations. They found out that, although the SCs were tested well beyond their tolerated limits, they could still be operated for several months.

2.5.4 Ageing Effect of Supercapacitor on Charge/Discharge cycling

Gualous et al. (2003) studied the effect of charging and discharging cycle, which induced heat generation in SC through joule heating, consequently reducing SC efficiency, (H. Gualous et al., 2003). The effect of charging was also investigated in (Schiffer et al., 2006). The authors used a symmetric square wave profile to charge and discharge SCs. The current profile used, raised the SC surface temperature to about $6.5K$. The temperature rise was due to the effect of irreversible Joule heating. Further to that, the authors also investigated the impact of current rate on SC surface temperature. $100A$ current profile generated two times the temperature generated from $50A$ current profile and $6\ times$ the temperature produced by $25A$ current

profile. In regards to the surface temperature generated from cycling, Omar et al. (2013) detected that the surface temperature of $1600F$ SCs increased by $4℃$ with $70A$ current, meanwhile $90A$ current increased the surface temperature to $8℃$, after both were cycled for $110{,}000\ cycles$ (Omar et al., 2013).

Pascot et al. (2010) developed a calorimetric technique to measure the heat generated from cycling in SC based on PC electrolyte, from the transient temperature change. During charge/discharge cycling, a fraction of the energy within the SC cell was dissipated into heat through Joule losses. The SCs were subjected to galvanostatic cycling with a current range between 0.1 and $1A$. After $200s$ and about 30 current cycles at $0.4A$, the temperature of the SC increased exponentially but not exceeding $2.5℃$. The thermogram of the SC, calculated by Finite Elements Method, displayed the heat dissipation during cycling where the hottest area was at the surface of the SC and the temperature gradually dropped further away from the cell as the heat was dissipated to the ambient (Pascot, Dandeville, Scudeller, Guillemet, & Brousse, 2010).

Time-dependent heat profiles as SCs go through charge-discharge cycling were also studied by Dandeville et al. (2011) in (Dandeville et al., 2011a). The profiles were gathered from the change of temperature as SCs were cycled in a customised calorimeter. It was found that two types of heat are generated: a reversible heat and an irreversible heat. They found that irreversible heat is caused by the Joule loss from the porous structure, whereas the reversible heat is produced by the ion adsorption on the carbon surface. Apart from SC of the type of double layer, heat generated by a hybrid SC based on carbon-manganese dioxide MnO_2 was also studied.

As it has been pointed out by many authors, charge and discharge cycling induces heat generation in SC. To accelerate ageing, H. Gualous et al. (2012) demonstrated the use of $62A$ constant current on $350F$ SCs, to achieve component temperature of $65℃$. The SCs were cycled continuously without any rest time in between charging and discharging, from voltage between $1.25V$ and $2.5V$. After $1{,}000\ hours$, the ESR increased to 20% above the initial value and the capacitance dropped 15% from the initial value.

Constant current cycling has been demonstrated by Omar et al. (2013) to have a significant effect on SC's impedance (Omar et al., 2013). The authors observed a shift of the impedance spectra along the real axis at different temperature and current. Consistent with what had been reported by other researchers, higher current contributes to a higher increase in resistance. Despite the findings, there is no clear trend that can explain the increasing resistance on the number of cycles—except for that the ageing of the SC is nonlinear, and the nonlinearity is observed at all test temperatures. Apart from that, at low frequency, the imaginary part increases during cycling, thus, showing that the capacitance has decreased.

2.5.5 Ageing Effect of Supercapacitor on Power and Drive cycling

SCs are also tested using charge/discharge pulses (Figure 2-19) where the pulsed current profiles are defined according to the typical profile of HEVs, as in reference (Briat, Lajnef, Vinassa, & Woirgard, 2006). This type of test is known as the power cycling test. A current profile with a period of $1\ min$ used in this type of test is based

on the acceleration/braking or start/stop operations in HEV, while the pulse width depends on the vehicle type: 0.5 to $2s$ for micro-hybrids and 2 to $10s$ for mild-hybrids (Briat et al., 2006). The purpose of this test is to generate self-heating in SC, so that it acts as an accelerating factor to SC deterioration. The RMS value of the current profiles is chosen based on the RMS current value that will lead to a rise of $60℃$ at the beginning of the power cycling test. The $60℃$ is normally the maximum temperature limit for SC based on organic electrolyte. The discontinuity in the pulsed current profile of the power cycling test has proven to have an effect on SC ageing by Briat et al (2006) (Briat et al., 2006). Two pulsed current profiles were used, $200A$ and $400A$ current profiles, but both having the same 200A RMS value. After $25{,}000\ cycles$, the 400A current profile leads to higher temperature rise, higher resistance increase and a bigger capacitance loss than those of the $200A$ current profile. This data proves that the current shape can impact the way SCs age.

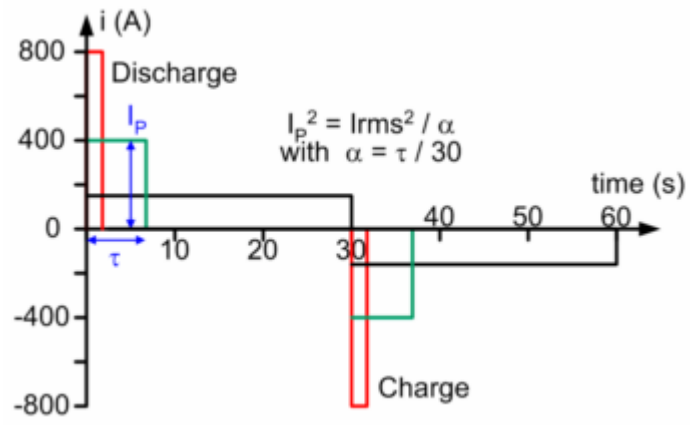


Figure 2-19: Current profile used in power cycling test (Briat et al. 2006).

Lajnef et al. (2007) studied the effect of power cycling on SCs from two different manufacturers. They found out that ageing rate depends on the cell design. Also studied was the effect of relaxation time on the SCs characteristics. A performance

recovery phenomenon was observed when the SCs were in resting periods. The results showed that the impedance real part, which corresponds to the ESR, is higher after $24\ hours$ of rest and, it gradually decreased with resting time, and whereas, the capacitance increased (Lajnef, Vinassa, Briat, Brouji, et al., 2007). In 2009, Brouji et al. reported that the recovery phenomenon was only observed in power cycling experiments and not in calendar life tests, which suggests that the ageing effect from calendar life is irreversible (El Brouji, Vinassa, et al., 2009). This finding was also reported in (Briat et al., 2010).

Brouji et al. (2009) reported that the effect of power cycling was more pronounced at low frequencies of the impedance results, in addition to the distortion observed in the impedance real parts (El Brouji, Briat, Vinassa, Bertrand, et al., 2009). Also reported was that power cycling affected the SCs by increasing the slope of the Nyquist plot, and this process was continued for the whole test duration. These findings showed that power cycling caused mechanical stress on the SCs resulting in the modification of the electrode structure.

Chaari et al. (2011) used a current profile based on repetitive start-stop, boost, and regenerative braking phases, typical in the micro-hybrid electric vehicle, the method being somewhat similar to W. Lajnef, J.-M. Vinassa, et al. (2007). They highlighted that the end-of-life criteria for SC regarding capacitance and ESR were not reached at the same time, as a matter of fact, 20% loss of capacitance was met before the 100% increase of the ESR (Chaari, Briat, Delétage, Woirgard, & Vinassa, 2011). The self-discharge and the charge redistribution mechanisms under various conditions i.e.

temperature, initial voltage, charge duration, the state of charge and short-term history, have been studied in Kaus et al. (2010) and Kowal et al. (2011).

While many efforts concentrated on the issue of ageing in SC cells, Rizoug et al. (2012) (Nassim Rizoug, Bartholomeus, & Le Moigne, 2012) found the need to study the ageing process of SC modules. In their experimentation, a SC module was exposed to power cycling. An important finding from the test was that, although all cells in the module were subjected to the same power cycling profile, the authors noted that ageing was more egregious at the cells situated inside than the SC cells located at the edges of the module. This observation was probably caused by the fan placed at the edges of the module; therefore, the temperature around the edges was lower than other areas in the module. This finding pointed out the need for careful planning of the thermal management system to ensure an equal temperature distribution inside the module so that ageing rate between each cell did not differ much. Moreover, Michel (2006) (Michel, 2006) had urged the need for a proper way of attaching the cooling elements with high electrical insulating and high thermal conductivity.

Although drive cycling effect on ageing has not been widely studied, nevertheless, the effect of drive cycle on SC EVs and HEVs is apparent, especially under high-temperature conditions observed in certain EV operation modes (Al Sakka, Gualous, Van Mierlo, & Culcu, 2009b).

Drive cycle is broken down into a series of sequentially isolated drive pulses (DP). DP is defined as an active driving period between two continuous stops on a trip. Distribution plot of Average speed Vs Distance is used as a basis to develop fuzzy logic membership functions and fuzzy rules to classify driving events using the variables of

average speed and distance. By classifying a driving event for each DP, a drive cycle profile can be constructed. Driving events: STOP N GO (SnG), URBAN (U), SUBURBAN (SU), RURAL(R), HIGHWAY (H) (as shown in Figure 2-25). The figure is an example of how the fuzzy logic pattern recognition was used to categorize a drive cycle into the five driving events (Manoj Embrandiri, 2013).

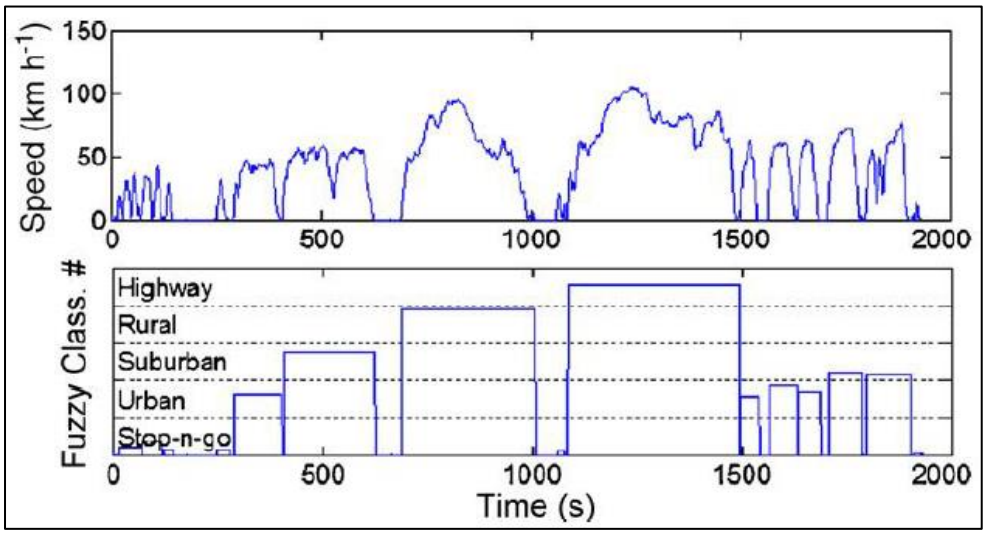


Figure 2-20: Drive cycle analysis; fuzzy classification of drive pulses (DP) (Liaw & Dubarry, 2007), appeared in (Manoj Embrandiri, 2013)

Jeon, Lee, Jeong, & Lim, developed a prototype vehicle of supercapacitor FCHEV, by replacing the battery FCHEV and DC/DC converter configuration developed in 2002 with a SC module. The module rated at $270V$ and $15.7F$ was made up of 108 cells ($2.5V$ and $1700F$). Two bench test were proposed to evaluate energy efficiency of the prototype vehicle which includes three standard driving cycles: FUDS, HWFET and, JAPAN10-15. The purpose of the bench tests are, (1) to verify the efficiency of a large-scale SC FCHEV system in its 'worst-case' charging and discharging tests and drive cycle tests, and (2) to develop control logics for starting up and power-limiting

strategy during vehicle operation. In the 'worst-case' charging and discharging, the step input of inverter power $(75, 50kW)$ or inverter current $(300, -300A)$ was applied to the hybrid system. But, in the drive cycle test, the simulated inverter current was used as the input programmable electrical loader. The results of the tests showed the dynamic response of SC module from idle state to maximum charge state at about $0.2\sim 0.4\ secs$, and the 'worst-case' charging and discharging duration was recorded at about $5\sim 7\ secs$. The drive cycle tests under FUDs driving cycle in the FCHEV system, had the SC module 'in operation' at high frequency and the fuel cell 'in operation' at low frequency. They proved through chassis dynamometer tests that a Santa Fe based SC FCHEV showed 11.2% better fuel economy than a baseline battery FCHEV under FUDS driving cycle (Jeon et al., n.d.).

Burke, 2010a, also simulated FCHEV on FUDS and US06 drive cycles with different powertrain configurations. The powertrain configuration investigated was categorized into three; (1) SC connected to FC directly, (2) SC coupled with FC via a 120Wh converter and (3) Li-ion Batteries coupled with FC via a 7.5Ah converter. Their simulation results on hybridization with SC showed to significantly reduced stress on FC through load levelling control, compared to FC vehicles without energy storage. SC FCHEV could achieve a fuel economy increase of up to 28% on FUDS cycle and up to 24% on the US06 cycle depending on the WH capacity of the SC unit. SC connected to FC directly, was reported to achieve the highest fuel economy, while SC coupled with FC via a $120Wh$ converter, and Li-ion Batteries coupled with FC via a $7.5Ah$ converter, utilised a large fraction of its stored energy for load levelling control strategy to mitigate the stress on the FC. Burke, 2010a, concluded after simulations that SC coupled with FC via a DC/DC converter was likely the best approach

considering its ability to achieve an increase in fuel economy as well as lessen the stress on the FC (Burke, 2010a).

Al Sakka, Gualous, Van Mierlo, & Culcu, 2009 investigated temperature influence on SC cell/module lifetime and performance for vehicle applications. A thermal model was developed based on a thermal-electric analogy which allowed the determination of SC temperature. Heat management in SC modules based on the model was studied using real life driving cycles to estimate the evolution of temperatures of SC according to electrical demands. The SCs module's model was simulated in Matlab/Simulink, with each cell modelled by a thermal-electric model. The convection heat transfer mode between cells was also modelled by resistances. The convection from a cell was modelled by resistances which depend on the heat exchange surface and the convective heat transfer coefficient. The convection between cells and the air was also modelled by a voltage source which represents the ambient temperature, and resistance which represents the convection heat transfer. In this study, SC module was subjected to real life drive cycles such as Scania and BMW driving cycles, which were considered for heavy duty vehicle and passenger car applications, respectively. Scania heavy duty vehicle driving cycle simulations were carried out under two ambient temperatures 25^0C and 50^0C for a total cycle duration of $22.766\,min\,(1366s/)$, while the BMW passenger car driving cycle characteristics simulations were also carried out under two ambient temperatures 25^0C and 50^0C for a total cycle time of $11.975\,min\,(718\,s/)$. The simulation results projected the need for a forced airflow cooling system in the middle of the SCs module (where the hotspot is located).

Results of the simulations showed that the Scania cycle under 50°C ambient temperature obtained a maximum temperature of 97.4^0C just after $2\ cycles$ (as shown in Figure 2-21), but with the added cooling system, after $30\ cycles$ the maximum temperature of the module didn't exceed 65^0C (manufactures specifications). The BMW cycle under 50^0C ambient temperature, showed a maximum temperature of 83.5^0C just after $7\ cycles$, but with the added cooling system, after $60\ cycles$, the maximum temperature of the module didn't exceed 65^0C (manufactures specifications). Detailed results of the simulations can be found in (Al Sakka et al., 2009b). This study demonstrated the importance of a cooling system in SC module especially in power profile during drive cycles, under high temperature.

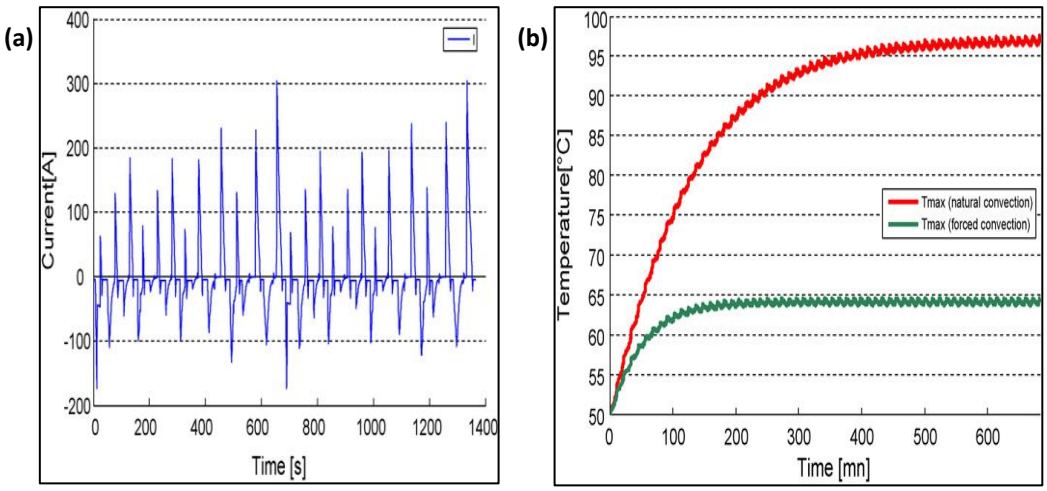


Figure 2-21: Scania heavy duty vehicle driving cycle; (a) Supercapacitors modules' current for Scania driving cycle as a function of time. (b) Evolution of the maximum temperature in the module as function of time ($30\ cycles$, ambient temperature $T_a = 50^0C$, natural and forced convection) with Scania driving cycle (Al Sakka et al., 2009b).

2.5.6 Quantification of Supercapacitor Ageing

SCs ageing is monitored periodically to follow the course of ageing. Electrochemical Impedance Spectroscopy (EIS) has been shown to be a pertinent tool to study the ageing phenomenon. EIS is usually applied on fresh SC and at every stage of the SC lifetime, to track the ageing course. Another method is the time domain characterisation, sometimes applied together with EIS.

In Alcicek et al. (2007), the characterisation was done every week after an eight hours rest at an ambient temperature of $20°C$. The ageing test increased the imaginary axis –ImZ of the impedance spectra, taken from EIS measurement, thus indicating that the capacitance value decreased as SC aged. A clear right shift along the ReZ axis signified that the ESR had increased with the ageing duration.

Bohlen et al. (2007) showed that the EIS was able to track the gradual change in the SCs electrical behaviour while they went through an ageing process (Bohlen et al., 2007a). Contrary to the method used in (Alcicek et al., 2007), mentioned previously, the SCs were not allowed to rest before characterization test. Nevertheless, a shift of the impedance spectra along the real axis is observed, identical to the observation in (Bohlen et al., 2007a). The real axis shift continued and then accelerated near the end of the test. A circuit model was fitted to the impedance spectra to aid in the analysis of the ageing behaviour.

Both methods above required the SCs to be disconnected from the test for regular check-ups, and they were reconnected afterwards to resume testing. Lajnef et al. (2007) devised a method which permitted the characterization to be performed

online while SCs were in test to minimize the effect of rest time on the test results (Lajnef, Vinassa, Briat, El Brouji, et al., 2007). The online method is based on the determination of charge resistance Rcy_c and the capacitance C_{cyc}, unfortunately, a detailed description of how the method was conducted was nebulous and was not provided by the authors. Chaari et al. (2011) (Chaari et al., 2011) also employed an online characterization method. The method was based on the determination of the capacitance and ESR which was in turn based on the voltage response to the current profile.

Perhaps, the use of EIS for age monitoring was best demonstrated by Brouji et al. (2008) in (Brouji, Briat, Vinassa, Bertrand, & Woirgard, 2008). To appreciate the significance of the data, they proposed a generic model that was built on the initial state of the SC. The model was based on the main physical description of the porous electrode and the electrode-electrolyte interface. The model parameters were identified using EIS. While the SC was going through ageing, these parameters also changed. The authors found that these parameters changed differently and were very much dependent on the type of ageing tests. Therefore, they compare the evolution of these parameters between two ageing tests: calendar life test and power cycling test, to identify the ageing mechanisms.

Outside the SC ageing research sphere, EIS as a diagnostic tool has been practised widely in the study of battery ageing. Hafsaoui and Sellier (2010), for instance, have employed a method whereby an initial model is built, which then is used as the reference model, and then the corresponding model parameters are periodically monitored throughout the different stages of battery life in order to follow the

evolution of the battery behaviour, which in turn, produced a numerical model of battery ageing that is able to simulate the dynamical voltage response of the battery as a function of current and temperature (Hafsaoui & Sellier, 2010). The model, based on an electrochemical model, simulates various physical phenomena observed, like diffusion, charge transfer, just to name a few, as battery experiences ageing.

2.5.7 Ageing Models

The lifetime of SCs can be quantified, for example, by plotting capacitance against time and deriving its mathematical relationship. In (Alcicek et al., 2007), the SC lifetime is calculated based on the law of Arrhenius, which is written as,

$$v = A \cdot e^{-\frac{E_A}{kT}} \tag{2.4}$$

Where, v: Reaction velocity; E_A: Energy activation in eV; k: Boltzmann constant; A: Factor of Arrhenius; T: Absolute temperature in K.

A similar approach has been adopted in (H. Gualous et al., 2010) to determine SC lifetime. The lifetime model is formulated by taking the inverse reaction rate of the Arrhenius law,

$$t_i = Be^{\frac{E_A}{kT_i}} \tag{2.5}$$

Where, t_i: The reaction time for T_i in hour; T_i: Absolute temperature i in K; B: Parameter to be determined

Equation (2.5) allowed the calculation of the energy of activation that will give the variation of the lifetime as a function of temperature at a fixed voltage of 2.7V. The

average life expectancy can be estimated by the accumulated useful life (wear) of a SC in function of a dynamic voltage profile as shown in Figure 2-22.

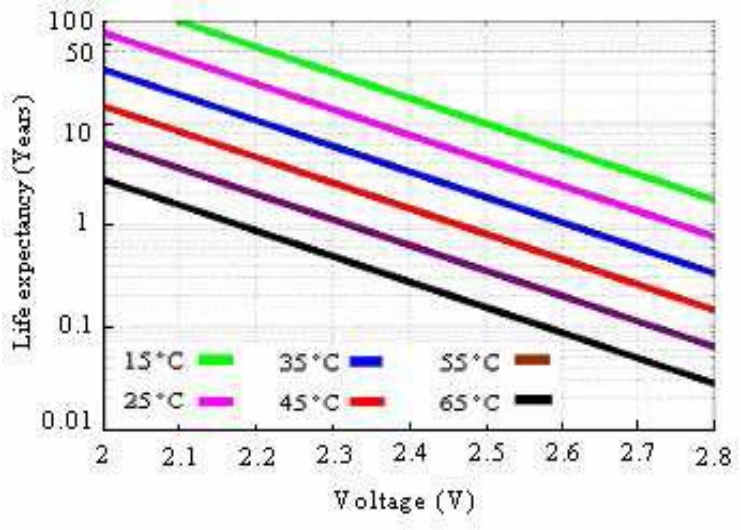


Figure 2-22: Life expectancy of a supercapacitor in function of operating voltage and temperature (Diab et al., 2006)

Uno and Tanaka (2012) proposed a cycle life prediction model that makes use of the acceleration factor and activation energy determined from the Arrhenius equation (Uno & Tanaka, 2012). The work can be traced back to Umemura et al., (2003) where they found that the degradation mechanism in SC is governed by the Arrhenius law, therefore, enabling the determination of the activation energy of a particular degradation process. Kötz et al. (2006) used the activation energy to determine the leakage current for a temperature range between $0℃$ to $60℃$ (Kötz et al., 2006). Kötz et al. (2006) reported that the acceleration factors of 2 can be expected for every $10℃$ increase in temperature. Uno and Tanaka (2012) reported an acceleration factor of 1.2 for the temperature range of $0℃$ to $40℃$, which signifies that the degradation occurs at a rate of 1.2 times faster for every $10℃$ increase.

Besides those, another method is based on the quantification of ageing through EIS measurements. This technique allows for a mathematical relationship of impedance parameters with stress level to be derived. Ageing directly affects the impedance spectra; thus, fitting a circuit model to the spectra and obtaining circuit parameters at various ageing states was done in (Bohlen et al., 2007a) to obtain an ageing trend. Therefore, the circuit model allows for the extrapolation of the ageing test results as a function of voltage and temperature, for the case in Bohlen et al. (2007a). In Part II of their work (Bohlen, Kowal, & Sauer, 2007b), the ageing model was improved to provide electrical and thermal simulation for a more holistic ageing model. The thermal simulation of their model showed the temperature distribution in the module after seven years simulated service time; the SC cells were hotter as they were placed closer to the hot wall. If the differences of temperatures between SC cells in the module were not addressed, this situation could lead to different ageing rate between cells. Moreover, the internal heat generation during operation will cause self-accelerated ageing processes. The holistic model will, therefore, be beneficial in the stack design and the cooling system design.

Omar et al. (2013) (Omar et al., 2013) argued that to model SC long-term performance, the model should not be based on fixed parameters. Therefore, they proposed a model based on three levels: (1) electrical model, (2) thermal model, and (3) lifetime model. The third level, the lifetime model, was based on following the evolutions of the calendar and the cycling tests at different conditions and formulating the relationships between the results. The authors, however, do not explain in detail how the process is conducted.

Concerning the heat generation during operation, particularly in HEV application, where the very large current rate to charge and discharge the SCs produces a considerable amount of heat, Gualous et al. (2007) (H. Gualous, Louahlia-Gualous, Gallay, & Miraoui, 2007) proposed a thermal model based on the finite-differential method. The proposed model took into account the material, structure and packaging properties. As the SCs went through a charging/discharging regime, the temperature increased exponentially with time as a result of accumulated heat. The heat transfer in SCs can be attributed to (1) conduction, (2) convection, and (3) radiation. A temporal evolution of the SC temperature for different charge and discharge current values was proposed. An update of their work can be found in (Hamid Gualous et al., 2009). D'Entremont and Pilon (2014) proposed a spatiotemporal physical model that took into account the irreversible Joule heat generation and the reversible heat generation due to diffusion, steric effects and entropy changes (d'Entremont & Pilon, 2014).

The evolution of ESR and capacitance as ageing proceeds have been used as ageing indicators and parameters to predict and calculate the lifetime of SCs in SC health diagnosis. Soualhi et al. (2013) predicted the ageing of SCs by monitoring the ESR and the capacitance, and this information was used to train neo-fuzzy neuron (NFN). In A. Oukaour et al. (2013), the evolution of ESR and capacitance from the beginning of ageing was realised by using least squares algorithm. The SC diagnosis method proposed in (Amrane Oukaour et al., 2013) calculates the correlation between capacitance loss as a function of ageing time by measuring two different points, M_1 and M_2 on the voltage-time charging curve. Similar approach of using an experimental dataset to establish the ageing model was also proposed in (Ayadi et

al., 2013). The ageing model consists of two parts, to take into account the two stages of SC ageing: the first stage involves a rapid chemical break-down in the SC structure, represented by the sum of an exponential part, and the second stage involves a slower process and it is related to the diffusion phenomenon, represented by a square root of the time function (Naim, 2015).

2.6 Summary

Performance improvement in supercapacitor technology has been a growing interest over the years, while some researchers focused their research on improving supercapacitor materials and cell designs, this research work takes a preventive method of improvement through diagnostics. Performance reliability on existing cell in the market today are not fully understood, especially in EV/HEV operations. There are many studies reported in literature, investigating the effect of voltage, temperature and cycling on SCs. While these studies successfully describe the ageing characteristics of SCs and add to the general understanding about the system, this knowledge has not been utilized to develop an ageing model that is not only able to elucidate failure mechanisms seen during degradation processes, but can also shed light on the dynamic interactions between ageing and electrical behaviour of the SC.

Therefore, to study ageing in SCs and also facilitate this research work, literature backgrounds in supercapacitor modules, voltage equalizations circuits within modules, supercapacitor ageing factors (temperature, voltage and cycling effects on ageing supercapacitor with methods of quantifying the factors) and finally ageing models was researched and documented in this chapter.

Observing ageing effects in supercapacitors is a long-term process; which takes between months to years, as demonstrated with subsequent chapters.

CHAPTER 3- METHODOLOGY

3 Outline

The reliability and performance of SCs in Electric Vehicles (EVs) are crucial as they relate to applications which involve the peak power demands and/or energy storage. As mentioned in section 1.2.1, an electrochemical reaction limits the life expectancy of a SC and eventually jeopardises the whole system. The voltage system of an EV is higher than the voltage system of a single SC, therefore the SC has to be connected in series to form a "module". As a result of the operations of the EV system and the over-voltage of a SC realised in a series module, a single failed/deteriorated SC could easily stop operations of the whole system of an EV without warning. To ensure the safety and reliability of the SC module, it is rather important to predict the EOL of a SC or the ageing behaviour of a SC under EV applications, and also to explore the mechanism behind the failure.

The life expectancy of SCs under normal conditions as predicted by Bohlen, Kowal, & Sauer, 2007 is in the range of 10-20 years for voltages below the rated maximum voltage and at room temperature, although a SC used in a system, especially in EV application, may not operate under these nominal conditions. The life expectancy of a SC should be revised to include the factors affecting the ageing behaviour due to the system operation modes coupled with the SC manufacturers' datasheet. According to the rule of thumb, the ageing rate doubles if either the SC voltage is increased by 100mV or the temperature is increased by 10K (Bohlen et al., 2007a). Depending on the applications, the general agreement for the EOL criteria is 20% loss of capacitance and/or more than 100% increase of the ESR (H. Gualous et al., 2012).

In this research, the ageing behaviour of a commercial Maxwell (25F, 2.7V) SC operating alone and in a module under accelerated degradation conditions was investigated. These tests were carried out until the SC developed an abrupt loss of performance (i.e. exhibit a short circuit with no stored charge) or when either one of the EOL criteria was exceeded.

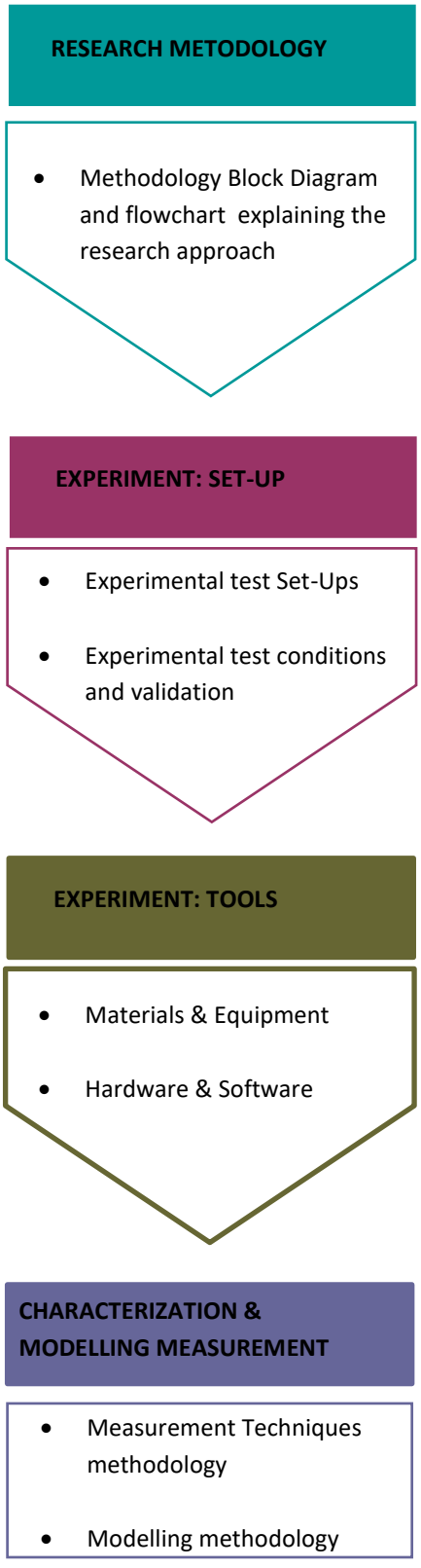


Figure 3-1: Methodology Overview

3.1 Research Methodology

A methodology is drawn up to examine SC reliability/behaviour and also to analyse its lifetime leading to the EOL under different conditions. For some years now organizations and pioneer researchers in the field of ELDCs (energy storage) have come up with different standards and various testing methods to measure, characterize, quantify and determine EOL of SCs. A list of such organizations compiled by Naim, 2015 include: IEC (International Electrochemical Commission), USABC (United States Advanced Battery Consortium) EINEL (Environmental Idaho National Engineering and Laboratory), EUCAR (European Council for Automotive R&D) (EUCAR Traction Battery Working Group, 2003), UC Davis (University of California Davis) (Miller & Burke, 1994) and HCV (Hybrid Commercial Vehicle) (H. Popp, 2010); manufacturer documents and datasheets (Current & Characterizations, 2009; Technologies, n.d.-b) (Alon, 2012) (Idaho & National, 2008) (Stryzhakova, 2012; Usabc, 1996); and journal papers(Kötz, Ruch, & Cericola, 2010) (H. Gualous et al., 2010)to name a few.

To further expatiate on SC ageing tests, testing methods governed by the two predominant factors, (i.e. voltage and temperature which are the main influence of ageing in SCs), had been investigated by some prominent research papers as summarized below:

Hammer et al. (Hammar, Venet, Lallemand, Coquery, & Rojat, 2010) had studied the ageing acceleration of SCs in transport applications, focusing on applications of SCs in power and railway systems, thus subjecting the SCs to power cycling using current profiles similar to railway applications. Uno et al. (Uno & Tanaka, 2011b) had studied

the ageing acceleration in SCs by power exerting charge-discharge cycles on the SCs; then going further to establish a lifetime model for SCs based on the Arrhenius law. Bertrand et al. (N. Bertrand, Briat, El Brouji, & Vinassa, 2010) had studied the cycling of SCs using HEV cycles. H Gualous (H. Gualous et al., 2012) also investigated the ageing acceleration in SCs as a function of voltage, temperature, and charge-discharge cycling solicitations. Bohlen et al. (Bohlen et al., 2007a) investigated accelerated ageing in SCs using a holistic model that combines electrical and thermal simulations of SCs module. This is just to name a few of the papers that investigate the ageing accelerations in SCs, and all of them have shown that the ageing of SCs is relative to voltage and temperature factors as mentioned above.

- **Voltage factor**

In an ideal case, the energy storage in SCs takes place in the electrode interfaces without chemical reactions. As a result of that, Bohlen et al., 2007 insinuates that the ageing of the SCs is independent of the repetitive cycles (constant current). The maximum voltage of a single SC, which is limited by decomposition of the electrolyte is about 5V, and therefore the slight increase in voltage of a SC beyond the maximum value (known as over-voltage) causes the presence of impurities in the electrodes and the electrolyte known as a redox reaction. This reaction accelerates the degradation of the electrolyte.

- **Temperature factor**

Temperature is another main factor used in accelerating the ageing of SCs. Its effect is seen in the chemical reactants, were evident by an increase/decrease of the

temperature above/below the normal temperature, increasing the reactivity of the chemicals in the SCs. Bohlen et al., 2007 explains that cycling at high current also increases general and localized temperatures caused by Joule-effect losses. However, in this research different low current values were explored and investigated, and the current criterion was chosen to be as high as 2A.

According to literature, it can be gathered that when investigating the end of life of SCs, the testing modes referred to are mostly;

1. **Temperature test:** SCs are placed in a climatic chamber under specific thermal conditions for a period of time.
2. **Constant Voltage test:** SCs are charged up to a specific value and stopped, this constant voltage is being observed for a period of time at room temperature.
3. **Calendar ageing test:** This ageing test is carried out on SCs by maintaining the samples at constant voltage and temperature. The voltage and temperature are varied by different researchers depending on the focus point of the research.
4. **Cycling test:** main aim is to induce self-heating on SCs, by using chargers that adopt constant current CC or constant voltage C-V charging schemes. In most cases this cycle implements a current profile suitable for the desired application. To accelerate the ageing process of SCs, researchers have gone ahead to induce thermal effect to this mode of testing. In other words, cycled samples are subject to temperaments below/above the nominal (room) temperature.

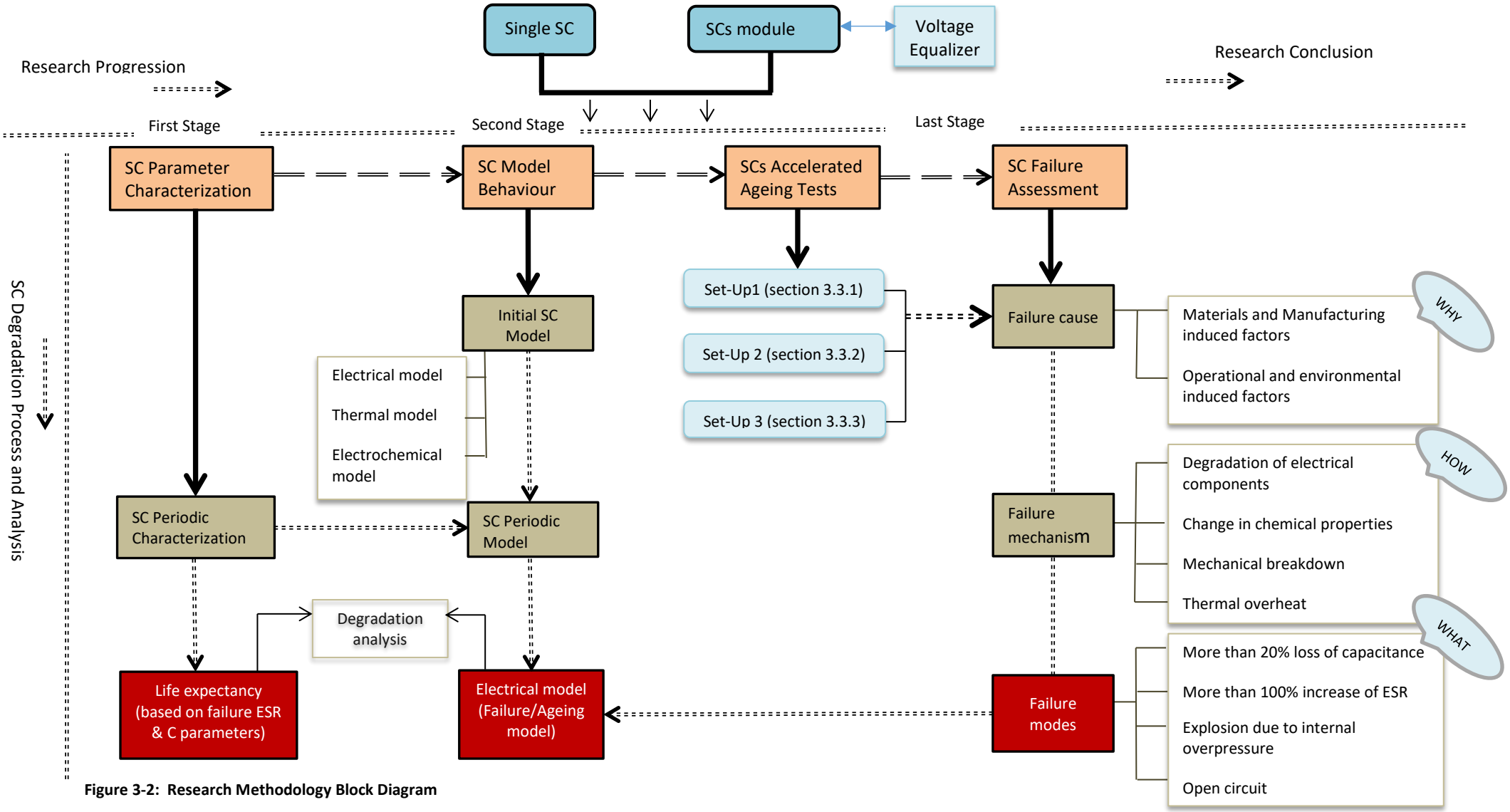


Figure 3-2: Research Methodology Block Diagram

Figure 3-2 is a block diagram showing a step-by-step methodological process of assessing the EOL in SCs. The figure is subtly divided into three stages of interest in this research work. Though divided, the three stages are connected and dependent on one another.

In the first and second stages, the ageing phenomena in SCs were quantified and analysed by conducting characterization tests, to determine the mechanism of failure and also model the electrical ageing behaviour of SCs. To determine the baseline upon which SC EOL is built and analysed, an initial parameter characterization and equivalent electrical circuit EEC were developed to create a foundation. After which, periodic characterization tests were used in the second stage to explore the possibility of developing a timeline on the life expectancy of SC EOL from the failure parameters during characterization. At the second stage, an electrical model (failure model) was developed to explain the degradation process using electrical parameters of the SC affected by the failure. This stage is known as the model failure representation of SCs.

The Last stage is a block compilation (situated at the extreme right with a downward degradation progression) of the failure assessments in both single SC and module SCs. This stage is vital in determining and evaluating the ageing criteria for SCs, the performance evolution of SCs degradation, and the failure assessments leading to the EOL. In other words, questions on what, why and how SCs fail were summarized at this stage. The methodology process started with this stage by determining the cause of failure, hence the accelerated ageing tests

The characterization tests carried out to fulfil the analysis in stage two and three are Electrochemical Impedance Spectroscopy, Cyclic Voltammetry, and Constant Current charge-discharge test using a Potentiostat/Galvanostat PGSTAT320N and controlled by software Autolab NOVA 1.10.3.

SC failure is arrested by determining the cause, mechanism and mode of failure.

The term that describes **WHY** SCs fail is called "Failure cause"; SCs usually start deteriorating at the early stage of manufacturing deign/process, or further back at the material development stage; this can be described as the early causes of failure. During SCs applications, operational factors such as overvoltage, overcurrent, and overtime, or the environmental factors such as temperature, humidity, vibration or shock are the main cause of failure (Group,; Peter Kurzweil, Frenzel, & Hildebrand, 2015; Roland Gallay, 2012; Supercapacitor, 2014). However, in this research, SCs were subjected to preconceived accelerated tests categorized in three set-ups as shown in figure 3-2, the test methods exerted being based on the operational and environmental failure factors of SCs shown in the same figure.

"Failure mechanism" is a term used in describing **HOW** SCs fail; the factors instrumental in inducing such stress that leads to SCs failure are categorized as mechanical, thermal, chemical or electrical stress. These stress factors lead to modes of failure such as swelling/bulging, overheating, pressure build-up, gas generation, corrosion, to name a few (Group; Roland Gallay, 2012)(Azaïs et al., 2007)

"Failure modes" are **WHAT** describes the physical behaviour of a failed SC; this description according to Gualous et al., (2012) has two recognizable modes:

The early failure mode is caused in the production/manufacturing stage due to design and process weaknesses that were not detected during development. The production variation is caused by tool wear, operator changes or lack of formation. This mode of failure is mostly detected during the screening routine tests performed by the manufactures.

The wear out failure mode occurs mainly during operational and environmental applications, and the main failure mechanism is the opening of the container due to an internal overpressure (Hahn, Kötz, Gallay, & Siggel, 2006) (Kötz et al., 2010). Ageing factors, voltage, and temperature increase the build-up of gas pressure due to electrolyte decomposition inside the cell, which consequently increases with operational time and gradually weakens the mechanical function, though leaving the electrical functions working. The electrical functions affected by the failure mode are the capacitance and the internal resistance due to electrolyte leakage.

Test methods applied in this project are for the sole purpose of accelerating the ageing in SCs, and both SC single accelerated tests and SC module accelerated test (tests use an EV operational behaviour) are investigated. The failure modes expressed by these methods of testing are summarized below:

- Cell container opening due to an internal overpressure (Hahn, Kotz, et al., 2006). The voltage and the temperature generate a gas pressure inside the cell which increases with the operation time. When the pressure reaches a determined limit, a mechanical fuse, generally a groove on the can wall or a pressure relief, may open softly, avoiding an explosion of the device.
- More than 20% capacitance loss of the electrode. The accessible carbon surface and the ions availability are reduced during the electrochemical cycling.
- More than 100% increase of the equivalent (ESR). The electrode adhesion on the collector is weakened in time by temperature, and the ion availability is reduced.

For a single SC cell, the mode of failure is as a result of the modes mentioned above;

In applications with high voltage system, the SC are connected in series to form a "module" to meet system requirements. In this case, the failure mode is characterized by a "short circuit" with ESR rising to infinity, as a result of electrolyte loss over time or the absence of voltage management circuit in a SC module, in addition to the three main failure modes mentioned above. The instance any of the failure modes mentioned above is evident in any single SC, that component must be replaced, or the whole system is jeopardised. However, in a system with more than one SC, the life expectancy decreases significantly even more than a single SC, as a result of over-voltage coupled with the possibility of uneven temperature distribution across the module. A voltage equalization circuit is therefore introduced into the

system in this research project, to balance the voltage across the module evenly, thereby increasing the life expectancy of the system.

Many system applications require SCs to be connected, in series and/or parallel combinations, to form a “module” with a specific voltage and capacitance rating for the application to operate at high voltage level or low current level (Sirmelis & Grigans, 2011). The most critical parameters for all capacitors, including SCs, are the voltage rating, capacitance, ESR, and EPR. Subjecting almost any capacitor to a substantially higher voltage than it was designed to withstand usually results in an irreparably damaged, nonworking capacitor. This is especially true for SCs, so they must be protected from overvoltage conditions. As mentioned above, for a series or parallel connection, the voltage rating, the capacitance, and the ESR (as the EPR is negligible) of the whole supercapacitor module were taken into account (illinois capacitor; Sirmelis & Grigans, 2011).

In this project, only the serial connection was exercised because the interest was to increase the voltage rating and the ESR of the system while maintaining the capacitance of a single SC.

Parameters, such as the capacitance and the ESR expressed in SC failure modes are electrical functions of the SCs that can be quantified by subjecting the SCs cells to periodic characterization methods in between accelerated testing employed in this project (as shown in figure 3-1). At first, the characterization of the SCs cells were conducted to measure the initial parameters and conditions before subjecting them to any form of accelerated testing.

The characterization methods employed in this research entailed the use of measuring tools such as: Electrochemical Impedance Spectroscopy, Cyclic Voltammetry, and Constant Current charge-discharge test

1. **Cyclic Voltammetry test:** This test method was one of the measurement methods used in this research and is recognized by P. Kurzweil & Chwistek, 2006 as the most precise and incorruptible method of determining rated capacitance (one of the SC parameter).
2. **Constant Current charge-discharge test**: This test method of measuring SCs was carried out in the time-domain analysis of the voltage response to constant current profiles with rest periods. In this measurement test, the initial and final parameters C and ESR were recorded and analysed, and a comparison of initial and final profile behavioural analysis made in determining life-expectance. This voltage response also helped in failure diagnostics and determining the mechanism of failure by explaining each periodically characterized profile and comparing it with the expected results.

   These measurements could determine the ageing behaviours and parameters. Parameters such as the capacitance and the ESR could be extracted from the voltage response; these two parameters were solely used in developing a time scale related to the ageing factors by collecting period parameters during accelerated tests. The time-line could only be limited to the specific method of ageing acceleration from which the parameters were retrieved, but this could not tell us much about the life expectancy.

Therefore, different accelerated tests using testing methods and profiles designated for that specific application need to be evaluated to determine the life- expectancy of a SC of any design.

3. **Electrochemical Impedance Spectroscopy test:** is a useful experimental method carried out in the frequency domain for parameter identification of SCs dynamic electric models (Karden, Buller, & De Doncker, 2002). These parameters were decoded by analysing the frequency spectrum of a SC. This experimental method helped to extract further parameters that defines a dynamic electrical model of SCs which was not static but which evolved into another "form" different from its initial model, as the accelerated tests were conducted.

After parameter characterization, the dynamic model of the SC evolving in degradation was quantified by the parameters collected from both the time domain and the frequency domain. This evolution explains the degradation of the SC at different time and frequency levels of the modelled spectrum.

The SC dynamics take place in a very wide range of time constants, starting from microseconds up to several years. This range may be divided into three: short-term effect, mid-term effect, and long-term effect. The short-term effect would take place between 10 kHz to 1 kHz in the frequency domain, or in minutes in the time domain, which relates to the operation effect and cell design. Mid-term effect would takes place between 1Hz to 1kHz in the frequency domain, or in hours in time domain with

regard to the charge redistribution phenomenon and double layer effect and finally, the long-term effect (1Hz to 10mHz frequency) caused by operation regimes and ageing (Rafik et al., 2007).

In this project, different materials, laboratory equipment, and electronics were employed to carry out the necessary measurements and analyse the data required. These tools, their purposes and how they were assembled will be discussed later in this chapter.

Experimental flow process, setup, timeline and reasons behind each experiment carried out will also be addressed and quantified in this chapter.

3.2 Experiment: Set-Ups

A detailed explanation of the experiments carried out and the experimental set-up are being discussed in this part of the project. The experiments were carried out to investigate SC degradation in single SCs and SC modules which were divided into three experimental set-ups:

3.2.1 Set-Up1

The first set-up was proposed to establish a reference line to this area of study by first putting to test the fundamental factors of SC failure as mentioned in section 3.2 (i.e. voltage and temperature). The tests carried out in set-up 1 as illustrated in Figure 3-3 was solely for single SCs, and three SCs samples **T2, M3, and M4** were subjected to explore three sets of tests, which were:

1. Temperature test

2. Constant Voltage test

3. Calendar test

Before the main experimental procedure stated above commenced, an initial model using the first sample **M1** was created from characterization test conducted under a wide range of conditions on frequency and time (to satisfy EV applications)

SC test samples	Test	Voltage (V)	Temp (°)	Cycle/Time periods	Rest time	Characterization tests/modelling
M1	Initial Model	0	Room	Initial	-	CV;CC;EIS/Circuit
T2	Temp. Test	0	75-85	Every 144H	24H	CV;CC;EIS/Circuit
M3	Const. Volt test	2.7	Room	Every 144H	24H	CV;CC;EIS/Circuit
M4	Calendar test	2.7	75-85	Every 144H	24H	CV;CC;EIS/Circuit

Table 3-1: Set-Up1 - Experimental Test Description

Each test sample **T2, M3, and M4** was subjected to individual test conditions tabulated above. After every 144h, the samples took 24h breaks to recuperate the machines and also to conduct characterization tests. These characterization tests (CV, CC, and EIS) were done immediately after every 144h test cycle and after every 24h rest time (before putting it back into the test chamber) to gather the necessary data used to quantify the test samples and also record a timeline in the degradation process of the samples.

1 week	144H
2 weeks	288H
3 weeks	432H
1 month	576H
2 months	1152H
3 months	1728H
4 months	2304H

*should take weekly breaks after every (144H)

*the cycle/time periods should be gradual for each SC (sample) moving from the initial period to the end of each experiment.

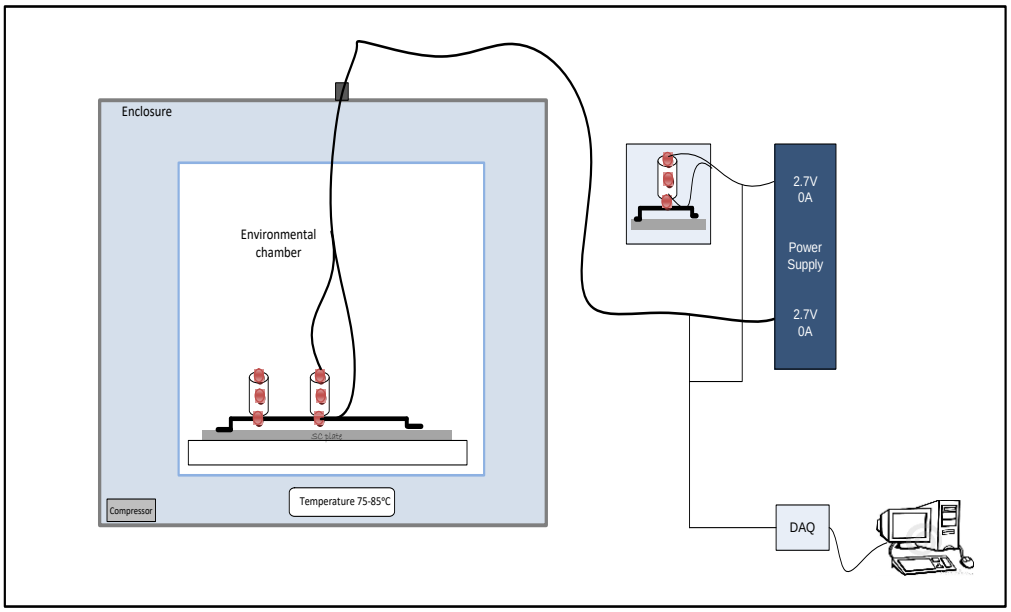


Figure 3-3: Set-Up 1 - a block description of the test bench for SC samples T2, M3, and M4

SC test samples	Set-Up 1 description
T2	Sample is immersed in an environmental chamber under high temperatures
M3	Sample is charged up to the maximum rated voltage $2.7V$ and retained at that value for the duration of the test
M4	Sample subjected to both high temperature and high voltage of $2.7V$ at the same time for the duration of the test

Table 3-2: Set-Up 1 – SC Sample Description

3.2.2 Set-Up 2

In the Second experimental set-up, SC module under cycling conditions were the main tests investigated in this part of the experiment as illustrated in Figure 3-4. Five sets of two $2.7V$ SCs connected in series (with and without a voltage equalization circuit) to form a module with a voltage rating of $5.4V$ were subjected to a series of constant current cycling tests represented in part A and B below.

3.2.2.1 Set-Up 2: Part A

SC module in this part employed a 'charge/discharge circuit 1' which acts as a switch; the module was then charged with a $500mA$ DC constant current till the voltage of the module reached its voltage limit of $5.4V$, and then the module was immediately discharged by reversing the current direction till its voltage reached to $0V$. This process of charge-discharge cycle continues until the operation is manually stopped.

In part A, three sets of two SC modules (with and without a voltage equalizer of some kind) subjected to some charge and discharge cycles using 'charge/discharge circuit 1' were investigated. The reason behind these tests was to compare the performance of the three SC modules so as to understand the effect of the voltage equalization circuits on SC modules as regards to temperature, voltage and life cycle.

SC test samples	Charging current (mA)	Temp (°)	Cycle/Time periods	Rest time	DAQ	Characterization tests/modelling
W5 & W6	500	75-85	Every 144H	24H	Voltage profile & Cycle counter	CV;CC;EIS/Circuit
B7 & B8	500	75-85	Every 144H	24H	Voltage profile & Cycle counter	CV;CC;EIS/Circuit
C9 & C10	500	75-85	Every 144H	24H	Voltage profile & Cycle counter	CV;CC;EIS/Circuit

Table 3-3: Set-Up 2 Part A – test description

Experimental data from the three sets of SC sample modules was collected using a DAQ (from a computer) during the charge/discharge tests cycles every 144h. The DAQ was used to monitor the voltage profile and number of charge/discharge cycles accumulated during the tests, including the 24h break characterization tests for the quantification and illustration of individual test samples degradation course.

3.2.2.2 Set-Up 2: Part B

SC module in this part employed a 'charge/discharge circuit 2' which acts as a switch, by charging the SC module with a $600mA$ DC constant current till its voltage reached a voltage limit of $5.4V$, then switching to discharge to a $5V$ DC motor (to stress SC module) till its voltage reached $0V$. This process of charge-discharge cycle would continue until the operation was manually stopped. After the results were acquired from part A, it became necessary to conduct more study on the effect of voltage equalizer especially when subjected to load stress (dc motor load). Comparison between the two equalizers during the experimental load tests used in this project as relates to the balancing technique employed by the circuits was the main focus of interest in this part. DAQ was also used to monitor and collect data from the 2 sets of SC sample modules during the charge/discharge test cycles every 144h as demonstrated in part A.

SC test samples	Charging current (mA)	Temp (°)	Cycle/Time periods	Rest time	DAQ	Characterization tests/modelling
MtA & MtB	600	75-85	Every 144H	24H	Voltage profile and Cycle counter	CV;CC;EIS/Circuit
MtC & MtD	600	75-85	Every 144H	24H	Voltage profile and Cycle counter	CV;CC;EIS/Circuit

Table 3-4: Set-Up 2 Part B – test description

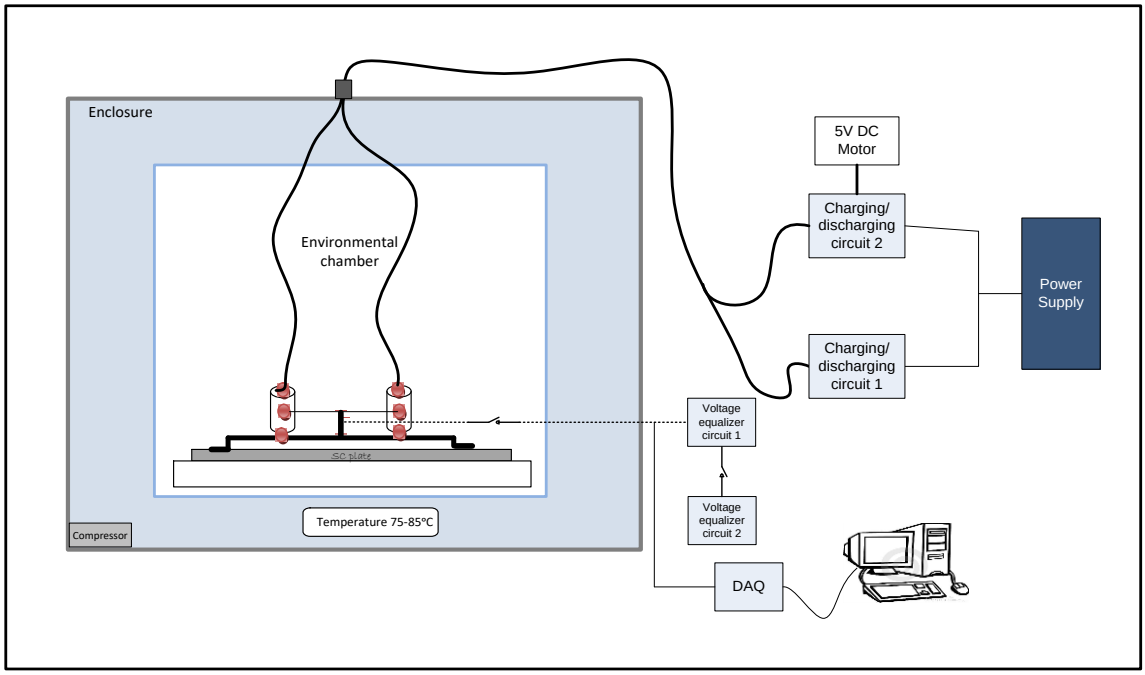


Figure 3-4: Set-Up 2 - a block description of the test bench with five sets of SC sample modules

SC test samples	Set-Up 2 Description
W5 & W6	A serially connected module submerged in an environmental chamber was subjected to charge/discharge cycles using charging/discharging circuit 1' under high temperature, without any form of voltage equalizer for balancing the voltages between the 2 SCs in the module
B7 & B8	This module was subjected to charge/discharge cycles using 'charge/discharge circuit 1' under high temperature, with 'voltage equalization circuit 1' (a modified design) to balance the voltage between the 2 SCs in the module
C9 & C10	This module was subjected to charge/discharge cycles using 'charge/discharge circuit 1' under high temperature, with 'voltage equalization circuit 2' (a Maxwell commercial equalization circuit) to balance the voltage between the 2 SCs in the module
MtA & MtB	This module was charged up to the maximum rated voltage and immediately discharged to the $5V$ DC motor load for many cycles using 'charge/discharge circuit 2' under high temperature, with 'voltage equalization circuit 2' (a Maxwell commercial equalization circuit) to balance the voltage between the 2 SCs in the module
MtC & MtD	This module was charged up to the maximum rated voltage and immediately discharged to the $5V$ DC motor load for many cycles using 'charge/discharge circuit 2' under high temperature, with 'voltage equalization circuit 1' (a modified design) to balance the voltage between the 2 SCs in the module

Table 3-5: Set-Up 2 - SC Module Sample description

3.2.3 Set-Up 3

This set-up employs a charge/discharge profile (acquired from a customised 'charging circuit and variable load discharging circuit') to charge/discharge the supercapacitor modules in cycles as illustrated in Figure 3-5. A set of three $2.7V$ SCs were connected in series with 3 'voltage equalization circuits 1' to form a module with a voltage rating of $8.1V$. The 3 SCs module was charged up with a current limit of $2A$ to be discharged to a $12V$ DC Brushed Permanent Magnet electric motor by a programmable load, represented in the set-up below.

The 'charging circuit and variable load discharging circuit' were programmed to generate different charge/discharge profiles, on the voltage range and the load motor speed selected. The 'variable load discharge circuit' provided the option to select manually the voltage range for charge/discharge profile (i.e., for a selection of $0V - 8.1V$, the SCs module was set to charge and discharge between $0V - 8.1V$) and also the option to select the speed of the motor; however for the load speed, this is in between the ranges of $120rpm$ to $220rpm$ and could be programmed to a specific speed level. The circuit also had the option of auto charge/discharge using random (auto) load speed selection.

A set of 3 SCs in a module, balanced with 3 'voltage equalization circuits 1' were charged up by a programmable 'charging circuit 1' and discharged by a 'variable load circuit 1' to a 12V DC Brushed Permanent Magnet electric motor. The charge/discharge profiles would be varied on a weekly basis as exhibited in Table 3-6. No particular EV drive cycle profile was considered during the selection process of the voltage range and load speed, as the primary aim was to accelerate the test levels

of the SCs module. However, the test validation and test conditions are explained in detail in section 3.3.4.

Selected voltage charge/discharge profiles 6, 7, 8, 9 (see Table 4-5) based on SC voltage and motor speed as shown in (Table 6-13) with explanations of the wave forms.

SC test samples	Voltage profile	Load Profile	Temp (°)	Cycle/Time periods	Rest time	Characterization tests/modelling
A; B; C	Voltage Profile 6	Load Profile 1	85	Every 144H	24h	CV; CC;EIS/Circuit
A; B; C	Voltage Profile 7	Load Profile 2	85	Every 144H	24h	CV; CC;EIS/Circuit
A; B; C	Voltage Profile 8	Load Profile 3	85	Every 144H	24h	CV; CC;EIS/Circuit
A; B; C	Voltage Profile 9	Load Profile 4 (Auto)	85	Every 144H	24h	CV; CC;EIS/Circuit

Table 3-6: Set-Up 3 Test description

Charge/discharge cycles were carried on the SC module A; B; C; for the duration of the experiment; although a rest period of 24hrs was required to recuperate the samples and the machine, and then the cycle continued till an eminent SC

degradation trait was established. Experimental data in set-up 3 was gathered and analysed the same way as the method used in set-up 1 and 2.

Set-up 3 comprised of collective circuits including a boost circuit, a charging circuit and a variable load circuit designed to fulfil charge/discharge profiles, on a set of three SCs module A; B; C; for experimental and investigative purposes. In this set-up, the module was charged up to a certain voltage (not necessary the maximum voltage) and also discharged to a certain voltage (not necessary the minimum voltage). This process was repeated continuously different voltage levels with load speeds to satisfy the required outcome of the different charge/discharge profiles 6,7,8,9 till the device is manually disconnected.

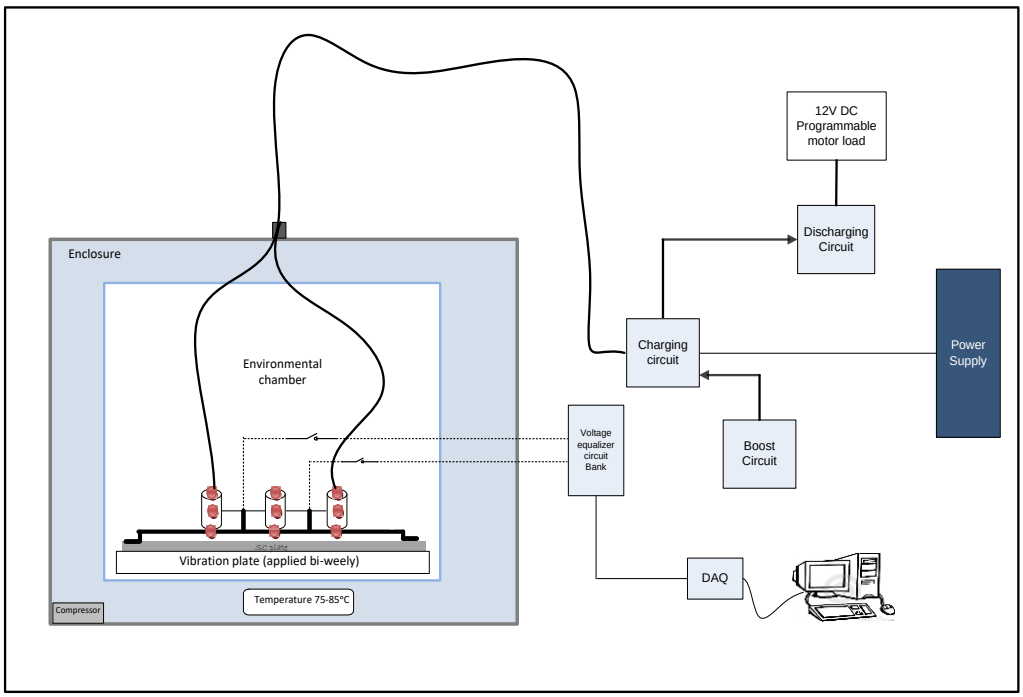


Figure 3-5: Set-Up 3- a block description of the test bench for SC samples module A, B, & C

3.2.4 Experiment: Test Conditions and Validation

The experiments carried out in this research work were for the sole purpose of accelerating SC end-of-life (EOL), as such predominant factors (i.e. the electrical and thermal conditions) responsible for the degradation of SC are crucial to this study.

- Thermal Factor

The temperature conditions applied in the experiments and carried out in this research work were between the ranges of $75^0C - 85^0C$. Although, this temperature range seemed harsh/abusive as the general boiling point of electrolyte is 81.6^0C (H. Gualous et al., 2012) (Alcicek et al., 2005). However, with reference to Kötz et al., 2010, H. Popp, 2010, Doughty & Crafts, 2006, this temperature condition is acceptable for SC accelerated ageing test in EVs and HEVs and in agreement with the datasheet (Technologies, n.d.-a) Operating temperature of the SC samples.

An initial temperature of 75^0C was first applied in set-up 1 (section 3.2.1) and set-up 2 (section 3.2.2) then gradually increased to 85^0C as shown in tables 3-1 and 3-3 respectively. While in set-Up 3 as shown in table 3-6, a temperature of 85^0C was used throughout the experiment to accelerate the ageing properties.

- Electrical Factor

In conjunction with the thermal effect on the SC samples, cycling test was also conducted during these experiments. The cycling tests varied with each experimental set-up to produce a methodological approach of assessing SC reliably. The voltage profiles generated from both set-up2 (section 3.2.2) and set-up 3 (section 3.2.3) were

all in one way or another (although not specifically) in respect to the power requirements according to acceleration/breaking or start/stop operations for normalized EV and HEV profile (Briat et al., 2006).

According to FreedomCAR test manual, the methods for testing SC lifetime and performance are based on either thermal, voltage, carlendar, cyclic, varing or constant load test (Ne-id, 2004). However the procedure and electronics employed in this work were chosen to satisfy the research work, just as; (S. H. Kim & Choi, 2009) (Kotz et al., 2010).

The electrical and thermal conditions defined in this work were selected to observe ageing rather quickly, therefore test phases, cycling duration, and rest time were chosen purely to protect the intergrity of the experimental results by providing a reasonable recuparative time for the laboratory equipments and a rest time needed to characterize the test samples. The values selected understandable random, is similar to values adopted by many research works, such as; (H. Gualous et al., 2012)(Amrane Oukaour et al., 2013).

3.3 Experiment: Tools

The tools used during this project have been categorized and tabulated into four tables based on their purposes, which are: Laboratory Equipment, Instruments, software, and hardware: power electronics.

The main material of interest and focus on this project is the supercapacitor SC. About three different commercial SC brands were examined, and a single brand was chosen to be analysed. The SC standard and specifications are explained below. Meanwhile Tables 3.7 to 3.10 explains the tools used in this project.

Equipment	Description	Experimental Use
Environmental Chamber **Model 7102-1** **By RANSCO**	Environmental chamber. Temperature range: -70℃ to +200℃	Thermal applications
Compressor and cooling system	Compress cool air pressure	Used in assisting the chamber from over-heating
Fibre glass product tray **TwoYSP Marketing & Trading**	A customised product tray to hold SC under test	SC holder
Wires	Temperature resistance wires	Used for connection in the chamber
Power Supply GPS-3303 **GW Instek**	3-Channel Power Supply	Used in powering the power electronics involved this project

Table 3-7: List of laboratory equipment

Instrument	Description	Experimental Use
NI USB-6212 **National Instruments**	16 analogue input data acquisition device	Use for voltage measurement
NI USB-9211 **National Instruments**	4-Channel Thermocouple Input module	Use with NI CDAQ-9171 for temperature measurement
NI CDAQ-9171 **National Instruments**	1-slot NI CompactDAQ USB chasis	Used with NI USB-9211
PGSTAT302N with FRA2 module **Metrohm Autolab B.V.**	Potentiostat/Galvanostat	Data analysis
FEI Quanta 400F FESEM **FEI**	Scanning electron microscopy (SEM)	SC post-mortem analyser
EDX with 20mm^2 X-Max Detector **Oxford-Instruments**	Energy Dispersive X-ray Spectroscopy (EDX)	SC post-mortem analyser

Table 3-8: List of Instruments

Software	Description	Experimental Use
MATLAB /SIMULINK(R2010a) MathWorks	A program for numerical computing and simulation	Assisted in the simulation and development of SC model (in the time domain)
Lt SPICE	Software implementing a spice simulator of electronic circuit	Equalization circuit simulation
P-SPICE (student version)	Is a software tool used in electronic design automation	Equalization circuit simulation
NOVA 1.10.3 Metrohm Autolab B.V.	Software to control Autolab instruments	Used in SC characterization and data analysis
NI LabVIEW 8.6 National Instruments	Software development environment for creating a custom application to interact with data acquisition device.	Used for Data acquisitions during test periods
Arduino 1.0.5 IDE Arduino Software	Arduino development environment for writing code and communicating with Arduino board	Used to relay commands and directions to the Arduino board in form of codes

Table 3-9: List of software

Equipment	Description	Experimental Use
Arduino Motor Shield (L298P) **SKU: DRI0009**	Moto driver shield based on L298P driver chip	Used in addition to a booster circuit to charge 2 SCs and discharge to a 5V DC motor load
Iteaduino Leonardo **Iteadstudio.com**	Microcontroller board based on ATmega32u4	Used in powering the 2 Arduino shield individually
MotoMama **Iteadstudio.com**	Arduino shield based on L298N H-bridge driver chip	Used in addition to a booster circuit to charge 2 SCs and discharge by reverse polarity
Voltage equalization circuit 1	Customized design of circuit on experimental specifications	Initial prototype used to balance the voltage of each SC during cycling
Voltage equalization circuit 2	Customized design of circuit on experimental specifications	Used to balance the voltage of each SC during cycling
Charging circuit	Customized design of circuit on experimental specifications	Charging a module using different profiles
Variable Load circuit	Customized design of circuit on experimental specifications	Discharging a module using different profiles
Battery charging/rejuvenation circuit	Customized design of circuit on experimental specifications	For rejuvenation

Table 3-10: List of hardware: power electronics

3.3.1 Material: Supercapacitor (SC)

SC is the main focus of investigation in this project and its model, size and type were chosen based on the requirements needed to satisfy and support a small lab-scale test bench. This test bench was used to conduct the experiment in a laboratory with limited supplies.

The tests carried out in the duration of this project were done to satisfy the SC applications in EVs and HEVs. In EVs (known widely for its high peak power), SCs specifications were chosen to complement the battery, in other words, the SCs were sized up with the same current and voltage values to match up the battery power. However in this project, SCs with low capacitance and current specifications (in a lab-scale test bench) were investigated under the same environmental conditions that occur during SC applications in EVs. This SC selective process, however, did not diminish or degrade the experimental procedures since analysis on SC degradation evolution, especially in the automotive sector, is highly in demand.

Considering that SCs used in automotive applications are typically based on the organic electrolyte, the SC chose also possessed the same electrolyte material as that typically used in automotive applications. The SCs chosen were from HC series (BCAP0025) Maxwell Technologies, USA. The SCs use organic electrolyte tetraethylammonium tetrafluoroborate ($TEABF_4$) in acetonitrile (AN) and electrodes made of activated carbon with aluminium casing.

A physical description and detailed specifications of the SCs are tabulated below with reference from the **(HC series)** datasheet (Technologies).

Maxwell SC (BCAP0025) Specifications		
Electrical	Initial Maximum Capacitance	25F
	Initial Maximum ESR	42mΩ
	Absolute Maximum Voltage	2.85V
	Rated Voltage (65°/85°)	2.7V/2.3V
	Maximum continuous current (ΔT = 15°/45°)	2.8A/4.5A
Temperature	Operating Temperature	-40°C to +65°/+85°C
	Storage Temperature	-40°C to +70°C
Power & Energy	Specific Power (65°/85°)	2,800/2,000 W/Kg
	Specific Energy (65°/85°)	3.4/2.4 Wh/Kg
Life	Room Temperature (rated voltage & 25°)	10yrs
	High Temperature (rated voltage & Max. temp.)	1,000hrs
	Cycle life (room temp.); test current	500,000 cycle
	Storage life (max. storage temp.)	2yrs
Physical	Mass	32 grams
Safety	Short circuit current (65°/85°)	64A/55A

Table 3-11: Maxwell SC Specifications

3.3.2 Laboratory Equipment

Laboratory equipment (Figure 3-6) used during the experiment were situated in the Shaz-Nano laboratory located at the University of Nottingham Malaysia Campus.

Ransco environmental chamber in conjunction with an RNS compressor was the main equipment used in this project. SC test samples on a tray were placed in an inbuilt metallic basket found in the environmental chamber which helps in transferring the samples between the cold and hot zones of the chamber using a transfer mechanism. This transfer mechanism in question was operated pneumatically by supplying pressurized air from the compressor to the mechanism.

However in this project, experiments were carried out only in the hot zone of the chamber for long hours at a time. Therefore a water cooling system combined with the compressor (which is also used to convey pneumatically the basket) was used to minimise the heat dissipated from the chamber.

(a): Environmental Chamber

(b): Inbuilt Basket & SC sample tray

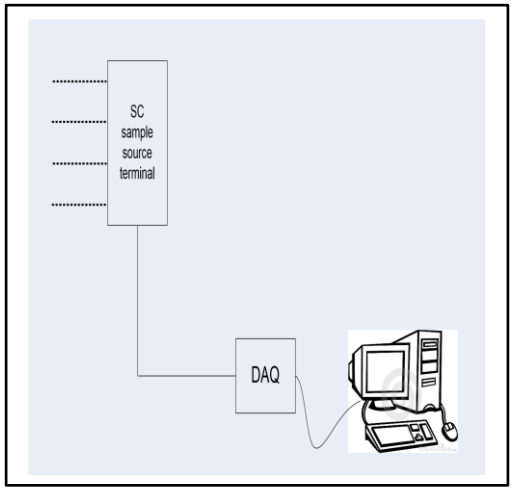
(c): RNS Compressor

Figure 3-6: (a): Ransco environmental chamber; (b): SC sample tray placed inside the chamber; (c): RNS cooling compressor

3.3.3 Instrument: DAQ system

The acquisition of data for this project during experimental procedures was gathered from a set-up comprising of a device called the NI USB-6212 and a computer. NI USB-6212 gotten from National Instruments was connected to a computer to record voltage profile of each one of the SCs terminals and also the SCs as a module during cycling. This was a system used not only to record but also to monitor the smooth operation of the experimental set-ups in terms of the expected values relating to the actual values (voltage) realised from this data. The NI USB-6212 is a USB powered

multifunction DAQ module with 16-analog input and 2-analog output optimized for superior accuracy at fast sampling rates for measurement solutions (in this case voltage measurement). The operation of the DAQ device is controlled by programmable software, LABVIEW. A photograph of NI USB-6212 and the setup of the DAQ system is illustrated in Figure 3-7**.**



(a): USB-6212 **(b): DAQ set-Up**

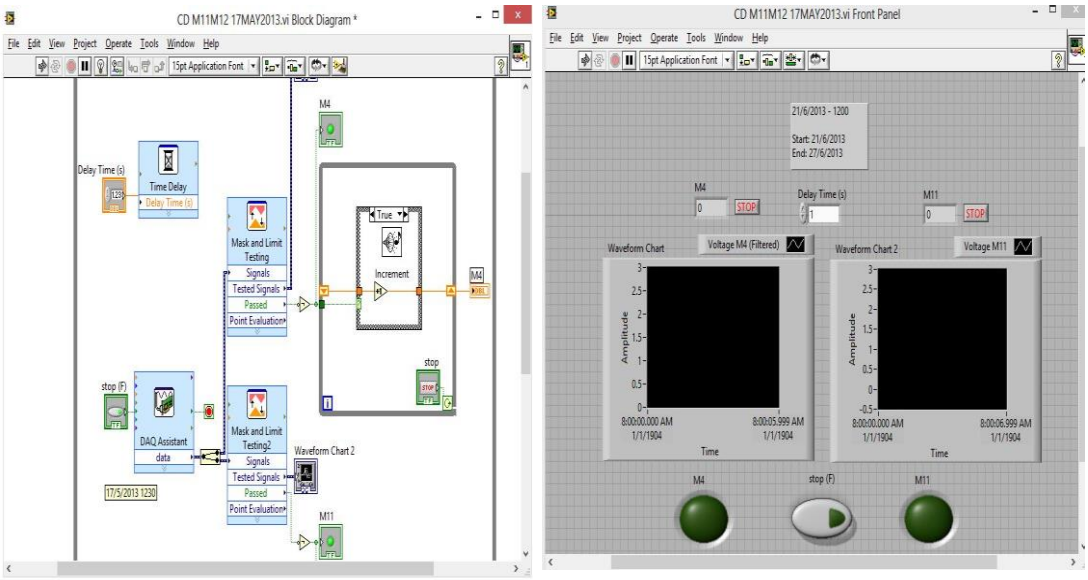
Figure 3-7: (a): DAQ and; (b): Set-Up with a PC

3.3.3.1 Software: LABVIEW

LabVIEW is a system-design software platform and development environment for a visual programming language from National Instruments. It employs a graphical programming platform to visualize the measurements and also analyse the data acquired. LabVIEW programs are called virtual instruments made of two windows, the front panel window, and the block diagram window. The block diagram is used to program and control the signals received from NI USB-6212 while the front panel

window is the user interface for the VI using the control palette and the indicators to define the inputs and display the output respectively.

The LabVIEW was used in this project to display the voltage profile using an oscilloscope and also to record the number of cycles the SC test samples obtained for the duration of the cycling tests using a clock counter. Figure 3-8 below is a screen shot of the program designed in LabVIEW illustrating the voltage profile (using the oscilloscope) and the cycle counter.



(a): block diagram window **(b): front panel window**

Figure 3-8: LABVIEW (a): block diagram window; (b): front panel window

3.3.4 Hardware: Voltage Equalization Circuit

There has been a few research in the area of voltage equalization, and different approaches have been investigated to help in choosing a suitable circuit. Voltage equalization circuits differ from application to application. Even in similar applications, equalization circuits design can be made flexible (regarding cost, weight, and efficiency) to satisfy user demand.

The working principle behind most voltage equalization circuits is simply to redistribute and balance the cells voltage. However, researchers have come up with additional measures by introducing sub-circuits with indicators to prevent over-voltage.

In this project, the coupling of voltage equalization circuits to SC samples was crucial to satisfying the premise of this research work. Therefore, a few circuit schematics collected from patents and journal papers that satisfied this project (set-up) power specification were investigated to understand their working principles.

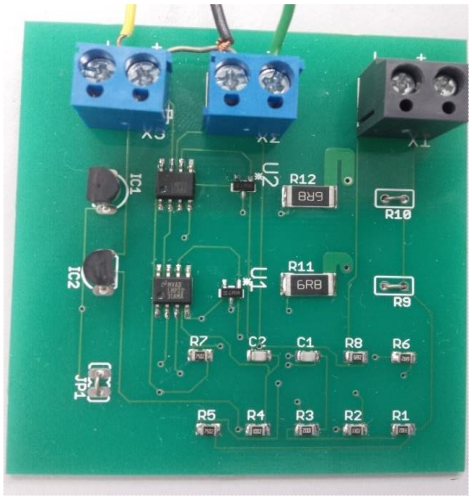
Simulations by software that implements a SPICE simulator of electronic circuits were carried out on a few selected circuits (Cheimonidis, 2009) (CAP-XX, 2008) (Guy C.Thrap, Del Mar, CA(US), 2004) (Johnson, 2009) to test, analyse working specifications and compare to see which best fits this project set up. Details of schematic circuits, design, and implementation, testing and results are explained in chapter 4.

However simulation results were not sufficient enough to tell if a circuit was working properly or not, so measures were taken to build hardware of the circuit design and

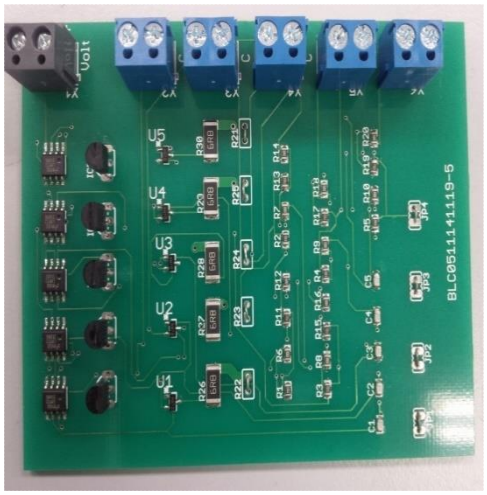
after a few adjustments and alterations a ‘voltage equalization circuit 1’ shown in figure 3-9, was proposed.

Three replicas of the hardware circuit were designed, two replicas were used in set-up 2 of the experiments and one in the set-up 3 of the experiment. Component description and selection process were critical to the design process and implementation of the proposed ‘equalization circuit 1,' therefore, discussions to that effect in Chapter 4 should be in order.

A commercial equalization from Maxwell called ‘voltage equalization circuit 2’ (shown in the figure 3-9) for experimental purposes was also employed in this project to compare and contrast experimental results. Circuit specifications, description and comparison of results with proposed ‘voltage equalization circuit 1’ were thoroughly investigated and discussed in chapter 4.



(a): Voltage equalization circuit 1



(b): Voltage equalization circuit 1

(c): Voltage equalization circuit 2

Figure 3-9: (a) & (b): Voltage equalization circuit 1 (for 2 & 5 SCs); (c): Voltage equalization circuit 2

3.3.5 Hardware: Charge/Discharge Circuits

Three circuits were employed in this project to satisfy the charge/discharge cycling phase of this project. The circuits differ in terms of design and energy power specifications to concur with the investigated questions this research deals on.

1. Charge/discharge circuit 1

Charge/discharge circuit 1 is made up of a motor driver (Arduino shield) called Motomama (Motomama, 2011) mounted on an Iteaduino Leonardo microcontroller board (based on ATmega32U4) (Leonardo, 2012) and extended to include a voltage divider circuit for the leonardo.

The motor driver (Motomama) is a dual full-bridge L298N used to control current flow in both directions (that is forward and reversed). It has two output channels which can connect two SCs at the same time, with a $2A$ current supply per channel. The Leonardo microcontroller board (based on Arduino ATmega32U4) analogue inputs can be used to measure DC voltage between $0V$ and $5V$ only, so in order to increase the voltage range over which the Arduino can measure, a voltage divider circuit was connected to the analogue input of the Arduino to decrease the measuring voltage so that it can fall within the range of the Arduino analogue inputs of $0V$ – $5V$. The actual voltage measured from the SCs is calculated by the code in the Arduino sketch.

The charge/discharge circuit 1 works as a switch, to charge the SCs when on and discharge (by reversing the polarity of the DC current when the voltage of the SC reaches a precise limit) when off. Two SCs (connected in series either with or without any form of balancing circuit) were connected to the output channels of the Moto-mama so that the analogue input pins can read the measured voltage of the SCs. The Arduino sketch was programmed to charge the SCs till it reaches the maximum voltage of $5.4V$ and discharge to $0V$ by current reversion.

The circuit schematics design with their connection and mode of operation is described and illustrated in Chapter 4. The coding program is written in Arduino IDE sketch (loaded to the Iteaduino Leonardo), and test profiles are also discussed in Chapter 4.

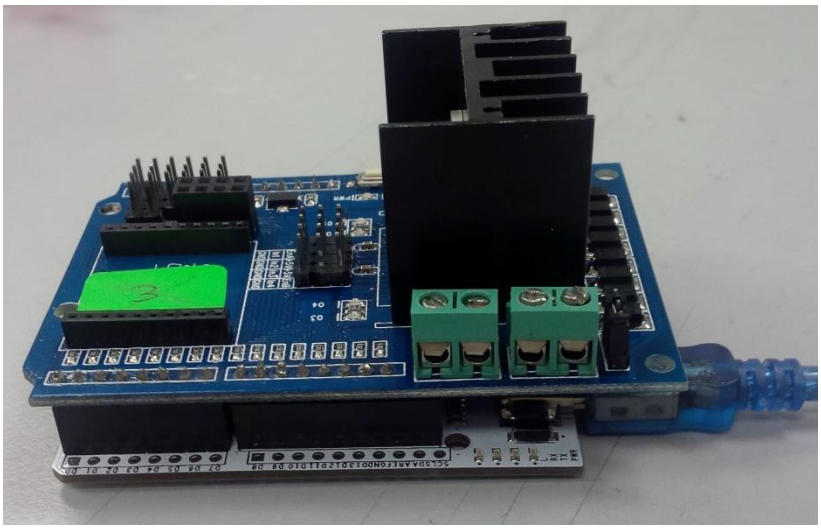


Figure 3-10: Charge/Discharge circuit 1

2. Charge/discharge circuit 2

Charge/discharge circuit 2 is made up of a L298P DC motor shield (Dfrobot, 2011) mounted on an Iteaduino Leonardo microcontroller board (based on ATmega32U4) and extended to include a voltage divider circuit for the Leonardo and a 5V DC motor. The difference between charge/discharge circuit 1 and charge/discharge circuit 2 regarding building components is the incidence of a 5V DC motor and the substitution of the motor driver. The Motomama shield was replaced with a L298P DC motor shield in the charge/discharge circuit 2 because two output channels were needed, one for the SCs and the other for the DC motor load.

L298P Motor Shield is controlled either by a PWM speed control mode or a PLL phase-locked loop mode with two output channels, and the power supply can be achieved either via Arduino VIN input or PWRIN with an external supply voltage between 4.8 – 35V and a driven current less than equal to 2A.

In charge/discharge circuit 2, the L298P motor shield uses the output channels to control phase signals through the PLL (phase-locked loop) mode. One of the two output channels is connected to two SCs (connected in series with two forms of balancing circuit) while the other output channel is connected to a $5V$ DC motor. The circuit operates, by reading the signals generated from the output channels; it is set in such a way that it charges up the SCs from $0V$ to $5.4V$ (by setting the signals from the SCs output channel to high), meanwhile keeping the DC motor disabled (by setting the signals from the motor output channel to low). At the point the SCs reaches $5.4V$ (which is the maximum rated voltage of the 2 SCs), it is programmed to discharge the SCs to $0V$ by powering the $5V$ DC motor (that is setting the motor output channel to high).

Leonardo microcontroller board and the voltage divider circuit used in this circuit is similar to the board used in charge/discharge circuit 2.

This circuit schematics design with their connection and mode of operation is also described and illustrated in Chapter 4. The coding program is written in Arduino IDE sketch (loaded to the Iteaduino Leonardo) and test profiles are also discussed in chapter 4.

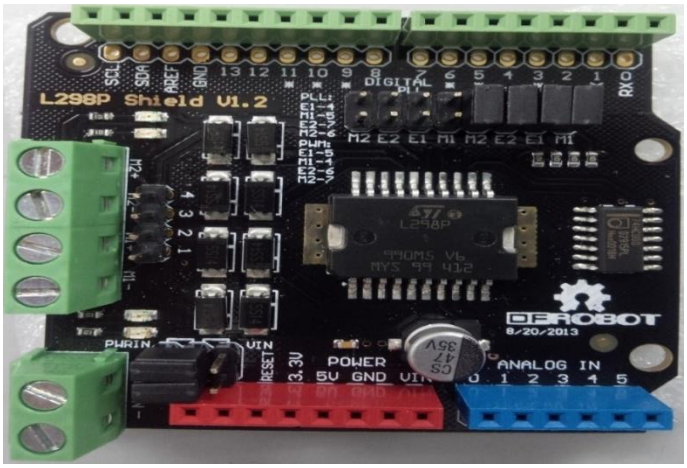


Figure 3-11: Charge/Discharge circuit 2

3.3.6 PGSTAT302N and AUTOLAB Software NOVA 1.10.3

A Potentiostat/Galvanostat (PGSTAT302N) is used to carry out electrochemical testing on SCs. PGSTAT302N is a high-performance modular Potentiostat/Galvanostat from Metrohm Autolab B.V. It consists of a data-acquisition system for data sampling and recording, and an FRA2 module for electrochemical impedance spectroscopy. The functions of PGSTAT302N are controlled by a control software NOVA 1.10.3 (Figure 3-12), also developed by Metrohm Autolab B.V. PGSTAT302N provides four electrode connections: uses two for current measurement; counter electrode (CE) and working electrode (WE) and the other two for voltage measurement; reference electrode (RE) and sense electrode (S). The 2-electrode connection is used in this project as shown in figure 3-13. This connection measures the potential across the whole electrochemical cell, including contributions from working electrode and electrolyte. The impedance measurement, therefore, is given by;

$$Z_{cell} = \frac{V_{WE} - V_{CE}}{I} \tag{3.2}$$

Electrochemical characterization and DC measurement of SCs were carried out using PGSTAT320N and controlled by Autolab NOVA 1.10.3. The software supports a series of measurement techniques including Electrochemical Impedance Spectroscopy, Cyclic Voltammetry and Constant Current charge-discharge test which was the main measurement method used for SC quantification.

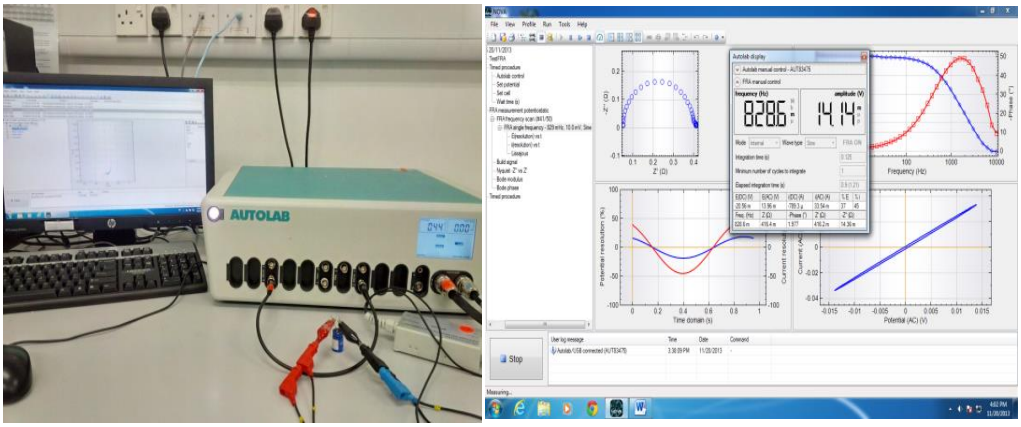


Figure 3-12: (a): PGSTAT302N and Nova 1.10.3 loaded on the PC. (b): The measurement view on Nova

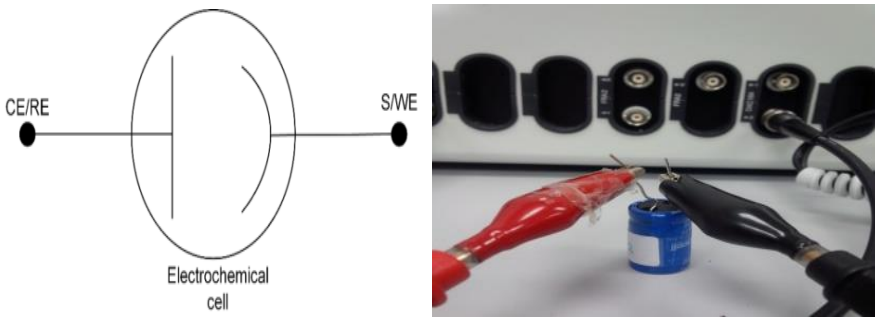


Figure 3-13: 2-electrode connection (theoretical and experimental)

3.4 Experiment: Electrochemical Characteristics and measurement techniques

When dealing with electrochemical properties, it is crucial to study different measurement techniques under various testing conditions to analyse and quantify SC characterization from inception all through failure evolution, as it affects SC leakage current on failure degradation characteristics (Burke, 2000). SCs with very low leakage current have long life as a low leakage current indicates the absence of low-level Faradaic reactions between the electrode material and the electrolyte; however, it is not the case when those same SCs are subjected to a stressful environment over long periods of time, as the leakage current increases thereby resulting in SC degradation, meaning a reduction in capacitance and an increase in resistance.

Electrochemical processes often overlap due to the contribution of different changes in an electrochemical cell. Therefore, it is often complex if they were to be analysed with standard methods. Therefore, a method that can, as precisely as possible, distinguish between the influence of different processes is needed. With that in mind, data collection in this project follows a measurement protocol comprising of electrochemical characterizations and DC measurement techniques. The measurement protocol was carried out to track changes in SC performance during the ageing test. The data collection was done in a systematic manner: Electrochemical Impedance Spectroscopy was done first, followed by Cyclic Voltammetry and constant current test.

3.5 Summary

This chapter provides a constructive methodology of understanding SC performance deterioration during long-term operations. Following the research objectives, a block diagram summarising the research methodology was drawn (see Figure 3-2). The block diagram shows the process of SC 'cell' and 'module' failure from accessing: The why? The how? And The what? Makes SC fail. To do that, experimental tests were drawn up to show why they fail, then failure mechanisms are derived from the results using measuring tools of quantification to understand how. It is not enough to know the causes and mechanisms of SC failure without knowing the symptoms categorized with each ageing factor. "What" type of failure, in form of failure modes (increase in ESR and decrease in capacitance) and SC EEC models were consequently necessary.

To convey the methodological process, it was important to establish the requirement that makes for a good SC from available testing standards, procedures and literatures. Then, test boundaries were drawn to include only environmental-caused and operational-caused failures. A chuck of this chapter centres on describing the experimental tests, the experimental tools and circuitry used in developing the accelerated tests used in this research work.

SC ageing is understood to be caused by many factors (governed by the predominant factors; temperature and voltage) and analysing the failure mechanisms can be daunting. Therefore, a brief overview of the different methods of quantifying these ageing mechanisms, which validates one another was introduced in this chapter. The collected data were useful for the development of an ageing model for the state of health monitoring.

CHAPTER 4- RESEARCH HARDWARE SIMULATION, DESIGN, AND TESTING

4 Overview

A bulk of this project was dedicated to the experimental test phase. Therefore, it 3demanded the employment of the necessary hardware electronics required to carry out these test.

This chapter will focus on the design and testing process carried out on the hardware, the electronic hardware supported with software (written codes) being characterized based on the working principle assigned to each experimental set-up discussed in the methodology chapter (section 3.3).

The electronics employed in this project Include:

1. Equalization circuits
2. Charge/discharge circuits 1 and 2
3. Charging circuit and variable load discharging circuit

4.1 Equalization Circuit

An equalization circuit is an integral part of the electronics employed in this project work and, as such, a brief review of this subject matter was carried out in chapter 2. As explained in Chapter 2 Voltage Imbalance of SC cells in a module is an important subject for the whole system life, hence the need for a balancing system to ensure a healthy and working operating system.

Supercapacitor and battery balancing topologies are categorized into passive and active balancing systems, and the difference between the two categories is that; the passive balancing methods removes excess charge from fully charged cell(s) through passive components until the charge matches those of the lower cells in the module or charge reference. The passive element could either be in a fixed mode (Diab et al., 2006) or a switched mode depending on the system (Cadar, Petreus, & Patarau, 2010; Stuart & Zhu, 2009). The active cell balancing method, on the other hand, removes charge from higher energy cell(s) and delivers it to lower energy cell(s). This method has different topologies on some active elements used for storing energy as presented in Cao, Schofield, & Emadi, 2008; Daowd, Omar, van den Bossche, & van Mierlo, 2011; Kong, Zhu, Lu, & Cheng, 2006.

Even with this basic distinction between the topologies, different methods based on these topologies have been proposed by various researchers (e.g. (Diab et al., 2006)) concerning their working principles and applications.

Equalization circuits reviewed and discussed in this project work were categorized under the active method**.** The basic function and general principle of a balancing/equalization circuit are simple and similar regardless of the approached

method of design. However, different designs proposed were based on application implantation, balancing speed, complexity, cost, size and efficiency. In this regard, three proposed balancing/equalization methods from CAP-XX, (2008); Guy C.Thrap, Del Mar, CA(US), (2004); Johnson, (2009); Pierre Mars, VP Applications Engineering, (2009) with different viewpoints were vetted and chosen accordingly to suit the design in order to perform the experiments needed in this project work.

Vetting process of the three circuits:

1. Understanding the working principles by highlighting its specifications and comparing them with this application project specification.
2. Carrying out software simulations using spice simulators to compare circuit power performance drawn from circuit components.
3. Modifying components to fit project specification and eventually building an equalization circuit.

4.1.1 Circuit Schematics, Simulations, and Hardware Design

The vetted circuits were subjected to further tests to ensure the circuits' power compatibility to the cycling properties employed in this research work for test ageing in SC modules. Simulations on the circuit schematics were first carried out to determine power compatibility, however when the simulations yields incomplete results, real life testing are carried out with the said designed hardware to confirm

results. The circuit that yields the most suitable results is then chosen to undergo experiments.

4.1.1.1 Circuit 1

The leakage current of each SC cell differ slightly from one other, so when more than one cell is combined in a series module without a balancing circuit, it becomes a disaster in the sense that the same current is meant to flow through the whole module. This is difficult to achieve without an equalization circuit to redistribute the charge between the cells, thereby adjusting their voltages to equate their leakage current (leakage current; meaning the minimum current needed to charge a SC from 0V).

With that in mind, circuit 1 (a low current active balancing circuit) from CAP-XX, 2008; Pierre Mars, VP Applications Engineering, 2009 was chosen. The circuit shows how a low current active balancing circuit was more suited for their application with energy harvester sources (such as solar cells and micro-generators) because of their nature to deliver only a few micro amps to SCs with a leakage current of about $1\mu A$.

This balancing/equalization circuit (Pierre Mars, VP Applications Engineering, 2009) is a low current active balancing circuit consisting of two resistors that serve as a voltage divider and an ultra-low current rail-rail op amp. It attracts very little current with the chosen op amp MAX4470 drawing approximately$750nA$, while drawing $250nA$ through the voltage divider. The whole circuit in theory draws a maximum of $2-3\mu A$, including supercapacitor leakage current, once the supercapacitor has reached equilibrium leakage current.

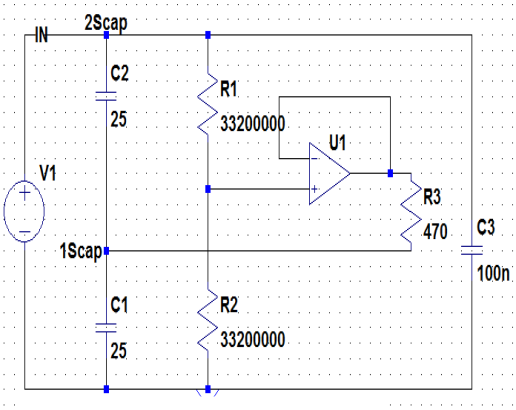
The schematic diagram shown in Figure 4.1a is a micro- power active balancing circuit with a single operational amplifier. Resistor R3 ($470\ Ohm$) protects the circuit by limiting the output current in case one of the SC cells short-circuit. During simulations, MAX4470 operational amplifier was replaced with LM385, a spice model operational amplifier believed to have similar low current properties as MAX4470. However, to simulate the circuit by way of attaining a desirable SC charge/discharge outcome, a voltage source V1 (of $5.4V$ value) was employed with an additional $80m\Omega$ resistor to act as a load to the SCs. Figure 4-1 is a collation of the simulation results of circuit 1 inclusive of the schematic circuit diagram, C1 and C2 voltage and current simulated graph, and also simulated current passing through the Op amp.

Components	Expected Values (During SC charging phase)		Simulation Values (During SC charging phase)	
	Voltage (V)	**Current (A)**	**Voltage (V)**	**Current (A)**
SC1	2.7	67.5m	0 – 2.7	70m - 0
SC2	2.7	67.5m	0 – 2.7	70m - 0
Op amp U+	-	+750n	+2.7	+68µ
Op amp U-	-	-750n	-2.7	-68µ

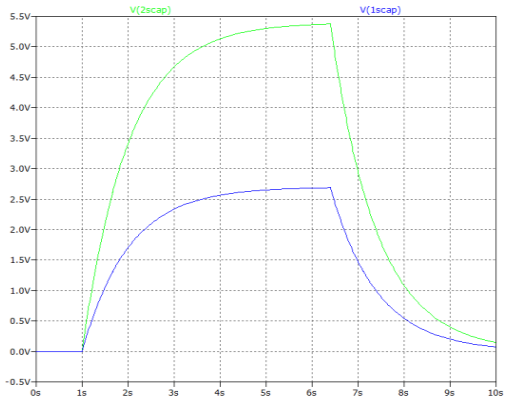
Table 4-1: Expected and simulation values for circuit 1

Figure 4-1b shows the voltage simulation of SC1 and SC2, with SC1 voltage simulating from $0V$ to $2.7V$ imitating a charging capacitor which then immediately discharges to $0V$ over a run time of $10sec$ (as pre-selected in the spice simulator). On the other

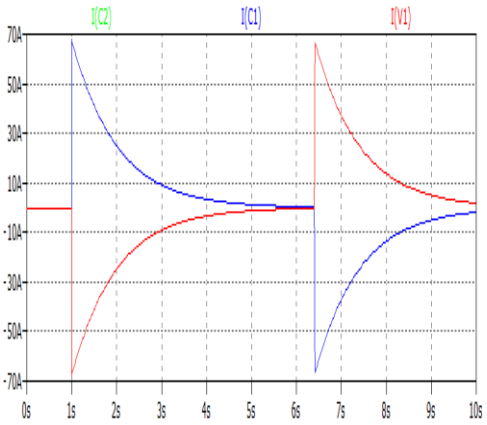
hand, SC2 (plotted at the positive terminal) charges to $5.4V$ before discharging, plotting the combined voltage of both C1 and C2 because of their series arrangement. Figure 4-1c records a current graph on SC1 and SC2 with a spike of current at the beginning (at 1s) then gradually increasing to $70mA$, and coinciding with SC1 and SC2 charging phase; The graph also records a negative spike at the point where SC1 and SC2 (6.4s) commence their descent to $0V$, while the reverse is the case for the current graph recorded at the source (V1). The high current value ($70mA$) recorded is as a result of the resistor load value selected 80Ω; i.e. $I = V/R = 67.5mA$ (theoretically). The simulated current on the op amp terminals in figure 4-1d also differ from the expected values with about 67µA because LM385 current ranges between 10µ -20mA (INSTRUMENTS, 2013a) which is better than MAX4470 of 740nA (Integrated, 2011).



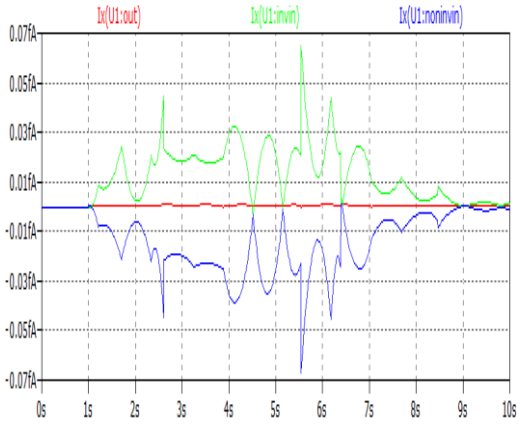
(a): Schematic Circuit 1



(b): Voltage simulated graph: C1 and C2



(c): Current simulated graph: V1, SC1 and SC2



(d): Current simulated graph Op amp terminals: U+, U-, Uout

Figure 4-1: Schematic and Simulation results of circuit 1

4.1.1.2 Circuit 2

Figure 4-2a based on Guy C.Thrap, Del Mar, CA(US), 2004 is a charge balancing circuit, i.e. a voltage balancing circuit in addition to being also a charging circuit, that contains a LM324 operational amplifier, a current limiting resistor R4, a voltage divider in between resistor R1 and R1 and a negative feedback resistor R2. The voltage divider here helps divide the supply voltage into half so that half the supply voltage flows into the non-inverting input of the operational amplifier. This will make sure that the

voltage flowing into the SC Scap1 and Scap2 is equal to prevent the super capacitors from overcharging. The output current of the operational amplifier is controlled by a current limiting resistor R4 to prevent the operational amplifier from overheating. In addition to that, limiting resistor R4 also functions as a monitoring and diagnostic tool on SC State of health in a module during the operation mode, by comparing the voltage drop across each resistor R4 with the average voltage drop across limiting resistor so as not to exceed it. The midpoint source voltage in between SC Scap1 and Scap2 is monitored by the negative feedback resistor R3. The voltage at the midpoint is used to check if the energy stored in the SCs is balanced or not. When there is voltage imbalance in the SCs, the operational amplifier will either sink or upsurge which causes energy to transfer from higher charge SC (usually the SC closest to the + terminal of the power source) to lower charge SC. To minimize the current drawn, resistor value for R1 and R2 must be large, to ensure that the current drawn by these resistors is smaller than the leakage current. Furthermore, to divide the supply voltage into half, both resistor R1 and R2 have to be of the same value. To cancel input of the bias current that flow into the operational amplifier, the value of negative feedback resistor R3 has to be about half of either resistor R1 or R2. When one of the SCs (i.e. Scap1 or Scap2) is short, the current limiting resistor R4 can protect the operational amplifier from getting damaged (Guy C.Thrap, Del Mar, CA(US), 2004).

Unlike the operational amplifier used in circuit 1 (section 4.1.1.1), LM324 (a 5pin Op amp) provides a higher rated current of about 0.3mA (Instruments, 2015). Simulations of circuit 2, using P-spice simulator, was carried out by supplying a 5.4V source and connecting a 20Ω resistor load R5 to the circuit to simulate a surge charge form of the two 25F SCs; Scap1 and Scap2 as shown in figure 4-2a. Figure 4-2 is a

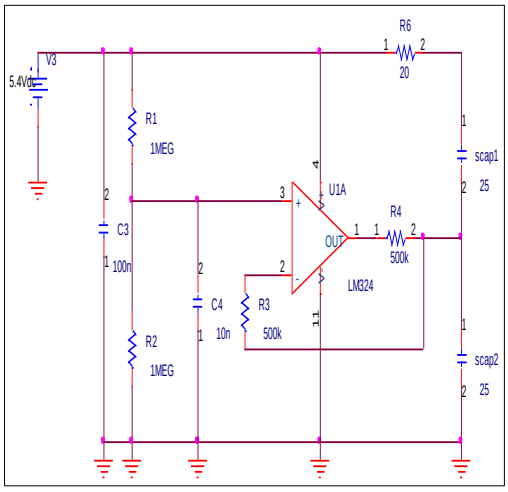
collation of the simulation results of circuit 2 inclusive of the schematic circuit diagram and hardware circuit design, Scap1 and Scap2 voltage simulated graph, plus the simulated voltage across the Op amp.

Components	Expected Values (During SC charging phase)		Simulation Values (During SC charging phase)	
	Voltage (V)	**Current (A)**	**Voltage (V)**	**Current (A)**
Scap1	2.7	-	0 – 2.7	-
Scap2	2.7	-	0 – 2.7	-
Op amp U+	2.7	+750n	2.7	-
Op amp U-	2.7	-750n	0 - 2.7	-
Op amp Uout	5 – 5.4	0.3m	4.5	-

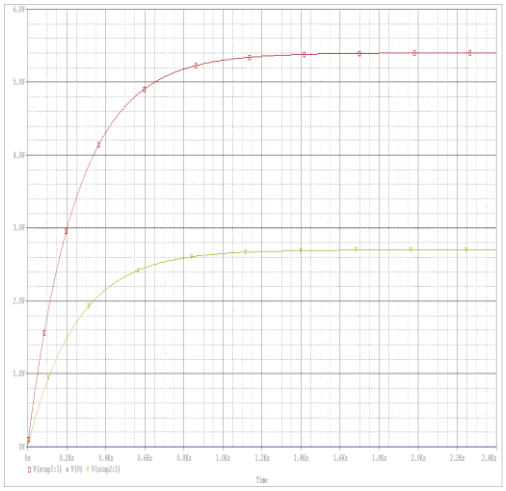
Table 4-2: Expected and simulation values for circuit 2

Figure 4-2b shows the voltage surge of Scap1 and Scap2 as it charges from $0V$ to $5.4V$ and $2.7V$ respectively over $2.4ks$ (as pre-selected from the simulator). The voltage across Scap1 is recorded as $2.7V$, but it simulates $5.4V$ because the graph plots the voltage at the positive termina,l thus recording the voltage across both SCs as a result of their serial connection. Figure 4-2c simulates voltages at the input and output of the Op amp LM324 terminals; the moment simulation starts running, the Op LM324 switches ON (and pull up the output voltage between the ranges of 5V-5.4V in reference to INSTRUMENTS, 2015) reading a voltage of $4.5V$ because of the current

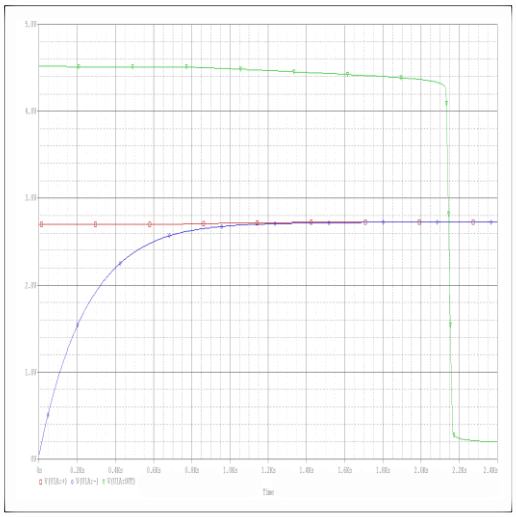
drawn by R4, the limiting resistor. The op amp output remains ON, while the positive input U+ is set still at $2.7V$ and the negative input U- exponentially travel from $0V$ to $2.7V$ (because of the feedback from Scap2), whilst the SCs charge up to the rated voltage value before they switch OFF, returning the output voltage Uout immediately to $0V$ (at $2.2ks$).



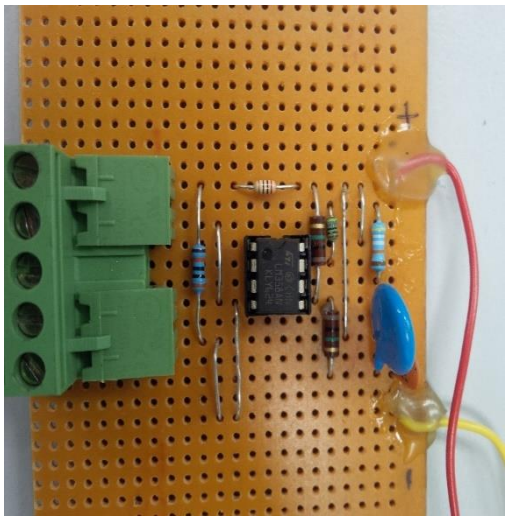
(a): Schematic



(b): Voltage simulated graph:



(c): Voltage simulated graph Op amp



(d): Hardware: Circuit 2 without the 2 SCs

Figure 4-2: Schematic, Hardware and Simulation results of circuit 2

From the simulation results in Figure 4-2, circuit 2 appears more encouraging than circuit 1, especially because the Op amp has a higher rated current of $0.3m$ and has the ability to limit current flow to the SCs after reaching its limit by using the limiting resistor R4. With improvement noticed in circuit 2, it seemed right to proceed with the hardware assemble as shown in figure 4-3. When testing the circuit, Two SCs were charged up with the circuit by first charging the SC closer to the positive terminal and transferring charge from the first SC to the second SC till the voltage was balanced. After charging, it was observed that the two SCs were perfectly balanced at the voltage limit with no flow of current, but the time it took for both SC cells to be fully charged was quite long, with a time record of under 5mins. This delay brought up some concerns on the current needed to fast charge the SCs. The commercial SC employed in this project had individual leakage current of $0.045mA$ (Technologies) and since more than one SC was being used, $0.3mA$ current of the Op amp was barely enough to charge up 2 SCs because of their accumulated leakage current, hence the delay.

4.1.1.3 Circuit 3

Circuit 3 inspired by Johnson, 2009 overcomes the overcharge problem by balancing the string with a voltage limiting circuit across each SC cell. From the schematic Figure 4-3a, two 25F SCs, 1Scap, and 2Scap are connected in series with each having its individual balancing circuit, to form an energy bank with a total of 5.4V with SC rating at 2.7V when fully charged. Each circuit consists of a low voltage operational amplifier LMP2231 (INSTRUMENTS, 2013b) with five pins, the positive and negative input terminals maintaining equal voltage levels at $1.2V$. The positive terminal is held at

$1.2V$ with the help of a voltage divider using two resistors $75K$ and $61.9K$, while the negative input to the amplifier is maintained at $1.2V$ with a voltage reference LT1004 (INSTRUMENTS, 1999). With the same amount of voltage entering the positive and negative input of the amplifier, it would give a zero output. When both SCs charge reaches 2.7V, a Mosfet transistor PMV30UN (Semiconductors, 2003) turns on, to drain the output voltage of the amplifier. The output voltage for the operational amplifier can be calculated using the formula of integrating amplifier in Equation (4.1).

$$V_o = -\frac{V_{IN}}{CR_1}[t]_0^t + V_o \qquad (4.3)$$

Where, V_o at right hand side is 0.

The circuit only works if the positive input voltage at the operational amplifier is bigger than $1.2V$. (David Johnson, 2015)

Simple calculations can be performed based on the schematic in Figure 4-3a:

$$2.65V / (75 + 61.9) = 0.01972$$

$$0.01972 \; x \; 61.9 = 1.22V$$

Theoretically from the calculation above, when the SCs voltage reaches $2.7V$, the positive input of the op amp would obtain a voltage bigger than $1.2V$, which makes the comparator output to turn ON, thereby activating the Mosfet which then drains the excess voltage. But when the voltage at the positive input is lower than the negative input, meaning the SCs are still charging and their voltages are less than $2.7V$, then the comparator turns OFF as there is no need for any voltage comparison.

The 6.8Ω resistor limits the current being drained by the Mosfet, and the Mosfet stops draining when the comparator is turn OFF.

From the original schematic diagram (Johnson, 2009), LM385 (INSTRUMENTS, 2013a) was replaced by LT1004, which is a micro-power voltage reference that has two-terminal band-gap reference diode. This type of designation has high accuracy and proper temperature specifications at low operating current. Besides, it is a pin-for-pin replacement of LM385 (LTD).

Simulations of circuit 3 using Lt-spice simulator were carried out by supplying a 5.4V source and replacing diode IN5819 in Figure 4-3a with a 80mΩ resistor load to simulate a surge charge form of the two 25F SCs; C2 and C4 as shown in figure 4-3a. Figure 4-3 is a collation of the simulation results of circuit 3 inclusive of the schematic circuit diagram (which is made up of two "circuit 3" for each SC), 1Scap and 2Scap current/voltage simulated graph, and simulated current/voltage on the Op amp.

Figure 4-3b is a summary of the prerequisites needed to simulate circuit 3 properties, and Figure 4-3c shows the voltage simulation of SC2 and SC4. SC2 voltage simulates from $0V$ to $2.7V$ imitating a charging capacitor which then immediately discharges to $0V$ over a run time of $10sec$ (as pre-selected in the spice simulator). SC4 (plotted at 2Scap), on the other hand, charges to $5.4V$ before discharging and plots the voltage combination of both C2 and C4 because of their series connection.

Components	Expected Values (During SC charging phase)		Simulation Values (During SC charging phase)	
	Voltage (V)	**Current (A)**	**Voltage (V)**	**Current (A)**
SC2	2.7	-	0 – 2.7	-70m-0
SC4	2.7	-	0 – 2.7	-70m-0
Op amp U1+	1.22	-	1.2	6p
Op amp U1-	1.2	-	1.2	12p
Op amp U1out	0	-	0	24n
Op amp U2+	3.92	-	3.85	24p
Op amp U2-	3.9	-	3.9	30p
Op amp U2out	2.7	-	2.69	24n

Table 4-3: Expected and simulation values for circuit 3

Figure 4-3d records a current graph on SC1 and SC2 with a reverse spike of current at the beginning (at $1sec$), which then gradually increases to $0A$ while SC2 and SC4 charges, whilst a positive spike at the point SC2 and SC4 ($6.4secs$) commence their descent to $0V$. The high current value ($70mA$) recorded is as a result of the resistor load value selected 80Ω; i.e. $I = V/R = 67.5mA$ (theoretically). Figure 4-3e simulates voltages at the input and output on both Op amp LMP2231 terminals; the moment simulation starts running, U1out switches ON and spikes to $0.6V$ within $0.5secs$ and then returns to 0V, while the negative input U1- quickly rises to $1.2V$,

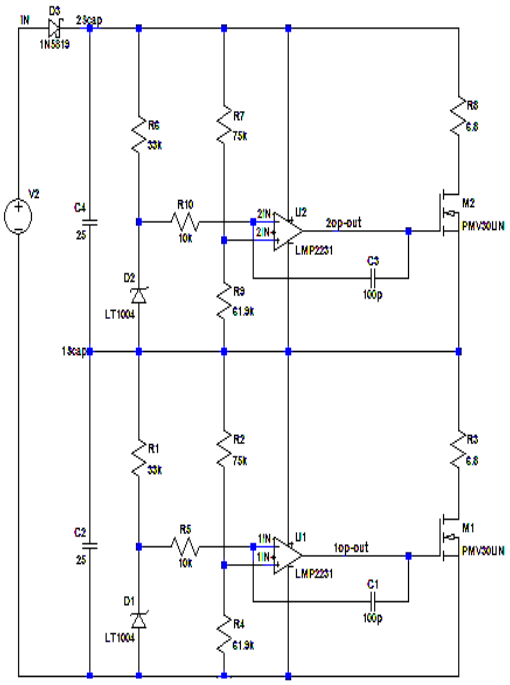
also within $0.5s$ecs, and maintains that voltage till SC2 sets to discharge then it drops to $0V$, the positive U1+ exponentially travelling from $0V$ to $1.2V$ (because of the voltage source from 1Scap) within SC2 charging limit ($6.4s$ecs), and then this also drops to $0V$. Op amp U2 also displays similar properties as U1, except the fact that all its simulations are increased by the presence of SC2 making all wave forms to rise $2.7V$ above ground level and simulating with SC charge/discharge properties. The simulated current on the op amp U1 and U2 terminals are presented in Figure 4-3f & Figure 4-3g.

Given how similar the simulation results on the voltage profiles are to its expected values in circuit 3, hardware design was proposed with reservations to the current simulations in Figure 4-3 which provided a faster charging time than circuit 2.

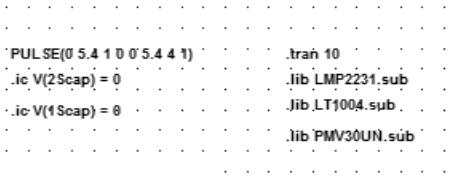
In summary, simulation results on all three circuits were incomprehensive to make a valid decision, therefore real-life cycling test were conducted with circuit 2 and circuit 3. The experimental tests proved circuit 3 to be more amiable with the researches experimental properties (providing a faster charging time) than circuit 2. Circuit 1 did not proceed beyond the simulation stage because the LM385 Op amp used which provided inconclusive results during simulations was replaced with the original MAX4470 Op amp of the circuit as it was difficult to get the model. Since both Op amps appeared capricious it was best suited not to develop the circuit's hardware.

Circuit 3 hardware referred to as ‘voltage equalization circuit 1’ (in chapter 3) was designed on two separate boards; comprising two balancing circuits on one board and five balancing circuits on the other board as shown in Figure 3-10a&b. After a few tests, ‘voltage equalization circuit 1’ (circuit 3) was best suited to satisfy the power demands needed for the experimental set-up.

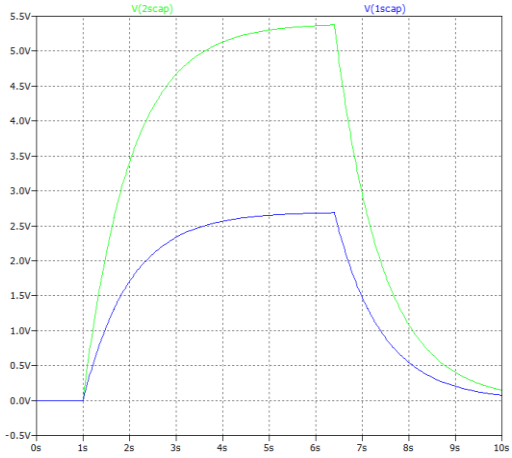
In addition to ‘voltage equalization circuit 1’, a commercial equalization from Maxwell referred to as ‘voltage equalization circuit 2’ (shown in the figure 3-10) was also employed in this research work to compare and contrast experimental results.



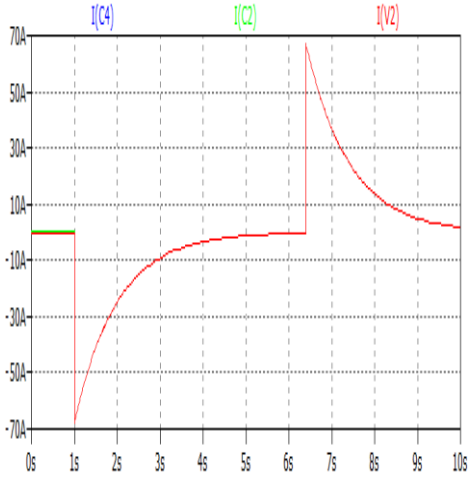
(a): Schematic



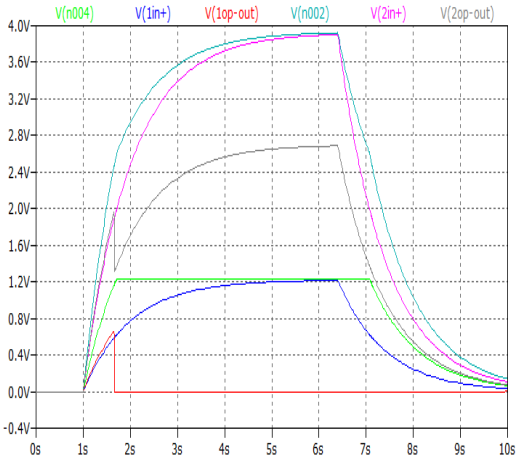
(b): Transient



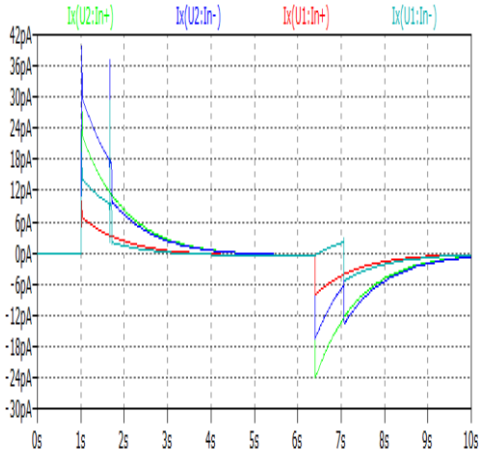
(c): Voltage Simulated graph: 1Scap & 2Scap



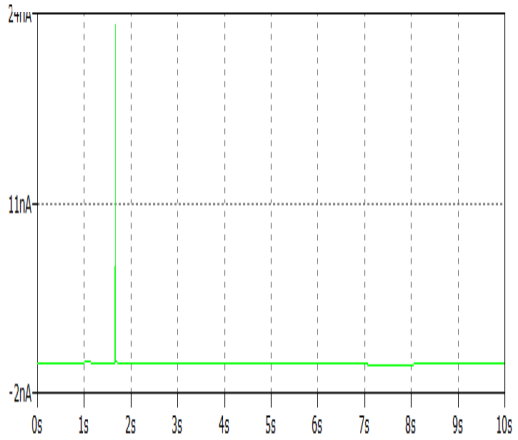
(d): Current Simulated graph: 1Scap &



(e): Voltage Simulated graph: U1+,U1-,U1out,U2+,U2-,U2out



(f): Current Simulated graph: U1+,U1-

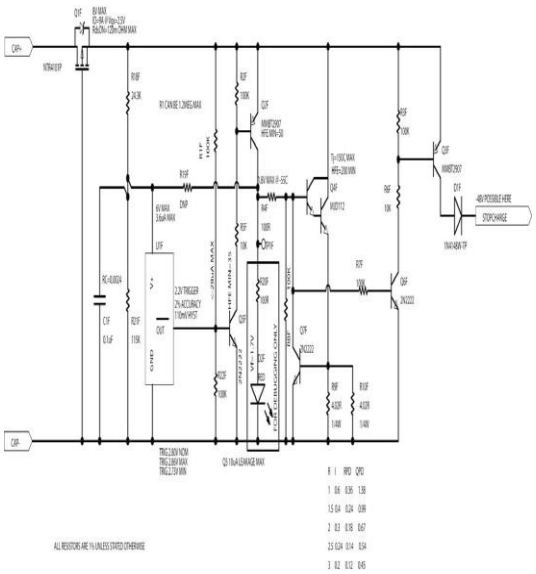


(g): Current Simulated graph: U1out, U2out

Figure 4-3: Schematic and Simulation results of circuit 3

4.1.2 Maxwell Active Voltage cell Management electronics

The active voltage management developed by Maxwell active balancing electronics (patents pending) is a sinking topology capable of sinking current at $300 - 400\ mA$ from each individual cell whenever a specific cell voltage is in the range above or equal to $2.73\ volts$. The on-off trigger of the voltage management circuits has been optimized for performance in consideration of temperature and other influences. Each cell voltage is individually monitored with an integrated analog – OR circuit against a nominal reference voltage. Every monitoring output has an integrated analog – OR circuit. The circuit is designed to "trigger" at $2.73\ volts$ and upon trigger, will function to reduce the voltage on the cell rapidly to below the threshold of $2.70V$, at which point the circuit goes into a quiescent state. Maintaining the cell voltage below this "trigger" level will assure a longer lifetime of the cells and, therefore, a longer lifetime of modules as well (Technologies, 2007).



Q1:	Reverse polarity protection.
R18, R21:	Voltage divider to set the voltage management circuit discharge level.
C1:	Low pass filter with R18 to prevent oscillations and give transient suppression.
U1:	Integrated reference, comparator. Open drain output. Device pulls low until voltage threshold reached, typically 2.2V for this device. Used in conjunction with the voltage divider, sets the voltage management circuit discharge level to 2.8V. Has 100mV of hysteresis built in.
R19:	Place holder for a resistor to add additional hysteresis.
R1:	Pull up to turn on Q5 when U1 shuts off.
Q5:	First gain stage. Needed to insure operation throughout Q4's gain range.
R5:	Current limiting resistor to pull down Q2's base.
R2:	Used to prevent the base of Q2 to self-bias.
Q2:	Second gain stage.
R4:	Current limiting resistor to the base of Q4.
R8:	Used to prevent the base of Q4 to self-bias.
Q4:	Primary transistor used to dissipate the energy in the cells. Operated in constant-current mode to dissipate the most power in Q4 and not in R9/R10.
R9, R10:	Part of the current feedback circuit. Adjusted so that 0.6V across them gives the circuit the desired current. Two in parallel for better power dissipation.
Q7:	Limits the voltage on the base of Q4 to set it to constant current mode.
R7:	Current limiting resistor for the base of Q6.
Q6:	Used as an inverter to turn on Q3.
R6:	Current limiting resistor for the base of Q3.
R3:	Used to prevent the base of Q3 to self-bias.
Q3:	Sources current when the voltage management circuit is active.
D1:	All voltage management circuits are wire-ored. D1 prevents another voltage management circuit from biasing Q3.
R20, D2:	Used for debugging. LED turns on when voltage management circuit is active.

Figure 4-4: Maxwell Active Voltage Management Circuit and Functional Description

For the purpose of this research work, Maxwell Active Voltage management circuit is referred to as ‘voltage equalization circuit 2’ and used to compare operation performance and reliability with ‘voltage equalization circuit 1’.

As explained in experimental set-up part A (section 3.3.2I), the effect of a cell voltage balancing circuit was put to the test by comparing SC performance with and without a balancing circuit to protect the cell from over-charging. The tests carried out were in the form of continuous charge/discharge profiles tabulated in section 4.4. The voltage profiles collected were in response to the test samples in Table 3-5.

SC performance on voltage imbalance and ageing behavior can only be evaluated over a period, which means continuous operation (in this case cycling). Therefore, it is nearly impossible to categorize SC performance between these three modules; (2 SCs without a balancing circuit W5&W6, 2 SCs with ‘equalization circuit 1’ B9&B10, 2SCs with ‘equalization circuit 2’ C7&C8) based on a single voltage profile as shown in Table 4-5. However, performance regarding charge-time, discharge time, the voltage drop can be evaluated, as this information provides insight to the balancing circuits working standard (that is if in fact the voltages between the cells were balanced).

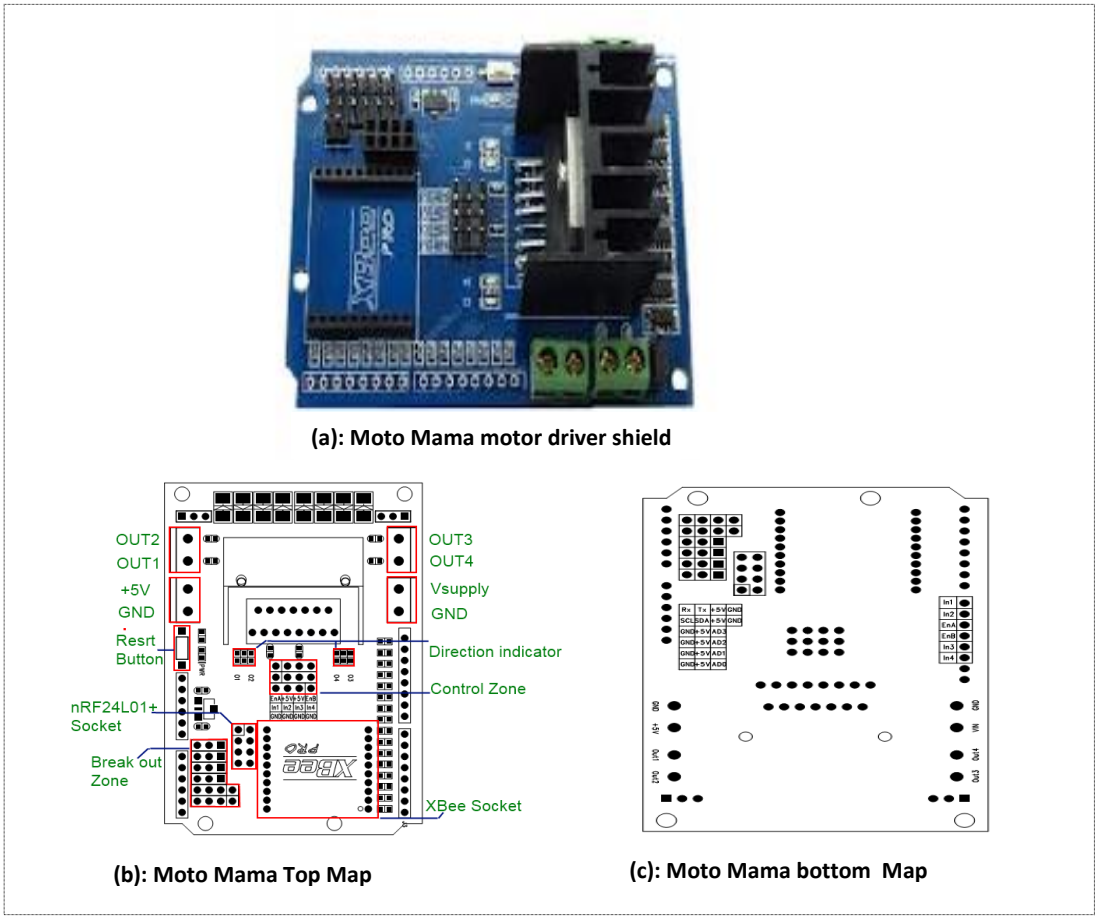
4.2 Charge/Discharge circuits 1 & 2

Charge/discharge circuits 1 & 2 were used in carrying out charge/discharge cycling tests shown in section 3.3.2. The main components used were: 1) Motor driver shield 1 & 2. 2) Arduino microcontroller board. 3) A voltage divider. 4) a 5V DC motor load, in the case of the latter (i.e. the charge/discharge 2). This section explains the hardware/software, connections, and limitations as related to this study.

4.2.1 Hardware Components

1. **Moto Mama**

   MotoMama is an H-Bridge motor driver shield based on ST L298N chip. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC motor and stepping motors. MotoMama is aimed to be easy with other sensors or wireless modules (Motomama, 2011).



(a): Moto Mama motor driver shield

(b): Moto Mama Top Map

(c): Moto Mama bottom Map

Figure 4-5: Moto Mama motor driver shield

Moto Mama can drive two DC motors at the same time using outputs OUT1/OUT2 and OUT3/OUT 4 on the board. However, in this project, only OUT3/OUT4 was exercised, as the purpose was to cycle SC samples by charging and discharging (thereby reversing the current) in both directions with little or no stress excreted on the samples. The power of the system depends on the voltage and current supplied to the output VSupply. The outputs OUT1/OUT2 and OUT3/OUT4 are controlled by input port A and port B respectively. Port A and B has three pins each, In1, In2 and EnA and In3, In4 and EnB respectively. The In (Interrupt pins) are digital ports which are used

to control the direction of the SC samples while the En (Enable pins) are connected with PWM port of control board to control the SC speed samples.

2. L298P DC motor shield

DFRobot L298 DC motor driver shield uses a high-power H-bridge driver Chip L298P, which can drive DC motor, i.e. two-phase or four-phase stepper motor with a maximum 2A current(Driver, 2000). The motor output uses eight high-speed Schottky diodes for protection. The circuit wiring of the shield is well-organized, and the stack design makes it directly mountable onto an Arduino compatible with ATmega32u4or Mega.

The Shield can switch between PWM speed control mode and PLL phase-locked loop mode through setting the appropriate jumpers. The power supply can be achieved either via Arduino VIN input or PWRIN input on the shield through setting the appropriate jumpers. The speed control is achieved through conventional PWM, which can be obtained from Arduino's PWM output Pins 5 and 6. The enable/disable the function of the motor control is signaled by Arduino Digital Pins 4 and 7.

The Motor shield can be powered directly from Arduino or its external power source with the specifications presented in Table 4-6 (Dfrobot, 2011).

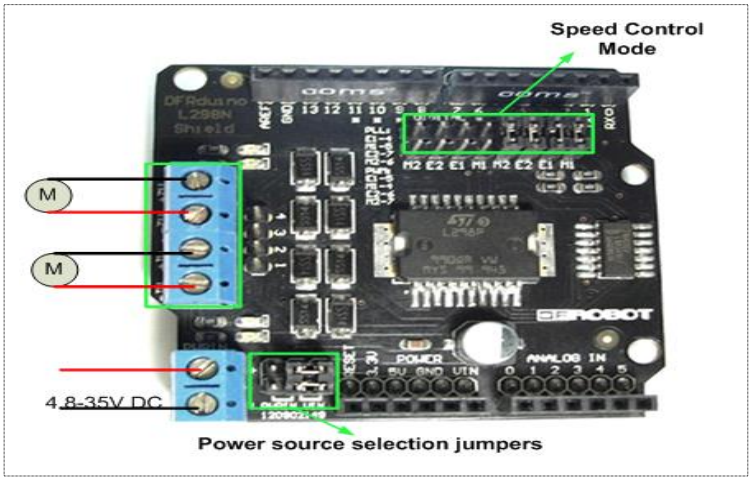


Figure 4-6: L298 Motor Shield marking control mode setting (Dfrobot, 2011)

Control Mode Selection Jumpers as demonstrated in Figure 4-6: The shield supports PWM and PLL (Phased Locked Loop) control Modes. The PWM mode uses E1 and E2 to generate PWM signal while the PLL mode uses M1 and M2 to generate phase control signal which was best suited for the experiments where the M1 output terminals connect to the SCs samples while M2 output terminals connect to a 5v DC motor.

As PLL (Phase Locked Loop) control mode was chosen as the mode of operation to drive both the SC samples and the 5V DC motor, it should be noted that direction was not a priority, therefore, pins allocated to the direction control (i.e. Digital 5 and 7) were not active during the testing process.

Power Supply shown in Figure 4-6: The motor shield can either be powered by either VIN (Arduino power) or PWRIN (external power) when the motor current exceeds the limits provided from the Arduino and, by choosing the latter (which was selected in this project), two jumpers were switched in favour of the PWRIN.

3. **Iteaduino Leonardo**

Iteaduino Leonardo is a microcontroller board based on ATmega32u4. It has 20 digital input/output pins (of which seven can be used as PWM outputs and 12 as analog inputs), a 16 MHz crystal oscillator, a micro USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller. It is powered by either connecting it to a computer with a USB cable, an AC-to-DC adapter or battery to get started. Iteaduino Leonardo differs from all preceding boards in that the ATmega32u4 was built-in USB communication, eliminating the need for a secondary processor. Which allows the Leonardo to appear to be connected to a computer as a mouse and keyboard, in addition to a virtual (CDC) serial / COM port (Leonardo, 2012).

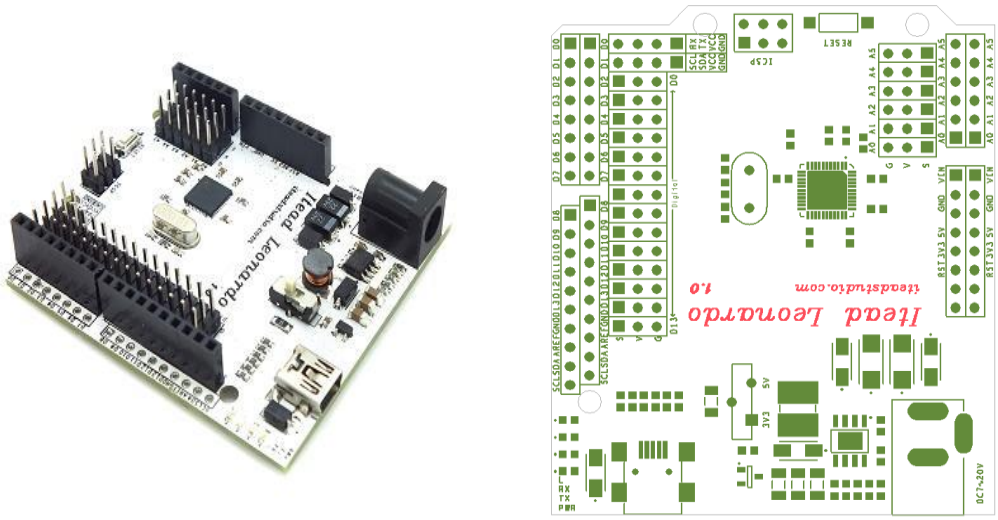


Figure 4-7: Iteaduino Leonardo with map layout

Power Options

5V regulated power supply was employed in this project by connecting a USB cable to the Itead-Leonardo through an AC-to-DC adapter. And from the map layout (Figure 4-7), the board has 20 digital i/o pins that are used either as input or output, using pinMode(), digitalWrite(), anddigitalRead() functions, and each pin can transmit or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of $20 - 50\ kOhms$.

4. Arduino Voltage divider

Under normal conditions Arduino has a $5V$ analog reference voltage, in other words, analog inputs can only measure DC voltage between $0V$ and $5V$. This normal condition becomes quite a conundrum when Arduino boards operate under higher voltage levels ($> 5V$). However, difficult as it may seem, measuring voltage range can be increased by using two resistors to create a

voltage divider. The voltage divider decreases the need for the voltage to be measured to fit within the range of the Arduino analog inputs. The actual voltage is later calculated and incorporated in the codes alongside the operating principle of the charge/discharge circuit written in the Arduino sketch.

The voltage divider allows voltages greater than 5V to be measured, just as recommended by the SC samples subjected to charge/discharge cycles (in section 3.3). Hence Figure 4-8, for a boost in power properties to satisfy the experimental tests.

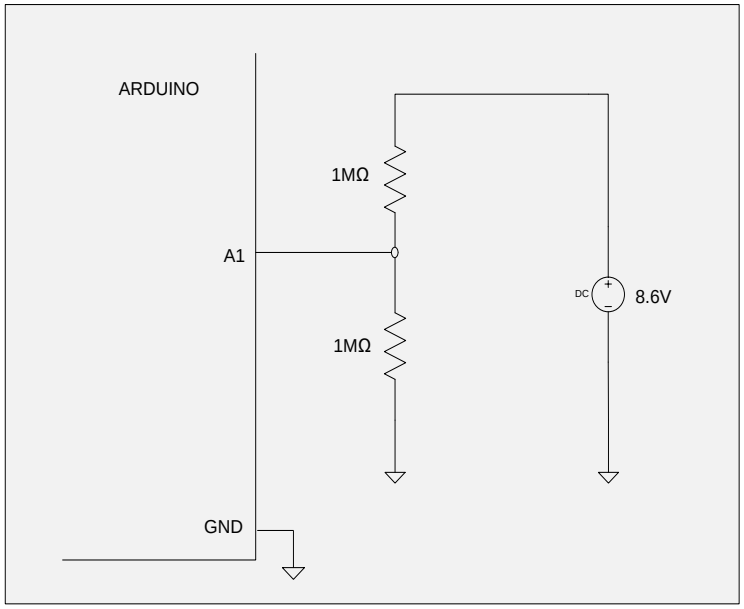


Figure 4-8: Arduino voltage booster

The voltage divider employed to boost the Arduino's voltage (Figure4-8) consists of two $1M\Omega$ resistors (it is generally advised to use high impedance for accurate results) in series with a DC power source (supplying a voltage of $8.6V$). The circuit divides the input voltage (i.e. the $8.6V$ from the power supply) by the output voltage at A1 (that is: $(1M\Omega \div (1M\Omega + 1M\Omega)) \times$

$8.6V = 4.3V)$ to produce a division factor of 2. Thus, when measuring the input voltage 8.6V, the Arduino analog pin will read a voltage of $4.3V$ which is less than the $5V$ reference (making the voltage acceptable to the Arduino). In this project though, the Analog pin A1 reads a maximum voltage of $5.4V/2V = 2.7V$ (which is also the rated voltage of the SC) to measure the voltage across the SC samples.

The resistor values used in the circuit provides over-voltage protection when measuring low voltages from $5V - 12V$. This measure is taken to avoid unfortunate incidents (such as blowing up Arduino), however, when faced with accidental higher voltage measurements, the protection will be of no use (Electronics, 2013).

4.2.2 Charge/Discharge Circuit 1 Design

A block diagram of charge/discharge circuit 1 (consisting of an Iteaduino Leonardo and MotoMama motor shield) showing the pin connections with an additional voltage divider, power supply, and SC samples, is presented below. Figure 4-9 is the hardware illustration of charge/discharge 1 in a power cycle mode with the SC samples.

The working principle of the circuit is simple. It acts as a switch by charging the positive terminal of the SC samples (connected to the output pin OUT3 and read to digital pin In3) with a positive (forward) current till the maximum voltage of the two SC samples 5.4V is reached. Then positive terminal is set to low while the negative

terminal of the SC samples (connected to the output OUT4 and read to digital pin IN4) is charged with the reversed current. This phenomenon is explained in the Arduino sketch with the code in Appendix A.

Arduino is a tool for making computers that can sense and control more of the physical world. It is an open-source physical computing platform based on a simple microcontroller board and a development environment for writing software for the board. Arduino can be used to develop interactive objects, taking inputs from a variety of switches or sensors, and controlling a variety of lights motors, and other physical outputs. Arduino projects can be stand-alone, or they can be communicating with software running on the computer. The Arduino programming language is an implementation of a similar physical computing platform based on the Processing multimedia programming environment (Mahender, 2013).

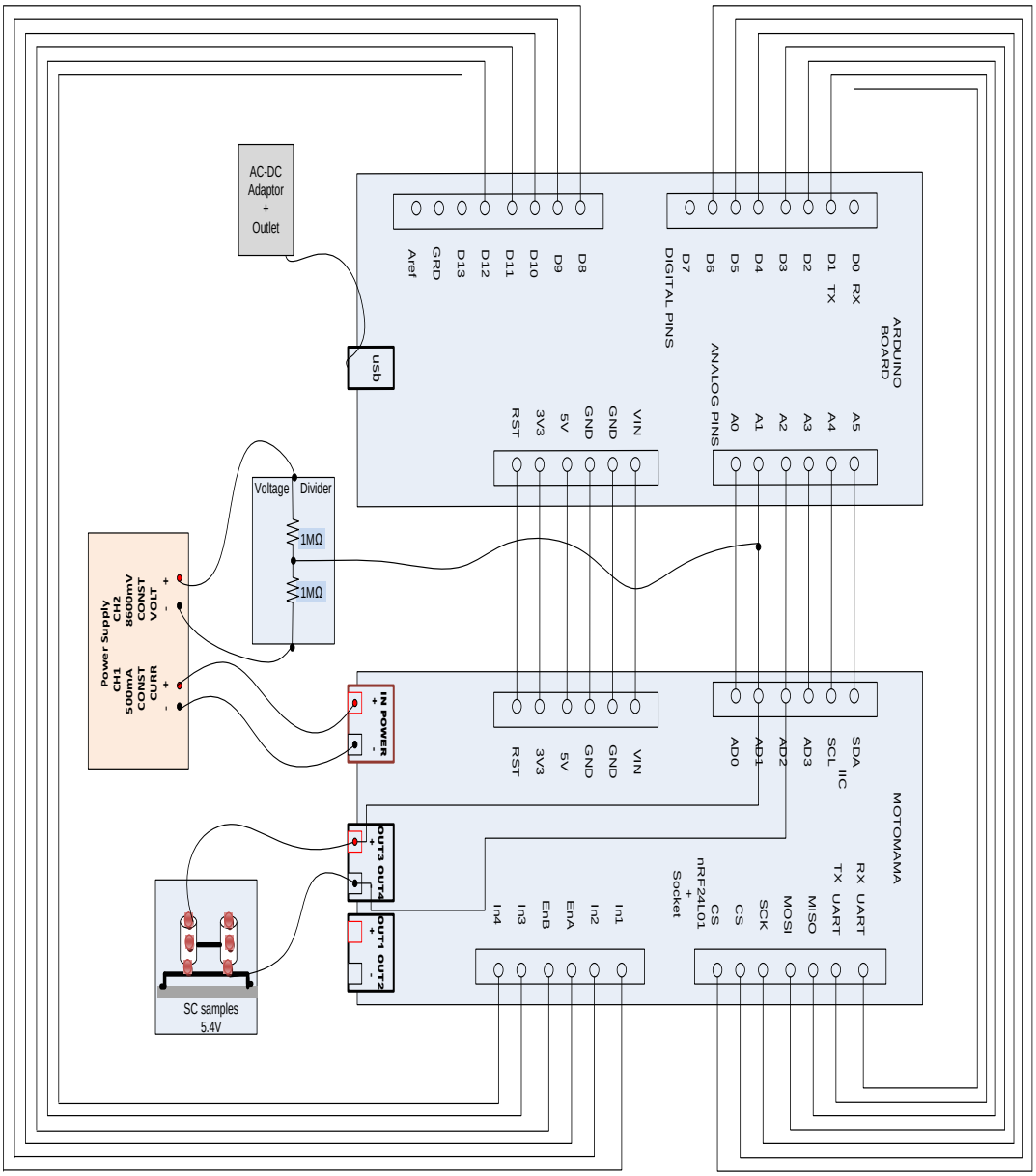


Figure 4-9: Charge/Discharge circuit 1 block diagram with hardware connections

The Arduino software includes a sketch pad in which codes are written and uploaded to the Arduino board via USB connection to the computer. The software also supports the transmission of textual data between the board and computer through the serial monitor function in the software. For visual effects, RX and TX LEDs on the board flashes when data is being transmitted via the USB connection to the computer (but not for serial communication on pins 0 and 1).

The sketch starts by defining SC terminal pins and assigning each a sensor pin, which sensors the actual voltage and measures it accordingly with the voltage divider. The codes go further to create a switch control that charges the SC samples when it senses the voltage to be lower than 5.4V and discharges the SC samples when the voltage is greater than $5.4V$, and this cycle continues with a counter to monitor the process. Appendix A contains the full codes.

4.2.3 Charge/Discharge Circuit 2 Design

A block diagram of charge/discharge circuit 2 (consisting of an Iteaduino Leonardo and L289P motor shield) demonstrating the pin connections with the additional voltage divider, 5V DC motor, power supply and SC samples, is shown in Figure 4-10. It is a hardware illustration of charge/discharge 2 in a power cycle mode with the SC samples.

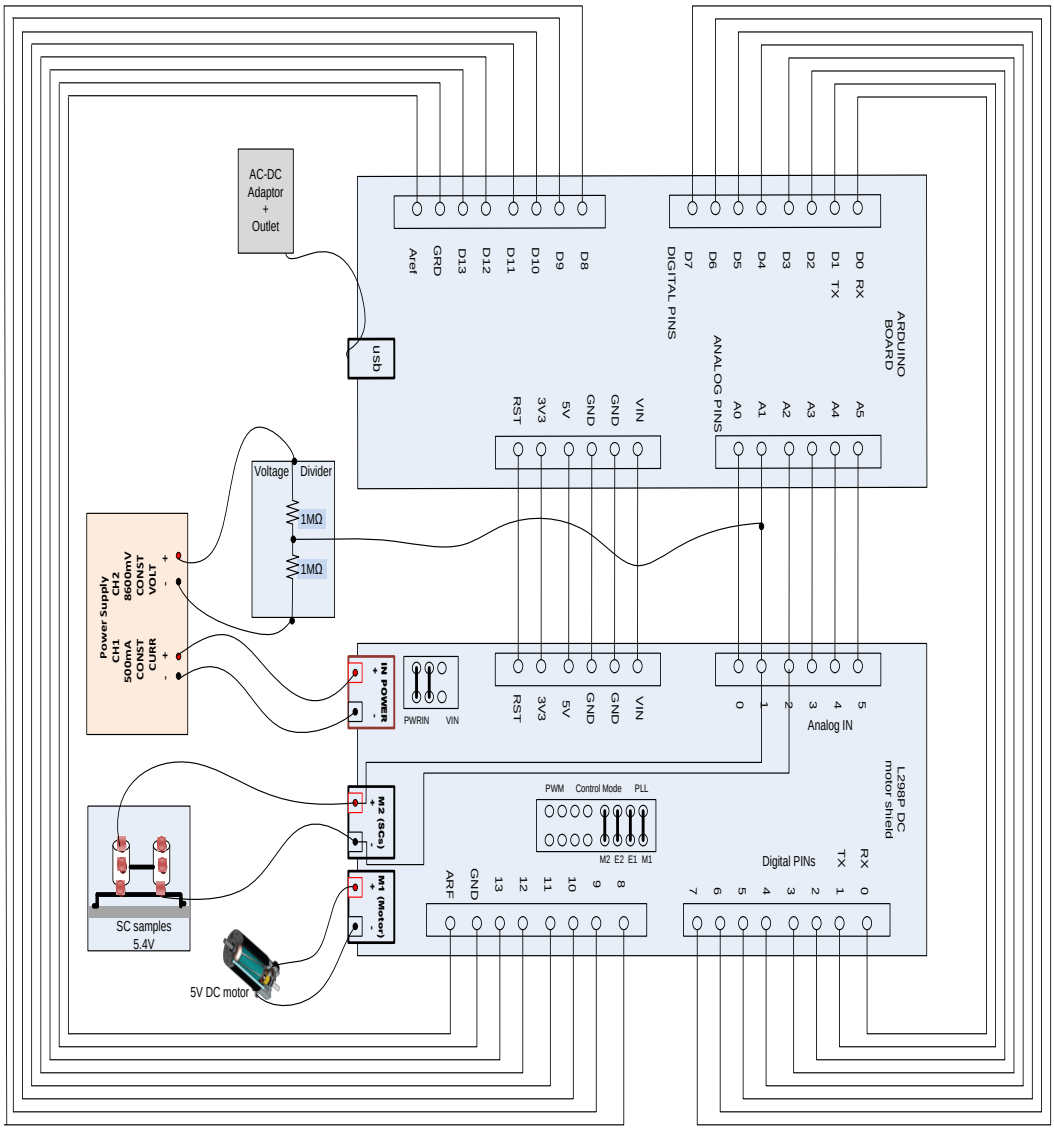


Figure 4-10: Charge/Discharge circuit 2 block diagram with hardware

The working principle of this circuit is similar to charge/discharge circuit with an additional 5V DC motor (connected to the M1 OUTPUT pins). The circuit charges up the SC samples (connected to the M2 OUTPUT) from 0V to 5.4V (by setting M2 output channel to high), meanwhile keeping the 5V DC motor disabled (by setting M1 output channel to low), then later discharging the samples to the 5V motor load (by setting the M1 OUTPUT channel to high).

Similar to charge/discharge circuit 1, Arduino sketch pad was also used to program the charge/discharge cycles between the SC samples and the 5V DC motor, as described with the full codes in Appendix B.

4.3 Charging circuit and Variable load Discharging circuit

Charging circuit and variable load discharge circuit were recommended to assist in testing the experimental set-up 3, described in (section 3.3). The Charging circuit was designed separately from the variable load discharge circuit, and the main components used were:

- Power Supply
- Microcontroller
- DC Load
- LCD keypad shield and LCD panel
- SC charger circuit
- Voltage booster circuit
- SC programmable discharge circuit
- Relay Switch circuit

4.3.1 Hardware Components

Microcontroller

Arduino Uno based on the AT Mega chip was the chosen microcontroller for the 'charging circuit and variable load discharging circuit', similar to the microcontroller used in 'charge/discharge circuit 1&2.' The microcontroller has six analog inputs, 14 digital I/O ports, six ports of which can be used as PWM outputs, and a 16 MHz core clock (Arduino). The Arduino can be powered using external power or a USB port from the computer. C/C++ language is the main programming language used. This microcontroller was selected for this project due to its compact size, ease of use, multiple analog input ports, multiple I/O ports and PWM ports which can be used to drive the IGBT or MOSFET. Due to the open source nature of this microcontroller board, it allows different disciplinary projects to be more accessible. This makes the Arduino the most appropriate selection for testing and prototyping of projects.

A total of three Arduino boards were used; the first board was used to program the charging circuit, the second board for the discharging circuit, and the third board to power the switch relay between the charging and discharging circuits.

DC Load

Load profiles were developed to emulate EV's operating cycle with a programmable load, using two identical motors that were clamped together along with a motor driver to form a programmable load as shown in Figure 4-11.

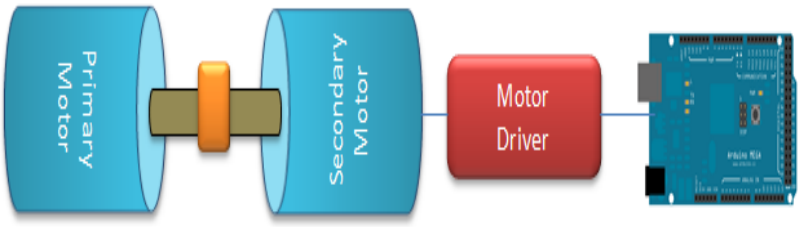


Figure 4-11: Programmable load block diagram (YIK, 2013)

The DC load comprised of a primary motor driven from the Software Control Board and a secondary generator driven by motor driver configured by Arduino UNO.

The primary and secondary motor parameters were inferred from datasheets downloaded online of similar motors since there was no datasheet available for the motor that was acquired for the experiment. A test process was carried out to determine the transient start-up current of the motor, which was up to $3.6A$. The motor exhibited a high start-up current of about 3 to 4 times its rated amount. This characteristic of the motor was used to simulate the peak current demands for the DC load. For steady-state conditions, at full load the motor would draw $1.1A$ whereas, at no load, it would draw $0.2A$. Based on these conditions, it was inferred that the motor's impedance at start-should be about 3.33Ω. Likewise, it was also inferred that at the steady state and rated conditions, the motor's impedance should be about 10.9Ω.

The motor driver powered by the supercapacitor module causes the secondary motor to rotate in the opposite direction of the primary motor according to the PWM output from the motor driver. Hence, the Secondary motor acts as a generator, and back e.m.f is fed into the motor driver. Moreover, by controlling the PWM output of the

motor driver with the variable discharge circuit, the current drawn by the primary motor can then be programmable (see chapter 6-13).

LCD keypad shield and LCD panel

LCD keypad shield is used with the Arduino Uno board as the Arduino does not contain any display panel or keypads to make it user-friendly and easier to key in commands. The term "shield" is used because the LCD keypad shield is mounted on top of the Arduino Uno board.

The LCD shield used for this project was a 16x2 HD44780 compatible LCD with white character and a blue backlight having adjustable contrast levels (Oxer, 2013). The six push buttons on the keypad which can be used for inputs could be programmed to be used in different applications.

Operating Voltage	5V
Display (Column x Row)	16x2
Character	White
Backlight	Blue
Inputs	Six momentary push buttons
Interfacing Pins from Arduino Uno	Digital pins 4, 5, 6, 7, 8, 9, 10
Reading Pins from Arduino Uno	Analog pin 0

Table 4-4: Summary specifications for Arduino Uno Keypad shield

The LCD keypad shield was mounted on the variable load discharging circuit with options on selecting discharge voltage range and load speed range. A separate LCD panel was also included in the whole system set-up to monitor SC module voltages as it charges and discharges, and also a counter to measure the number of cycles as the process continues.

4.3.2 Charging circuit with Voltage booster

A schematic of the charging circuit and booster circuit is presented in Figure 4-11. The charging circuit was aimed at charging a bank of SC samples of voltage rating 13.5V, and with a power supply of 12V, it was necessary to boost the voltage with a boost circuit of 12V to 15V. The booster circuit was then used to power the SC charger circuit by generating PWM signals (SV2) as shown in Figure 4-12.

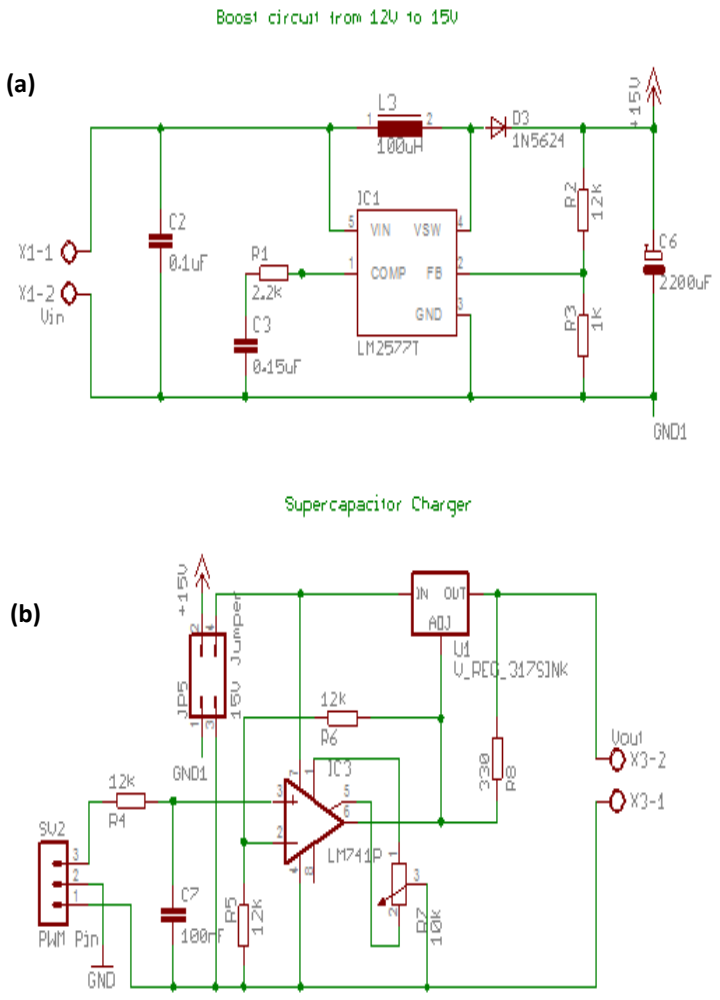


Figure 4-12: (a) Charging circuit with (b) booster circuit

An Arduino board was connected to charging circuit to generate PWM signals to charge an SC module. The Arduino was used to program the charging voltage (i.e. the voltage required to charge up a SC module, the value varies depending on the size of the bank) and set voltage limit (meaning the maximum voltage the SC module is allowed to charge up to). Although for easy access, an LCD with knobs was attached to the system to adjust manually the charging voltage from $(1V\ to\ 10V)$ and the voltage limit which ranges from $(1V - 12V)$. A well-detailed written sketch with pin definitions and descriptions is presented in Appendix C.

4.3.3 Discharging circuit with Relay switch

A schematic representation of the discharging circuit with a relay switch (used to switch the module operation from the charging circuit to the discharging circuit as soon as it reaches its programmed voltage limit) is shown in Figure 4-13.

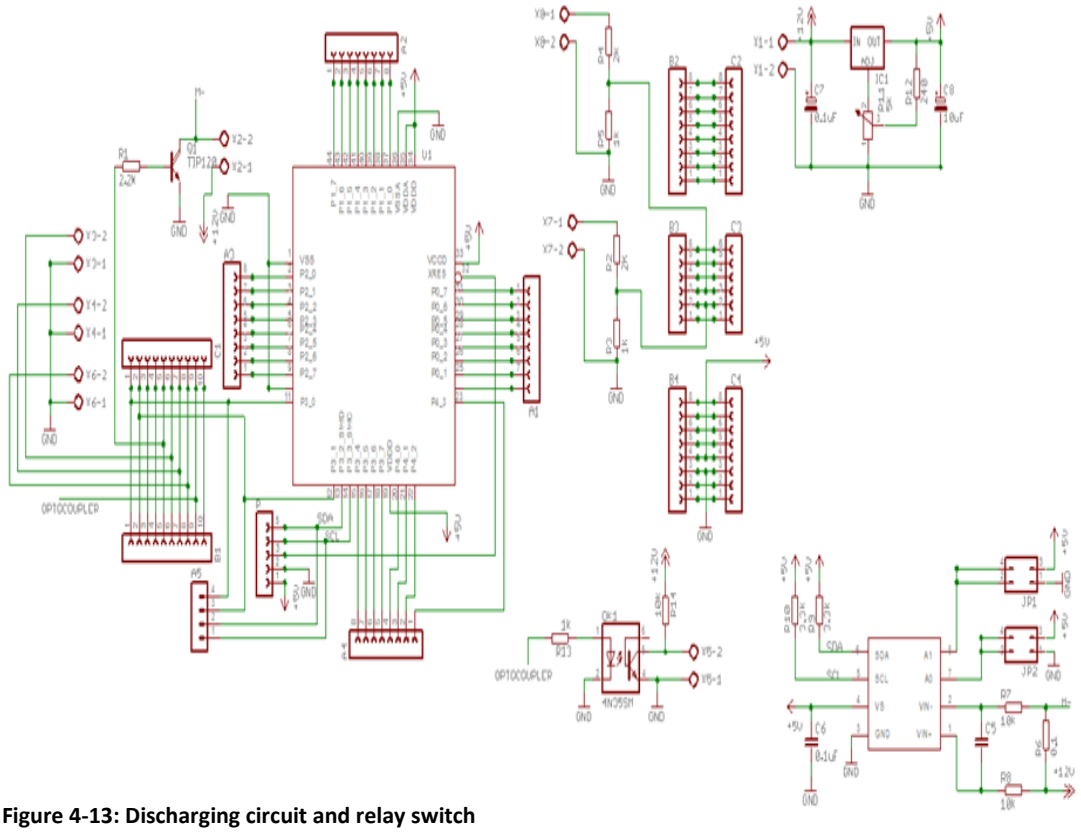


Figure 4-13: Discharging circuit and relay switch

The discharging circuit is also programmed with an Arduino; to set the discharge voltage (i.e. setting the voltage limit at which the SC module switches from discharge mode to charge mode), the load speed range should be fixed between load voltages $0V$ to $5V$ in manual or auto mode (i.e. choosing random speed from the minimum value to the maximum value). Manual mode allows the option of selecting specific

load speed (in other words, load current profiles). However, in this research work only four load profiles were selected to represent certain drive cycles. The load voltage is displayed during the discharge mode of the operation. The LCD keypad shield mounted on the discharging circuit made it easier to manually select the programmable options. Appendix D shows details of the codes for the discharging circuit.

4.3.4 Set-Up 3 Hardware Structure

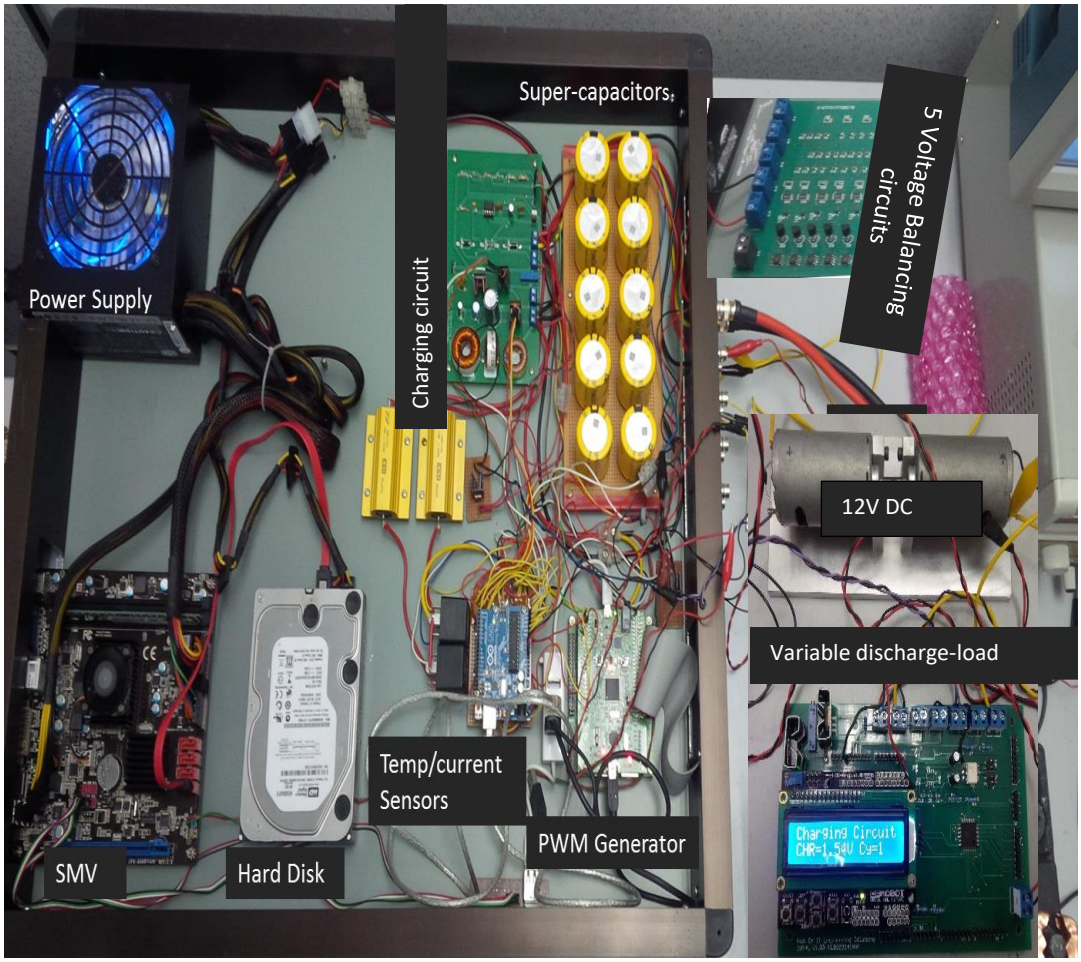


Figure 4-44: Set-Up 3 hardware configuration in a receptacle with labelled components

Figure 4-15: Set-up 3 running experiments with configuration receptacle sealed the output display on Arduino program

4.4 Voltage profiles of Supercapacitor test samples

To fulfill the test process of this research work as presented in experimental set-up (section 3.2). Hardware electronics employed, in sections 4.1 through 4.3, generated charge/discharge waveforms on the SC modules to expedite the ageing process of SCs.

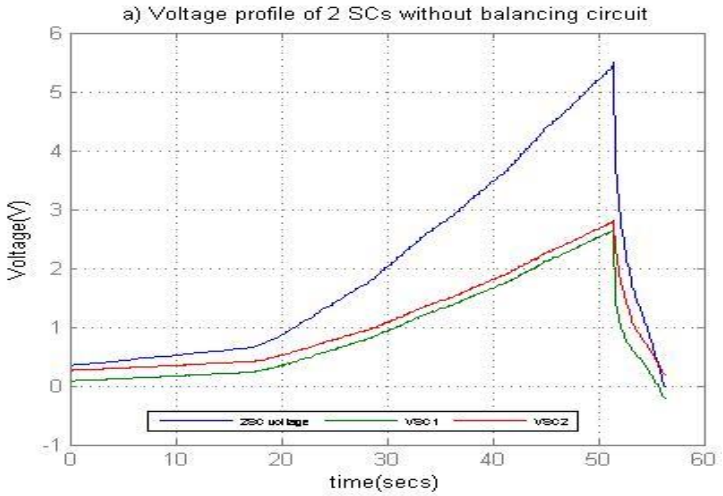
Table 4-5 represents 9 voltage profiles from 6 different SC module samples, with voltage profiles 1-3 generated from charge/discharge circuit 1 (section 4.1), voltage profile 4-5 from charge/discharge circuit 2 (section 4.2), and voltage profiles 6 through 9 from charging circuit and variable load discharging circuit (section 4.3). Each SC module sample presented in Table 4-5 also has a column describing its profile specifications.

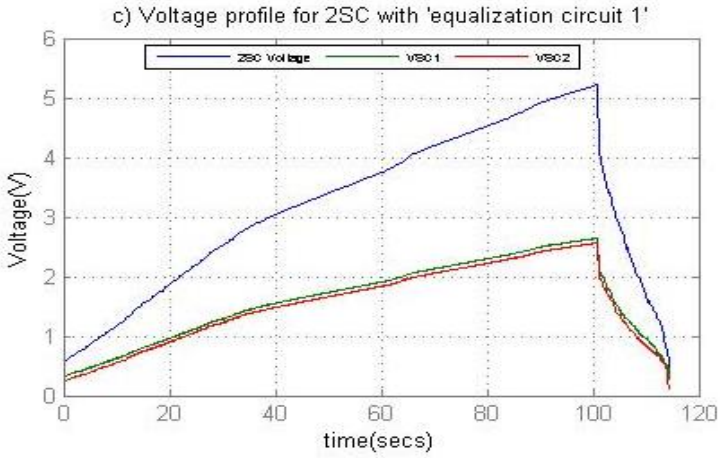
Voltage profiles 1 to 3 were generated to investigate the importance of balancing circuit in a SC module, although a study of such importance cannot be realized at the initial stage with just a single profile (without considering the ageing factors such as temperature and voltage (Bohlen et al., 2007a)). Nonetheless, it was still relevant to screen the calibre of balancing circuits chosen for the test process and compare them to modules without a balancing circuit. Hence the voltage profile 1 to 3 with their profile descriptions comparing their charge/discharge time, voltage drop and overall profile appearance against each other.

To investigate the load discharge effect on SC modules, voltage profiles 4 & 5 were generated, and Table 4-5 gives profile descriptions by comparing both waveforms with respect to charge/discharge time and voltage drop (which is used to determine internal resistance ESR, a potential end-of-life EOL criteria if the ESR recorded is more than a 100% increase from its initial impedance (H. Gualous et al., 2012))

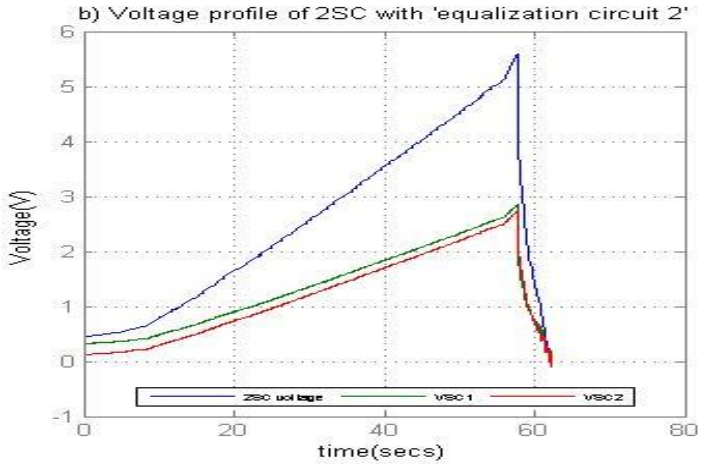
Whereas, voltage profiles 6 to 9 were generated under different conditions described in the same table 4-5 to simulate harsh conditions supporting drive cycle modes witnessed in specific EV/ HEV applications on load speed and charge/discharge cycles.

<table>
<tr><th>Test Samples</th><th>Profile Description</th><th>Voltage Profile</th></tr>
<tr><td>W5&W6
Voltage Profile 1</td><td>Voltage profile 1 was created from charging and discharging SCs (W5&W6) without a balancing circuit to protect the samples from over-voltage under a constant 0.5A. And because there was no added circuit to yield a load effect, the samples completed a cycle in less than a minute as shown in the table below. The reverse V-like shape at the apex gives the impression of a large voltage drop that produces an equally large ESR (Paul et al., 2015) (which over time degrades SC performance)

<table>
<tr><td>Samples</td><td>2SC voltage</td><td>VS1</td><td>VS2</td></tr>
<tr><td>Charge time (secs)</td><td>52</td><td>52</td><td>52</td></tr>
<tr><td>Discharge time (secs)</td><td>4</td><td>4</td><td>4</td></tr>
<tr><td>Discharge Voltage drop (V)</td><td>NV</td><td>1.78</td><td>1.8</td></tr>
<tr><td colspan="4">NV- Not Visible (unclear)</td></tr>
</table>
</td><td> 
</td></tr>
<tr><td>B7&B8
Voltage Profile 2</td><td>Voltage profile 2 was created from charging and discharging SCs (B7&B8) with ‘equalization circuit 1’ under a constant current of 0.5A. Unlike profile 1, profile 2 has longer charge time but charges faster by doubling the voltage of profile1 in the first 20secs. The increase in charge time and slow response can be expounded by the presence of ‘equalization circuit 1’. However, though, the decrease in voltage drop and subsequently ESR compensates for a healthier system operation over time.

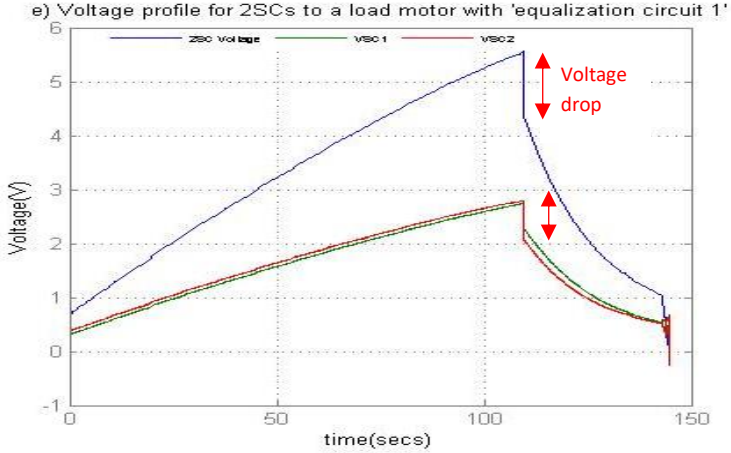
<table>
<tr><td>Samples</td><td>2SC voltage</td><td>VS1</td><td>VS2</td></tr>
<tr><td>Charge time (secs)</td><td>102</td><td>102</td><td>102</td></tr>
<tr><td>Discharge time (secs)</td><td>12</td><td>12</td><td>12</td></tr>
<tr><td>Discharge Voltage drop (V)</td><td>1.3</td><td>0.65</td><td>0.6</td></tr>
</table>
</td><td> 
</td></tr>
</table>

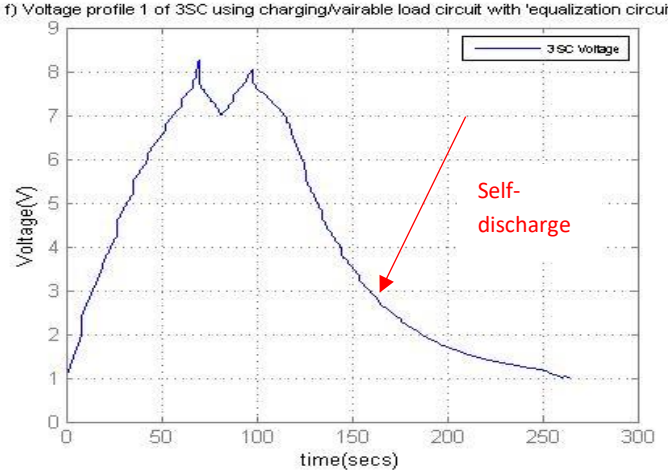
<table>
<tr>
<td>C9&C10

Voltage Profile 3</td>
<td>Voltage profile 3 was created from charging and discharging SCs (C9&C10) with ‘equalization circuit 2’ under a constant current of 0.5A. Profile 3 set to have completed a cycle just under a minute, similar to profile 1. Even with the presence of a balancing circuit, profile 3 exhibits no load effect or decrease in voltage drop (like profile 2), although it unveiled a faster charge than profile 1 in the first 20sec of the profile. This profile poses an unsettling response compared to the first two profiles.
<table>
<tr><td>Samples</td><td>2SC voltage</td><td>VS1</td><td>VS2</td></tr>
<tr><td>Charge time (secs)</td><td>58</td><td>58</td><td>58</td></tr>
<tr><td>Discharge time (secs)</td><td>7</td><td>7</td><td>7</td></tr>
<tr><td>Discharge Voltage drop (V)</td><td>NV</td><td>1.92</td><td>1.82</td></tr>
<tr><td colspan="4">NV- Not Visible (unclear)</td></tr>
</table>
</td>
<td> 
</td>
</tr>
<tr>
<td>MtA&MtB

Voltage Profile 4</td>
<td>Profile 4 is the voltage response to SC samples (MtA&MtB) that was charged up and discharged to a motor load (5V DC motor). Equalization circuit 2 is used to balance the voltage between the SCs (VSC1 and VSC2) with equal charge and discharge rate, but a large difference in their voltage drop, with VS2 showing a higher voltage drop of 1.05V to VS1. Another voltage drop can be noticed at the end of the discharge mode with similar voltage level aa the first voltage drop.
<table>
<tr><td>Samples</td><td>2SC voltage</td><td>VS1</td><td>VS2</td></tr>
<tr><td>Charge time (secs)</td><td>116.4</td><td>116.4</td><td>116.4</td></tr>
<tr><td>Discharge time (secs)</td><td>34.6</td><td>34.6</td><td>34.6</td></tr>
<tr><td>Discharge Voltage drop (V)</td><td>1.4</td><td>0.55</td><td>1.05</td></tr>
<tr><td colspan="4">NV- Not Visible (unclear)</td></tr>
</table>
</td>
<td> 
</td>
</tr>
</table>

<table>
<tr>
<td>MtC&MtD

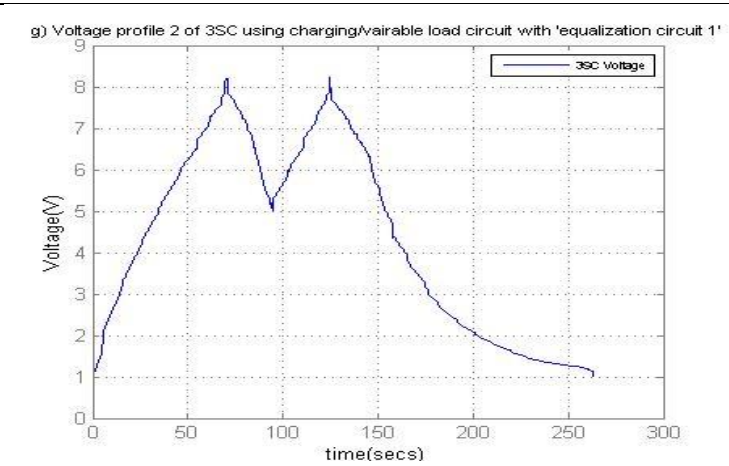
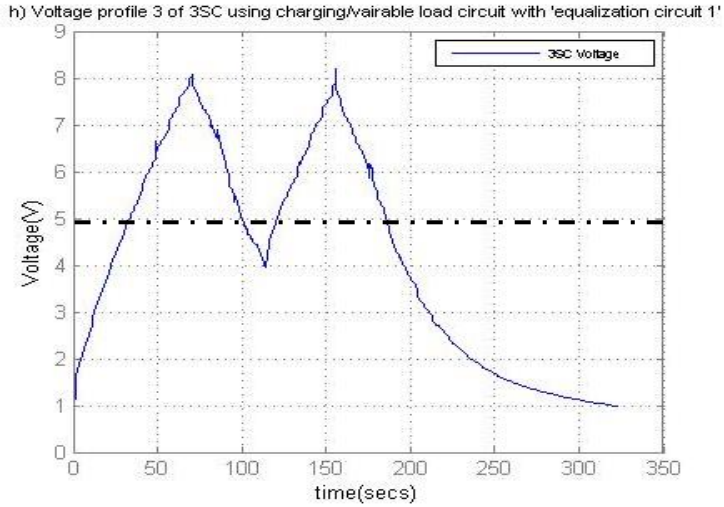
Voltage Profile 5</td>
<td>Voltage profile 5 have a similar response to profile 4 with a shorter charge/discharge time and a voltage drop difference of 0.2V between VS1 and VS2. Unlike profile 4, the Samples (MtC&MtD) voltage response coalesce at the end of the discharging phase, thus creating a single voltage drop on both VSC1 and VSC2.
<table>
<tr><td>Samples</td><td>2SC voltage</td><td>VS1</td><td>VS2</td></tr>
<tr><td>Charge time (secs)</td><td>109</td><td>109</td><td>109</td></tr>
<tr><td>Discharge time (secs)</td><td>37</td><td>37</td><td>37</td></tr>
<tr><td>Discharge Voltage drop (V)</td><td>1.14</td><td>0.45</td><td>0.65</td></tr>
<tr><td colspan="4">NV- Not Visible (unclear)</td></tr>
</table>
</td>
<td rowspan="2">e) Voltage profile for 2SCs to a load motor with 'equalization circuit 1'
 

f) Voltage profile 1 of 3SC using charging/vairable load circuit with 'equalization circuit 1"
 
</td>
</tr>
<tr>
<td>A;B;C

Voltage Profile 6

Using Load profile 1

(see Table 6-13)</td>
<td>Voltage profile 6 is the voltage response of a module with 3 SC samples (A; B; C). The module is charged up to the maximum voltage rating (8.1V) then discharged through a 12V DC load with a low Load current profile 1 (that could be manually selected as the maximum speed with a load voltage of about 5V) till the module reaches a set voltage of 7V, in which it is programmed to repeat the process automatically until the program is manually disconnected. After the system is disconnected, the samples self-discharges (with no load) as indicated in Table 4-5 graph f. The 12V motor load was used to simulate peak current demands for a steady-state condition during discharge mode.</td>
</tr>
</table>

A;B;C Voltage Profile 7 Using Load profile 2 (see Table 6-13)	Voltage profile 7 is the voltage response generated from SC module samples (A; B; C) after performing experimental tests using voltage profile 6 with the same samples under a predetermined timeframe. In this profile the module is charged up to the maximum voltage rating (8.1V) then discharged through a 12V DC load with a Load current profile 2 (i.e. the minimum speed with a load voltage of about 2.5V which is manually selected) till the module reaches a set voltage of 5V, in which it is programmed to repeat the process automatically until the application is manually disconnected. This profile simulates a steady-state condition during the discharge stage.	
A;B;C Voltage Profile 8 Using Load profile 3 (see Table 6-13)	Profile 8 on the other hand charges the same module to 8.1V then discharges it all the way to 4V with a Load current profile 3 (programmed with random load voltages between 0V to 5V). It was noticed however, during operation that the 12V DC motor load turns off (because the minimum power required to turn on the motor is 5V (which is also the voltage across the SC module)) forcing the SC module to self-discharge from 5V to 4V before it automatically charges up again to repeat the process all over again.	

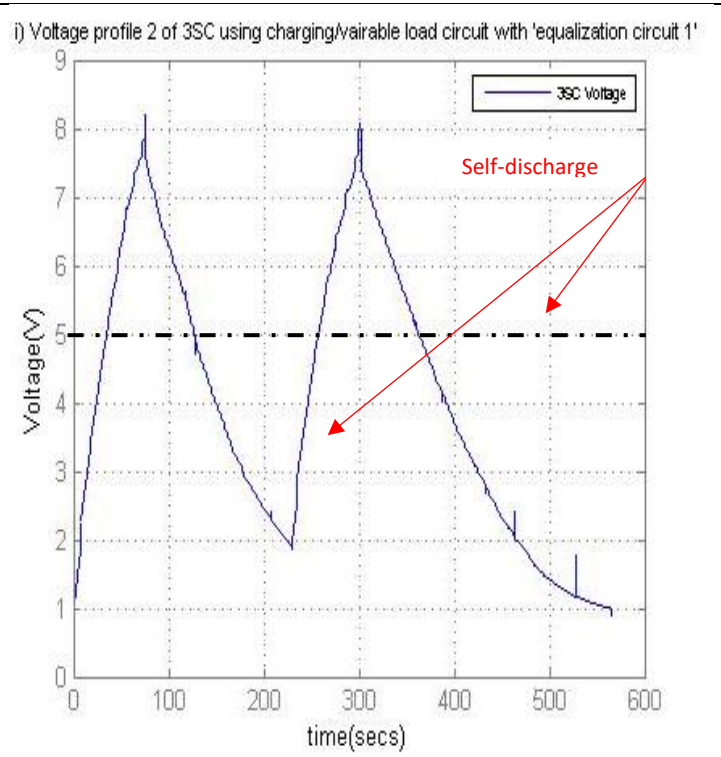
A;B;C Voltage Profile 9 Using Load profile 4 (see Table 6-13)	Similar to voltage profile 8, this profile also charges the SC module to 8.1V but in this case discharges it all the way to 2V with a Load current profile 4 (programmed with random load voltages between 0V to 5V). SC module samples A; B; C are almost entirely discharged in this profile with a random load speed (that is until the 5V limit mark) to simulate an unsteady operation condition thence creating a strenuous environment condition for the SC samples. The four profiles (i.e. 6-9) were chosen randomly to simulate a harsh and an irregular cycling condition to expedite the samples ageing behaviour. Experimental tests with this four profiles were initially set to observe the samples ageing behaviour. However, it is not normal to observe ageing effect on the samples with only four profiles, so if more tests are required to observe the ageing effect on samples A;B;C, the cycle is repeated again with the same four profile (6 to 9)	

Table 4-5: Test Samples voltage profiles with their descriptions

4.5 Summary

This chapter studied the electronic hardware employed in the acceleration tests carried in this research work. The chapter began by studying and comparing three types of voltage equalization/balancing circuits by; their working principles and power requirements, through simulation results from a spice model simulator. The simulations assisted in selecting “Circuit 3” as the preferred balancing circuit, to meet up the accelerated test specifications.

The chapter also describes hardware and software designs of charge/discharge circuits and charge/variable discharge load circuits used to perform the accelerated tests described in Set-Up 2 and Set-Up 3 respectively (section 3.3). Experimental results in the form of voltage profiles were presented and discussed according to accelerated test in Table 4-5.

CHAPTER 5 - PARAMETER MEASUREMENT TECHNIQUES AND SUPERCAPACITOR MODELLING

5 Outline

This chapter proposes a methodology to both characterize SC parameters and to model SC electrical and dynamic behaviour. It is divided into two parts; the first part focuses on SC measurement techniques, that is, measurement tools and methods currently used in the industry to characterize SC parameters are reviewed and compared. Based on the comparable results, this thesis proposes a suitable method(s) of parameter characterization.

The second part of this chapter describes the development of an initial model in the form of an electric equivalent circuit (EEC) using measuring techniques presented in the first part. This is done to model the electrical and dynamic behaviour of the SC, taking into account power requirements (in the form of accelerated ageing tests presented in chapter 6) and also considering SC ageing behaviour on specific ageing factors and environmental conditions. Also, model validation simulated both in frequency and time domains in comparison to experimental results is presented to prove model validity.

To understand and quantify SC ageing behaviour, SC parameters especially capacitance C and internal resistance ESR need to be characterised at its dormant stage (before undergoing experiments) so as to establish a benchmark to subsequent parameter characterization during accelerated test process. Periodic C and ESR parameter characterization is vital to the study of SC performance, as it is a collective agreement that SC end-of-life (EOL) is mostly characterized by a 20% loss of capacitance C and/or more than 100% increase in ESR (H. Gualous et al., 2012). In addition to the parameter characterization, modelling the electrical behaviour also provides a means of enumerating SC ageing behaviour.

While measurement methods for packaged SCs are well developed, different methods are currently being used in the industry and in laboratories worldwide which result in varying opinions being reported on papers. This raises uncertainties in interpreting the data on literature and manufacturer's datasheet for SC devices (Burke & Miller, 2010).

Most of the laboratory testing involved the application of cyclic voltammetry (CV) and Electrochemical Impedance Spectroscopy (EIS) test approaches. These approaches in most cases utilize small currents and limited voltage ranges and/or AC frequencies and are intended primarily to determine the electrochemical characteristics of the materials and electrodes used in the capacitors (Burke & Miller, 2010). However, testing on commercial devices is usually done using DC test procedures such as constant voltage/power test (Lajnef, Vinassa, Briat, Azzopardi, et al., 2007) (Chu & Braatz, 2002), but constant current test (CC) is largely the most popular method of testing used in the industry.

Rafik et al. in particular, has demonstrated the dependency of capacitance C on voltage (Rafik et al., 2007). Kurzweil et al. also agrees that capacitance determined by constant current test strongly depends on the discharge current and the voltage (state of charge) of the capacitor (P. Kurzweil & Chwistek, 2006b).

In summary, this chapter seeks to study the effect of measurement methods on SC capacitance C and ESR and consequently develop an EEC model, hence, the findings from this study will become a basis for the measurement methods used during the experimental process, and also a benchmark model for all subsequent EEC models developed after accelerated tests in chapter 6.

5.1 Parameter measurements using Industrial and Commercial Standards

Many industries have come up with several standard procedure to determine SC parameters with emphasis on DC tests. However, this research work reviews the most referenced standard IEC (International Electrochemical Commission) that provides a platform for developing International Standards. Reviews on (1) IEC 62391 standards for testing EDLCs, developed in 2006 (IEC 62391, 2006), and (2) IEC 62576 standardized test of ELDCs for HEVs (IEC 62576, 2009) were carried out. This research work does not simply end at studying SCs. Therefore, it was necessary to include standard (2) IEC 62576 to focus the study on the main research topic; i.e. studying SC behaviour for EV/HEV applications, thus putting its mode of operation into test consideration.

5.1.1 IEC 62391 Standard for testing EDLCs

IEC 62391 describes two methods of measuring capacitance: (1) constant current discharge method and (2) constant resistance charging method. And for measuring resistance, IEC 62391 recommends the following: (1) AC resistance method and (2) DC resistance method.

In the constant current discharge method, the SC is charged and discharged with a constant current. The charging and discharging cycle are separated by a voltage hold period for 30 minutes as shown in Figure 5-1. The capacitance is measured during the discharging cycle using Equation (5.1).

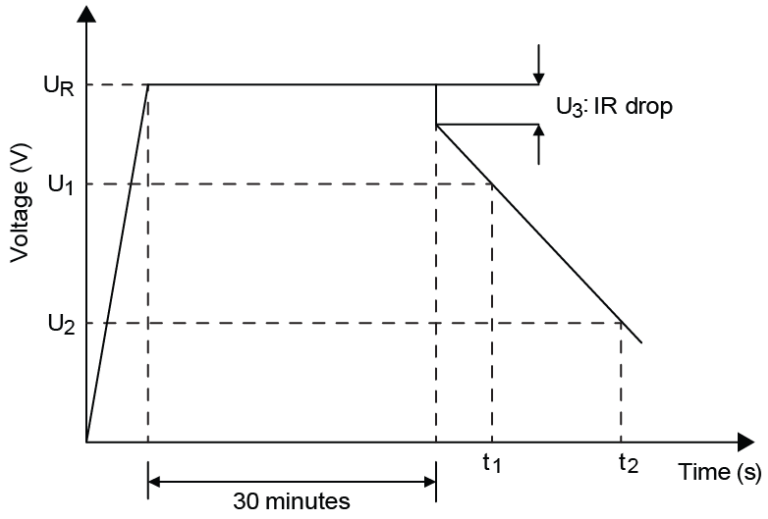


Figure 5-1: Voltage characteristic between supercapacitor terminals in IEC 62391 constant current discharge method. Adapted from (IEC 62391, 2006)

$$C = \frac{I \times (t_2 - t_1)}{(U_1 - U_2)} \tag{5.1}$$

Where C is the capacitance (F); I is the discharge current (A); U_1, U_2 is the measurement starting and ending voltage (V) respectively; t_1, t_2 is the time it takes for the discharge to reach $U_1\ and\ U_2$ (s) respectively.

The discharge current has to meet the conditions set by IEC 62391 based on the SC application; the discharge conditions are given in Table 5-1.

Classification	**Class 1**	**Class 2**	**Class 3**	**Class 4**
Application	Memory backup	Energy storage	Power	Instantaneous power
Charge time	30 min	30 min	30 min	30 min
I (mA)	$1 \times C$	$0.4 \times CU_R$	$4 \times CU_R$	$40 \times CU_R$
$\boldsymbol{U_1}$	The value to be 80% of the charging voltage $0.8 \times U_R$			
$\boldsymbol{U_2}$	The value to be 40% of the charging voltage $0.4 \times U_R$			
Note: C is the rated capacitance in F (Farad) and U_R is the rated voltage in V (Volt)				

Table 5-1: IEC 62391 Discharge conditions for measuring capacitance in supercapacitors (IEC 62391, 2006)

Meanwhile, in the constant resistance charging method, the capacitance was calculated by measuring the time constant for the SC to reach its rated voltage. The constant resistance charging method is not as widely used as the constant current discharge method. Hence, this method is not discussed in this chapter.

To measure resistance ESR of the SC, the AC resistance method recommends the frequency of the measuring voltage to be 1 kHz and the AC current should be from 1mA to 10mA. The ESR is then calculated by the following equation (IEC, 2006):

$$R_a = \frac{U}{I} \tag{5.2}$$

Where, R_a is the ac internal resistance (Ω), U is the effective value of ac voltage (V_{rms}), I is the effective value of ac current (I_{rms}).

In the DC resistance method, the method used is similar to the constant current discharge method for measuring capacitance, but with a different discharge current, depending on the class of the SCs.

The discharge current is specified in Table 5-2. ESR is measured at the beginning of the voltage drop observed at the discharging stage of the cycle using Equation (5.3).

$$R_d = \frac{\Delta U_3}{I} \tag{5.3}$$

Where, R_d is the ac internal resistance (Ω),ΔU_3, is the voltage drop (V), I is the discharge current (A).

Classification	**Class 1**	**Class 2**	**Class 3**	**Class 4**
I (mA)	$10 \times C$	$4 \times CU_R$	$40 \times CU_R$	$400 \times CU_R$
Note: C is the rated capacitance in F (Farad) and $U_R$is the rated voltage in V (Volt).				

Table 5-2: Discharge current in the DC resistance method (IEC 62391, 2006)

5.1.2 IEC 62576 standardized test of ELDCs for HEVs

Similar to IEC 62391, IEC 62576 adopts the constant current charging and discharging method to measure the capacitance and internal resistance ESR. The charging and discharging method similar to Figure 5.1 charges and discharges the SC with a constant current (capable of charging the SC with a 95% charging efficiency based on the nominal resistance), but this method, holds the voltage for only 300sec.

Before measurement, this standard has been pre-conditioned to be fully discharged and then incubated for 2h to 6h under reference temperature (the temperature set at 25°C ± 2°C as specified in IEC 60068-1).

Charging current I_c used in this standard is calculated using Equation (5.4)

$$I_c = \frac{U_R}{38R_N} \tag{5.4}$$

Where, I_c is the charging current (A); U_R is the maximum voltage (V); R_N is the capacitor's nominal resistance (Ω).

Moreover, the discharging current was chosen from the discharge conditions shown in Table 5-1. Since HEV performs Instantaneous power application, a class 4 current has been selected.

$$I_d = \frac{U_R}{40R_N} \tag{5.5}$$

Where, I_d is the discharge current (A); U_R is the rated voltage (V); R_N is the nominal internal resistance

The capacitance is measured during the discharging cycle using Equation (5.6).

$$C = \frac{2W}{(0.9U_R)^2 - (0.7U_R)^2} \tag{5.6}$$

Where, C is the capacitance (F); W is energy (J) dischargeable from $(0.9U_R)$ 90% of U_R to $(0.7U_R)$ 70% of U_R; U_R is the rated voltage (V)

Moreover, the internal resistance ESR is determined similarly to IEC 62391 standard using Equation (5.3).

Although IEC 62391 provides guidelines on how the measurement method should be conducted and the amount of current to be used when discharging SCs, SCs manufacturers have provided their discharge current condition. Moreover, manufacturers like Maxwell Technologies have published their test procedure to suit their production line environment (Maxwell Technologies, 2010). In fact, a survey of 15 SC manufacturers all over the world shows that the discharge current used by these manufacturers varies from 1mA/F to 75mA/F (see Table 5-3 to Table 5-5). Despite the variation, the discharge current chosen did not affect the lifetime of the SCs.

Besides the variation of SC discharge current, the differences in the voltage holding period between charging and discharging cycle seem to influence the capacitance and ESR values. IEC 62391 recommends a $30\ minutes$ voltage holding, while IEC 62576 recommends a much shorter voltage holding period of $300\ seconds$, which is familiar in the industry to manufacturers like NESSCAP (South Korea) Illinois capacitor (USA) holds the voltage for $5\ minutes$ before applying discharge current on their SCs during characterization tests. In contrast, Maxwell (USA), has a 6 step process for measuring capacitance and ESR, and it advocates the use of a resting period between charge and discharge; that is, the SC is left at open circuit for a predefined time (Maxwell Technologies, 2010).

Manufacturer (Origin)	Commercial Name	V (V)	C (F)	T (℃)	Type	Parts/ Test Current
NEC TOKIN (Japan)	Super capacitor	2.7 to 12V	0.01 – 200F	-2.5 to 70℃	Bulk, taping, winded	HV series/ 1mA/F
Panasonic (Japan)	Gold capacitor	2.3 to 5.5V	0.022 to 70F	-10 to 70℃	Coin type, Cylin-drical	HW series/1mA /F
ELNA (Japan)	DYNACAP, POWERCAP	2.5 to 6.3V	0.047 to 1500F	-25 to 85℃	Cylin-drical cell	DZ series/ 1mA/F
MAXWELL (USA)	BOOSTCAP Ultracapacitor	2.7-160V	1 to 3400F	-40 to 85℃	Cylin-drical cell, module	HC series/ 75mA/F
VINA Tech (South Korea)	Hy-Cap	2.5-6V	0.5 to 500F	-40 to 70℃	Cylin-drical cell, module	Single cell series/ 1mA/F
NICHICON (Japan)	EVerCAP	2.5-2.7V	0.47 to 6000F	-40 to 70℃	Cylin-drical cell, stacked	UK series/ 0.01A
NESSCAP (South Korea)	NESSCAP EDLC	2.3 to 2.7V	3 to 3000F	-25 to 65℃	Cylin-drical cell, primatic	10mA/F

Table 5-3: Discharge current used by supercapacitor manufacturers adopted from (Naim, 2015)

Manufacturer (Origin)	Commercial Name	V (V)	C (F)	T (℃)	Type	Parts/ Test Current
Vishay (USA)	196 DLC	5.5 to 6.3V	0.047 to 1F	-25 to 85℃	Cylin-drical	(0.047 to 0.33F)/ 0.1mA (0.47 to 1F)/ 1mA
Taiyo Yuden (Japan)	PAS capacitor	2.3 to 3V	0.011 to 50F	-25 to 70℃	Cylindri-cal	(1 – 22F)/ 1A 56F/ 5A 4F/0.5A (9 & 20F)/ 1A 50F/ 2A
Illinois capacitor (USA)	Super capacitor	2.3 to 5.5V	1 to 3800F	-25 to 70℃	Cylin-drical cell	DCN series/ 10mA/F
Korchip (South Korea)	STARCAP	2.3 to 7.5V	0.047 to 120F	-40 to 70℃	Coin type, cylin-drical, stacked	DR series/ n/a
Tecate (USA)	Powerburst	2.3 to 2.7V	0.33 to 400F	-40 to 85℃	Cylin-drical	TPL series/ n/a
CAP-XX (Australia)	CAP-XX Supercapacit or	2.3 to 5.5V	80mF to 2400 mF	-40 to 85℃	Pris-matic	100mA

Table 5-4: (Continuation) Discharge current used by supercapacitor manufacturers adopted from (Naim, 2015)

Manufacturer (Origin)	Commercial Name	V (V)	C (F)	T (°C)	Type	Parts/ Test Current
Cooper Bussman (USA)	PowerStor	2.5-16V	0.1-600F	-40 to 70°C	Coin, cylin-drical, module	n/A
AVX (USA)	BESTCAP	3.6V to 15V	6.8mF to 1F	-20 to 70°C	Planar	BZ series/4mA
Note: V is the rated voltage, C is rated capacitance, T is the operating temperature. All data are obtained from manufacturers' product data sheets and technical documents, available on their respective websites.						

Table 5-5: (Continuation) Discharge current used by supercapacitor manufacturers adopted from (Naim, 2015)

5.2 Capacitance and ESR measurement tests

This chapter explores some measurement methods for characterizing SC capacitance and ESR; comprising of constant current (CC), cyclic voltammetry (CV) and Electrochemical Impedance Spectroscopy (EIS) test. The constant current test (CC) is a DC measurement method that includes the IEC standard test process discussed in section 5.1 and the Maxwell 6 process (Maxwell Technologies, 2010). In addition to the IEC standard and Maxwell's method, other CC methods were considered using direct charge-discharge cycle without any voltage holding/open circuit usually carried out in laboratories with reference to; (Ban et al., 2013),(Cazorla-Amorós et al., 2010), (Dandeville et al., 2011b) and (Masarapu, Zeng, Hung, & Wei, 2009).

Cyclic voltammetry (CV) and Electrochemical Impedance Spectroscopy (EIS) test methods, on the other hand, are not widely used in the industry. Hence, there are no standard procedures available to adopt. However, literature on laboratory testing such as (Stoller & Ruoff, 2010b) have indicated the dependency of capacitance particularly on scan rate and voltage range in CV measurements. Likewise, capacitance also depends on the applied frequency in EIS measurement. In IEC 62391, EIS measurement method is given less emphasis, although it is recommended as an alternative to dc measurement methods, particularly in a time-constrained situation.

With some uncertainties in SCs measurement methods, the following experimental procedure is designed to seek the appropriate test settings for the SCs tested in this thesis, thus finding how results from these methods differ from one another.

5.2.1 Measurement Set-Up

The Supercapacitor employed for this test process is Maxwell Technologies product with a rated voltage of 2.7V and rated capacitance of 25F. All three test methods; Constant Current test, Electrochemical Impedance Spectroscopy, and Cyclic Voltammetry were carried out. The measurements were performed using AUTOLAB PGSTAT302N potentiostat/galvanostat, equipped with the FRA2 module from Metrohm Autolab B.V, by connecting the supercapacitor sample to a two-electrode attached to the AUTOLAB.

5.2.2 Constant Current Test (CC)

5.2.2.1 IEC Standards and Maxwell 6 step process Test methods

The constant current (CC) test identified in IEC 62391 and IEC 62576 were compared with the Maxwell 6 Step Process.

The test procedure for IEC 62391 was carried out by applying SC terminals to imitate the voltage characteristic described in Figure 5-1. To measure capacitance, the SC is charged to its rated voltage $2.7V$ using a charging current I_c at high current value of $2A$ (which is also the maximum current value administered by the AUTOLAB PGSTAT302N) to charge the SC for a duration of $30minutes$ till the rated voltage is reached. The SC charge is held at constant voltage of $2.7V$ for $30\ minutes$ and then discharged with an applied current I_d of class 2 (used for energy storage application) obtained from discharge conditions shown in Table 5-1, which approximately gives the current value of $0.025A$ to discharge the SC till $0V$. To measure the ESR, the same process is applied to the SC, but a different discharge current using similar application class 2 as measuring capacitance is selected from discharge current in Table 5-2, which approximately gives the current value of $0.25A$.

IEC 62576 standard test also employs the voltage characteristics between the SC terminals shown in Figure 5-1 to measure both capacitance and ESR values, but with a shorter voltage hold duration of 300 seconds. This test applies a charging current I_c and a discharging current I_d, from Equation 5.4 and 5.5 respectively, which are valued at approximately 1.5A.

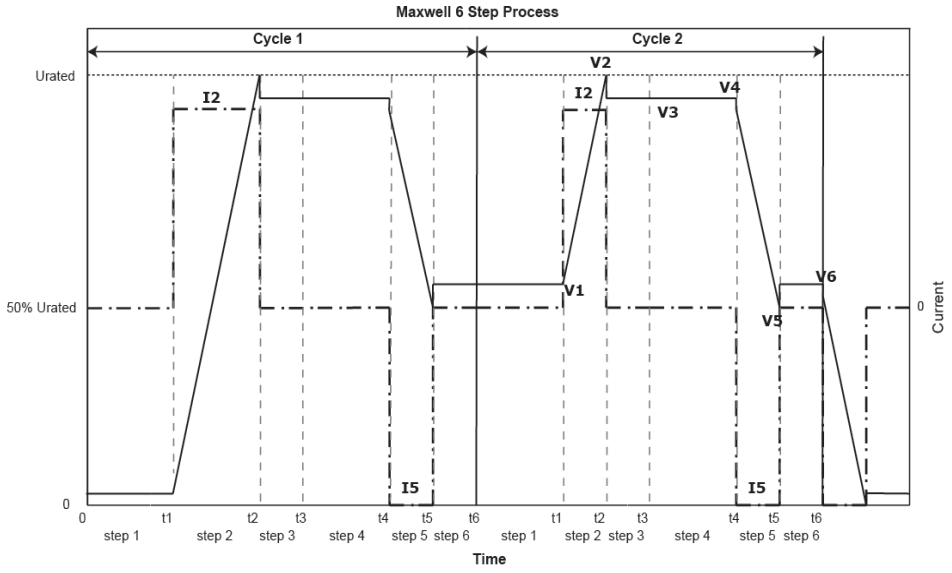


Figure 5-2: The current profile used in Maxwell 6 step process and the voltage response at SC terminals. Figure adapted from (Maxwell Technologies, 2010)

Maxwell 6 step process, on the other hand, emulates the voltage and current characteristics in Figure 5-2. The Process postulates a charge and discharge current rate of $75mA/F$ which gives a test current of $2A$. The process begins with a rest period of 10s. Then using the specified test current, the SC is charged to $2.7V$, after that, it is left at open circuit for 15s. Next, the SC is discharged to one-half its rated voltage ($1.35V$). This process is repeated twice. After the second cycle, the SC is left to rest again for 5s before being completely discharged to $0V$. Capacitance and ESR, according to Maxwell step process are determined from the profile characteristics using the Equations (5.7) and (5.8) respectively below:

$$C = \frac{I_5 \times (t_5 - t_4)}{(V_5 - V_4)} \tag{5.7}$$

$$R = \frac{(V_5 - V_6)}{I_5} \tag{5.8}$$

In IEC 62391, the capacitance is determined from constant current discharge curves using Equation (5.1), and the ESR is calculated according to Equation (5.3) while IEC 62576 calculates its capacitance with Equation 5.6, and ESR according to IEC 62391 standard (using Equation (5.3)). On the other hand, Maxwell 6 step process uses the discharge curve of the second cycle to calculate the capacitance and the ESR with Equations (5.7) and (5.8) respectively. The first cycle is not used because, during this time, the SC is not fully activated. Hence, the capacitance and the ESR values will be different from the second cycle.

Table 5-6 shows the capacitance and ESR from three methods. IEC 62391 reports the highest capacitance of all three methods while IEC 62576 has the highest ESR value of all three methods. Both IEC standards 62391 and 62576 uses the voltage hold method at different rest times and different discharge currents of $0.025A$ and $1.5A$ respectively, while Maxwell 6 process uses the open-circuit method with an even shorter rest time than the standards, with the highest discharge current at $2A$, IEC 62391 with the highest capacitance followed by IEC 62576, and then Maxwell's 6 process. On the other hand, the ESR was measured using similar method as the capacitance, observing the highest ESR result with the IEC 62576, followed by IEC 62391; and the lowest result was recorded by the Maxwell's 6 step process. The irregularities observed by these three widely used standard methods may have been contributed by two main characteristics of the standard method, which are; (a) variance in the discharge current and (b) the technique (of either voltage hold or open circuit) and the rest time duration between charge and discharge.

Constant Current (CC)				
Methods		**IEC 62391**	**IEC 62576**	**Maxwell 6 Process**
REST TIME (secs)		**Voltage Hold**		**Open Circuit**
		1800	300	15
Test current to measure capacitance	Charge Current I_c (A)	2	1.5	2
	Discharge Current I_d (A)	0.025	1.5	2
Capacitance (F)		29.08188	27.70888	26.27857
Test current to measure ESR	Charge Current I_c (A)	2	1.5	2
	Discharge Current I_d (A)	0.25	1.5	2
ESR (Ω)		0.0516	0.071267	0.0456

Table 5-6: Capacitance and ESR from IEC Standards and Maxwell 6 Step Process.

5.2.2.2 Supplemental Constant Current Test methods

The discrepancies shown by the results (in Table 5-6) from the IEC standards and Maxwell 6 process test fostered the need to test further the effects of voltage holding and be open to specific test currents on SCs. Various SC manufacturers have adopted different discharge current conditions and have also recommended specific voltage hold/open circuit durations which create a rest time that generates a voltage drop

suitable for parameter measurement. Therefore, the effect of holding the voltage between charge and discharge on the capacitance and the ESR is studied. For the test, two voltage holding/SC open circuit periods were used: $30\ minutes$ and $3\ minutes$, to ensure accurate comparison between the effects of holding the voltage and leaving the SC at open circuit between charge and discharge set to $2A\ (75mA/F)$. For the purpose of investigating the effect of different current level on capacitance and ESR, the experiment was repeated with $0.025A\ (1mA/F)$ discharge current, to calculate the capacitance, and then with $0.25A\ (10mA/F)$, to calculate the ESR. And for reference, the direct charge and discharge method is conducted on the SC.

Constant Current (CC) test method					
Capacitance (F)					
Rest Duration	**30 mins**		**3 mins**		**Direct charge-discharge**
	Voltage hold	**Open circuit**	**Voltage hold**	**Open circuit**	
2A	27.8760	27.0073	28.2035	27.5429	27.3067
0.025A	29.0819	28.5815	-	-	28.6155
ESR (Ω)					
2A	0.04315	0.07383	0.042875	0.042575	0.15368
0.25A	0.0516	0.0536	0.044	0.044	0.0416

Table 5-7: The effects of voltage hold and open circuit rest duration on the capacitance and ESR

Table 5-7 shows the influence of voltage hold and open circuit duration on capacitance and ESR. The result from voltage hold gives a higher capacitance than the open circuit method, regardless of the test current and the rest duration, while the open circuit method gives the smallest capacitance, followed by the direct charge-discharge. The most pronounced observation shows the capacitance is higher with the 0.0252A discharge current than with the discharge current leveled at 2A for all three methods. Effect of capacitance is measured at the discharge phase of the voltage profile, so it is not surprising that the results recorded with $0.025A$ between all three methods have a small difference of $\pm 0.5F$ and those with the $2A$ have a difference of $\pm 0.8F$. Even with the lowest capacitance registered at the $30mins$ open circuit as $27.0073F$, a $+2F$ increase to the manufacture's datasheet specifications of 25F (Technologies) is recorded and the discrepancy between these two values renders these three methods unsatisfactory to measure SC capacitance.

The variation in ESR values gathered in Table 5-7 confirms how significantly each method affects the ESR. The direct charge-discharge produces the highest ESR, followed by the results from the open circuit method and the voltage hold method, where all methods are conducted in $30\,minutes$ duration, with $2A$ discharge current. When the discharge current is reduced to $0.25A$, the trend no longer holds; the open circuit method produces the highest ESR, followed by the voltage hold method, and then the direct charge-discharge method.

In the $3\,minutes$ duration with $2A$ discharge current, voltage hold method gives a higher ESR compared to the open circuit method, with a microscopic difference. This observation contradicts the one in the $30\,minutes$ test, in which the open circuit

method produces a higher ESR than the voltage drop method, with a larger difference that cannot be simply overlooked. When the discharge current is reduced to $0.25A$ in the $3\ minutes$ test, both the voltage hold and the open circuit methods give the same ESR. The $30\ minutes$ test with $0.25A$ discharge current records similar results for both voltage drop and open circuit method with negligible difference. In addition to the results of both the $30\ minutes$ and $3\ minutes$ methods, a record of the lowest ESR value with the direct charge-discharge method is an un expected one as it was initially assumed that the direct charge-discharge method, regardless the level of discharge current, would produce the highest ESR.

Comparing the results from both durations, we can see there is a consistency in the results from the $30\ minutes$ test, no matter if it is a $2A$ discharge current or a $0.25A$ discharge current, the open circuit method will give a higher ESR than that of the voltage hold method.

The purpose of voltage hold is to compensate for the voltage drop due to charge redistribution effect. During the voltage hold period, charges will have more time to penetrate deeper inside the pore, thus charging the entire surface (Kaus, Kowal, & Sauer, 2010b) (a detailed analysis of the charge redistribution in SCs can be found in Kowal et al., 2011). It is noteworthy that the difference in the results from the $30\ minutes$ voltage hold and the $3\ minutes$ voltage hold, where both tests use $2A$ discharge current, is so small that it is almost negligible. Furthermore, the $3\ minutes$ voltage hold also yields nearly the same ESR with that of the $3\ minutes$ open circuit method. This shows that $3\ minutes$ is actually enough to let the charge to redistribute inside the pore and become uniformly distributed.

Reducing the current to $0.25A$, increases the discharging time, which provides enough time for the charge to travel deep inside the porous electrodes and sufficiently charge the entire surface area. In the 3 minutes duration, the charge has already become uniformly distributed using the $0.25A$; that is the reason why the ESR values from the open circuit method are equal to the ESR from the voltage hold method. Similarly, the ESR after $30\ minutes$ of open circuit is almost the same as the ESR measured after $30\ minutes$ of voltage hold. This shows that, the smaller the discharge current, the shorter the rest duration needs to be; as the ESR records the lowest value with the charge-discharge method, followed by the $3\ minutes$ method and $30\ minutes$ method. In the case of the $30\ minute$s method, no real voltage drop is observed during testing. Based on these findings, it shows that the $3\ minutes$ open circuit duration is sufficient for the charges to rearrange themselves and charge the electrode surface. Similarly, if voltage hold method is employed to minimize the effect from voltage drop due to charge distribution, this duration is enough to hold the charge.

As expected the ESR from the direct charge-discharge method with the $2A$ charge current triples the value of the manufacturer's ESR specification (Technologies). Under a high $2A$ current charge, a very short charge/discharge time with an incomplete charge regime is very likely. Usually when charging, the charge will fill the pores located near the outer surface, that is the meso-pore, and then progressively charging into the inner pores. After the charging is stopped, the charges begin to distribute themselves to fill the pores located deeper in, until a uniform voltage distribution is achieved (Kowal et al., 2011). But in this method in which the charge time is shortened, the charges do not have sufficient time to charge the inner pores,

which consists of a much smaller pore size. In the direct charge-discharge method, the measurement is recorded immediately after discharge. This means that the charge has yet to redistribute to sufficiently charge the electrode surface and achieve a uniform voltage, thus voltage drop is higher. In contrast, the charge is given some time to penetrate and charge the electrode surface in open circuit method, thus giving a smaller ESR than that from the direct charge-discharge method. The redistribution of charges inside the porous electrode of the SC can be observed visually when the SC is left in open-circuit i.e. by monitoring the voltage decay. Therefore, voltage lost is higher in the direct charge-discharge method than the open circuit method and the voltage hold method.

In conclusion, the high voltage lost not only gives a rise to ESR but it but also affects the capacitance indirectly, by reducing the charge-discharge time of the SC as has been observed in the results earlier. It has been said previously that the charging time affects the amount of voltage lost in SC. The charging time can be extended so as to increase the charge penetration, by introducing a voltage hold period between charge and discharge cycle, or by using a smaller current.

5.2.3 Cyclic Voltammetry Test (CV)

In cyclic voltammetry (CV) test, an electric potential is imposed at the SC electrodes which vary periodically and linearly with time (H. Wang & Pilon, 2012), i.e. the voltage is swept respectively between $0V$ and $2.7V$ with a fixed scan rate. After the sweep reaches the set $2.7V$, the scan is reversed and the voltage ramp is also reversed from $2.7V$ to $0V$ to measure the resulting current. Capacitance is typically measured at

different scan rates to gauge SC performance (W.G Pell & Conway, 2001) (Byon, Lee, Chen, Hammond, & Shao-Horn, 2011) (Yan et al., 2010) (H. Wang & Pilon, 2012). According to Kurzweil & Chwistek, 2006, Wang & Pilon, 2012, measured capacitance increases with lower scan rates and predicted to be close to the actual capacitance under equilibrium conditions. As a result, the effect of scan rate is studied by testing and measuring capacitance at six different scan rates, that is; $10mV/s, 20mV/s, 30mV/s, 40mV/s\ 50mV/s$, and at $100mV/s$. For each test, the CV is repeated twice. The resulting current is measured and recorded on a current-voltage curve.

In the case of an ideal SC, the CV plot will be a rectangle. Therefore, the capacitance can easily be calculated by using the following equation (Wendy G Pell & Conway, 2001) (W.G Pell & Conway, 2001),

$$C = I/\frac{dv}{dt} \tag{5.9}$$

Where, I is the average current during discharge and $\frac{dv}{dt}$ is the scan rate.

However, In the case of a SC, the CV creates a leaf-like shape waveform, due to the non-ideality in real devices. Therefore, the charge is calculated by integrating the current-voltage curve, as per Equation (5.10) (Kovalenko, Bucknall, & Yushin, 2010). The relation between charge Q and the scan rate can be written as follows,

$$Q = \int_0^{\Delta t} I(t)dt = \frac{1}{v}\int_0^{\Delta U} I(U)dU \text{ and } v = \frac{dU}{dt} \tag{5.10}$$

Where, v is the scan rate.

The capacitance can then be computed using the following equation,

$$C = \frac{Q}{V_{max} - V_{min}} \tag{5.11}$$

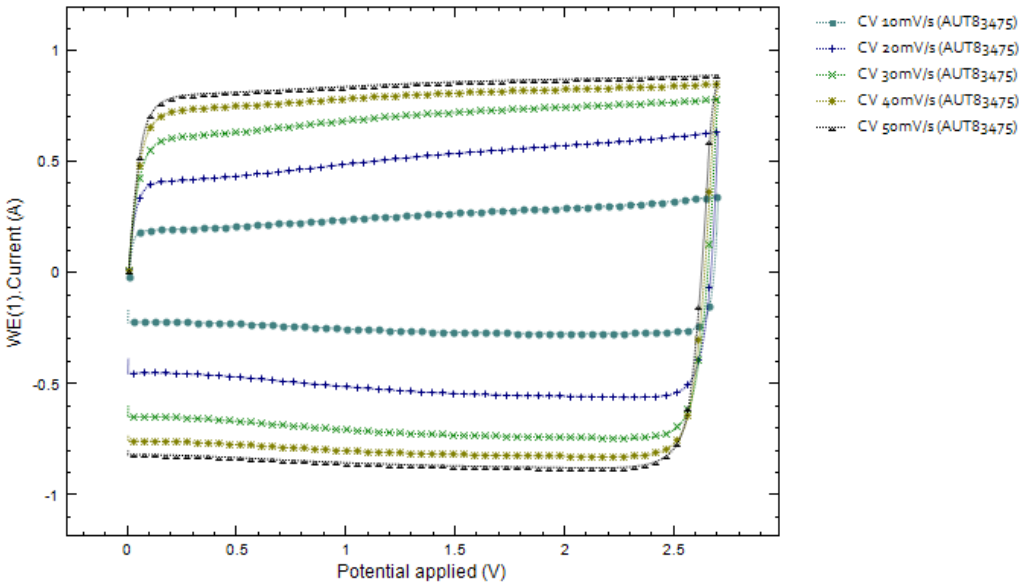


Figure 5-3: Cyclic Voltammetry at scan rates 10mV/s, 20mV/s, 30mV/s, 40mV/s and 50mV/s

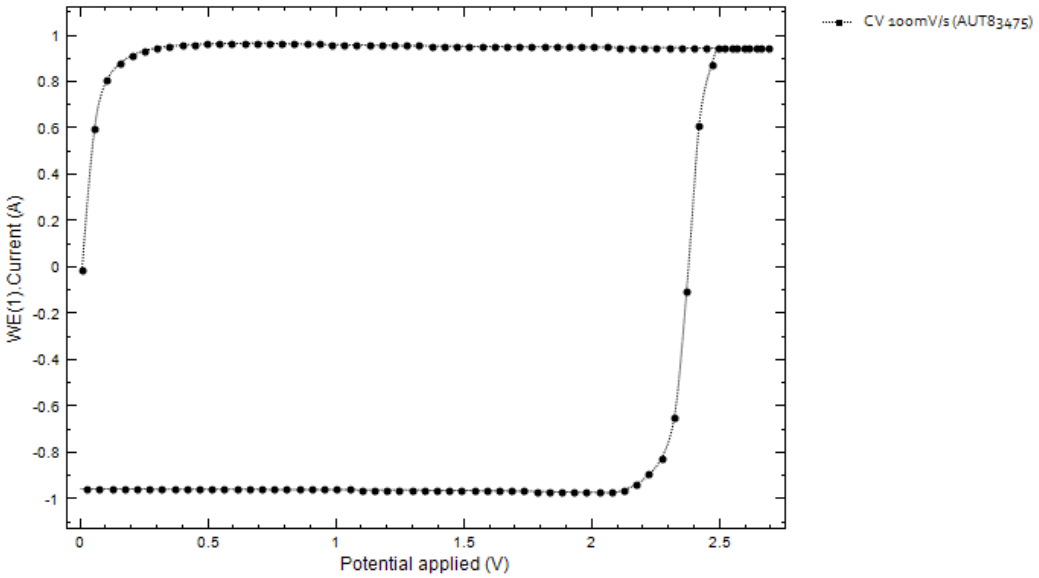


Figure 5-4: Cyclic Voltammetry at scan rates 10omV/s

Figure 5.3 shows five SC CVs at scan rates $10mV/s$ to $50mV/s$ in $10mV/s$ increments and Figure 5-4 shows SC CV at $100mV/s$. It can be seen that the selection

of scan rate influences the current-potential wave-shape. The width of the wave-shape increases with higher scan rate. As the scan rate is increased to $100mV/s$, the wave-shape become distorted, particularly when reversal of the scan begins. $100mV/s$ scan may be too fast for the electrochemical reactions to occur, thus, the CV wave-shape drifts away from the usual rectangular wave-shape.

Scan Rate (mVs^{-1})	Capacitance (F)
10	23.4055
20	24.6510
30	24.8595
40	24.7401
50	24.6722
100	21.5300

Table 5-8: Effect of Scan rates on SC capacitance

The capacitance measured and calculated at each scan rate is given in Table 5-8. While the capacitance was initially expected to increase with slower scan rate, as observed in Kurzweil, Frenzel, & Gallay, 2005 and Masarapu et al., 2009, the measured capacitances show opposite trends to decreasing scan rate. From $10mV/s$ to $30mV/s$, the capacitance climbs gradually; however, when the scan rate is increased further, the capacitance starts to drop, with a noticeable plunge/bump at $100mV/s$. It is also noted that the capacitance at 30mV/s is the closest to the capacitance in the manufacturer's, specification of $25F$.

The fluctuation in the measured capacitance at different scan rates is also seen in the work of Stoller & Ruoff, 2010. This observation shows that it is important to find the most suitable scan rate for the material tested. The assumption, in which slow scan

rate produces higher capacitance, may not hold true in all materials. Therefore, it is recommended for researchers to run tests at several scan rates before deciding on a scan rate.

Apart from that, in reality, real applications have a 'scan rate ceiling', observed by Zhang, 2010. Often, the upper limit of a scan rate of material can be perceived from the CV wave-shape—the voltammogram becomes leaf-shaped or olive-shaped. A change in the CV wave-shape is a sign that the electrochemical reactions have some trouble in proceeding properly (S. Zhang, 2010). The upper limit of scan rate is contributed to many factors like ion accessibility and bulk conductivity in electrodes. For the case tested in this thesis, the upper limit for the SC was $100mV/s$, in which the wave-shape became more of a leaf-shaped. From the CV results, $30mV/s$ was the most suitable scan rate for the SC.

5.2.4 Electrochemical Impedance Spectroscopy Test (EIS)

EIS is carried out on the SC by applying a small sinusoidal signal to the system. If the system is linear, the current response will also be a sinusoid and have the same frequency as the applied voltage signal but shifted in phase by the angle ϕ (Gamry, 2010), as shown in Figure 5-5.

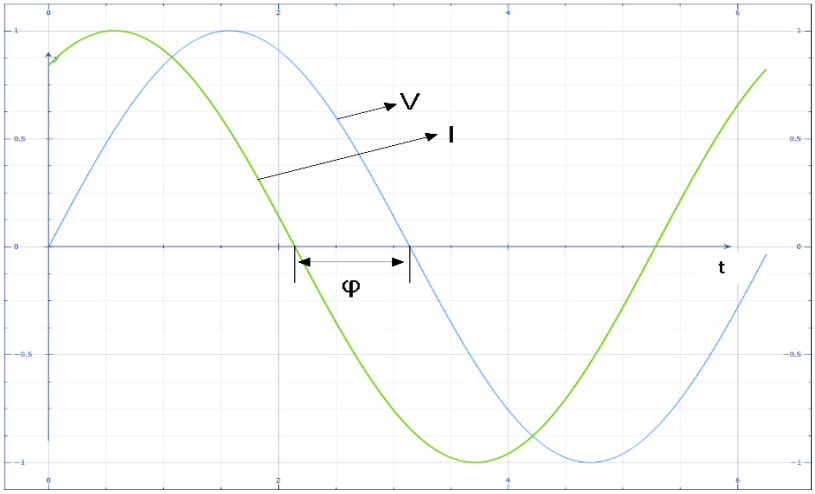


Figure 5-5: Sinusoidal voltage perturbation and current response in a linear system.

The sinusoidal voltage is given by,

$$V_t = V_0 \sin(\omega t) \tag{5.12}$$

Where V_t is the voltage at time t, V_0 is the signal amplitude, $\omega = 2\pi f$ is the angular frequency.

The responding current signal is,

$$I_t = I_0 \sin(\omega t + \varphi) \tag{5.13}$$

Therefore, the impedance of the system, by Ohm's law, can be calculated as,

$$Z = \frac{V_t}{I_t} = \frac{V_0 \sin(\omega t)}{I_0 \sin(\omega t + \varphi)} = Z_0 \frac{\sin(\omega t)}{\sin(\omega t + \varphi)} \tag{5.14}$$

The impedance of the system is displayed in a bode plot and is expressed regarding magnitude Z_0, and a phase shift ϕ.

EIS measurement method of the SC design depends on the selection of (1) the frequency range and a number of frequencies and (2) the signal perturbation amplitude, to minimize the risk of error of judgement and to ensure the information

obtained is adequate for identifying all possible processes involved in the overall response.

The frequency range selected should be sufficiently wide to observe the dynamic response of the system under study. Depending on the system's time constants, typically the range starts from $10kHz$ down to $10mHz$. Although the duration of a complete measurement is largely influenced by the low frequency, generally, the lower the frequency, the longer the time it takes to complete the test (refer to Table 5-9). In addition, a careful selection in the number of frequencies and integration time is also necessary to avoid erratic and futile data. The frequencies should be equally distributed and all responses be captured in a logarithmic distribution. The integration time is the time during which the impedance response of the cell is recorded for data analysis. The $1.25s$ecs integration time used in this thesis was a compromise between the test duration and the signal to noise ratio.

Frequency range	No of frequencies (10 points per decade)	Estimated duration	Integration time
10,000Hz to 1Hz	40	3m	1.25s
10,000Hz to 0.1Hz	50	6m	1.25s
10,000Hz to 0.01Hz	60	19m	1.25s
10,000Hz to 0.001Hz	70	2h44m	1.25s
10,000Hz to 0.0001Hz	80	26h47m	1.25s
10,000Hz to 0.00001Hz	90	267h32m	1.25s

Table 5-9: Shows the estimated duration of the frequency scan computed by the commercial software, NOVA 1.10.1.

To fulfil the linearity requirement for a valid EIS data, the applied AC perturbation signal has to be small enough not to disturb the system from its steady state. This amplitude depends on the system under investigation. Usually, there is a need for a compromise between minimizing nonlinearity, which exists in most electrochemical systems, and the level of noise that accompanies such a low signal amplitude. Although the amplitude should be small to ensure, at the minimum, a quasi-linearity, it needs to be adequately large to have a measurable response. Typical signal amplitude is between the ranges of 5 to 10mV in SC testing.

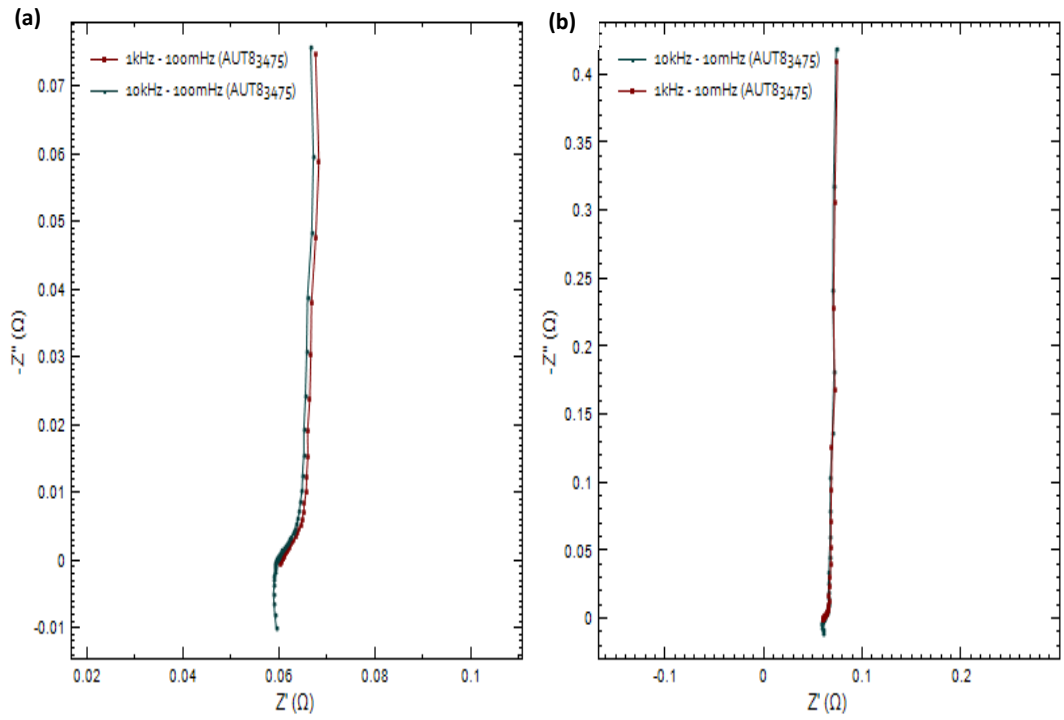


Figure 5-6: Nyquist plot of the SC at four different frequency ranges: (a) data from 1kHz to 100mHz and 10kHz to 100mHz frequency ranges and (b) data from 1kHz to 10mHz and 10kHz to 10mHz frequency ranges

Figure 5-6 displays the Nyquist plots of the four frequency ranges tested in this study: 1kHz - 100mHz, 1kHz - 10mHz, 10kHz - 100mHz and 10kHz - 10mHz. The capacitances are derived in terms of frequency from the expression in Equation (5.16)

$$I = j2\pi fCV \tag{5.15}$$

Where, I and V are the phasor representations of current and voltage.

Since the impedance of capacitance has only the imaginary component, the capacitance can be calculated from the imaginary part of the complex impedance as,

$$C = -\frac{1}{2\pi fImZ} \tag{5.16}$$

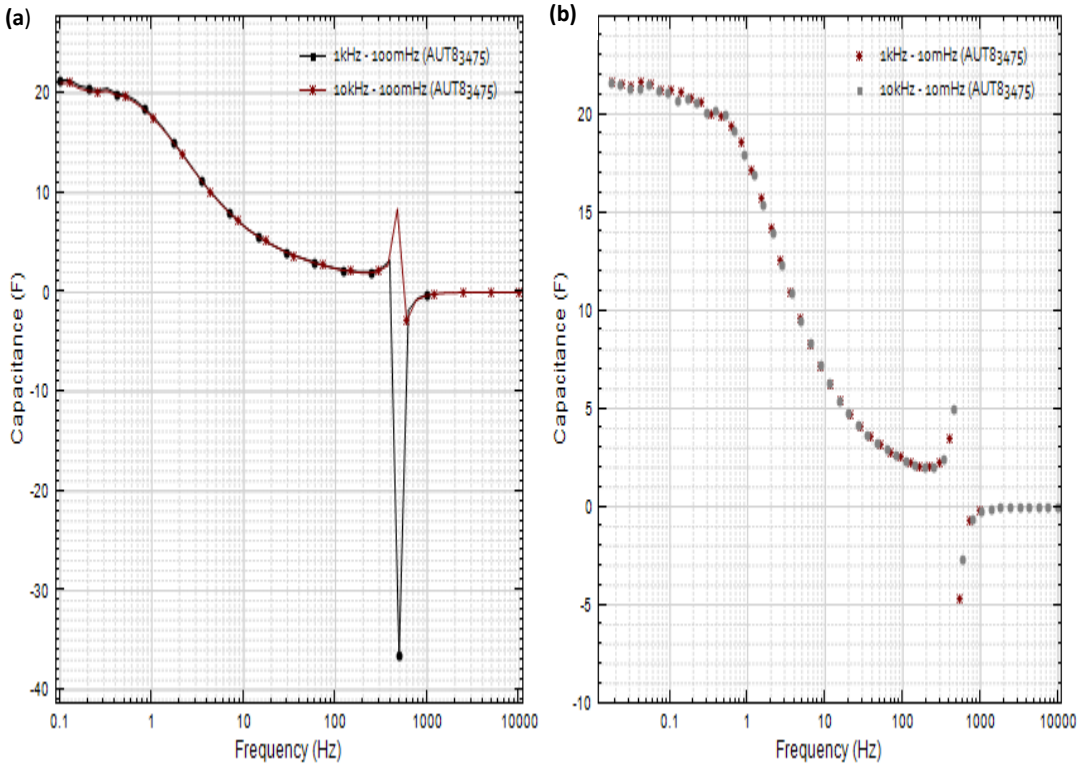


Figure 5-7: Capacitance vs frequency: (a) data from 1kHz to 100mHz and 10kHz to 100mHz frequency ranges and (b) data from 1kHz to 10mHz and 10kHz to 10mHz frequency ranges

Figure 5-7 plots the capacitance of the four frequency ranges as it varies with frequencies. The capacitive part of the data concludes at the point the graph crosses the horizontal origin to the negative vertical, where the inductive part of the system commences as seen in Figure 5.7.

Frequency Range	Capacitance (F)
1kHz to 10mHz	21.7341
1kHz to 100mHz	21.2915
10kHz to 10mHz	21.6848
10kHz to 100mHz	21.0014

Table 5-10: Capacitance values recorded at the lowest frequency

The highest capacitance is recorded at low frequency, as such the capacitor values of the four frequency range is shown in Table 5-10. Frequency range $1kHz$ to $10mHz$ shows the highest measured capacitance with 21.7341F at 10mHz, while the lowest capacitance is measured at the frequency range $10kHz$ to $100mHz$ which gives $21.0014F$ at $100mHz$. This result is expected, as capacitance increases with decreasing frequencies. Moreover, the graph shows a rising trend at low frequencies, whereby it can be assumed that the capacitance will continue to increase if the frequency is lowered even more, although lowering the frequency will affect the duration of the test tremendously as tabulated in Table 5-9. Therefore, there should be a compromise between the accuracy of the data and the duration of the test, particularly in an environment where there is a time constraint.

Consortiums such as IEC 62391 and USABC (Thong, 2011) and most researchers recommend $1\,KHz$ as the frequency standard to measure ac (Martynyuk, Makaryshkin, & Boyko, 1800). Many SC manufacturers like NEC Tokin, Panasonic, RUBYCON, Vishay and NESSCAP, just to list a few, report ac ESR at this frequency in their product datasheets instead of the dc ESR. Whereas, Maxwell only reports the dc ESR; while Tecate and Vina Tech includes both dc ESR and ac ESR in their product datasheets.

Accordingly, the AC ESR from the four frequency ranges tested in this study is given in Table 5-11. There is only a slight difference in the ESR values obtained from the two frequency ranges. Since the difference is so small, it can be said that the frequency ranges tested here do not affect the ESR.

Frequency Range	**ESR_{AC} (at 1kHz)**
1kHz to 10mHz	0.06033
1kHz to 100mHz	0.06030
10kHz to 10mHz	0.05948
10kHz to 100mHz	0.05913

Table 5-11: ESR_{AC} at 1kHz of four frequency ranges, 10 points per decade and AC amplitude of 10mV RMS.

5.3 Supercapacitor Modelling

Before a supercapacitor can be employed in any given application, especially EV/HEV application, it is necessary to study its electrical and thermal behaviors in its operational environment (H. Gualous et al., 2003) and, as such, various literature have developed several R-C electrical models based on those behaviors both in the time domain and frequency domains.

Ideally, EEC model R-C branches should be large, but to simplify and ensure a satisfactory accuracy in the modelling process, a three or two branch is the typical choice of model (Shi & Crow, 2008). The parameters in these R-C branches are usually determined in the time domain by using constant current tests such as Zubieta & Bonert, (2000)'s three-branch model with a range of $30\ mins$ (N Devillers et al.,

2014). A two-branch model describing the thermal behaviour proposed by (H. Gualous et al., 2003). Deliverable D3100.5 also proposed another version of a three-branch model as referenced in Ceraolo, 2013.

The electrical behaviour of a SC, particularly the charge propagation, can also be modelled either with a transmission line model and a non-linear model identified in the frequency domain (N. Bertrand et al., 2010). Identifying the parameters of a transmission line can be done by combining temporal and frequency approaches (Nassim Rizoug et al., 2012), just like most researchers i.e. (Lajnef, Vinassa, Briat, Azzopardi, et al., 2007) (Fletcher et al., 2014) (Rafik et al., 2007) (Lajnef, Vinassa, Azzopardi, Briat, et al., 2004) have resorted to a multi R-C branch model that represents charge distribution during transient periods. Non-linear models, on the other hand, demonstrate SC pore distribution and charge permeability. Hence the non-linear phenomena governing its behaviour only witnessed in the frequency domain for small voltage variations. This non-linear method of model has been explored by various researchers (N. Bertrand et al., 2010) (Dhirde et al., 2010) (Kulsangcharoen et al., 2010) (Wu, Hung, & Hong, 2012b) (Hirschorn et al., 2010) (Buller et al., 2002) to model SC frequency, voltage and temperature behavior with a degree of accuracy.

When selecting an EEC model from the typical types of models (discussed in chapter 2 section 2.3.2) or developing a new SC model, the important features to be taken into consideration (gathered from Gualous et al., 2003, Dănilă, Luchache, & Livint, 2011) are:-

- The model should be as simple as possible and should describe the thermal behaviour of the SC over a range of few minutes with sufficient accuracy.
- The parameters of the model should be determined from suitable measurement methods using either constant current method in time domain or electrochemical impedance spectroscopy in frequency domain
- Capacitance depends on physical parameters of a supercapacitor, so it is not be influenced by temperature.
- When modelling voltage dependence on capacitance a nonlinear component is introduced to the model system (to increase voltage, i.e. the internal electric field attracts more ions and the concentration near the electrode increases).
- Internal resistance ESR increases with decreasing temperature, and twice as much when in a SC bank due to reduced mobility of ions in the electrolyte at low temperatures.
- At higher currents, the voltage fluctuates greatly and cannot accurately determine the effects on capacitance (ions in the electrolyte migrate to the harder surfaces of carbon at low temperatures).
- At the same voltage, at different temperatures, the capacitance varies more in the charging state. The possible explanation is that during the charging cycle, the diffusion and electrical forces are “of rejection” and during the discharge cycle, they are “of attraction”.

5.3.1 Basic Model

A conceptual model adopted from the SC datasheet of EPCOS (Ambade & Joshi, 2014) (Al-janad, Omar, Rasheed, Ibrahim, & Mustapha, 2014) (Dănilă et al., 2011) (Johansson & Johansson, 2008) was selected as the EEC base model. The model in Figure 5-8 consists of standard circuit components, with three resistors and two capacitors (contrary to EPCOS datasheet model, that consisted of two variable nonlinear capacitors instead of the standard ones employed in this thesis and an additional voltage balancing resistance in parallel with the circuit).

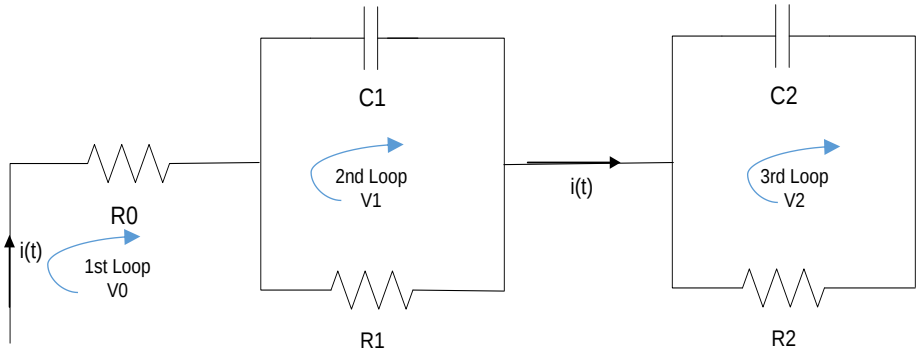


Figure 5-8: Basic Model (inspired by EPCOS datasheet)

The behaviour of the entire circuit depends on capacitance C1 to determine the maximum state of charge of the supercapacitor. The amount of stored energy and the value of energy level variations are determined mainly by the capacitance. Resistance R1, connected in parallel with the capacitor, represents the quantification of self-discharge effect. Resistance R0 represents losses in charge/discharge cycle, as a result of the resistance of the conductor element, and the process is not an ideal one (Yonghua Cheng, 2010). Resistance R2 and capacitance C2 are included in the

circuit to shape the fastest processes in the SC's behaviour (Johansson & Johansson, 2008).

To develop the basic model presented in Figure 5-8, parameters were extracted from experimental measurements of a single SC Maxwell's $25F$ product with a maximum voltage rating of $2.7V$.

This measurement was carried out by charging the SC at a constant current of $2A$ using PGSTAT302N from Metrohm Autolab B.V. (by modelling its time constant), until the voltage reaches it maximum rated voltage ($2.7V$); then the current was cut off for about $3mins$ (as specified in IEC standard). After that a negative current of $-2A$ was applied, in-order to discharge the supercapacitor.

From the experimental results, the parameters of the basic model Figure 5-8 were determined Loop by Loop using calculations presented below:

- **1st Loop**

The value of the series resistance R0 is determined by observing a rapid change in charging current and measuring the first voltage drop. This voltage drop has a steeper inclination than the drop that occurs right after because of the supercapacitor self-discharge. The value of R0 is calculated using the voltage drop that occurs right after the current is cut off using the following equations:

$$R0 = \frac{\Delta u}{\Delta i} \tag{5.17}$$

From measurement points selected, the value was calculated to be;

$R0 = 65.86m\Omega$

- **2nd Loop**

The capacitance value can be calculated in two different ways. The first method is to look at the voltage derivative during a charging state of the SC. The relation between voltage derivative and the capacitance is:

$$i(t) = C\frac{d}{dt}u(t) \tag{5.18}$$

Using the relation, the capacitance can be calculated from different parts of the voltage curve. When high currents are used, effects other than the capacitance can affect the voltage level. These effects can cause the calculated capacitance value to be incorrect.

$$Q = \int i(t)\,dt \tag{5.19}$$

Therefore, the capacitance (C) is

$$C = \frac{\Delta Q}{\Delta \mathrm{u}} \tag{5.20}$$

Where, $i(t)$ is the charging current, C is the capacitance, Q the charge and u the voltage.

Since the energy level can be calculated using only one value on the voltage, only two points on the voltage curve are needed to be able to calculate the energy storage capability. Using Equation (5.20) capacitance was calculated, with data gathered from the experimental measurement, to be:

$C1 = 25.204199F$

Since the self-discharge at this stage is low, the value of R1 resistance is hard to acquire from the measurement analysis. A slow discharge means that the resistance value must be high, but according to our measurements, the self-discharge is not very slow. The conclusion from observed results was that the value was likely to be high,

so there was a need to bring this down, by qualitative testing of these parameter alterations to fit the curve shape of the voltage received from the SC model. A starting value of 200Ω was estimated in order to model the EEC.

- **3rd Loop**

This value is chosen to be the one thirteenth of C1 (Johansson & Johansson, 2008), The capacitance C2 illustrates the influence of the voltage in the total capacitance of SC. The impact of the C2 component in the model is very small, which means that a change in its value does not impact model accuracy much. The value for C2 is:

$$C2 = \frac{C1}{13} = \frac{25.204199}{13} = 1.938F$$

Similar to R1, resistance R2 cannot be determined by looking at measurement data because its effect on the waveform is not visible enough. Hence, an estimated value of $10m\Omega$ was proposed as a starting point, till when the value can be tuned to fit the experimental waveform during simulation.

5.3.1.1 Basic Model Simulations

Simulating the basic model in Figure 5-8, a voltage equation representing the EEC model in loops was defined and transformed into block diagrams in Simulink (Matlab).

$$V_{SC} = V_0 + Z \times I + ESR \times I \quad (5.21)$$

Where, V_{SC} = supercapacitor voltage, V_O = initial supercapacitor voltage (set at 0V during simulation), Z = SC impedance, internal resistance ESR = E_Ω + E_P (series and parallel resistance)

With Equation (5-21) in mind, V_{SC} was redefined to develop a Simulink model using derivative block diagrams to express the voltage response in terms of input current I

$$V_{SC} = V_1 + V_2 + V_3 + (I \times ESR(R_\Omega)) \quad (5.22)$$

1st Loop

$V_0 = V_{R0} = i(t) \times R_0$

2nd loop	**3rd loop**
$V_1 = V_{C1} = V_{R1}$	$V_2 = V_{C2} = V_{R2}$
$i(t) = I_{C1} + I_{R1}$	$i(t) = I_{C2} + I_{R2}$
$I_{R1} = \frac{1}{R_2} V_1$	$I_{R2} = \frac{1}{R_2} V_2$
$I_{C1} = C_1 \frac{dV_1}{dt}$	$I_{C2} = C_2 \frac{dV_2}{dt}$
$i(t) = \frac{1}{R_1} V_1 + C_1 \frac{dV_1}{dt}$	$i(t) = \frac{1}{R_2} V_2 + C_2 \frac{dV_2}{dt}$
$\frac{1}{C_1} i(t) = \frac{1}{R_1 C_1} V_2 + \frac{dV_1}{dt}$	$\frac{1}{C_2} i(t) = \frac{1}{R_2 C_2} V_2 + \frac{dV_2}{dt}$
$\boldsymbol{\frac{dV_1}{dt} = \frac{1}{C_1} [\, i(t) - \frac{1}{R_1} V_1 \,]}$	$\boldsymbol{\frac{dV_2}{dt} = \frac{1}{C_2} [\, i(t) - \frac{1}{R_2} V_2 \,]}$

Equations derived at each voltage loop of Figure 5-8 using differentiation as expressed above as Equations (5.22a).

Equations (5.22a) expresses the derivative of the basic model in the time domain, and the combination of Equations (5.22a) expressing it as Equation (5-22) was used to develop a Simulink block diagram. The Simulink model of the basic circuit for the SC, with the calculated values of the components previously computed, is subjected to a

simulation test. The simulation time was set at $360sec$, while the model was subjected to a simulation process that reproduced the 6 step process voltage response specified in Maxwell's preferred method of SC characterization, using Maxwell's current profile as the input source presented in Figure 5.9.

After all the blocks in the basic model were connected correctly, they were assigned values according to parameters extracted from the measurement data and simulated under $360secs$ with an $ode45s$ solver. The simulation response of SC basic EEC model was compared to the experimental voltage response, so as to fit the simulated response to the experimental response, by altering the model's component values one at a time, till the simulation response that best fitted the voltage experimental response was achieved as shown in Figure 5-9. The component values recorded after the final simulation were compared to their actual values and presented in Table 5-12. No mathematical method was used to find the most appropriate values, only qualitative testing by individual parameter alterations.

Components	**R0 (mΩ)**	**C1 (F)**	**R1 (Ω)**	**C2 (F)**	**R2 (mΩ)**
Calculate/Estimated value	65.86	25.204	200	1.938	10
Simulated Values	63.00	27.266	400	1.938	12.423

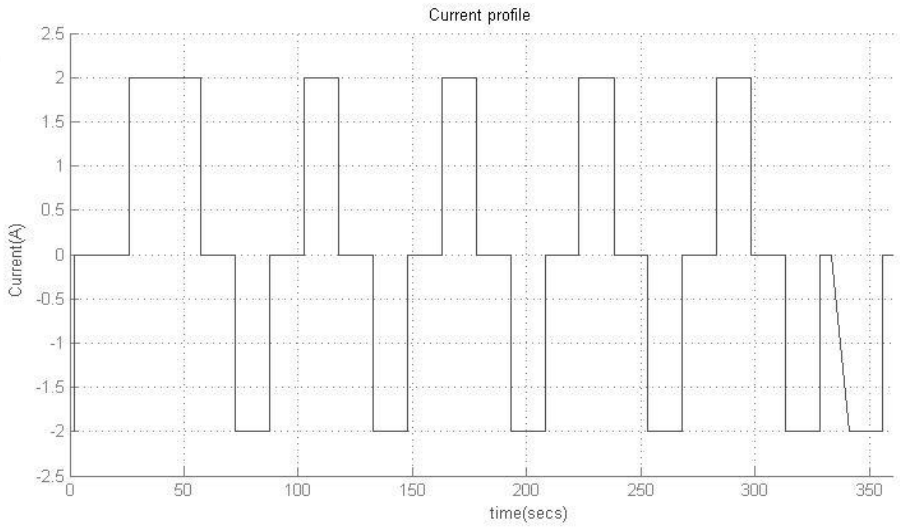
Table 5-12: Measured and Simulated component values of the basic model

5.3.1.2 Basic Model Validation in Time domain

The basic model was validated in the time domain with voltage profile presented in Figure 5-9. Figure 5-9 voltage profile shows the voltage profile of both the experimental and simulation results, and even though the voltage profiles in its

totality looks similar, there were areas in the simulation profile that did not fit in perfectly with the experimental profile. Differences in responses circled at areas A, B, C, and D shown in Figure 5-9, raised some concerns in model choice. Voltage irregularities observed between experimental data and Basic model at area A, and D (that is the beginning and end of the voltage response) are as a result of the initial integrator value of 0.2 selected in the Simulink model to successfully simulate the basic model. The error observed at C is assumed to be as a result of the voltage dependence omitted from the capacitor C1 of the basic model. In theory, the first R-C branch in a model represents the charge/discharge phenomena in SC (N Devillers et al., 2014), therefore modelling the inaccurate area of C. The lack of a voltage dependent capacitor C1 is observed at areas C and B, but more prominently at area B which requires a non-linear capacitor, which is best modelled in the frequency spectrum (N Devillers et al., 2014). The second branch comprising of R2 and C2 takes into account the influence of the voltage on the capacitance and the slow phenomena such as charge redistribution and self-discharge. These representations illustrate the simulation modelled inaccuracies of area B. At B, the simulation profile observes a longer voltage drop than the experimental results and also a more linear voltage drop due to self-discharge (during the open-voltage mode) than the experimental profile. At this point, it is safe to say the basic model is not satisfactory enough and therefore it needs to be developed to satisfy EV/HEV applications that can model voltage, temperature influences. As such, a non-linear model validated in both frequency and time domain is a smart choice with the simplistic arrangement as the basic model is the way forward.

(a)



(b)

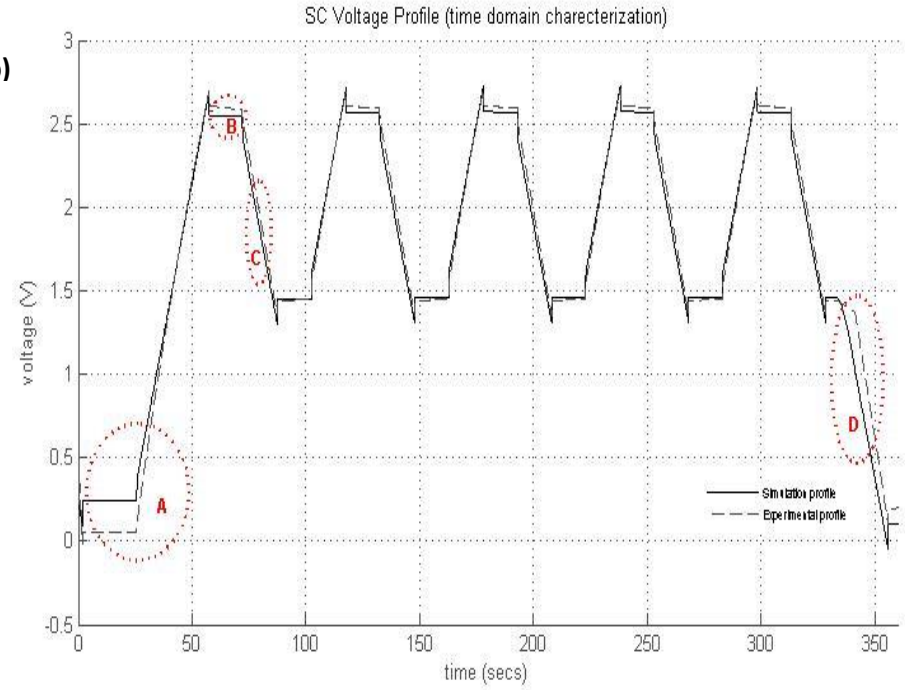


Figure 5-9: SC (a) Current and (b) Voltage profile representation in the time domain

5.3.2 Proposed Model

The impedance responses of SC were measured using the PGSTAT302N from Metrohm Autolab B.V. This impedance spectrum in the form of a Nyquist plot would be used to develop the proposed model in the form of a fitted EEC using complex

least squares (CNLS) to obtain accurate values for the circuit components. The proposed EEC model would use the same R-C arrangement as the basic model in section 5.3.1, so as to focus and limit the CNLS fittings rather than broadening the model to a trial and error arrangement. There are so many EEC models developed by various researchers, so when selecting one, it is smart to choose a type based on the intended application and develop it using linear or non-linear components. This process is carried out on a commercial software Nova 1.10 under the frequency range between $10kHz$ to $100mHz$ with $10mV\ AC$ amplitude signal. Impedance response would not be sufficient enough to validate the authenticity of an EEC model, as many circuit combinations could also result in such similar response; therefore caution would have to be taken when analyzing the fit based on the chi-square, x^2 to indicate whether the simulated response is a good fit to the data, and the estimated errors for each individual circuit component are also used to evaluate the significance of this component to the EEC. In addition to these precautions, validation in the time domain using Maxwell's 6 step process voltage profile is also carried out.

5.3.2.1 Impedance Modelling

The modelling of the impedance spectrum was done by sectioning the Nyquist plot into three frequency regions and modelling each part separately as shown in Figure 5-10. Classified as; (1) High Frequency ($< 500Hz$), (2) Medium Frequency ($1Hz - 500Hz$), (3) Low Frequency ($> 500Hz$). It should be noted however, that the frequency regions specified above are only applicable to the Impedance spectrum

provided in Figure 5-10, which was based on test specifications and the particular SC product used for testing.

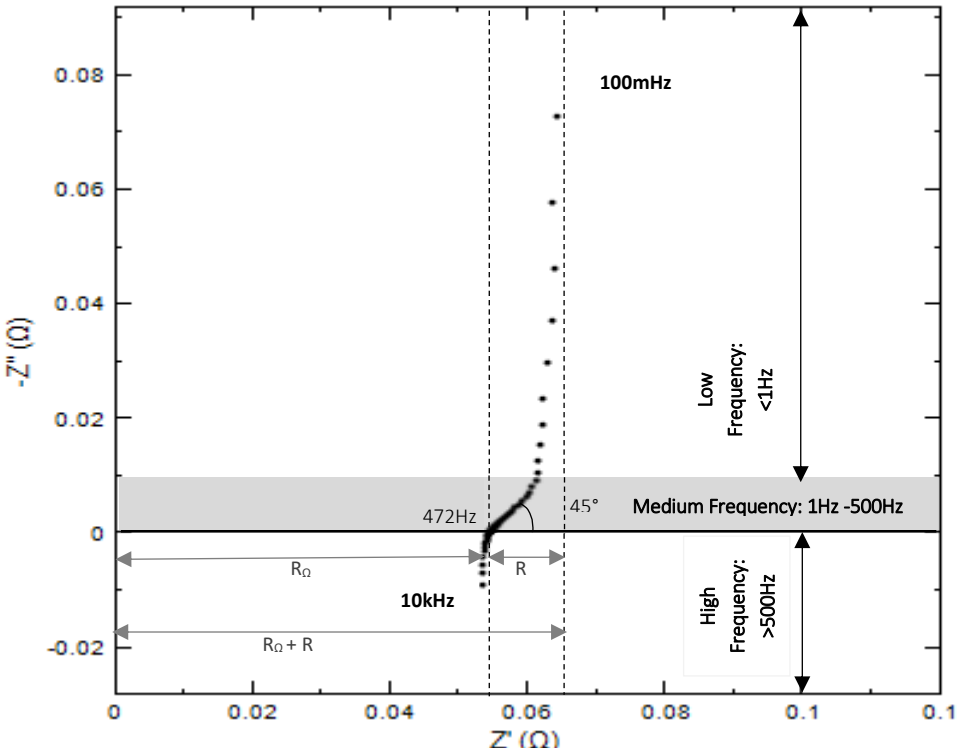


Figure 5-10: Nyquist plot of impedance spectrum for a SC's initial response at 0 DC bias and 10mV ac amplitude, divided into three frequency regions from 100mHz to 10KHz:

I. High-Frequency region ($500Hz - 10kHz$)

The intercept of the impedance with the real axis at $472Hz$ is referred to as the ohmic resistance (also known as ESR) and is represented by a series resistance, R_Ω (Shown in Figure 5-10). The ohmic resistance originates from the contributions of the cell leakage resistance varying from the electronic resistance of the electrode material and thickness, the contact resistance at the current collector, current collector, the electrolyte including the separator, and other contact resistance. (N Devillers et al.,

2014) (Masarapu et al., 2009) (Stoller & Ruoff, 2010b) (H. Gualous et al., 2003). As shown in Figure 5-10, the Nyquist plot is shifted by an amount of R_{Ω}.

The imaginary part of the high-frequency region models the inductive behaviour of the SC. However in this research work, the inductive behaviour of the spectrum is so small (almost negligible) that it was thought wise to ignore it during the development of the EEC model. Nevertheless, the inductive line has been attributed to the external artefacts such as external wiring and measurement system, and also due to the wounded technology of the SC cylindrical cell (Lajnef, Vinassa, Azzopardi, Briat, et al., 2004).

II. Medium-Frequency Region (1Hz – 500Hz)

The medium frequency range, where a $45°$ line inclines at the real part, is referred to as Warburg region (Quintana et al., 2006) (Del Toro Garcia, Roncero-Sanchez, Parreno, & Feliu, 2010). The Warburg region is a consequence of the distributed resistance/capacitance in a porous electrode (Pintelon & Schoukens, 2012), theoretically describing the DeLevie transmission line model of a porous electrode with straight pores considered as cylindrical capillaries (Ko & Carlen, 2000).The Warburg region exhibits a fractional behaviour at this point where the SC transitions from an inductive behaviour to capacitive behaviour, therefore this region is governed by a capacitor (that models the distributed capacitors inside the pore) and a resistor (equivalent distributed resistance). The semicircle (observed in the region) can be generated with a parallel combination of resistor and capacitor. However, since the semicircle is depressed below the Z' axis, it is not plausible to simply use a

capacitor to model this region. As it has been shown in García, Roncero-sánchez, Parreño, & Feliu, 2010, Dzieliński, Sarwas, & Sierociuk, 2011, Quintana et al., 2006, this region is better characterized by a fractional-order integrator.

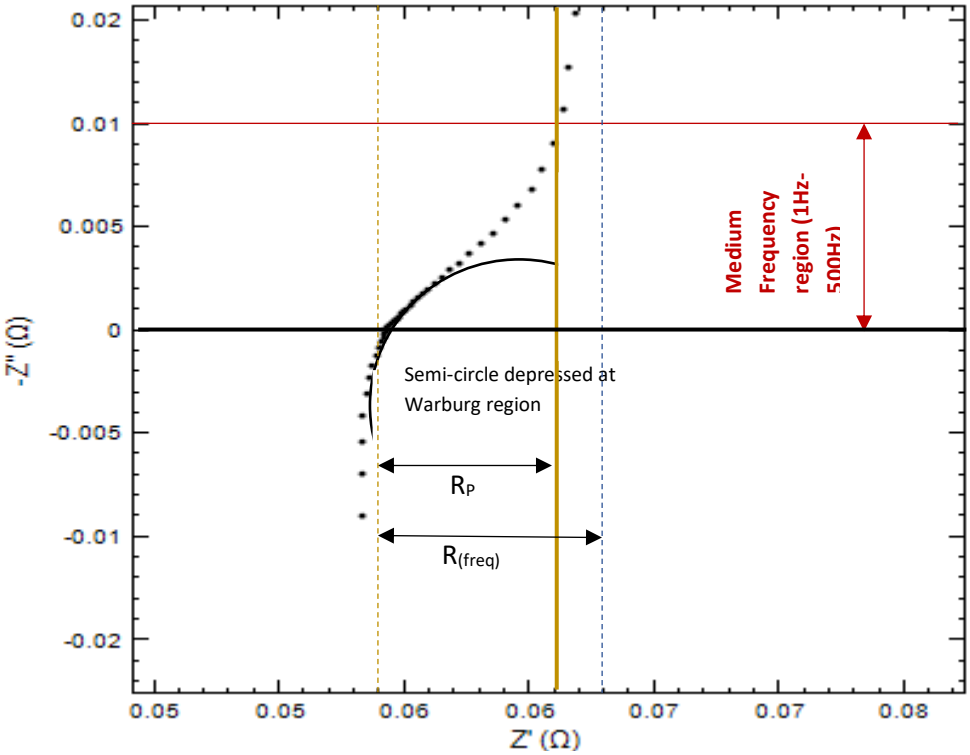


Figure 5-11: A more pronounced view of the impedance spectrum in the medium frequency range with emphasis on the depressed semi-circle in the Warburg region (from the vertical intercept of the high frequency (dotted yellow line) to the vertical intercept of the medium frequency (solid yellow line) and contact resistance R_p

When modelling the imaginary part of the medium frequency region, an ideal capacitor modelled at a $90°$ phase angle to the real axis could not be used, as a $45°$ line (considered to be part of an arc depressed below the Z' axis (see Figure 5-11)) is generated at the impedance spectrum, thereby replacing the capacitor with a CPE with a fractional exponent n (of approximately 0.5) in the EEC.

The resistance R_P is the sum of the contact resistor at the current collector R_c and the electronic resistance of the electrodes R_e, modelling the distributed resistance at

the medium frequency. In the medium region, the real part as shown in Figure 5-11 models the equivalent distributed resistance in the SC pore structure R_P, which is determined by the diameter of the arc on the real axis from the vertical intercept of the high frequency to the vertical intercept of the medium frequency (see Figure 5-11).

The angle of depression of the semicircle can be accounted by the exponent n of the CPE term. When n is close to 1, the CPE behaves like a capacitor, although the phase angle is not 90°. Therefore, a resistor in parallel with a CPE having n equals to 1 will produce a semicircle that equals to that of a resistor in parallel to a capacitor. As n decreases, the semicircle is pushed below the Z' axis, as illustrated in Figure 5-12.

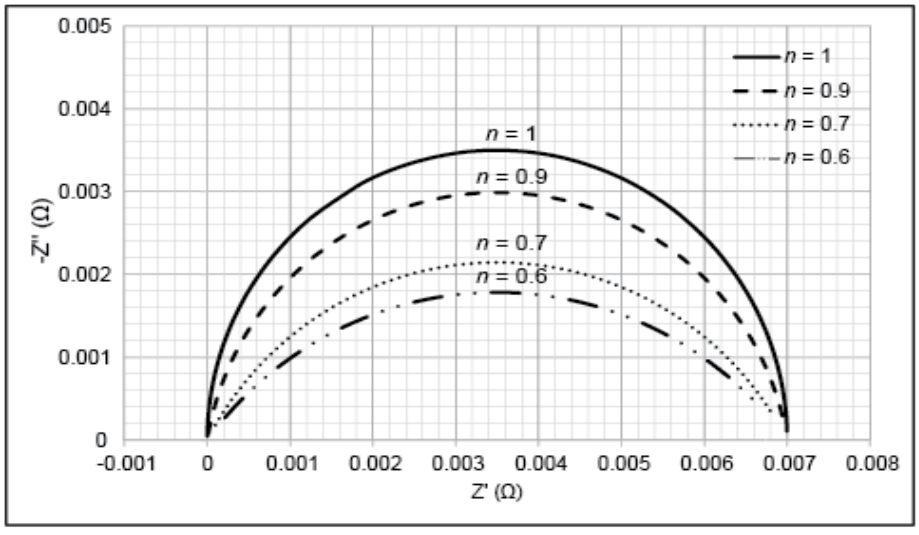


Figure 5-12: Nyquist plot of a resistor in parallel with a CPE used to model the Warburg region with various values of n. The CPE fractional exponent n, reflects the angle of the semicircle. Adopted from (Naim, 2015)

III. Low-Frequency Region ($1Hz - 100mHz$)

At low frequencies, the impedance spectrum is capacitive, and it is denoted by an inclined-vertical slope to the imaginary plane, which almost resembles the behaviour of an ideal capacitor of a straight line (as seen in Figure 5-10). This inclined- vertical slope describes the frequency dispersion of capacitance behavior or the distributed characteristic, as referred to in Song, Jung, Lee, & Dao, (1999), which occurs during electrochemical charging processes, and may be as a result of distribution in macroscopic path lengths, (non-uniform active layer thickness) (Mathias & Haas, 1993) or distribution in microscopic charge transfer rates (Scher & Lax, 1973), absorption processes, or surface roughness (Ko & Carlen, 2000). With the imaginary part of the spectrum in this region mainly capacitive, it shows that the capacitance of a SC is frequency dependent, and the highest capacitance can be achieved at the lowest frequency. This observation, therefore, prevents modelling the region with just a capacitor. Instead, what is needed is a model that can describe the capacitive dispersion effect, with a parallel combination of a capacitor with a resistor.

The real part in this region is modelled with a resistor R which comprises of the electronic resistance of the electrodes R_e, the contact resistance at the current collectors R_c and the ionic resistance of the electrolyte R_i. The resistor R is therefore equivalent to the sum of $R_e + R_c + R_{i(Freq)}$, with the ionic resistance R_i dependent on frequency (N Devillers et al., 2014).

Combining a capacitor C in parallel with resistor R creates an inclined vertical line replicating the SC impedance spectrum at low frequencies and modelling the capacitive dispersion in this region.

IV. Model Simulation

The EEC model was developed using Complex nonlinear least squares (CNLS) to fit the SC EIS experimental data. The model parameters were first selected and arranged accordingly, with a rough estimate of the start value for each circuit component in the analysis window of Nova 1.10. The application then modified the parameter values in the model until a satisfactory fit is achieved, verified by a simulation of the Nyquist plot.

Impedance modelling, as explained above was modelled within frequency regions, in which the experimental data of the Nyquist plot helped in determining rough estimates of the EEC imaginary and real parameters at each region, which were later adjusted by the CNLS tool to fit the experimental data. The developed EEC model was then remodelled and simulated under the frequency range between $500Hz$ to $100mHz$ with a $10mV$ AC amplitude signal so as to eliminate the inductive part of the model, as observed in the high frequency region (section 5.3.2.1I). Figure 5-13 compares the impedance experimental results to the simulated results of the proposed EEC model. The proposed EEC model with parameter values (shown in Table 5-13) was then generated and presented in Figure 5-14. Nova 1.10 also provided estimated error percentage of each parameter value which represented the margin of confidence of the calculated value of the component (Autolab, n.d.) also presented in table 5-13.

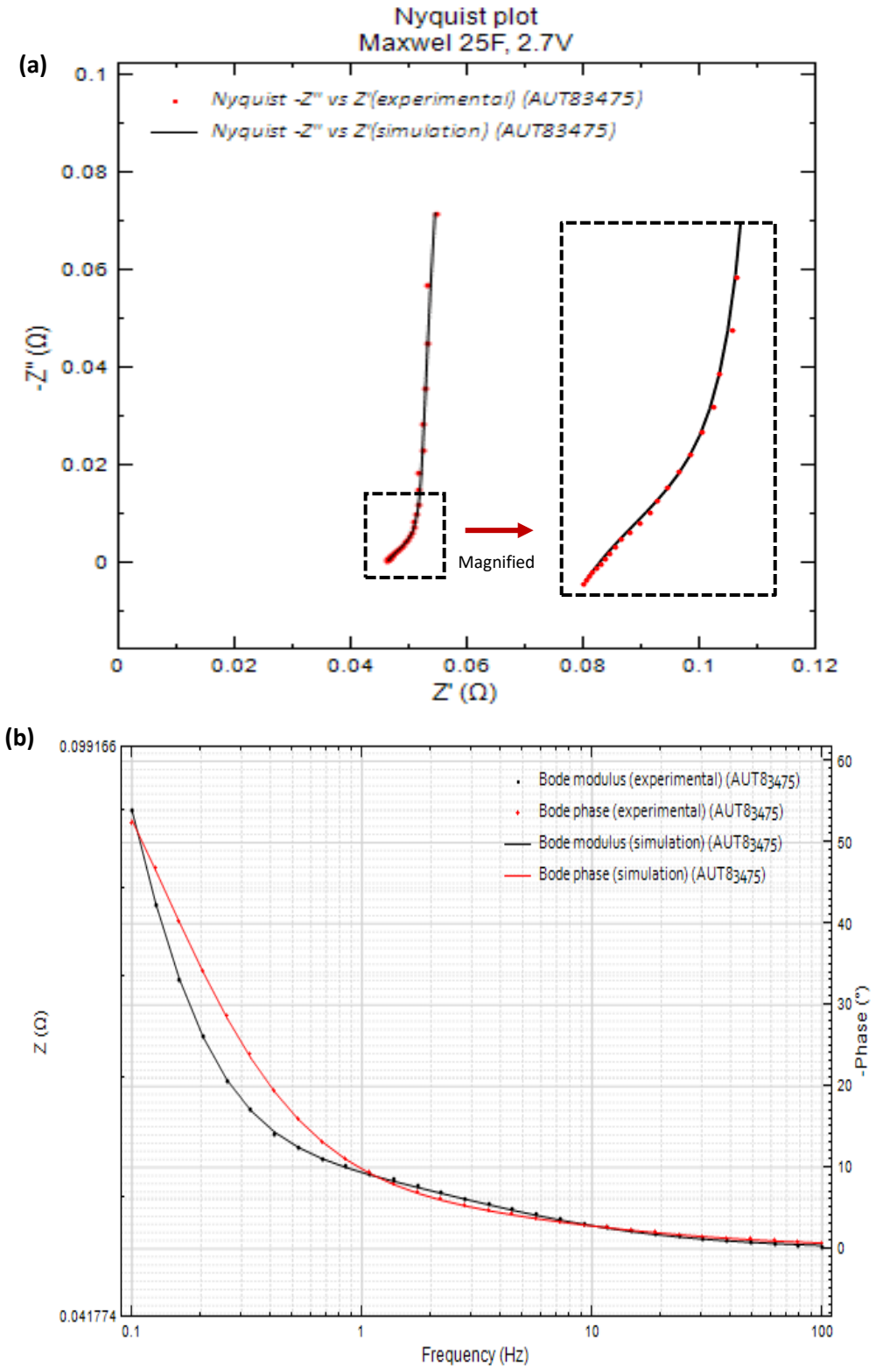


Figure 5-13: Experimental and simulation results of the proposed EEC model (between 500Hz to 100mHz): (a) Nyquist plot with a magnified view of the Warburg region and (b) Bode phase and modulus plot

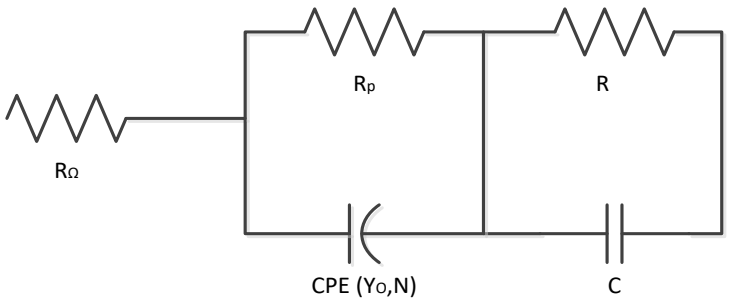


Figure 5-14: Proposed EEC SC model

To further measure the fitness of the EEC model to SC experimental data, chi-square value, x^2 is also used to analyse if the fitting is good. in this work a chi-square value ranging from 10^{-1} to 10^{-4} is often observed, although in some reported work like Dhirde et al.,(2010), the chi-square value can be as low as 10^{-6}. This is because, even though the model will look correct in form, the extra term or component will make the fitting more flexible than it should be and hence, CNLS attempts to describe the variation in the data, which may be due to a measurement error in some electrochemical process.

Components	[R(CPE/R)(C/R)] Proposed Model					
	R_Ω(mΩ)	R_P(mΩ)	R(Ω)	Y_O(Mho)	N	C(F)
Values	60.2	6.73	2.82	19.2	0.645	22.3
Error (%)	0.20%	3.61%	15.56%	6.85%	3.47%	0.28%
X_2	2.3102×10^4					

Table 5-13: Proposed EEC model's component values with each percentage error

The proposed model is represented in an impedance form as shown in Equation (5.23)

$$Z = R_{\Omega} + Z_{wargurb\ region} + \frac{R}{1+RC} \quad (5.23)$$

The Warburg region can be described mathematically in the impedance form (Raistrick, Franceschetti, & Macdonald, 2005) as:

$$Z_{warburg\ region} = \frac{R_p}{1+Y_o R(jw)^n} \quad (5.24)$$

Where, R_p is the medium frequency intercept at real axis and $0 \leq n \leq 1$.

$$Z_{warburg\ region} = \frac{R_p}{1+Y_o R(jw)^n} \quad (5.25)$$

$$Z_{warburg\ region} = R_p + \frac{1}{Z_{CPE}} \quad (5.26)$$

CPE can be expressed as a capacitor using Equation (5.27);

$$C = Y_o {w_c}^{n-1} \quad (5.27)$$

The derivation of Equation (5.23) by C.H. Hsu and F. Mansfeld (Hsu & Mansfeld, 2001) was based on the fact that Z' is independent of n at w_c, which is also independent of n (Qin, 1887).

Derived from Equation (5.28)

$$Z_C = Z_{CPE} = \frac{1}{Y_o(jw_c)^n} = \frac{1}{jw_c C} \quad (5.284)$$

However in the case of normal distribution, the distributed time constant $R_p\,C_p$ at the Warburg region (medium frequency) is derived by;

$$w_c = \frac{1}{\tau} = \frac{1}{R_p\,C_p} \tag{5.29}$$

Where, C_p is the equivalent capacitance at the Warburg region and w_c is the resonance frequency at which $-Z''$ is maximum at the cutoff frequency, where energy entering the system gets reflected instead of transmitted.

The equivalent capacitance C_p can be expressed in terms of the time constant $R_p\,C_p$ at the medium frequency range

$$C_p = Y_o(\frac{1}{R_p\,C_p})^{n-1} \tag{5.30}$$

$$C_p = Y_0(R_pC_p)^{1-n} \tag{5.31}$$

$$C_p{}^n = Y_oR_p{}^{(1-n)} \tag{5.32}$$

$$C_p = Y_o{}^{\frac{1}{n}}\,R_p{}^{(1-n)\frac{1}{n}} \tag{5.33}$$

Equation (5.33) derivation is equivalent to the admittance representation of CPE presented by Brug et al. (Brug, Eeden, Sluyters-Rehbach, & Sluyters, 1984) for a blocking electrode, and the derivation of both Burgs and Mansfield conversion of CPE to capacitance presented in (Hirschorn et al., 2010).

However, it should be noted that to convert CPE to a capacitor using either the Burg conversion method or the Mansfield conversion method the exponent n must be in the range of 0.8-1 (Qin, 1887). Therefore with a lower range it is better to use the impedance functionZ_{CPE}. The EEC model can be expressed as an impedance function, as follows:

$$Z = R_{\Omega} + \frac{R_p}{1+Y_o R(jw)^n} + \frac{R}{1+RC} \quad (5.34)$$

5.3.3 Model Validation in Frequency and Time Domains

The basic model was modelled in the time domain using time constants derived from the constant current test while; the EEC proposed model was modelled in the frequency domain using the impedance spectrum to develop the circuit by describing each frequency region with an electrical parameter.

Given that the basic model and the EEC proposed model were created in separate domains, to make a suitable and calculated choice, it is necessary to validate each model in both frequency and time domains.

Figure 5-15 shows frequency simulations of both the basic model and the EEC proposed model. The EEC proposed model was developed in the frequency domain, so the simulation was straight forward, but to simulate the basic model in the frequency domain, the CNSL tool which was used, modified the model parameter values from the original values as presented in Table 5-12. The best impedance fit the basic model could achieve using the refined values was overemphasized by a chi-square value x^2 of 2.311×10^3.

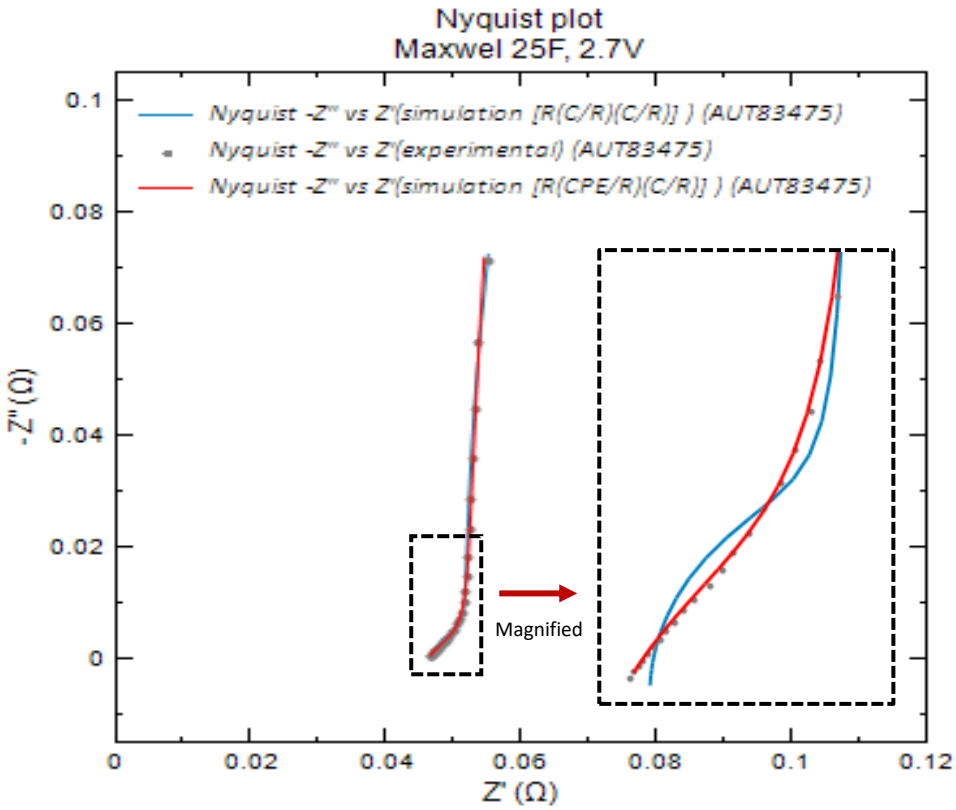


Figure 5-15: Nyquist plot with the proposed EEC model simulated (to a suitable fit to the experimental data in black dotted lines) with the red-line and the Basic model simulated (to an unsatisfactory fit to the experimental data in black dotted lines) with the blue-line

The Basic model developed in the time domain was simulated in Simulink using differentiation as shown in section 5.3.1. The EEC model, on the other hand, was also simulated in MATLAB/SIMULINK with a FOMCON toolbox, developed by Tepljakov, Petlenkov, & Belikov, 2011a. The FOMCON toolbox is an extension of the MATLAB class FOTF, which was previously developed by Chen & Petras, (2009). Due to non-linearity of the model, the fractional-order term of the EEC model was adopted and presented in the form of a Laplace transform with zero initial condition. The fractional-order transfer function (FOTF) can, therefore, be obtained as follows:

$$G(s) = \frac{Y(s)}{X(s)} = \frac{b_m s^{\beta_m} + \cdots + b_1 s^{\beta_1} + b_0 s^{\beta_0}}{a_n s^{\alpha_n} + \cdots + a_1 s^{\alpha_1} + a_0 s^{\alpha_0}} \qquad (5.35)$$

Moreover, the transfer function (FOTF) of the EEC proposed model is derived using Equation (5.34):

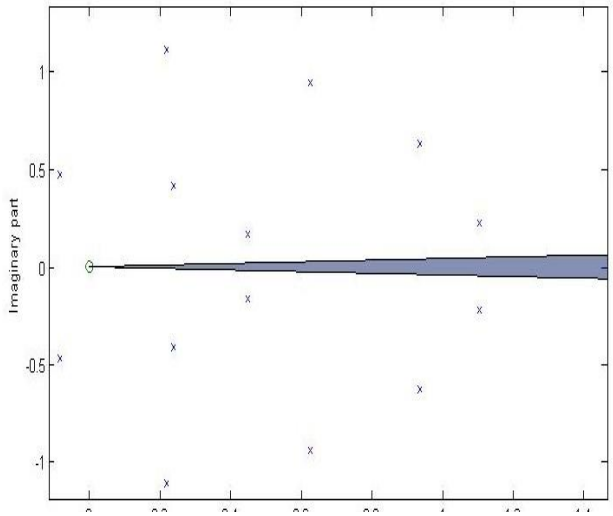
$$Z(s) = \frac{0.52854s^{1.645}+5.24738s+0.17624s^{0.645}+4.007}{15.92251s^{1.645}+102.224s+0.12922s^{0.645}+0.05} \quad (5.36)$$

For a stable function, The FOTF function (Equation (3.36)) has to satisfy the Matignon's stability theorem (Chen & Petras, 2009),

$$\left|\arg\left(eig\ (A)\right)\right| > q\frac{\pi}{2} \quad (5.37)$$

Where, $0 < q < 1$ and $eig\ (A)$ is the eigenvalues of matrix A (Tepljakov, Petlenkov, & Belikov, 2011b). The following condition can be tested using the FOTF viewer toolbox GUI.

The stability function K shows whether a system is stable, with 1 for a stable system and 0 for an unstable system (Chen & Petras, 2009). The result obtained shows that K = 1, thus, the system appears stable with order $q = 0.04$. The results from the stability test are shown in Figure 5.16. The figure shows no poles inside the shaded area, reassuring the stability of the impedance model.



Impedance model Stability Test	
K	1
q	0.0400
ERROR	8.8816×10^{-5}
APOL	0.1963

Figure 5-16: Stability model analysis of LTI (Linear Time-invariant) fractional order systems with tabulated results

The time response of the EEC proposed model was obtained from MATLAB/SIMULINK, using fractional transfer function block-set provided in FOMCON SIMULINK library with a 2A charge current experimental results as shown in Figure 5-9a. The model appeared to be stiff. Therefore, an ode15s invariable-step solver was used in the simulation to ensure fast, efficient and accurate simulation (Tepljakov et al., 2011a).Similar to the Basic model Figure 5-8, the EEC proposed model respond in the time domain with a sequential charge-discharge and an open-circuit response in between.

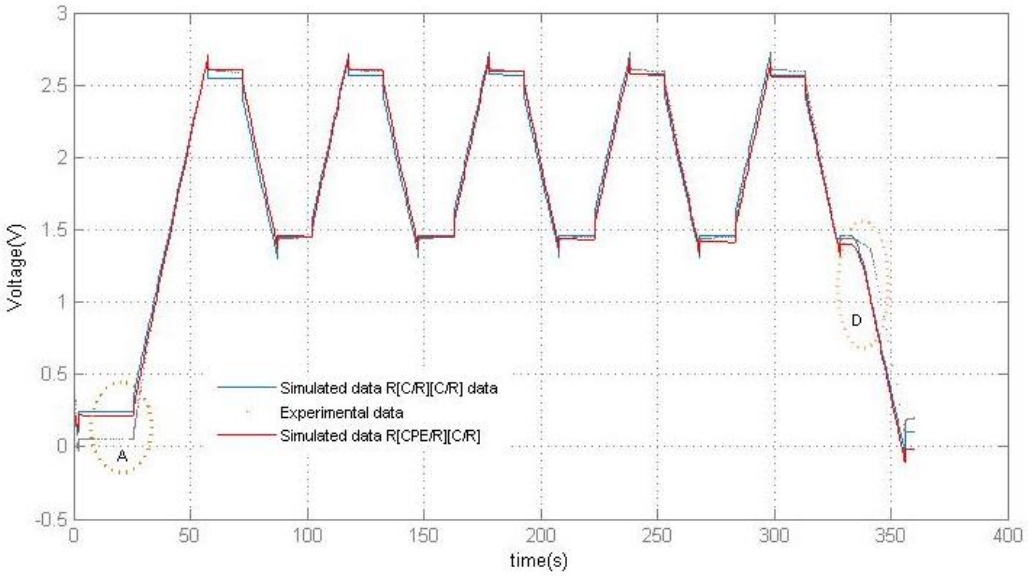


Figure 5-17: Voltage Maxwell 6 process response in time domain of *both Basic model and EEC proposed* model against the experimental results (dotted lines)

Figure 5-17 compares the voltage responses of the basic model with the ECC proposed model against the experimental results. Ideally, the two simulation results seems to observe a similar response to the experimental results, with an exception at areas A and D. As explained in section 5.3.1.2, both the simulated basic model (R[C/R][C/R]) and EEC proposed model (R[CPE/R][C/R]) showed voltage irregularities at the beginning and end of the voltage response, denoted by the presence of a 0.2

initial value in both Simulink block models to initiate successful simulation of both models

However, during the open circuit response after each charge and discharge cycle, the basic model failed to address the non-linear voltage response at the open circuit, instead lengthening the voltage drop below both the experimental results and the EEC proposed simulated model, as magnified in Figure 5-18.

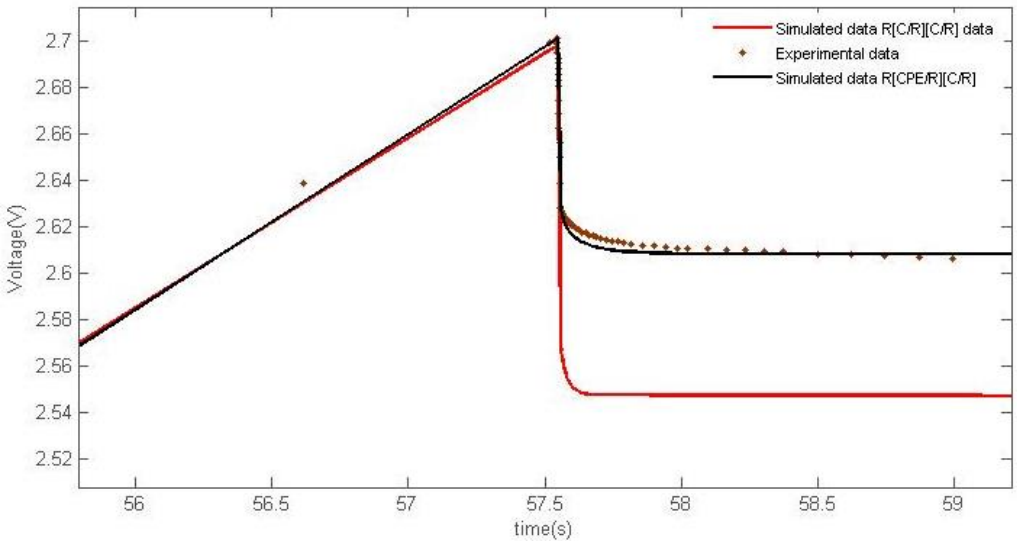


Figure 5-18: Magnified voltage response of both Basic model and EEC proposed model against the experimental results (dotted lines) at the beginning of the open-circuit response

The cause of the voltage decay in SC transient response is as a result of a phenomenon called asynchronous charging denoted by an inclined-vertical slope to the imaginary plane at the low-frequency region (Fletcher et al., 2013). This response is represented by the parallel combination of capacitance C and R in the EEC proposed model. However, according to Fletcher et al., 2013, the capacitor parameter C representation of the low frequency needs to be replaced with a CPE to reflect the open circuit voltage decay in SCs by adjusting the value of the fractional exponent as shown in Figure 5-19. With the exponent n = 1, no voltage decay is

observed upon the current turn-off. As n gets smaller, the decay is larger, and the slope decreases.

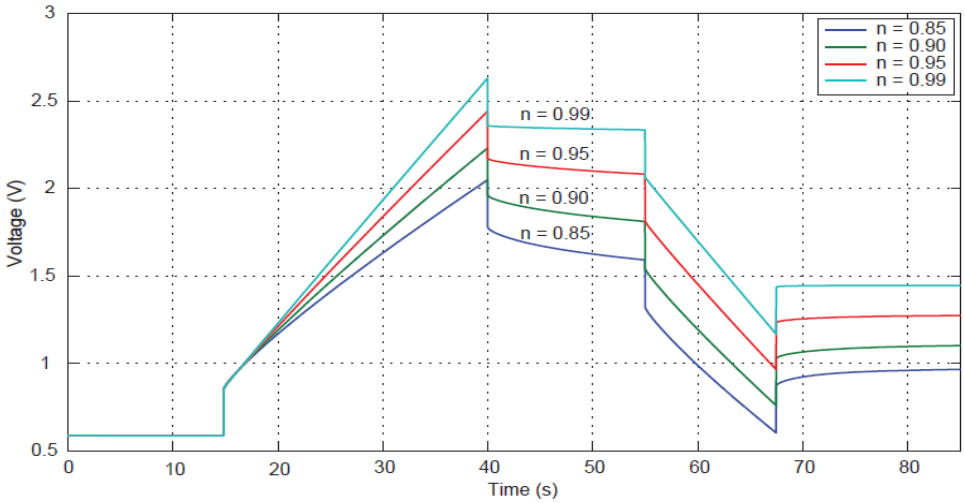


Figure 5-1: The influence of the series CPE exponent, n on the voltage decay adopted from (Naim, 2015)

The EEC proposed voltage response give a more satisfactory simulation result with a root mean square error (RMSE) value of 0.0509 than that of the basic model with an RMSE value 0.0927, calculated using Equation (5.38). Although the RMSE values of the EEC proposed model and the basic model seem small, the frequency and voltage response of the EEC proposed model simulate a more satisfactory result to the experimental data than the basic model, thus, proving to be the more suitable choice of SC model to represent the SC in real-time.

$$RMSE = \sqrt{\frac{\sum(experimental\ data - simulated\ data)^2}{N}} \qquad (5.38)$$

Where N is the total number of simulated data points.

5.4 Summary

Characterization tests in the form of EIS, CC, and CV measurement methods were carried out to compare SC capacitance and ESR results using manufacturer's specifications under certain conditions. In summary, the results reported constant current test (CC); as the method that yielded the highest capacitance, irrespective of the method in which it was carried out, followed by the cyclic voltammetry test (CV); while the EIS test gave the lowest capacitance among all. It was also obvious that the results of the DC measurements (that is the constant current method) including the standard tests attained capacitance values higher than the $25F$ specified by the manufacturer; with the Maxwell's 6 process method being the closest at $26.27857F$ (refer to Table 5-6). Whereas, the AC measurements (carried out in the cyclic voltammetry test (CV) and EIS test) yield capacitance values lower than the manufacture's specification with CV test at 30mVs^{-1} recording the highest capacitance of $24.8595F$. ESR value, on the other hand, varied in all three methods with the most suitable method (close to the manufactures specification $42m\Omega$) recorded by the Constant current tests and Maxwell's 6 process method.

The second aspect of the chapter used the characterization methods presented above to develop an initial supercapacitor model based electrical and dynamic responses. The chapter explored EEC methods developed from both time and frequency domains. The basic model developed from the constant current method (time domain) and the proposed model developed from the impedance response (frequency domain) were both based on a two R-C/CPE branch arrangement. The difference however, was that, the proposed model, because of its non-linear

electrochemical behavior (with diffusion element CPE) demonstrated SC pore distribution and charge permeability at small voltage variations (validated with simulation results in both frequency and time domains) thus proving the impedance model as the better fit to interpret and evaluate the electrochemical process that contributes to the dynamic response in SCs.

CHAPTER 6- ACCELERATED SUPERCAPACITOR AGEING TEST RESULTS AND MODELS

6 Overview

This chapter presents accelerated test results performed on both SC individual cells and modules. The tests conducted were environmentally and operationally induced (as illustrated in Figure 3-2) to study the thermal and electrical effect on SC ageing. The aim of this study is therefore to understand the ageing process and mechanism that contribute to the failure in SCs. The study was conducted, by periodically monitoring the state of health (SOC) of the SC cells in between test phases. This chapter not only presents accelerated test results but also explains the results in details, using characterization methods and ageing models as a tool.

As mentioned in earlier chapters and previous studies such as (Azaïs et al., 2007)(El Brouji, Briat, Vinassa, Henry, et al., 2009), (Hammar et al., 2010) and (Bittner et al., 2012), voltage and temperature are the predominant ageing/stress factors that cause changes to the physical and chemical properties of SCs, thus decreasing their lifespan. These two main factors have been studied extensively, both individually and

simultaneously, in mild and harsh environments to understand SC failure/degradation behaviour. Although, studies on ageing tests in SCs are available in the literature, EV and HEV operation conditions associated with SC failure are far from understood, hence this study.

The results presented in this chapter are divided into three sections, to study ageing effect of:

1) SC cells under voltage and temperature stress factors
2) SC module with and without voltage equalisation circuits during constant current charge/discharge tests (with and without a load), under high temperature.
3) SC module during variable load profile (charge/discharge tests) under high temperature.

6.1 Accelerated Ageing Tests

SCs are predicted to have long life cycle under normal conditions, with a prediction of more than ten years or one million charge/discharge cycles by (G. Wang et al., 2012).Therefore to shorten test duration and accelerate ageing, ageing tests are performed at high temperature and high voltage conditions, but still abiding by the maximum capability of the device specification to stress endurance. Hence, the end of life (EOL) criteria can be met within a few months.

A few commercial SC cells from HC series (BCAP0025) Maxwell Technologies, USA, with a voltage rating of 2.7V and a capacitance value of 25F, were used in carrying

out all the experimental tests in this research work. The experimental tests performed used both single cell and module SCs in different set-ups to study ageing behaviour. The accelerated tests were grouped into three test set-ups, with each set-up having a predefined area of focus in the behavioural study of SCs.

A. SET-UP 1: Effect of SC cells under voltage and temperature stress factors

Set-Up 1 (as illustrated in Figure 3-4) is a test method where 3 SC cells were subjected to 3 different test; (1) Temperature test (at 75^{o}-85^{o}), (2) Constant Voltage (at 2.7V, 20^{o}) and (3) Calendar test (at 27V, 75^{o}-85^{o}). Set-Up 1 was proposed to establish a reference to this area of study by first putting to test the fundamental stress factors; voltage and temperature. Usually, in practice, two or more stress factors are applied together on SCs. Therefore, it is often difficult to associate the observed ageing process with a particular type of stress factor since the resulting ageing process is a product of the contribution of many factors at a time. Hence, set-up 1, so as to identify the ageing process specific to the stress factor, and consequently create a baseline for further test methods.

B. SET- UP 2: Effect of SC modules with and without voltage equalisation circuits during constant current charge/discharge tests (with and without a load), under high temperature

Set-Up 2 test method (illustrated in Figure 3-5) was based on the study of voltage balancing with-in a SC module during constant current charge/discharge under high-temperature conditions. Set-Up 2 is divided into two set-ups; set-up 2A and set-up 2B, to study the effect of constant current

charge/discharge in a system with and without a load attachment. The constant current profile employed have no rest time between charge and discharge, so that it gives the electrolyte no time to settle between charging and discharging to represent a stressful condition in terms of electrolyte ageing.

C. SET-UP 3: Effect of SC module during variable load profile (charge/discharge tests) under high temperature

The accelerated test method employed in this test Set-Up (as shown in Figure 3-6) emulates certain EV's drive cycles using four different current load profiles. These tests were carried out in a temperature chamber at $85^{o}C$ to simulate harsh environmental and operational conditions perceived in EV applications.

The tests conditions are selected according to the manufacturer's specification and the equipment capability in the Sahz-Nottingham NANO Supercapacitor Pilot Plant. It should be noted that these tests are extreme to SCs especially the test temperature used in this study, as it is over the boiling point of AN (81.6℃) (H. Gualous et al., 2012)(Alcicek et al., 2007).

6.1.1 Supercapacitor Periodic measurement tests

The accelerated ageing tests are followed by a periodic measurement procedure to characterise SCs and to monitor degradation in their state of health (SOH). The SOH of the SCs were measured by comparing characteristic data before commencing the tests with the data obtained during characterization at different stages of SC lifetime (as shown in sections 6.2. 6.3 and 6.4). Periodic characterization measures the age of the SC cell and cell functionalities at every given rest time between test phases. In this work, characterization tests are performed every 144H test duration during rest time. A 24H open circuit rest time was introduced between test phases to provide the SC cell samples ample time to return to a stable voltage and temperature condition for a more suitable characterization process. Accelerated tests with periodic characterizations are repeated over and over, and are only stopped when either one of the following end-of-life (EOL) criteria is met:

- 20% loss from the initial capacitance
- 100% increase in ESR
- Cell opening due to the build-up of pressure in the cell
- Open/Short circuit

Three characterization tests were performed at room temperature at 0V after 24H rest time on each SC cell in no particular manner i.e.: (1) Electrochemical Impedance Spectroscopy (EIS) test, (2) cyclic voltammetry (CV) test and (3) constant current (CC) test.

1. Electrochemical impedance spectroscopy (EIS) test is performed on each SC cell sample with no bias voltage, before and after each accelerated ageing test using a potentiostat (PGSTAT302N) equipped with a frequency response analyser (FRA) module from Metrohm Autolab B.V. The EIS test is done in potentiostat mode by sweeping frequencies over the range of 10kHz to 100mHz with 10 points/decade using an AC sine wave signal of 10mV.

   EIS measurement tool is used to track the ageing course of the cell samples in its impedance spectrum by;

   - Identifying changes in the cell samples' electrochemical process at the electrode/electrolyte interface, thus, identifying their ageing mechanisms, by isolating changes/anomalies observed at different frequency range within the impedance spectrum.
   - Developing electrical equivalent circuit (EEC) models to help interpret ageing dynamic behaviour of the test samples within a wide frequency range for EV operations.

2. Constant current (CC) test is performed to measure the capacitance and the ESR of SC samples to quantify ageing. The SC is charged at constant current with a current rate of 75mA/F (current of 2A). The SCs are then set to rest at open circuit for 15s between charge and discharge cycle according to the Maxwell 6 step process (shown in Figure 5-2), as it has been proven to be the most suitable method of testing under the experimental condition (illustrated in section 5.2.2 of chapter 5). Capacitance and ESR are calculated using Equation 5.7 and Equation 5.8 respectively. Apart from measuring

capacitance and ESR, CC test method is also used to evaluate ageing behaviour in terms of; Charge/discharge (whole cycle) time, charge/discharge voltage, the voltage drop at open circuit rest, and charge time on load tests, all which affect SC behaviour during ageing tests.

3. Cyclic voltammetry (CV) test is performed by applying a linear voltage ramp to the SC between 0V to 2.7V, at a scan rate of 30mV/s. The resulting current is measured and recorded on a current-voltage curve. As part of the electrode condition process, CV test is done in many cycles until there is very little change in the data between cycles. Although this particular test method doesn't provide as much information as EIS and CD tests, but in conjunction with the other two methods, this characterization method can be valuable when studying SC ageing behaviour, especially when observing shape-curve changes that occur with every experimental test phase: and how these changes affect the current needed for the sample to reach its rated voltage.

6.2 **SET-UP 1**: Effect of Supercapacitor cell performance under voltage and temperature ageing factors

Set-Up 1 EIS, CC and CV test results performed on 3 SC cell samples are presented here, and Table 6-1 shows the test durations of each cell sample. Cell samples T2 and M4 were subjected to two different temperature levels, $75^{o}C$ and $85^{o}C$ as show in Table 6-1. The temperature increase from $75^{o}C$ to $85^{o}C$ was done without any rest time between tests, except for the periodic 24H open circuit rest time after every 144H.

SC cell Samples	**Stress Factors**	**Overall test duration (Hours)**
T2	Temperature set at 75^{o}C	1296H
	Temperature set at 85^{o}C	1152H
M3	Constant Voltage at 2.7V and Room Temperature 20^{o}C	2592H
M4	Constant Voltage at 2.7V and Temperature set at 75^{o}C	432H
	Constant Voltage at 2.7V and Temperature set at 85^{o}C	432H

Table 6-1: SET-UP 1- SC cell samples duration under stress conditions

6.2.1 Electrochemical Impedance Spectroscopy Test Results (EIS)

During accelerated tests the sample cell's impedance spectrum deviates from its initial spectrum. This observation is considered to be due to reactions that occur in the cell at the electrode/electrolyte interface or of the active material. Accordingly, the initial impedance spectrum is compared with the measurements obtained at different stages during the lifetime to monitor this change.

A. Cell sample T2

Appendix E-1 presents the Impedance evolution of T2 during high temperature according to Table 6-1. Appendix E-1a provides a more illuminating response of the changes that occur during ageing than the other three graphs in the figure. Appendix E-1 shows the changes during the ageing process from the beginning of the test until the test ends in terms of frequency response. At each stage of SC life, it is observed that new changes are being encountered or that the change becomes more emphasised over time.

The most obvious change, which also seem to be the most prominent effect of ageing at high temperature is observed by a semi-circle formation at high frequency and a shift of the impedance spectra along the real axis. The semi-circle replaced by the original 45^{o} line (of a SC cell initial impedance spectrum) increases in size (diameter) and the spectrum shifts further along the real axis with ageing frequency.

As ageing time proceeds in Appendix E-1a, the first semi-circle was observed after 1296H when the temperature was increased from $75^{o}C$ to $85°C$. The semi-circle becomes clearer at the 1584H and continues to grow in diameter till the 2592H, which occupies a great portion of spectrum. This observation, clearly shows how an increase in temperature expedites ageing process in SCs.

In Appendix E-1b, calculated capacitance seemed to be unaffected with ageing time at high frequency, as the value fluctuated at a ±2 rate of $20F$ value from 0H to 2592H. There also seemed to be a uniform plot across the frequency range, except when a spike was observed between 100Hz and 1kHz at 0H, 720H and

1152H. This observation shows that temperature alone as a stress factor has little effect on ageing.

The shift of the impedance spectra observed along the real axis, indicating the real impedance Z' increasing with ageing is clearly seen in the Z' vs frequency plot (Appendix E-1c), whereby at 0H, the Z' is 0.42Ω at 100mHz, and at 2592H, the Z' increased to 0.19Ω. However the Z' vs frequency plot shows a non-uniform change. Initially, the real part of the impedance is not frequency dependent; however, as ageing progresses, the real part becomes distorted and becomes more frequency dependent, particularly at higher frequencies, as evident in the 2448H and 2592H Z' responses.

At 2592H, Capacitance and Z' (ESR) are affected at the same frequency value, with the Z' starting a decent at 145Hz, at the point the capacitance plummet to the 0F value. The beginning and the ending of the distortion observed at Z' vs frequency plot are also in concordance to the start and the end of the semicircle formation in Appendix E-1.

Similarly, in the Frequency vs –Phase graph (Appendix E-1d), the phase from 1584H onwards are also distorted, evident by a sudden hump at high frequencies. The rest of the plots, however, seem unaffected by frequency.

B. Cell sample M3

Appendix E-2 presents the Impedance results that studies the principle effect of constant voltage test on M3 at room temperature 20^{o}C.

The Nyquist plot (in Appendix E-2a) shows no changes to the impedance spectrum of the cell M3. Even after 2592H, the impedance spectrum still preserved its initial shape at 0H. However, the noticeable ageing change observed over time is the shift of the impedance spectrum towards higher values along the Z' axis. Another change observed in Appendix E-2a, though not really obvious, but worth mentioning, is comparing the impedance spectrum at 2592H with the spectrum at 0H. The impedance spectrum at 2593H deviates with a little tilt towards the right at the low frequency part of the spectrum from the spectrum at 0H.

Appendix E-2c shows the Z' vs frequency graph; the graphs shows a slight frequency dependent behaviour of the impedance real part. The Z' values increases with decreasing frequency. Nevertheless, the whole response is nearly linear, with no sudden increase nor fall. The Z' vs frequency graph confirms the earlier observation pertaining to the movement of the Nyquist plot along the real axis. At 0H the Z' value recorded is 0.0451Ω and at 2592H the Z' recorded is 0.079 at 100mHz. Appendix E-2c and Appendix E-2b shows the capacitance and phase plots have little to no effect on the frequency, even after 2592H

Cell sample M4

Cell sample M4 is used to investigate the influence of both temperature and voltage effect on SC performance. M4 is tested by applying a constant voltage 2.7V while at the same time is exposed to high temperature at 75℃ for 432H which is then increased to 85℃ for the next 432H. Appendix E-3 presents the results of this test.

Appendix E-3a shows the evolution of the impedance spectrum from 0H to 1008H. Besides a clear shift of the impedance real part along the Z' axis, the shape of the impedance spectra certainly deviated from the initial response at 0H. Not only does the spectrum at 1008H tilted by a high degree and decreases in slope at low frequency, there was also a semicircle of small radius (but large base diameter) at high frequency of the spectrum which replace the 45° line of the 0H spectrum, and also what seemed like a semicircle-like bump at the medium-frequency. The emergence of the semicircle and bump-like was detected in the spectrum at 864H. Unlike the temperature test which only showed the appearance of one semicircle, this test condition raised a semicircle at high-frequency and a semicircle-like bump at the medium-frequency in which both of them differ in sizes and magnitudes. The differences in size signify that they both have different time constant.

In the Z' vs frequency graph (Appendix E-3c), the Z' response after 864H escalates with decreasing frequency. This increase is significant, compared to the responses in the earlier hours. Similarly, the phase vs frequency response at 864H and 1008H also deviates from the rest. In addition, the SC capacitance appears to be more affected than the previous two tests presented above. At the 1008H, the capacitance dropped from its initial value 21.2F to 15F.

6.2.2 Constant Current Test Results (CC)

CC test is carried out on cell samples T2, M3 and M4 using a 2A quasi-square charge/discharge current profile separated by a 15s rest period between charge and discharge, during periodic characterization. The main purpose of this test as mentioned above is to calculate SC capacitance and ESR, but besides that, it is a great tool in analysing ageing behaviour in SC.

A. Cell sample T2

Figure 6-1 shows the CC voltage response evolution from 0H to 2592H, due to the limited space in the graph and for the sake of visibility, only significant changes to the CC voltage response that occurred during the ageing period are displayed.

The most obvious ageing change in Figure 6-1 is the decrease in charge/discharge time from 0H to 2592H. Initially, the duration it takes to charge/discharge a cell through 5 cycles using Maxwell's six process method is about 380secs, but after subjecting sample T2 to a high-temperature level for 2592H, the overall charge/discharge time is reduced to about 298secs. The decrease in charge/discharge time over accelerated tests time is in correlation to the voltage drop witnessed, before and after the 15secs open circuit just after charging and also after discharging. The voltage drop which also represents the cell's ESR (see Equation 5.8) increases as the ageing process continues just as seen with the voltage response at 2592H. Even with the changes observed at the voltage drop and the cycle time over the samples lifetime, the first charge at 0H, 1584H and

2594H seemed to be unaffected and remained at the same level, unlike the rest of the charge or discharge level that shifted with time.

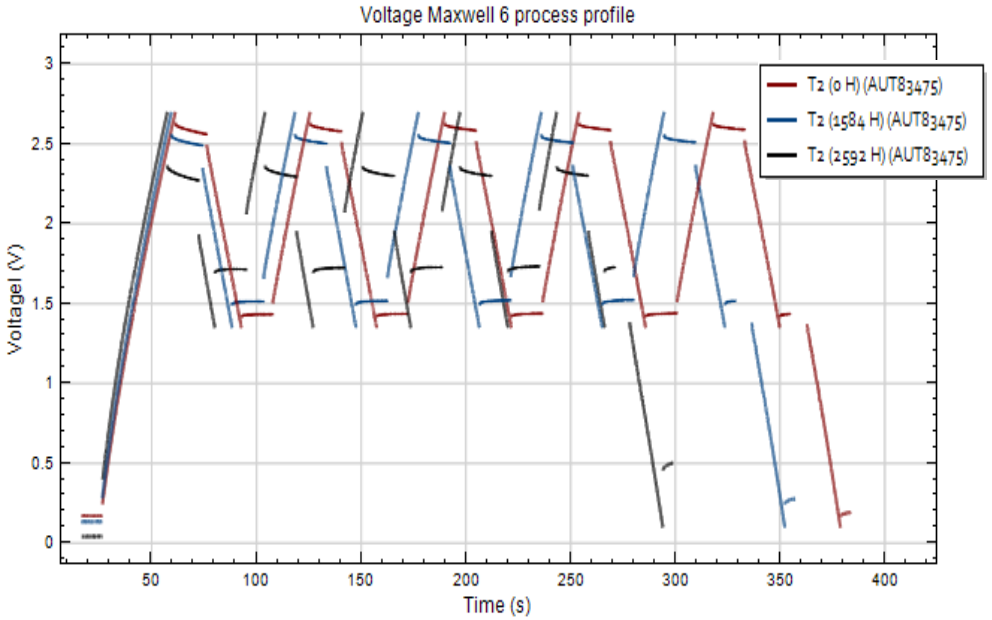


Figure 6-1: T2 CC test results (displaying SC lifetime voltage response to a 2A charge/discharge current profile over the accelerated test timeline)

B. Cell sample M3

M3 CC results correspond to its EIS test results, which indicates voltage alone as a stress factor have little effect on SC ageing. Figure 6-2 show little to no voltage drop or any significant decrease in ESR even after 2448H. The charge/discharge time after 2448H test recorded 330H in contrast to its original cycle time of 350H.

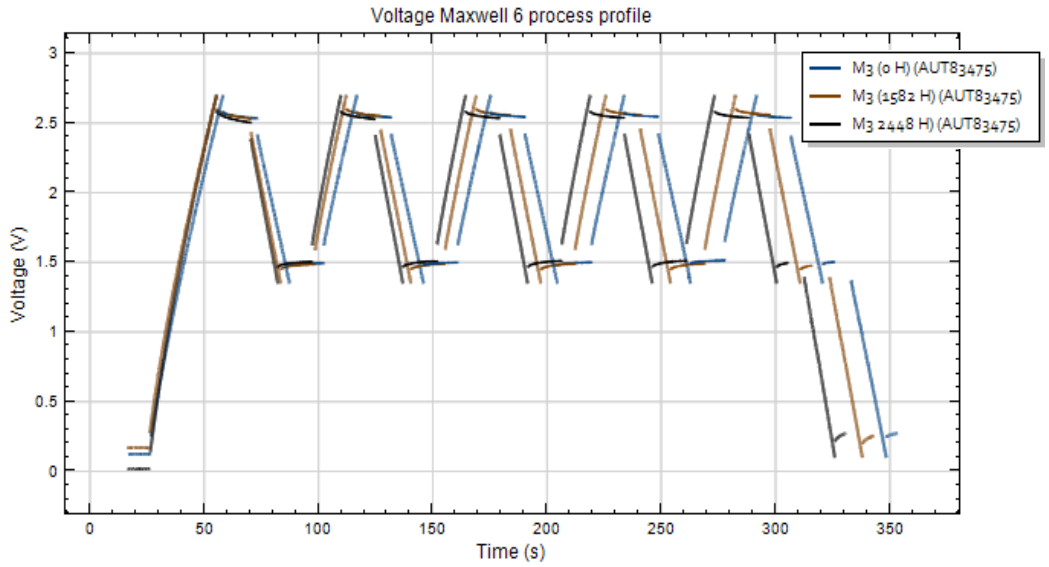


Figure 6-2: M3 CC test results (displaying SC lifetime voltage response to a 2A charge/discharge current profile over the accelerated test timeline)

C. Cell sample M3

Sample M4 presents its ageing evolution as shown in Figure 6-3, with an obvious drastic change in voltage response just after 720H of accelerated test. At 720H, the shape of the voltage response deviated from its initial response at 0H. The voltage at 720H sky rose to 1.7V before and after each charge/discharge phase, and the charge time seemed to decrease with each cycle, and the mid-voltage between charge/discharge deviated from its original constant value 1.35V through the five cycles to a lower voltage which differs between each cycle. The discharge time at 720H seemed to be none existent with each cycle and as the accelerated tests continued to 864H (not shown in the Figure 6-3) the cell displayed a negative discharge level of about 1.7V with each of the five cycles.

The overall charge/discharge time of cell M4 after 720H was recorded at approximately 195secs, as to its initial duration of 390secs. The change in the

shape of the charge phase from a tilted line to a straight line could be due to the decrease in charge time.

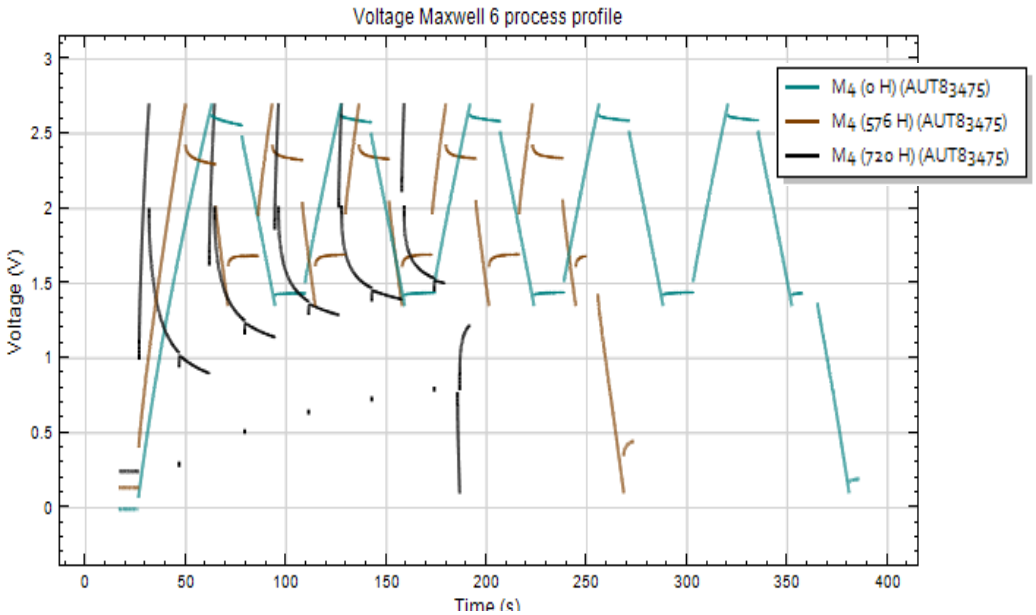


Figure 6-3: M4 CC test results (displaying SC lifetime voltage response to a 2A charge/discharge current profile over the accelerated test timeline)

6.2.3 Cyclic Voltammetry Test Results (CV)

Figures 6-4 to 6-6 show cyclic voltammograms at different stages of SCs life test conditions described in set-up1 (see Table 6-1). The shape of CV curves of all fresh cells is almost rectangular. The current slowly rises when charging the SCs from 0V and decreases when the scan is reversed. No 'hump' pertaining to redox reactions at the electrode surface is observed during measurement. This observation is auspicious indicating that the cells are in a good condition before the start of the accelerated ageing test.

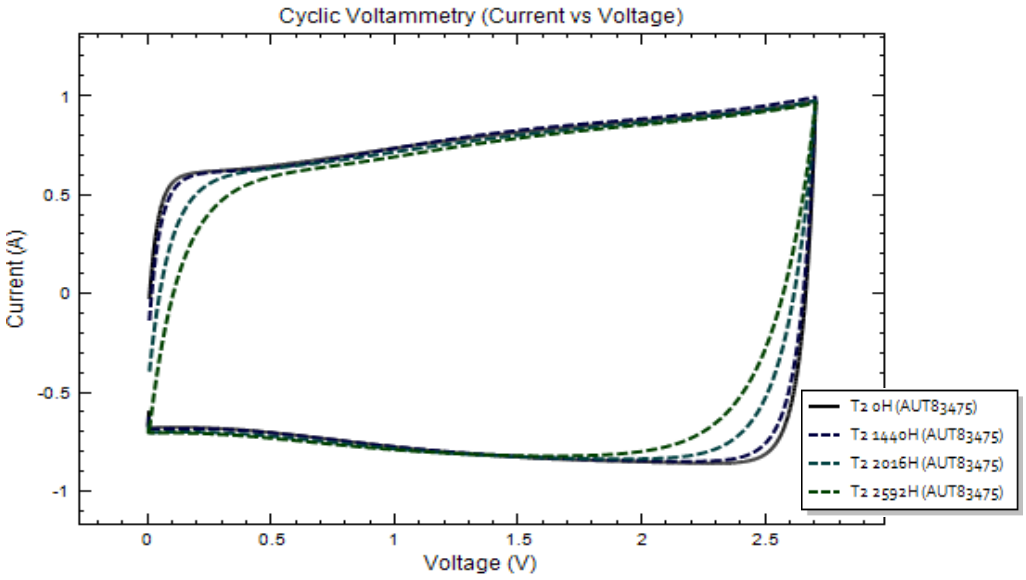


Figure 6-4: T2 CV test results (showing cyclic voltammograms at different stages of SC lifetime during temperature test) at scan rate 30 mV/s.

After ageing tests are stopped, there is a notable change in the CV shape which shows that the SCs have aged. The recorded cyclic voltammograms after ageing tests show distortions particularly in samples that are exposed to high temperature, such T2 (Figure 6-4) and M4 (Figure 6-6). As SC ages, the CV wave shape becomes more of a leaf-shaped.

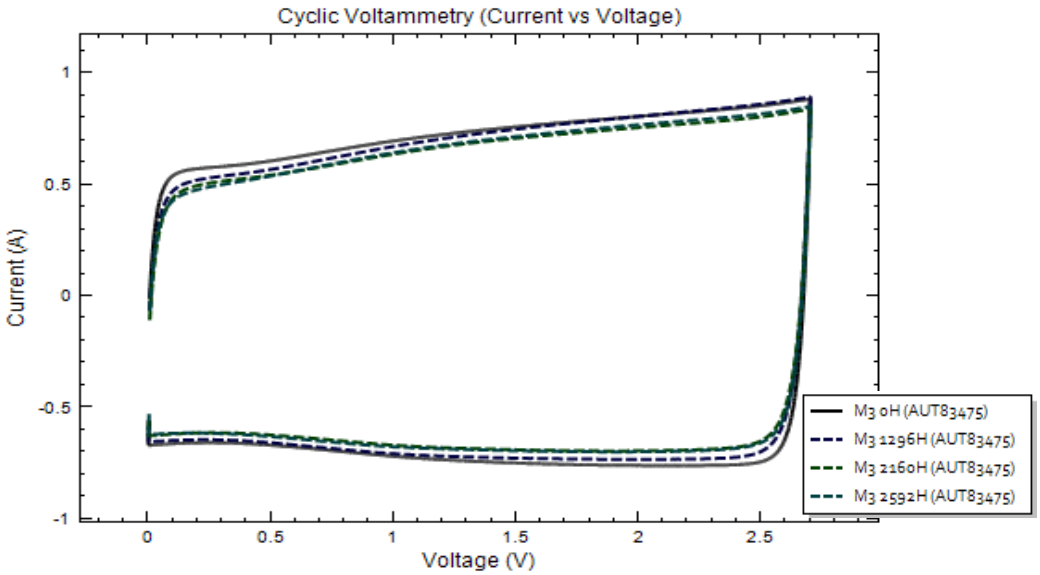


Figure 6-5: M3 CV test results (showing cyclic voltammograms at different stages of SC lifetime during constant voltage test) at scan rate 30 mV/s.

The observed distortions are more conspicuous in samples T2 and M4, compared to sample M3 (Figure 6-5) where the stress from high temperature is absent in the test conditions. The results show a minimal effect on the CV wave shape even after 2592H. This observation suggests that this test condition does not significantly affect the cell capacitance. Nevertheless, no redox behaviour is observed in all test condition, suggesting that Faradaic reaction does not take place in the SCs during the accelerated ageing test.

In sample M4, the distortion in the CV wave shape is more pronounced, whereby after 1008H, the CV wave shape changed considerably. This could be due to the reason that 30mV/s scan rate was no longer suitable at this stage; the electrochemical reactions in aged SC have slowed down and the 30mV/s scan rate is too fast to allow the electrochemical reactions to occur.

The distortion is accompanied with a narrowing of the CV wave shape, indicating that the cell capacitance has decreased. Since the charge Q, is simply the area between the CV curves, therefore, Figure 6-6 has the lowest remaining capacitance as Q.

These findings show that if more than one ageing factor is present, the ageing effect is greater. In fact, SC sample M4 shows the most shrinking of the CV wave-shape after being stressed for 1008H (Figure 6-6), followed by cell sample T2, then M3, which shows the slightest wave-shape change after 2592H.

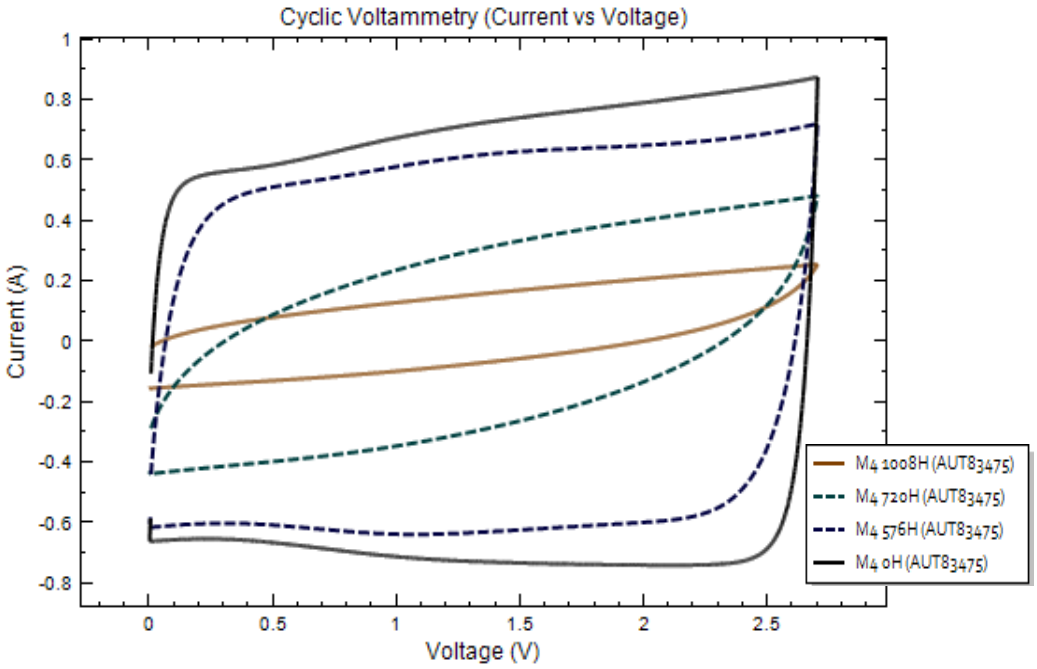


Figure 6-6: M4 CV test results (showing cyclic voltammograms at different stages of SC lifetime during temperature and constant voltage test) at scan rate 30 mV/s.

6.2.4 Capacitance and ESR comparisons

The loss of capacitance and the increase in ESR in aged SC samples under set-up1 test conditions are compared in Figure 6-7. The capacitance and the ESR are calculated based on Equations (5.7) and (5.8) from the constant current test. It is found that the end-of-life (EOL) criteria for both capacitance and ESR are not reached at the same time.

The strong effect of both voltage and temperature in cell sample M4 is clearly seen, as the EOL criteria reached the earliest in set-up 1. A drastic 20% loss in capacitance is found as soon as 430H, whereas the 100% increase of ESR is only seen after 575H. In cell sample T2, the ESR seemed to be more affected, in which the 100% increase of ESR is measured at 1580H, while the capacitance value took longer (2300H) to

show any degradation effect, after the 20% loss line. Meanwhile, the constant voltage test observed in cell sample M3 does not show any remarkable change in capacitance after 2592H. However, a fluctuation in the ESR is detected between 100% to 167% mark, although the ESR EOL criteria was not yet met after the test stopped.

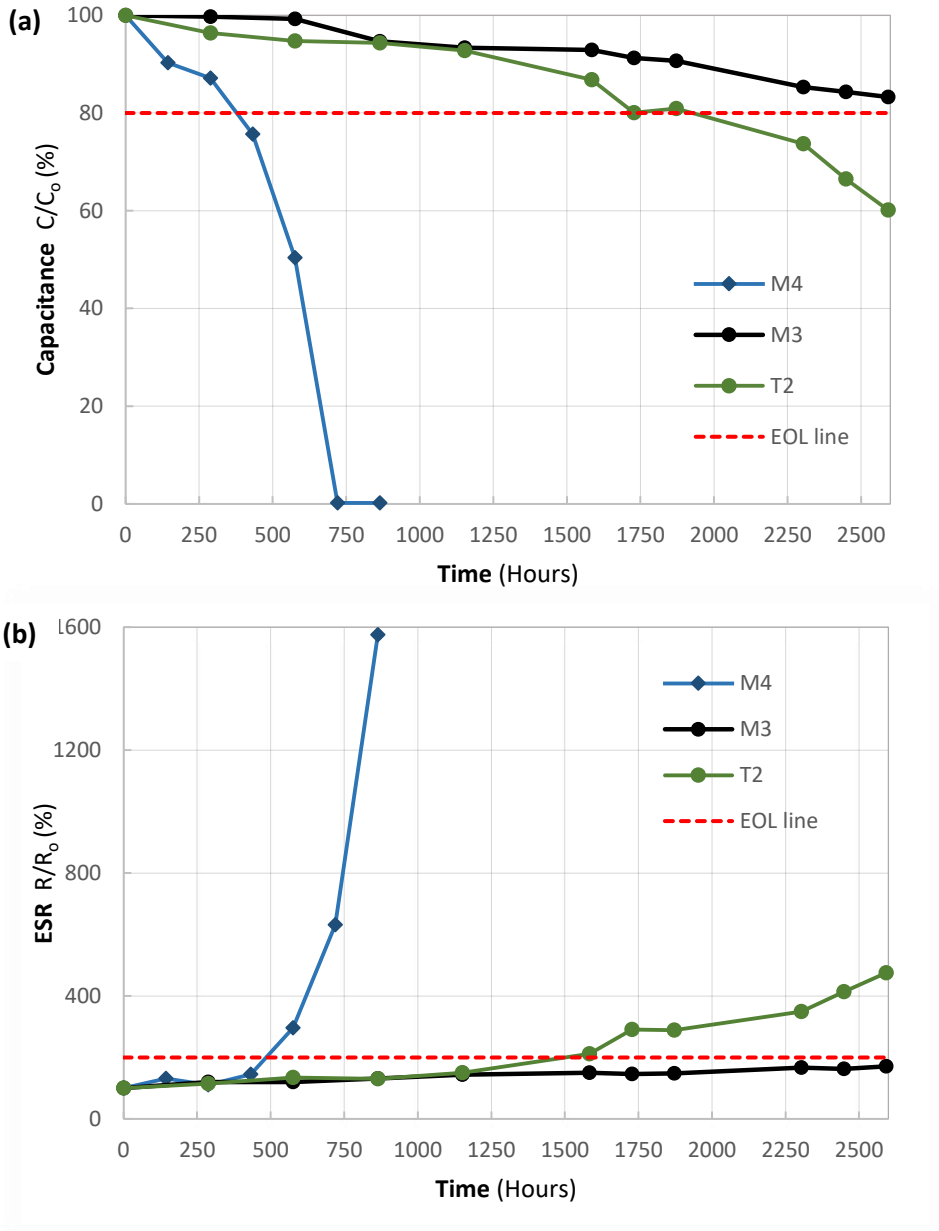


Figure 6-7: Comparing SC set-up1 samples' normalised parameters through their degradation stages: (a) C/Co capacitance normalised its initial value, (b) R/R_o resistance normalised to its initial value.

It is interesting to note that in all the three conditions tested in set-up 1, the SC samples reached its EOL, either in terms of capacitance and/or ESR, only in samples T2 and M4. This finding agrees with previous observations from the periodic characterization test, hence, confirming the firm effect of these conditions on SC ageing. Note that, in the periodic characterization test, the impedance spectra, constant current cycles and the cyclic voltammograms are greatly affected in the said cell samples. However, test sample M3 showed no effect on ageing after 2448H, which could be caused by the lack of ample test time for the internal heating to cause enough warming to degrade the cell quickly. The lack of test time, however, was not the case for cell M4, where the constant voltage effect caused enough warming of the cell in the form of Joule losses in no time, consistent with (Dandeville et al., 2011a).

6.2.5 SET-UP 1: Ageing models

Set-Up 1 test results in the form of EIS, CV and CC characterization tests have demonstrated the deterioration of the SC material in terms of electrical behaviour as the SC samples endures each ageing stimuli. From the data gathered above, ageing models are developed to illuminate the ageing characteristic of SCs and as a tool to assess the impact of ageing on the SCs dynamic behaviour.

The ageing models were built by fitting an EEC to the impedance response similar to the modelling process carried out to obtain the initially proposed model in chapter 5. Therefore, the observable failure mechanisms can be reflected in the model and also

aids in clarifying the electrochemical processes that take place during the ageing course. Moreover, the ageing model shows the relations between the ageing behaviour of the SC and its electrical and dynamic behaviour.

During this research, it was found that the ageing process is specific to the ageing factors applied, thus test samples generate different ageing model according to their ageing factors. For that reason, two ageing models are proposed based on their test conditions and ageing factors experimented in set-up 1. Set-Up 1 ageing factors were tested on three SC samples; T2, M3 and M4, in which only M3 of the three samples did not meet any of the end-of-life (EOL) criteria mentioned above. Hence, there was no need to develop a different model as the initial model was still sufficient to model the sample's behaviour after 2592H of continuous constant voltage test at room temperature.

A. T2 Ageing model

The impedance response of the aged T2 SC sample under high-temperature test (Figure 6-8a) shows the presence of new electrochemical processes; that demonstrates the diffusion process in aged SCs. The difference between the initial and the aged impedance spectrum on its electrochemical process showed that the initial model, previously developed (in chapter 5) was no longer fitting to embody the aged response. Therefore, the initial model was revisited to include this response:

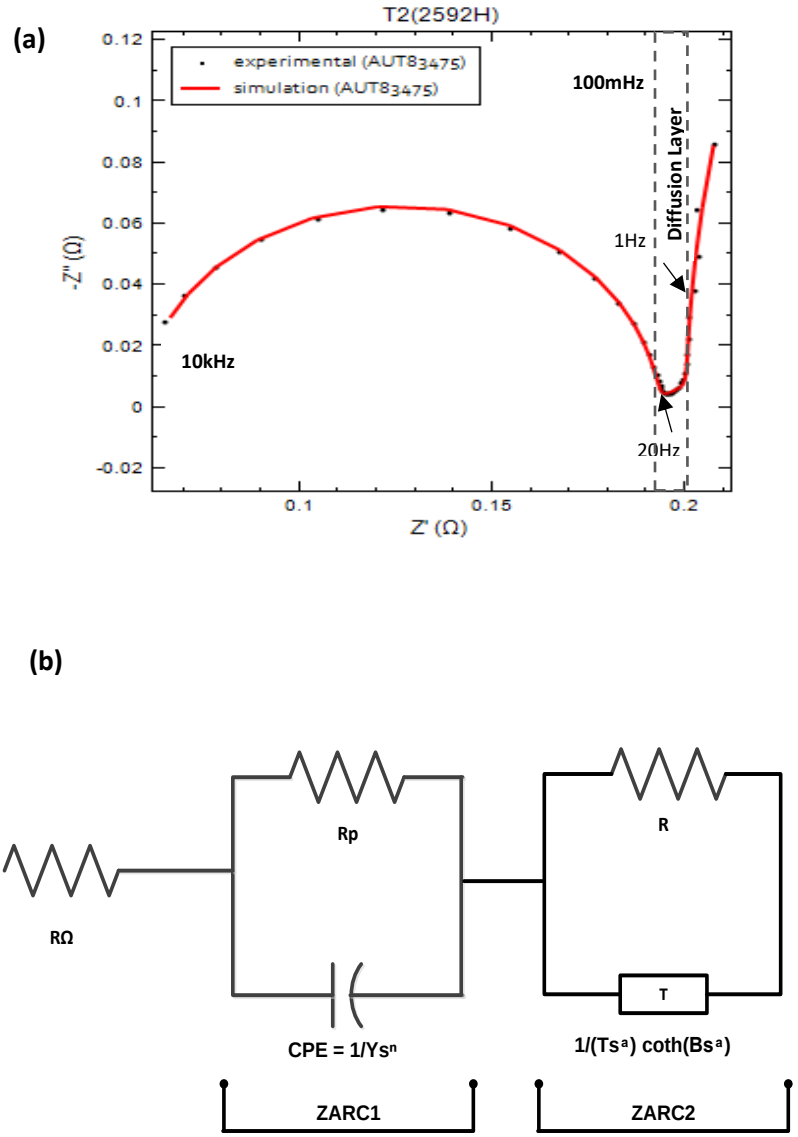


Figure 6-8: Impedance spectrum of aged T2 after 2592H of been subjected to a high temperature chamber: (a) experimental (dotted line) and simulated (red line), (b) the EEC used to simulate the impedance spectrum

Although the initial model in (Figure 5-14) was valid to fit sample T2 during the accelerated test from test period 0H to 1584H (when the capacitance value dropped to 86% of its original value and the ESR increased to about 150% of its original value) at which the state of sample T2 was still healthy and yet to exhibited any EOL criteria. The change of state from the initial model to the ageing model (in Figure 6-8b) occurred after 1728H when the sample began to develop anomalous behaviour in

their frequency and voltage responses, indicating changes in the sample's health status. Moreover, it should be noted that the transition from the initial model to the ageing model is in correlation with the semicircle formation in the impedance spectrum under experiment. The ageing model in Figure 6-8b was the most appealing fit that best described the EEC behaviour of T2 from 1728H to the point of complete failure (i.e. cell not able to hold any charge), though the model validity was only tested from 1728H to 2592H.

The high-frequency intercept (10kHz) corresponds to the value of the ohmic resistance, R_{Ω}. This resistance is usually related to the resistance from current collector, electrolyte and separator. The second electrochemical process is the contact resistance between electrode and current collector, marked by a semicircle at frequencies between 10kHz to 20Hz. The semicircle was drawn with a circuit consisting of a parallel connection resistor R_P and a CPE. The third process which occurs between frequency 20Hz and 1Hz shows a transition from the semicircle to a more capacitive region as frequency decreases and this response is pertaining to the diffusion effect. The 45° line at the bend of the low frequency part has the form of a diffusion layer. The bounded diffusion element T with reflective boundary that extends to lower frequencies in the spectrum was used in a parallel connection with a resistor R to model both medium and high frequency of the spectrum. As frequency decreases, the diffusion layer becomes more capacitive but not quite of the ideal capacitance response. This non-vertical line of the low-frequency part shows what is known as an asynchronous charging (Fletcher et al., 2013) which causes open circuit voltage decay, capacitance loss at high frequency and voltammetric distortions. Nonetheless, this transition is still with the bounded diffusion element T. Suggesting

that the diffusion layer is restricted, possibly due to the aluminium oxide layer that forms on the electrode surface on the aged SC. The particle size distribution may also cause the low frequency part to be shunted to the left as the particle geometry becomes more curved, as has been reported in (J. Song & Bazant, 2013) for the case of battery electrode. Equation (6.1) gives the equation of the impedance of the T element where B is the time ($s^{1/2}$) it takes for a reactant to diffuse from one side of the layer to the other, D is the diffusion coefficient and δ is the thickness of the thin layer and is described in Equation (6.2).

This type of diffusion is normally observed, for example, in battery materials, where the active material or electrolyte layer has a limited thickness (Barsoukov, 2005).

The impedance of T is given by,

$$Z_T = \frac{1}{Y_0\sqrt{j\omega}}\coth\left(B\sqrt{j\omega}\right) \tag{6.1}$$

$$B = \frac{\delta}{\sqrt{D}}\ (s^{1/2}) \tag{6.2}$$

B is the time ($s^{1}/_{2}$) it takes for a reactant to diffuse from one side of the layer to the other, D is diffusion coefficient and δ is the thickness of the thin layer.

The ageing model is made up of a serial combination of resistor R_Ω, and two complex plane Z_{ARC1} and Z_{ARC2}. Z_{ARC1} consists of a parallel combination of a CPE and a resistor R_P, while Z_{ARC2} was made up of a parallel combination of a bounded diffusion element T and a resistor R.

The ageing model $Z(s)$ in s plane is thus;

$$Z(s) = R_\Omega + \frac{R_p}{1 + (R_p Y)s^n} + \frac{R.coth(Bs^a)}{R.Ts^a + coth(Bs^a)} \quad (6.3)$$

Where, a is 0.5 and n was determined from CNLS fitting.

However, the coth function in Equation (6.3) makes it difficult to simulate in a circuit simulation software. Thus, the coth function need to be approximated to form a rational model. According to (Nicolas Bertrand et al., 2010), Padé approximant gives a better approximation than the Taylor series because of its rational function. Following (Riu & Retière, 2004), the coth function for low frequencies is approximated as follows,

$$\coth(x) = \frac{\cosh(x)}{\sinh(x)} \underset{x \to 0}{\cong} \frac{1 + x^2/2}{x} \quad (6.4)$$

From the development of $\sqrt{1 + x^2}$, the Equation (6.4) becomes:

$$\coth(x) \underset{x \to 0}{\cong} \frac{\sqrt{1 + x^2}}{x} \quad (6.5)$$

Substituting Equation 6.8 to Z_T in equation (6.1), the impedance of the T-element is then equal to:

$$Z_T(s) = \left\{\frac{1}{Ts^a}\right\} \coth(Bs^a) = \frac{\sqrt{1 + (Bs^a)^2}}{TBs^{2a}}; a = 0.5 \quad (6.6)$$

Therefore, the approximated impedance of Equation (6.3) now becomes,

$$Z(s) = R_\Omega + \frac{R_p}{1 + (R_p Y)s^n} + \frac{R\sqrt{1 + (Bs^a)^2}}{RTBs^{2a} + \sqrt{1 + (Bs^a)^2}} \quad (6.7)$$

Expanding and arranging equation (6.7) yields the FOTF transfer function of $Z(s)$ in the form of,

$$Z(s) = \frac{V(s)}{I(s)}$$

$$Z(s) = \frac{As^{am} + Bs^{bm} + Cs^{cm} + Ds^{dm} + Es^{em} + Fs^{fm} + Gs^{gm} + Hs^{hm} + Is^{im}}{Js^{jn} + Ks^{kn} + Ls^{ln} + Ms^{mn} + Ns^{nn} + Os^{on} + Ps^{pn} + Qs^{qn}} \quad (6.8)$$

Where the coefficients of the transfer function and their circuit parameters are given in Table 6-3 and Table 6-3.

Transfer function coefficients	
$A = R_\Omega + R_p + R$	
$B = \sqrt{B^2 + R_p B^2 + R_\Omega B^2}$	$b_m = a$
$C = \sqrt{{R_p}^2 R^2 T^2 B^2 + {R_\Omega}^2 R^2 T^2 B^2}$	$c_m = 2a$
$D = \sqrt{{R_p}^2 R^2 Y^2 + {R_\Omega}^2 {R_p}^2 Y^2}$	$d_m = n$
$E = \sqrt{2R_p R^2 Y + 2R_p {R_\Omega}^2 Y}$	$e_m = \frac{n}{2}$
$F = \sqrt{{R_p}^2 B^2 Y^2 + {R_\Omega}^2 {R_p}^2 B^2 Y^2}$	$f_m = a + n$
$G = \sqrt{2R_p B^2 Y + 2R_p {R_\Omega}^2 B^2 Y}$	$g_m = \frac{2a + n}{2}$
$H = R_\Omega R_p RTBY$	$h_m = 2a + n$
$I = \sqrt{2R_p {R_\Omega}^2 R^2 B^2 T^2 Y}$	$i_m = \frac{4a + n}{2}$

Table 6-2: Set-Up1 (T2): Transfer function coefficients according to the aged model circuit parameters presented in Figure 6-8b

Transfer function coefficients	
$J = B$	$j_n = a$
$K = \sqrt{2R_pY}$	$k_n = \frac{n}{2}$
$L = R_pY$	$l_n = n$
$M = RTB$	$m_n = 2a$
$N = RR_pTBY$	$n_n = 2a + n$
$O = R_pBY$	$o_n = a + n$
$P = \sqrt{2R_pYB^2}$	$p_n = \frac{2a+n}{2}$
$Q = \sqrt{2R_pR^2T^2YB^2}$	$q_n = \frac{4a+n}{2}$

Table 6-3: Continuation… Set-Up1 (T2): Transfer function coefficients according to the aged model circuit parameters presented in Figure 6-8b

B. M4 Ageing model

The effect of the voltage at high temperature in cell sample M4 required a slightly different ageing model than that of T2. The difference in the ageing model was as a result of the semicircle at high frequency and the bump at the medium frequency that emerged on the spectrum on the aged M4 cell, shown in Figure 6-9a. The first semicircle emerged between frequency 10kHz and 233Hz, while the bump that seemed like an arc lies between frequencies 222Hz and 0.8Hz.

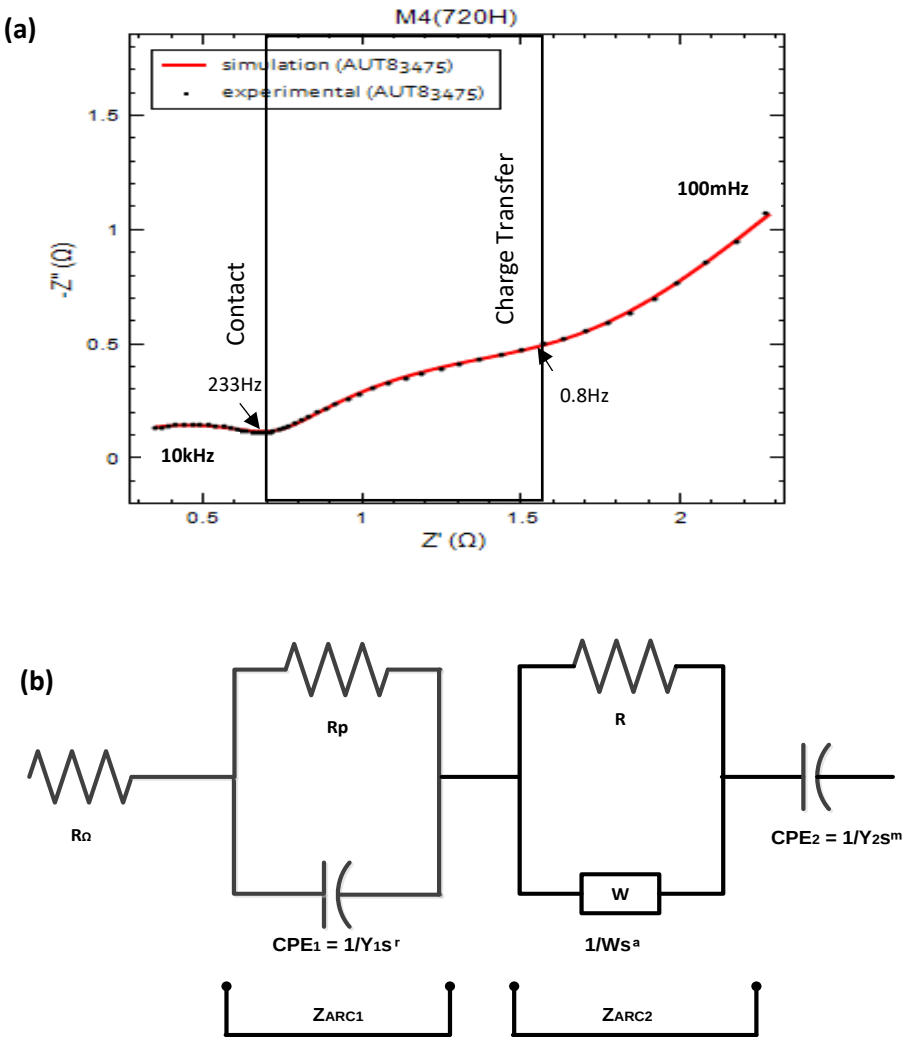


Figure 6-9: Impedance spectrum of aged M4 after 720H in constant voltage test 2.7V and high temperature: (a) experimental (dotted line) and simulated (red line), (b) the equivalent circuit used to simulate the impedance spectrum.

The first semicircle Z_{ARC1} consists of a parallel connection of resistor R_P and a CPE_1 which is related to an increase of the contact resistance between electrode and current collector. However, the appearance of the bump at medium frequency was unexpected and cannot be assigned directly to any electrochemical process, although if observed thoroughly, it showed a response of a charge transfer reaction, consisting an Z_{ARC2} with a parallel connection of a resistor R and a Warburg element W. Given that the distortion at the medium frequency was not a complete semicircle placed at

a 45^{o} angle, the behaviour was modelled with a Warburg element instead of the usual CPE element.

The Warburg element is given in Equation 6.9 (Juan Bisquert, Garcia-Belmonte, Fabregat-Santiago, & Bueno, 1999) (J. Bisquert, 2002)(Raistrick et al., 2005).

$$Z_W = \frac{1}{Y_0\sqrt{j\omega}} \tag{6.9}$$

Warburg impedance Z_W is sometimes written as,

$$Z_W = \frac{\sigma(1-j)}{\sqrt{\omega}}\ (\Omega) \tag{6.10}$$

moreover, σ relates to Y_0 in Equation (6.9) by;

$$\sigma = \frac{1}{\sqrt{2}\cdot Y_0}\ (\Omega \cdot s^{-1/2}) \tag{6.11}$$

Presently, the explanation for this phenomenon has not yet been found; therefore, the discovered behaviour is open to interpretation. Nonetheless, it is possible that this condition is likely to occur due to the formation of corrosion products or may be related to the increase of the distributed resistance.

A similar response had been reported in (Ruch, Cericola, Foelske-Schmitz, et al., 2010) for SCs aged at elevated voltages. The response is also similar as the one appeared in (Gaberscek, Moskon, Erjavec, Dominko, & Jamnik, 2008) in the study of interphase contacts in lithium ion electrodes. Perhaps, the bump is a unique effect from voltage stress.

Meanwhile at low frequencies between 0.8Hz and 0.01Hz, the diffusion lead the end of the bump to rise from the real axis and this behaviour is represented by a series CPE_2 in the aged EEC model.

The M4 ageing model was made up of a serial combination of a resistor R_Ω, a CPE_2 element, two circuit impedance Z_{ARC1} and Z_{ARC2} .

The ageing model $Z(s)$ in s plane is thus;

$$Z(s) = R_\Omega + \frac{R_p}{1 + Y_1 s^r} + \frac{R}{1 + W s^a} + \frac{1}{Y_2 s^m} \tag{6.12}$$

Where, a is 0.5 and m and r was determined from CNLS fitting.

Expanding and arranging Equation (6.12) yields the FOTF transfer function of $Z(s)$ in the form of,

$$Z(s) = \frac{V(s)}{I(s)}$$

$$Z(s) = \frac{A + Bs^{bm} + Cs^{cm} + Ds^{dm} + Es^{em} + Fs^{fm} + Gs^{gm} + Hs^{hm}}{Is^{in} + Js^{jn} + Ks^{kn} + Ls^{ln}} \tag{6.13}$$

Where the coefficients of the transfer function and their circuit parameters are given in Table 6-4.

Transfer function coefficients	
$A = 1$	
$B = R_p Y_1$	$b_m = r$
$C = R_\Omega Y_2 + R_p Y_2 + R Y_2$	$c_m = m$
$D = R_\Omega R_p Y_1 Y_2 + R R_p Y_1 Y_2$	$d_m = r + m$
$E = RW$	$e_m = a$
$F = R_\Omega R Y_2 W + R R_p Y_2 W$	$f_m = a + m$
$G = R R_p Y_1 W$	$g_m = a + r$
$H = R_\Omega R_p R Y_1 Y_2 W$	$h_m = a + r + m$
$I = Y_2$	$i_n = m$
$J = R_p Y_1 Y_2$	$j_n = r + m$
$K = R Y_2 W$	$k_n = a + m$
$\mathrm{L} = R_p R Y_1 Y_2 W$	$l_n = a + r + m$

Table 6-4: Set-Up1 (M4): Transfer function coefficients according to the aged model circuit parameters presented in Figure 6-9b

6.2.5.1 Ageing model validation

The two ageing models developed for T2 and M4 were simulated in MATLAB, FOMCON toolbox using Equations (6.8) and (6.13) as the fractional transfer function block-set provided in FOMCON SIMULINK library. The circuit component values used in both ageing models T2 and M4 to derive the transfer function coefficients presented in Table 6-2, Table 6-3 and Table 6-4 were summarised in Table 6-5 along with their chi-square, x^2.

Components (units)		***Fitted Values***			
		Ageing model ***T2 (2592H)***		Ageing model ***M4 (864H)***	
		Values	Errors (%)	Values	Errors (%)
$\boldsymbol{R_\Omega}$ *(Ω)*		0.0589	0.91	0.08197	8.37
$\boldsymbol{R_p}$ *(Ω)*		0.1329	0.56	0.77541	10.09
$\boldsymbol{R}$ *(Ω)*		1.0709	23.91	0.67769	0.78
$\boldsymbol{CPE}$	Y (mho)	0.00112	4.49	-	-
	n	0.9917	0.55	-	-
$\boldsymbol{CPE_1}$	Y_1 (mho)	-	-	0.18106	4.01
	r	-	-	0.70373	3.14
$\boldsymbol{CPE_2}$	Y_2 (mho)	-	-	1.0254	5.48
	m	-	-	0.5788	4.81
$\boldsymbol{W}$	W (mho)	-	-	0.00873	3.19
$\boldsymbol{T}$	T (mho)	26.63	4.31	-	-
	B	0.6835	4.59	-	-
$\boldsymbol{x^2}$		1.9358×10^{-3}		2.8123×10^{-3}	

Table 6-5: EEC circuit parameters of ageing models T2 and M4

Before simulations, the impedance transfer function $Z(s)$ (substituting the circuits component values presented in Table 6-5) stability test of the ageing models were determined using the stable function in the FOMCON FOTF viewer, and the results are presented in Figure 6-10. As it can be seen, all poles are located in the stable area and no poles fall in the shaded area. Therefore, the stability function K for the model is 1, indicating the ageing models stability with their parameters and their RMSE simulated voltage response in Table 6-6.

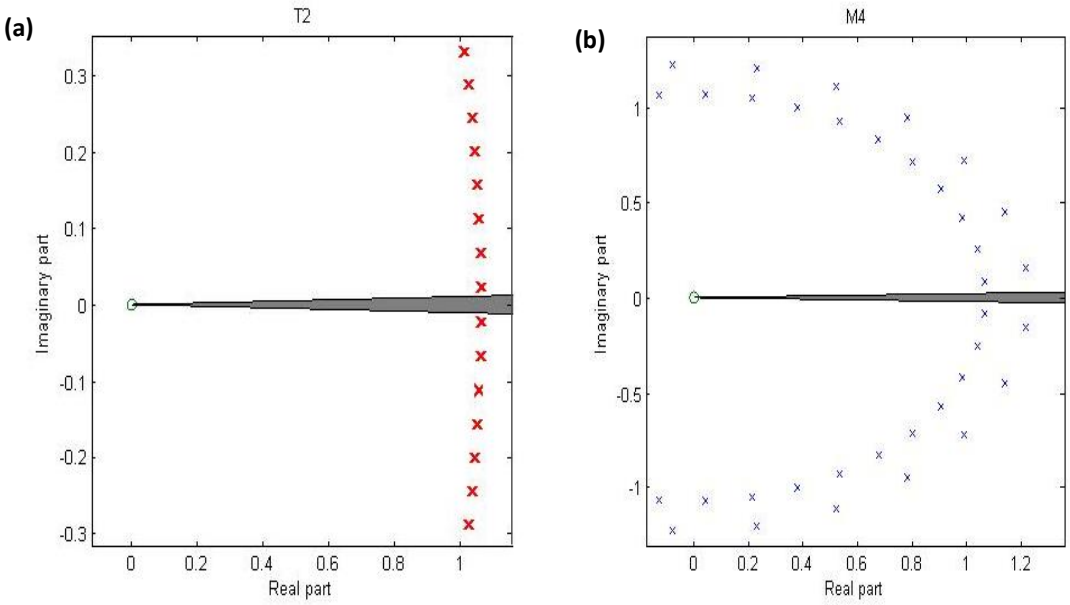


Figure 6-10: FOTF Stability test results (a) using the parameters in equation (6.8), and (b) using the parameters in Equation (6.13)

Stability Test Parameters	T2(2592H)	M4(720H)
K	1	1
q	0.0100	0.0200
ERROR	0.01204	0.002182
APOL	0.0211	0.0806
RMSE (voltage profile)	0.0740	0.3224

Table 6-6: FOTF Stability test results with emphasis on the parameter accuracy of the transfer functions, including the RMSE results between the simulated and experimented voltage response

The ageing models were simulated to output a voltage response from an input current made of 2A charge and discharge pulses. Since the model is stiff, the solver ode15s in variable-step is used for fast simulation and accuracy. The voltage response is simulated according to the following relation,

$$V(t) = V_0 + ESR \cdot I + IZ(s) \tag{6.14}$$

Where, V_0 is the initial voltage, $Z(s)$ is the impedance of the ageing models and the ESR is the internal resistance

Figure 6-11 shows the simulated voltage response of the ageing model from the 2A current pulses input. It can be seen that the ageing model gives a satisfactory result over a large duration, although there was a small difference between the simulated and the experimental results at the end of the simulation when the current source was completely removed. Although, the RMSE between the experimented and the simulated data compared to the SC voltage responses in Figure 6-11 was small.

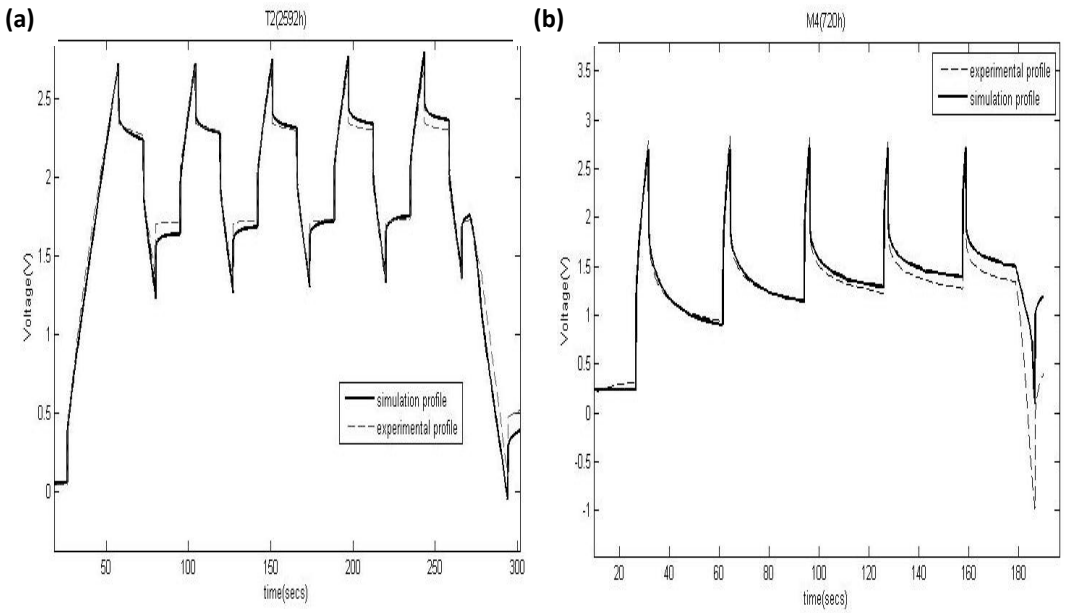


Figure 6-11: Validation test of the ageing models (a) T2 and (b) M4 using a 2A current profile: voltage simulated from the ageing models (solid line) and experimental data (dash line).

6.3 **SET-UP 2:** Effect of Supercapacitor module performance (with and without voltage equalisation circuits) during constant current charge/discharge tests (with and without a load), under high-temperature conditions

Set-Up 2 used Five sets of SC module of two cell connected in series in a module rated at 5.4V each. Three sets of the module were used to study the effects of SC performance with and without equalization circuits during constant current charge/discharge tests under high temperature conditions, while the other two sets were used to study SC performance with equalization circuits during constant current charge/discharge tests with an additional motor load under high-temperature conditions. For easy analysis, set-up 2 was divided into two parts, with set-up 2A addressing the three sets of SC module (without load) and set-up 2B addressing the remaining two sets of SC module (with a motor load).

6.3.1 SET-UP 2A Test Results

EIS, CC and CV test were performed on each of the cells in all three sets of the SC module. Module samples W5 & W6, B7 & B8 and C9 & C10 test descriptions are presented below in Table 6-7, according to each module's stress factor and test duration.

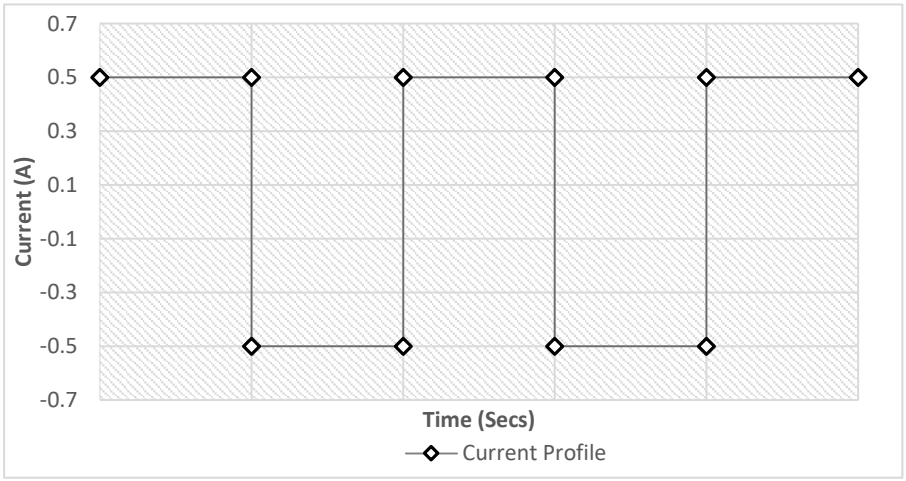


Figure 6-12: Current profile of set-up 2A using a 0.5A current with no rest time in between charge and discharge cycle

The cycling test observed in set-up2A is based on a consecutive charge/discharge current cycle presented in Figure 6-12. The module cell samples are cycled between 0V and 2.7V using the current profile above. The resulting voltage response of each module's samples were presented in chapter 4 (section 4.4) with varying voltage response duration observed with each module set.

SC module cell Samples	Stress Factors		Overall Cycle duration (equivalent hours)
	Constant Current charge/discharge with no load	Temperature Factor	
W5 & W6	Without a voltage equalization circuit	75°C	44,680 Cycles (720H)
		85°C	17,880 Cycles (288H)
B7 & B8	With equalization circuit 1 (shown in 3-10a)	75°C	13,642 Cycles (432H)
		85°C	22,737 Cycles (720H)
C9 & C10	With equalization circuit 2 (shown in 3-10c)	75°C	39,876 Cycles (720H)
		85°C	15,951 Cycles (288H)

Table 6-7: SET-UP 2A- SC module cell samples duration under stress conditions

6.3.1.1 Electrochemical Impedance Spectroscopy Test Results (EIS)

This test is focused on investigating the contribution of temperature in SC degradation during cycling. Cycling tests are performed on SC cells in pairs, with each pair retaining its position throughout the test period. It is essential for each cell in the module to maintain its initial position when subjected to a charge/discharge regime, as the first cell positioned at the positive terminal to the source stores more charge than the cell at the negative terminal, hence the cells in the module displaying ageing at different rates. Thus, SC module cell presented in Table 6-7 are connected accordingly, with **W5** as the first cell and **W6** the second cell, **B7** as the first cell and **B8** the second cell, and **C9** as the first cell and **C10** the second cell.

A. Module cell samples W5 & W6

Appendix E-4 and Appendix E-5 shows the impedance changes during cycling test aged at 75℃ for the first 44,680 cycles (720H) and 85℃ for the next 17.880 cycles (288H), at different stages of the SC cell life. This module takes about 58 secs to complete a test cycle. The graph only displays important changes to the shape of the impedance spectra as ageing proceeds.

Appendix E-4a and Appendix E-5a displays changes in W5 and W6 respectively in two forms: (1) movement of the impedance spectrum along the real axis, and (2) emergence of a semicircle replacing the 45° slope line and a continual expansion of the size and diameter of the semicircle as ageing progressed. These changes occurred in a similar manner and almost at the same time with little to no difference in each cell. However, after the 62,560 cycles mark (1008H) the shape of the impedance spectrum suddenly changed (as shown in a separate panel in Appendix E-4a and Appendix E-5a) to record a ridiculously high ESR of about 40000Ω at 100mHz for W5 and about 6.5Ω for W6, which is confirmed in the Z' vs frequency graph (Appendix E-4c and Appendix E-5c). An addition change in form of a prominent inclination of the low frequency part to the right was also observed at this stage. The astronomical difference in ESR values observed between W5 cell and W6 cell implies that the ageing of both cells in the module occurred at different rate, even though both cells were subjected to the same test process.

The Capacitance vs. Frequency graph (Appendix E-4b and Appendix E-5b) seemed to generate a uniform graph even after 53,620 cycles for both cells W5 and W6,

with an average of 20F recorded at 100mHz. However, after 62,560 cycles, both cells capacitance dropped without warning to record a value of 0F for W5 and 1.5F for W6 at 100mHz.

Z' is frequency dependent that it increases as frequency decreases. The Z' value at 100mHz fluctuates with each periodic characterization, at first, the Z' (ESR) value seemed to increase gradually with every characterization till, after 35,750 cycles where the values of W5 and W6 increased quickly to 0.095Ω and 0.098Ω respectively, but then decreased in the next two characterization, recording ESR values of 0.078Ω and 0.072Ω at 53,620 cycles (as seen in Appendix E-4c and Appendix E-5c). Although the ESR values fluctuates with each characterization, it does not generate a sequential increasing/decreasing pattern, the ageing rate seemed to be uniformly distributed between both cells, till after 62,560 cycles when the ESR recorded about a 4000Ω value difference between the two cells.

The Phase vs. Frequency plot (Appendix E-4d and Appendix E-5d) on the other hand, generated a similar and uniform plot for both cells W5 and W6 till after the 53,620 cycle, where each plot gradually decreased in phase with increasing frequency. After 62,560 cycles, both cells totally deviated from the plot pattern to show the Phase decreasing with decreasing frequency. Although the phase at 10kHz of cell W5 doubled the phase value of W6.

Appendix E-4 and Appendix E-5 is a very good representation in terms of frequency, SC evolution from inception to total failure.

B. Module cell samples B7 & B8

Appendix E-6 and Appendix E-7 shows the impedance changes during cycling test aged at 75℃ for the first 13,642 cycles (432H) and 85℃ for the next 22,737 Cycles (720H), at a different stage of SC life. A total of 1152H accelerated test period was allocated to test the module, unlike the 1008H allocated test time to module W5 and W6. In module B7 and B8, the test duration was reduced in the 75℃ chamber and increased in the 85℃ chamber, thus introducing a harsher environment than that of module W5 and W6.

Appendix E-6a and Appendix E-7a shows the impedance changes of B7 and B8, the spectrum of both cells in the module seemed to change with time in a similar pattern and at the same rate. The movement of the spectrum along the real axis of both cells is completed almost at the same rate, with B7 always a few ohms ahead (about $10^{-2}\Omega$). The semi-circle which began to form in both cells after the 13,643 cycle, increased in diameter with every characterization. However it was noticed that the diameter of the semi-circle, particularly at 31,831 cycles and 36,379 cycles, increased more in cell B7 than in cell B8. A slight inclination of the lower frequency part of the spectrum to the right was also observed with increasing number of cycles.

Z' is frequency dependent, that it increases as frequency decreases. Similar to the module W5 and W6, a curvature distortion is also observed, particularly at 22,736 cycles, 31,831 cycles and 36,379 cycles in both cells B7 and B8. At 36,379 cycles, the distortion starts at 200Hz after a gradual decrease of Z' at the beginning and quickly plunges between 200Hz to 10kHz (as seen in Appendix E-6c and E-7c).

These two frequencies, 200Hz and 10kHz, are where the semicircle curve begins and ends in the Nyquist plot.

The semi-circle causes distortion not only to the impedance real part but also to the Phase vs. Frequency plot. The distortion is described as a hump, which appears to be more prominent at 31,831 cycles and 36,379 cycles (refer to Appendix E-6d and E-7d).

As the number of cycles increases during tests, the more inclined the spectrum at low frequency gets, which in turn decreases the slope at the low-frequency part of the impedance spectrum. The decreasing slope of the low-frequency tail of the impedance spectra (B7 & B8) is directly translated into the drop of capacitance after 36,379 cycles, as visible in the capacitance vs. frequency plot (Appendix E-6b and E-7b). The capacitance initially stands at 20.25F for both cells, but after 36,379 cycles, the capacitance of both cells dropped to 17.24F (the same value).

C. Module cell samples C9 & C10

Appendix E-8 and E-9 shows the impedance changes during cycling test aged at 75℃ for the first 39,876 Cycles (720H) and 85℃ for the next 15,951 Cycles (288H), at a different stage of SC life. A total of 1008H accelerated test period was allocated to test module, similar to the test period allocated to module W5 and W6.

Cells C9 & C10 exhibits similar impedance change to B7 & B8 with an increase in the number of cycles, from the movement of the impedance spectrum along the

real axis, to the emergence and increase in diameter of a semi-circle, and finally the tilting of the impedance real part. Although this module was tested under lesser environmental conditions than B7 & B8, at 55,827 cycles, the semi-circle observed in C9 seemed to double in diameter the semi-circle in cell C10 (as shown in Appendix E-8a and E-9a), which wasn't the case in module B8 & B9.

Similar to module B7 and B8, a curvature distortion is also observed, particularly at 39,876 cycles and 55,827cycles in both cells C9 and C10. At 36,379 cycles, the distortion starts at 70.29z after a gradual decrease of Z' at the beginning (as seen in Appendix E-8c and E-9c). These two frequencies, 70.29Hz and 10kHz, are where the semicircle curve begins and ends in the Nyquist plot.

The distortion in the Phase vs. Frequency plot is also described as a hump, which appears to be more prominent at 39,876 cycles and 55,827 cycles (refer to Appendix E-8d and E-9d).

The decreasing slope of the low-frequency tail of the impedance spectra (C9 & C10) is directly translated into the drop of capacitance after 55,827 cycles, as visible in the capacitance vs. frequency plot (Appendix E-8b and E-9b). The capacitance which was initially at 21.19F for both cells, after 55,827 cycles, the capacitance of C9 decreased to 19.07F while C10 dropped to 18.14F (the same value).

6.3.1.2 Constant Current Test Results (CC)

To correlate the results from the EIS measurement tests on SCs electrical performances, it was appropriate to plot the charge and discharge characteristics.

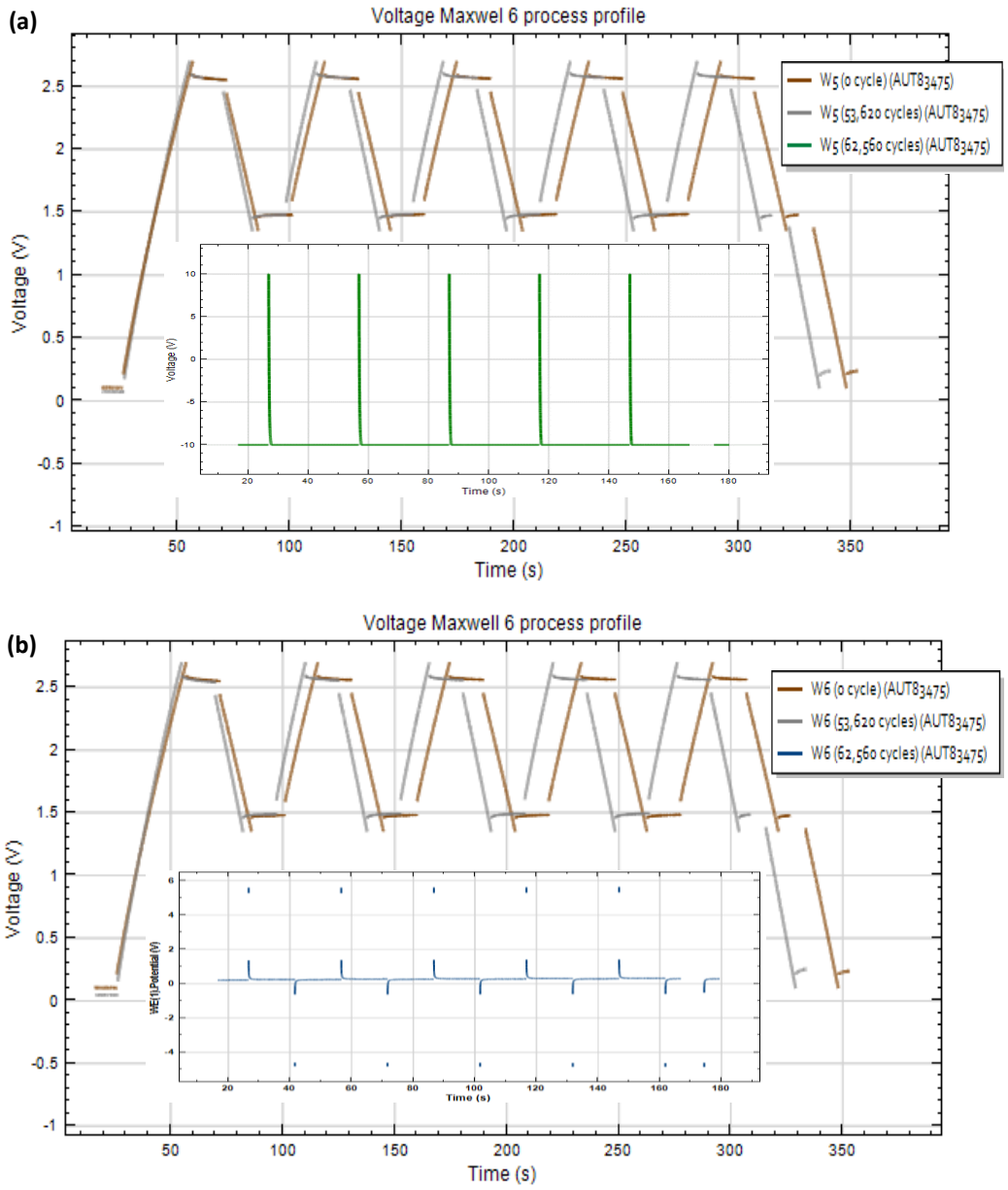


Figure 6-13: Module sample (a) W5 & (b) W6 CC test results (displaying SC lifetime voltage response to a 2A charge/discharge current profile over the accelerated test timeline)

A. Module cell samples W5 & W6

Figure 6-13 shows the CC voltage response evolution from 0 cycle to 62,560 cycles. At the 53,620th cycle, the voltage response of both samples W5 & W6 exhibited a slight shift in time from 350 secs to 330 secs for W6 and 340 secs for W5. Although an increase in the shift was noticed at each of the five cycles that

made up the voltage response, both cells maintained equal charge/discharge time at each cycle.

After the 62,560th cycle, both cells' voltage responses abruptly changed in appearance and cycle duration. Cell W5 at its 62,560th cycle completed the five cycle duration in 180secs (about half its original duration) and charged up from -10V to 10V (instead from 0V to 2.7V pre-selected during the measurement) with 0V recorded discharge phases. Given the abnormality of the charge/discharge regime and the fact that the cell charged up from a negative voltage plot, further un-simulated (real) tests revealed that the cell could not be charged up nevertheless hold a charge. W6, on the other hand, was able to charge up to 1.5V but only start holding the charge at 1.33V which ends up self-discharging rapidly after disconnecting the charge. Unlike W5, W6 was able to charge up in the positive plot between 0V to 5V but discharge in the negative plot between 0V to -5V. Although both cells aged at separate rates with W5 being the first not able to hold a charge and W6 the second cell just able to hold half the original charge, both cells in an application are rendered useless.

B. Module cell samples B7 & B8 and C9 & C10

Appendix E-10 shows the voltage responses of module cells B7 & B8 (Appendix E-10a and E-10b) from 0 cycle to 36,379 cycles (1152H), and module cells C9 & C10 (Appendix E-10c and E-10d) from 0 cycle to 55,827 cycles (1008H).

Module cells B7 & B8 after 36,379 cycles, showed equal changes in voltage drop and charge/discharge duration. In both cells, the initial response duration is about 380 cycles and after 36,379 cycles, the test completed the response in about 323 secs. The voltage drop of both cells after 36,379 cycles increased from 0.14V of the initial value to 0.19V.

Module cells C9 & C10 after 55,827 cycles, on the other hand, showed a slight rate of change between the cells regarding voltage drop and charge/discharge duration. C9 being the first cell, aged faster with a complete response time of 330secs after 55,827 cycles compared to its initial response time of about 382secs, and observed a higher voltage drop of 0.16V after 55,827 cycles which was initially at 0.13V. C10 as the subsequent cell, aged a bit slower than C9 with a complete response time of 334secs after 55,827 cycles compared to its initial response time of about 380secs, and observed a higher voltage drop of 0.15V after 55,827 cycles which was initially at 0.13V.

6.3.1.3 Cyclic Voltammetry Test Results (CV)

Figure 6-14 and Appendix E-11 show cyclic voltammograms at different stages of SCs life test conditions described in set-up2A (see Table 6-2). The shape of CV curves of all fresh cells are almost rectangular, but as they age they exhibit changes in the form of a leaf-shaped waveform.

In Figure 6-14, Samples W5 and W6 after 1008H of accelerated tests (which is also 62,560 cycles) showed a considerable change in the CV wave-shape, indicating that the cell capacitance has decreased. The CV shape in W5 at this stage seemed to be none existent with zero capacitance (since there is no area in the CV curve), while W6's CV shape at this stage shrank considerably from its initial shape to a barely leaf-like shape (of a small area within the curve) indicating a very low capacitance.

In Appendix E-11, module samples B7 & B8 after 1152H had shown that the cells performed the cyclic voltammograms test at the same rate. Being that samples B7 & B8 make up the serial module and the cycling tests were carried out at the same time, it was not farfetched to expect the module cells to age at the same rate. Thus, the module samples having similar capacitance value. Similarly, module samples C9 & C10 after 1008H also showed a similar change in CV waveform. Unlike B7 & B8, their change from the initial CV shape was very minimal with very little to no change in current at 2.7V. B7 & B8, on the other hand, observed a small but noticeable change especially, the decrease in current as the CV curve approached the rated voltage 2.7, after 1152H.

The difference in aged CV test between the two modules could be that B7 & B8 were subjected to harsher environmental condition than C9 & C10, and not to mention the differences in their voltage balancing electronic components.

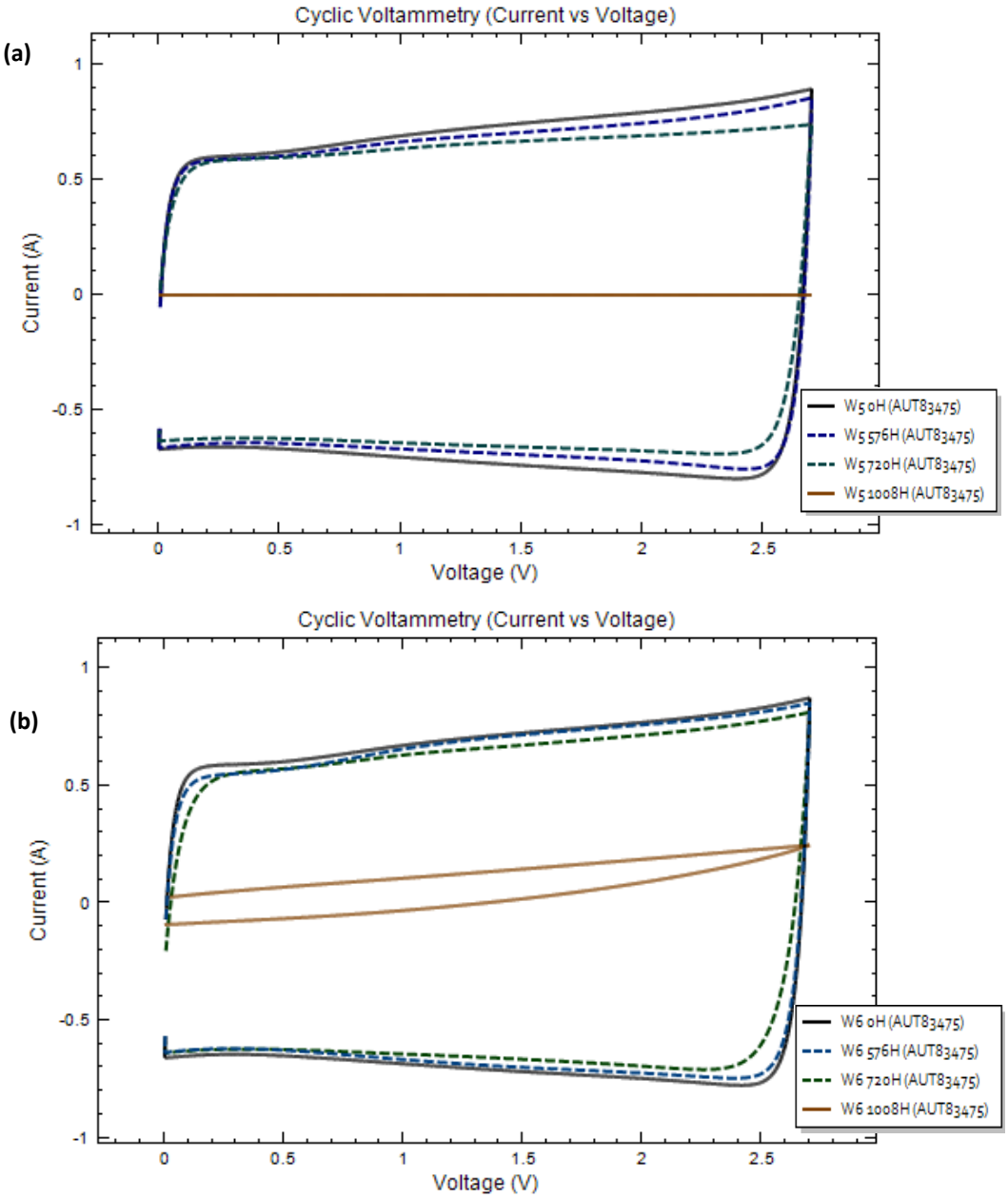


Figure 6-14: Module samples (a) W5 and (b) W6 CV test results (showing cyclic voltammograms at different stages of SC lifetime during cycling test) at scan rate 30 mV/s.

6.3.2 SET-UP 2B Test Results

Characterization test results (EIS, CC and CV tests) of set-up2B SC samples are presented in this section. The cell samples; MtA, MtB, MtC and MtD, were used to carry out the test process of set-up 2B. The cycling test observed in set-up2B is based on a consecutive charge and discharge to a motor load, under environmental conditions described in Table 6-8. The module cell samples are cycled between 0V and 2.7V using a current profile in Figure 6-15. The resulting voltage response of each module's samples were presented in chapter 4 (section 4.4) with varying voltage response duration observed with each module set.

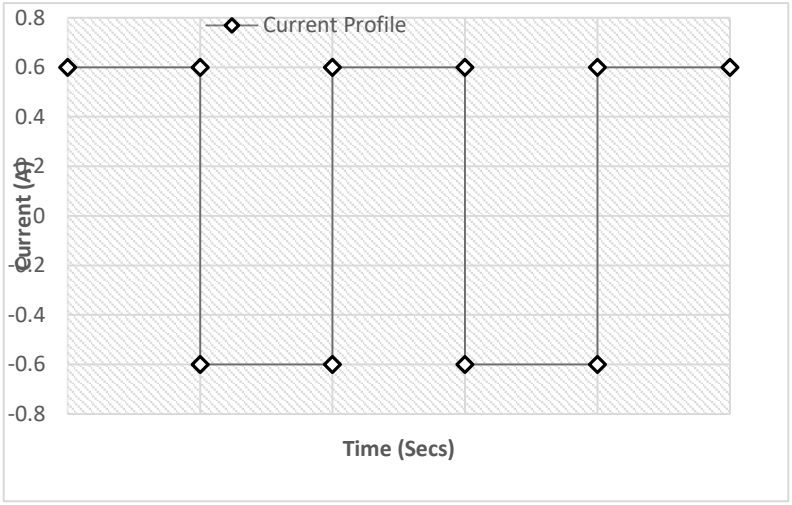


Figure 6-15: Current profile of set-up 2B using a 0.6A current with no rest time in between charge and discharge cycle

The current in set-Up 2B was increased to 0.6A from 0.5A (used in set-up 2A), to accommodate the load included to the set-up (while also minimising the charging current as possible) so as to study external electrical stress factors. A total of 1152H test duration was allocated to both module cell samples MtA & MtB and MtC & MtD for easy comparison.

Although the test period distributed to set-up 2A and set-up 2B tests were the same, because of the differences in hardware, MtA & MtB recorded a longer cycle time (with 1 cycle = 151secs), than MtC & MtD (with 1 cycle = 146secs). Similar to the samples in set-up 2A, each sample in this set-up were also placed strategically and retained throughout the test duration in the module, with **MtA** placed in front as the first cell and **MtB** the second cell to make-up the module, and also **MtC** as the first cell and **MtD** the second cell to make-up the other module.

SC module cell Samples	Stress Factors		Overall Cycle duration (equivalent hours)
	Constant Current charge/discharge with 5V motor load	Temperature Factor	
MtA & MtB	With equalization circuit 2 (shown in 3-10c)	75^{o}C	10,299 Cycles (432H)
		85^{o}C	17,165 Cycles (720H)
MtC & MtD	With equalization circuit 1 (shown in 3-10a)	75^{o}C	10,650 Cycles (432H)
		85^{o}C	17,753 Cycles (720H)

Table 6-8: SET-UP 2B- SC module cell samples duration under stress conditions

6.3.2.1 Electrochemical Impedance Spectroscopy Test Results (EIS)

Set-Up 2B EIS test results are presented here; the results show the influence of temperature on SC cells during load cycles in terms of frequency. The results illustrate impedance response with its supporting graphs.

A. Module cell samples MtA & MtB

Appendix E-12 and E-13 shows the impedance evolution of MtA and MtB during load cycling test at 75℃ for the first 10,299 Cycles (432H) and at 85℃ for the next 17,165 Cycles (720H), at a different stage of SC life, to give a total of 1152H accelerated test period.

MtA and MtB both exhibit similar impedance change over time as samples B7&B8 and C9&C10 with a few noticeable distinctions. As already established in the results shown in set-up 2A, the sample closest to the positive terminal age rather faster than subsequent cells. This manifestation is also observed in module MtA&MtB, where a semi-circle (replaced by the 45^{o} line) is noticed at the 13,732 cycle, 20,598 cycle and the 27,464 cycle in sample MtA while the semi-circle was only observed at the 20,598 cycle and 27,464 cycle in sample MtB. As shown in Appendix E-13a, the semi-circle at 20,598 cycle is barely noticeable and as the test proceeds to the 27,464th cycle it becomes more pronounced but far lesser in diameter than cell MtA at the same cycle mark (see Appendix E-12a). Apart from the difference in semi-circle diameter between the two samples, at the 27,464th cycle, the impedance spectrum seemed to shift further from its initial spectrum in MtA than cell MtB. These two changes when put together, shows MtA aged at a faster rate than MtB.

The Z' vs frequency graphs gives a clearer illustration on how ESR increases as frequency decreases. The Z' at 100mHz differed from each other, where cell MtA at 27,464th cycle recorded a value of 0.113Ω (with a 269.048% increase from its initial value), and MtB at 27,464th cycle recorded a value of 0.0775Ω (with a

176.136% increase from its initial value). A curvature distortion signifying the semi-circle in the Impedance spectrum Nyquist plot is also observed between 100Hz and 10kHz in Appendix E-12c and E-13c, particularly at 13,732 cycle, 20,598 cycle and the 27,464 cycle in MtA and at 20,598 cycle and the 27,464 cycle in MtB.

The capacitance vs. frequency graph (Appendix E-12b and E-13b) and phase vs. frequency graph (Appendix E-12d and E-13d) gives a uniform and expected form with little distortions. Unlike the ESR, the capacitance seemed to have little effect in this test process, as the ageing rate in both cells were synonymous, recording a value of 17F in both cells after 27,464 cycles at low frequency.

A. Module cell samples MtC & MtD

Appendix E-14 and E-15 shows the impedance evolution of cells MtC and MtD during load cycling test at 75℃ for the first 10,299 Cycles (432H) and at 85℃ for the next 17,165 Cycles (720H), at a different stage of SC life. A total of 1152H accelerated test period was allocated to test module, similar to the test period allocated to module MtA and MtB.

The impedance spectrum of both cell samples MtC and MtD show similar ageing pattern as the load cycle test progresses. The impedance shift of both cells along the real axis with each characterization seemed evenly proportioned. The semi-circle emergence, signifying ageing was also observed after 14,202 cycles, 17,753 cycles and 28,405 cycles in both cells, with similar diameter size at each stage, except at 17,75th cycle where the semi-circle diameter in MtD looked slightly

smaller than MtC (see Appendix E-14a and E-15a). Apart from that, the impedance spectrum of both cells seemed alike.

Z' is also frequency dependent that it increases as frequency decreases. Similar to the module MtA and MtB, a curvature distortion is also observed, particularly at 14,202 cycles, 17,753 cycles and 28,405 cycles in both cells MtD and MtD. Z' at the 28,405th cycles (100mHz) in both MtC and MtD record the same ESR value of 0.105Ω (with a 228.261% increase from its initial value). At 28,405 cycle, the distortion starts at 170Hz after a gradual decrease of Z' at the beginning and quickly plunges between 170Hz to 10kHz (as seen in Appendix E-14c and E-15c). These two frequencies, 170Hz and 10kHz, are where the semicircle curve begins and ends in the Nyquist plot.

The decreasing slope of the low-frequency tail of the impedance spectra (C9 & C10) is directly translated into the drop of capacitance after 28,405 cycles, as visible in the capacitance vs. frequency plot (Appendix E-14b and E-15b). The capacitance of both cells was affected by ageing at the same rate, thereby recording a value of 17.12F in both cells at 100mHz after 28,405 cycles.

The distortion in the Phase vs. Frequency plot is also described as a hump, which appears to be more prominent at 28,405th cycle (refer to Appendix E-14d and E-15d).

6.3.2.2 Constant Current Test Results (CC)

The load cycle tests carried out on samples MtA, MtB, MtC and MtD presented some abnormalities compared to the samples subjected to just cycle tests, especially in the first cycle during CC characterization test. These abnormalities were observed during characterization, immediately after the samples were disconnected from the load cycle test. A curve-like charge instead of the usual linear line was observed, in conjunction with a drastic and also curve-like drop in voltage at the open-circuit phase (as seen in Figure 6-16). Although, by the time the CC test completed the 5th cycle, the cell samples' voltage drop seemed to have reduced in voltage considerable, and when the test was repeated 24H later the cell characteristics were completely recovered to a lesser aged form.

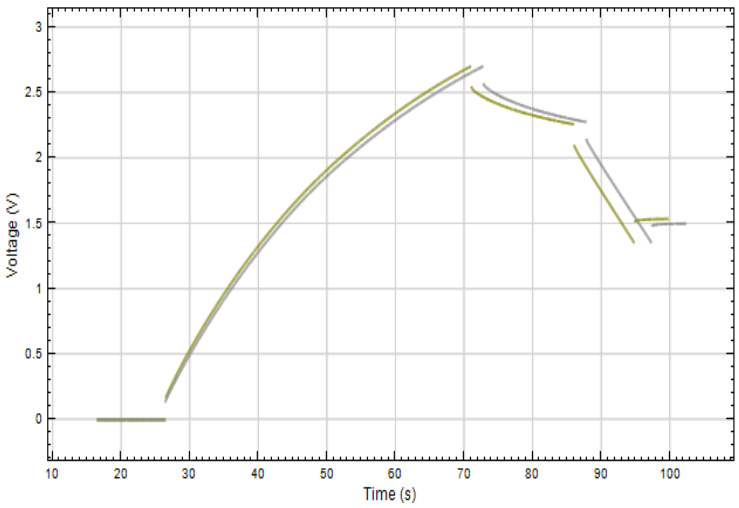


Figure 6-16: A projected graph of the set-up 3 samples' CC test, immediately after an accelerated tests phase, showing a curve-like charging pattern at the first cycle (indicating the present of a DC motor at the load)

Module cells MtA & MtB after 27,465 cycles, showed a slight rate of change between both cells regarding voltage drop and charge/discharge duration (see Appendix E-16a & E-16b). MtA being the first cell, aged faster with a complete response time of 320secs after 27,465 cycles compared to its initial response time of about 380 secs, and observed a higher voltage drop of 0.294V after 27,465 cycles which was initially at 0.157V. MtB as the subsequent cell aged a bit slower than MtA with a complete response time of 334 secs after 27,465 cycles compared to its initial response time of about 380 secs, and observed a higher voltage drop of 0.256V after 27,465 cycles which was initially at 0.159V.

Module cells MtC & MtD after 28,405 cycles, on the other hand, showed a more symmetrical change in both voltage drop and charge/discharge duration (see Appendix E-16c & E-16d), between the cells. In both cells, the initial response duration is about 380 cycles and after 28,405 cycles, the test completed the response in about 290 secs. The voltage drop of both cells after 28,405 cycles increased from about ±0.05 of 0.17V of the initial value to ±0.05 of 0.36V.

6.3.2.3 Cyclic Voltammetry Test Results (CV)

In Appendix E-17a & E-17b, cell sample MtA after 1152H of accelerated tests showed a smaller surface area within the CV curve, compared to its consecutive cell MtB. The difference in CV shape between the cells indicates that each cell ages differently, with more voltage drop, observed in MtA's cell capacitance than MtB's cell capacitance despite the balancing circuit between the cells.

In Appendix E-17, module samples MtC & MtD after 1152H had shown each cell performing cyclic voltammograms test at the same rate. A small but noticeable change in shape size and the drop in current as the CV curve approached the rated voltage 2.7 after 1152H was observed in the test. Being that samples MtC & MtD make up the serial module and the cycling tests were carried-out at the same time, it was not farfetched to expect the module cells to age at the same rate. Thus, the module samples having similar capacitance value.

6.3.3 Capacitance and ESR comparisons

This section of the chapter studied the cycling effect on SCs with emphasis on the importance of balancing circuits in respect to their capacitance and ESR EOL criteria. Set- up 2A samples W5, W6, B7, B8, C9 and C10 in Figure 6-17a and 6-17b shows the normalised percentile of their capacitance and ESR values over the accelerated tests duration.

The percentile value of sample module W5 and W6's capacitance and ESR after 864H as shown in Figure 6-17a and 6-17b sample module W5 and W6 did not reach the EOL line. Although the actual duration of the test was 1008H, which showed a sudden drop in capacitance and increase in ESR after the 1008th hour. The change in capacitance and ESR was so low and high respectively that it could not fit into the graph. Nevertheless the ESR and capacitance values clearly surpassed the EOL line, thereby considered as failed cells.

Modules B7&B8 and C9& C10 exceeded the capacitance EOL mark as shown in Figure 6-17, with module B7&B8 ageing throughout at marginal proximity to each other,

while module C9&C10 aged at slightly different rates to each other, but completed the ageing process after 1008H at the same time recording a 78% loss of capacitance.

The ESR of module B7&B8 seemed to have also aged at proximity to each other (Figure 6-17b), except at 864H when the B7 spiked a bit but came around at bout 1152H to record an equal 205% increase in both cells. Module C9&C10 similar to the capacitance result, presented their ESR ageing at different rates, with C9 after 1008H crossing the EOL mark at 204% increase in ESR while C10 remained below the EOL line recording an increase of 176% in ESR.

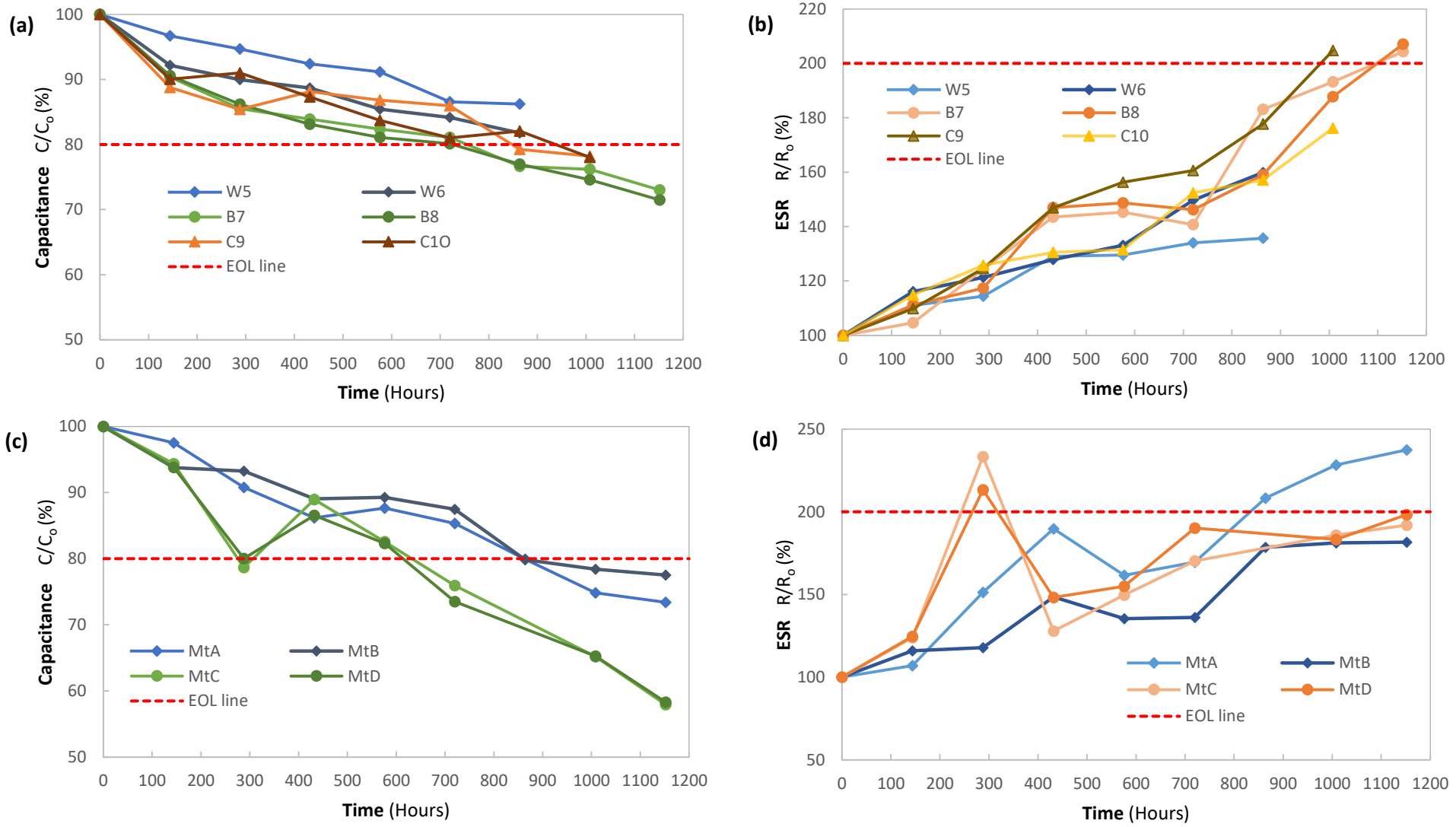


Figure 6-17: Comparing SC set-up2 samples' normalised parameters through their degradation stages: (a) C/C_o capacitance normalised its initial value (set-Up 2A), (b) R/R_o resistance normalised to its initial value (set-Up 2A), (c) C/C_o capacitance normalised its initial value (set-Up 2B), (d) R/R_o resistance normalised to its initial value (set-Up 2B)

Set- up 2B samples MtA, MtB, MtC and MtD EOL criteria in capacitance and ESR were not reached at the same time. In fact, the majority of the samples did not even reach the ESR EOL criteria. In addition to comparing EOL criteria (that is the 20% loss in capacitance and/or 100% increase in ESR) between module samples MtA & MtB and MtC & MtC, ageing proximity between the cells in each module was also a huge concern, given that, the study was based on how effective the balancing circuits were at equalizing the voltages within the module.

In Figure 6-17c, both MtC & MtD reached their 20% loss in capacitance after 720H. Although at 288H, a large drop in capacitance was noticed from 93% to 78%, which quickly recovered after 432H to 88% capacitance mark. This unusual drop at the 228H mark could be related the load delay observed in the “voltage equalisation circuit 1”. The proximity between MtC and MtD normalised capacitance was shown to be marginal, that after 1152H both cells’ capacitance aged equally reading a 58.3% loss of capacitance. Meanwhile, the ageing proximity between MtA and MtB’s normalised capacitance seemed to be a bit apart from each other, where MtA recorded a 74.3% loss in capacitance while MtB recorded a 77.5% loss in capacitance after 1152H. However, a 20% loss in capacitance for both cells were observed at the same time, after 560H mark.

In Figure 6-17d, MtA crossed over the 100% EOL line just after 860H, and after 1152H reached the 237.4% mark while MtB remained below the line at an 181.6% increase in ESR. Meanwhile, MtC and MtD increased steadily through out the test, except for the spike observed at the 288H mark which crossed the EOL line, but then elapsed by the next periodic characterization. Both cells after 1152H test duration did not reach the ESR EOL criteria, instead aged at the same percentile.

6.3.4 SET-UP 2: Ageing models

The effect of cycling on SC ageing is demonstrated using an ageing model generated to fit all set-up 2 samples irrespective of each SC modules behaviour. Five sets of SC modules were tested in set-up 2 to evaluate the effect of ageing in respect to voltage balancing between the cells in a module during charge/discharge cycles. Characterization results above have extensively shown the importance of a balancing circuit especially in module samples W5&W6 where both cells abruptly failed (with no charge) just after 1008H of testing, as a result of that, an ageing model was not generated. Although since all samples in set-up 2 could be modelled with the same ageing model, it is safe to say that it could also apply to samples W5&W6 before their sudden demise.

On the other hand, a single ageing model was generated to embody ageing sample modules B7&B8, C9&C10, MtA&MtB, MtC&MtD. Although the ageing model embodied all four modules, it was able to do so at different ageing stages with different electrochemical parameter values. The ageing model seemed to be viable (after the cells have reached either one or both of the EOL criteria) for B7&B8 after 720H, for C9&C10 after 846H and both MtA&MtB and MtC&MtD after 720H. It should also be noted that the transition from the initial model to the ageing model was in correlation to the semicircle formation in the impedance spectrum.

To explain the cycling ageing model in all the cell samples, cell C9 impedance response at 1008H was selected for simplicity (Figure 6-18a) to describe the electrochemical processes; that demonstrates the diffusion process in aged SCs.

The high-frequency intercept (10kHz) corresponds to the value of the ohmic resistance, R_{Ω}. This resistance is usually related to the resistance from current collector, electrolyte and separator. The second electrochemical process is the contact resistance between electrode and current collector, marked by a semicircle at frequencies between 10kHz to 140Hz. The semicircle was drawn with a circuit consisting of a parallel connection resistor R_P and a CPE. The third process which occurs between frequency 140Hz and 1Hz shows the transition from the semicircle to a more capacitive region as frequency decreases and this response is pertaining to the diffusion effect. The U-bend at the low frequency part has the form of a semi-infinite diffusion layer which represents a parallel connection of resistor R and Warburg element W. As the frequency decreases, the Warburg behaviour becomes more capacitive. The non-vertical line of the low frequency part shows what is known as an asynchronous charging (Fletcher et al., 2013). Nonetheless, the transition from the semi-infinite diffusion to a capacitive behaviour can only be modelled with a bounded diffusion element T.

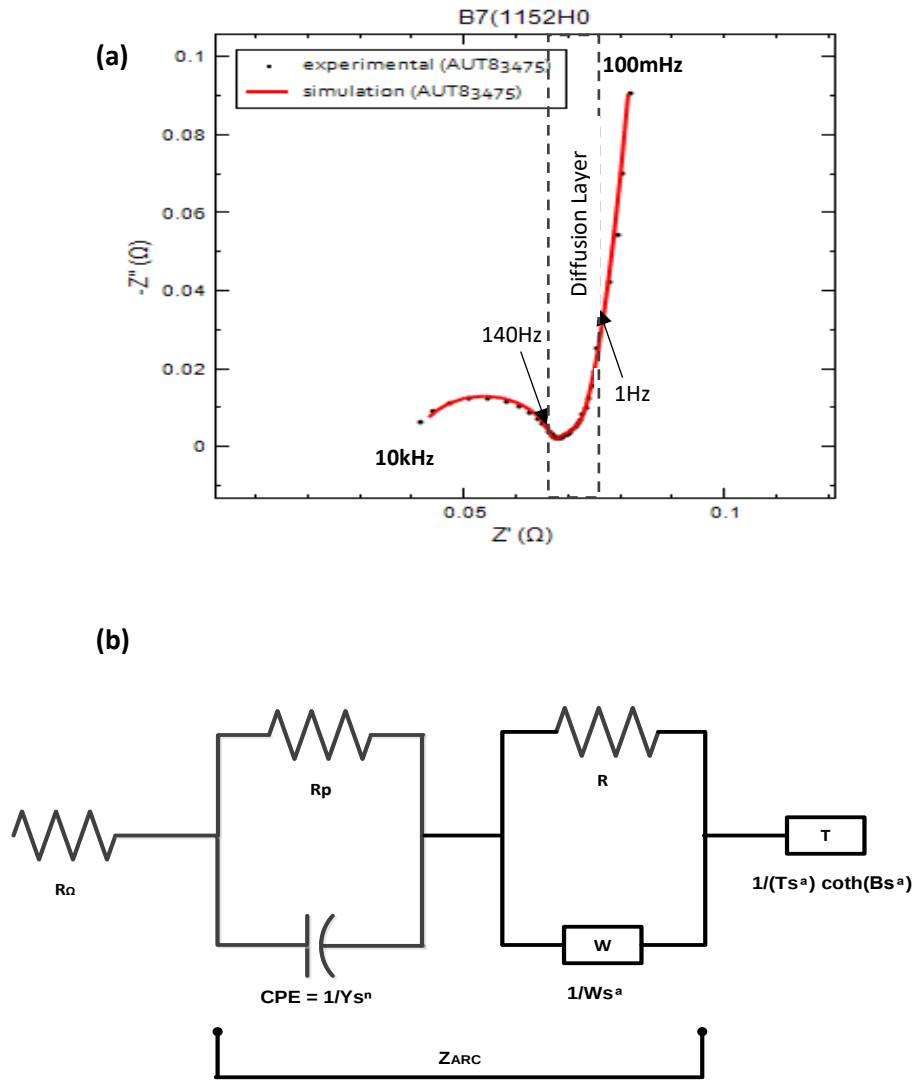


Figure 6-18: Impedance spectrum of aged C9 after 1008H under charge/discharge cycle test: (a) experimental (dotted line) and simulated (red line), (b) cycling ageing EEC model used to simulate the impedance spectrum (and all set-up2 SCs)

Since each SC module was connected in series for the accelerated tests, after completing the tests, a cell from each module was modelled to record the EEC circuit component values as summarised in Table 6-9 along with its chi-square, x^2.

Components (units)		***Fitted Value***							
		Ageing model ***C9 (1008H)***		Ageing model ***B7 (1152H)***		Ageing model ***MtB (1152H)***		Ageing model ***MtD (1152H)***	
		Values	Errors (%)	Values	Errors (%)	Values	Errors (%)	Vales	Errors (%)
$\boldsymbol{R_\Omega}$ *(Ω)*		0.046	1	0.0406	1.27	0.0592	0.73	0.0666	1.87
$\boldsymbol{R_p}$ *(Ω)*		0.0256	2.16	0.0253	2.43	0.00637	8.09	0.0159	9.78
$\boldsymbol{R}$ *(Ω)*		2.790	-	2.030	-	3.823	-	2.820	-
$\boldsymbol{CPE}$	Y (mho)	0.00343	-	0.00329	-	0.0214	-	0.0649	-
	n	1.01	1.75	1.015	1.99	0.975	6.52	0.731	7.92
W	*W* (mho)	68.7	6.45	78.5	10.20	102	7.18	70.4	5.82
T	T (mho)	50.4	9.75	40.38	8.93	57.9	9.67	66.77	23.33
	B	0.397	8.74	0.497	7.47	0.352	8.94	0.259	22.78
$\boldsymbol{x^2}$		2.7335×10^{-3}		4.615×10^{-3}		2.086×10^{-3}		2.3173×10^{-3}	

Table 6-9: EEC circuit parameters of ageing models C9, C10, MtB and MtD

The ageing model is made up of a serial combination of a resistor, a bounded diffusion element T and a complex impedance Z_{ARC}. The Z_{ARC} consists of a parallel combination of a CPE and a resistor R_P and a parallel combination Warburg element W and a resistor R.

The ageing model $Z(s)$ in s plane is thus;

$$Z(s) = R_\Omega + \frac{R_p}{1 + Y_1 s^n} + \frac{R}{1 + W s^a} + \frac{\sqrt{1 + (Bs^a)^2}}{TBs^{2a}} \quad (6.15)$$

Where, a is 0.5 and n was determined from CNLS fitting.

Expanding and arranging equation (6.15) yields the FOTF transfer function of $Z(s)$ in the form of,

$$Z(s) = \frac{V(s)}{I(s)}$$

$$\frac{As^{am} + Bs^{bm} + Cs^{cm} + Ds^{dm} + Es^{em} + Fs^{fm} + Gs^{gm} + Hs^{hm} + Is^{im} + Js^{jm} + Ks^{km} + Ls^{lm} + Ms^{mm} + Ns^{nm} + Os^{om} + Ps^{pm} + Qs^{qm}}{Rs^{rn} + Ss^{sn} + Ts^{tn} + Us^{un}} \quad (6.16)$$

Where, the coefficients of the transfer function and their circuit parameters are given in Table 6.10 and Table 6-11.

6.3.4.1 Ageing Model Validation

The ageing model (Figure 6-18b) developed due to cycling effect in SCs was simulated in MATLAB, FOMCON toolbox using equations (6.16) as the fractional transfer function block-set provided in FOMCON SIMULINK library. Before the simulation was carried out, the impedance transfer function $Z(s)$ (6.16) (substituting the circuits component values presented in Table 6-9) was first vetted with a stability test using the stable function in the FOMCON FOTF viewer to determine if the transfer function is feasible for simulating the aged samples. Figure 6-19 presents the stability results of SC B7, C9, MtB and MtD aged cells, which shows all the poles located in the stable area with a stability function $K = 1$, indicating the aged transfer functions are stable as shown in Table 6-12 with additional stability test parameters and their RMSE simulated voltage response.

Transfer function coefficients	
$A = 1$	
$B = \sqrt{2RW}$	$b_m = \frac{a}{2}$
$C = RW + B$	$c_m = a$
$D = \sqrt{2R_p WB^2}$	$d_m = \frac{3a}{2}$
$E = TR_\Omega B + BWR_p + TBR_p + TBR$	$e_m = 2a$
$F = \sqrt{T^2 {R_\Omega}^2 R^2 B^2 W^2 + 2T^2 B^2 W^2 R^2 R_\Omega R_p + T^2 B^2 W^2 R^2 {R_p}^2}$	$f_m = 3a$
$G = \sqrt{2YR_p}$	$g_m = \frac{n}{2}$
$H = R_p Y$	$h_m = n$
$I = \sqrt{4R_p RYW}$	$i_m = \frac{a+n}{2}$
$J = \sqrt{2R_p B^2 Y + 2R_p R^2 W^2 Y}$	$j_m = \frac{2a+n}{2}$
$K = \sqrt{2{R_p}^2 RY^2 W}$	$k_m = \frac{a+2n}{2}$
$L = \sqrt{4R_p RWYB^2}$	$l_m = \frac{3a+n}{2}$
$M = \sqrt{2{R_\Omega}^2 RWB^2 Y^2}$	$m_m = \frac{3a+2n}{2}$
$N = \sqrt{2R^2 R_\Omega W^2 B^2 Y}$	$n_m = \frac{4a+n}{2}$

Table 6-10: Set-Up2: Transfer function coefficients according to the aged model circuit parameters presented in Figure 6-18a

Transfer function coefficients	
$O = R_p BY + RR_p WY$	$o_m = a + n$
$P = \sqrt{T^2 {R_\Omega}^2 {R_p}^2 B^2 Y^2 + 2T^2 B^2 Y^2 R_\Omega R_p + T^2 B^2 Y^2 R^2 {R_p}^2 + W^2 B^2 Y^2 R^2 {R_p}^2}$	$p_m = 2a + n$
$Q = TBWYR_\Omega RR_p$	$q_m = 3a$+n
$R = TB$	$r_n = 2a$
$S = TBWR$	$s_n = 3a$
$T = TBYR_p$	$t_n = 2a + n$
$U = TBWYRR_p$	$u_n = 3a + n$

Table 6-11: Continuation… Set-Up2: Transfer function coefficients according to the aged model circuit parameters presented in Figure 6-18a

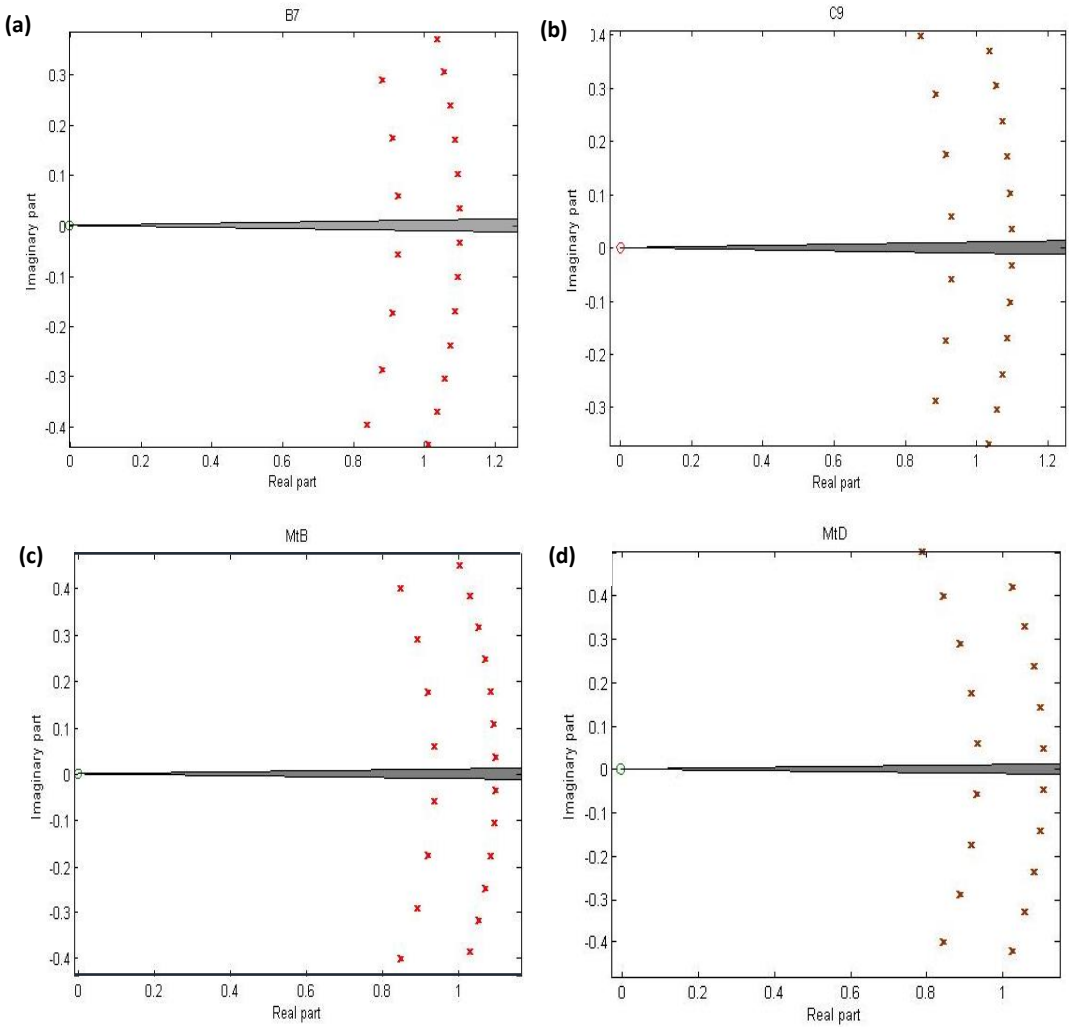


Figure 6-19: FOTF Stability test results of aged cells (a) B7, (b) C9), (c) MtB and (d) MtD using the parameters in equation (6.16)

Stability Test Parameters	B7(1152H)	C9(1008H)	MtB(1152H)	MtD(1152H)
K	1	1	1	1
q	0.0100	0.0100	0.0100	0.0100
ERROR	0.3772	0.3012	0.4105	0.1237
APOL	0.0311	0.0311	0.0324	0.0430
Voltage profile (RMSE)	0.0987	0.0859	0.0596	0.0688

Table 6-12: FOTF Stability test results with emphasis on the parameter accuracy of the transfer functions, including the RMSE results between the simulated and experimented voltage response

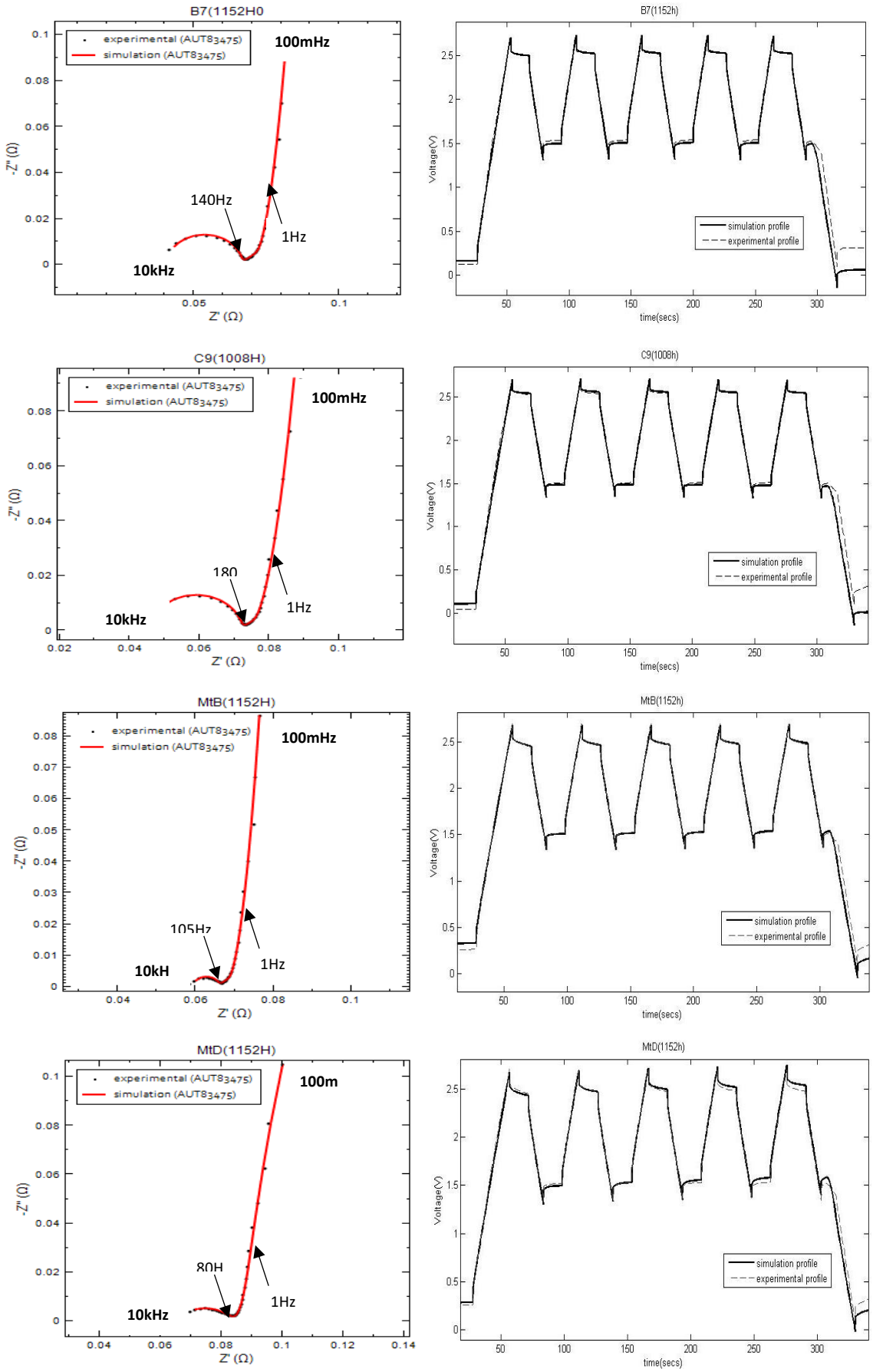


Figure 6-20: Validation test of B7, C9, MtB and MtD ageing models in their impedance spectrum (simulated data on red solid lines and the experimental data on black dotted lines) and their voltage response using a 2A current profile (simulated data on solid lines and the experimental data on dash lines).

The ageing models were simulated to output a voltage response according to the relation presented in (6.14). Figure 6-20 shows the simulated frequency and voltage response of the ageing model given a satisfactory fit at both frequency and voltage responses confirmed by the chi-square, x^2 values generated in the frequency domain (see Table 6-9) and the RMSE values calculated from the voltage responses (see Table 6-12) .

6.4 SET-UP 3: Effect of Supercapacitor module on system performance during variable load profiles (Charge/Discharge tests) under high-temperature conditions

Set-Up 3 is made up of three SC samples A;B;C (rated at 8.1V) subjected to accelerated charge/ discharge tests with the SC module discharged to a programmable motor load under a 85^{o}C temperature chamber. Unlike Set-Up 2 where the charge/discharge tests carried out were focused on the voltage balancing circuitry, Set-Up 3 in addition to SC module voltage management, emphases on the module's endurance during discharge phases where the module is forced to power the DC motor load generating pulsed waveforms (profiles). The load conditions programmed (using the set-Up in Figure 4-15), were to vary the SC module and load voltage creating a diverse operating environment based on acceleration/braking or start/stop drive cycle operations in HEV. Four selected load voltage profiles as shown in Table 6-13 were applied to the module discharge phase, starting with load profile

1 all the way to load profile 4. Module samples A;B;C were tested over a period of 4 weeks, with four 144H test phases and a 24H break between test phases.

Each 144H test duration was assigned to the SC module voltage profiles (as shown in Table 4-5, voltage profiles 6-9) with their selected load profiles (seen in Table 6-13).

The charge/variable load discharge tests were carried out until either one or all the three end-of-life criteria stated above is reached.

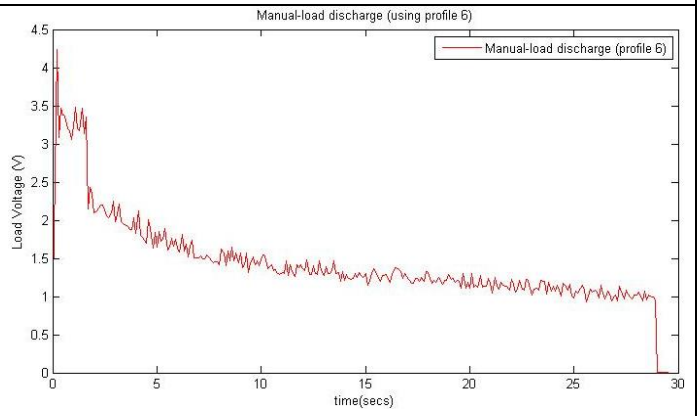
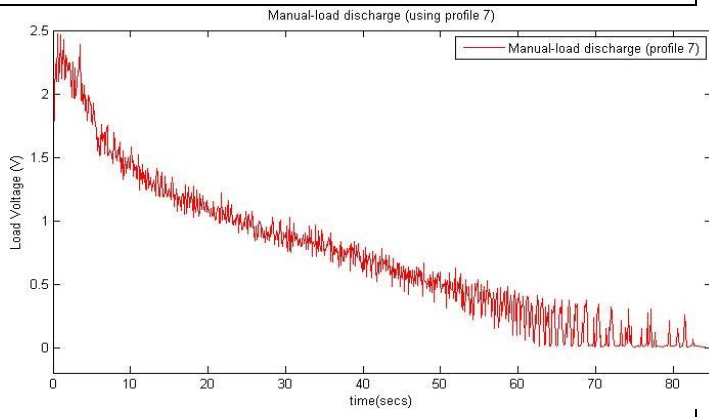
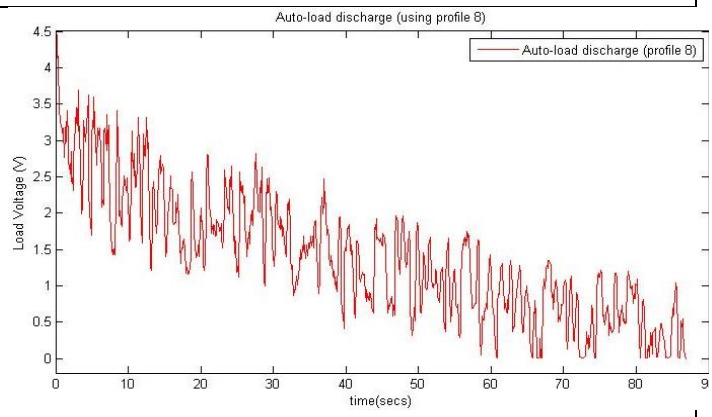
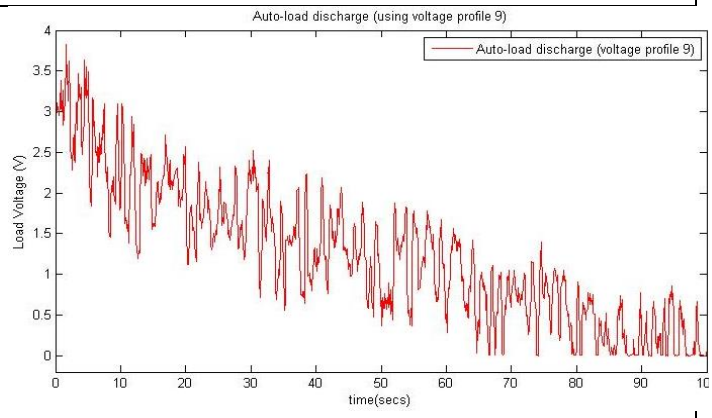
Discharge Load selection	Motor-Load Discharge profile
Load Profile 1 • Manual speed selection • Applied from SC voltage 8.1V to 7V (see profile 6 in Table 4-5) • Maximum load speed selected starting at 5V	
Load Profile 2 • Manual speed selection • Applied from SC voltage 8.1V to 5V (see profile 7 in Table 4-5) • Maximum load speed selected starting at 2.5V	
Load Profile 3 • Auto speed selection • Applied from SC voltage 8.1V to 4V (see profile 8 in Table 4-5) • Random load speed fluctuating between voltage 5-0V, to generate peaks	
Load Profile 4 • Auto speed selection • Applied from SC voltage 8.1V to 2V (see profile 9 in Table 4-5) • Random load speed fluctuating between voltage 5-0V, to generate peaks	

Table 6-13: 12V DC Motor variable discharge load profiles performed in set-up 3 experimental tests

6.4.1 Electrochemical Impedance Spectroscopy Test Results (EIS)

Appendix E-18 to Appendix E-20 shows the impedance changes during charge/discharge tests at 85℃ at different stages of SC life. A total of 576H accelerated test period was subjected to module samples A;B;C.

Appendix E-18a, E-19a and E-20a, shows the impedance (Nyquist plot) changes in A, B and C, respectively in three forms: (1) movement of the impedance spectrum along the real axis, (2) emergence of a semicircle replacing the 45° slope line and a continual expansion of the size and diameter of the semicircle as ageing progresses (which seemed to be more obvious in all three cells at 576H. These changes occurred in a similar manner and almost at the same time with little to no difference in each cell. (3) A slight inclination of the low-frequency part to the right was also observed as the ageing progressed.

As the ageing tests progress, the more inclined the spectrum at low-frequency gets, which in turn decreases the slope at the low-frequency part of the impedance spectrum. The decreasing slope of the low-frequency tail of the impedance spectra of cells A;B;C are directly translated into the drop of capacitance after 576H, as visible in the capacitance vs. frequency plot (Appendix E-18b, E-19b and E-20b). The capacitance initially stands at 21F (at 100mHz) for all three cells, but after 576H of accelerated tests, the capacitance of the cells dropped to 16F (on all three cells).

Z' increases as frequency decreases. A curvature distortion (in correlation to the emergence of the semi-circle observed in the Nyquist plots) was observed at 432H and 576H in all three cells. At 576H, the distortion starts at 100Hz after a gradual

decrease of Z' at the beginning and quickly plunges between 100Hz to 10kHz (as seen in Appendix E-18c, E-19c and E-20c).

The semi-circle causes distortion not only to the impedance real part but also to the Phase vs. Frequency plot. The distortion is described as a hump, which appears to be more prominent after 576Hs of testing (refer to Appendix E-18d, E-19d and E-20d).

6.4.2 Constant Current Test Results (CC)

Appendix E-21 shows the voltage responses of module cells A;B;C. The cells after 576H of test duration showed equal changes in voltage drop and charge/discharge duration. The cells initial response duration is about 380 cycles and after 576H, the test completed the response in about 332 secs. The decrease in charge/discharge time over accelerated tests time is due to the voltage drop witnessed, before and after the 15secs open circuit just after charging and also after discharging. The voltage drop which also represents the cell's ESR (see Equation 5.8) increases as the ageing process continued recording a 0.185V boost after 576H, compared to its initial voltage drop of 0.142V at 0H.

Module cells A;B;C throughout the experimental period maintained a gradual and symmetrical change among the three cells in both voltage drop and charge/discharge duration.

6.4.3 Cyclic Voltammetry Test Results (CV)

Appendix E-22 show cyclic voltammograms at the initial and final stages of SC samples A;B;C. The shape of CV curves of all the cells at the initial stage are almost rectangular, but as they age they exhibit changes in the form of a leaf-shaped (distorted) waveform. After 576H, given samples were made-up of a serial module with voltage management circuitry, it was not implausible to expect the module cells to age at the same rate. Thus, the module samples having similar capacitance value. The narrowing of the CV waveshape indicates the decrease in cell capacitance, which also relates to the reduction in charge Q (i.e. the area between the CV curves).

6.4.4 Capacitance and ESR comparisons

The loss of capacitance and the increase in ESR in aged SC samples A;B;C are compared in Figure 6-21. The capacitance and the ESR are calculated based on Equations (5.7) and (5.8) from the constant current test. It was found that the end-of-life (EOL) criteria for both capacitance and ESR are not reached at the same time, in fact, ESR 200% EOL criteria was not achieved in the given test time frame of 576H.

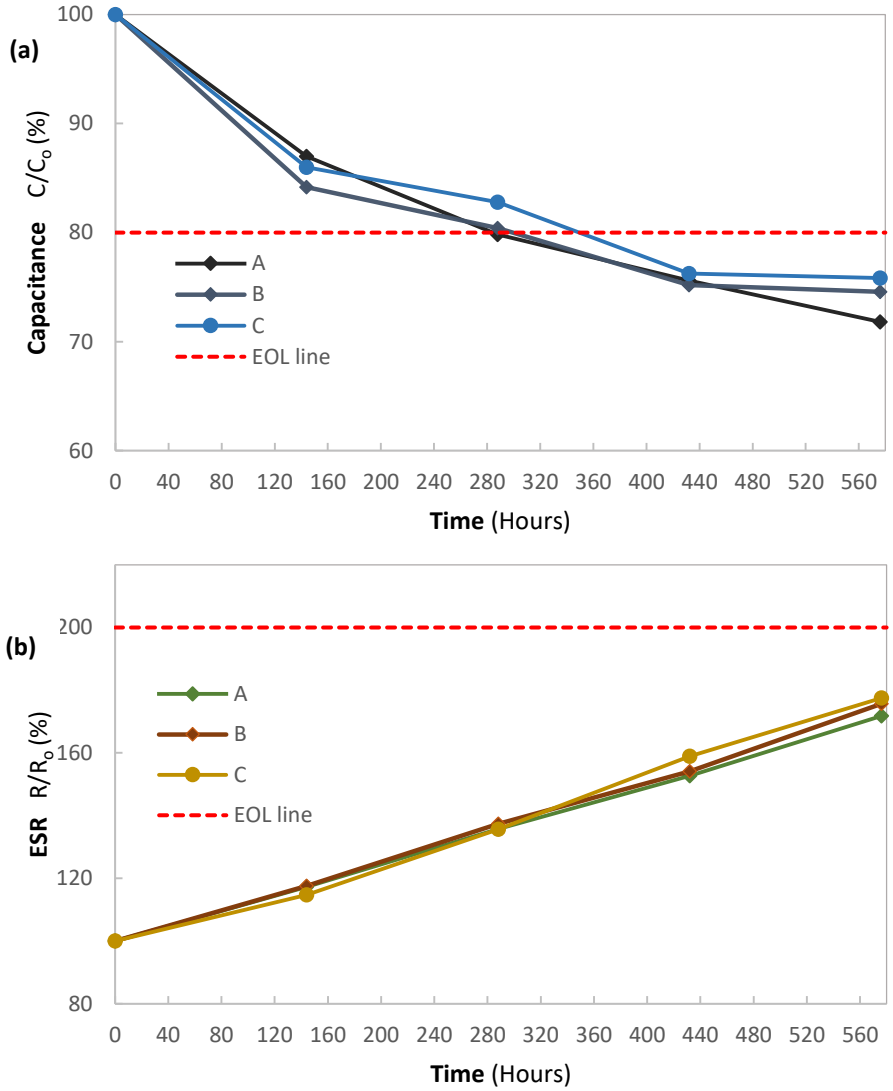


Figure 6-21: Comparing SC set-up3 samples' A;B:C normalised parameters through their degradation stages: (a) C/C_o capacitance normalised its initial value, and (b) R/R_o resistance normalised to its initial value

Figure 6-21a shows samples A;B;C normalised percentile of their capacitance values over the accelerated tests duration. Moreover, all three samples exceeded capacitance EOL 80% percentile a few test hours after the second periodic characterization (after 288H), it was observed that samples A and sample B reached the 80% percentile at the same time, with sample C just a few hours behind them. After 576 hours of testing and apparent loss of capacitance, the experiment came to a halt with a 72% loss in sample A, a 74% loss in sample B and a 75% loss in sample C. The ageing proximity between the cells seemed to adjacent to each other, with cell A leading because it was positioned closest (in the module) to the power source.

Figure 6-21b shows samples A;B;C the normalised percentile of ESR values over the accelerated tests duration. As seen, all three cells did not reach the 100% ESR EOL criteria after 576H of testing, but steady increase in ESR at marginal proximity to one another was observed among the cells as the experiment proceeded recording a 177% increase in all three cells by the end of the experiment.

6.4.5 SET-UP 3: Ageing models

The ageing model created from set-up 3's aged cells is similar to that of set-up 2 (see Figure 6-18b). Although they possessed different operating and environmental conditions, they were both subjected to similar charge/discharge cycles. For the cells ageing response in set-up 3 to satisfy the developed cycling ageing model, cell 'A' impedance response at 576H was used (represents all three cells to prevent repetitive results, since their ageing parameters (as seen in Figure 6-21) aged similarly) to simulated similar response using the cycling ageing model in Figure 6-18b.

Although the ageing model developed to describe the effect of ageing in SC module is similar as demonstrated with set-up2 and set-up3 cell samples, the impedance response of cell 'A' of set-up3 showed a more pronounced distortion at the medium frequency between 74HZ and 1Hz. The distortion, which emulates a charge transfer reaction, which is likely to occur due the increase of the distributed resistance, as seen in experiments with elevated voltages. This ageing phenomenon is interpreted in the cycling ageing model with a parallel connection of a resistor R and a Warburg element W

Since the module consists of cells A;B;C connected in series, all three cells from the module was modelled to record the EEC circuit component values as summarised along with its chi-square, x^2 in Table 6-14.

Components ***(units)***		***Fitted Value***					
		Ageing model ***A (576H)***		Ageing model ***B (576H)***		Ageing model ***C (576H)***	
		Values	Errors (%)	Values	Errors (%)	Values	Errors (%)
$\boldsymbol{R_\Omega}$ *(Ω)*		0.050642	0.69	0.05365	0.64	0.04969	0.60
$\boldsymbol{R_p}$ *(Ω)*		0.005324	7.30	0.004073	9.77	0.003035	11.98
$\boldsymbol{R}$ *(Ω)*		2	-	2	-	2	-
$\boldsymbol{CPE}$	Y (mho)	0.01914	-	0.04282	-	0.06207	-
	n	1.01	4.95	0.9787	7.31	1.005	9.60
$\boldsymbol{W}$	W (mho)	103.09	5.29	101.06	5.64	102.65	6.83
$\boldsymbol{T}$	T (mho)	41.781	3.89	43.136	4.64	41.415	5.17
	B	0.453	3.34	0.4315	4.07	0.4381	4.49
$\boldsymbol{x^2}$		1.0519×10^{-3}		1.2463×10^{-3}		1.9138×10^{-3}	

Table 6-14: EEC circuit parameters of ageing models A;B;C

6.4.5.1 Ageing model validation

Similarly, the cycling ageing model (Figure 6-18b) was simulated in MATLAB, FOMCON toolbox using equations (6.16) as the fractional transfer function block-set provided in FOMCON SIMULINK library. And a stability test for cell 'A' was carried out using the component values of Table 6-14. Figure 6-22 presents the stability results of aged cell 'A', which shows the poles located in a stable area with a stability function $K = 1$, indicating the aged transfer functions are stable as shown in Table 6-15 with additional stability test parameters and their RMSE simulated voltage response.

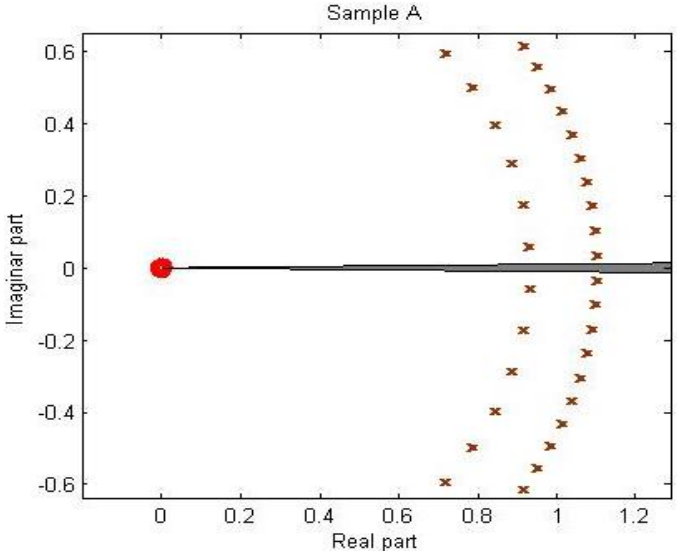


Figure 6-22: FOTF Stability test results of aged cells A using the parameters in equation (6.16)

Stability Test Parameters	A(576H)
K	1
q	0.0100
ERROR	0.01548
APOL	0.0317
Voltage profile (RMSE)	0.0392

Table 6-15: : Cell 'A' FOTF Stability test results with emphasis on the parameter accuracy of the transfer functions, including the RMSE results between the simulated and experimented voltage response

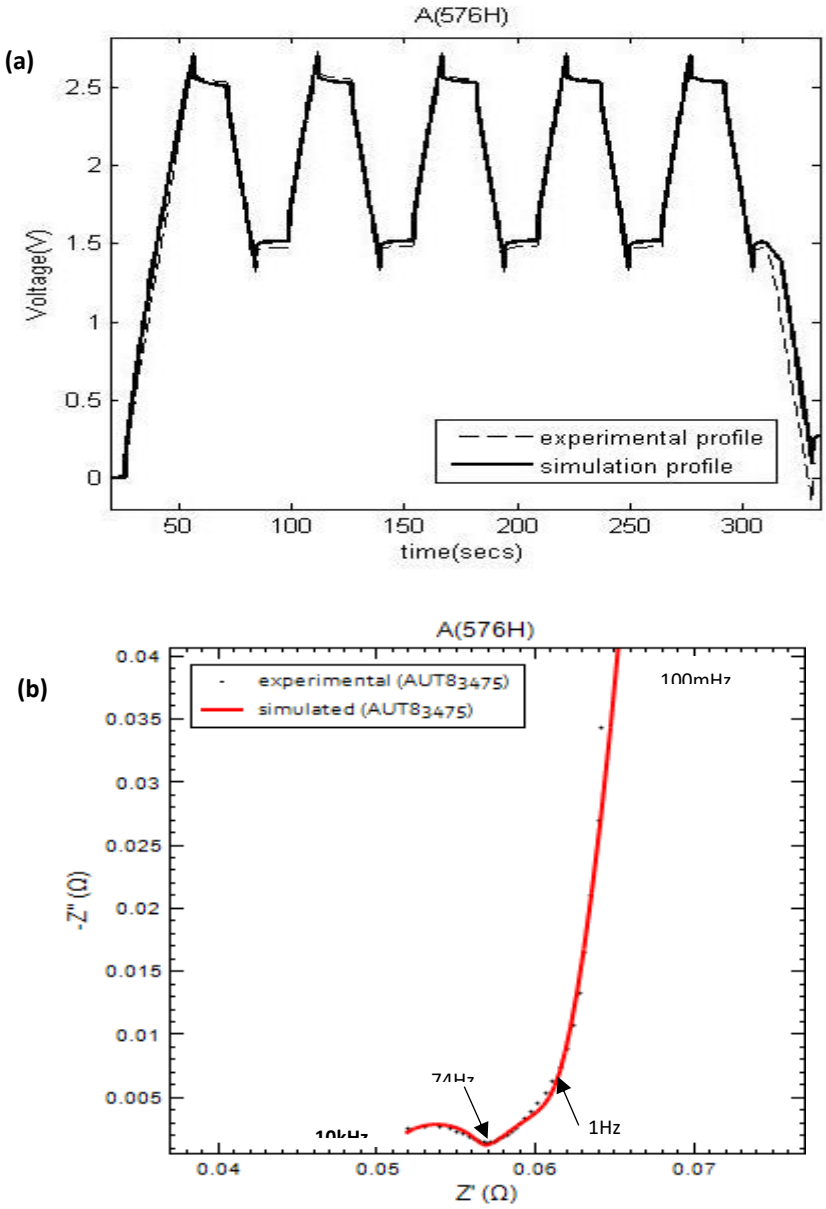


Figure 6-23: Aged cell A validation test of cell A (a) Voltage response using a 2A current profile (simulated data on solid lines and the experimental data on dash lines) (b) Impedance spectrum (simulated data on red solid lines and the experimental data on black dotted lines).

Figure 6-23 shows both the impedance and voltage response simulated by aged cell 'A'. Both responses simulated satisfactory fit at both frequency and voltage responses confirmed by the chi-square, x^2 values generated in the frequency domain (see Table 6-14) and the RMSE values calculated from the voltage responses (see Table 6-15) .

6.5 Discussion

This chapter showed the effect of SCs under various operating conditions categorised by three set-ups:

1. **Set-Up 1:** Studying the effect of SC cells under voltage and temperature stress factors; which were subdivided to include:
    1. High temperature test
    2. Constant Voltage (at 2.7V, 20^{o}) and
    3. Calendar test (at 27V, high temperature)
2. **Set-Up 2:** Studying the effect of SC modules with and without voltage equalization circuits during constant current charge/discharge tests (with and without a load), under high temperature; divided into:
    4. SC module of two cells connected in series under cycling test at high temperature
    5. 2 SC modules of two cells each connected in series (by different voltage equalisation circuits) under cycling test at high temperature
    6. 2 SC modules of two cells each connected in series (by two different voltage equalisation circuits) with a motor attachment at the load, under cycling test at high temperature
3. **Set-Up 3:** Studying the effect of SC module during variable load profile (charge/discharge tests) under high temperature; i.e.
    7. 3 SC modules of two cells each connected in series (by different voltage equalisation circuits) with a programmable motor attachment at the load, under varying cycling test at high temperature

The findings in this research showed, six of the seven conditions presented above exhibited at least one mode of SC failure characterized as; (1) 20% loss from the initial capacitance, (2) 100% increase in ESR, (3) Cell opening due to the build-up of pressure in the cell and/or (4) open/short circuit. Therefore, these four failure modes were periodically monitored during the course of the accelerated tests, however ESR and capacitance (the first two EOL criteria) where the main focus, because the other two EOL criteria could occur only if and when SC cells had already exhibited, both loss in capacitance and increase in ESR beyond reproach. Thus, ageing in SC was quantified by periodic calculations of ESR and capacitance values from charge/discharge test, in addition to the changes observed in the electrochemical behaviours at the impedance spectra and the cyclic voltammograms characterization tests.

SC sample M3 Constant Voltage (at 2.7V, 20^{o}) test, was the only test condition to have very little effect on SC ageing. The possible explanation for these results could be that the tests were carried out at a temperature that had very little influence on the cell properties. According to the rule of thumb, the ageing rate doubles if either the SC voltage is increased by 100mV or the temperature is increased by 10K (Bohlen et al., 2007a) (Uno & Tanaka, 2012), thereby suggesting, the ageing tests are governed by voltage and temperature. For that reason, the fact that sample M3 did not reach any EOL criteria after 2592H of testing (as seen in Figure 6-7) indicated that temperature is the dominant of the two ageing factors. This assumption is fuelled by the results obtained from M4 under similar constant voltage conditions as M3 but subjected to a high-temperature environment.

Nevertheless, the effect of high-temperature test, calendar test, and cycling tests (conditions 4 to 7) on SC were clearly quantified by the failure modes; ESR and capacitance in concurrence to the electrical and electrochemical changes observed during the characterization tests. During the ageing quantification of the SC cells, the changes observed during EIS, CC and CV tests were shown to have directly influenced the rate at which capacitance declined and the ESR increased during ageing tests, as summarised in Table 6-16.

AGEING MODES	CHARACTERIZATION TESTS		AGEING MECHANISMS
Increase in ESR	Electrochemical behaviour	EIS Tests	• A shift of the impedance spectrum along the real axis, or • An emergence and continual growth of a semicircle in the impedance spectrum at high frequency, or • A visible (arc-like) bump in impedance spectrum at medium frequency, or • A change in the slope of the imaginary part of the impedance spectrum at low frequency
		CV Tests	• Change and narrowing of the cyclic voltammograms wave-shape
	Electrical behaviour	CC Tests	• Voltage drop between charge/ discharge or discharge/charge
Decrease in Capacitance	Electrochemical behaviour	EIS Tests	• An emergence and continual growth of a semicircle in the impedance spectrum at high frequency, together with a change in the slope of the imaginary part of the impedance spectrum at low frequency
	Electrical behaviour	CC Tests	• Reduced charge/discharge time

Table 6-14: Relationship between SC ageing modes and their ageing mechanisms using electrochemical and electrical behaviour

The shift of the impedance spectrum along the real axis present in all aged SC cells is related to the increase of ohmic resistance over time. The ohmic resistance has typically been ascribed to the sum of the resistance contributions from the electrolyte, separator, current collector and electrode material and thickness (Masarapu et al., 2009). Therefore, the movement of the real part of the impedance along the real axis shows that the ageing process in SC increases the resistance of the SC's internal components.

From the impedance ageing test results, a semicircle has consistently appeared at high frequency in all test where high temperature stress was present. As the ageing in the cells progressed, the semicircle matured in both circumference and base diameter especially in the case of cell T2 (high-temperature condition) while the increase in only base diameter was observed in cell M4 (calendar test condition). The appearance of the semicircle is associated with an increase in contact resistance between the electrode and the current collector (Kötz, Ruch, & Cericola, 2010) and an increase in the distributed resistance in the electrode (Ruch, Cericola, Foelske-Schmitz, et al., 2010), which progressively increased with ageing. The appearance of semicircle has been reported by various researchers to be consistent with the formation of aluminium oxide and the delamination of the electrode from the current collector (Kötz et al., 2010). The crystallisation of AN electrolyte also gives rise to the formation of the semicircle in the complex plane at high frequency (Iwama, Taberna, Azais, Brégeon, & Simon, 2012). Also, (S. Zhang, 2010) and (Gaberscek et al., 2008) have demonstrated the effect of poor interphase contacts on the size of the semicircle.

Electrochemical parameters used in ageing models to imitate the appearance of semicircle at high frequency in all test conditions consists of a complex plane of parallel combination of a CPE and a resistor R_P. As the SC test samples age, the semicircle at high frequency increases in circumference, and this ageing phenomena is interpreted in the ageing models by decreasing the magnitude value of CPE with increasing circumference. This effect is seen in aged cell T2 with the largest semicircle circumference and the smallest CPE magnitude value, and in aged cell M4 with the smallest circumference with a larger CPE magnitude value (see Table 6-5). The parallel resistor R_P in the other hand, is translated to the semicircle base diameter (observed along the real axis of the spectrum), contrary to CPE's disposition, the resistor R_P was perceived to increase in value with increasing semicircle base diameter. This ageing mechanism is only observed in the condition where SC is exposed to high temperature, thus, reveals that this ageing mechanism is a product of long-term exposure to high temperature. Hence, when temperature is high, it affects the contact resistance in SCs.

In some cases, an extra bump appears at the medium frequency as seen clearly in the calendar test condition in cell M4. This ageing phenomenon though not thoroughly researched, is a similar response reported in (Ruch, Cericola, Foelske-Schmitz, et al., 2010) at elevated voltages, and at (Gaberscek et al., 2008) (a. Eddahech et al., 2011) in the study of interphase contacts in lithium ion electrodes. Nonetheless, the response emulates a charge transfer reaction, which is likely to occur due to the formation of corrosion products or may be related to the increase of the distributed resistance. This ageing phenomenon is interpreted in the ageing model consisting of a parallel connection of a resistor R and a Warburg element W. A Warburg element

W was used instead of a CPE, to imitate a semi-infinite diffusion layer aiming the bump on a $-\pi/4$ slope angle, forming an arc instead of a semicircle of a CPE at a slightly <90^{o} angle. Apart from aged cell M4, the bump observed in the medium frequency was also present in SC cells under all four cycling conditions. Although, the bump observed on aged cells under cycling conditions was smaller without load conditions than the systems with load attachments and possible hard to see from a full spectrum, it wasn't insignificant. Similar to the calendar test ageing model, the cycling condition in SCs at medium frequency is also modelled with a complex plane consisting of a parallel connection of a resistor R and a Warburg element W. Nonetheless, unlike aged cell M4 in which the Warburg element W magnitude value was small (indicating a large bump), the values in the cycling condition were very large compared to that of M4 (see Table 6-5). This ageing phenomena is associated to test conditions that includes the voltage stress factor, and as the voltage stress level increases, the ageing mechanisms becomes more pronounced.

The change in slope of the impedance imaginary part at low frequencies occurs in two forms, (1) reduction of slop and (2) tilting of the impedance line from its original response. This phenomenon is induced by mechanical stress on the electrode in which this ageing factor causes obstruction of the pores (El Brouji, Briat, Vinassa, Bertrand, et al., 2009)(Briat et al., 2010)(Amrane Oukaour et al., 2013), thereby modifying the electrode structure. Similar to the ageing mechanism observed at medium frequency, the change in slope at low frequency is only observed in the conditions where SC is exposed to cycling, constant voltage and calendar test (i.e. test conditions that include voltage stress factor);

On that note, this observation permits an interpretation that that this type of ageing mechanism is a result unique to applications involving repeated cycling or a long-term constant voltage on SCs.

The ageing phenomena witnessed at low frequency usually arise from a decrease of a constant phase exponent (Bohlen et al., 2007a)(Briat et al., 2010)(El Brouji, Briat, Vinassa, Bertrand, et al., 2009) modelled from a system that exhibits either infinite diffusion layer (CPE), semi-infinite diffusion (W) or finite length diffusion (T) (Juan Bisquert et al., 1999)(Raistrick et al., 2005). The constant phase exponent has been associated to inhomogeneity in the electrode, surface roughness and non-uniformity of the double layer thickness (Bohlen et al., 2007a), porosity and effective surface area (Briat et al., 2010), pore size dispersion (El Brouji, Briat, Vinassa, Bertrand, et al., 2009). The decreased of the constant phase exponent and the deviation from the capacitive behaviour suggest that there is a modification of the electrode structure—perhaps related to a change in pore size distribution as has been observed in (J. Song & Bazant, 2013).

Concerning the narrowing of the cyclic voltammograms on aged SCs during the CV test, the changes to the CV wave-shape shows that the capacitance reduces as SC ages since the charge Q is the area between the CV curves and capacitance decreases as Q decreases. This change to the CV waveshape has been associated to the modification of the chemical composition in the electrode surface in (El Brouji, Briat, Vinassa, Henry, et al., 2009). Additionally, this narrowing has also been related to the saturation of the active surface area of the electrode material by the stored ions which contributes to a fading of capacitive current (Ratajczak et al., 2013).

Briat et al. (2010) reported that a large amount of ions that flows during charging/discharging can affect the integrity of the porous electrode (Briat et al., 2010). This phenomenon is therefore observed in CC tests at the open circuit between charge/discharge or discharge/charge phases as voltage drop, affecting the porous behaviour of electrodes which also leads to the de-cohesion of some carbon particles, and consequently, gives rise to the ESR. It is evident though that ESR increased with increase in voltage drop. Change in capacitance is also observed in this characterization method, as charge/discharge phases decrease with time so does the capacitance rate. This behaviour provides a standardised method of calculating both ESR and capacitance values. Therefore, the reason some researchers opt for this method as the single technique of SC ageing quantification; (Lajnef, Vinassa, Briat, Azzopardi, et al., 2007) (Fletcher et al., 2014) (Rafik et al., 2007) (Lajnef, Vinassa, Azzopardi, Briat, et al., 2004).

In addition to using CC test method in determining ESR and capacitance values, researchers; (Ambade & Joshi, 2014) (Al-janad et al., 2014) (Dănilă et al., 2011) (Johansson & Johansson, 2008) including this research have experimented in CC modelling.

Another form of ageing mechanism (or failed mechanism) known as 'open circuit failure' is observed in the cycling test of two cells connected in series. Cells W5 and W6 characterization results showed a very drastic and sudden change in electrical and electrochemical behaviour.

Open circuit failure with its ESR rising to infinity is usually as a result of electrolyte loss over time (during high temperature or high voltage tests) and in some cases due to the lack of voltage management circuit in a system with more than one SC cell (Ltd,

2014). This ageing phenomenon is beheld after an astronomical increase in ESR and decrease in capacitance is present, in some cases, the cell loses its ability to store any charge or at most lessens the amount of energy being stored (as seen in module W5&W6.

During the ageing test, the build-up of pressure in the SC cell due to chemical reactions of AN-electrolyte with the ageing factor, causes the X-groove at the base of the casing to swell and eventually open up to allow the accumulation of gas inside the cell to escape, thus, preventing any explosion (Mohammad Naim, 2015). This "can opening" act, however, does not only swell but according to Mohammad Naim, (2015) also opens up when the internal of the cell experiences increasing overpressure with time. The electrolyte then leaks out from the cell and evaporates through the groove to form some residue. Although the analysis of the content of the gas is not conducted in this thesis, Ruch et al., (2010) and El Brouji, Briat, Vinassa, Henry, et al., (2009) have reported that the main gaseous decomposition product in $TEABF_4$/AN is CO_2. Azaïs et al., (2007) relates the emission of CO_2 to the binder decomposition. Nevertheless, consistent to (M. Zhu et al., 2008), the decomposition of electrolyte does indeed affect SC performance in two ways: first, the active material is irreversibly consumed, and second, it is due to gassing and blockage pores that give rise to the internal pressure within the cell.

Though a visible leakage of the electrolyte was not noticed in this research work, the evidence of can swelling at the X-groove casing was observed in tests under calendar and cycling conditions.

This study isolates ageing factors in SCs by relating ageing mechanism to their ageing modes and further interpreting them in ageing models. Studying the impact of each ageing factor individually have indeed enabled the identification of the ageing mechanism in relation to the ageing factor in SCs. Each ageing factor affects SC ageing differently depending on the level of stress the SC is exposed. Based on the results gathered here, Set-Up 1 test conditions proves temperature to be the dominant of the two ageing factors (i.e. temperature and voltage); while cycling (under high temperature conditions) have also proved to affect ageing in SC, the presence of load attachments aggravates ageing in SCs compared to cycling systems with non-attachments. Although, cycling in SC module as proven by set-up 2 is only possible with the presence of a voltage management system.

6.6 Summary

This chapter shows the effect of ageing in both single and module SCs under various operational and environmental conditions classified in the form of experimental set-ups. These set-ups were divided into three categories to tackle isolated ageing effects with set-up 1 limited to studying the effect of the predominant ageing factors temperature and voltage individually and together on single SC cells, while set-up 2 and set-up 3 studied the effect of cycling on SC modules under additional conditions consisting of temperature condition, voltage management circuits and load attachments with/without programmable functions. The ageing process and ageing mechanisms are identified in accordance with their ageing factors using CC, CV and EIS characterization test method. Not only does the results from this characterization methods aid in the identification of the cause of failure in SCs, but the results also show which ageing factor is dominant to SC ageing. Also, solutions can now be targeted individually based on which ageing mechanism is observed.

Electrical and electrochemical ageing mechanism seen in characterization tests, as shown in Table 6-16 in terms of ESR and capacitance ageing modes were used to quantify ageing effects in SCs. Although ageing mechanisms are specific to ageing factors (i.e. high temperature, constant voltage and cycling conditions), there are usually two identified ageing mechanisms in SCs: First, is the loss of contact with the electrode, which gives rise to the contact resistance. Second is the changes to the SC porous electrodes. While, the increase of contact resistance is always consistent to the effect from long-term exposure to high temperature, the changes to the SC porous electrodes is an effect from mechanical stress caused by long-term cycling and also the long application of constant voltage on SCs. In addition to the two

observed ageing mechanism, open circuit failure was also encountered during cycling in SC module, which is an aggravated form of both ageing mechanisms combined, due to the lack of voltage balancing system between the cells in the module.

This chapter not only quantifies ageing in SCs in terms of ageing modes, but it also went further to develop ageing models to imitate ageing behaviours specific to ageing factors.

It was observed during the accelerated test when the SC cells began to show signs of ageing (either a 100% increase in ESR or 20% decrease in capacitance) due to chemical reactions inside the cell; the initial model developed based on the cells original response was no longer suitable. Therefore, new models (ageing models) were created taking into account the new observed electrochemical processes representing the current state of health of aged SCs.

Since the ageing models were developed in the frequency domain using electrochemical components, the models took the form of fractional order for easy simulation. The ageing models were validated in the time domain with simulated voltage responses following the experimental response.

CHAPTER 7-CONCLUSION

7 Conclusion

This thesis has presented an accelerated test bench method on studying the ageing effects in supercapacitors. The main aim of this research was to study supercapacitor reliability under EV/HEV operating conditions drawn up in chapter 3. The reliability study was achieved by identifying ageing causes and mechanisms in relations to specific ageing factor in SCs for effective product improvement and reliability prediction.

It is understood that much research is being done in this regard. However this thesis contributes in this area of study by proposing a method that analyses ageing mechanism of SCs during operation conditions. Making it easier to identify the failure cause and mode in SCs, the moment it begins to show traces of degradation. Unlike the common method of analysing failure in SC by combing all the ageing factors during testing which leads to uncertainty on a direct ageing effect, this research work

provides a platform to studying failure effects in both SC single cells and SC module under individual and combined ageing factors.

The research objectives highlighted below were successfully met within the duration of the study;

- **To analyse the effect of SC ageing factors one at a time before combining them together, so as to understand and distinguish between the ageing mechanisms of each ageing factor, thereby creating a baseline to explain the mechanism of SC failure in operation whereby more than one ageing factor is present.**

The ageing factors tested in this thesis categorised by three set-ups, were; high-temperature tests, constant voltage tests, calendar test and cycling tests (under various environmental and operational conditions). These factors exhibited specific ageing behaviours that prompted the development of three separate ageing models describing electrical and electrochemical changes observed with each ageing factor.

Each ageing factor as shown in Chapter 6 had indeed shown a distinctive effect on SCs. The changes observed by the characterization tests; EIS, CC and CV during the ageing process modified the SCs properties. The changes observed in CC and CV test were pretty much the same for all the ageing factors; which were, (1) the increase of voltage at open circuit and (2) decrease of charge/discharge time in CC tests. While in CV tests the change observed was the alteration of the wave shape as the surface area shrank. The changes observed in these tests were present in all the tested ageing

factors at different rates depending how much the factors affect the SC cells. Since the response produced by these two characterization tools were similar regardless of the ageing factor, CC test were reserved to calculating ageing modes for easy quantification in the gradual regression of SC properties; capacitance and ESR values using Equation (5.7) and Equation (5.8) respectively, while CV tests verified the capacitance results with voltammograms changes observed in the tests.

However this was not the case with EIS characterization test were each ageing factor exhibited different changes especially at the impedance spectra, thereby indicating the ageing process associated with each ageing factor in SC.

The impedance spectrum identified three notable ageing process in SCs, they were: (1) the emergence and continual growth of semicircle at high-frequency (10kHz-500Hz) as ageing persists, (2) the appearance and gradual increase in diameter of a bump at medium-frequency (500Hz-1Hz) as ageing continues, (3) tilting of the impedance spectrum at the low-frequency (1Hz-100mHz) part of aged SCs. The thesis found that each of these ageing processes were ageing factor-dependent. Besides the above ageing process, SCs in all conditions showed an increase of the real impedance. All of these ageing processes were, in fact, consistent with the findings in several literatures for big cell SCs (e.g. (El Brouji, Vinassa, et al., 2009), (Kötz et al., 2010), (N Bertrand et al., 2010), (El Brouji, Briat, Vinassa, Bertrand, et al., 2009), (Bohlen et al., 2007a), (El Brouji, Briat, Vinassa, Henry, et al., 2009), (Alcicek et al., 2007) (Mohammad Naim, 2015)).

From the three observed ageing processes, the thesis concludes that the main ageing mechanisms in SCs, respective to the ageing process above, are: (1) the loss of contact

within the electrode, which gives rise to the contact resistance, and (2) the changes to the SC porous electrode. Based on the results of the accelerated ageing test (Chapter 6).

The thesis identifies the emergence and the continual growth of semicircle present at a high frequency in the impedance spectrum as an effect of high temperature. This behaviour is observed at different ageing stages and ageing intensity in (1) high-temperature test, (2) calendar test, and (3) all the cycling tests, because of the presence of high temperature in the tests. Thereby, affecting the contact within SCs electrodes and also between electrodes to the current collector interface by an accumulation of heat and pressure inside the cell. The contact loss can be linked to (1) the increase in contact resistance between the electrode and the current collector, (2) the formation of aluminium oxide and the delamination of the electrode from the current collector, and (3) the crystallisation of AN electrolyte.

Whereas, the behaviour observed in the medium and low frequency of the spectrum were only present at; (1) calendar test and (2) cycling tests, with a more protruding behaviour observed at the calendar test results. This behaviour affects changes to the SC porous electrode. The appearance of the bump emulates a charge transfer reaction, which is likely to occur due to the formation of corrosion products or may be related to the increase of the distributed resistance. Moreover, the tilting at the low frequency indicates reducing the slope of the line. This behaviour suggests that there is a modification to the electrode structure pertaining to the change in the pore size distribution.

AGEING FACTORS	AGEING ELECTROCHEMICAL PROCESS	AGEING MECHANISMS
HIGH TEMPERATURE	• An emergence and continual growth of a semicircle in the impedance spectrum at high frequency	Loss of contact within the electrode, given rise to contact resistance (Kötz, Ruch, & Cericola, 2010)
HIGH VOLTAGE AND CYCLING	• A visible (arc-like) bump in impedance spectrum at medium frequency • A change in the slope of the imaginary part of the impedance spectrum at low frequency	Changes of SC porous electrode emulating a charge transfer reaction (Ruch, Cericola, Foelske-Schmitz, et al., 2010) due to formation of corrosion products or increase of distributed resistance (Ruch, Cericola, Foelske-Schmitz, et al., 2010)

Table 7-1: Summary of the Relationship between Ageing factors and Ageing mechanisms

Another important finding is that, the increase in ESR in aged SCs was caused by either one of these two ageing mechanisms and that the loss of capacitance only took place when SCs experienced both of the ageing mechanisms.

The ageing modes (described as a 100% increase in ESR and a 20% decrease in capacitance) and the ageing processes observed in the impedance spectrum, is observed in ageing factors subjected to both single SCs and module SCs.

During this research work, it was understood that while SC cells exhibited ageing mechanisms specific to its ageing factors, SC cells in a module exhibited a harsher form of ageing, mainly due to voltage imbalance within the module. Hence the second research objective;

- **To distinguish and analyse the ageing mechanism between a single SC cell and 'SC module'. According to previous studies, results have shown a difference of ageing modes between single cells and module (Kötz, Ruch, & Cericola, 2010b). The failure pattern seen in SC modules is so abrupt that the mechanism of failure is mostly linked to the voltage imbalance between cells coupled with uneven temperature dispersion (Kötz et al., 2007)(Al Sakka et al., 2009). Therefore, a suitable equalisation/balancing circuit was proposed and introduced to improve SC module performance. The failure mechanism is to be understood, analysed and compared between SC module with a balancing circuit and SC module without a balancing circuit within the span of this research work.**

In this thesis, ageing effect during cycling is observed in a SC module (serial arrangement). Four type of cycling conditions in SC modules were performed;

1. SC module of two cells connected in series under cycling test at high temperature
2. 2 SC modules of two cells each connected in series (by different voltage equalisation circuits) under cycling test at high temperature

3. 2 SC modules of two cells each connected in series (by different voltage equalisation circuits) with a motor attachment at the load, under cycling test at high temperature
4. 3 SC modules of two cells each connected in series (by different voltage equalisation circuits) with a programmable motor attachment at the load, under varying cycling test at high temperature

Although the tests were carried out in a module arrangement, characterization tests were performed on individual cells after experimental tests. During characterization, all cells exhibited similar ageing modes comparable to the ageing process witnessed on experiments carried out on single cells, except for the cycling test condition of two cells connected without a voltage equalisation. At this test condition, an additional ageing mode known as the 'open circuit failure mode' was noticed just after 62,560 cycles without warning or display of any ageing signs. This consequence resulted in the idea of introducing voltage equalisation circuits to the module's serial arrangement, which proved to be beneficial to the subsequent cycling tests.

Although the voltage equalisation circuits rectified the abrupt failure of SC cells, the ageing proximity between cells was an issue dependent on the equalisation circuit used. As seen in (Figure 6-17) ageing proximity between the cells in each module was reported, at the ESR percentile results, the first cell in the module exceed the ESR 100% mark before the subsequent cell with the commercial 'equalization circuit 2' while the designed 'equalization circuit 1' completed the ageing test at the same rate, in cycling conditions with and without load attachments.

While these cycling conditions satisfied the thesis curiosity pertaining to the importance of voltage equalisation circuits in serially arranged SC modules. Ageing effects during cycling conditions with programmable discharging load and variable SC voltage profiles was also investigated using the preferred 'voltage equalisation circuit 1'. Moreover, it was understood that ageing effects in SC under cycling tests irrespective of the operational condition yielded similar electrical and electrochemical behaviour as demonstrated in the characterization tests in chapter 6.

- **The main research deliverables, also considered the main contribution and novelty of this research work is the modelling SC ageing process and development of SC EEC models representing short-time and long-time operations**

The thesis adds to the understanding of ageing in SC by modelling of the ageing process in SCs using electrical equivalent circuit (EEC). This was achieved by first developing a basic EEC model in the time domain (in Chapter 5), the initial model was modelled using linear time constants with values derived from CC test based on a two branch R-C circuit arrangement (inspired by (Ambade & Joshi, 2014) (Al-janad et al., 2014) (Dănilă et al., 2011) (Johansson & Johansson, 2008)). While simulating the voltage response, the basic model failed to simulate the influence of voltage observed in the charge-redistribution and self-discharge during open-circuit/voltage-hold responses in SCs. According to Devillers et al., (2014), the charge-redistribution and self-discharge behaviour are best modelled with a non-linear capacitor in the

frequency domain. This observation led to the development of an impedance model known as the 'initial model' which maintained the same arrangement as the basic model but substituted a linear capacitor C in the model for an electrochemical component CPE, by modelling the electrochemical properties at one frequency region at a time.

This method of quantifying ageing in SCs was opted for to interpret the underlying mechanisms observed in the impedance spectrum during the ageing process. In Chapter 6, the thesis found that the changes of the SC properties due to ageing led to the emergence of new electrochemical processes thereby requiring an updated EEC interpretation of the SC ageing process. The consequence of this finding signified that a SC model is useful only for the state at which the model was developed. As a result of that, this thesis developed ageing models representing each ageing factor, without completely altering the initial model or complicating the complexity of the model to its initial model. The initial and ageing models, although consists of different electrochemical components, maintained a two branch R-C/CPE branch. The initial model represents the SC before it degrades and the ageing models represent the aged condition of the SCs.

Following the transition from the initial model to the ageing models, based on the electrochemical changes observed in the impedance spectrum during the ageing process. The ageing models were developed by modelling the high-frequency region, the medium-frequency region and the low-frequency region of the spectrum separately. Since all the ageing factors employed in this thesis includes the presence of high temperature, denoted at high-frequency spectrum with the emergency of a

semicircle, all ageing models at this region were modelled with a $R\text{-}CPE$ parallel branch. At medium-frequency region, the calendar test and the cycling tests modelled the diffusion region and charge-transfer region, donated as a bump, with an $R\text{-}W$ (semi-infinite Warburg diffusion element) parallel branch. Whereas, the temperature test at this region was modelled with an $R\text{-}T$ (a bounded finite-length diffusion element with reflective boundary to the low-frequency region) parallel branch interpreting the diffusion impedance, but at low frequency, the diffusion length becomes limited (hence using bounded element T) due to the formation of the thin layer on SC electrode, concluding the ageing model for high temperature test (aged cell T2). While at the reduced slope in the low-frequency region, the calendar test was modelled with a CPE (interpreting a wider inclination the constant phase element at 45^{o}), while the cycling tests were modelled with a T (interpreting a reduced inclination with an finite-length boundary element).

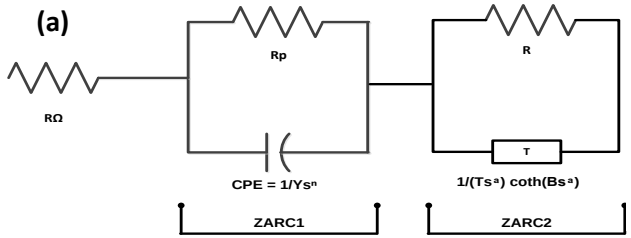
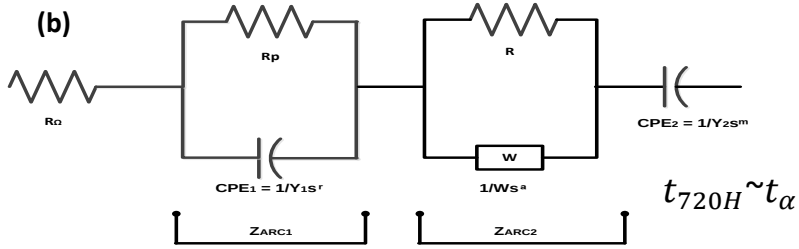
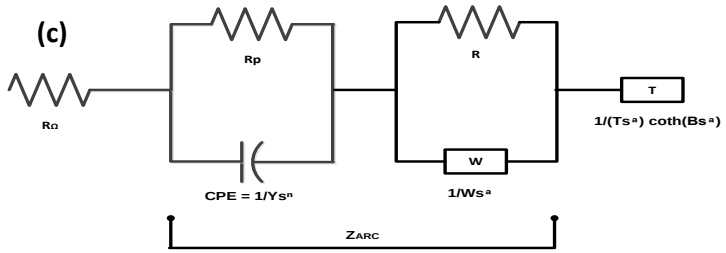
SC Ageing Tests	Ageing Models	EEC Description
Temperature Test	**(a)**  $t_{2592H} \sim t_{\alpha}$	During SC temperature test, the initial model (as shown in Figure 5-14) was viable between test periods 0H to 1584H, at which the sample remained healthy, exhibiting no EOL criteria. Although after 1728H when the sample began to display traces of EOL behaviour, the sample's model transitioned to an ageing model (Table 7-2(a)) describing the samples EEC behaviour from 1728H to 2592H of tested time (also believed to be viable till the point of complete failure)
Calendar Test	**(b)**  $t_{720H} \sim t_{\alpha}$	During SC calendar test, the initial model (as shown in Figure 5-14) was only viable between test periods 0H to 720H, after which the sample suddenly deteriorated to introduce a charge transfer reaction at medium frequency of the impedance spectrum (as shown in Figure 6-9(a)) describing an electrochemical process of a R in parallel with a W in the EEC ageing model
Cycling Tests	**(c)** 	The ageing model derived from cycling yielded one single EEC model (Table 7-2(c)) that was able to describe SC cycling behaviour under voltage equalization, temperature range, different load conditions. Regardless of the conditions experimented, the ageing behaviour witnessed in cycling denoted the same EEC model. The difference however was the ageing time for each condition; a. Cycling under high temperature transitioned to the ageing model after 864H for samples B7,B8 and C9, and 1008H for sample C10 b. Cycling with load attachment under high temperature transitioned to the ageing model after 864H for samples MtA&MtB and 720H for MtC&MtD c. Cycling with variable voltage load profiles under high temperature transitioned to the ageing model after 432H for all the samples in the module

Table 7-2: Summarized table showing Ageing models and their descriptions specific to their Ageing factors

Modelling the EEC SCs dynamic behaviour, have provided several benefits as follows;

- It provided a better and wider frequency range of approximation than the conventional circuit elements
- The components are electrochemical process-related elements. Thus, the relation of the component to an electrochemical process can be made directly
- Reduces the circuit components complexity in the proposed models by taking the form of fractional-order. Thereby making it easy to simulate the SC electrical voltage response accurately in MATLAB/SIMULINK.

In summary, this thesis met the main objective of this thesis, which is to investigate not only SC cell performance on the predominant factors of ageing but also SC module performance in various cycling conditions that emulates EV operation principles. This is done by modelling their electrical and electrochemical behaviour in an EEC.

7.1 Suggestions for Future studies

This thesis has demonstrated the simplicity and efficiency of interpreting and monitoring ageing effects in SCs with EEC models. However, the ageing process in cycling conditions could be understood better with further studies. Although, this thesis studied ageing effects in cycling conditions, extending the experimental duration till a complete failure of SC cells is perceived would be more efficient in understanding the ageing model more accurately. While the ageing model holds electrochemical components similar to the calendar test at the medium-frequency region, the similarities of their impedance response at that region seemed to be minimal. These findings suggest that with a longer cycling duration, an impedance response very similar to the calendar test at the medium frequency range is possible.

Even with that knowledge, deeper investigations to the appearance of the bump at the medium-frequency region of both calendar test and cycling tests (which appeared to be similar to the ageing effect in battery during power cycling (a. Eddahech et al., 2011)) is prudent, as this thesis was unable to come up with a definite answer. The thesis assumes it is a charge transfer response which may have been initiated by a redox reaction due to the non-entirely inert carbon materials of the electrode.

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APPENDIX

Appendix A: Charge/discharge circuit 1 Arduino sketch code

```
int enA = 10;

int in2 = 9;

int in1 = 8;

int enB = 11;

int in3 = 12;

int in4 = 13;

int flag = 0; // charge = 1, discharge = 0

int i = 1; //cycle counter

int y = 0; //cycle

void setup()

{  pinMode(enB, OUTPUT);   // sets the pin as output

  pinMode(in3, OUTPUT);   // sets the pin as output

  pinMode(in4, OUTPUT);

  Serial.begin(9600);

  //while(!Serial)

  //{ ;  }

  Serial.println("Start");}

void loop()

{  int n = 10;

  int s0 = 0;

  int s1 = 0;
```

```
for (int x = 0; x < n; x++)
{    s0 += analogRead(1);
  delay(10);
  s1 += analogRead(2);
  delay(10); }
s0 = s0/n;
s1 = s1/n;
float voltage0 = s0 * (3.28/ 1023.0);
voltage0 = voltage0 * 2;
float voltage1 = s1 * (3.28/ 1023.0);
voltage1 = voltage1 * 2;
int sensorValue = s0-s1;
float voltage = voltage0-voltage1;
Serial.print("sensor = ");
Serial.print(sensorValue);
Serial.print(" V = ");
Serial.print(voltage);
Serial.print(" flag = ");
Serial.println(flag);
if(voltage >= 0 && voltage <= 5.4 && flag == 0)
{    digitalWrite(in3, HIGH);
  digitalWrite(in4, LOW);
  for(sensorValue = 0; sensorValue < 1024; sensorValue++)
  {     analogWrite(enB, sensorValue);
  }  }
 if(voltage > 5.4)
{   flag = 1;
```

```
  y++; }
if(flag == 1)
{   digitalWrite(in3,LOW);
  digitalWrite(in4,HIGH);
  for(sensorValue = 0; sensorValue <1024; sensorValue++)
  {     analogWrite(enB, sensorValue); } }
if(flag == 0)
{   digitalWrite(in3,HIGH);
  digitalWrite(in4,LOW);
  for(sensorValue = 0; sensorValue <1024; sensorValue++)
  {     analogWrite(enB, sensorValue);   } }
if(voltage <= -0.01)
 {   flag = 0; }
 Serial.print(" Cycle = ");
 Serial.println(y);
 delay(1000);}
```

Appendix B: Charge/discharge circuit 2 Arduino sketch code

```
int E1 = 5;
int M1 = 4;
int E2 = 6;
int M2 = 7;
int flag = 0; // charge = 1, discharge = 0
int i = 1; //cycle counter
int y = 0; //cycle
void setup()
{    pinMode(M1, OUTPUT);
    pinMode(M2, OUTPUT);
   Serial.begin(9600);
 // while(!Serial)
 // {  ;}
   Serial.println("Starting...");}
void loop()
{  int n = 10;
  int s0 = 0;
  int s1 = 0;
  for (int x = 0; x < n; x++)
  {    s0 += analogRead(1);
    delay(10);
    s1 += analogRead(2);
    delay(10); }
  s0 = s0/n;
```

```
s1 = s1/n;
float voltage0 = s0 * (3.265/ 1023.0);
voltage0 = voltage0 * 2;
float voltage1 = s1 * (3.265/ 1023.0);
voltage1 = voltage1 * 2;
int sensorValue = s0-s1;
float voltage = voltage0-voltage1;
Serial.print("Sensor = ");
Serial.print(sensorValue);
Serial.print(" S0 = ");
Serial.print(s0);
Serial.print(" S1 = ");
Serial.print(s1);
Serial.print("  V = ");
Serial.println(voltage);
Serial.print(" flag = ");
Serial.println(flag);
if(voltage >= 0 && voltage <= 5.4 && flag == 0)
{    digitalWrite(M1,LOW);
  digitalWrite(M2, HIGH);
  analogWrite(E1, 0);   //PWM Speed Control
  for(sensorValue = 0; sensorValue < 1024; sensorValue++)
  {     analogWrite(E2, sensorValue); //PWM Speed Control
  }  }
if(voltage >= 0 && voltage <= 5.4 && flag == 1)
{    digitalWrite(M1,HIGH);
  digitalWrite(M2, LOW);
```

```
  analogWrite(E2, 0);   //PWM Speed Control
  for(sensorValue = 0; sensorValue < 1024; sensorValue++)
  {     analogWrite(E1, sensorValue); //PWM Speed Control }   }
   if(voltage > 5.4)
 {   flag = 1;
  y++;  }
if(flag == 1)
{   digitalWrite(M1,HIGH);
  digitalWrite(M2, LOW);
  for(sensorValue = 0; sensorValue <1024; sensorValue++)
  {   analogWrite(E1, sensorValue);   //PWM Speed Control
  analogWrite(E2, sensorValue);   //PWM Speed Control } }
 if(flag == 0)
{   digitalWrite(M1,LOW);
  digitalWrite(M2, HIGH);
  analogWrite(E1, 0);   //PWM Speed Control
  for(sensorValue = 0; sensorValue <1024; sensorValue++)
  {     analogWrite(E2, sensorValue); //PWM Speed Control  }}
 if(voltage <= -0.01)
 {   flag = 0;  }
  Serial.print(" Cycle = ");
 Serial.println(y);
  delay(1000);}
```

Appendix C: Charging circuit Arduino sketch codes

```
#include <LiquidCrystal.h>

//---------------------------------Pin Out-------------------------------------

 int RELAY=2;                    // DIGITAL OUT Switches between charging and discharging
circuit

 int SETUP = 3;                 // DIGITAL IN  Input from switch to select between setup menu
and charging circuit

                               // DIGITAL IN  Input from the discharge circuit once discharge
completed

 int OUT_DISCHARGE = 10;        // DIGITAL OUT Output to discharge circuit once charging
completed

 int OUT_EnB = 11;              // DIGITAL OUT Sends a PWM signal to select the charging
voltage

 int OUT_IN3 = 12;              // DIGITAL OUT Supplies charging voltage connected to +ive
pin of capacitor bank

 int OUT_IN4 = 13;              // DIGITAL OUT Supplies charging voltage connected to -ive
pin of capacitor bank

//---------------------------------Variables-----------------------------------

 int i = 0;                     //Initial charge counter

 int n = 10;                    //Sample size of Sensor Readings

 int y = 1;                     //Charge - Discharge Cycle Counter

 int s0 = 0;                    //Capacitor +ive pin (Across 5V potential divider)

 int s1 = 0;                    //Capacitor -ive pin (Across 5V potential divider)

 int sensorValue;               //Difference between s0 and s1

 int p0 = 0;                    //Charging Voltage (Potentiometer)

 int p1 = 0;                    //Set Voltage (Potentiometer)

 int x=0;                       //PWM counter
```

```
 float CapBankVoltage, voltage0, voltage1, ChargingVoltage, SetVoltage;
 float pwmValue;
 void Measure_Voltages();
LiquidCrystal lcd(8, 9, 4, 5, 6, 7);     // select the pins used on the LCD panel
void setup()
{
 analogReference(DEFAULT);            //setting the reference voltage across analog pins as
default
 pinMode(RELAY, OUTPUT);
 pinMode(OUT_EnB, OUTPUT);
 pinMode(OUT_IN3, OUTPUT);
 pinMode(OUT_IN4, OUTPUT);
 pinMode(OUT_DISCHARGE, OUTPUT);
 pinMode(SETUP, INPUT);
 pinMode(digitalRead(A4),INPUT);
  Serial.begin(9600);
 Serial.print("---------------- SUPERCAP CHARGER ---------------");
 Serial.println();
 }
void loop(){
  digitalWrite(RELAY, HIGH);           //Relay is initially set to charging circuit
  while(digitalRead(SETUP)== 1){       //If switch is OFF goes to setup menu
  lcd.begin(16, 2);
  digitalWrite(OUT_IN3, LOW);
  digitalWrite(OUT_IN4, LOW);
  Measure_Voltages();
   Serial.print("Idle");
```

```
 Serial.println();
/*
 Serial.print("Setup = 1");
 Serial.println();
*/
lcd.setCursor(12,0);
lcd.print("Cp V");
lcd.setCursor(12,1);
lcd.print(CapBankVoltage,1);
lcd.setCursor(6,0);
lcd.print("Cs V");
lcd.setCursor(6,1);
lcd.print(SetVoltage,1);
lcd.setCursor(0,0);
lcd.print("Ch V");
lcd.setCursor(0,1);
lcd.print(ChargingVoltage, 1);
delay(1000);
lcd.setCursor(0,1);
lcd.print("              "); }
while( digitalRead(SETUP)== 0 ){ //If switch is ON begins charging capacitor bank
  lcd.begin(16, 2);
  Measure_Voltages();
  if (digitalRead(OUT_DISCHARGE) == 1 && (digitalRead(A4) == 1 )){
  y=y+1; }
  if((((digitalRead(A4)) == 1 ) && (CapBankVoltage < SetVoltage)) || (i == 0)) {
  digitalWrite(OUT_DISCHARGE,LOW);
```

```
  digitalWrite(OUT_IN3, HIGH);
  digitalWrite(OUT_IN4, LOW);
  digitalWrite(RELAY,HIGH);
  for(x=0; x < 255; x++){
   analogWrite(OUT_EnB, pwmValue); }
  lcd.setCursor(0,0);
  lcd.print("    Charging    ");
  lcd.setCursor(5,1);
  lcd.print(CapBankVoltage);
  delay(500);


  Serial.print("**********Charging**********");
  Serial.println();
/* Serial.print("RELAY = "); Serial.print(digitalRead(RELAY));
  Serial.println();
  Serial.print("digitalRead(A4) = ");Serial.print(digitalRead(A4));
  Serial.println();
  Serial.print("i = "); Serial.print(i);
  Serial.println();
  Serial.print("OUT_IN3=");Serial.print(digitalRead(OUT_IN3));
  Serial.println();
  Serial.print("OUT_IN4=");Serial.print(digitalRead(OUT_IN4));
  Serial.println();
  Serial.print("PWM Value = ");Serial.print(pwmValue);
*/ Serial.print("Capacitor Bank Voltage = ");
  Serial.print(CapBankVoltage);
  Serial.println();
```

```
Serial.print("**************************************************");
Serial.println();
Serial.println();
Serial.println();
delay(200);
}
if((CapBankVoltage >= SetVoltage) && (digitalRead(OUT_DISCHARGE)== 0)) {
i=1;
digitalWrite(OUT_DISCHARGE, HIGH);
digitalWrite(RELAY,LOW);
digitalWrite(OUT_IN3, LOW);
digitalWrite(OUT_IN4, LOW);
lcd.clear();
lcd.setCursor(0,0);
lcd.print("Discharge");
lcd.setCursor(0,1);
lcd.print(CapBankVoltage);
lcd.setCursor(11,0);
lcd.print("Cycle");
lcd.setCursor(11,1);
lcd.print(y);
delay(500);  }
if (digitalRead(OUT_DISCHARGE) == 1 && (digitalRead(A4) == 0 )){
lcd.clear();
lcd.setCursor(0,0);
lcd.print("Discharge");
lcd.setCursor(0,1);
```

```
  lcd.print(CapBankVoltage);
  lcd.setCursor(11,0);
  lcd.print("Cycle");
  lcd.setCursor(11,1);
  lcd.print(y);
  delay(500);


  Serial.print("********************Discharging*********************");
  Serial.println();
 /*Serial.print("RELAY = "); Serial.print(digitalRead(RELAY));
  Serial.println();
  Serial.print("OUT_DISCHARGE =  ");Serial.print(digitalRead(OUT_DISCHARGE));
  Serial.println();
  Serial.print("i = "); Serial.print(i);
  Serial.println();
  Serial.print("OUT_IN3 = ");Serial.print(digitalRead(OUT_IN3));
  Serial.println();
  Serial.print("OUT_IN4 = ");Serial.print(digitalRead(OUT_IN4));
  Serial.println();
 */Serial.print("Capacitor Bank Voltage = ");
  Serial.print(CapBankVoltage);
  Serial.println();
  Serial.print("Cycle = ");
  Serial.print(y);
  Serial.println();
  Serial.print("**************************************************");
  Serial.println();
```

```
    Serial.println();
    Serial.println();
    } } }
//----------------------------------------Functions----------------------------------------
void  Measure_Voltages()
  {delay(500);
        // start the library
     for (int x = 0; x < n; x++){
  s0 += analogRead(1);  // A1 Reads Positive Capacitor Pin
  delay(10);
  s1 += analogRead(3);  // A3 Reads Negative Capacitor Pin
  delay(10);
  p0 += analogRead(0);  // A0 Controls ChargingVoltage
  delay(10);
  p1 += analogRead(2);  // A2 Controls SetVoltage
  delay(10); }
  s0 = s0/n;
  s1 = s1/n;
  p0 = p0/n;
  p1 = p1/n;

  voltage0 = s0 * (5.00/ 1135.0);
  voltage0 = 2.6 * voltage0;
  voltage1 = s1 * (5.00/ 1135.0);
  voltage1 =  2.4 * voltage1;
  ChargingVoltage = p0 * (5/ 1135.0);
  ChargingVoltage = 2.4 * ChargingVoltage;
```

```
SetVoltage = p1 * (5/ 1135.0);
SetVoltage = 2.4 * SetVoltage;


sensorValue = s0-s1;
CapBankVoltage = (voltage0 - voltage1);
pwmValue = (p0/1135)* 255;
if(SetVoltage < 0)
{     SetVoltage = 0;    }
if(SetVoltage > 0 && SetVoltage <=1)
{     SetVoltage=1;   }
if(SetVoltage > 1 && SetVoltage <=2)
{     SetVoltage=2;    }
if(SetVoltage > 2 && SetVoltage<=3)
{     SetVoltage=3;    }
if(SetVoltage > 3 && SetVoltage<=4)
{     SetVoltage=4;    }
if(SetVoltage > 4 && SetVoltage <= 5)
{     SetVoltage=5;    }
if(SetVoltage > 5 && SetVoltage<= 6)
{     SetVoltage=6;    }
if(SetVoltage > 6 && SetVoltage<=7)
{     SetVoltage=7;    }
if(SetVoltage > 7 && SetVoltage<= 8)
{     SetVoltage=8;    }
if(SetVoltage > 8 && SetVoltage<= 9)
{     SetVoltage=9;    }
```

```
if(SetVoltage > 9 && SetVoltage<= 10)
{     SetVoltage=10;    }
if(SetVoltage > 10){
 SetVoltage = 11;    }
if(ChargingVoltage < 5)
{     ChargingVoltage=5;
 pwmValue = 19;     }
if(ChargingVoltage > 5 && ChargingVoltage<=6)
{     ChargingVoltage=6;
 pwmValue = 46;     }
if(ChargingVoltage > 6 && ChargingVoltage<=7)
{     ChargingVoltage=7;
 pwmValue = 73;    }
if(ChargingVoltage > 7 && ChargingVoltage<=8)
{     ChargingVoltage=8;
 pwmValue = 102;    }
if(ChargingVoltage > 8 && ChargingVoltage<=9)
{     ChargingVoltage=9;
 pwmValue = 131 ;    }
if(ChargingVoltage > 9 && ChargingVoltage<=10)
{     ChargingVoltage=10;
 pwmValue = 164;    }
if(ChargingVoltage > 10 && ChargingVoltage<=11)
{     ChargingVoltage=11;
 pwmValue = 204;    }
if(ChargingVoltage > 11)
{     ChargingVoltage=12;
```

```
  pwmValue = 255;    }

/*

Serial.print(" Analog 0 p0= "); Serial.println(p0);

Serial.print(" Analog 2 p1= ");Serial.println(p1);

Serial.print(" Analog 1 s0= ");Serial.println(s0);

Serial.print(" Analog 3 s1= ");Serial.println(s1);


Serial.print("Cap Voltage Set To: ");

Serial.print(SetVoltage);

Serial.println();

Serial.print("Charging Voltage Set To: ");

Serial.print(ChargingVoltage);

Serial.println();

Serial.print("Sensor Value =  ");

Serial.print(sensorValue);

Serial.println();

Serial.print("  V = ");

Serial.print(CapBankVoltage);

Serial.println();

Serial.println();

*/   }
```

Appendix D: Variable load discharging circuit Arduino sketch codes

```
#include <LiquidCrystal.h>

const float referenceVolts = 5;       // the default reference on a 5-volt board

const float R1 = 2000;                // value for a maximum voltage of 15 volts

const float R2 = 1000;

const float resistorFactor = 341.0;

//---------------------------------Variables-----------------------------------


float volts, volts2 = 0.00;

int toggle = 1;

int left_button, right_button = 0;

int v2_min = 5;

int v2_max = 11;

int s_min = 120;

int s_max = 220;

int v2_max_flag,volts2_flag = 0;

int charge=0;

int cycle, cycle_flag = 0;

// define some values used by the panel and buttons

float volts2_Array[3];

int input;

int charging_flag, discharge_flag, Auto_flag, Manual_flag, Speed_flag = 0;

int charging_on, charging_off = 0;

int pwm_value, tmp_pwm_value;

int lcd_key     = 0;

int adc_key_in  = 0;
```

```
#define btnRIGHT  0

#define btnUP     1

#define btnDOWN   2

#define btnLEFT   3

#define btnSELECT 4

#define btnNONE   5


void LCD_Start();

void LCD_Auto();

void LCD_Manual();

void LCD_Charge();

void LCD_Charging();

void LCD_Speed();

int read_LCD_buttons();

void LCD_read();

void Read_Voltages();



//--------------------------------Pin Out-----------------------------------------


LiquidCrystal lcd(8, 9, 4, 5, 6, 7);          // select the pins used on the LCD panel

const int MOTOR_PIN = 1;     //Digital 1

const int BATTERY_PIN = 1;   //Analog 1

const int BATTERY_PIN2 = 2;  //Analog 2

const int OUT_CHARGE = 10;   //Label red

const int IN_DISCHARGE = 11; //Label yellow

#define FADE_PIN 13         //Digital Pin
```

```
void setup()
{  pinMode(FADE_PIN, OUTPUT);   //Controls PWM
  pinMode(MOTOR_PIN, OUTPUT);
  pinMode(IN_DISCHARGE, INPUT);
  pinMode(OUT_CHARGE, OUTPUT);
  pwm_value = s_min;
  LCD_Start();
  Serial.begin(9600); }
byte x = 0;
void loop(){
    Read_Voltages();
   if(digitalRead(IN_DISCHARGE)==0){
   Serial.print("IN_DISCHARGE = ");Serial.print(digitalRead(IN_DISCHARGE));
   Serial.println();
   Serial.print("Charging Circuit Connected");
   Serial.println();
   Serial.println();
   digitalWrite(MOTOR_PIN, LOW);

    if ((volts2 < (float)v2_min) && (volts2_flag == 0) && (input != 0 && input != 3 && input
!= 4)){
      digitalWrite(OUT_CHARGE,HIGH);
      Auto_flag = 0;
      Manual_flag = 0;
      LCD_Charging();     }
   else if ((volts2 >= (float)v2_max) && (volts2_flag == 0) &&(input != 0 && input != 3 &&
input != 4)){       digitalWrite(OUT_CHARGE, HIGH);
```

```
      Auto_flag = 0;
      Manual_flag = 0;
      LCD_Charging();     }
   else{       if (volts2 > (float) v2_min) volts2_flag = 1;
      charging_flag = 0;
     if (input == 1 || input == 2  && volts2_flag == 1){
       if (volts2 < v2_min) volts2_flag = 0;
        digitalWrite(OUT_CHARGE,HIGH);
       lcd.setCursor(2,0);
       lcd.print(volts);
       lcd.setCursor(11,0);
       lcd.print(volts2);          }    }
LCD_read();
 }
 if(digitalRead(IN_DISCHARGE)== 1){
  Serial.print("IN_DISCHARGE = ");Serial.print(digitalRead(IN_DISCHARGE));
  Serial.println();
  digitalWrite(OUT_CHARGE,LOW);
    if (volts2 < v2_min){
       volts2_flag = 0;
       discharge_flag=0;
       digitalWrite(OUT_CHARGE, HIGH); }
    if (volts2 > v2_min && input == 1) {
      volts2_flag = 1;
      discharge_flag=1;
      digitalWrite(OUT_CHARGE,LOW);      }
      if (volts2 > v2_min && input == 2) {
```

```
 volts2_flag = 1;
 discharge_flag=2;
 digitalWrite(OUT_CHARGE,LOW);      }
if( input == 0 || input == 3 || input == 4){
 Serial.print("State = Select");
 Serial.println();        }
else if (input == 1 && charging_flag == 0 && volts2_flag == 1 || discharge_flag == 1)
 {        int randNumber = random(s_min, s_max + 1);
  analogWrite(FADE_PIN,randNumber);
  LCD_Auto();
  Serial.print("State = Auto");
  Serial.println();
  Serial.print("Voltage = ");
  Serial.print(volts2);
  Serial.println();
  Serial.println();        }

else if (input == 2 && charging_flag == 0 && volts2_flag == 1 || discharge_flag == 2)
 {        discharge_flag = 2;
 if (volts2 < v2_min) volts2_flag = 0;
  digitalWrite(MOTOR_PIN, HIGH);
  LCD_Manual();
  analogWrite(FADE_PIN,pwm_value);
  Serial.print("State = Manual");
  Serial.println();
  Serial.print("Voltage = ");
  Serial.print(volts2);
```

```
        Serial.println();
        Serial.println();       }
          LCD_read();  }}


//------------------------------------ Functions ----------------------------------------
void Read_Voltages(){
  int val = analogRead(BATTERY_PIN);  // read the value from the sensor
  volts = (val / resistorFactor) * referenceVolts ; // calculate the ratio
  int val2 = analogRead(BATTERY_PIN2);  // read the value from the sensor
  volts2 = (val2 / resistorFactor) * referenceVolts ; // calculate the ratio
}
void LCD_Start(){
 input = 0;
 digitalWrite(MOTOR_PIN, LOW);
 lcd.begin(16, 2);
 lcd.setCursor(0,0);
 lcd.print(" Variable Load");
 lcd.setCursor(0,1);
 lcd.print("< Auto  Manual >");
 analogWrite(FADE_PIN,0); }


void LCD_Auto(){
 Read_Voltages();
 toggle = 1;
 input = 1;
 lcd.clear();
 lcd.setCursor(0,0);
```

```
  lcd.print("V=");
  lcd.print(volts);
  lcd.setCursor(8,0);
  lcd.print("V2=");
  lcd.print(volts2);
  lcd.setCursor(0,1);
  lcd.print("Speed=Auto");
  delay(400);
  if (Auto_flag == 0){
    digitalWrite(MOTOR_PIN, HIGH);
    Auto_flag = 1;
    toggle = 0;  }}

void LCD_Manual(){
  Read_Voltages();
  toggle = 2;
  input = 2;
  lcd.clear();
  lcd.setCursor(0,0);
    lcd.print("V=");
    lcd.print(volts);
    lcd.setCursor(8,0);
    lcd.print("V2=");
    lcd.print(volts2);
    lcd.setCursor(0,1);
    lcd.print("Speed=");
    lcd.print(pwm_value);
```

```
   delay(400);
  if (Manual_flag == 0){
   digitalWrite(MOTOR_PIN, HIGH);
   Manual_flag = 1;
   toggle = 0;  }}
void LCD_Charge(){
  input = 3;
  left_button = 0;
  right_button = 0;
  digitalWrite(MOTOR_PIN, LOW);
  lcd.clear();
  lcd.setCursor(0,0);
  lcd.print(" Charging Range");
  lcd.setCursor(0,1);
  lcd.print("Min<");
  lcd.print(v2_min);
  lcd.print("V");
  lcd.setCursor(9,1);
  lcd.print("Max=");
  lcd.print(v2_max);
  lcd.print("V");
  analogWrite(FADE_PIN, 0);}

void LCD_Charging(){
  //input = 4;
  lcd.clear();
  lcd.setCursor(0,0);
```

```
 lcd.print("Charging Circuit");
 lcd.setCursor(0,1);
 lcd.print(" Connected ");
 delay(300);
 if (charging_flag == 0)
 {  digitalWrite(MOTOR_PIN, LOW);
 charging_flag = 1;
 toggle = 0;
 analogWrite(FADE_PIN, 0);  }}

void LCD_Speed(){
 toggle = 3;
 input = 4;
 digitalWrite(MOTOR_PIN, LOW);
 lcd.clear();
 lcd.setCursor(0,0);
 lcd.print("  Speed Range");
 lcd.setCursor(0,1);
 lcd.print("Min=");
 lcd.print(s_min);
 lcd.print(" Max=");
 lcd.print(s_max);
 Speed_flag = 1;
 analogWrite(FADE_PIN, 0);}

// read the buttons
int read_LCD_buttons(){
```

```
 adc_key_in = analogRead(0);      // read the value from the sensor

 // my buttons when read are centered at these valies: 0, 144, 329, 504, 741

 // we add approx 50 to those values and check to see if we are close

 if (adc_key_in > 1000) return btnNONE; // We make this the 1st option for speed reasons since it will be the most likely result

 // For V1.1 us this threshold

 if (adc_key_in < 50)   return btnRIGHT;

 if (adc_key_in < 250)  return btnUP;

 if (adc_key_in < 450)  return btnDOWN;

 if (adc_key_in < 650)  return btnLEFT;

 if (adc_key_in < 850)  return btnSELECT;


 return btnNONE;  // when all others fail, return this...}


void LCD_read(){

 lcd_key = read_LCD_buttons();  // read the buttons

 switch (lcd_key)               // depending on which button was pushed, we perform an action

 {   case btnRIGHT:

    {      if (input == 0)

      {        LCD_Manual();

        charging_flag = 0;

        Manual_flag = 0;      }

      else if (input == 3 || input == 4)

      {        right_button = 1;

        left_button = 0;      }

    break;    }

  case btnLEFT:    {
```

```
  if(input == 0)     {
     LCD_Auto();
     charging_flag = 0;
     Auto_flag = 0;     }
  else if (input == 3 || input == 4)     {
    left_button = 1;
    right_button = 0;  }
  break;     }
 case btnUP:
  {       if (input == 2 && charging_flag != 1)
    {       if (pwm_value < s_max) pwm_value++; else pwm_value=s_min;
     lcd.setCursor(6,1);
     lcd.print("   ");
     lcd.setCursor(6,1);
     lcd.print(pwm_value);
     delay(150);
     tmp_pwm_value = pwm_value;       }
    else if (input == 3 && left_button == 1)
    {       if (v2_min < v2_max - 1) v2_min++; else v2_min = v2_max - 1;
     lcd.setCursor(4,1);
     lcd.print(v2_min);
     lcd.print("V ");
     delay(150);      }
    else if (input == 3 && right_button == 1)
    {       if (v2_max <= 10) v2_max++; else v2_max=11;
     lcd.setCursor(13,1);
     lcd.print(v2_max);
```

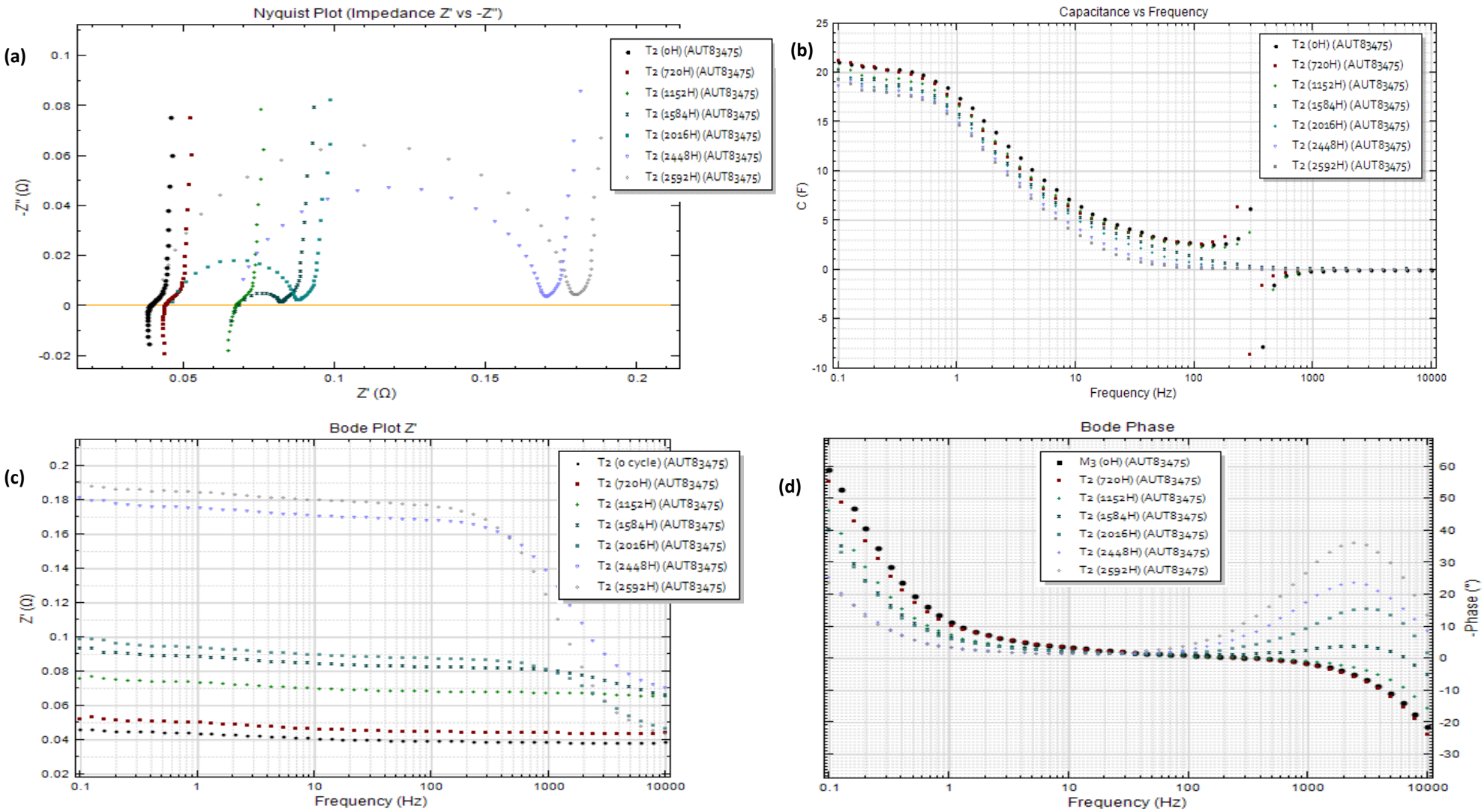
```
    lcd.print("V  ");
    delay(150);      }
  else if (input == 4 && left_button == 1)
  {       if (s_min < s_max && s_min < 255) s_min++; else s_min = s_max;
    lcd.setCursor(4,1);
    lcd.print(s_min);
    lcd.print("  ");
    delay(150);      }
  else if (input == 4 && right_button == 1)
  {       if (s_max < 255) s_max++; else s_max = 255;
    lcd.setCursor(13,1);
    lcd.print(s_max);
    lcd.print("  ");
    delay(150);      }
 break;    }
case btnDOWN:
 {      if (input == 2 && charging_flag != 1)
  {       if (pwm_value > s_min) pwm_value--; else pwm_value=s_max;


    lcd.setCursor(6,1);
    lcd.print("   ");
    lcd.setCursor(6,1);
    lcd.print(pwm_value);
    delay(150);
    tmp_pwm_value = pwm_value;      }
  else if (input == 3 && left_button == 1)
  {       if (v2_min > 1) v2_min--; else v2_min = 1;
```

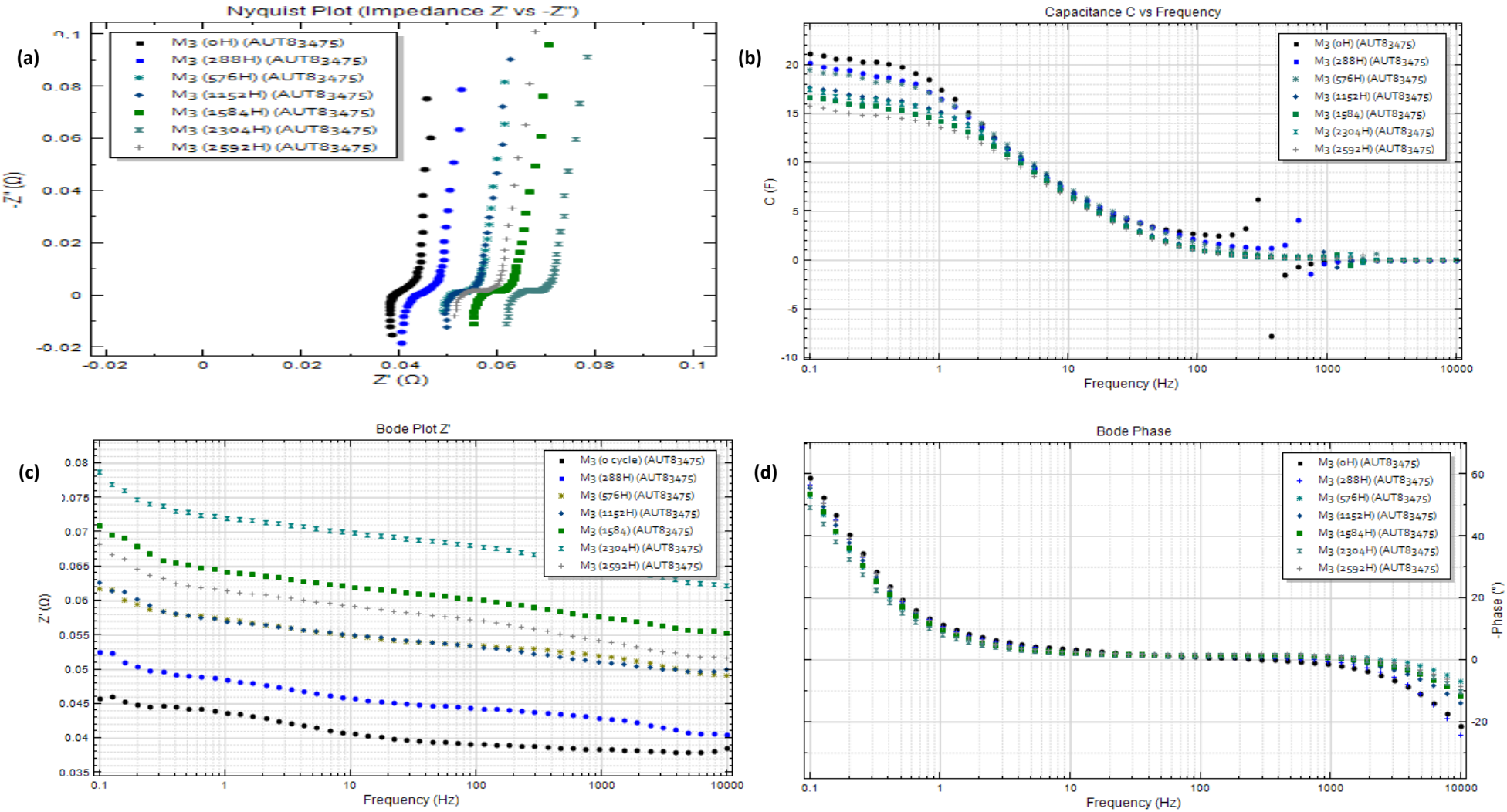
```
    lcd.setCursor(4,1);
    lcd.print(v2_min);
    lcd.print("V ");
    delay(150);      }
  else if (input == 3 && right_button == 1) //Set charging voltage range
  {       if (v2_max > v2_min + 2 && v2_max < 12) v2_max--; else v2_max = v2_min + 1;
    lcd.setCursor(13,1);
    lcd.print(v2_max);
    lcd.print("V  ");
    delay(150);      }
  else if (input == 4 && left_button == 1)
  {       if (s_min > 0) s_min--; else v2_min = 0;
    lcd.setCursor(4,1);
    lcd.print(s_min);
    lcd.print("  ");
    delay(150);      }
  else if (input == 4 && right_button == 1)
  {       if (s_max > s_min && s_max < 256) s_max--; else s_max = s_min;
    lcd.setCursor(13,1);
    lcd.print(s_max);
    lcd.print("  ");
    delay(150);      }
 break;    }
case btnSELECT:
 {      cycle = 0;
  if (toggle == 0)
  {       LCD_Start();
```

```
    delay(150);
    toggle = 1;      }
  else if (toggle == 1)
  {       LCD_Charge();
    delay(150);
    toggle = 2;      }
  else if (toggle == 2)
  {       LCD_Speed();
   delay(150);
   toggle = 0;       }
break;    }
case btnNONE:
{    //lcd.print("NONE  ");
break;   } }}
```

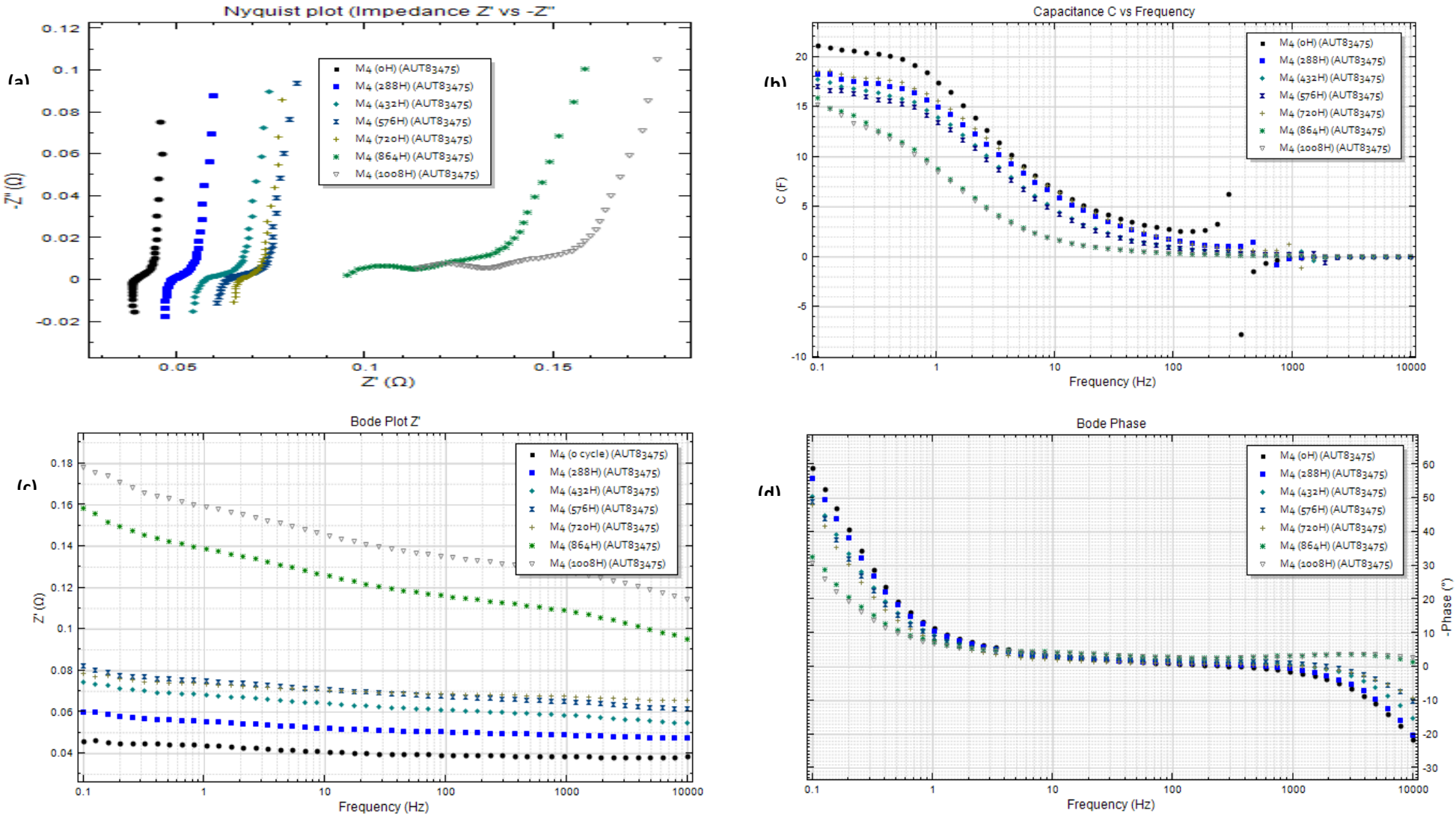
Appendix E: SC samples Characterization Results



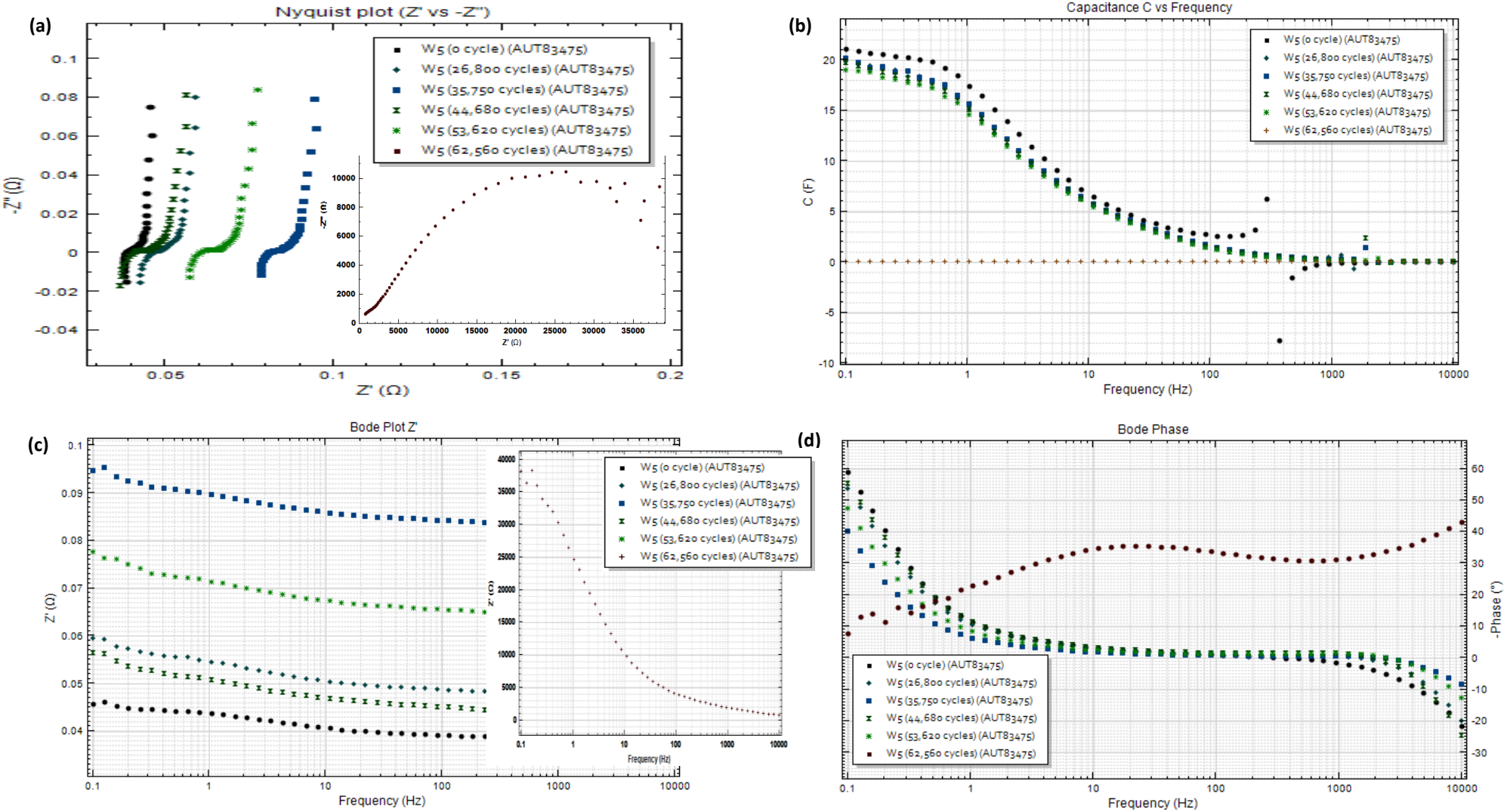
Appendix E-1: T2 EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



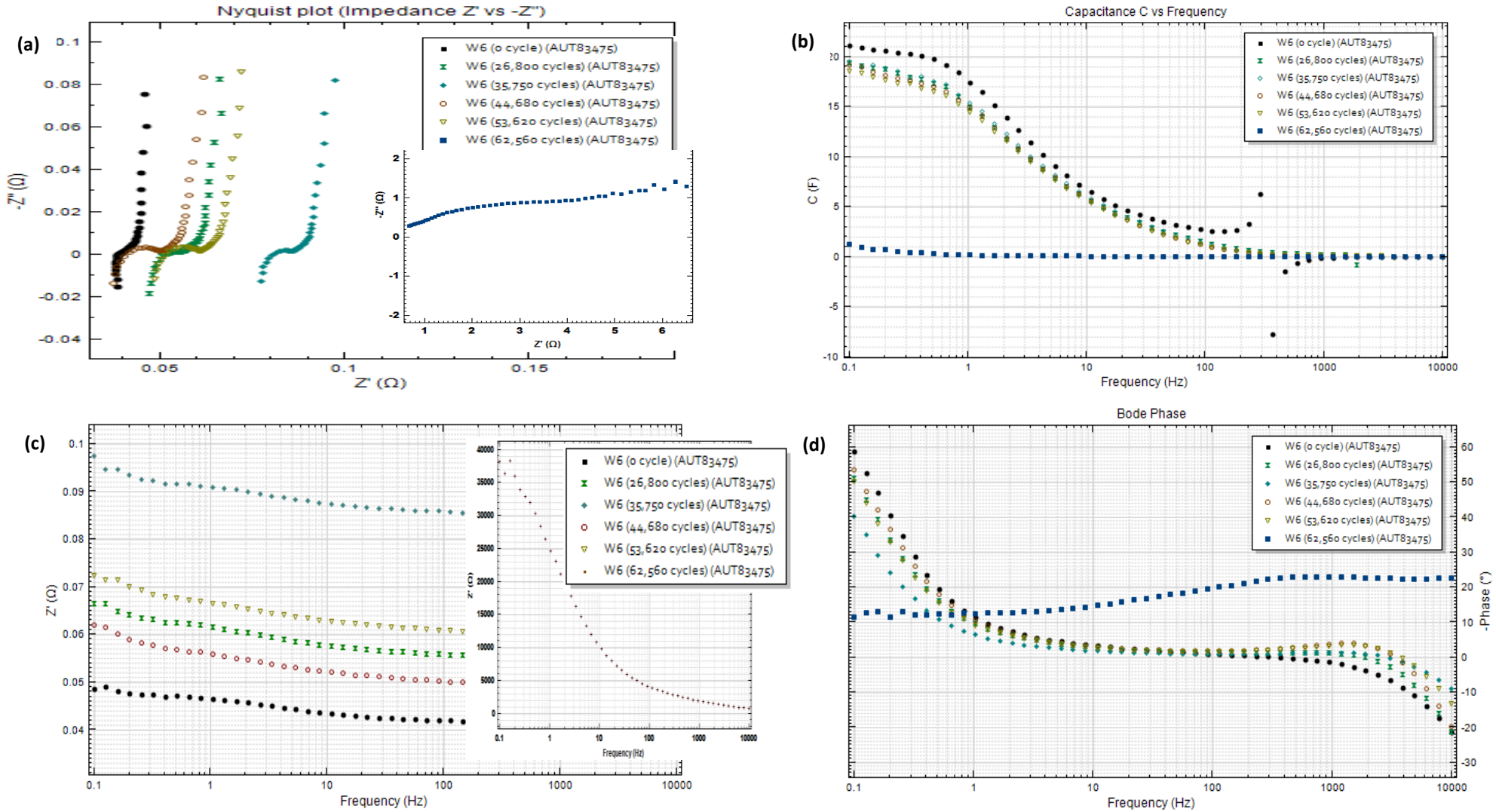
Appendix E-2: M3 EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



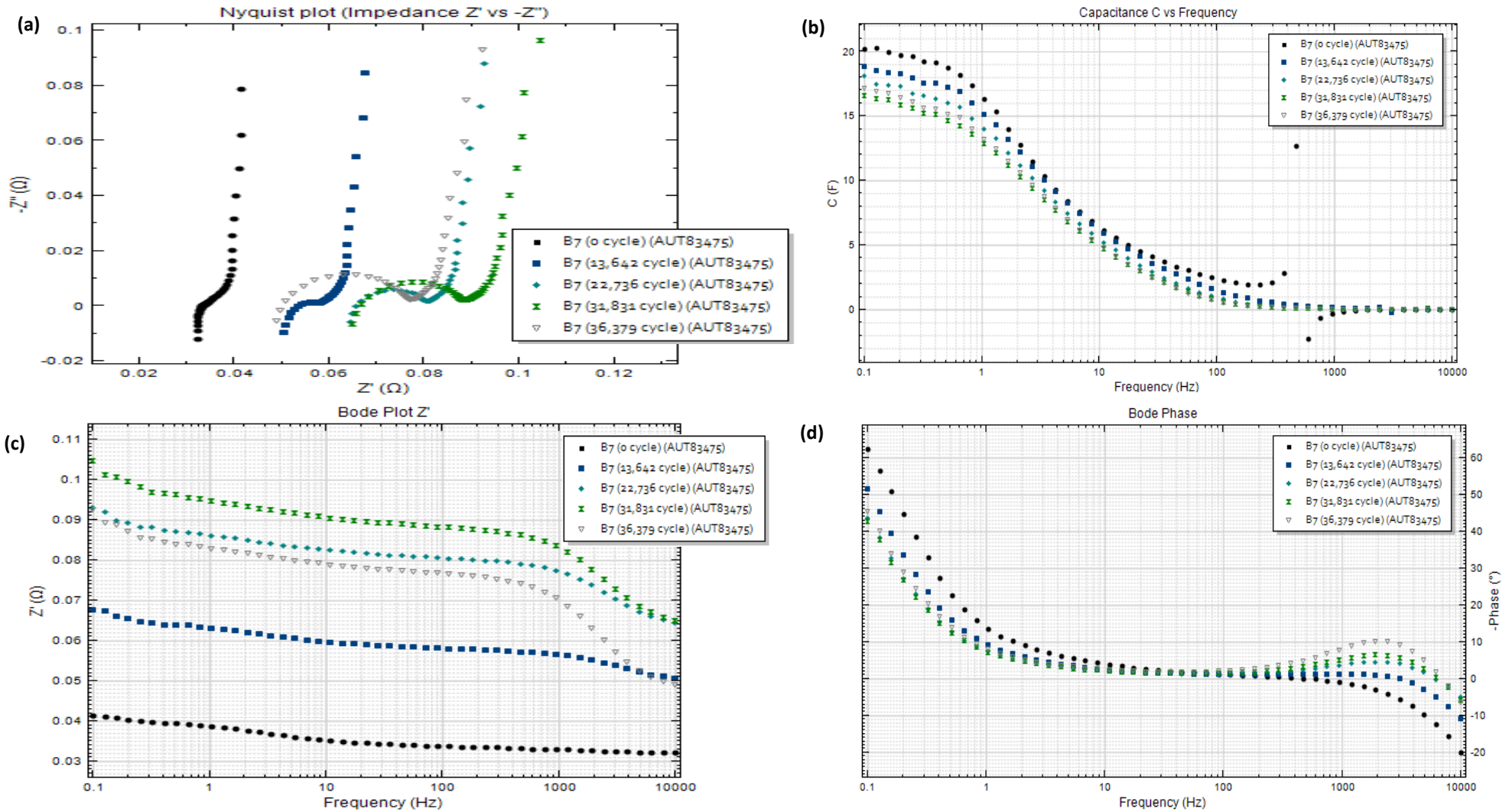
Appendix E-3: M4 EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z"), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



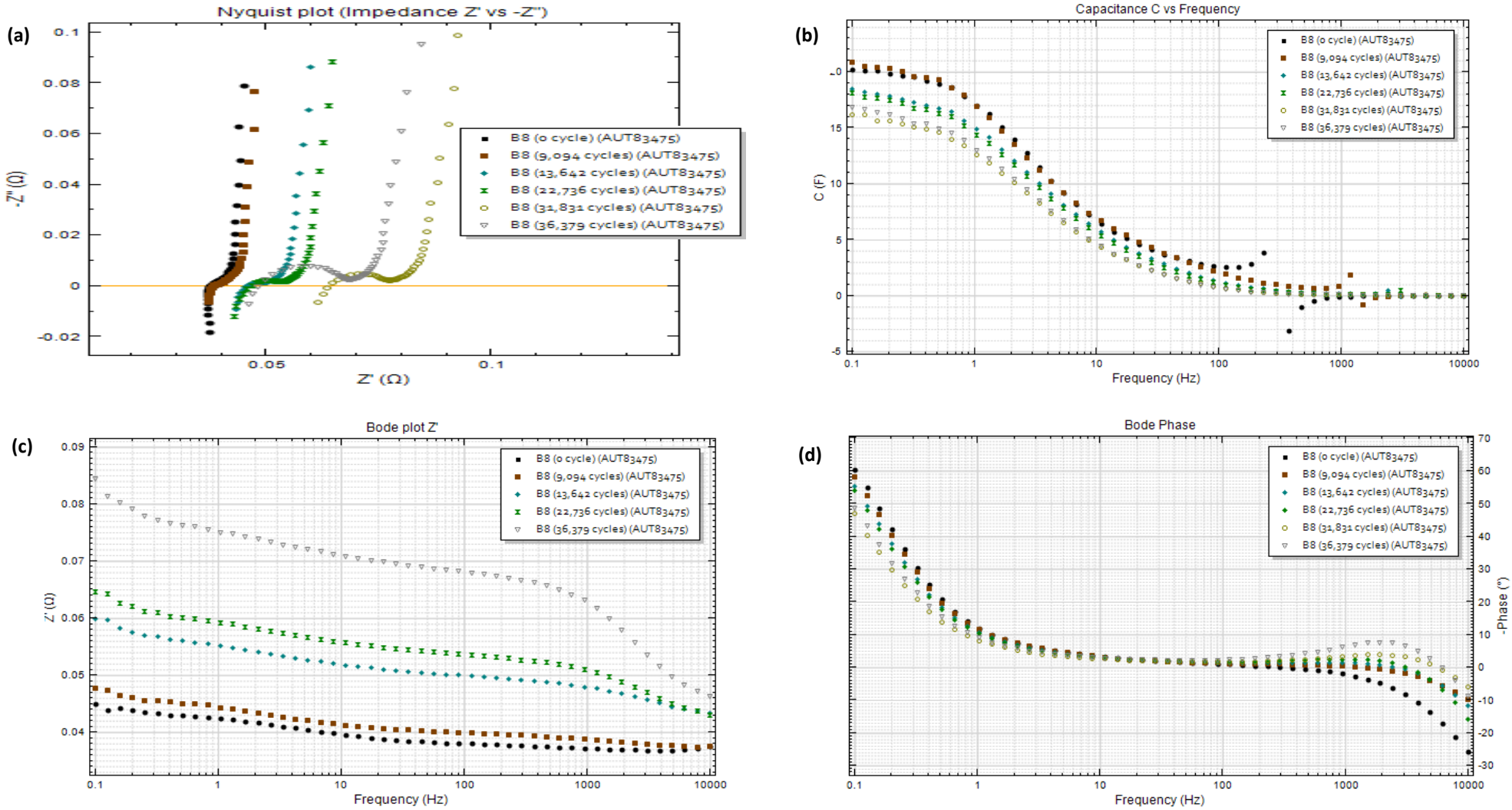
Appendix E-4: W5 EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



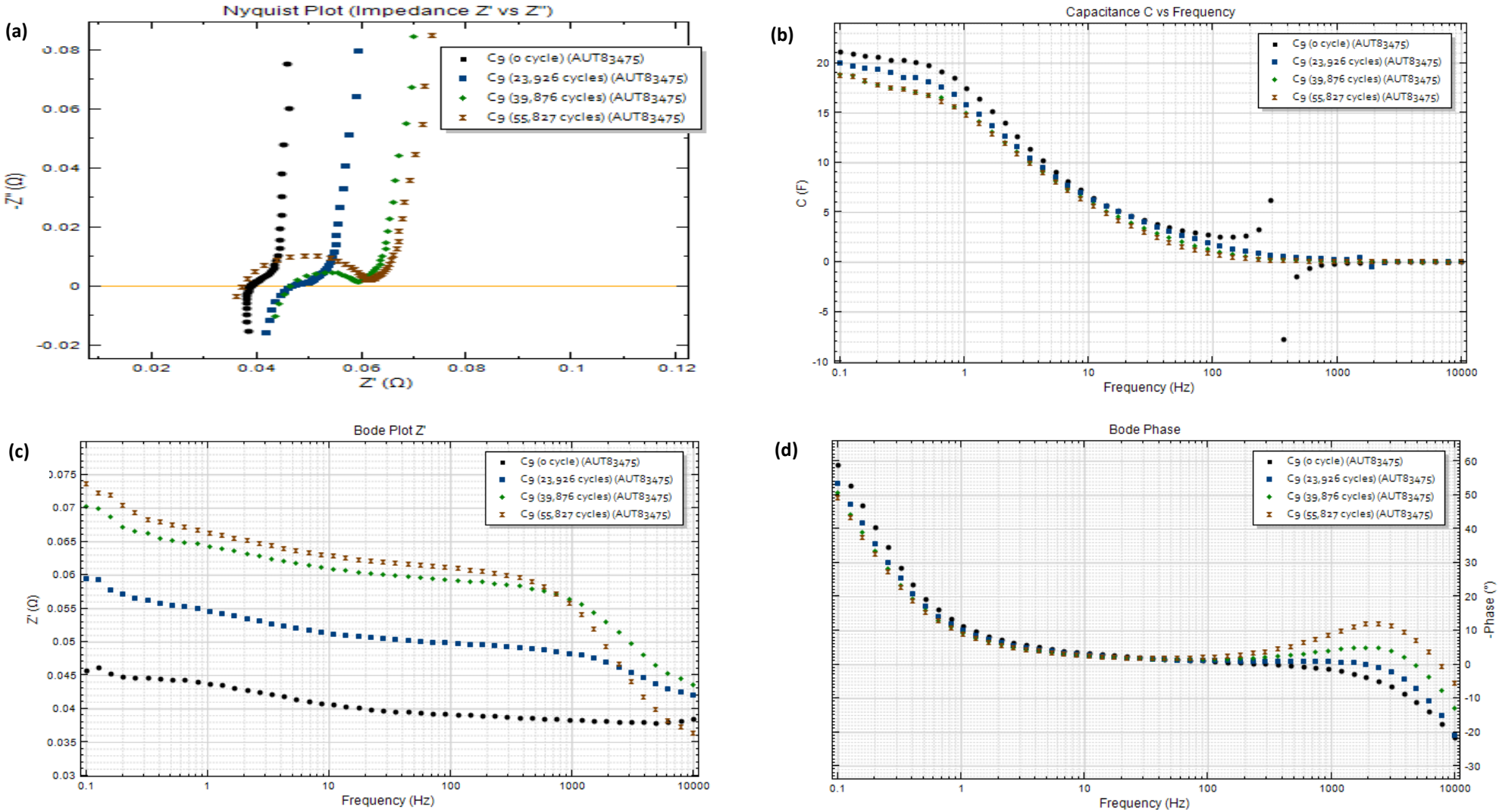
Appendix E-5: W6 EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



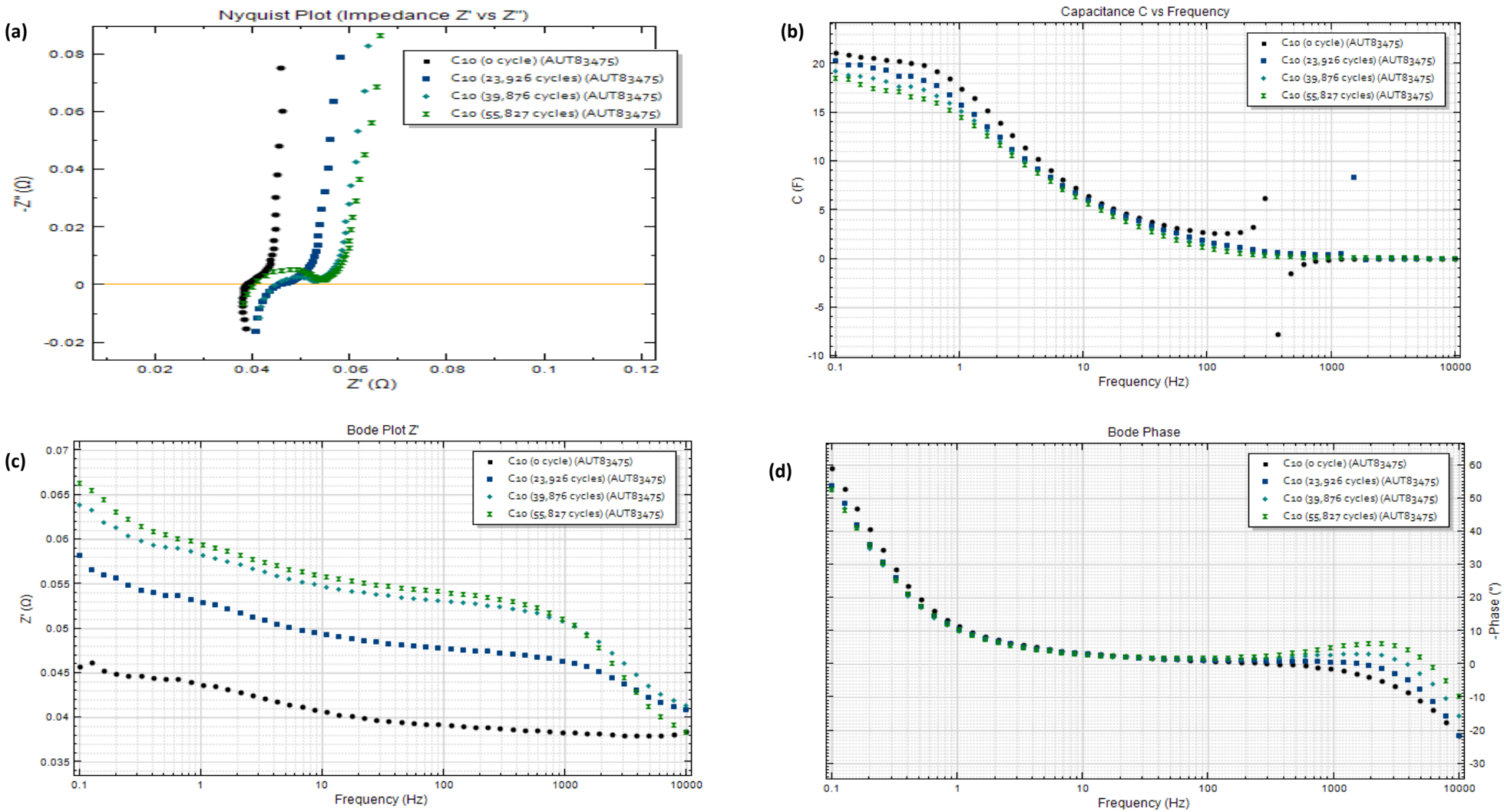
Appendix E-6: B7 EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z"), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



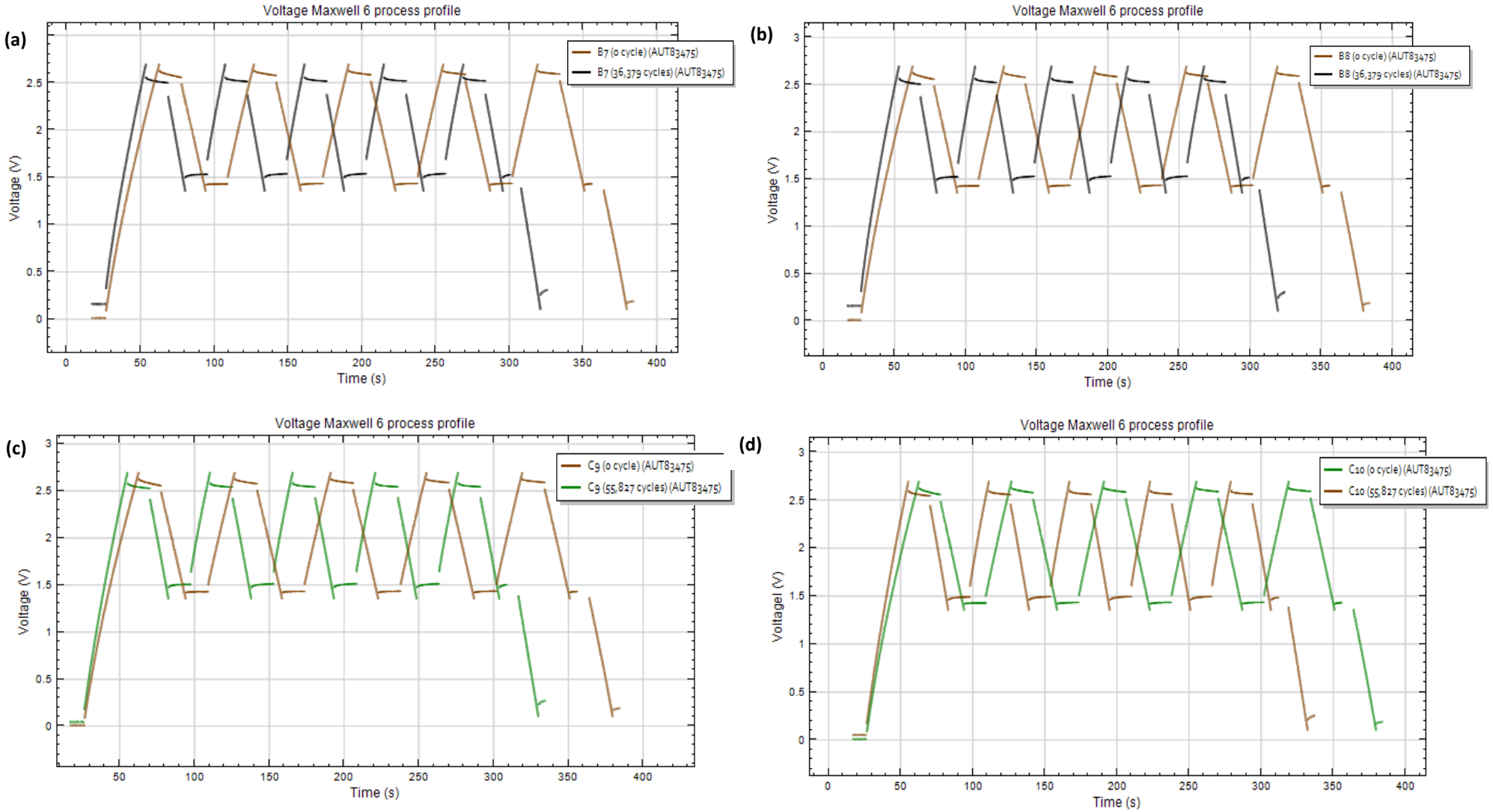
Appendix E-7: B8 EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



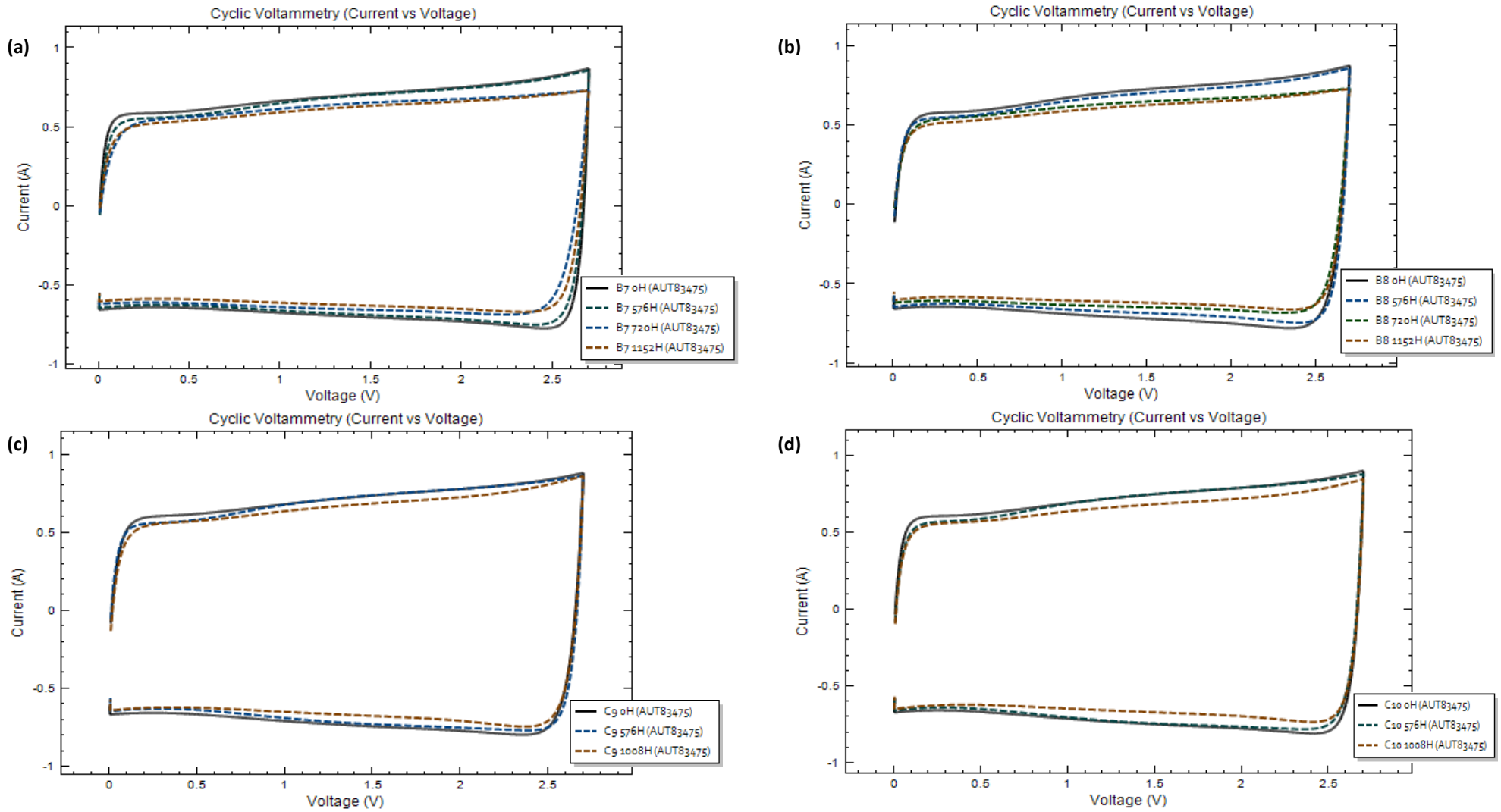
Appendix E-8: C9 EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



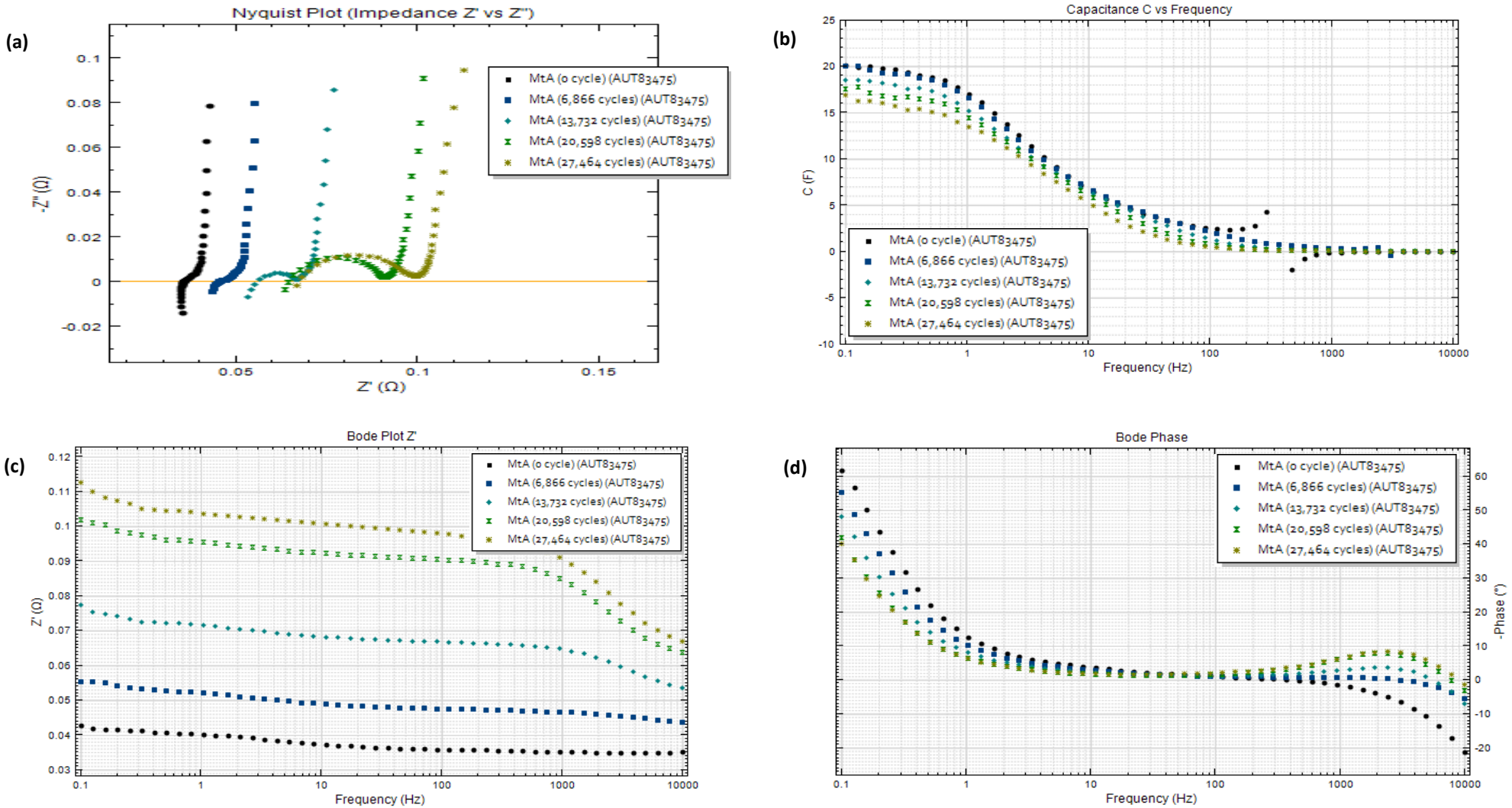
Appendix E-9: C10 EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z"), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



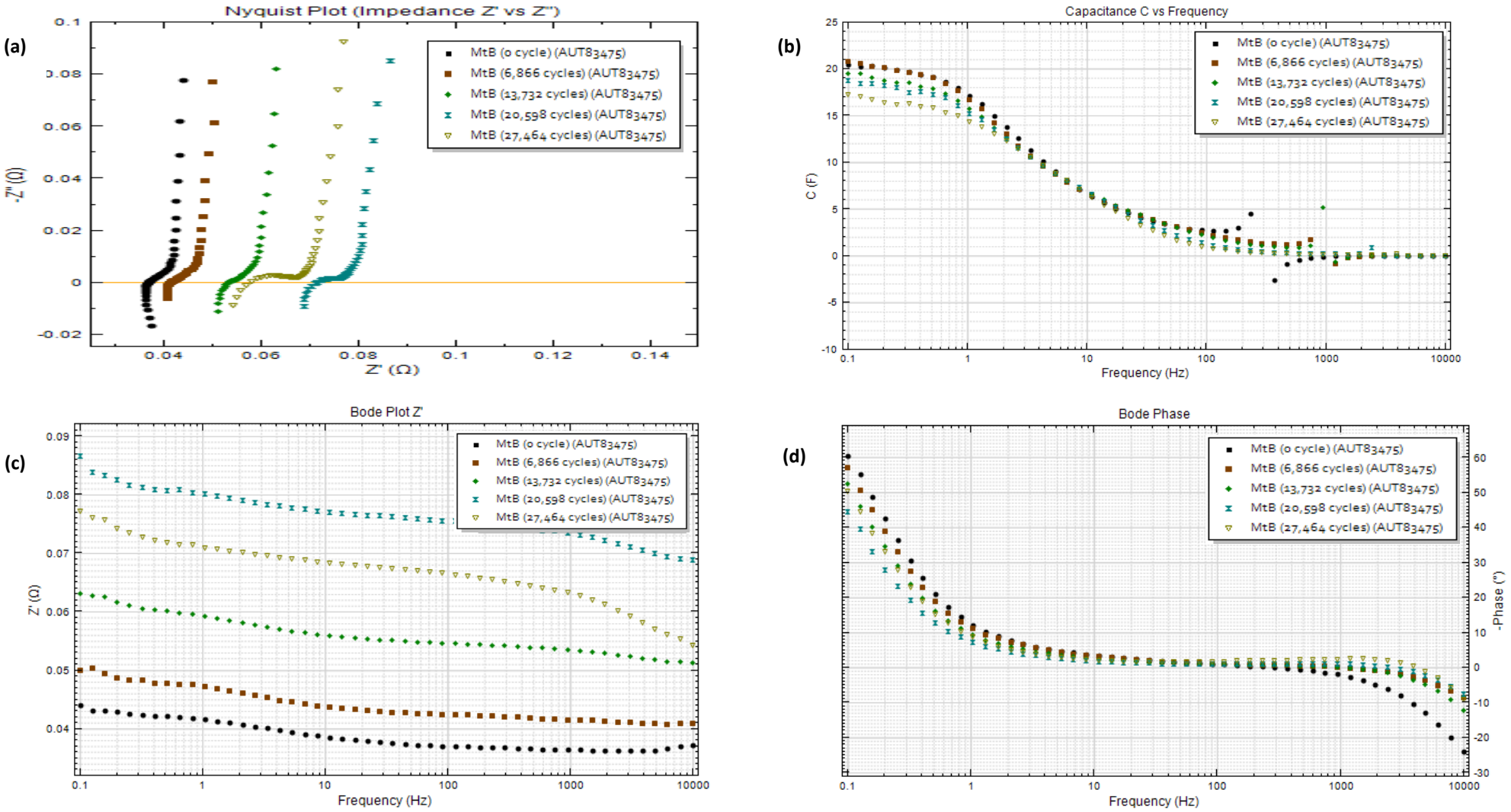
Appendix E-10: Module samples (a) B7, (b) B8, (c) C9 and (d) C10 CC test results (displaying SC lifetime voltage response to a 2A charge/discharge current profile over the accelerated test



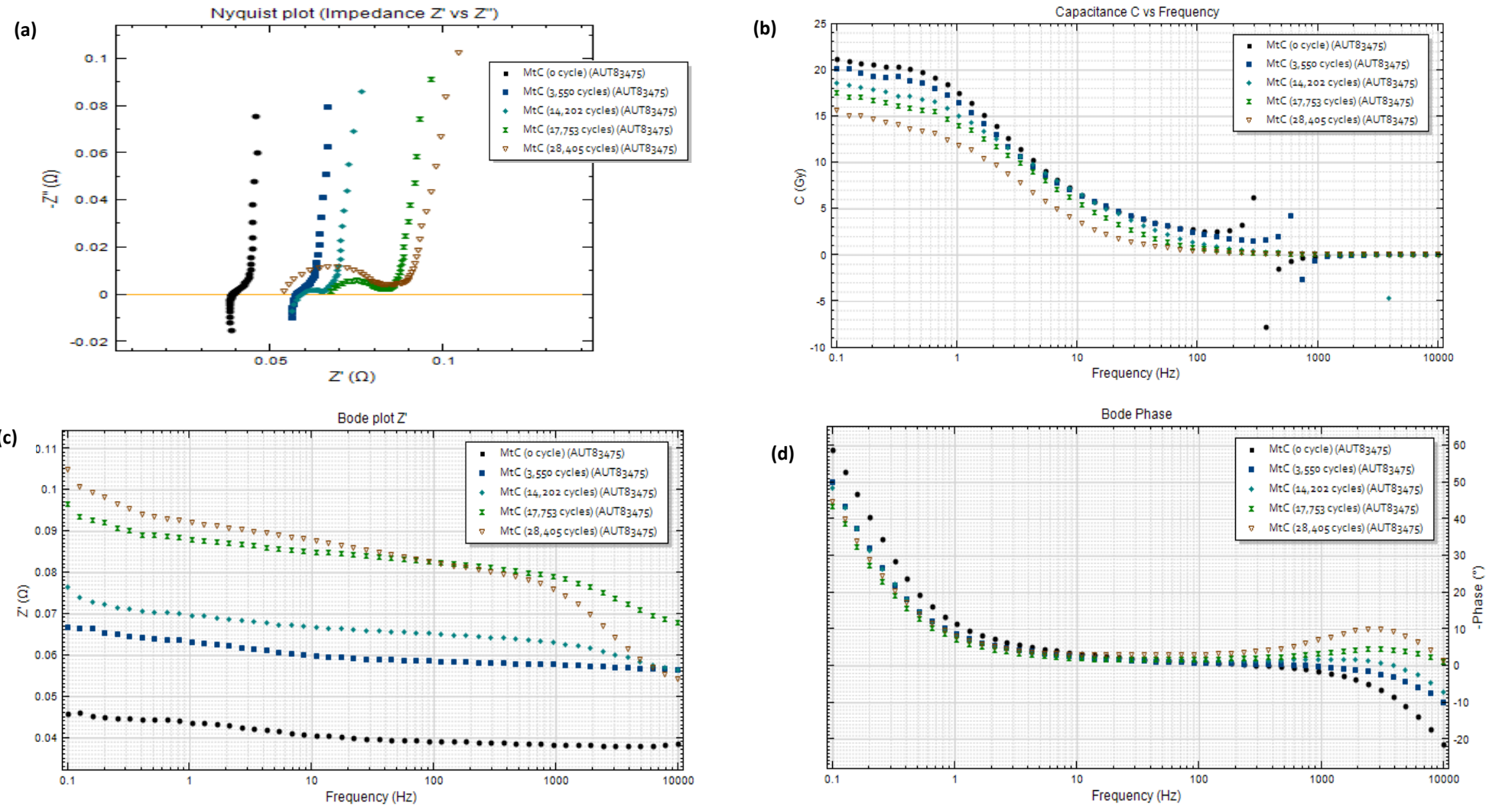
Appendix E-11: Module samples (a) B7, (b) B8, (c) C9 and (d) C10 CV test results (showing cyclic voltammograms at different stages of SC lifetime during cycling test) at scan rate 30 mV/s.



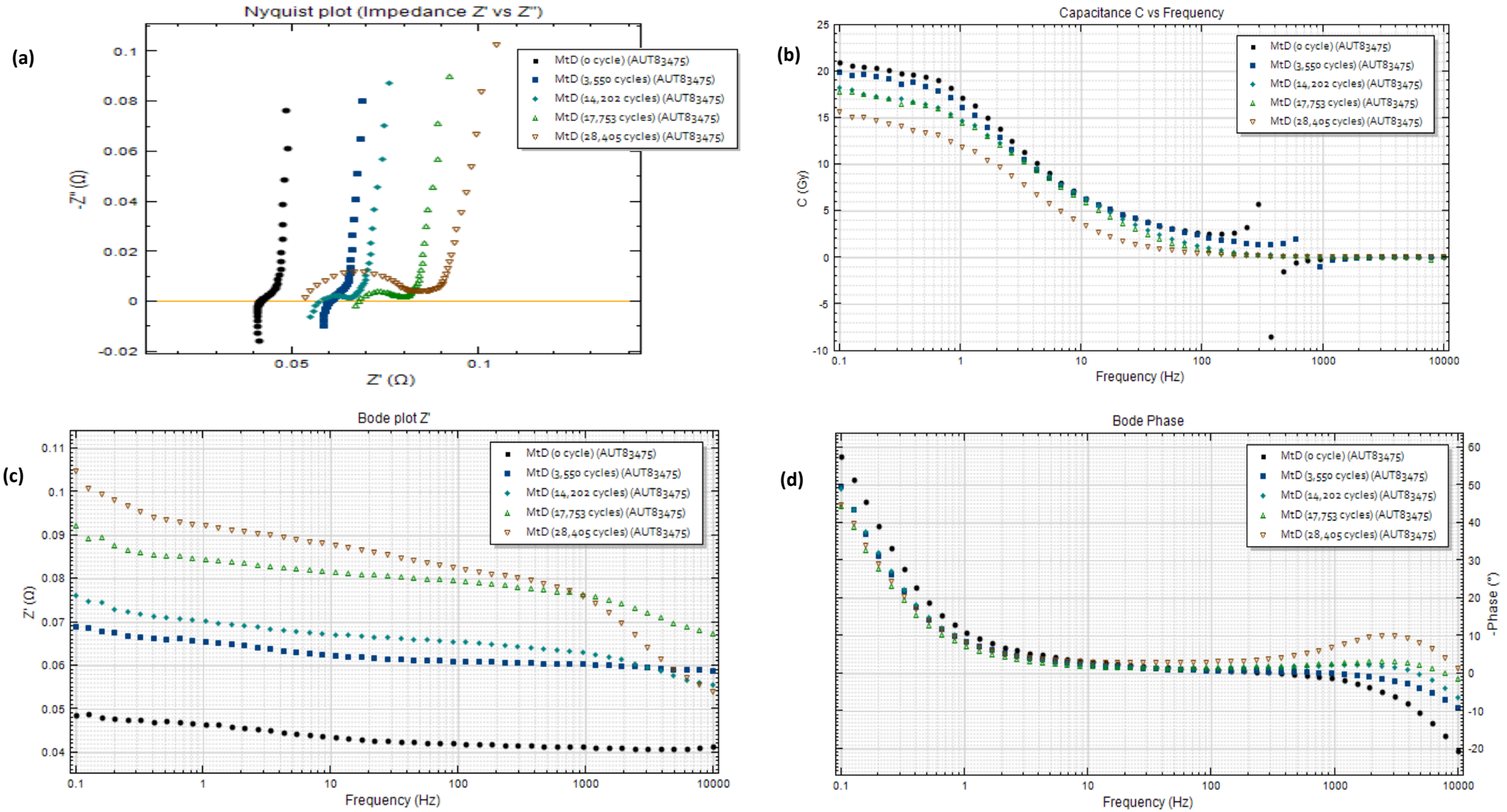
Appendix E-12: MtA EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



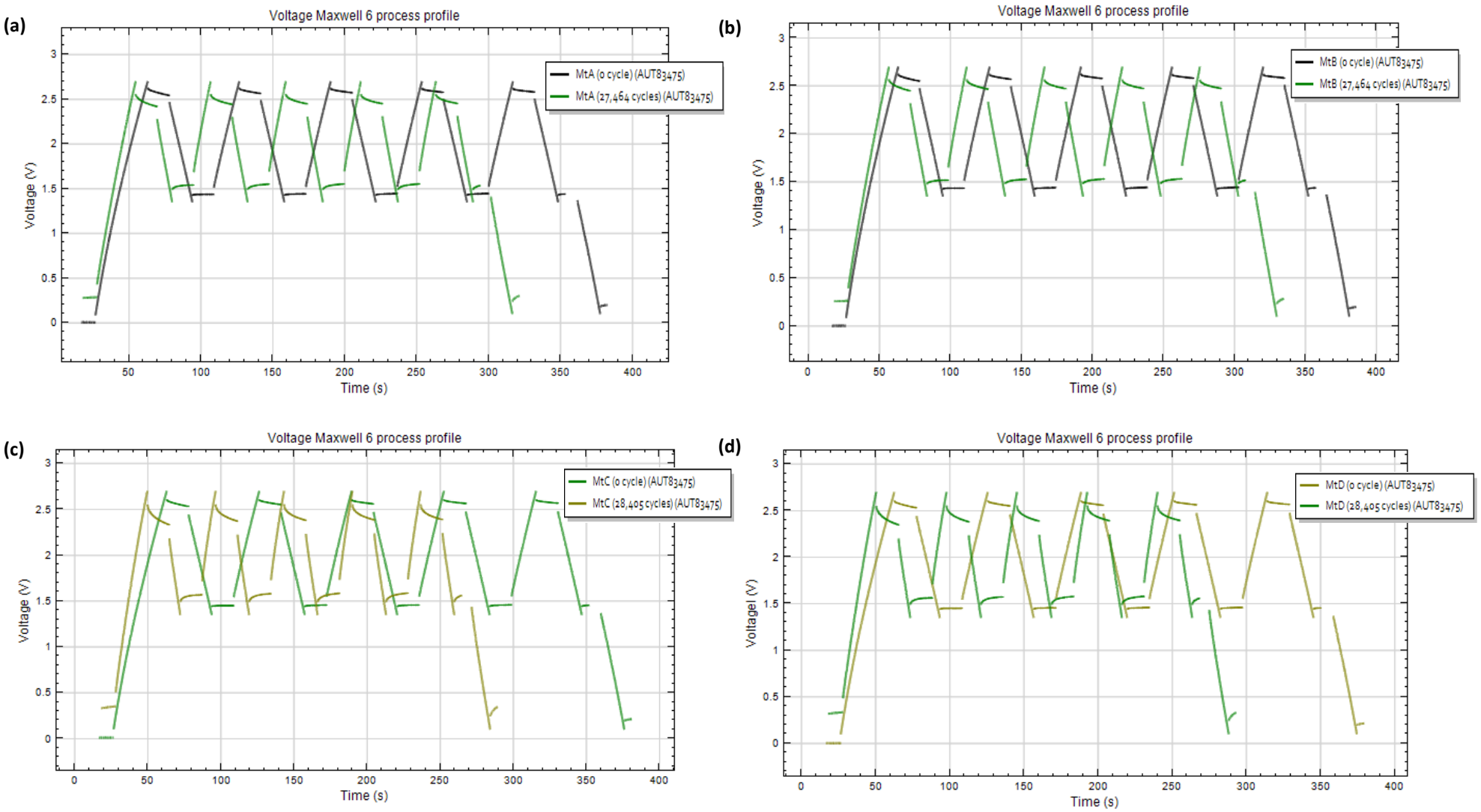
Appendix E-13: MtB EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



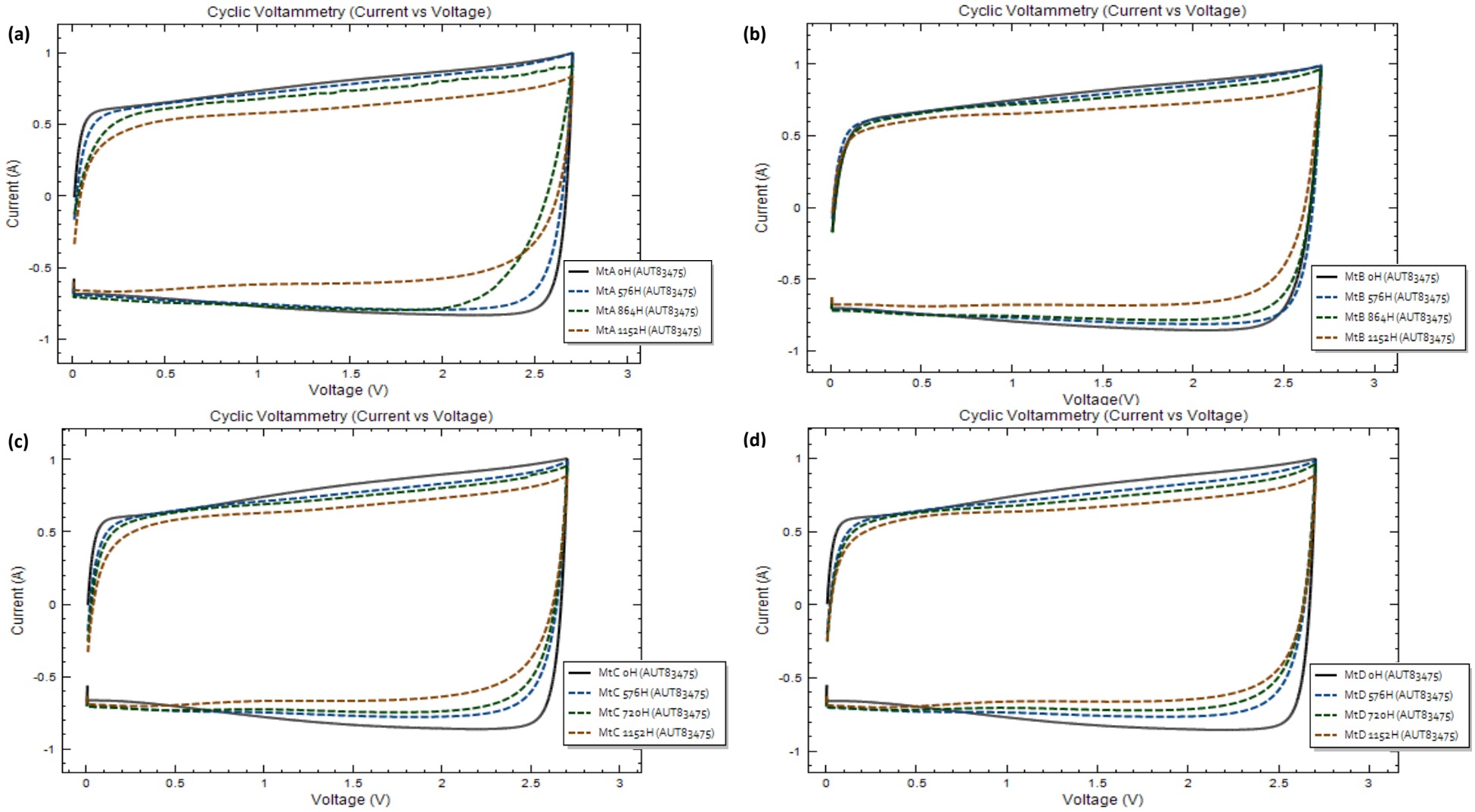
Appendix E-14: MtC EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



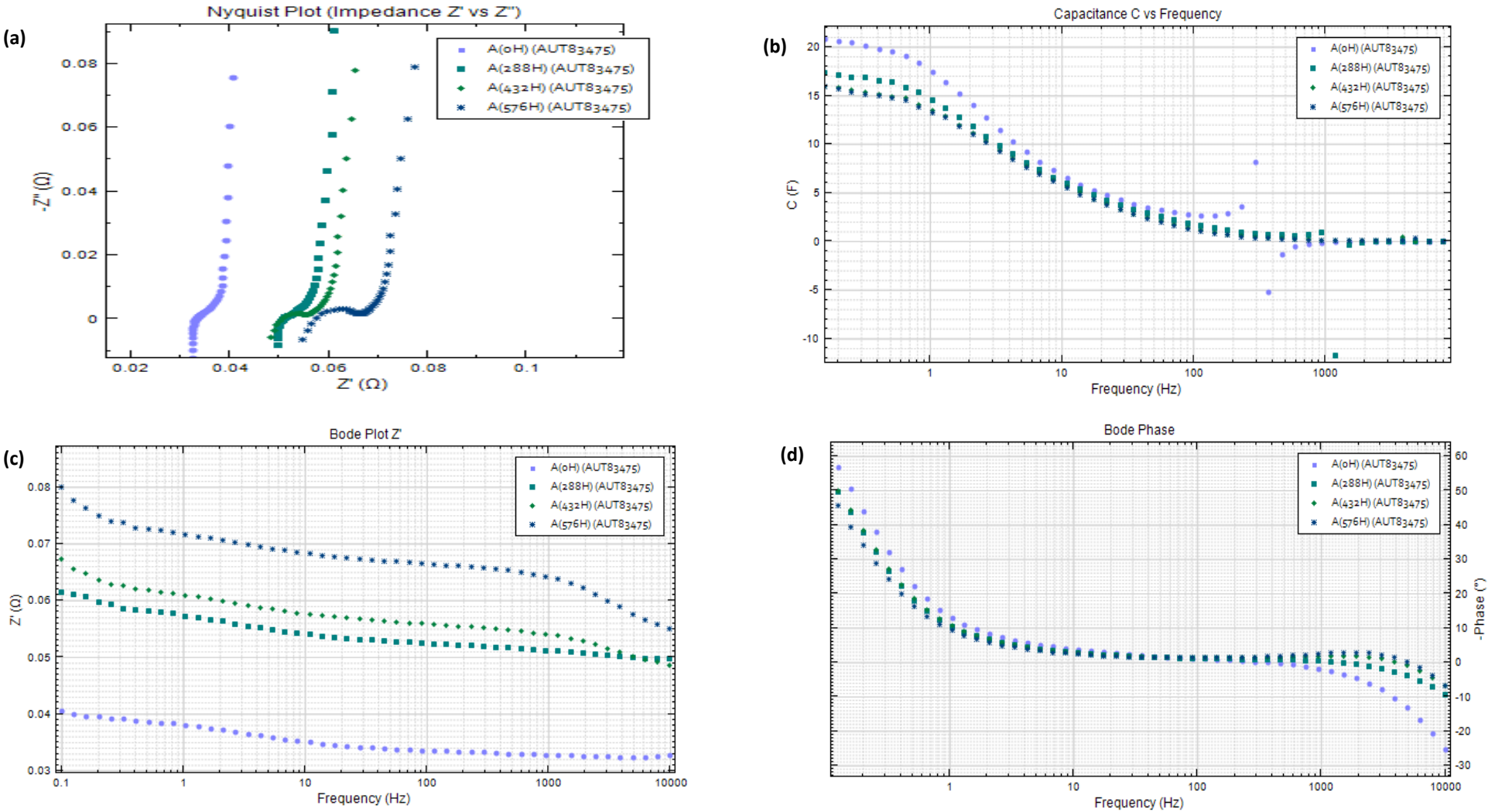
Appendix E-15: MtD EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z"), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



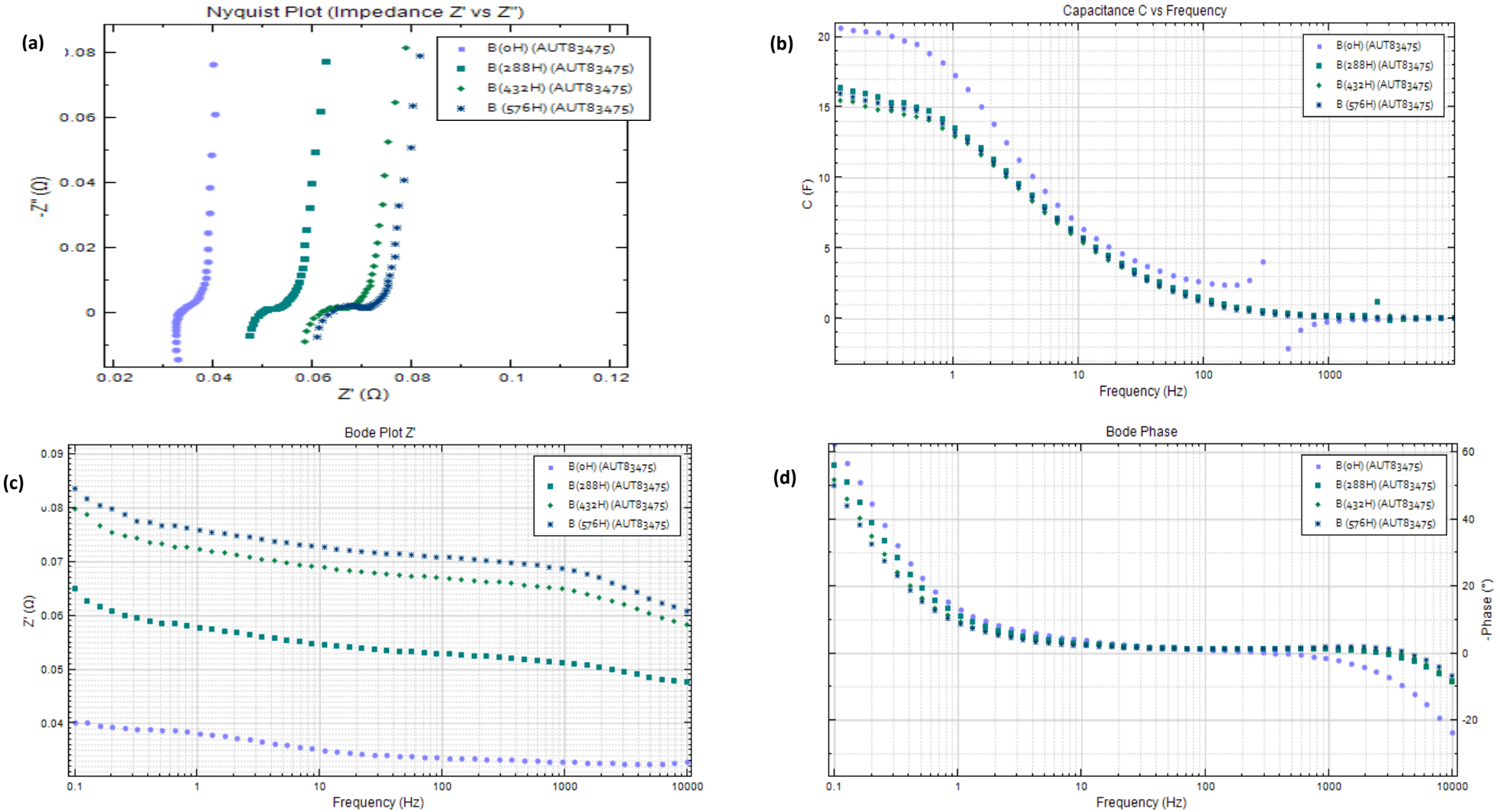
Appendix E-16: Module samples (a) MtA, (b) MtB, (c) MtC and (d) MtD CC test results (displaying SC lifetime voltage response to a 2A charge/discharge current profile over the accelerated test timeline)



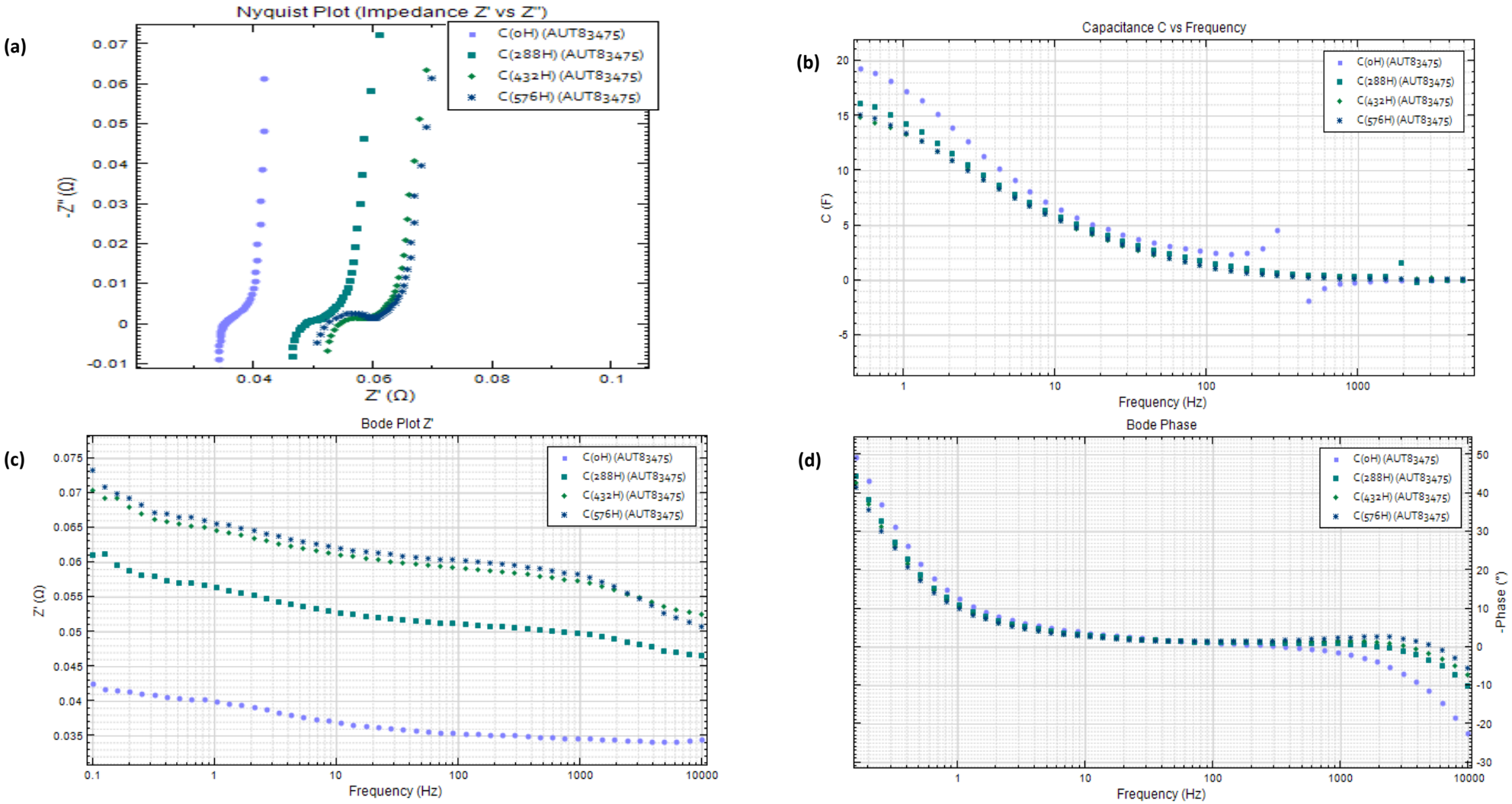
Appendix E-17: Module samples (a) MtA, (b) MtB, (c) MtC and (d) MtD CV test results (showing cyclic voltammograms at different stages of SC lifetime during load cycle tests) at scan rate 30 mV/s.



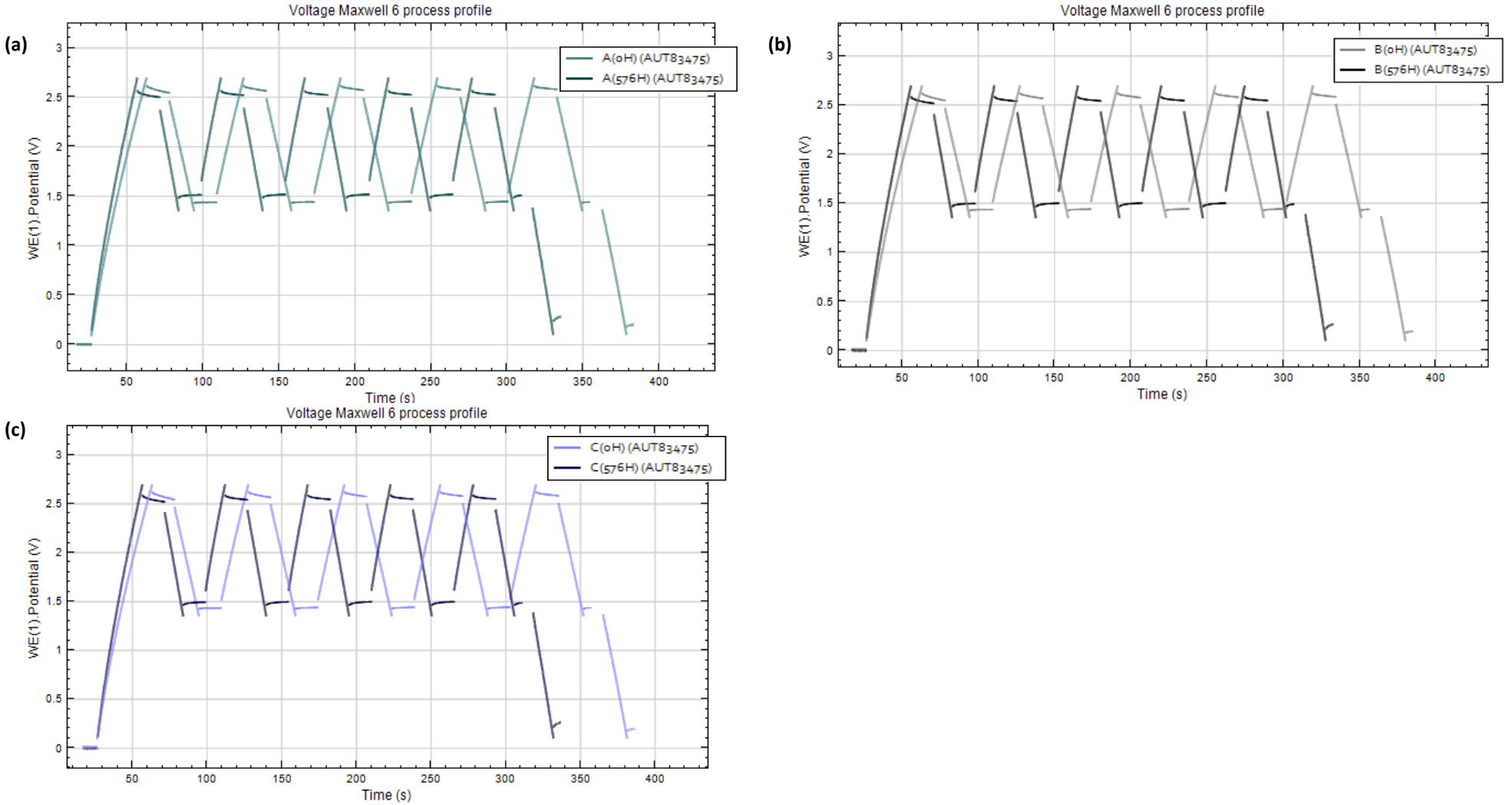
Appendix E-18: A EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



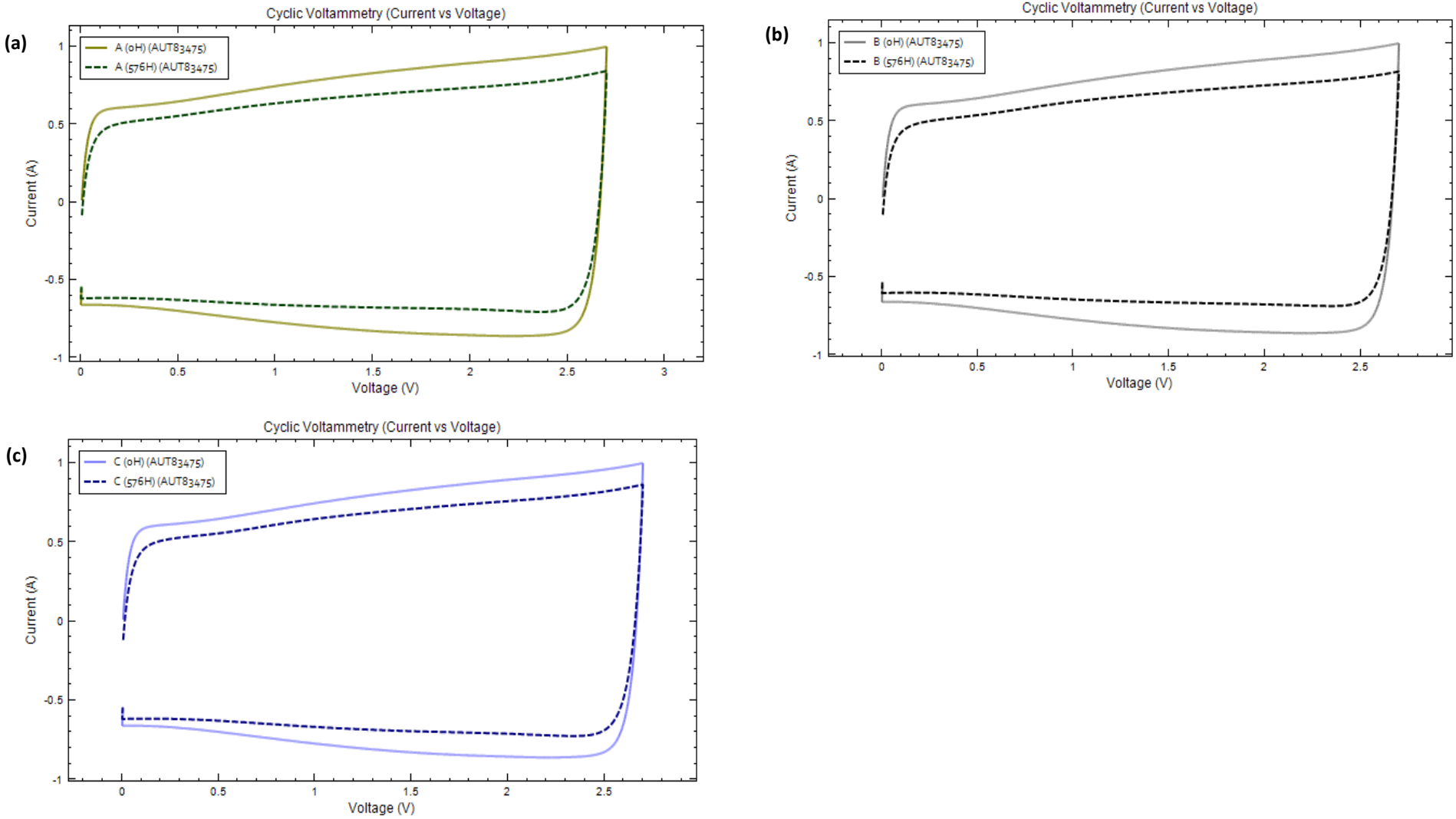
Appendix E-19: B EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



Appendix E-20: C EIS test results (showing SC lifetime where the most significant change is observed); (a) Nyquist plot (Impedance Z' vs –Z''), (b) Capacitance vs Frequency, (c) Bode Plot (Frequency vs Z'), (d) Bode Phase (Frequency vs Phase)



Appendix E-21: Module samples (a) A, (b) B, and (c) C CC test results (displaying SC lifetime voltage response to a 2A charge/discharge current profile over the accelerated test timeline)



Appendix E-22: Module samples (a) A, (b) B, and (c) C CV test results (showing cyclic voltammograms at different stages of SC lifetime during load cycle tests) at scan rate 30 mV/s.