Department of Electrical and Electronic Engineering

On-Board Health Monitoring of Power Modules in Inverters Driving Induction Motors

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MEng

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To

My respected parents,

Abstract

This thesis presents an on-board methodology for monitoring the health of power (converter) modules in drive systems. The ability to keep regular track of the actual degradation level of the modules enables the adoption of preventive maintenance, reducing or even eliminating altogether the appearance of failures during operation, significantly improving the availability of the power devices.

The novelty of this work is twofold: the complete system that is used to achieve degradation monitoring; combining the heating technique (to obtain thermal transient) and the measurement without additional power components such as IGBT, MOSFETS, which affects the reliability, power density and complexity. The only additional component is an analog measurement circuit, which can be integrated into the gate drive board. The test routine is carried out during non-operational periods and idle times. Trains are used as a case study, where checks for degradation are made when the train is not in use, such as at the end of the day, after daily operation or at the start before daily operation and other non-operational periods. It is important to keep the train at standstill while tests are carried out. Hence a methodology to heat the devices with current from the input supply while keeping the motor load at a stand-still is presented. Experimental results obtained from this show that it is possible to implement an on-board health monitoring system in converters which measures the degradation on power modules.

The work uses the concepts of vector control heating and structure function to check for degradation. It puts forward a system that is used on-board to measure the cooling curve and derive the structure function during idle times for maintenance purposes. The structure function is good tool for tracking the magnitude and location of degradation in power modules. Vector control gives the advantage of controlling the motor with field current and torque current (similar concept to DC motors).

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Thesis Contribution

The work presented in this thesis has resulted in two conference and one journal publications.

- A.M. Aliyu, S. Chowdhury and A. Castellazzi, "In-situ health monitoring of power converter modules for preventive maintenance and improved availability," *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, Geneva, 2015, pp. 1-10.
- A.M Aliyu and A. Castellazzi, ” Extracting Structure Functions of Power Devices in Induction Motor Drives” *Therminic 2016, Budapest*
- A.M Aliyu and A. Castellazzi,” Prognostic System for Power Modules in Converter Systems Using Structure Function” *IEEE Transactions on Power Electronics, (Under review).*

Learning from this activity has also resulted in a Journal

- J. Ortiz Gonzalez, A.M. Aliyu, O. Alatise, A. Castellazzi, L. Ran, P. Mawby, Development and characterisation of pressed packaging solutions for high-temperature high-reliability SiC power modules, *Microelectronics Reliability*

Contents

List of Symbols and Acronyms

Symbols	Definition
q_k	The rate at which the heat is transferred by conduction
λ	Thermal Conductivity
A	Surface Area
T	Temperature
ρ	Material Density
c	Specific Heat Capacity
c_v	Volumetric Heat Capacitance
R_{th}	Thermal Resistance
C_{th}	Thermal Capacitance
τ	Time Constant
t	time
Z_{th}	Thermal Impedance
°C	Celsius
ppm	Parts Per Million
μ	Micro ($x10^{-6}$)
Al	Aluminium
Si	Silicon
Cu	Copper
Al_2O_3	Aluminium Oxide
AlN	Aluminim Nitride
Si_3N_4	Silicon Nitride
AlSiC	Aluminium Silicon Carbide
SiC	Silicon Carbide
AlGaN	Aluminium Gallium Nitride
GaN	Gallium Nitride
AsGa	Arsenic Gallium
BeO	Beryllium Oxide
DBC	Double Bonded Copper
V_{ce}	Collector Emitter Voltage
$V_{ge(th)}$	Threshold voltage

R_G	Gate Resistance
I_h	Heating Current
I_m	Measurement Current
K	Kelvin
m	Milli($x10^{-3}$)
Rgint	Internal Gate Resistance
Ω	Ohms
Vge	Gate-Emitter Voltage
T_j	Junction Temperature
f	Frequency
n	Nano($x10^{-9}$)
ε	Rate of Change of Voltage With Temperature(K factor)
CΣ	Cumulative Thermal Capacitance
RΣ	Cumulative Thermal Resistance
$R_{channel}$	Channel Resistance
R_{drift}	Drift Resistance
ω	Angular Speed
V_s	Stator Voltage
V_r	Rotor Voltage
I_s	Stator Current
I_r	Rotor Current
R_s	Stator Resistance
R_r	Rotor Resistance
φ_s	Stator Flux
φ_r	Stator Flux
ω_e	Electrical Speed
ω_r	Rotor Speed
ω_{sl}	Slip Speed
L_o	Magnetizing Inductance
L_r	Rotor Inductance
L_{lr}	Rotor Leakage Inductance
L_{ls}	Stator Leakage Inductance
ζ	Damping Factor

ω_n	Natural Frequency

Acronym	Definition
IGBT	Insulated-Gate Bipolar Transistor
CTE	Coefficient of Thermal Expansion
TSEP	Temperature Sensitive Electrical Parameters
TIM	Thermal Interface Material
SEM	Scanning Electron Microscope
SAM	Scanning Acoustic Microscope
NTC	Negative Temperature Coefficient
HV	High Voltage
DUT	Device Under Test
DC	Direct Current
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NPT	Non-Punch Trough
IEC	International Electrotechnical Commission
DAQ	Data Acquisition
RMS	Root Mean Square
EMF	Electromotive Force
AC	Alternating Current
A/D	Analog to Digital Converter
IM	Induction Motor
FPGA	Field Programmable Gate Array
DSP	Digital Signal Processor
VSI	Voltage Source Inverter
SVM	Space Vector Modulation
HPI	Host Port Interface
PWM	Pulse Width Modulation
CMMR	Common Mode Rejection Ratio
ANPC	Active Neutral Point Clamped
MVD	Medium Voltage Drives
HEMTs	High Electron Mobility Transistors
WBG	Wide Band Gap

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Chapter 1: Introduction

1.1 Motivation

Power semiconductors are the basic building blocks of electrical power conversion applications and are central to a number of key societal infrastructures. Fig 1.1 gives an overview of the various silicon based semiconductor devices used for a wide range of power levels and switching frequencies[1]. Most of these applications are integral to our daily lives. In fact, according to [2], electric motors and the systems they drive are the single largest electrical end-use, consuming more than twice as much as lighting, the next largest end-use. It is estimated that electric motor driven systems account for between 43% and 46% of all global electricity consumption[2]. Over 90 % of this is represented by induction motors. About 25-30% of induction motor drives are driven by switched power converters using power semiconductors[3]. The number of switched power converters is growing in motor drive applications, automotive, renewable and other applications.

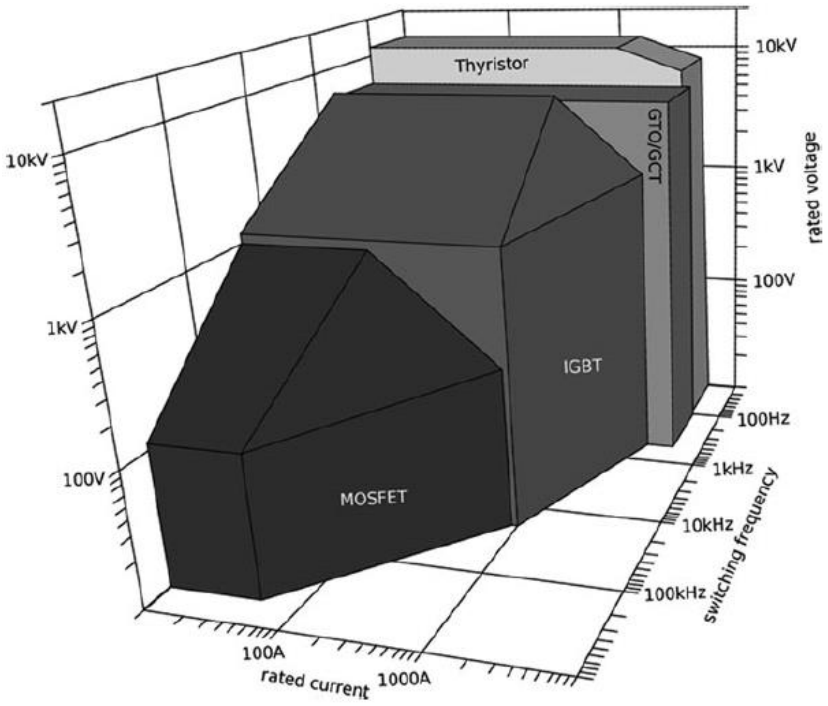

Fig 1.1: Power semiconductor devices and applications (reprinted from[1])

The drive for ever increasing power density in power electronics has led to tougher requirement of reliability and health management/monitoring as devices are exposed to more and more stressful operational conditions in harsher environment. Power converters that use insulated gate bipolar transistors (IGBT) modules are well established in automotive, rail-traction, aerospace, renewable energy and several other applications where the combination of environmental and load-derived thermal cycling can result in large and unpredictable fluctuations in operational temperature [4].

During operation the semiconductor device induces a temperature field inside the IGBT module, which evolves depending on the mission profile. The power module experiences several local thermal cycles defined by the train acceleration and braking processes [5]. In grid connected photo-voltaic (PV) and wind applications, the temperature variation is also dependent on the operating conditions and the unpredictable variation in the wind speed [6] .

For the sake of clarity in the previous and subsequent sections, some relevant definitions will be introduced:

- Mission profile- is defined as power processed over time of intended operation.
- Reliability- is defined as the ability of an item to perform required function under stated conditions for a certain period of time, which is often measured by probability of failure (chances that the item will fail) and frequency of failure (the number of times the item fails) [7]
- Availability- is defined as the probability to which an item will function as required when needed during the period of a mission. Availability is a function of both reliability and maintainability and is relevant to mainly repairable systems.
- Stress- is defined as the result of an applied force which causes a material to deform.

1.1.1 Power Module

A typical semiconductor power module is made up of different layers and several materials as illustrated in Fig 1.2. This is designed to provide

mechanical stability, electrical insulation and thermal conductivity [8]. The coefficient of thermal expansion (CTE) indicates the change of a component's size with a change in temperature. Specifically, it measures the fractional change in size per degree change in temperature at a constant pressure. As the temperatures of components inside the power module increases and decreases, the different materials expand and contract at different rates; this induces mechanical stress in layers between the different materials. A major reason for failures in IGBT modules is mismatched CTE of the various layers of materials used in their construction. The main failure mechanisms are wire-bond cracking, wire-bond lift off, solder joint fatigue, solder voids, aluminium reconstruction [9]. Fig 1.3 shows some of the main failure mechanisms, wire-bond lift off, solder fatigue and solder voids.

As a result of improvements made in wire bond reliability, it was shown in [10, 11] that solder fatigue of the substrate-to-base interface rather than wire bond lift-off is the limiting reliability factor. It has also been discussed in [8] that the substrate-baseplate location (X) features the highest mismatch in the CTE and the maximum temperature swing. For this reason, the focus is on the substrate-baseplate solder as a region of failure in the power module.

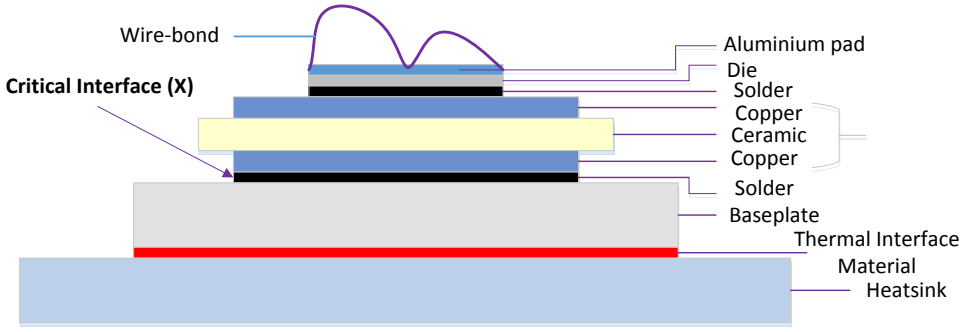

Fig 1.2**:** Illustration of conventional power module cross section

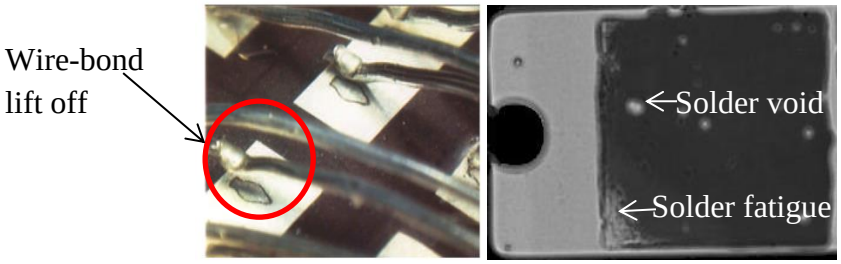

Fig 1.3: (Left) Wire-bond lift off (right) solder fatigue and solder voids[12]

The failure mechanisms need to be detected in order to prevent abrupt destruction of the devices and subsequent risk of system inoperability. The reliability and the availability are improved by monitoring the failure mechanism. The smaller the time it takes for a system to be repaired/maintained the higher its availability. Therefore to increase availability and detect the impending failure, pre-cursors of failure need to be defined. Some parameters related to the device or device structure are related to the failure mechanisms. The thermal response function (cooling or heating curve) as a result of power step excitation contains information of the device structure. Hence by measuring the thermal response function a change in the structure can be detected. The junction temperature then is an important variable to monitor degradation; the power modules are enclosed and provide no opportunity for a direct measurement of the junction temperature.

1.2 Aims and Objectives of the Work

With the prevalence of induction motor drives in power electronics applications and the need for health monitoring for reliability as motivation; this thesis presents the development and proof-of-concept demonstration of an on-board methodology for monitoring the health of power converter modules in induction motor drives. The aim of this thesis is to present a system that can measure the cooling profile of a power module (3 phase 2-level inverter) to derive the structure function during idle times of the equipment. The structure function, presented in detail in chapter 3 is a powerful tool for tracking the extent and location of degradation in power modules. The stated aim is carried out by combining the power device heating technique and the measurement without additional power components [13], except for the measurement circuit

which consists of only analog components and can be integrated into the gate drive board. Single chip, non-punch through (NPT) power modules have been used in this work. The specifics of other technologies such as trench devices have not been considered. The concept in this work however, can be applied to multichip modules and other IGBT technologies.

In order to implement and validate the on-board health monitoring methodology the objectives are as follows:

I. Identifying the parameter to be used to measure degradation to meet the aims of the project.

II. Extracting thermal transients, thermal impedance curves, time-constants and structure function

III. Implementing a control strategy to heat up devices on a 3 phase 2-level inverter without rotating the motor or changing the connections or adding components

IV. Designing a measurement circuit that will give an accurate temperature measurement without interfering with the converter operation

V. Presenting a system prototype to validate on-board health monitoring

1.2.1 Background

Similar research in online health monitoring of power devices/modules have been carried out in the past. Prognostic real-time systems in [14, 15] present a method that uses compact thermal models to predict temperatures of inaccessible locations of a power module; the information then obtained is combined with data about the reliability analysis to predict failure mechanisms. Although those methods might be able to predict failure, they give an estimate, hence doesn't provide the actual variation in the quantity of the failure mechanism. Also, as time elapses the aging of the power modules will affect the integrity of the thermal model. Adaptive models for real-time monitoring have been presented in [16-20], which compare physical measurements with a model estimate to accurately track the junction temperature of the device under consideration. The limitations of [16-18] are

that they use the collector emitter voltage, which is noisy and intermittent due to the non-linearity of the I-V characteristic of the IGBT, hence this method is dependent on the operating region. [19] requires extending the turn-on time by making modifications to the gate drive in order to measure the temperature online. In [20] temperature sensors need to be embedded in the baseplate to detect the change in temperature distribution, this method is affected by the positioning of the sensors.

As opposed to the real-time monitoring solutions, which take measurements of the TSEP of the device during operation of the inverter, in the methodology proposed here, measurements are taken when the system is not operation(during maintenance routines). The in-situ method in [21-23] to which this work mainly makes reference to, works by injecting external currents into the power module during idle times. The high current is injected externally to heat the devices. The methods presented in these papers show the ability to successfully measure degradation due to wire-bond lift off and solder fatigue by measuring the voltage at high currents (wire-bonds) and the heating curve (solder fatigue). However, in [21-23] a set of relays need to be inserted to select which device undergoes test, somewhat limiting of the applicability of the solution in some on-board applications. The method in [24] presents a similar control concept of a quasi-real-time prognostic method in simulation, however in practice this will also be subject to noisy and intermittent collector emitter voltage which makes it hard to implement.

The work presented in this thesis provides a system that uses the structure function [25] to measure degradation on-board without making changes to the connections, making use of additional components or dismounting it; it is also able to point out if and where degradation occurred in the structure of the device.

1.3 Thesis outline

In Chapter 2, the power module structure and its reliability are discussed. Chapter 3 entails obtaining the thermal impedance and the theory behind the structure function and how the structure function can be extracted. In Chapter

4, the heating scheme and the measurement circuit design methodologies are introduced. In Chapter 5 the experimental implementation of the heating scheme and measurement system are elaborated. The challenges encountered are presented along with the results validating the on-board measurement methodology in Chapter 6. Conclusions are presented in Chapter 7.

Chapter 2: Power Modules Structure & Reliability

2.1 Introduction

This chapter presents the theory of heat conduction in the power module. This provides the opportunity of introducing a simplified method of analysing the heat flow path and how the heat flow path is relevant to this work. The structure of power modules and the materials used in a conventional power module will be presented. It will elaborate the benefits of the materials in the power module and how the properties of these materials are susceptible to the failure mechanisms. This chapter will also discuss the failure mechanisms and how they develop in modules. Additionally in this chapter the variables used to determine and evaluate failure mechanisms are elaborated, identified and their functions are discussed. A suitable variable will be chosen for this work and the reason behind this choice will be presented.

2.2 Heat Transfer in Power Devices

Conduction, convection and radiation are the three main mechanisms by means of which heat is transferred. When there is a temperature gradient existing in a solid, heat flows from the higher temperature region to the low temperature region. This process is known as conduction. In this mode, heat transfer is achieved through a complex sub microscopic mechanism in which atoms interact by elastic and inelastic collisions to propagate the energy from regions of higher to regions of lower temperature [26].

Conduction occurs in liquids and gases, but is not the dominant heat transportation mechanism. Convective currents set in motion bring about the transportation of heat in fluids. Hence, transportation of heat on both the microscopic and macroscopic scale. Convection is a more effective way of transporting heat than conduction which is limited to microscopic transport of energy.

The third means of transporting heat from one point to another is radiation. Heat transfer by radiation in solids occurs when the object is transparent or translucent. For the sake of analysis heat conduction and convection is solely considered in power semiconductors because other forms of heat transfer are negligible. Convection happens between the heat sink and its surroundings, and because convection is more effective way of transporting heat, the heat sink is considered to be a constant thermal termination for the heat path in most cases.

2.2.1 Analysis (Conduction)

Power semiconductor devices have heat transfer in the form of heat conduction. The general equation that describes heat transfer in conduction can be written as [27]:

$$\rho c \frac{\partial T(x,y,z,t)}{\partial t} = \nabla\left(K \nabla T(x,y,z,t)\right) + H(x,y,z,t) \tag{2.1}$$

Where:

ρ = *material density*

c= specific heat

K= matrix of thermal conductivity coefficients

T=Temperature

H=Heat Generation rate

The heat conduction in power device packages can be analysed in a simpler way by considering a thermally isotropic material, where heat conduction in power semiconductor devices can be considered as one-dimensional if the following statements are true:

- Thermal conductivity of silicon is constant (λ). There are some exceptions, silicon has a nonlinear heat conductance at higher temperatures and radiation effects are at higher magnitudes. These effects are not very pronounced in the temperature range used when characterizing the packages.

- Uniform power density and heat generation should occur in a volume with lateral dimensions much bigger than the vertical dimension of the chip, so negligible temperature gradient exists in adjacent cells [27].
- Heat is mainly extracted from the baseplate/heatsink[28]

So for a thermally isotropic material with a constant λ equation (2.1) can be written as:

$$\rho c \frac{\partial T(x,y,z,t)}{\partial t} = \lambda \nabla^2 T(x,y,z,t) + H(x,y,z,t) \tag{2.2}$$

For one dimensional heat conduction and uniform power density equation (2.2) can be written as:

$$\rho c \frac{\partial T}{\partial t} = \lambda \frac{\partial^2 T}{\partial x^2} + H \tag{2.3}$$

The analytic solution for conduction in a one-dimensional system is presented in Appendix 1.

2.2.1.1 Thermal Resistance/Impedance

Provided there is a temperature gradient in a solid as stated earlier, heat will flow from a high temperature region to a lower temperature. The rate at which the heat is transferred by conduction, q_k is proportional to the product of the temperature gradient dT/dx and area A through which heat is transferred[26]:

$$q_k \propto A \frac{dT}{dx} \tag{2.4}$$

In the above relation T(x) is the temperature at a given location and x is the distance in the direction of the heat flow. Heat flow is also affected by a constant known as thermal conductivity λ, which is a material property of the medium. The above equation can then be written for a homogeneous as

$$q_k = -\lambda A \frac{dT}{dx} \tag{2.5}$$

The negative sign indicates the slope of the temperature with respect to the distance x. As the rule is that heat will move from the higher temperature to lower as the distance increases, the sign will be negative.

The heat conduction process can be modelled by a circuit diagram, which consists of resistive and capacitive elements R/C elements only. The similarities between electrical and thermal systems are shown in Table 2.1. The thermal resistance can be elaborated by considering (2.5), and the volume presented in Fig 2.1.

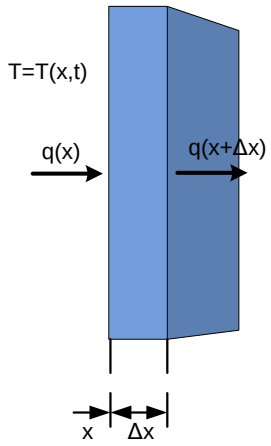

Fig 2.1: Illustration of one dimensional heat flow

The starting point x, can be considered as the origin (x=0) in this case and the temperature at the origin is T1 while the temperature at Δx is T2. Equation (2.5) can then be written as

$$\frac{q_k}{A}\int_0^{\Delta x} dx = -\lambda \int_{T1}^{T2} dT \tag{2.6}$$

$$\frac{q_k}{A}\left[x\right]_0^{\Delta x} = -\lambda \left[T\right]_{T1}^{T2} \tag{2.7}$$

$$q_k = \frac{A\lambda}{\Delta x}\left(T1 - T2\right) = \frac{\Delta T}{\frac{\Delta x}{A\lambda}} \tag{2.8}$$

Table 2.1 Correspondence of electrical and thermal quantities

Thermal quantities		**Unit**	**Electric quantities**		**unit**
T	Temperature	K, C	V	Voltage	V
q_k	Heat flow	W	I	Current	A
Rth	Thermal resistance	K/W	R	Electric resistance	ohms
Cth	Thermal capacity	J/K	C	Capacity	F
$\boldsymbol{\tau_{th}}$	Time constant	s	τ	Time constant	s
Zth	Thermal impedance	K/W	Z	Impedance	ohms

In the equation above ΔT, the temperature difference between two points causes the heat flow. This is the same in electrical circuits where potential difference leads to a current flow. For this reason, current and the heat flow can be considered to be analogous. The electrical equivalent to (2.8) is Ohms law

$$I = \frac{\Delta V}{R} \tag{2.9}$$

It can be observed that Δx/Aλ is equivalent to the thermal resistance, also inversely proportional to the heat flow, in a similar way the electrical current is inversely proportional to the electrical resistance. This analogy is a convenient tool, especially for visualizing complex situations.

The thermal resistance can be used to visualize situations only during equilibrium. For most applications the use of thermal resistance is sufficient, but for this work, as the aim is to ascertain any changes in the structural integrity, the thermal impedance is needed.

The thermal impedance (Z_{th}) is equivalent to RC-network of certain order which represents the physical layers of the system with individual thermal resistances and capacitances; this is explained in more detail in the next

chapter. Generally the transfer function of the thermal system for an arbitrary power profile as suggested in [29, 30], is:

$$\Delta T(t) = \int_{-\infty}^{\infty} \dot{Z}_{th}(\tau) * \Delta P(t-\tau) d\tau \qquad (2.\ 10)$$

Where

$$\dot{Z}_{th}(t) = \frac{d\, Z_{th}}{dt}(t) \qquad (2.\ 11)$$

For constant power dissipation, the thermal impedance in (2.10) can be reduced to

$$Z_{th}(t) = \frac{\Delta T(t)}{\Delta P} \qquad (2.\ 12)$$

2.3 Structure of Power Modules

The conventional power module is usually made up of eight layers plus the wire bond as seen in Fig 2.2 . The colors are indicative of the material used, as surmarissed in Table 2.2, which also indicates typical thickness and the coefficients of thermal expansion. The coefficient of thermal expansion indicates change of a component's size with a change in temperature. Specifically, it measures the fractional change in size per degree change in temperature at a constant pressure. The purpose of the various layers will be outlined in the following subsections.

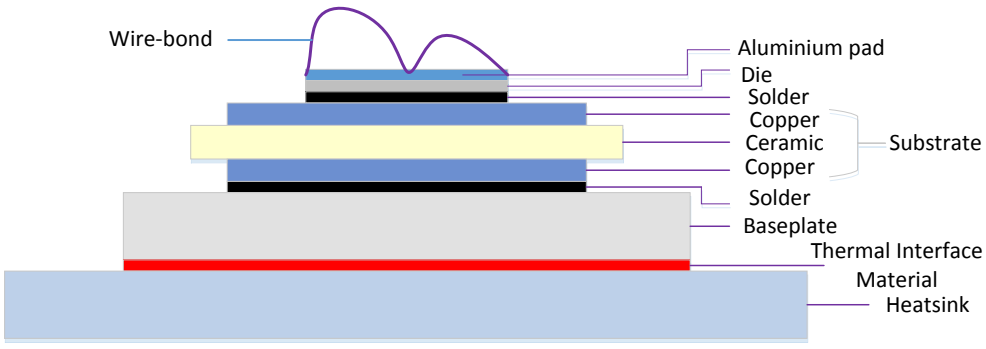

Fig 2.2: Cross-section representation of a conventional power module

Table 2.2: Properties of materials used in conventional power module [8]

No	Material	Thickness (µm)	CTE ppm/°C
1	Aluminium (Al)	4-5	~22
2	Silicon (Si)-Chip	70-500	~3
3	Solder	100	-
4	Copper (Cu)-Substrate	280	~17
5	Al_2O_3 or AlN or Si_3N_4-Substrate	1000	~7/4/3.3
6	Copper (Cu)-Substrate	280	~17
7	Solder	180	-
8	Cu or AlSiC-Baseplate	4000	~17/8

2.3.1 Die

The chip is a silicon semi-conductor device, although other semiconductors have been also introduced (SiC, GaN, AsGa)[12]. The die is usually connected to other chips, gate terminal and power teminal by wire bonds or bump interconnection technology. The wire bond is made up of either aluminium or copper. The wire bonds are attached to the silicon chip via ultra-sound bonding[8]. A conventional commercial power module is presented in Fig 2.3.

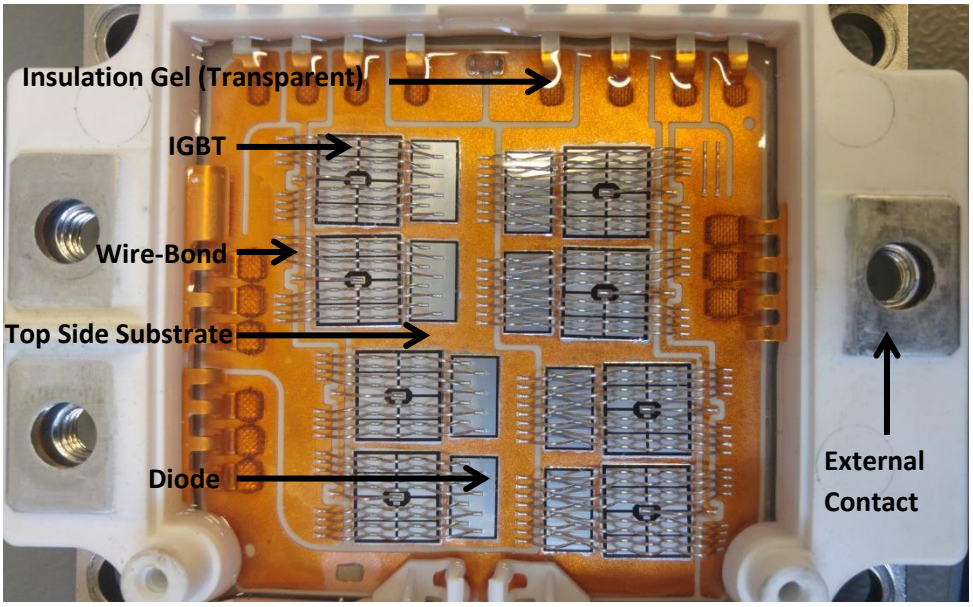

Fig 2.3: Conventional half bridge module with devices connected in parallel

Fig 2.3 shows that wire-bonds connect IGBTs and diodes both directly and via the substrate. Both the IGBT and the diodes have two sides to which connection must be made. For the IGBT the top side consists of the gate and the emitter, while the bottom side is the collector. For the diode, the bottom is the cathode and the top side is the anode.

2.3.2 Solder

The solder in the power module structure provides a mechanical support for the die to be attached on the substrate, electrical contact for the collector and the cathode and also a thermal path to cool down the device. The solder used is usually an alloy of tin, silver, lead, copper or nickel. In most applications the tin-lead alloy is common. Recently other alloys have been introduced that exclude lead due to its harmful effects and worldwide health and safety regulations. Therefore, tin-silver (Sn-3.5Ag) is a preferable solder in a flux-less reflow soldering process [31, 32]. The acoustic scan of the solder layer of the IGBT and the diode and an image of a cross section showing solder are presented in Fig 2. 4.

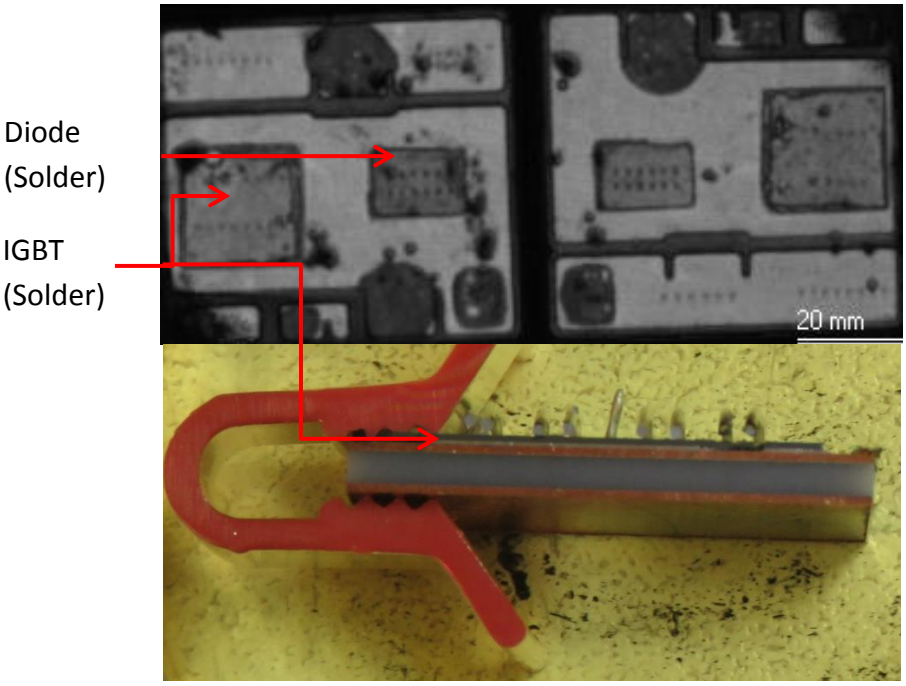

Fig 2.4: Scanning acoustic microscope image of IGBT and diode solder & cross-section showing solder layer

2.3.3 Substrate

The substrate is designed to be electrically insulating and thermally conducting. It consists of two copper layers on its sides (top and bottom) with ceramic inbetween. The copper on the top provides electrical connection between the various chips as mentioned. Typical materials used for substrate manufacturing are Al_2O_3, AlN, Si_3N_4, BeO. These substrates are coated with copper layer by one of the following methods: copper thick film technology using screen printing, copper on ceramic by electro-less plating, direct copper bonding through eutectic oxide bonding, and active metal braising.

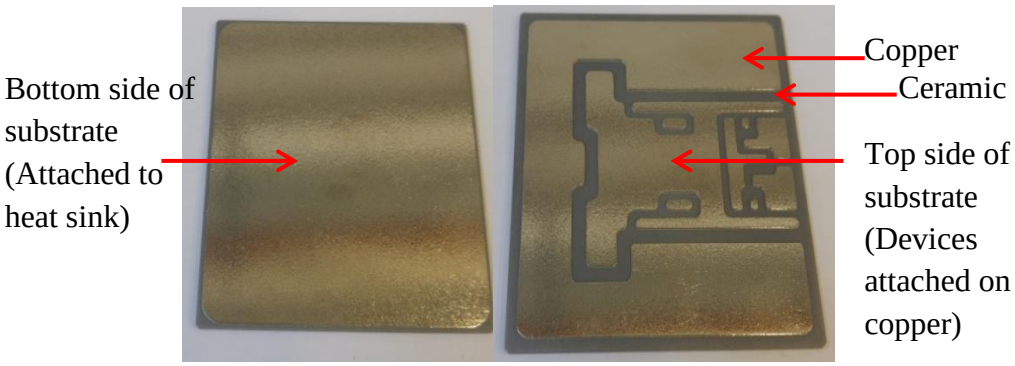

Fig 2.5: Bottom and top side of ceramic substrate

Fig 2.5 shows the photographs of bottom and top side of a DBC substrate. In such a structure the copper layer provides the ability to carry high current and the ceramic tile provides high voltage insulation[33]. AlN has a higher thermal conductivity than Si_3N_4, resulting in better heat removal from the device attached to it. However, Si_3N_4 has the advantage when considering the thermal expansion and fracture toughness. This is because the CTE of Si_3N_4 is closer to the silicon as it can be seen from Table 2.2 and it has high resistance to brittle fracture during thermal cycle.

2.3.4 Base Plate

The baseplate is the external interface to the heatsink. It is situated between the solder underneath the substrate and the thermal interface material/heatsink. The base plate is based on nickel plated copper slabs. Other materials are metal matrix composites such as copper matrix composites reinforced with diamond, aluminium matrix reinforced with SiC or carbon-reinforced composites. The baseplate provides an effective thermal path that links the substrate to the heatsink or cold plate by spreading the heat. An image of a typical baseplate is presented in Fig 2.6.

Fig 2.6 : Baseplate of an IGBT module & plastic housing

2.3.5 Silicone Gel

The devices are covered by an encapsulating silicone gel as shown in Fig 2.3. Silicone gel and a combination of hard epoxy are used to produce this material. The power devices are coated by silicone gel for environmental and mechanical protection. An additional plastic housing shown in Fig 2.6 is used to contain the gel.

2.3.6 Thermal Grease

A thermal grease is used to improve the thermal conduction from the baseplate to the heatsink. The thermal grease is used to fill in the air gaps between the baseplate and the hatsink as shown in Fig 2.7. Air has very low thermal conductivity, so thermal grease is used. Heat transfer occurs at a slower rate with the airgaps than with the thermal grease filled gaps.

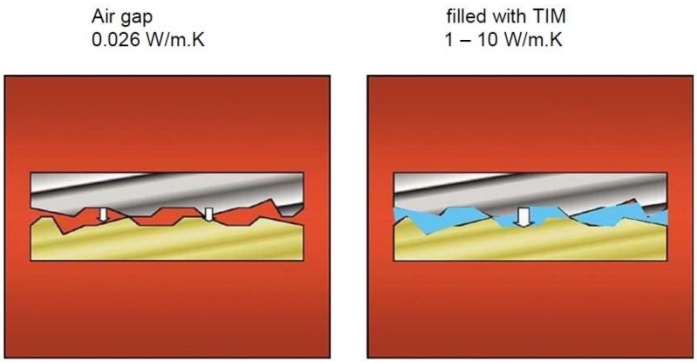

Fig 2.7: Illustration of thermal grease used to fill air gaps (reprinted from [34])

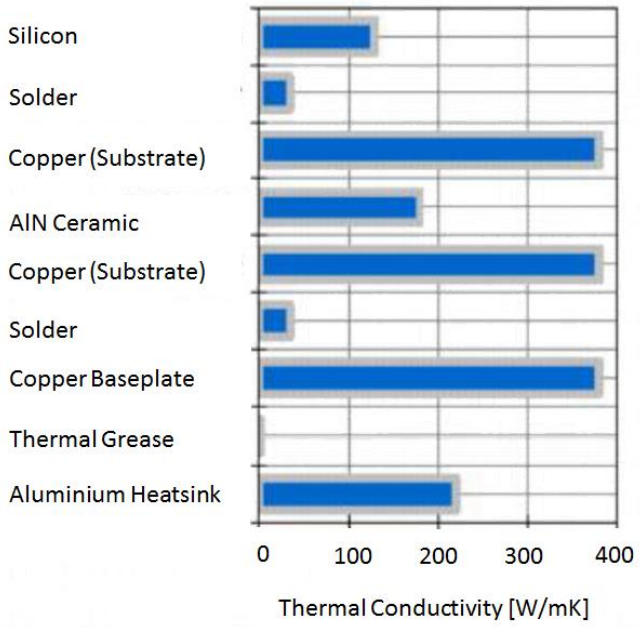

Fig 2.8: Thermal conductivity of materials used in a module compared to thermal grease (reprinted from[34])

It is important to note that, although the thermal grease has a higher heat conductivity than the air gaps, it has a relatively low conductivity compared to

the other components used in the power module structure as it can be seen in Fig 2.8. This means that although the thermal grease is needed to fill in the air gaps, an excessive amount will actually increase the thermal resistance. A solution to this is proposed by using an inhomogeneous stencil pattern (Honeycomb shape) to minimise the air being trapped under the module after mounting. A range of thermal foils are also used as thermal interface materials example of these are: thermosilicone foil, thermal wax coated Aluminium foil and carbon foil. Knowledge of the application can aid in choosing the best thermal interface material. The potential for the use of nano-technology has been discussed in [34] to improve thermal conductivity.

2.4 Failure mechanisms

A major reason for failures in IGBT modules is mismatched coefficients of thermal expansion (CTE) of the layers an IGBT consists of. This mismatch causes strains to both the bond wires and the soldering of the IGBT modules thus causing the IGBT modules to fail over time [8, 35]. These failure mechanisms wire-bond cracking, wire-bond lift off, solder joint fatigue, solder voids, aluminzation e.t.c are presented below[9].

2.4.1 Wire-bond Fatigue

Power modules with multichips for high power applications usually include up to 800 wedge bonds. Most of the wire-bonds are located on the active areas of the chips. This means that the wire-bonds experience the full temperature swing due to power dissipation in the power devices and the ohmic self-heating of the wires.

Failure of wire-bonds relate to the stress between the wire bond and point of contact by repeated expansion and contraction. The failure of a single or of multiple bond wires causes a change either in the contact resistance or in the internal distribution of the current, such that it can be traced by monitoring V_{ce} [36]. The loss of a single wire-bond leads to a cyclic process that leads to the quick destruction of the power module. The loss of wire-bonds means that the remaining wire-bonds need to carry an increased amount of current, which

leads to an increase in the ohmic self-heating of the wire-bonds. Wire-bond fatigue can occur in the form of wire-bond lift off and wire-bond cracking.

2.4.1.1 Wire-bond Lift Off

Wire-bond lift off usually occurs on the bonds present on the chip region. This is due to the fact that the connections made on the copper substrate experience a lower temperature swing than the connecting points on the chip. Moreover the CTE disparity between copper and the aluminium wire-bonds is less than that between aluminium and silicon.

There is experimental evidence that the crack leading to failure is initiated at the tail of the wire-bond and propagates within the material until the wire-bond completely lifts off [8]. Fig 2.9 shows a scanning electron microscope (SEM) image of a single wire-bond lift off.

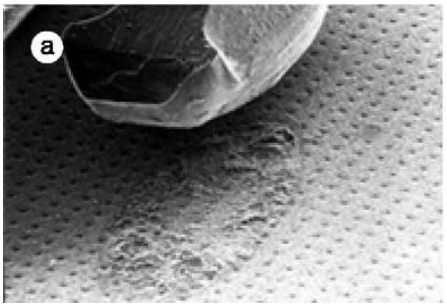

Fig 2.9: SEM image wire-bond lift off (reprinted from [8])

There are two main methods used in order to dampen the progress of this failure mechanism. Some power modules have a strain buffer on the chip. This is one of the countermeasures employed using a molybdenum plate soldered onto each chip as a strain buffer; the wires are then bonded on the molybdenum plate [37]. The aim of this buffer is to eliminate the thermo-electric stress that occurs by distributing the CTE mismatch across the molybdenum layer. The other solution is covering the wire-bonds with a coating layer. In [8], a comparison between non-coated wire-bonds and coated wire-bonds was carried out. The results indicate that the coated wire-bonds effectively slow down the failure mechanism by a considerable number of cycles.

2.4.1.2 Wire-bond Heel Cracking

Wire-bond cracking is caused by cyclical lateral bond area displacement as can be seen in Fig 2.10. This can be induced by sinusoidal excitation with 10-20Hz [38]. It is usually experienced when the ultrasonic bonding process is not optimized. This failure mechanism is also due to the thermo-mechanical stress. The wire is exposed to thermal stress as it expands and contracts undergoing fatigue. An SEM image of the wire-bond cracking is shown in Fig 2.11.

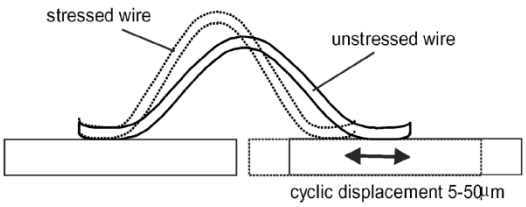

Fig 2.10: Wire-bond subjected to thermo-mechanical stress (reprinted from [38])

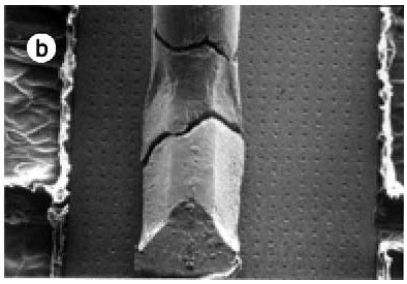

Fig 2.11: SEM image of wire-bond cracking (reprinted from [8])

It is important to note that both wire-bond lift-off and wire-bond cracking can occur simultaneously. [38] suggest that the loop height to width ratio has a certain degree of proportionality to the number of cycles to failure as presented in Fig 2.12.

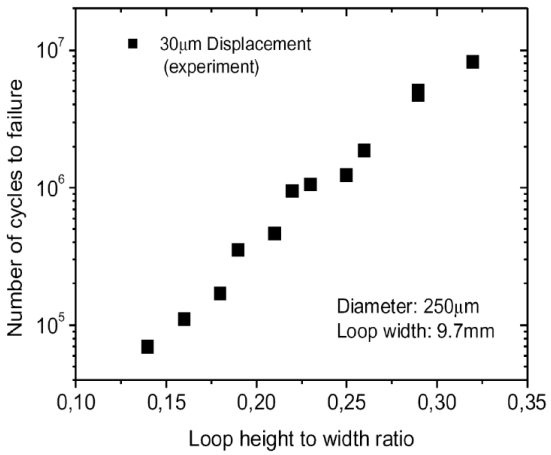

Fig 2.12: Relationship between loop height to width ratio and number of cycles to failure (reprinted from [38])

2.4.2 Solder Fatigue and Solder Voids

As a result of improvements made in reliability, it was found that for the module used in [10], solder fatigue of the substrate-to-base interface is one of the limiting reliability factor for power cycling stress, if the duration of a cycle is chosen to be sufficiently large. It has been presented in [8] that in the substrate-baseplate location the worst mismatch in the CTEs, the maximum temperature swing combined with the largest lateral dimensions are present. Also this failure mechanism occurs in the solder layer between the device and the substrate. There are also process induced voids, which can interact with thermal flow and the crack initiation within the solder layer.

2.4.2.1 Solder Voids

Solder voids increase the junction temperature of the devices which becomes a trigger for other failure mechanisms such as solder fatigue and wire bond fatigue. The heat flow in a power module is considered to be one dimensional; the large solder voids in the heat path makes the heat spread. This incident further inhibits the heat extraction performance. On the contrary, small voids have less impact on the thermal performance of the power module. Fig 2.13 shows a scanning acoustic microscope image (SAM) of the voids in the solder layer between the substrate and the baseplate. Caution is taken in advanced processes for producing the power modules to prevent the formation of voids.

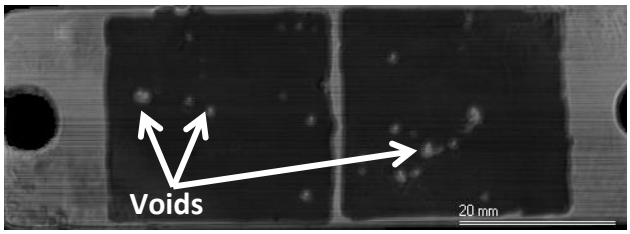

Fig 2.13: SAM image of solder between substrate and baseplate indicating solder voids

2.4.2.2 Solder Fatigue

This failure mechanism develops when the solder between the substrate and the baseplate or the solder between the device and the substrate cracks. This mechanism usually propagates from the edges of the solder where shear stress (defined as result of force vector component parallel to the cross section) reaches its maximum and moves towards the centre of the solder until the solder layer is compromised. An acoustic scan of solder fatigue can be observed in Fig 2. 14.

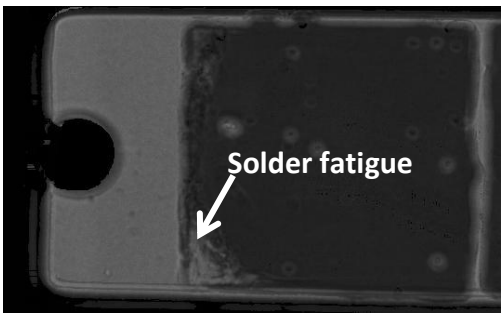

Fig 2.14: Acoustic scan showing solder fatigue

A comparison between two type of baseplates was made in [39]; copper and AlSiC baseplates using the same substrate material (AlN) were compared. The two modules were subjected to thermal cycling; the same temperature swing of 50°C was applied to both samples. From Fig 2.15 it can be observed that the solder on the copper baseplate (module 1) experiences solder fatigue as opposed to the AlSiC (module 2) baseplate. The image of the solder on the copper baseplate was taken after 16,000 cycles while the image of the solder on the AlSiC was taken after 90,000 cycles. This means that under the same

conditions the solder on the copper baseplate degrades much faster than that of the AlSiC baseplate.

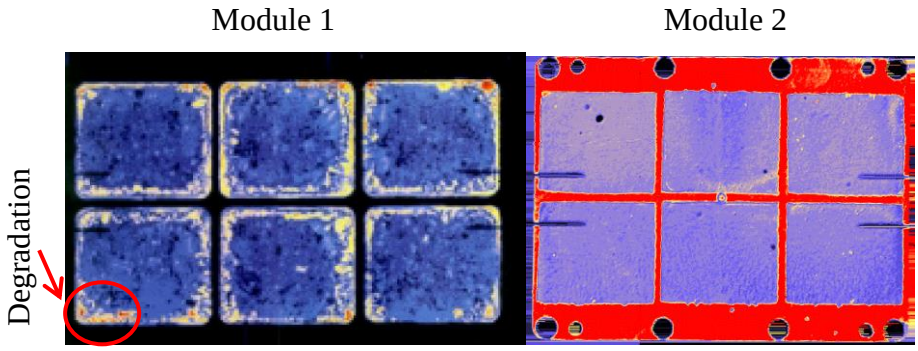

Fig 2.15: SAM images of cycled solder layer of modules using copper(left) and AlSiC(right) baseplates (reprinted from [39])

2.4.3 Aluminium Reconstruction

Aluminium reconstruction occurs due to the large thermo-mechanical mismatch between aluminium and silicon chip and due to the stiffness of the silicon substrate, the stresses, which arise within the aluminium thin film during pulsed operation of the device can be far beyond the elastic limit [40]. The elastic limit is defined as the limit to which a solid may be stretched without permanent alteration of form or size. Surface reconstruction sometimes occurs as a secondary mechanism in conjunction with wire bond lift off. In Fig 2.16 the image on the left side shows the metallization layer before cycling and the image on the right shows the metallization layer after 3.2 million cycles with a temperature swing of 40°C [8].

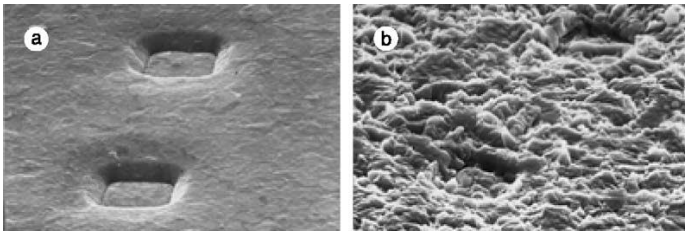

Fig 2.16: Metallization before power cycling (left) and after (right) (reprinted from [8])

2.4.4 Other Failure Mechanisms

Other failure mechanisms such as cracking, corrosion of the interconnection, latch up and cosmic rays can also affect the power modules. These failure mechanisms are not as common as the aforementioned. Failure mechanisms such as corrosion and cosmic rays depend on the application. For example, corrosion is a considerable failure mechanism in offshore wind turbines or marine applications due to humidity.

2.4.5 Effects of Failure Mechanisms

Failure mechanisms are important because they have an effect on the electrical and thermal properties of the module. Increase in electric resistance due to wire bond lift-off as mentioned earlier means that less wire bonds are allowed to carry the same amount of current. An increase in resistance means that there is an increase in Vce for IGBT and forward voltage for diodes. An increase in thermal resistance also occurs due to solder fatigue and solder voids due to a distorted thermal path or thermal conducting area. As these problems develop with time they eventually lead to the destruction of the device. Therefore an effective monitoring of the major failure mechanisms is required.

2. 5 Monitoring Degradation

Failures need to be detected in order to prevent abrupt destruction of the devices. Therefore to detect the impending failure, precursors of failure need to be defined. These precursors are temperature, collector emitter voltage (V_{ce}), threshold gate voltage ($V_{ge(th)}$), gate resistance (R_G), thermal resistance/impedance, turn off time and voltage across the parasitic inductance between the power emitter and gate emitter (di/dt). The collector emitter voltage, threshold voltage, gate resistance, V_{ge} turn off time and di/dt all have a defined dependence on temperature and are therefore called temperature sensitive electric parameters (TSEP). There are several TSEPs in addition to the ones mentioned above[41]. TSEPs can either be static (measured at steady state) or dynamic (measured at transients). The thermal resistance and impedance is obtained from the temperature.

The temperature then is an important parameter to monitor degradation; the power modules are enclosed and provide no opportunity for a direct measurement of the junction temperature. The state of the art methods to obtain the junction temperature include the integration of NTC resistors, on – chip diodes and the use of TSEP. The NTC resistors are placed on the substrate and reveal the baseplate temperature with a time constant of a few seconds [42]. The on-chip diodes are integrated within the IGBT and return the local temperature with a time constant of about 1ms [43]. Both types require special consideration during design and manufacturing process to ensure electrical isolation from HV traces on the substrate and require additional external pins and separate copper traces, which might increase manufacturing cost and give rise to additional reliability issues [16]. In the absence of direct measurement, the TSEP is a feasible way of measuring the junction temperature.

2.5.1 IGBT Structure and Operation

In order to gain an understanding of the TSEPs used, the structure and the operation of the IGBT is presented. The IGBT structure is formed by using four (N–P–N–P) alternating semiconductor layers. The basic structure of an N-channel nonpunch-through (NPT) IGBT is presented in Fig 2.17. The nonpunch-through IGBT differs from the punch-through IGBT due to the inclusion of N-buffer layer in N-drift region in the case of PT IGBT. The punch through structure is optimized for DC circuit applications where no reverse bias is applied to the device because it operates exclusively in the first quadrant of the *i*–*v* characteristics [44].

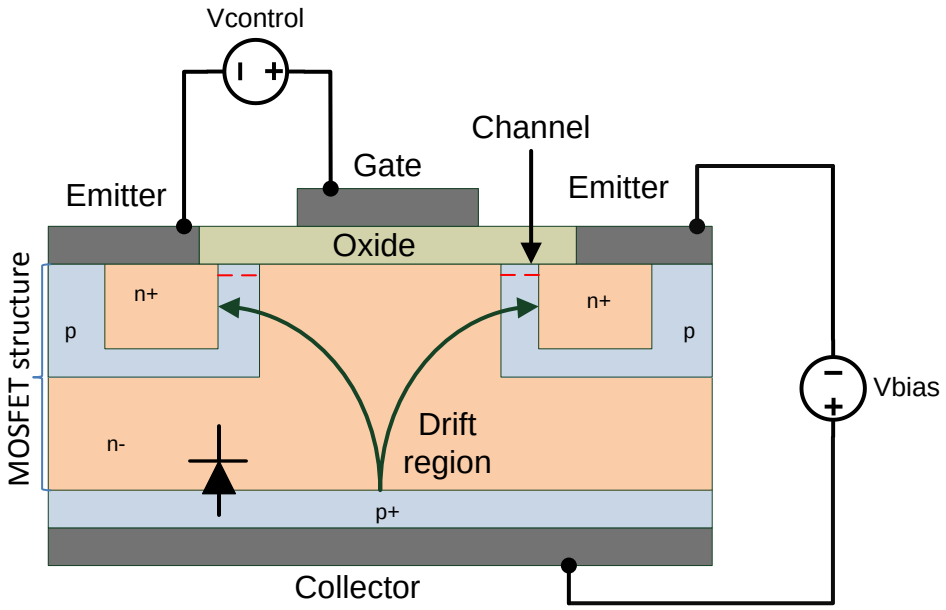

Fig 2.17: N-channel IGBT (NPT) cross-section

When a positive gate bias (V control) is applied, an inversion channel layer below the gate which connects the emitter to the drift region. When the collector is biased by positive Vbias, electrons flow from the emitter (n+) through the channel creating a connection between emitter and collector.

2.5.2 Threshold Gate Voltage as TSEP

The threshold voltage for silicon IGBT has a linear relationship with temperature which can be represented by (2.13).

$$V_{th1} = V_{th0} - k\ \left(T_{j1} - T_{j0}\right) \tag{2.13}$$

Where V_{th0} is the threshold voltage at room temperature (T_{j0}) and V_{th1} the threshold voltage at temperature (T_{j1}) in the range of operation. *k* is the constant of proportionality which is related to the device properties [45]. The threshold voltage is the gate voltage at which the inversion layer forms to produce a conduction path just below the gate oxide. This inversion channel is indicated by the red dotted lines in Fig 2.18. Measuring the threshold voltage is a very sensitive process because it involves switching of the gate control circuit. A basic circuit for the measurement of the threshold voltage can be seen in Fig 2.19. Due to the layout of the conventional power module, there are resistances and inductances related to the wire-bonds and terminals. This

means that if measurement is carried out at the terminals the voltage drop includes the voltage across wire bonds and module terminals. The temperature dependence of the bond wires at low current can be considered negligible [46].

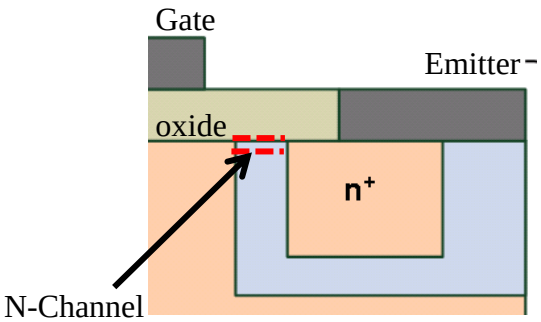

Fig 2.18: Inversion channel IGBT

Threshold voltage is measured after heating current I_h passes through the device; the measurement is carried out when the measurement current I_m flows through the DUT by measuring the gate voltage. This measurement system needs to be fast, which is one of the limitations in real operating conditions.

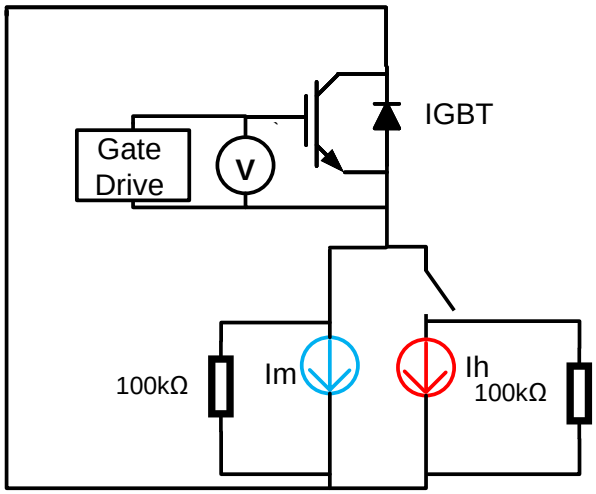

Fig 2.19: Basic schematic for threshold voltage measurement

An advantage of using the threshold voltage is the fact that it has a good sensitivity of about 10mV/K and represents the hottest semiconductor path which is the channel region [45]. The disadvantage of using the threshold voltage is that the values of the same batch can differ by about 0.2 V due to its dependence on gate properties and concentration of carriers. This system also

needs a really complicated gate driver system. There were attempts to realize threshold voltage measurements with DUT heating pulses similar to those obtained under real operating conditions but the experiment required too many modifications to be implemented in the normal converter circuit. There are no known realized methods using standard threshold voltage measurement under real operating conditions of standard power electronic circuit [45]. A quasi-threshold voltage measurement is proposed in [45] by measuring the small voltage across the parasitic inductance between the power emitter and the gate emitter; this gives rise to a really complicated gate drive.

2.5.3 Gate Resistance as TSEP

The internal gate resistance is the equivalent electrical resistance due to the elements of the device structure such as the P-body, gate oxide, and gate contacts design. The internal gate resistance can be used as a TSEP, as it has well-known temperature dependence and is located in the centre of the die. The measurement of this internal gate resistance in the presence of high voltage currents presents a challenge. Additional connectors (V2 & A2) need to integrate into the chip in order to realise measurements. A sophisticated circuitry to obtain the internal gate resistance is presented in [47]. The principle of using the internal gate resistance as TSEP is presented in Fig 2.20. A constant current similar to that of the threshold voltage measurement is applied through the internal gate resistance (Rgint) which creates a voltage drop (Vgint) dependent on the temperature. This voltage is measured by making connections across the resistor and using an accurate voltage measurement system.

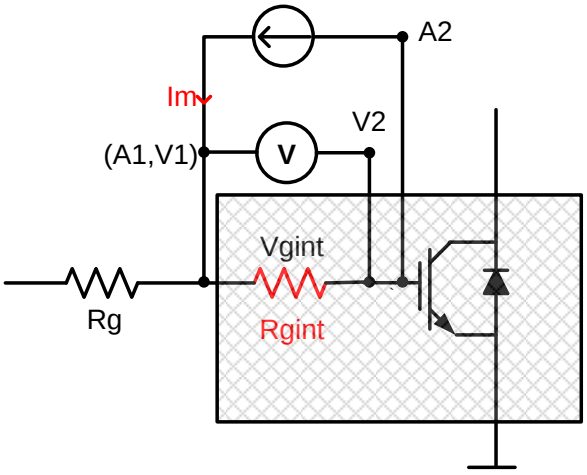

Fig 2.20: Principle of using Rgint as a TSEP (reprinted from [47])

The resistance dependence with temperature is stated in [47] to be about 1.5mΩ/K. When the low constant current is applied to this it is observed that the voltage dependence with temperature will be significantly low. Therefore a Kelvin measurement is carried out as seen in Fig 2.20. This necessitates a change in the substrate design to account for the Kelvin connection without affecting the thermal performance.

2.5.4 V_{ge} Turn-Off Time as TSEP

This is a method that measures temperature by measuring the gate voltage and keeping track of the turn off time. [48] presents a figure of the off times at different temperatures which is shown in Fig 2.21. It can be observed that there is proportionality between time vs the temperature. The time shift is detected by using two triggers; one at the first falling edge and the other at the second falling edge. This region is known as the Miller plateau. The dependence in temperature according to [48] is due to the depth of the plasma (mixture of mobile electrons and holes) up to the n^- drift layer. The amount of plasma present in the IGBT increases with higher temperatures and hence, more charge has to be removed during the turn-off process before blocking voltage can be supported again.

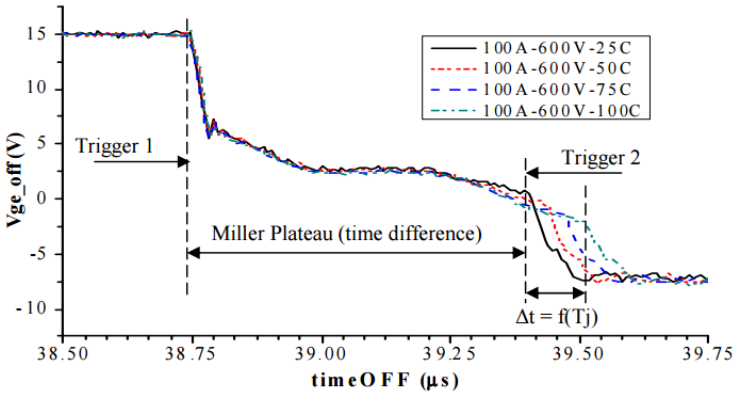

Fig 2.21: Vge voltage at different temperatures (reprinted from [48])

The Miller Plateau is not only dependent on the temperature but also on the collector current, as well as the DC-link voltage. The sensitivity of the Vge curve with respect to collector current is between 0.12ns/A and 0.18ns/A for a certain DC-link voltage and temperature. Also it was found out that the sensitivity of Vge with respect to the DC link voltage is between 0.17ns/V to 0.11 ns/V for currents between 100A to 400A respectively. The sensitivity of Vge with respect to temperature range is approximately from 0.8ns/°C to 3.4ns/°C for currents ranging from 100A to 1500A and voltages ranging from 30V-1800V [48]. These dependencies on a wide range of current and voltage can significantly invalidate the temperature measurement.

2.5.5 Recovery Rate (di/dt) as TSEP

The di/dt is a TSEP used to measure the temperature in anti-parallel diodes by establishing a relationship between the recovery rate di/dt and the temperature. This is carried out in [49] on the widely employed half-bride topology as shown in Fig 2.22. The methodology is defined by measuring the voltage across the parasitic inductance between the Kelvin and power emitter.

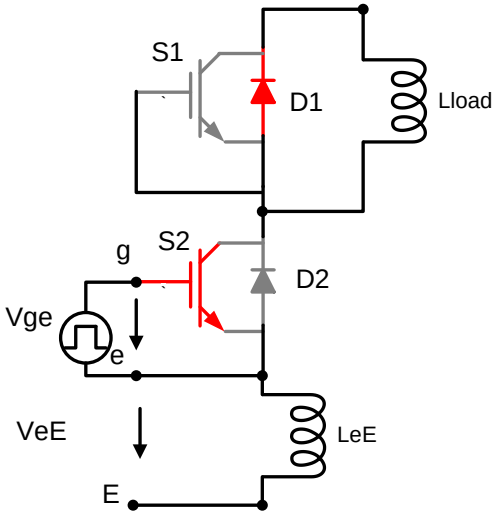

Fig 2.22: di/dt measurement circuit

This method uses the conventional double pulse test sequence whereby S2 is switched on till the current in the inductor reaches the desired value. The current free wheels when S2 is switched off. S2 is turned on again for a shorter period in which the device parameters are measured [50]. At the instance at which S2 is turned on the second time, the reverse recovery current of diode D1, which is dependent on chip temperature, induces a voltage VeE across the parasitic inductor *L*eE during the S2 turn-on transition.

2.5.6 Collector–Emitter Voltage as TSEP

Research has shown that Vce is the dominant monitoring parameter to detect the degradation of the IGBT module [51-54]. An N-channel IGBT can be considered as an N-Channel MOSFET on a p type substrate; this can be deduced from Fig 2.17. The p-n junction at the collector forms a diode; hence, the equivalent circuit of an IGBT can be represented by Fig 2.23

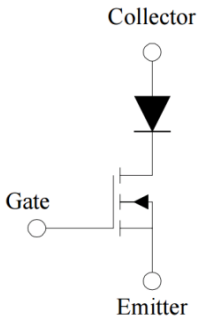

Fig 2.23 IGBT Equivalent Circuit [55]

The p-n junction provides the advantage of the temperature dependence on its diffusion voltage [53]. This dependence is created by constant low current used to calibrate the device at different temperatures. A low current is used to prevent self-heating of the IGBT and also to make use of the p-n junction diffusion voltage. The low current also has the advantage of rendering the parasitic effects (voltage drop across bond wires and terminals) related to the conventional power module shown in Fig 2.24 insignificant. At low currents (100mA range) the voltage drop measured is mainly due to the p-n junction as stated earlier. The voltage drop across the bond wires (R_c & R_e) is relatively insignificant compared to the voltage across the p-n junction. At high current however, V_{ce} is erroneous due to the inherent series resistance contribution of the bond wires and packaging [46, 56, 57].

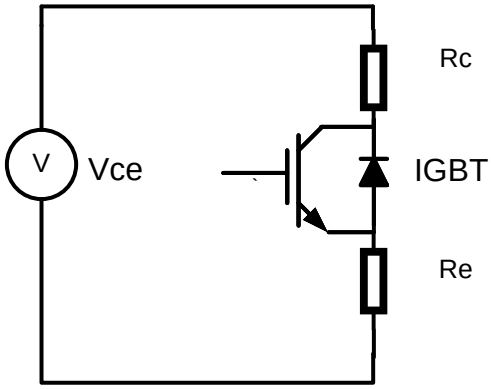

Fig 2.24: Vce measurement showing parasitics

The method proposed in [56, 57] takes two V_{ce} measurements in quick succession at two different levels of V_{ge} (15V and 13V). The measurements should also be performed at the same current level. If the two measurements are taken within a small time span (under 200μs) the junction temperature and the temperature of the interconnections can be said to be constant for the two different gate voltage levels. In this case the voltage across the chip changes while the voltage across the interconnections (R_c & R_e) remains constant. Therefore the contribution of the inherent resistances can be compensated for and the V_{ce} can be accurately measured.

Although the I-V characteristic of a modern IGBT chip exhibits a positive temperature coefficient at nominal current levels, i.e. Vce increases with increasing temperature for a constant injected current; the temperature

coefficient is generally negative for low currents. In this current regime Vce decreases almost linearly with growing temperature at a rate ε of approximately -2mV/K [53]. Therefore a linear relationship can be created by the equation

$$T_o = T_1 - \frac{V_0 - V_1}{\varepsilon} \quad (2.14)$$

V_{ce} is relatively small compared to the blocking voltage of the device. Adding to this, it's the change in V_{ce} that is required. This means a very accurate voltage measurement is required which has the ability to distinguish between noise and the change in V_{ce}[35].

2.5.6 Choice of TSEP

In [5] an increase in 5% of V_{ce} is a sign of approaching failure of the pack and also an increase in thermal resistance by 20% indicates failure. But [58, 59] suggest that the change is dependent on the power rating of the device. Therefore the equation presented in [58, 59] shows how failure can be estimated differently

$$V_{ce}[\%] = \frac{1500}{I_{rated}} \quad (2.15)$$

The standards have been set by the International Electro-technical Commission (IEC) in the Updated version IEC 60747-9:2007 that requires all parameters to remain within the specification limits for endurance tests:

Table 2.3: IEC standards limits

TESP	Limits
Rds(on) / Vce	+ 20 % of the initial value
Vgs(th) / Vge (th)	+ 20 % of the upper specification limit - 20 % of the lower specification limit
Rth	+ 20 % of the initial value

The above limits can be used to indicate when a device is at the end of life. The choice of the TSEP depends on the application and the several criteria presented [60]:

• Temperature sensitivity; various TSEPs have different values of temperature sensitivity, a greater TSEP temperature sensitivity gives better measurement results

• Measurement error; the influence of non-thermal effects during measurement is different for each TSEP

• Linearity; the linear relation between TSEP and temperature is a desired property, which is not always fulfilled

• Repeatability; there should be no large scattering of TSEP values between different samples.

The choice of TSEP in this work is based on the fact that the aim is to measure the dynamic temperature of the device. Therefore a continuous measurement of the temperature is needed. This eliminates the use of the threshold voltage, turn-off time, recovery rate as regular switching is needed in order to obtain the temperature. The Vce as presented in [46], exhibits the characteristics mentioned above such as a high repeatability and linearity. The sensitivity of this mechanism depends on the current levels as can be noticed from the relationship between current, voltage and temperature in the I-V curves. In this work, since the measurement is to be carried out at low currents, the sensitivity is relatively high (2mV/°C).

2.6 Conclusion

This chapter has presented the structure and the different materials used in the conventional power module. It has presented the benefits of these materials in the power module and how their behaviour in an environment with a varying temperature contributes to the manifestation of failure mechanisms. The main failure mechanisms that affect the conventional power module which are relevant to this work have been outlined and discussed. Moreover, the different

variables used to measure temperature have been presented; the choice of parameters for this work and the reason behind that are also stated. Finally an analysis of heat conduction in a simple case representing the power module has been discussed. It is evident that it provides the opportunity of presenting a simplified method of analysing the heat flow path and how the heat flow path is relevant to this work which will be found in the next chapter.

Chapter 3: Representation of Module Structural Features: Thermal Impedance & Structure Functions

3.1 Introduction

This chapter presents the derivation of thermal networks starting from a physical model and the transient cooling curve of power semiconductor devices. Two types of thermal networks are typically used, Foster network and Cauer Network. There are 3 methods used in this work to extract the thermal networks using the heating and cooling curves. These methods which are discussed in this chapter are the graphical method, curve fitting and deconvolution. After obtaining the Foster network from the methods mentioned above, the Cauer network is derived from the Foster network.

Measuring thermal transients is a typical method for thermal characterisation of semi-conductor device packages. The method itself relies essentially on the recording of the thermal response function of the structure for a step function excitation [25]. This means that the cooling and heating curves contain information about the power semi-conductor device packaging structure. The structure function is a graphical representation of the device structure that makes uses of the thermal models (Foster and Cauer). The schematic shown in Fig 3.1 shows the process involved in obtaining the structure function. The thermal transient measurement is affected by noise; therefore the measurement will be noisy. Proper filtering needs to be applied in other to make use of the thermal transient curve for further processing. After filtering the thermal transient curve, the next step is calculating the thermal impedance curve from the thermal transient; time constants can be derived from time constant estimation methods [25, 27].

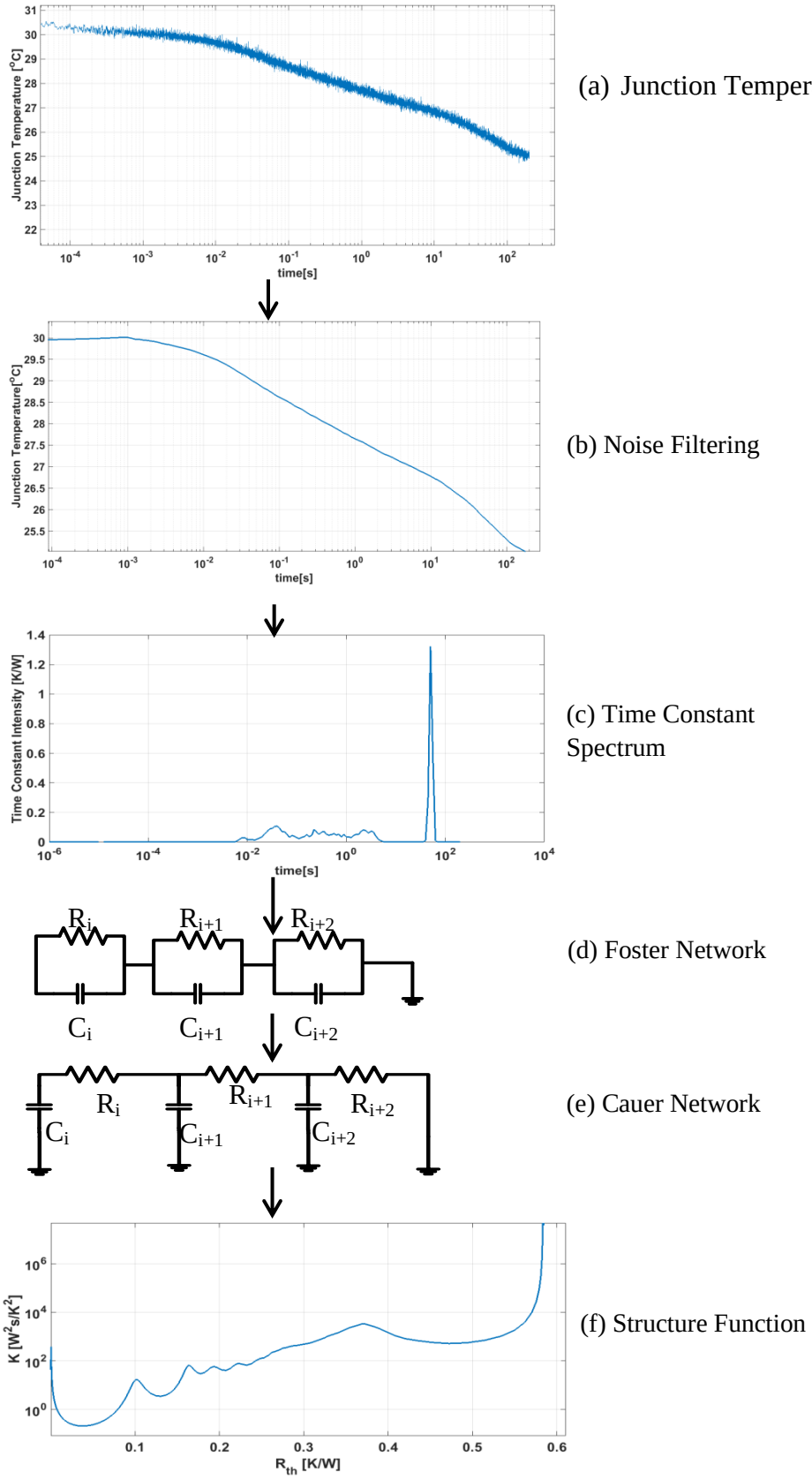

Fig 3.1: Schematic process of obtaining the structure function. Junction temperature (a) is measured using V_{ce} as TSEP. The measurement is noisy, (b) shows the filtered version (a). The time constant spectrum (c) derived from

tunction temperature using deconvolution (b). The Foster network (d) is directly obtained from (c).The Foster network is converted to Cauer network (e) and then the Cauer netwok (e) is used to derive the structure function (similar to the process flow in [61])

From the time constants spectrum the thermal resistances and capacitances that make up the Foster network can be obtained. The Foster network of power semi-conductor modules allow for both the dynamic and static characterisation of the modules. Although the Foster network allows for the dynamic and static characterisation, it has no physical relation to the structure of the power semi-conductor device packages. Therefore a so called Cauer network needs to be derived from the Foster network in order to have a physical relation between the thermal network and the device structure. The structure function is derived from the thermal resistances and capacitances of the Cauer network.

3.2 Thermal Networks

A solid system can usually be described from the thermal point of view by means of a discrete element electrical circuit, composed by resistances and capacitances, in which the temperatures and the thermal powers are retained as voltages and currents, respectively [62]. Two types of networks (resistances and capacitances) are commonly used for equivalent modelling of thermal problems. One is called Foster and the other Cauer Network [63]. In Fig 3.2 and 3.3 the heat source represents the silicon die and the symbol of electrical ground represents the ambient.

The cooling curve can be approximated by a sum of decaying exponentials (n). In the Foster network the time constants of these exponentials are calculated by the products of the individual resistance (R_{th}) and capacitances (C_{th}). In the Cauer network the product doesn't equal the time constant because it depends on all the thermal resistances and thermal capacitances.

The Foster network is shown in Fig 3.2. The Foster network is the most frequently used thermal equivalent circuit. It is mathematically very simple to use but as a purely formal description has no relation to the real physical structure. The foster network cannot be related to a physical structure because of the existence of the node to node capacitors. Real thermal capacitors are

always connected to ground, since the stored energy is proportional to the temperature of one node and not the temperature difference between two nodes.

To elaborate on this, in electrical circuits when a capacitor is in the dynamic regime, the current on both sides are the same. This is due to the symmetrical variation of both positive and negative charges. In thermal circuits, there are no properties corresponding to negative electric charges. This means that only current flow (heat flow) on one side of the capacitor has an actual meaning. That side of the capacitor must be used to determine the variation of the voltage (temperature).

The consequence of this is that the electro-thermal analogy is valid only if all the capacitors are connected to ground. Hence the use of the Foster network does not thermally represent the internal points of the system. On the other hand the Cauer network is representative of the structure of the device. The Cauer network is shown in Fig 3.3. The reasoning behind an equivalent model makes the idea of associating circuit components and physical regions possible.

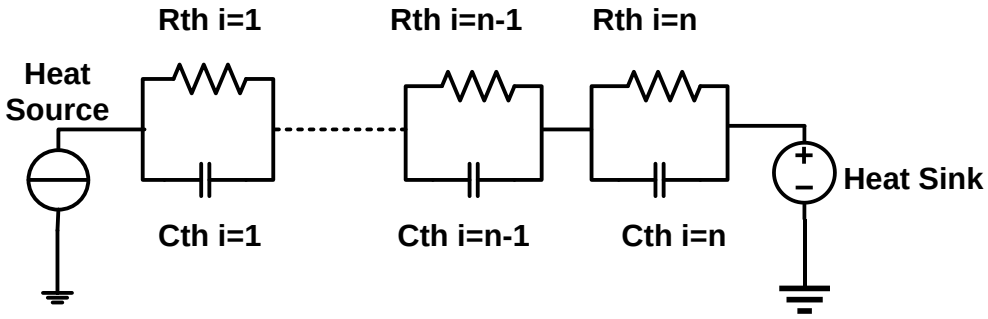

Fig 3.2: Foster network

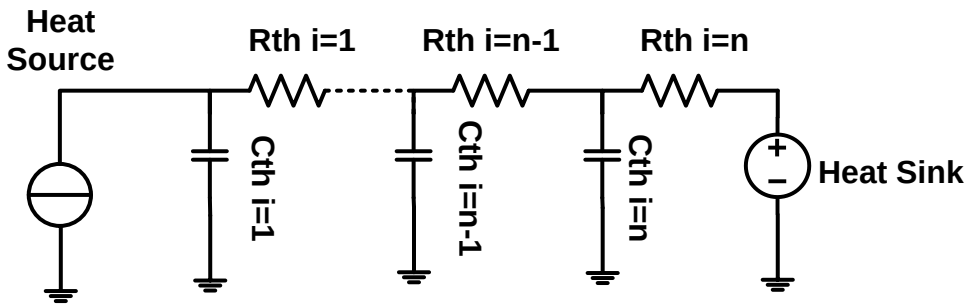

Fig 3.3: Cauer network

Both circuits represent a solid which behaves thermally one directional: this means that when there is only one heat source and one heat sink, the thermal energy from the heat source flows to the heat sink through a single path both in static and dynamic regimes. As far as electronic systems are concerned, this property is practically satisfied when the thermal losses toward the environment by radiation or convection through the lateral walls or the top surface of the packaging are negligible in comparison with the 1-D heat flow due to the conduction mechanism [62].Consequently a very good one-dimensional effect is achieved when cooling boundary conditions are very good. For this to be satisfied convection at the heatsink ought to be high. The methods used to extract the Foster and the Cauer Network from the physical model and thermal transients are presented in the next paragraphs.

3.2.1 Derivation of Thermal Network from Physical Model (Cauer)

As mentioned earlier the thermal network is a representation of the solid structure. The thermal capacitances and the resistances can be derived from the solid structure provided the solid exhibits one-dimensional heat flow. This can be done by examining the materials present in the physical structure. By considering Fig 3.4, it can be appreciated that there'll be to some degree lateral spread of heat. For heat propagation in homogeneous media it is helpful to assume a spreading angle of about 45° [64]. By dividing the structure into a given number of elements, it is valid to apply the one-dimensional approach within each segment.

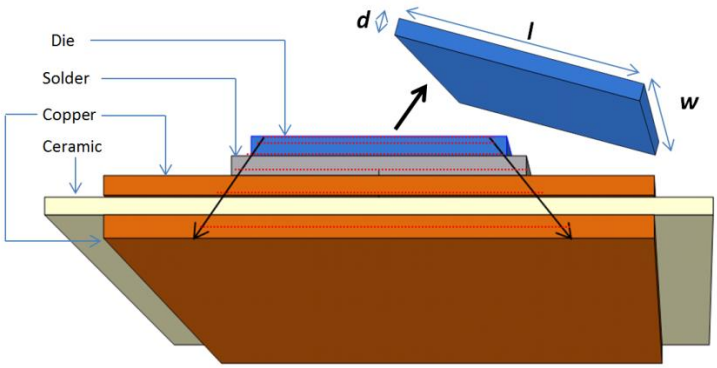

Fig 3.4: Physical structure indicating heat flow

The segments can be associated to equation (3.1) and (3.2) where λ is thermal conductivity; c is specific heat and ρ is density. The equations using dimensions of the segments are used to derive the thermal resistances and capacitances that form a Cauer network (each segment contains a resistance and a capacitance). The segments are shown by the red dotted lines in Fig 3.4 which produces a cuboid for each segment. Equation (3.1) shows the thermal resistance *Rth* is proportional to the thickness *d* and inversely proportional to thermal conductivity λ , length *l* and width *w***.** The thermal capacitance as derived in equation (3.2) is proportional to the volume *(d.l.w)*, the density ρ and the specific heat capacity *c*.

$$R_{th} = \frac{d}{\lambda * l * w} \tag{3.1}$$

$$C_{th} = c * \rho * d * l * w \tag{3.2}$$

The segments thickness should be chosen so that progressively larger thermal time constants (τ) are produced in the direction of heat propagation. Experience has shown that the time constants should differ respectively by a factor of 2 to 8 for the best results [64]. These segments as shown in Fig 3.4 are used to calculate the different thermal resistances and capacitances. The segmentation with a factor of 2 to 8 ensures more detail in the area with fast response (smaller time constants) i.e. the chip and the substrate.

3.2.2 Derivation of Thermal Networks from Thermal Transient

The thermal impedance and resistance is defined as the ratio between temperature rise and the power dissipation that causes temperature change. The most important difference between thermal resistance and impedance is that thermal impedance is the dynamic behaviour and thermal resistance is the steady behaviour. Thermal modelling of electronic packaging can be classified into two groups: the static behaviour and dynamic thermal behaviour. The static thermal behaviour is when the temperature of the device is in a steady state. This behaviour is usually represented by thermal resistances as the temperature doesn't change with time. The junction to case or junction to

ambient values of thermal resistance mostly found in the data sheets are just single resistances without more information about the heat flow details. The information of the dynamic thermal behaviour does not exist. The dynamic thermal behaviour contrary to the static occurs when temperature changes with time. The dynamic behaviour is shown in Fig 3.5 which shows the junction temperature of an IGBT heated by current conduction. The dynamic behaviour occurs during the cooling and the heating.

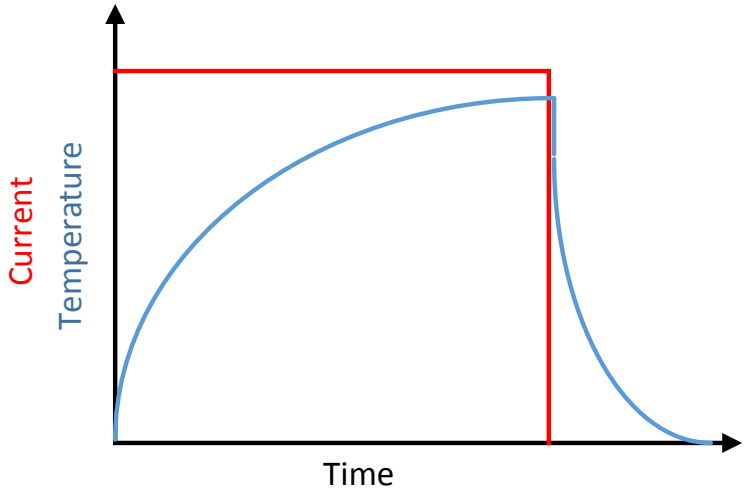

Fig 3.5: Junction temperature and heating current

There are two types of transient curves, the heating and the cooling curve. These curves are used to characterise the thermal behaviour of power semiconductor devices. According to [65] both the cooling and the heating curves are the same if the description of the transient thermal behaviour is considered. They contain in principle the same information. The measured thermal transient curves are usually monotonously increasing or decreasing functions with many intervals of different slopes. This results from the fact that heat conduction and convection mechanisms are mostly linear effects, i.e. when increasing power the temperature grows proportionally. There are some exceptions, e.g. silicon has a nonlinear heat conductance at higher temperatures and radiation effects are at higher magnitudes. Still these effects are not very pronounced in the temperature range used when characterizing packages and they can be linearized without a significant loss of accuracy[66]. The disadvantage using the heating curve for thermal impedance measurements is the heating current must be periodically interrupted for the junction

temperature measurement. The heating current introduces a delay time, as the charge has to be removed from the junction area before the temperature can be measured [67]. The time delay increases with the increase in current. If the time is in the range of millisecond, the die region will begin to cool down because the thermal time constant of the die is in the range of milliseconds too [62, 68]. The cooling curve is used in this work due to the independence of the devices to the heating current during the cooling period. The cooling curve can be described in the simplest form by the response function of a single time constant system. It has the mathematical form of [25]:

$$a(t) = a * e^{-(t/\tau)} \tag{3.3}$$

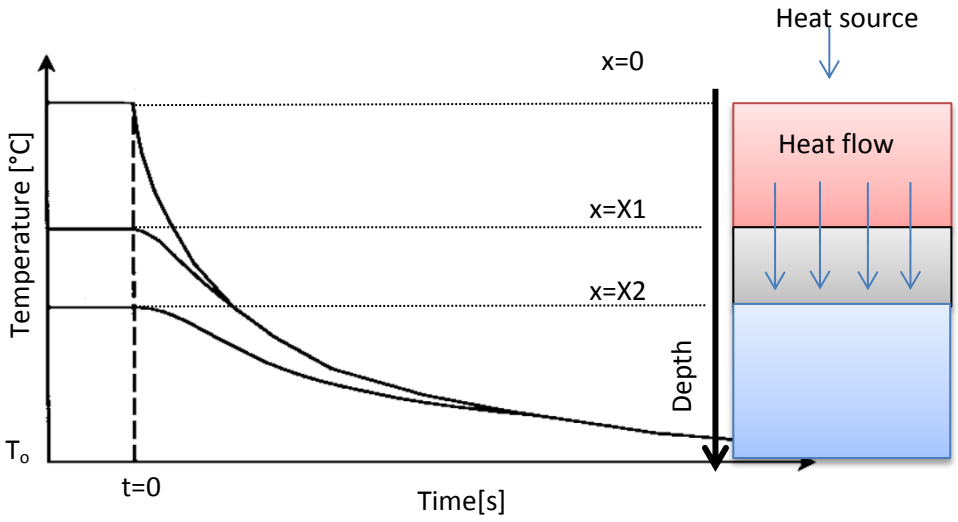

Fig 3.6: Temperatures at different points in a solid structure in relation to depth

Fig 3.6 shows a solid figure made up of different materials with one dimensional heat flow. The heat source is located at a distance x=0. It also shows the curves when a power pulse has been applied and the temperature was measured at various points (0, X1 and X2) in the structure of the device.

According to [62] all the curves have the same analytical expression with the same set of time constants but with different set of values for the amplitude factor a_i. In this case the series of coefficients a_i (x=0), which is the whole temperature variation of the transient converges to finite value which can be related to the total thermal resistance Rth of the system**.** Therefore the following two relationships hold:

$$R_{th} = \frac{T(x=0,t=0) - T_0}{P_0} \tag{3.4}$$

$$|R_{th} = \sum_{i=1}^{\infty} R_i(0) \tag{3.5}$$

Where T(0,0) is the steady state temperature of the heat source at the instant the power (P_0) is turned off and R_i is a_i divided power by power. If a single exponential represents a simple function response as in equation (3.3), for a more complex thermal structure it can be considered as an infinite sum of the individual exponential terms with different time constants and magnitudes.

Despite the fact that the function T(0,t) is the sum of an infinite number of exponential functions, it can be described in approximated way only by taking into account the first 'n' terms of the series, so that the following relationship stays valid:

$$T(0,t) \approx T_0 + P_0 \sum_{i=1}^{n} R_i(0) * e^{-(t/\tau)} \tag{3.6}$$

The dynamic version of equation (3.4) is thermal impedance:

$$Z_{th} = \frac{T(x=0,t) - T_0}{P_0} \tag{3.7}$$

Therefore equation (3.6) can be written as:

$$Z_{th} \approx \sum_{i=1}^{n} R_i(0) * e^{-(t/\tau)} \tag{3.8}$$

From this equation if the thermal impedance curve is obtained (which can be derived from the thermal transient curve) then the thermal resistances and capacitances can be obtained from the time constants (τ=R*C). There are several methods of achieving this, the graphical method curve fitting and deconvolution will be discussed in this work.

3.2.2.1 Graphical method

The thermal capacitance and resistance can be derived by the thermal impedance curve from equation (3.8) [27, 69]. By plotting the thermal impedance curve on a semi logarithmic scale, the sum of exponentials in equation turns into a sum of linear terms[70]. By asymptotically extending the

line representing the cooling curve, the value of R_i can be directly read from the y-axis (which represents the thermal resistance) by the intersection of the extended line and the y-axis. The point where the line departs from the cooling curve on the x-axis is the time constant of the corresponding thermal resistance and the unknown thermal capacitance. The thermal capacitance can be calculated now knowing that $\tau = RC$. This process is shown graphically in Fig 3.7 and 3.8

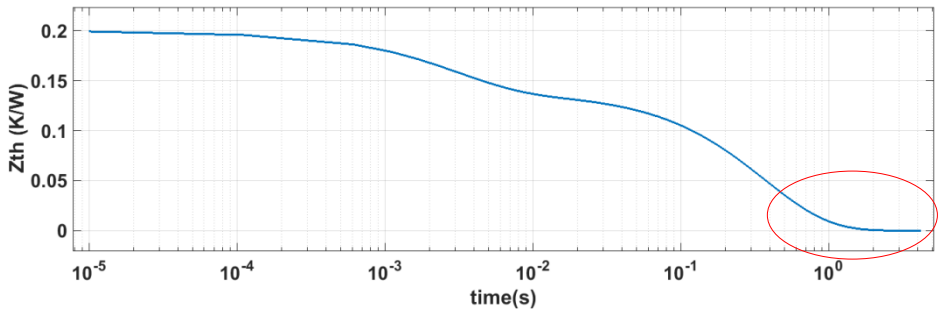

Fig 3.7: Thermal impedance curve on a semi-logarithmic scale

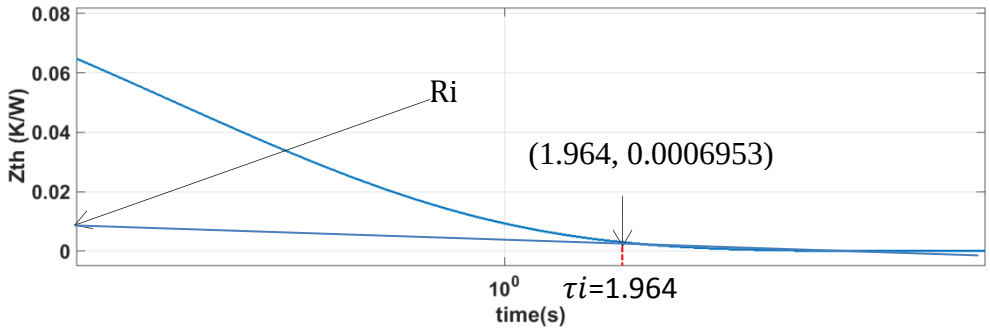

Fig 3.8: Illustration of data extraction in the graphical method

The thermal resistance and capacitance is derived for one component of the Foster network. The thermal resistance and capacitance are shown in equation (3.10) and (3.12). Those terms (R and τ) can then be put back in equation (3.8) as a single exponential and subtracted from the total as shown in equation (3.14). The process is repeated again until nothing is left of the curve. The first extractions have bigger time constants and those extracted last have smaller time constants.

$$R_i = 0.0006953 * e \qquad \text{[K/W]} \qquad (3.9)$$

$$R_i = 0.00189 \quad [\text{K/W}] \tag{3.10}$$

$$C_i = \frac{\tau_i}{R_i} \tag{3.11}$$

$$C_i = 982 \quad [\text{J/K}] \tag{3.12}$$

$$Z_{th1} \approx 0.00189 * e\left(-\frac{t}{1.964}\right) \quad [\text{K/W}] \tag{3.13}$$

$$Z_{thdif} = Z_{th} - Z_{th1} = \left(\sum_{i=1}^{n} R_i(0) * e\left(-\frac{t}{\tau}\right)\right) - \left(0.00189 * e\left(-\frac{t}{1.964}\right)\right) \tag{3.14}$$

3.2.2.2 Curve Fitting Method

Curve fitting method can be used to derive the Foster network. The derivation of the Foster was carried out using the curve fitting app in MATLAB. The first step is to use the thermal transient from a cooling curve or to flip the thermal transient from a cooling curve to a heating curve. This is done by first obtaining the difference between the maximum value of the cooling curve with the rest of the curve. This gives us a cooling curve in the negative domain; by multiplying the curve with negative unity we get the equivalent heating curve. Shown below in figure 3.9 is the thermal impedance curve represented in both the heating and the cooling curve.

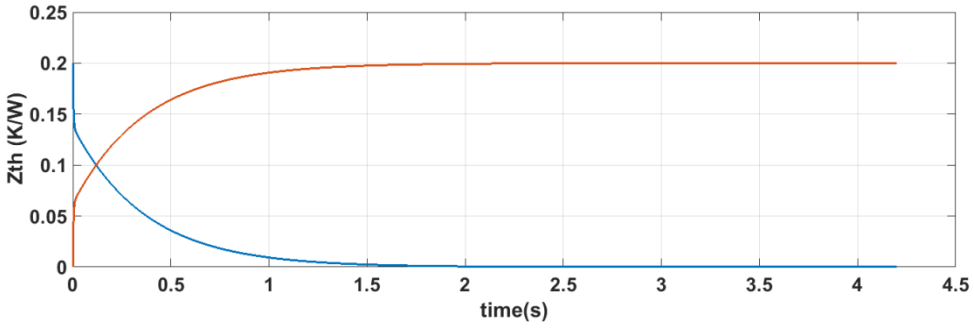

Fig 3.9: Thermal impedance represented in the cooling and heating form.

It is known that both these curves can be used to derive the thermal capacitances and resistances by assuming the cooling and the heating curve are a sum of exponentials.

Cooling:

$$Z(t) = R_1 * e\left(-\frac{t}{\tau 1}\right) ..... + R_{n-1} * e\left(-\frac{t}{\tau_{n-1}}\right) + R_n * e\left(-\frac{t}{\tau_n}\right) \quad (3.15)$$

Heating:

$$Z(t) = R_1\left(1 - e\left(-\frac{t}{\tau 1}\right)\right) ..... + R_{n-1}\left(1 - e\left(-\frac{t}{\tau_{n-1}}\right)\right) + R_n\left(1 - e\left(-\frac{t}{\tau_n}\right)\right) \quad (3.16)$$

Where n is the total number of thermal resistor or capacitors in the network. Before using the fitting app in MATLAB there is some information available. The equation which gives an idea of what the curve is supposed to look like and the thermal impedance curve.

Least squares fitting is used to extract the unknowns τ and R from equation 3.15 or 3.16. This is a mathematical procedure for finding the best-fitting curve to a given set of points by minimizing the sum of the squares of the offsets ("the residuals") of the points from the curve[71]. The thermal impedance curve is nonlinear, therefore nonlinear least squares fitting is applied to it. For nonlinear least squares fitting to a number of unknown parameters, linear least squares fitting may be applied iteratively to a linearized form of the function until convergence is achieved [72]. Fig 3.10 shows the original curve (black) and the fitted curve (green).The app gives the values of R and τ related to the green curve depending on the number of time constants put in equation 3.15 and 3.16.

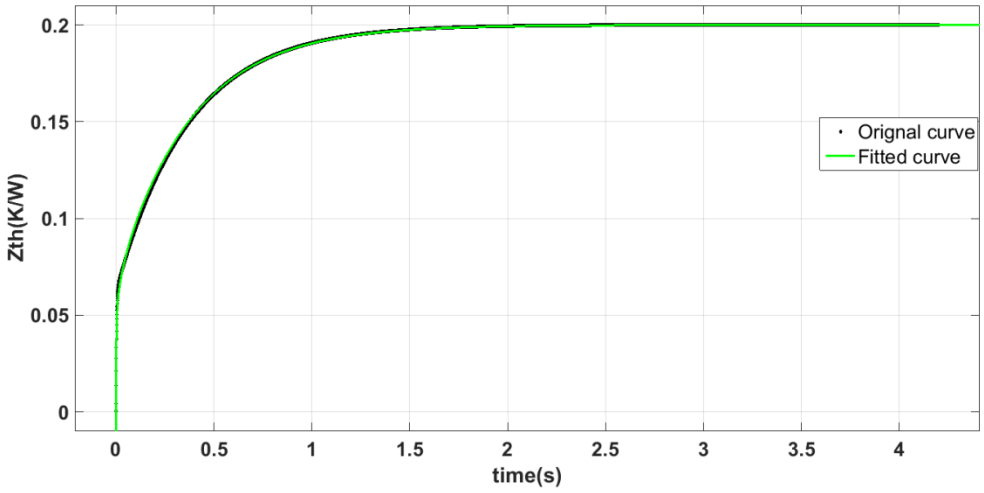

Fig 3.10: Thermal impedance with fitted heating curve

3.2.2.3 Deconvolution

The deconvolution method has been used in [25] to extract the time constants spectrum (Foster network) from the thermal transient curve. The cooling curve after a heat pulse is applied is essentially a step-function response. The cooling curve as well as the heating curve is a summation of exponentials. The heating curve was used in [25] to derive the time constants using deconvolution. The simplest form of the heating curve is a single time constant which can be represented as

$$a(t) = a * \left(1 - e\left(-\frac{t}{\tau}\right)\right) \tag{3.17}$$

For a more complex response, the equation will be a summation of different time constants of different magnitudes. For a Foster network with n time constants

$$a(t) = \sum_{i=1}^{n} a_i * \left(1 - e\left(-\frac{t}{\tau}\right)\right) \tag{3.18}$$

Due to varying range of time constants that are important (from range of 10^{-6} to several seconds) a logarithmic scale will help in simplifying the process.

$$z = \ln t \tag{3.19}$$

$$l = \ln \tau \tag{3.20}$$

Now the time response can be represented as

$$a(z) = \int_{-\infty}^{\infty} R(l)\left(1 - e\left(-e^{(z-l)}\right)\right) dl \tag{3.21}$$

Differentiating both sides with respect to z (see Appendix 2) a convolution type equation that is obtained which leads to finding the unknown function of the thermal resistance with respect to the time constant. Where R(l) are the magnitudes related to the time constant which needs to be divided by the power dissipation to get the resistance as the derivation is done using the thermal transient.

$$\frac{da(z)}{dz} = R(z) \otimes W(z) \tag{3.22}$$

Where

$$W(z) = e^{(z - e^{(z)})} \tag{3.23}$$

This process was applied for two cases. For a cooling curve derived from a simulation and a cooling curve derived from experiment. The simulation parameters were obtained by calculating the thermal capacitance and resistance from the physical structure of the device under test.

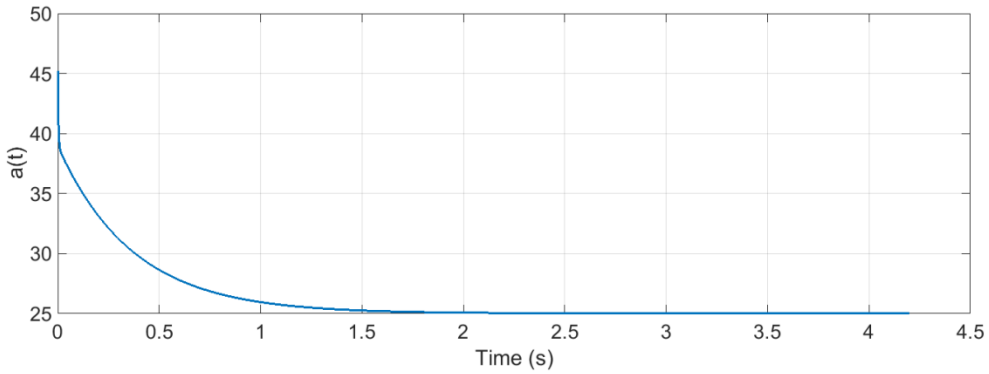

Fig 3.11: Simulated cooling thermal transient

The cooling curve above in Fig 3.11 was changed to a heating curve in order to conform with equation 3.18 so that the deconvolution process can be carried out. Because of the resolution needed to get the small time constants (10^{-4} s), if small points are taken there will be numerous points for the curve of several seconds. When these points are plotted on a log scale as shown in Fig 3.12 a few points appear in the early part of the curve with a dense number of points at the end. This information mostly represents the heat sink with a large time constant that doesn't require a resolution of the order (10^{-4} s). To solve this problem a log of the time points was taken to help redistribute the points on the curve. After the redistribution of points, numerical differentiation was carried out as in equation (3.22) to give Fig 3.13.

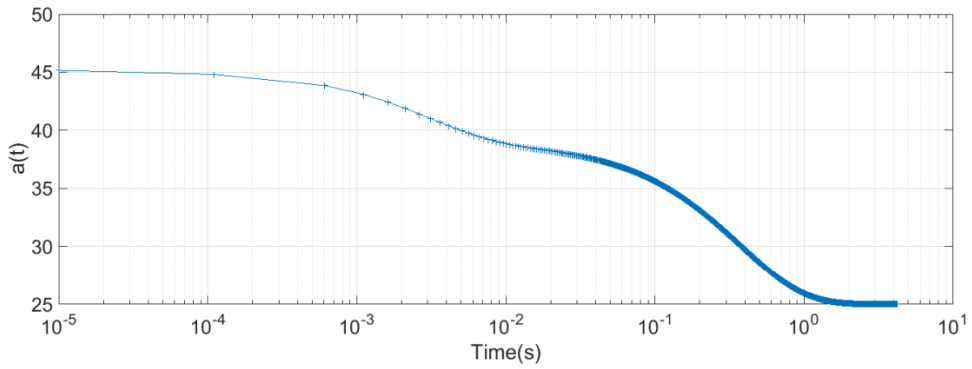

Fig 3. 12: Cooling thermal transient (log scale)

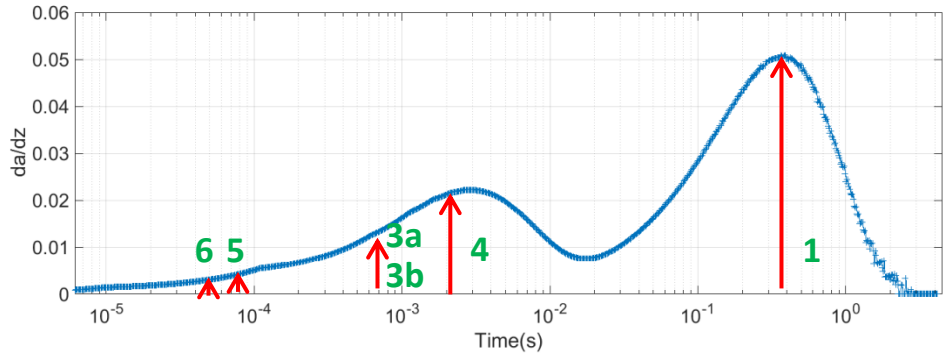

Fig 3.13: Convolution of thermal transient

The convoluted form in Fig 3.13 contains the information of the time constants. The red arrows show the actual time constants used in the simulator to obtain the transient cooling curve. The peaks in the convolution form give an indication of the presence of a time constant. To make these peaks more pronounced, the deconvolution is used on equation (3.22) to find R(z). The simplest form of the deconvolution process is by deriving the Fourier transform of equation (3.22)[73]. Although this method for the extraction of the R(z) is theoretically correct it is important to consider that the deconvolution can be derived only approximately. Especially in experimental measurements, the accurate transient response is never obtained. The measured functions are always affected by measuring inaccuracies, quantization and other noise, which could be enhanced by exact deconvolution [25]. Other methods have been proposed to reduce the noise such as using Bayes iteration [74] Jansson's and Gold's method [75] and the METs [76].

Resolution of the deconvolution form is important. This depends on the weighting function W(z) in equation (3.23). The degree of blurring can be

characterised by the Δz half value width of the weight function [73]. The Δz value for the weighting function (shown in Fig 3.14) is 2.4464 which is just higher than a decade. Note that z is the natural log of time; 1 decade=ln(10); 1z unit =2.3026.

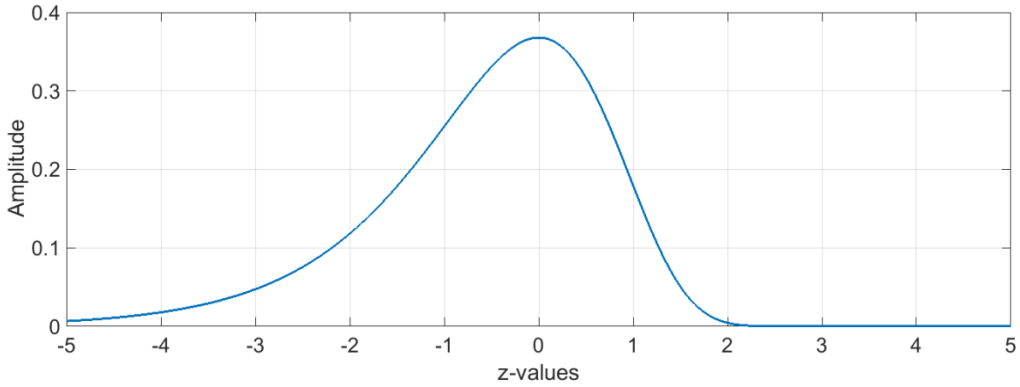

Fig 3.14: Weighting function

This explains Fig 3.13. Although 7 time constants were used, only 2 apparent peaks can be seen. Peaks 3a, 3b (one arrow used because they are very close together) and 4 have been smeared because they lie within $\Delta \boldsymbol{z}$ which is about a decade. The same with 5 and 6 (peak not clear). As a result, after deconvolution to find the time constants, only three resulting peaks at tau= 0.25s, $3x10^{-3}$s, $1x10^{-4}$s were obtained.

The same technique was applied on the experimental measurement shown in Fig 3.15 using the filtered curve. The figure also shows the experimental measurement with a lot of noise. This noise produces a big challenge. The exact form of the waveform is not known as in other applications thereby making it difficult to differentiate between noise and useful data. The impact this has in the deconvolution process is shown in Fig 3.16. It is expected that in a normal situation that the da/dz should not have a negative value. This is one of the computational issues associated with the structure function. More issues associated with the structure function will be discussed further in the subsequent parts.

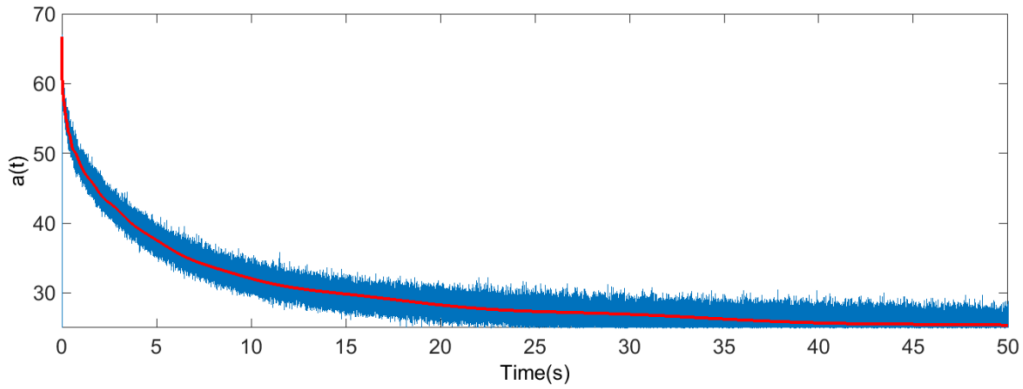

Fig 3.15: Experimental cooling curve, filtered (red) and unfiltered (blue)

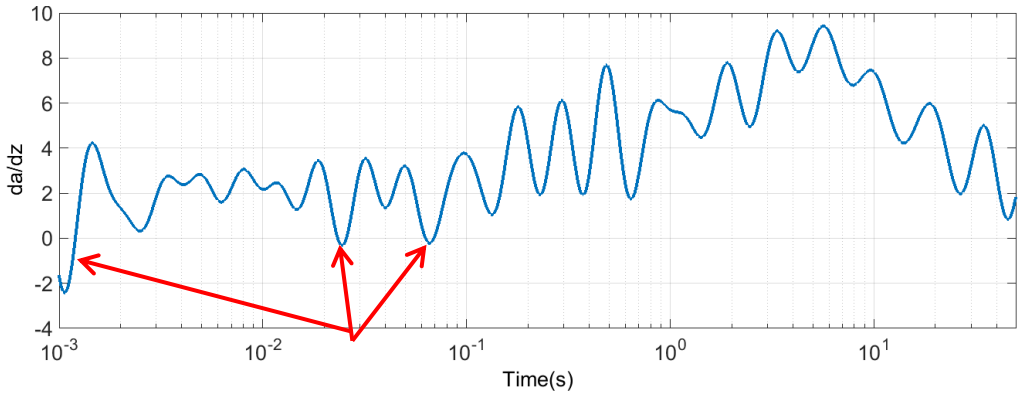

Fig 3.16: Experimental convolution form

3.3 Foster to Cauer Conversion

As mentioned earlier the Foster network does not have any relation to the physical structure. Therefore the Foster network derived from the thermal transient has to be converted to a Cauer type network. The synthesis of passive networks is used to convert the Foster network. The Cauer network is first explained by deriving its equation analytically [77].

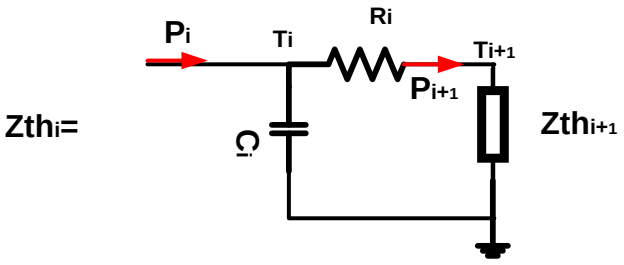

Fig 3.17: Cauer Network Analysis

From Fig 3.17 the following equations hold true:

$$P_{i+1}(s) = \frac{\left(T_i(s) - T_{i+1}(s)\right)}{R_i} \tag{3.24}$$

$$P_i(s) = P_{i+1}(s) + s C_i T_i(s) \tag{3.25}$$

$$T_i(s) = P_i(s)\, Zth_i(s) \tag{3.26}$$

$$T_{i+1}(s) = P_{i+1}(s)\, Zth_{i+1}(s) \tag{3.27}$$

From equations (3.24)-(3.27) and Fig 3.17 the total impedance Zth_i can be considered as the impedance of the capacitor in parallel with the resistance and the impedance Zth_{i+1} as presented in (3.28).

$$\frac{T_i(s)}{P_i(s)} = Zth_i(s) = \frac{1}{\left(s C_i + \frac{1}{R_i + Zth_{i+1}(s)}\right)} \tag{3.28}$$

The thermal capacitances and resistances can be calculated from the heat source to the heat sink by considering the equation of the input impedance in (3.28). The method was shown in [63] where the impedance and the admittance as presented in (3.30) and (3.31) are both used to achieve the goal of extracting the thermal resistances and capacitances sequentially and in a recursive manner. This process is carried out for each capacitor and resistor pair in the Foster network.

$$i = 1.....n \tag{3.29}$$

$$\frac{1}{Z_i(s)} = s C_i + Y_i \tag{3.30}$$

$$\frac{1}{Y_i(s)} = R_i + Z_{i+1} \tag{3.31}$$

Where $Z_{n+1}=0$

To derive the Cauer network from the Foster network, the equation for the Foster network needs to be considered. The equation for the Foster network is derived from the input impedance (Laplace form) using a similar technique as

the Cauer network equation derivation [78]. Therefore, the Foster network for a of a two chain network can be written as

$$Z_{in}(s) = \frac{R_i}{1 + s R_i C_i} + \frac{R_{i+1}}{1 + s R_{i+1} C_{i+1}} \tag{3.32}$$

This can be re-arranged as:

$$Z_{in}(s) = \frac{s(R_i R_{i+1} C_{i+1} + R_i R_{i+1} C_i) + (R_i + R_{i+1})}{1 + s(R_{i+1} C_{i+1} + R_i C_i) + s^2 (R_i R_{i+1} C_i C_{i+1})} \tag{3.33}$$

The relationship between the Foster network and the Cauer network is established as the format of (3.33) matches format equation (3.28) when factorised. By inverting equation (3.33), the capability to obtain the first thermal capacitance in the Cauer network using factorisation is gained because the equation becomes identical to (3.30). The remainder is then inverted to conform to equation (3.31), as a result of which the corresponding thermal resistance is obtained. An example of this process with a two chain Cauer can be found in Appendix 2.

It should be noted that the Cauer parameters (resistances and capacitances) are determined unequivocally by the Foster-Cauer transformation indicating the physical meaning of the Cauer-circuit. On the other hand, the representation of the Foster impedances is ambiguous, since every permutation of pairs of resistances and capacitances in (3.32) leads to a mathematically identical expression [77].

3.4 Structure Function

Structure functions are obtained by direct mathematical transformations from the heating or cooling curves [79]. These curves may be obtained either from measurements or from the simulations of the detailed structural model of the heat flow path. In both cases a unit power step function has to be applied to the structure, and the resulting increase (or decrease, in case of switching off) in temperature at the same location has to be measured in time, following the switching on of the device [80].

The structure function is derived from the thermal resistances and capacitances in the Cauer form (because Cauer networks have a link with the physical structure). The advantage of the structure function is that it does not only reveal the value but also the location of the thermal resistance and capacitance in the heat flow path. There are two types of structure functions: differential and cumulative.

3.4.1 Cumulative Structure Function

The cumulative structure function is also known as the Protonotarios-Wing function[81]. This function presents a graphical representation of structure based on the thermal capacitance and thermal resistance. The cumulative structure function is the sum of thermal capacitances CΣ (cumulative thermal capacitance) in the function of the sum of thermal resistances RΣ (cumulative thermal resistance) of the thermal system, measured from the point of excitation towards the ambient. Discretization of the structure function results in a Cauer network. As pointed in Fig 3.18 each slice represents a corresponding Cauer thermal capacitance and resistance.

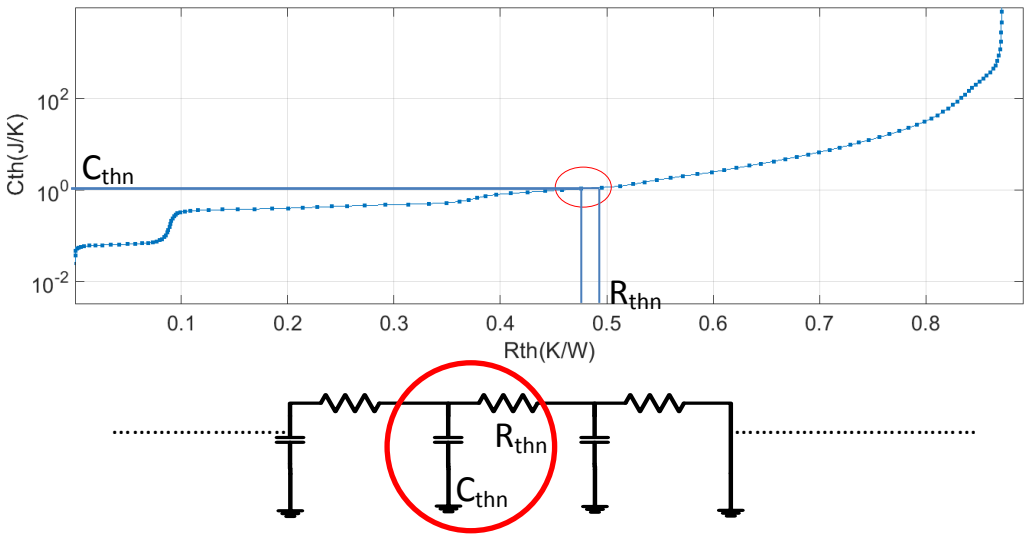

Fig 3.18: Cumulative structure function

Where R_{thn} and C_{thn} :

$$R_{thn} = \sum_{i=1}^{n} R_{thi} - \sum_{i=1}^{n-1} R_{thi} \tag{3.34}$$

$$C_{thn} = \sum_{i=1}^{n} C_{thi} - \sum_{i=1}^{n-1} C_{thi} \quad (3.35)$$

The X-axis which is the thermal resistance is representative of the depth of the device because thermal resistance is proportional to the thickness. The thermal capacitance is on the Y-axis and the step represents sudden transition from one material to another.

3.4.2 Differential Structure Function

In [80] the *differential structure function* is defined as the derivative of the cumulative thermal capacitance with respect to the cumulative thermal resistance, by

$$K(R_{\sum}) = \frac{d\,C_{\sum}}{d\,R_{\sum}} \quad (3.36)$$

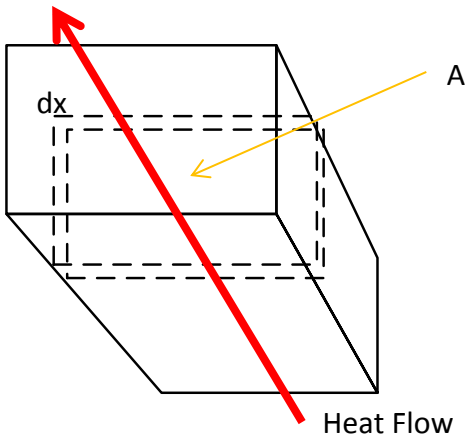

Fig 3.19: One dimensional heat flow model

Considering a *dx* wide slice of a single matter of cross section *A*, this value can be calculated. In this case, the slice resistance is (3.37) and the slice capacitance is (3.38), where c_v is the volumetric heat capacitance, λ is the thermal conductivity and *A* is the cross sectional area of the heat flow, the *K* value of the differential structure function is represented by (3.39)

$$dR\Sigma = dx/\lambda A \quad (3.37)$$

$$dC\Sigma = c_v A dx \quad (3.38)$$

$$K(R_{\sum}) = \frac{c_v A dx}{\frac{dx}{\lambda A}} = c_v \lambda A^2 \quad (3.39)$$

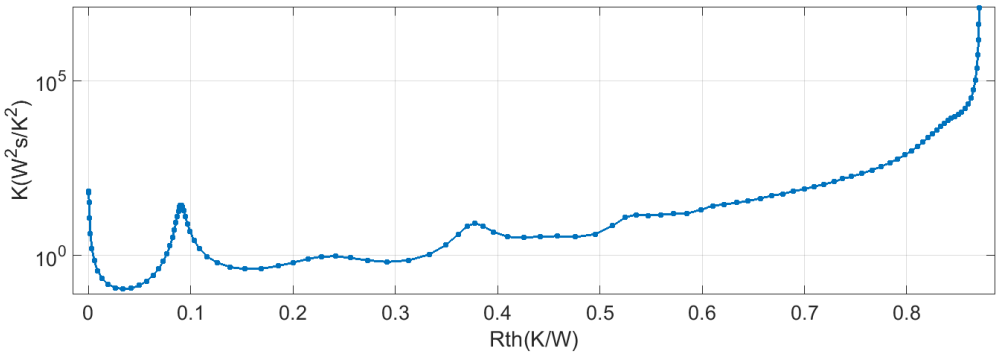

Fig 3.20: Differential structure function of a diode

This parameter is proportional to the *c* and λ material parameters, and to the square of the cross sectional area of the heat flow, consequently it is related to the structure of the system. In other words: this function provides a map of the square of the heat flow cross section area as a function of the cumulative resistance. In these functions, the local peaks indicate reaching new surfaces (materials) in the heat flow path, and their distance on the horizontal axis gives the partial thermal resistances between these surfaces. More precisely the peaks point usually to the middle of any new region where both the areas, perpendicular to the heat flow and the material are uniform.

3.4.3 Computational Issues of the Structure Function

There are some computational issues related to the structure function apart from the ones mentioned previously. The issues with the deconvolution process covers from obtaining thermal impedance curve to the Foster network. It has been indicated that data can be obtained from both experiments and simulations (where noise is practically zero). High sampling frequencies are important to have information of the parts of the device that are closer to the heating element which means more noise. The deconvolution process has been stated previously to be only able to derive the time constants approximately. This applies to all the methods because they have a theoretical limit due to the non-orthogonality of the exponentials which affects the filtering.

Once the cooling curve is filtered and the Foster network is obtained then the transformation from Foster to Cauer becomes the next step. In [61] a reference

model was used to highlight the issues related to the process of obtaining the structure function. In order to be able to calculate analytically the time constant spectrum, a simple geometry is considered and is shown in Fig 3.21.

The slab's dimension are simplified into a uniform slab of length, L and constant cross-sectional area, A. The equation for the structure function as in (3.39) is also used in this scenario. If all the parameters in equation (3.37) are set to the unit value (1) then the structure function will be a straight line as shown in Fig 3.22.

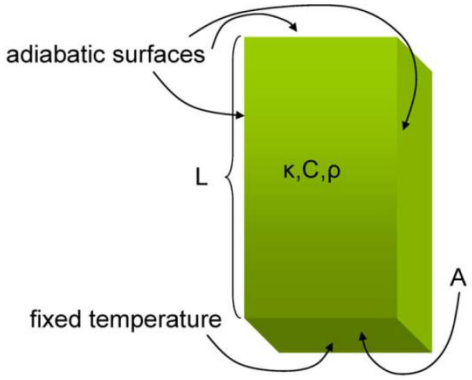

Fig 3.21: Reference model. [61]

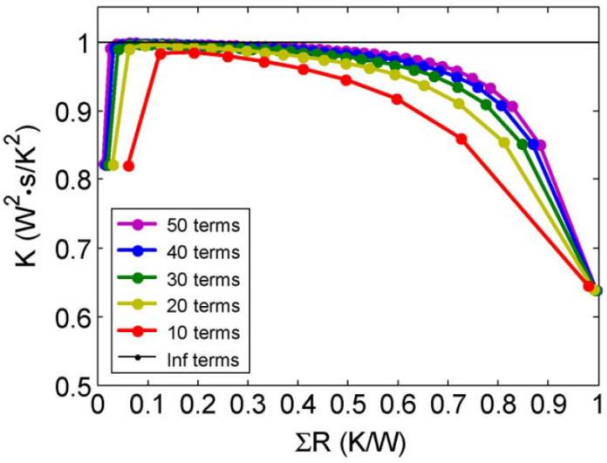

Fig 3.22: Differential structure function showing truncating effects. [61]

The accuracy of the structure function depends on the number of terms used. It can be seen from Fig 3.22 that the number of terms (which means the time constant or RC components in the Cauer network) affects the accuracy of the structure function produced. For an infinite number of terms the structure function is as expected. As the number of terms decreases a truncation effect is

observed. The lesser the number of terms, the more different the structure functions appear in relation with the original. A large number of terms also help to give resolution when plotting the structure function. In the simulation results shown previously only three time constants were identified. This means that only three points will appear on the structure function plot which wouldn't make much sense to use. The obvious solution will be to use a lot of points but this has a setback as well.

A high precision of digits is needed to convert Foster to Cauer. [79] states that if the lumps (RC pairs) exceed a several lumps then extended arithmetic is needed with precision digits of 70 decimal digit and practically unlimited exponential range. There is no analytical formula to know how many precision digits are needed to compute the Foster to Cauer transformation with enough accuracy.

It can be seen that for different digit precision there is a difference in the structure function. In Fig 3.23 the 26 digits has a lot of oscillations which appears different from the 28 and 27 precision digits.

A difference in the precision digit will have an impact on the structure function. Due to all these challenges the focus has moved to implementing the measurement system and using a dedicated system to process the cooling curve into the structure function.

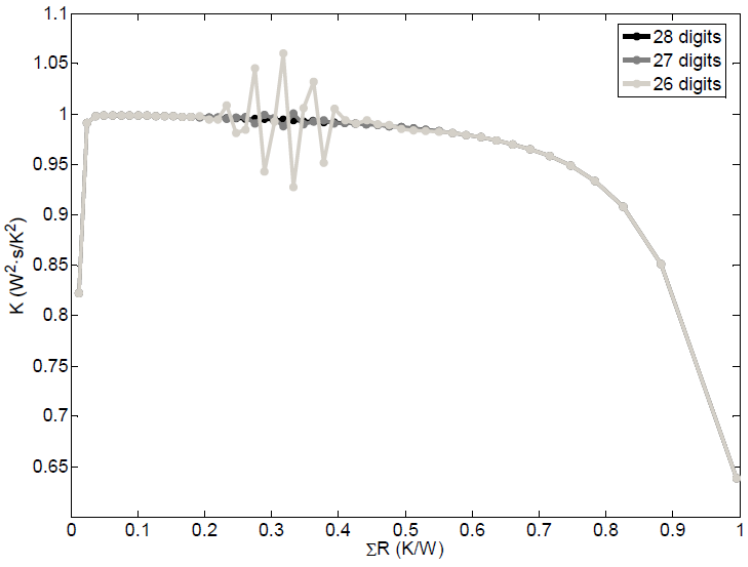

Fig 3. 23: Structure functions showing the influence of precision digits.[61]

3.5 Conclusion

In this chapter the structure function, its relation to the thermal networks and the power devices have been extensively discussed. The process of obtaining the structure function has been elaborated and the challenges associated with it have been discussed. It has been pointed out that there are mainly two thermal networks which are needed for thermal problems in power electronics, the Foster network and the Cauer network. These models can be derived from various sources. It has been shown that the Foster network can be derived from the thermal impedance curve using the graphical method, curve fitting and deconvolution method. The deconvolution method was used in this work to derive the Foster network from the thermal impedance curve. The Cauer network is then derived from the Foster network using the Foster to Cauer conversion. The two types of structure functions have been presented. The challenges related to deriving the structure function have been elaborated.

Chapter 4: On-Board Temperature Profile Acquisition

4.1 Introduction

This chapter discusses the design of the measurement circuit considering its application in inverters used in induction motor drives. As mentioned in Chapter 1 the aim is to do the measurement during maintenance routine, when the mechanical system is idle. The measurement process is to be carried out in such a way that the connections in the inverter are not changed and no additional power components are needed, except for the analogue circuitry used to measure temperature, which can be easily incorporated in a gate-driver board.

In this work, the cooling curve of the power device is needed in order to obtain its structure function. Therefore, a methodology is presented which enables heating up of the power devices (with constant power) in a 3-phase 2-level inverter configuration without the motor load moving. Vector control (Indirect rotor flux orientation) is used to achieve this goal.

4.2 Measuring Technique

As mentioned in Chapter 2, the collector-emitter voltage (Vce) is used to measure the temperature of the IGBT. An N-channel IGBT can be considered as an N-Channel MOSFET on a p type substrate; this is shown in Fig 4.1. The p-n junction at the collector forms a diode.

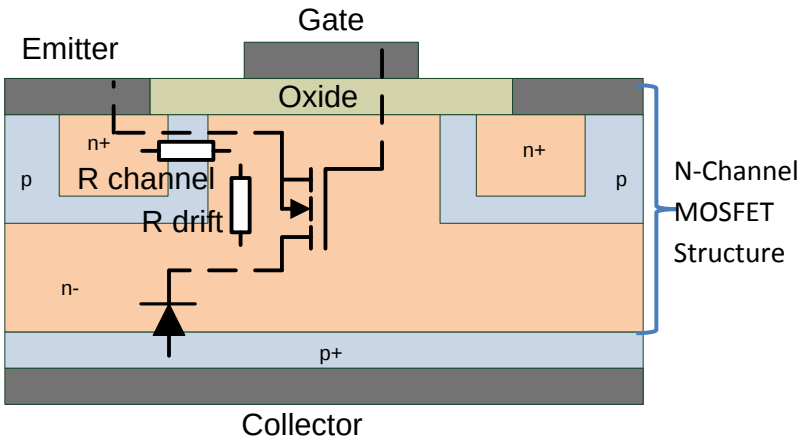

Fig 4.1: (a) N-Channel IGBT (NPT) Cross Section (b) IGBT Equivalent Circuit[55]

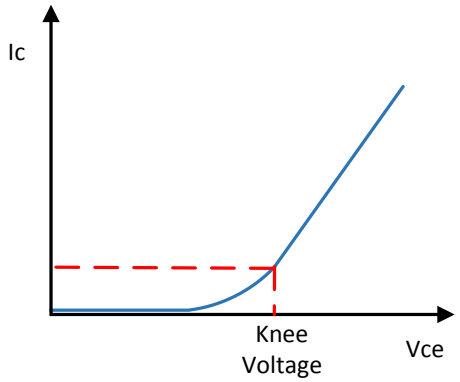

Fig 4.2: Relationship between the Collector Emitter Voltage (Vce) and Collector Current (Ic) in an IGBT

The p-n junction features a well-known temperature dependence on its on-state voltage[53]. This dependence can be used to calibrate the device at different temperatures by using a constant low bias current to prevent self-heating of the IGBT. The characteristic of the MOSFET begins to come into effect after the knee voltage as illustrated in Fig 4.2 of the diode has been surpassed. After the knee voltage, the voltage drop due to the channel resistance ($R_{channel}$) and drift resistance (R_{drift}) shown in Fig 4.1 dominate.

Although the I-V characteristic of a modern IGBT chip exhibits a positive temperature coefficient at nominal current level, that is, V_{ce} increases with increasing temperature for a constant injected current; the temperature coefficient is generally negative for lower currents. In this current regime V_{ce}

decreases almost linearly with growing temperature at a rate ε of approximately -2mV/K [53]. Therefore a linear relationship can be created by measuring the Vce at different reference temperatures as it can be seen in Fig 4.3 for Magna Chip MPMB75B120RH IGBT.

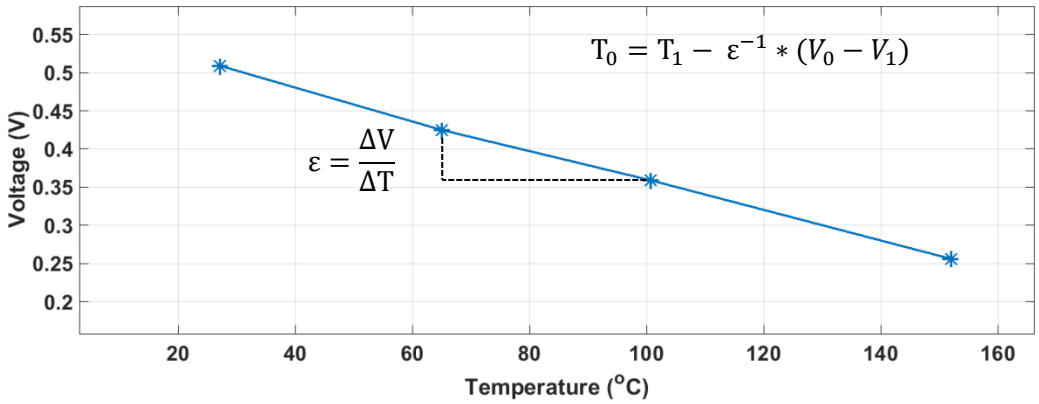

Fig 4.3: Measured temperature dependence of V_{ce} for a sense current I=100mA

In order to obtain the figure shown above, the calibration process needs to be carried out. The calibration process is carried out on a hot plate or oven that has the ability to provide different fixed temperature levels. A fixed temperature is needed in order to ensure homogeneity of temperature at the chip; meaning the whole module is held at a constant temperature.

4.2.1 Basic Off-line Measurement Method

Once the calibration is carried out, the Vce can be used to obtain the cooling curve of the IGBT. A basic method of measuring the cooling curve is, passing a constant high current through the device under test (DUT) to heat up the device using a high current source; a switch is placed in the high current path to turn on and off the high current during heating and measurement respectively. The switch is controlled by the control platform; the controller provides an interrupt to start the measurement of the cooling curve.

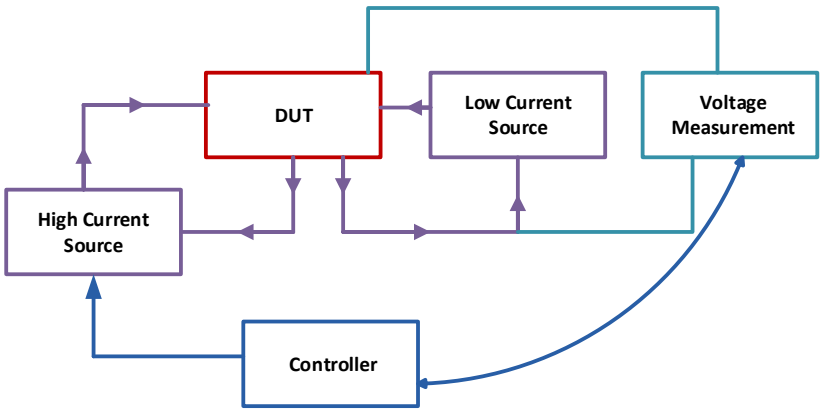

Fig 4.4: Cooling curve measurement chart

The voltage measurement is connected to the controller through a data acquisition assistant (DAQ). When the interrupt is received, the DAQ acquires the cooling curve measurement. During the measurement the constant low current used for calibration passes through the device to create a voltage drop proportional to temperature. This relationship will have been obtained from the device calibration mentioned earlier. The measurement system is illustrated in Fig 4.4.

The different layers of the power module as explained in the previous chapters have different material properties and dimensions. As a result, the different materials have different time constants. Due to the different time-scales involved in thermal dynamics, the logarithmic time-scale is used to process thermal transient after obtaining them. Thermal measurements tend to be noisy, making noise below 0.1 °C very difficult to obtain especially for measurements with high sampling rates.

Different filtering techniques exist [82]. The following techniques are based on determining every new point in the logarithmic time-scale by averaging the linear time-scale [83, 84]. The result is that the number of samples used to compute every new point in the logarithmic time-scale is bigger for the final part of the transient than for the beginning. Therefore, different levels of filtering are applied to the original transient. The final decades of time are more filtered than the initial decades of the transient, therefore noise becomes non-stationary. Another method using moving average filter was developed in

[85]. The problem of this optimal theory is the second derivative computation. When experimental measurements are used, the numerical computation of the second derivative is very problematic due to the presence of noise [86, 87]. The approach used in [82] based on [88, 89] consists in using a multiexponential signal which fits the experimental measurement in a least squares sense.

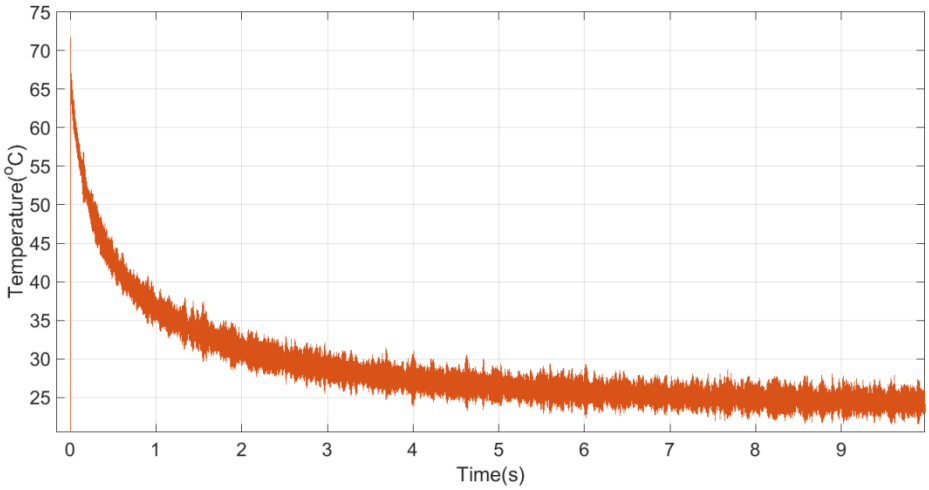

Fig 4.5: Measured Cooling Curve

A measurement obtained using the system in Fig 4.4 is shown in Fig 4.5. The cooling curve is obtained by carrying out multiple measurements and is a result of 10 averages. The aim for this multiple measurement is to eliminate the noise measured in the cooling curve without losing part of the original cooling curve, as opposed to the other techniques mentioned above that make use of a single cooling curve extraction.

As stated earlier, the power module has different layers and different time constants (some fast, some slow). The measurement is taken at a constant sampling rate, with consideration of the total cooling curve time and the smallest time constant. If a high sampling rate is chosen to accommodate the smallest time constant, it might be the case that the number of data points will be in the order of 10^6. This puts a strain on the computation time. On the other hand choosing a low sampling rate to accommodate the time of the cooling curve might lead to a loss of the information contained in the smaller time constants. Processing the curve is made easier by distributing the data points

exponentially to produce the curve in Fig 4.6. It can be observed that the blue curve has more points at the beginning at the curve where the most information on the power devices exists.

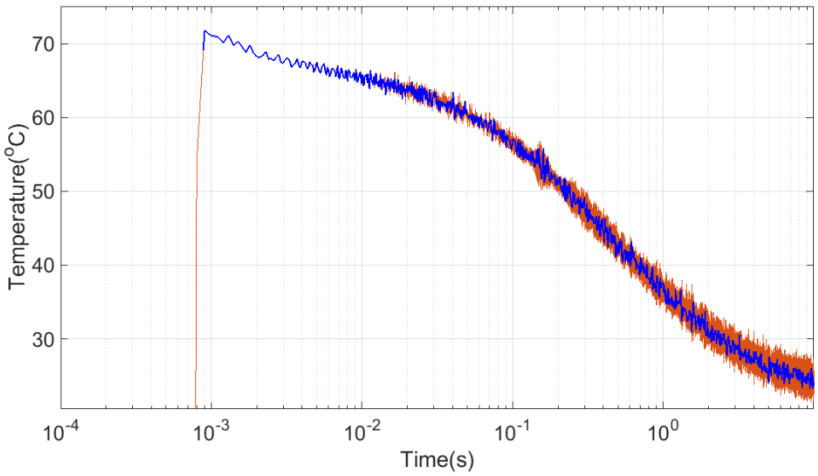

Fig 4.6: Measured cooling curve (log scale-time axis)

4.3 On-Board Module Heating-Up Method

A method of in-situ measurement for traction inverters during non-operational periods is presented. This method makes use of structure function in order to detect degradation in the inverter modules. The structure function is derived from the cooling curve of the device. In order to obtain the cooling curve a heating pulse needs to be applied to the device. This needs to be incorporated in a functioning inverter system driving an induction motor. The process is to be carried out during non-operational phases and without additional devices and components except the analogue circuit for measurement. The method used is passing of heating current through the motor without rotating the rotor as system needs to be stationary during maintenance routines. To understand the methodology used in this work the principles of an induction motor need to be understood (See Appendix 3 section A3.2).

4.3.1 Vector Control

It has been established that in order to rotate an induction motor, a rotating magnetic field is required. In this work the aim is to heat the devices without rotating the motor. A good start in search for a solution is to have a look at the

DC machines. The DC machine operates on the principle that a current carrying conductor placed in a magnetic field experiences a force perpendicular to both the magnetic field and the current. This concept is illustrated in Fig 4.7. A good mnemonic for this concept is the Fleming's left hand rule which states that the thumb is representative of the force acting on the current carrying conductor, the forefinger represents the direction of the magnetic field and the centre finger represents the direction of the current.

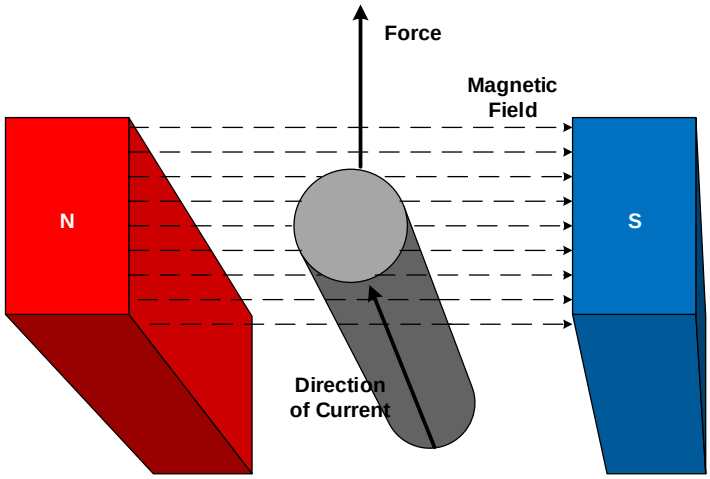

Fig 4.7: Principle of DC motor

The magnetic field is produced by a permanent or an electro-magnet. The current in the current carrying conductor is produced by a DC voltage via the brushes (motors with brushes). This current is called the armature current. In the case where armature current or the field current is non-existent the DC motor remains stationary. To relate this to the induction motor the stator can be considered as the electromagnet and the rotor can be considered as the armature. The induction motor can be controlled in a similar way to the DC machine using vector control. The aim is to make the motor stationary while having current through the stator windings in order to heat the devices. This concept will be explored by considering the dynamic equation of an induction motor. The stator has 3 coils A B C which can be represented by two stationary coils $\alpha \; and \; \beta$. Each coil has a resistance and inductance as shown in Fig 4.8.

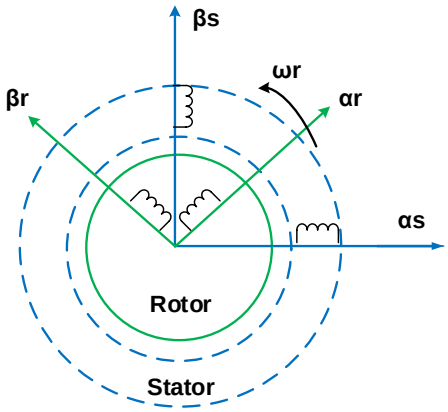

Fig 4.8: Induction motor represented in $\boldsymbol{\alpha\beta}$

$$V_{s\alpha} = i_{s\alpha} * R_s + \frac{d\varphi_{s\alpha}}{dt} \tag{4.1}$$

$$V_{s\beta} = i_{s\beta} * R_s + \frac{d\varphi_{s\beta}}{dt} \tag{4.2}$$

The rotor has 3 coils A B C which can be represented by two moving coils $\alpha \; and \; \beta$. Each coil has a resistance and inductance.

$$V_{r\alpha} = i_{r\alpha} * R_r + \frac{d\varphi_{r\alpha}}{dt} \tag{4.3}$$

$$V_{r\beta} = i_{r\beta} * R_r + \frac{d\varphi_{r\beta}}{dt} \tag{4.4}$$

The above equations can be written for a rotating frame (dq) at electric speed ω_e. The details on how the dq transformation can be found in the appendix 3 in section A3.3. Where

Stator

$$V_{sd} = i_{sd} * R_s + \frac{d\varphi_{sd}}{dt} - \omega_e * \varphi_{sq} \tag{4.5}$$

$$V_{sq} = i_{sq} * R_s + \frac{d\varphi_{sq}}{dt} + \omega_e * \varphi_{sd} \tag{4.6}$$

Rotor

$$0 = i_{rd} * R_r + \frac{d\varphi_{rd}}{dt} - \omega_{sl} * \varphi_{rq} \tag{4.7}$$

$$0 = i_{rq} * R_r + \frac{d\varphi_{rq}}{dt} + \omega_{sl} * \varphi_{rd} \tag{4.8}$$

Where V_s , V_r, I_s, I_r, R_s, R_r, φ_s, φ_r are the stator and rotor voltages, currents, resistances and fluxes respectively. Considering the rotor equations and the fact that ω_e (electrical speed) ω_r(rotor speed) and ω_{sl} should be zero as the rotor should be stationary and the field should not be rotating .Equation (4.8) will be

$$0 = i_{rq} * R_r + \frac{d\varphi_{rq}}{dt} \tag{4.9}$$

The stator and rotor fluxes of the two coils in dq frame are

$$\varphi_{rq} = L_o * i_{sq} + L_r * i_{rq} \tag{4.10}$$

$$i_{rq} = \frac{\varphi_{rq} - L_o * i_{sq}}{L_r} \tag{4.11}$$

$$\varphi_{rd} = L_o * i_{sd} + L_r * i_{rd} \tag{4.12}$$

$$i_{rd} = \frac{\varphi_{rd} - L_o * i_{sd}}{L_r} \tag{4.13}$$

Substituting (4.11) in (4.9)

$$0 = \frac{d\varphi_{rq}}{dt} + \frac{R_r}{L_r}\varphi_{rq} - \frac{L_o}{L_r} R_r i_{sq} \tag{4.14}$$

Where L_o, L_r, and ω_{sl}, are the magnetizing inductance, rotor inductance and slip respectively. Using rotor flux orientation [90], the rotor flux φ_r (yellow) is positioned on the d axis (see Fig 4.9) . This means that the rotor flux has no q component (φ_{rq}=0)

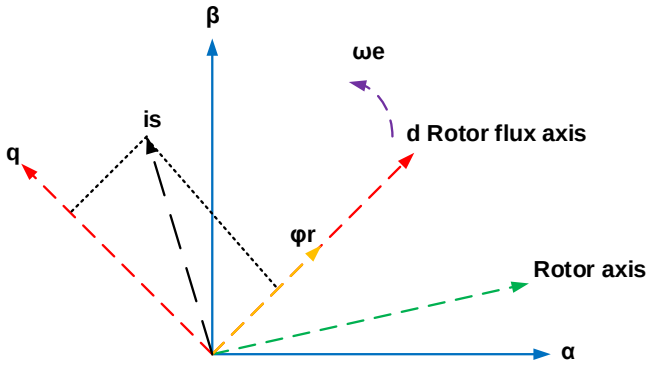

Fig 4.9: Rotor flux orientation [90]

Therefore:

$$-\frac{L_o}{L_r} R_r i_{sq} = 0 \tag{4.15}$$

$$i_{sq} = 0 \tag{4.16}$$

Substituting (4.13) in (4.7)

$$i_{sd} = \left(\frac{d\varphi_{rd}}{dt} + \frac{R_r}{L_r} \varphi_{rd} \right) / \left(\frac{L_o}{L_r} R_r \right) \tag{4.17}$$

Defining the Magnetising current i_m as: $\varphi_{rd} = L_o i_m$

$$i_{sd} = \frac{L_r}{R_r} \frac{d\, i_m}{dt} + i_m \tag{4.18}$$

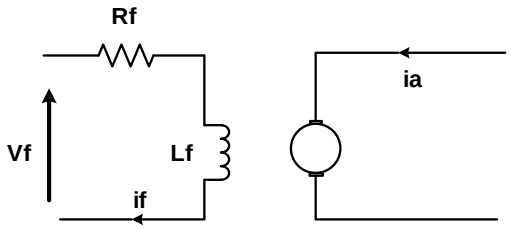

Fig 4.10: Schematic of a DC motor

$$V_f = R_f i_f + L_f \frac{d\, i_f}{dt} \quad \Longrightarrow \quad \frac{L_f}{R_f} \frac{d\, i_f}{dt} + i_f = \frac{V_f}{R_f} \tag{4.19}$$

Comparing (4.19) and (4.18) it is apparent that isd≡if provided field conditions are constant. This means just like in the DC machine isd can be used in the induction motors as the field current [90]. This is true for the isq being the torque current component if the d axis is oriented on the rotor flux axis as shown in Fig 4.9. In this condition, equation (4.8) can be written as where Lr/Rr=τr

$$\omega_{sl} = -\frac{R_r}{L_r i_m} i_{sq} \quad \Longrightarrow \quad \omega_{sl} = -\frac{1}{\tau_r i_m} i_{sq} = K_{sl} * i_{sq} \tag{4.20}$$

The torque equation is defined as:

$$Torque = K * i_{sq} \varphi_{rd} \quad \Longrightarrow \quad Torque = K * i_{sq} L_o i_m \tag{4.21}$$

It can be seen from (4.21) and (4.20) that i_{sq} has a proportionality to the torque. This means that the induction motor can be controlled like a DC machine. The isd serving as the field current and the isq serving as the armature current. From the equations above it has been obtained that for zero speed the isq (torque/armature current) needs to be 0. The isd (field) current can be applied as long as the isq is 0 and the rotor will not rotate. This provides the opportunity to heat up the device without turning the motor. Therefore applying zero torque current i_{sq} and a certain fixed value for the magnetizing i_{sd} was carried out in simulation using indirect rotor flux orientation (IRFO).

There are two known methods the direct vector control and the indirect vector control. The direct vector control derives the rotor flux angle from measured voltage and currents. For the indirect vector control the rotor flux angle is derived from the vector controlled constraint equation. In this work the indirect vector control will be used. This is due to the fewer amounts of sensors needed compared to the direct vector control.

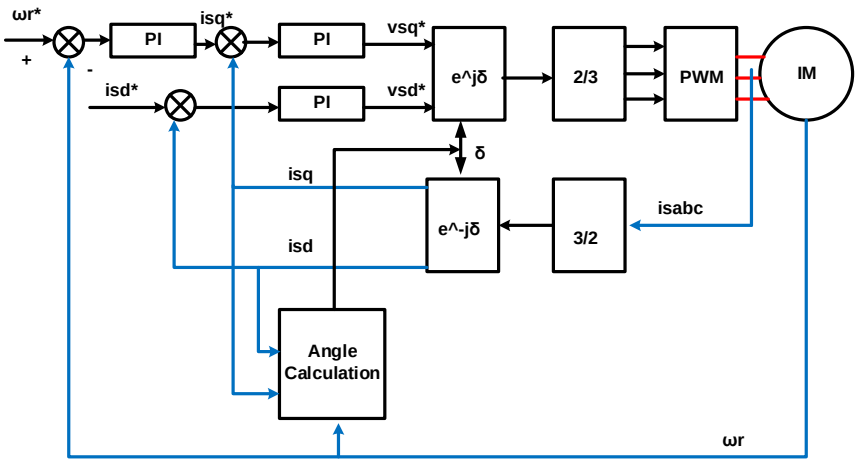

Fig 4.11: Fundamental structure of vector control (IRFO)

The vector control outputs the voltage references in dq domain, these references are then fed into the pulse width modulation (PWM) after a conversion to three phase system. The current from the three phases of the motor are converted to alpha-beta, then to dq currents and then used for feedback. The second feedback is the rotor speed which is then used as a reference to the q current component. Also the rotor speed is used to calculate between the reference point and the d-axis (See Appendix 3 Section A3.3 & A3.4) in order to obtain the conversion from alpha-beta to dq and dq to alpha-beta. A simulation using the parameters shown in Table 4.1 produces the three phase currents shown in Fig 4.12 by applying the zero torque current reference (zero speed reference) and a field reference of 7 amps. The current reference of 7A is based on the maximum magnetising current for the induction motor used in the experiment. This shows a constant current flowing in the three phases, which indicates that the process of heating the device for junction temperature measurement can be achieved. Shown in Fig 4.13 is the temperature of the top IGBT of the first phase.

Table 4.1: Simulation Parameters

Simulation Parameters	Value
Switching Frequency	10kHz
Stator Resistance	2.3 Ω
Stator Leakage Inductance	0.01H
Rotor Resistance	1.5Ω
Rotor Leakage Inductance	0.01H
Magnetizing Inductance	0.1H
Inertia	0.01 $kg.m^2$
DC Link Voltage	700V

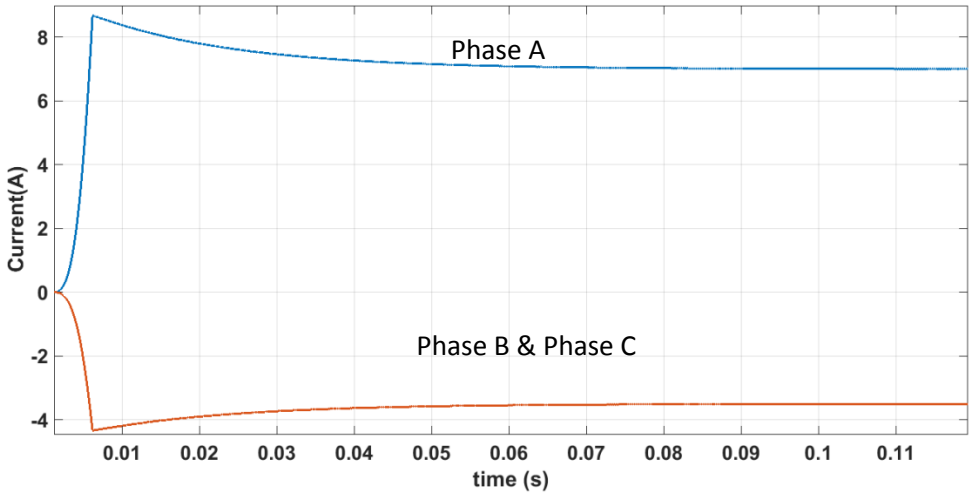

Fig 4.12: Simulation of three phase currents

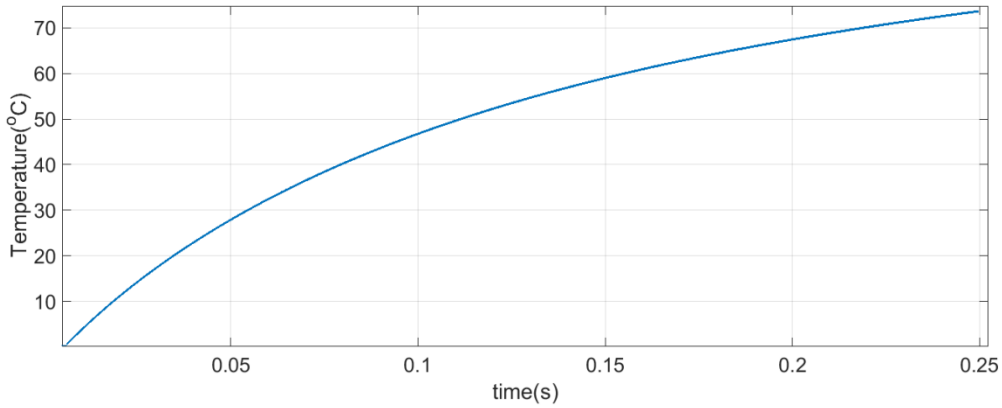

Fig 4.13: Simulation of junction temperature of top switch (Phase A)

Due to the nature of current through the phases, it can be deduced that not all the switches are heating in this condition. A map of the heating IGBTs and the direction of the currents are shown in Fig 4.14. From Fig 4.15 it can be noticed that the only three switches conduct current in this technique. The top switch in phase A and the two bottom switches in Phase B and C. It can be seen from Fig 4.15 that the devices only conduct for a short amount of time. This time is determined by the controller, because the stator resistance of the motor is quite small. Therefore a huge amount of current above the rated current might flow if the timing is not kept under a certain constraint. It is shown in Fig 4.15 by the dashed lines the short time in which a current path is created. The current flows from the top switch of phase A, through the motor and divides equally into phase B and C as confirmed by Fig 4.12.

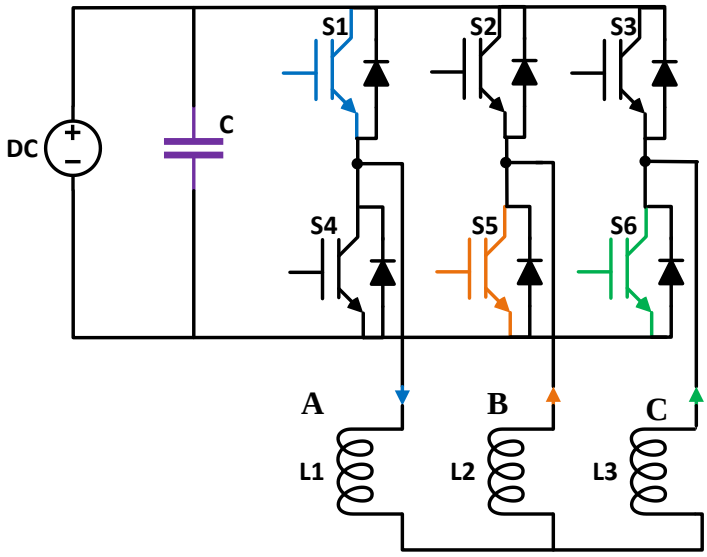

Fig 4. 14: Simulation of three phase inverter showing currents and heated devices

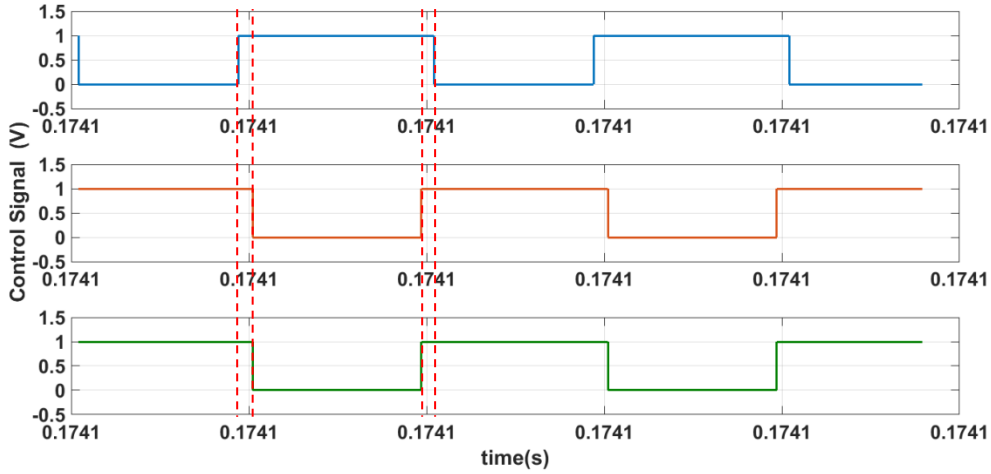

Fig 4.15: Simulation switching sequence of heated devices (time scale = 50μs/div)

In this case the dq transformation is affected by the order of the phases. The instance shown above is ABC, with phase A being first. To heat the other switches the following orders have to be used: BCA and CAB. All these sequences produce zero torque and speed which can be seen in Fig 4.16 and Fig 4.17 .

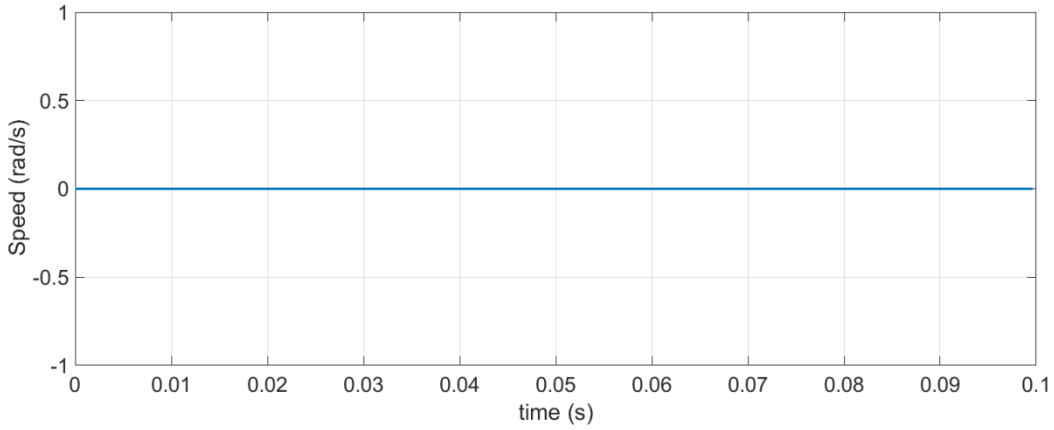

Fig 4.16: Simulation of rotor speed

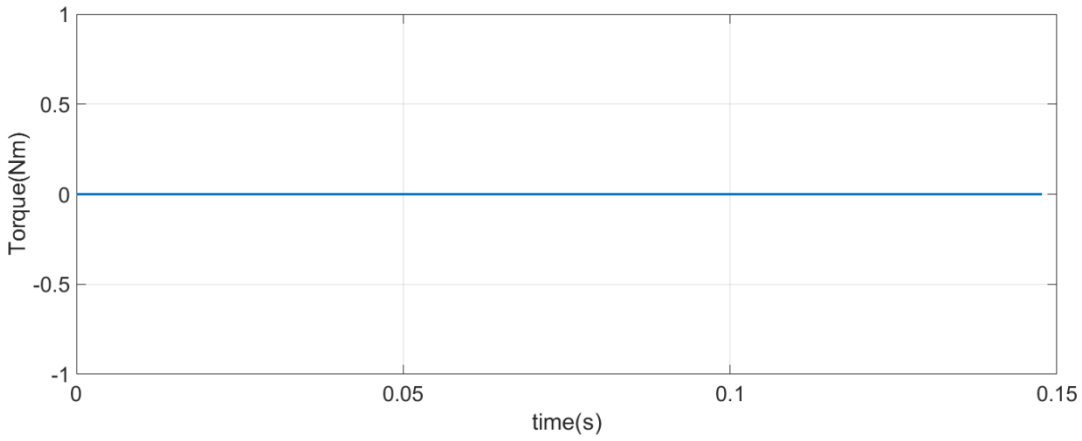

Fig 4.17: Simulation of torque

4.4 Temperature Measurement in the Inverter

The measurement system needs to be applied to a three phase half bridge inverter system that drives an induction motor. This makes the environment which the Vce will be measured a challenging one. The challenge is trying to measure hundreds of millivolts in the presence of hundreds of volts as illustrated in Fig 4.18. Therefore high voltage protection and high accuracy is needed.

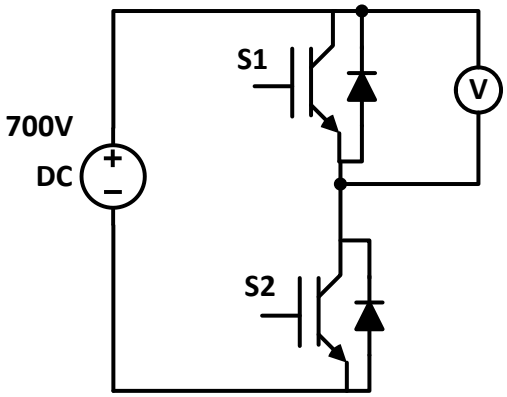

Fig 4.18: Illustration of measurement circuit on inverter

A number of on-board measurement methods for inverter set-up have been proposed in literature. [91] proposes a method to measure the on-state resistance of a CoolMOS devices during operation to determine the junction temperature. The method is implemented by using a detector MOSFET and a resistor in parallel with the MOSFET under test. A large resistance is chosen to limit the dissipation in the detector MOSFET. The voltage across the resistor is measured which is considered to be the same as the drain source

voltage. [16] combines the Vce and a thermal model to determine the temperature. It uses a potentiometer in combination with a differential amplifier to measure the temperature. [92] is similar to [16], it uses an isolation amplifier in conjunction with Zenner diodes, Schottky diodes, capacitors and resistors. This work uses the method presented in [51] to implement the measuring circuit. It follows the principle of a method known as the desaturation protection usually used in IGBT gate drives to protect against short circuits and overload currents. The Vce is measured in order to detect if the current enters the saturation region.

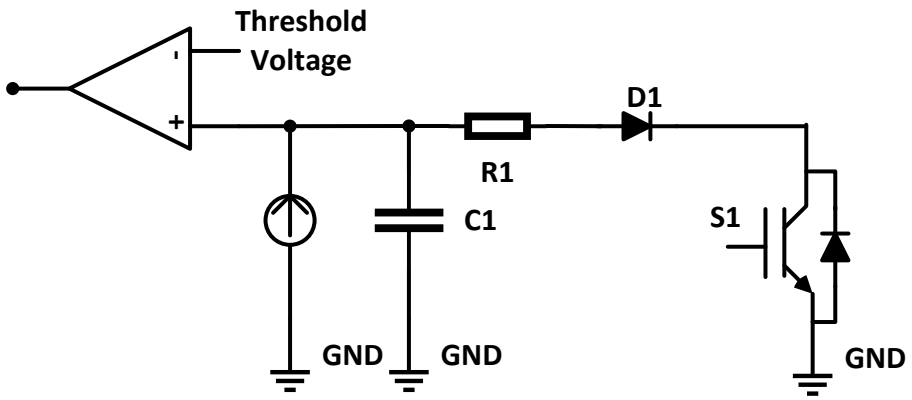

Fig 4.19: Desaturation protection circuit

The desaturation circuit is shown in Fig 4.19; the current source is used to forward bias the diode D1. The Vce and the voltage drop across the diode are measured and compared with the threshold voltage using a comparator. Fig 4.20 shows the basic principle of the measurement system that is used in this work. The current source forward biases the two diodes D1 and D2 when the IGBT is turned on. When IGBT is turned off the diode D1 blocks the high voltage protecting the measurement circuitry from damage.

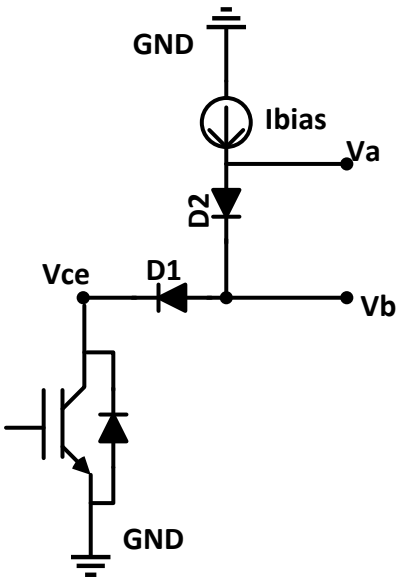

Fig 4.20: Vce measurement

The assumption is that the two diodes D1 and D2 are identical and have the same voltage drop across them (V_{D1}=V_{D2}). So the V_{ce} can be inferred by subtracting the voltage drop across the diode D2 from the potential V_b.

$$V_{ce} = V_b - V_{D2} = V_b - (V_a - V_b) = 2V_b - V_a \tag{4.22}$$

Equation (4.22) can be obtained in a practical sense by the use of operational amplifiers as shown in Fig 4.21. A non-inverting amplifier and a differential amplifier are used to carry out the mathematical operation in equation (4.22). First V_b is amplified by a factor of 2 using the non-inverting amplifier to obtain $2V_b$. The closed loop voltage gain equation of a non-inverting amplifier is:

$$A_{(v)} * V_b = \left(1 + \frac{R_5}{R_6}\right) * V_b = 2 * V_b \tag{4. 23}$$

Where $R_5 = R_6$

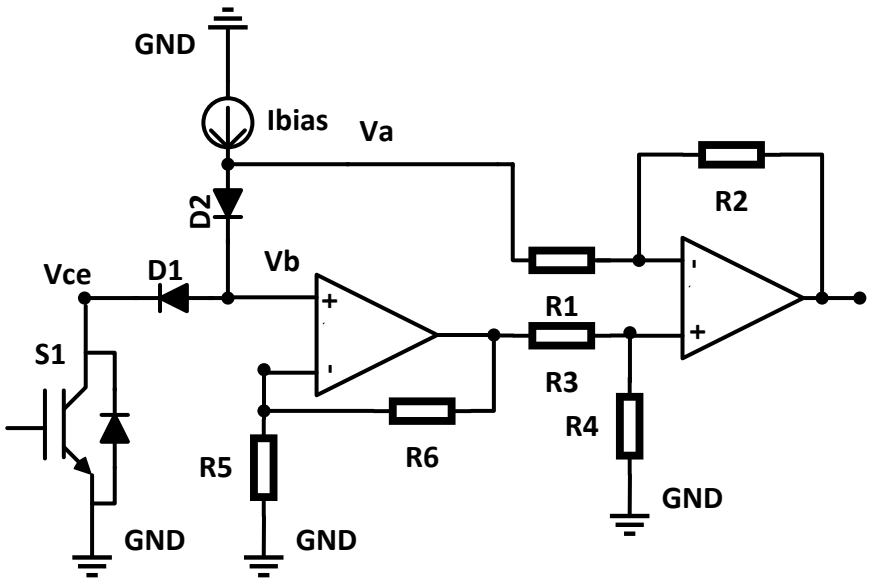

Fig 4.21: V_{ce} calculation using operational amplifiers

V_{ce} is obtained by using a differential amplifier to obtain the difference between the output of the non-inverting amplifier and V_a. The output voltage of a differential amplifier is defined by (4.24); assuming all the resistors are the same, the output of the differential amplifier can be defined by (4.25). The additional benefit of using the differential amplifier is the ability to add gain to the signal. This is helpful because it can provide an optimum use for the range of the analog to digital (A/D) converter. This means an increase in the resolution.

$$V_{out} = 2V_b\left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_1}\right) - V_a\left(\frac{R_2}{R_1}\right) \quad (4.24)$$

$$V_{out} = V_{ce} = (2V_b - V_a) \quad (4.25)$$

According to [51] in order for the measurement circuit to meet the desired specifications, D1 and D2 need to meet certain criteria:

1. the current through the two diodes should be equal. Connecting diodes' common terminals to high impedance input op the amplifier fulfils this condition.

2. the diodes should be thermally coupled to keep the junction temperatures on similar level. This can be done for example by using a two diode in a single package or keeping the diodes in very close proximity.
3. the diodes need to have similar forward voltage temperature coefficients.

4.5 Conclusion

This chapter has presented the design of the measurement circuit considering its application in inverters used for induction motor drives. Details on how the measurements circuit functions have also been presented. The methodology has been presented in this chapter that explains how to heat up the power devices with constant current in a 3-phase 2-level inverter configuration with an induction load. Simulation results have been presented that show a zero speed has been achieved while heating up the power devices. The next chapter will present how the measurement system and the heating technique will be used together to obtain the thermal transient.

Chapter 5: Implementation of On-Board Diagnostics Capability

5.1 Introduction

In this chapter, the theoretical notions presented in chapter 2, 3 and 4 will be deployed as a practical solution. First an overview of the experimental (prototype) set-up of the on-board health monitoring system is presented. The overview of the whole test set-up is shown in Fig 5.1. The experimental rig consists of the power converter, induction motor load, current and voltage measurement, control platform and a PC. The DC-AC converter is a 3 phase 2-level converter which contains 3 half bridges to make up the 3 phases which supply the induction motor. The converter is supplied by a DC power source. The PC is used as an interface to the control platform and also as an interface to obtain the measured data. The control platform has analog to digital converters (A/D) through which all the measurements are converted to digital form. The control platform produces the gate signals that control the devices in the power converter which are as a result of the current measurement (feedback) carried out by the current sensors on each phase. The voltage measurement is used to obtain the temperature. The voltage is converted to digital form and processed to obtain temperature in the PC by using the linear equation.

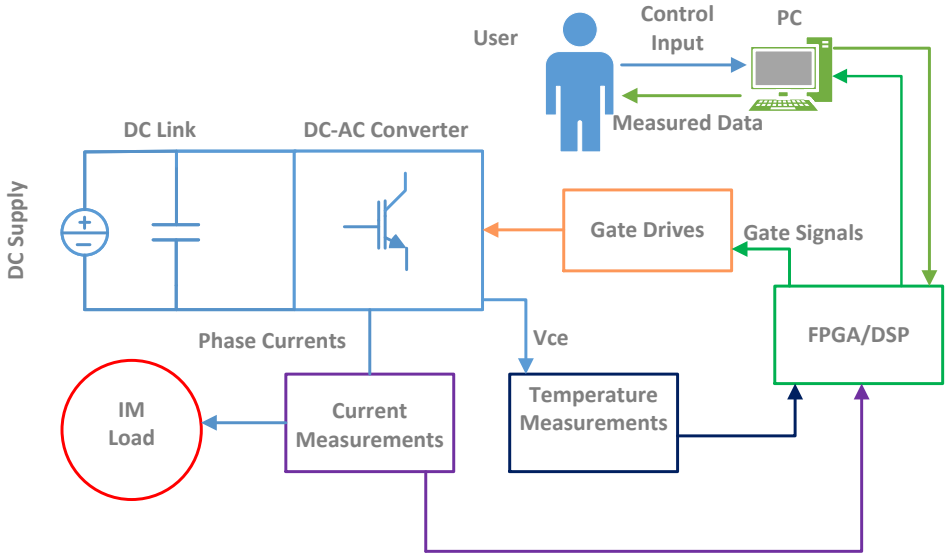

Fig 5.1: Overview of experimental set-up

The different aspects of the experimental prototype such as the power-cell, measurement circuit, gate drives, the control platform, modulation technique and the control design are explained in the next paragraphs. A list of the equipment used in the experimental set-up is shown in Table 5. 1.

Table 5. 1: List of equipment

Component	Specification	Number of units
DC Power Supply	15kW(750V 20A)	1
Power Module	MPMB75B120RH	3
Current Transducer	LEM LA 25-P	3
Electrolytic Capacitor DC	820uF 500V	4
Film Capacitor	5uF 500V& 1u 1200V	2/2
FPGA	ProASIC3 A3P1000	1
DSP	TMS320C6713	1
Temperature Measurement Board	Own Design	1
Gate Drive Board	Own Design	3

5. 2 Power Inverter

As mentioned earlier a Voltage Source Inverter (VSI) is used in this work to drive an induction motor as shown in Fig 5.2. The electrolytic and film capacitors shown in Fig 5.2 are used to decouple the effects of parasitic inductance. The capacitors provide a low impedance path for ripple currents due to hard switch inverters. A combination of electrolytic capacitors and film capacitors has been used in this inverter design. The electrolytic capacitors are used due to their cost advantage and availability of large capacitances. However, they suffer from the limitation of low current ripple capability; the film capacitors are used in tandem with the electrolytic to compensate for this. The value of the capacitance used is calculated using the method presented in [93]. The capacitance value chosen is 820uF; due to the 500V maximum voltage of the capacitors two are used in series. To make the value of the total capacitance 820uF both series capacitor were paralleled. The film capacitors are placed physically close to the switching devices in order to deal with switching transients.

The current measurements are placed on the same power board. Three LEM LA 25-P current transducers are placed on the board with the output of each phase going through a current sensor. The measurements are taken from the board (output of sensors) to the FPGA (controller). The inverter comprises of 6 active switches and the anti-parallel diodes (two switches per module). An image of inverter is shown in Fig 5.3. The switches are controlled using space vector modulation. Space vector modulation (SVM) is one of the preferred real-time modulation techniques and is widely used for digital control of voltage source inverters [94, 95].

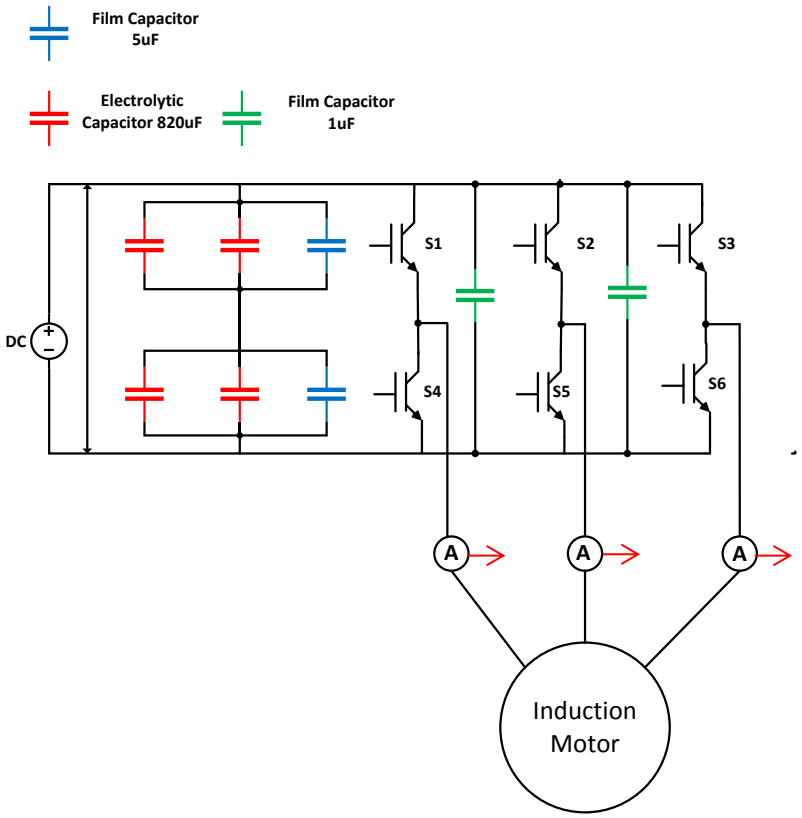

Fig 5.2: Schematic of the power inverter

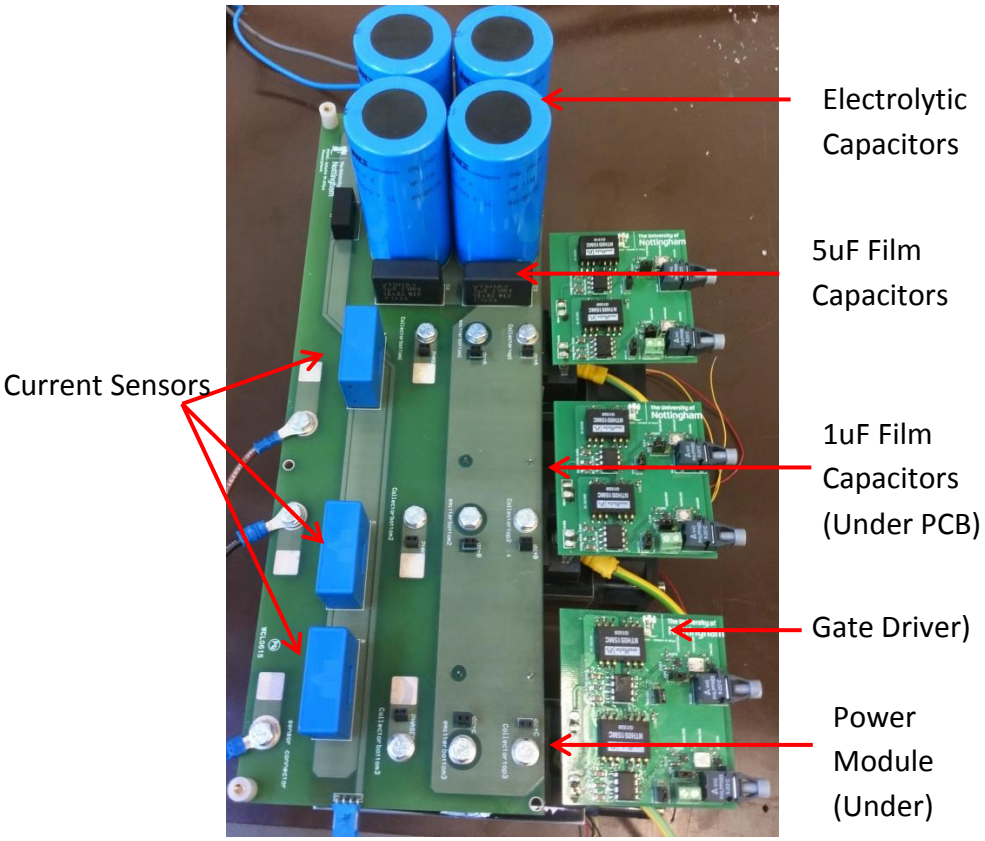

Fig 5.3: Image of power inverter

5.2.1 Space Vector Modulation Scheme

The converter is operated in a way that the top switch of certain phase has to be the opposite with the corresponding switch in the same phase. For example from Fig 5.2, S1 and S4 are always opposites, hence when S1 is on S4 is off to avoid shorting the DC supply. The switching states can be defined as in Table 5.2. This holds for the other two phases. Consequently it can be deducted that the converter will have 8 possible switching combinations as seen in Table 5.3. The table is usually visualized using the space vector diagram. This is represented by a hexagon with a vector on each edge of the geometry having six equal sectors as seen in Fig 5.4. The zero states are represented by the zero vectors (shown in Table 5.3) which corresponds to the center of the hexagon. The other active states are represented by active vectors which are distributed along the edges of the hexagon. The relationship between the space vectors and the switching states can be derived starting from the output voltage of the three phase inverter assuming that it is in the balanced condition.

Table 5.2: Definition of switching states

Switching State	**Phase A**		**Phase B**		**Phase C**	
	S1	S4	S2	S5	S3	S6
1	on	off	on	off	on	off
0	off	on	off	on	off	on

Table 5.3 Switching states and space vectors [96].

Space Vector	Switching State (Three Phases)	On-State Switch	Vector Definition
Zero Vector $\overline{V0}$	111 000	S1,S2,S3 S4,S5,S6	$\overline{V0} = 0$
Active Vectors: $\overline{V1}$	100	S1,S5,S6	$\overline{V1} = \frac{2}{3}V_d e^{jo}$
$\overline{V2}$	110	S1,S2,S6	$\overline{V2} = \frac{2}{3}V_d e^{j\frac{\pi}{3}}$
$\overline{V3}$	010	S4,S2,S6	$\overline{V3} = \frac{2}{3}V_d e^{j\frac{2\pi}{3}}$
$\overline{V4}$	011	S4,S2,S3	$\overline{V4} = \frac{2}{3}V_d e^{j\pi}$
$\overline{V5}$	001	S4,S5,S3	$\overline{V5} = \frac{2}{3}V_d e^{j\frac{4\pi}{3}}$
$\overline{V6}$	101	S1,S5,S3	$\overline{V6} = \frac{2}{3}V_d e^{j\frac{5\pi}{3}}$

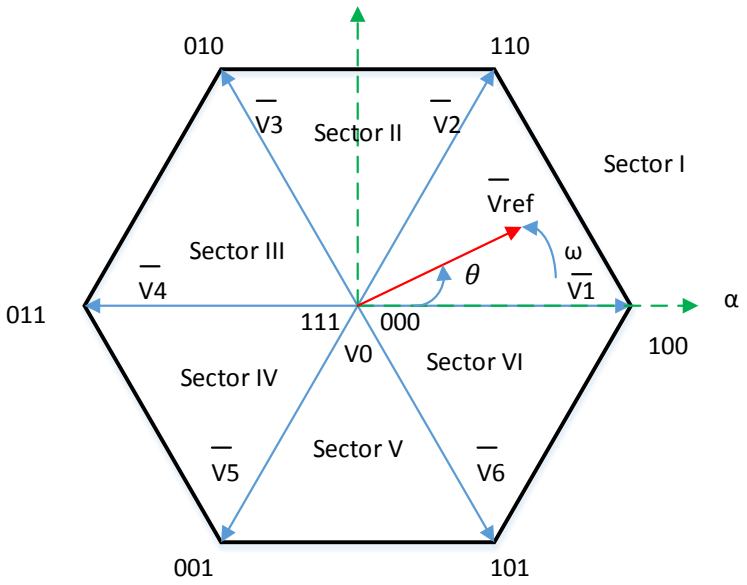

Fig 5.4: Space vector diagram [96]

Mathematically given any of the two phases the third phase can be calculated. The three phases can be converted to two phases by using the Clarke (αβ)

transformation/ (see Appendix 4 A4.1). The space vector can be represented in the αβ plane by

$$\bar{V}(t) = v_\alpha(t) + j\,v_\beta(t) \tag{5.1}$$

Hence the six vectors can be derived using

$$V_n = \frac{2}{3} V_d\, e^{j(n-1)\frac{\pi}{3}} \qquad \text{n=1…..6} \tag{5.2}$$

The active vector and the zero vectors are stationary vectors as they do not move in space. A reference vector ($\overline{Vref}$) rotates passing the various sector moving at a speed of the fundamental frequency. For a given magnitude (length) and position, $\overline{Vref}$ can be synthesized by three nearby stationary vectors, based on which the switching states of the inverter can be selected and gate signals for the active switches can be generated. When $\overline{Vref}$ passes through sectors one by one, different sets of switches will be turned on or off. As a result, when $\overline{Vref}$ rotates one revolution in space, the inverter output voltage varies one cycle over time. The inverter output frequency corresponds to the rotating speed of $\overline{Vref}$, while its output voltage can be adjusted by the magnitude of $\overline{Vref}$. [96]

At any time, the reference rotating vector is in any sector it is surrounded by three stationary vectors. The stationary vectors have a dwell time which represents the duty cycle of the switching states during a switching period (T_s) of the modulation scheme. The volt–balancing principle is used to calculate the dwell time. The volt-balancing is defined by equation (5.3).

$$\overline{Vref} \times T_s = (\overline{V1} \times T_a) + (\overline{V2} \times T_b) + (\overline{V0} \times T_0) \tag{5.3}$$

$$T_s = T_a + T_b + T_0 \tag{5.4}$$

Where T_a,T_b and T_0 are the dwell times for the static vectors, $\overline{V1}$, $\overline{V2}$ and $\overline{V0}$ respectively. The dwell times can be calculated by substituting the vectors from Table 5.3 into (5.3). The equation for the dwell times in the first sector will be

$$T_a = \frac{\sqrt{3} \times Ts \times V_{ref}}{V_d} \sin\left(\frac{\pi}{3} - \theta\right) \tag{5.5}$$

$$T_b = \frac{\sqrt{3} \times Ts \times V_{ref}}{V_d} \sin\theta \tag{5.6}$$

Where θ is the displacement angle of $\overline{Vref}$ from the α axis. The dwell time of the zero vectors can be derived using equation (5.4). The relationship between the dwell time and the $\overline{Vref}$ can be visualised by assuming $\overline{Vref}$ is in the middle of the sector ($\frac{\pi}{6}$) between $\overline{V1}$ and $\overline{V2}$; this results equal times in their respective dwell times. The same process is applicable to the other sectors provided the angular displacement is normalised so as the range of θ can be within 0 and ($\frac{\pi}{3}$). The systematic arrangement of the switching sequence is the next step. This should be carried out under the following conditions according to [96]:

- The transition from one switching state to the next involves only two switches in the same inverter leg, one being switched on and the other switched off.
- The transition for $\overline{Vref}$ moving from one sector in the space vector diagram to the next requires no or minimum number of switchings.

The sequence used in this work can be seen below which match the conditions mentioned above to minimize the device switching frequency.

000 100 110 111
111 110 010 000
000 010 011 111
111 011 001 000
000 001 101 111
111 101 100 000

5.3 Control

The control platform used in this work consists of three boards. It consists of a TI C6713 development starter kit (DSK), FPGA board and an HPI (host port interface) daughter card. In addition to the FPGA chip, the FPGA board

contains connectors for the data transmission between the FPGA and DSP, A/D converters (up to ten channels), hardware comparators for over-current or over-voltage protection (up to ten channels), optical transmitters for the PWM signals, data buffers for the data transmission between the FPGA and other devices. The minimum and maximum voltage range that can be measured at the input of the A/D is ±5V, applying a voltage higher than this will saturate the A/D converter input.

5.3.1 Closed Loop Control

The parameters of induction machines are very important when considering advanced control techniques like vector control. Two procedures used to extract induction motor parameters presented in Table 5.4 are to test the motor under no-load and locked rotor conditions. With the parameters it is possible to calculate the control parameters shown in Fig 5.5. The speed loop is not included because the same results for this application have been achieved by using only the current control loop.

Table 5.4: Motor parameters

	Motor Parameters	**Values**
Magnetising inductance	L_o	0.35H
Rotor resistance	R_r	2 Ω
Rotor leakage inductance	L_{lr}	15.7mH
Stator leakage Inductance	L_{ls}	15.7mH
Stator resistance	R_s	2.3Ω

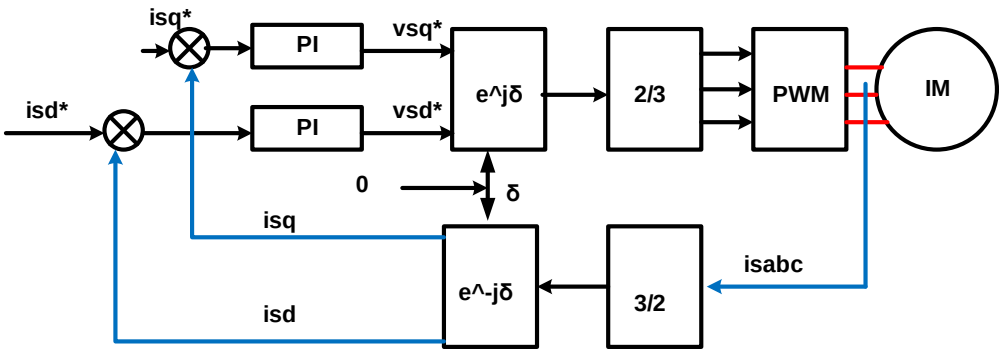

Fig 5.5: Block diagram of vector control (IRFO)

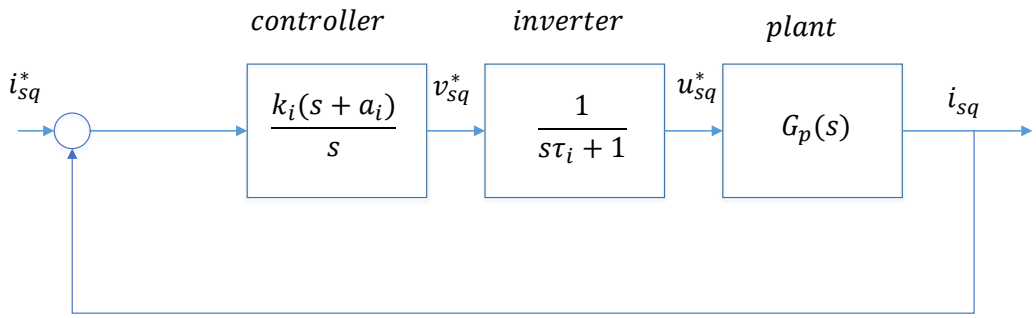

Fig 5.6: Control block

The PI controllers for the isd and isq current are identical hence the same design can be used for both controllers. The control blocks can be seen in Fig 5.6. The dynamic equation for the stator coil (dq) frame while considering the plant design can be written as

$$u_{sq} = R_s i_{sq} + \sigma L_s \frac{d}{dt} i_{sq} \tag{5.7}$$

The Laplace form of (5.7) can be written as

$$u_{sq} = R_s i_{sq} + \sigma L_s s i_{sq} \tag{5.8}$$

$$i_{sd} = \frac{1}{(s\sigma L_s + R_s)} u_{sd} \tag{5.9}$$

The plant can be represented as in

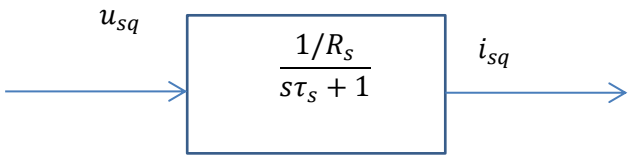

Fig 5.7: Plant transfer function of induction motor winding

The time constant of the plant (τ_s) is much slower than the delay of the inverter. This means the plant transfer function is dominant than the inverter transfer function. With this information the closed loop gain can be written as

$$G_{cl}(s) = \frac{x(s)}{x^*(s)} = \frac{G(s)}{1+G(s)} = \frac{K_i K(s+a_i)}{s^2 + (p + K K_i)s + K K_i a_i} = \frac{K_i K(s+a_i)}{s^2 + 2\varsigma \omega_n s + \omega_n^2} \quad (5.10)$$

Where the damping factor ζ and natural frequency ω_n can be chosen to be 0.7 and 628.32 rad/s. From equation (5.10) the constants of the controller K_i and a_i can be calculated by deriving the following equations

$$p + K_i K = 879.648 \quad (5.11)$$

$$K K_i a_i = 394786.0224 \quad (5.12)$$

Where

$$K = \frac{K_p}{\tau_s} = \frac{1/R_s}{\tau_s} \quad (5.13)$$

$$p = \frac{1}{\tau_s} \quad (5.14)$$

$$\tau_s = \frac{\sigma L_s}{R_s} \quad (5.15)$$

$$\sigma = \frac{1 - L_o^2}{L_s L_r} \quad (5.16)$$

$$L_s = L_o + L_{ls} \tag{5.17}$$

$$L_r = L_o + L_{lr} \tag{5.18}$$

The values from ((5.13) – (5.18)) which can be derived from table 5.4 is then substituted to solve equation (5.11) to derive K_i. The result is then substituted in equation (5.12) to derive a_i. K_i and a_i have been derived to be 2108.18 and 449.28 respectively. These values were inputted in the host PC for both the i_{sd} and i_{sq} controllers. Using the i_{sq}=0A as derived from chapter 4 and the isd reference as 7A zero speed (see Fig 5.9) of the motor is achieved while still being able to heat the devices. The output currents are shown in Fig 5.8 (b), the current in phase A is 7A and the other currents in phase B and C are -3.5A, hence a balanced condition. The isd feedback and reference is shown in Fig 5. 8(a) with the measured value following the current reference.

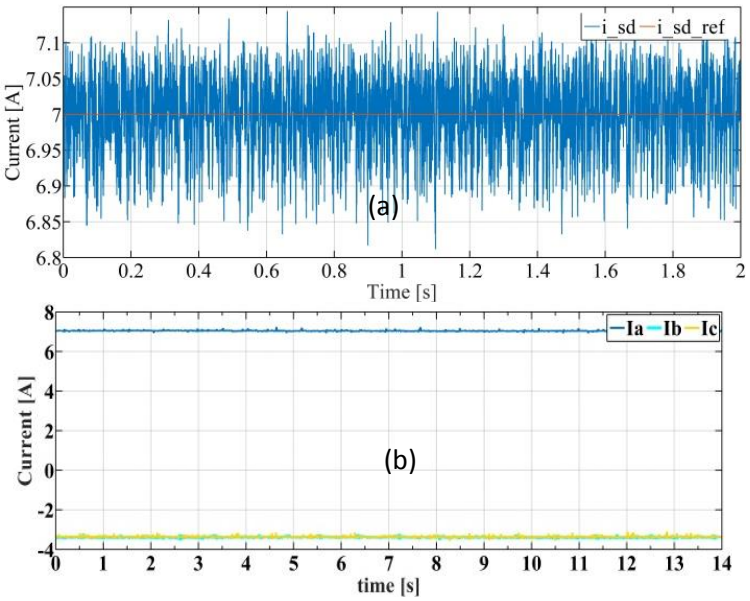

Fig 5. 8: (a) i_{sd} current and reference (b) Phase currents

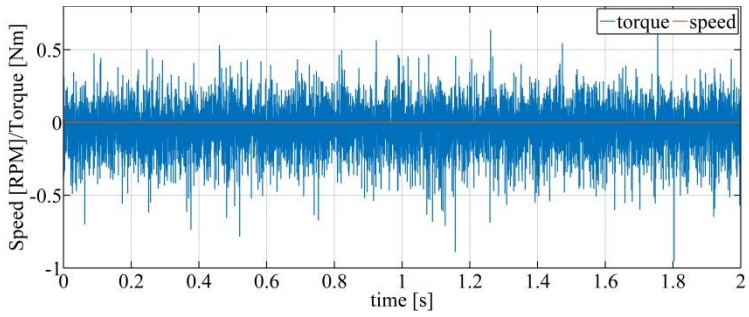

Fig 5.9: Speed and torque of induction motor during heating

5.4 Gate Driver

The schematic of the gate driver design is shown in Fig. 5.10. In this work the dead time is provided in the controller, but additional circuit is used on the gate driver to provide options. The circuit consists of a resistor Rd, a diode D and a capacitor Cd. This introduces a delay at the rising edge of the driving signal and this delay can be adjusted by changing the value of Rd. The gate driver IC (HCPL-3120) and ±15V power supply (NTM0515MC) are used to achieve the required isolation in the gate drive circuit. The gate resistance Rg is chosen depending on the output current of the gate driver IC and the internal gate resistance of the IGBT; the gate resistance is used to control dv/dt of the gate signal. The two Zener diodes at the output of the gate drive are used for protection, to supress any voltage overshoots. The image of the actual gate driver circuit built is shown in Fig 5.11.

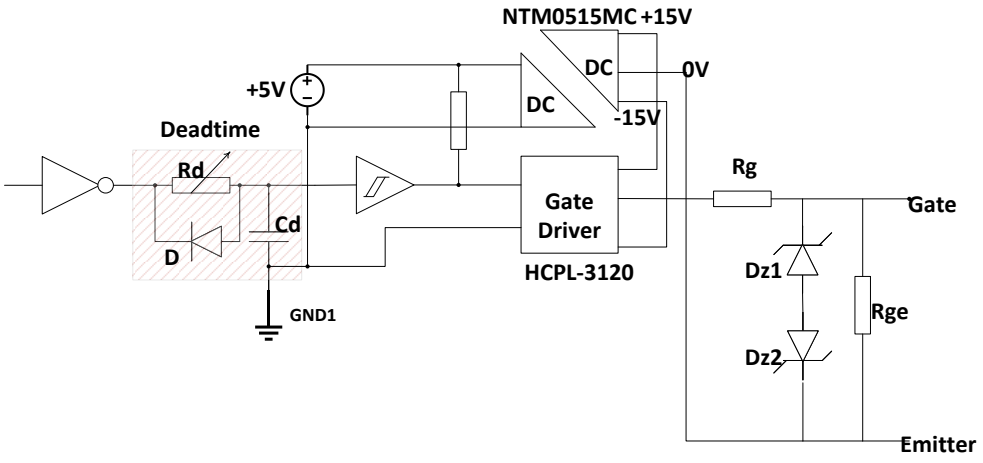

Fig. 5.10: Gate driver schematic

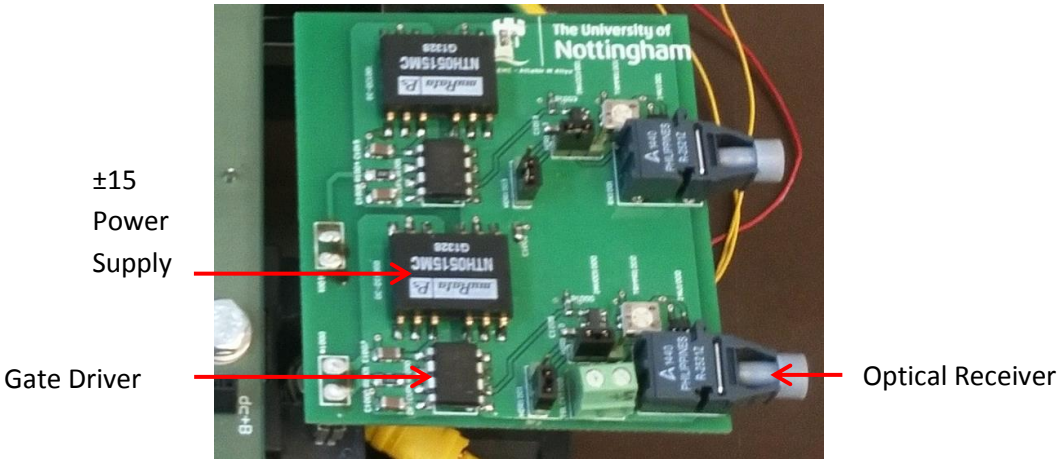

Fig 5.11: Image of gate driver for 2 IGBTs

5.5 Measurement Circuit Design

The measurement circuit was designed with the resolution of the temperature measurement using collector-emitter voltage in mind. The resolution of the collector-emitter voltage with respect to temperature is ~2mV/°C, thus a direct measurement of the collector-emitter voltage inevitably yields to noisy data. The voltage range of the collector-emitter voltage in relation with the temperature is 0.14612V-0.56612V for the range of temperature 0°C-200°C. The range used in this work for the sake of convenience is 0.1-0.6. The A/D converter chosen in order to achieve high resolution is a 12 bit chip LTC1407. For a 12 bit A/D the number of discretization levels is

$$N = 2^{12} = 4096 \tag{5.19}$$

It has been stated in the previous section that the limits for the input of the A/D converter is ±5V. Hence :

A/D full range=10V= 4096 levels

Collector-emitter voltage range=0.5≈205 levels

This means that the minimum voltage that can be recorded in the host PC is 0.0024 V. As mentioned earlier the relationship between the voltage and the temperature is 2mV/°C. Therefore with a direct measurement into the FPGA the minimum temperature that can be measured is just above 1°C. To improve this, the full range of the FPGA has to be utilised by applying a gain and an

offset to the measured signal. This is implemented by making the value of the highest voltage measured (0.6) correspond to the upper limit of the FPGA voltage input (+5V) and the lowest voltage measured (0.1) correspond to the lower limit of the FPGA voltage input (-5V). The gain and the offset needed to achieve this is calculated by solving the simultaneous equations

$$5 = 0.6gain + offset \tag{5.20}$$

$$-5 = 0.1gain + offset \tag{5.21}$$

Yielding: gain 20; offset 7V. This can be implemented using electronics. The principle of the measurement circuit has been presented in Chapter 4. In the practical implementation the values of gain and offset need to be incorporated into the circuit design. A practical simulation of the measurement circuit was carried on LT spice using real components. The schematic of the practical measurement circuit is shown in Fig 5.12. The op-amps 1 & 2 result in the Vce voltage as explained in Chapter 4. The differential amplifier (op-amp) can be used to partly implement the gain derived from equations (5.20) & (5.21). The differential amplifier (op-amp 1) is used to produce a gain of 10 although a gain of 20 is needed. The gain of 20 is obtained in 2 stages due to the configuration used to achieve the offset as will be seen.

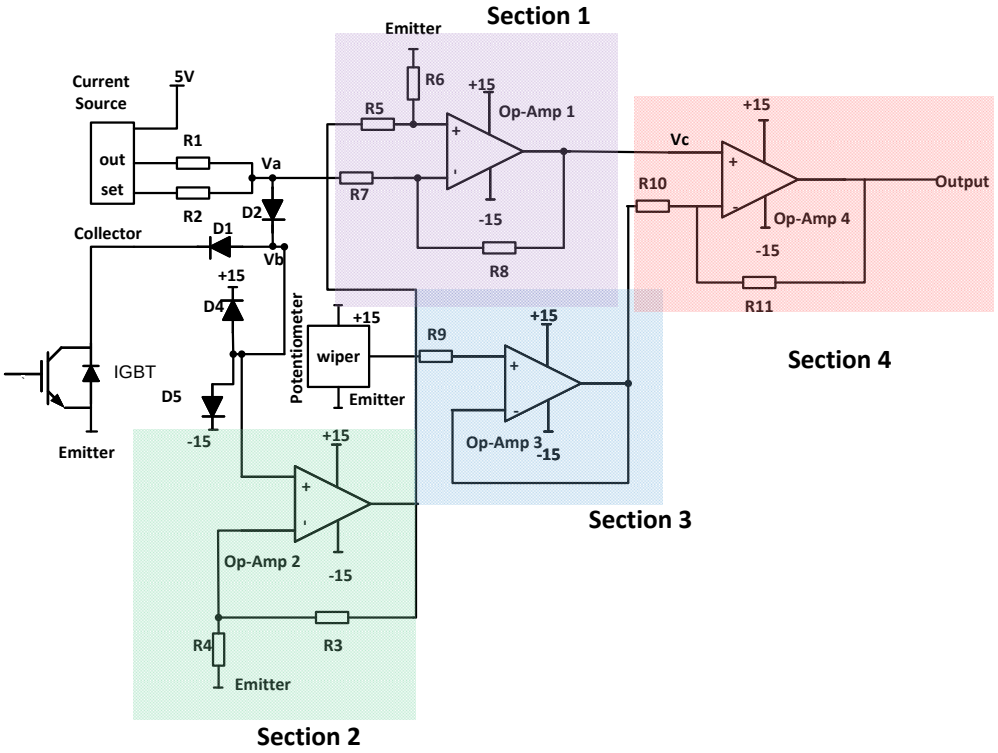

Fig 5.12: Schematic of the for the top device measurement circuit

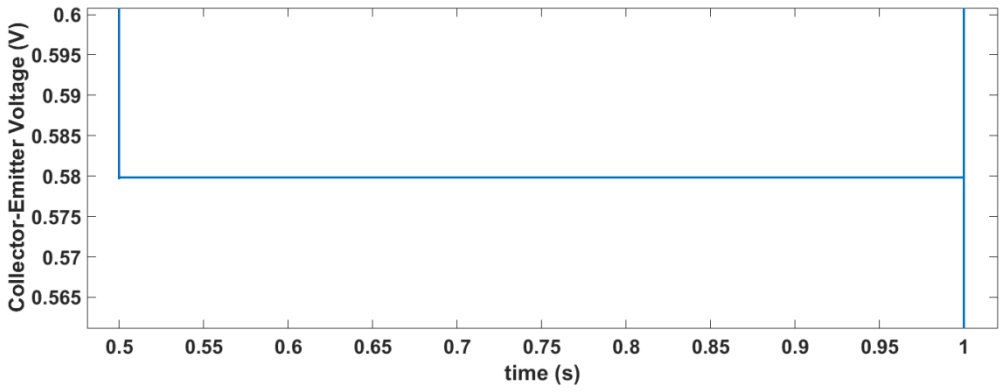

Fig 5.13: Simulation of collector emitter voltage

In the simulation, for the IGBT, an FGA180N33ATD Fairchild 330V IGBT was used. Its V_{cesat} is given in Fig 5.13 as 0.579834 V. From Chapter 4 equation (5.22) is used to derive Vce using the op-amps in section 1(purple) and section 2 (green) shown in Fig 5. 12. Op-amp 2 (green) is a non-inverting amplifier with a gain of 2 and V_b as an input. The output (2Vb=3.25693V) of the op-amp 2 (green) and the node Va (2.67709) is shown in Fig 5.14. By using equation (5.22) the inferred Vce is derived to be 0.57984V, which is the same value as the value measured across the collector emitter.

$$V_{ce} = V_b - V_{D2} = V_b - (V_a - V_b) = 2V_b - V_a \quad (5.\ 22)$$

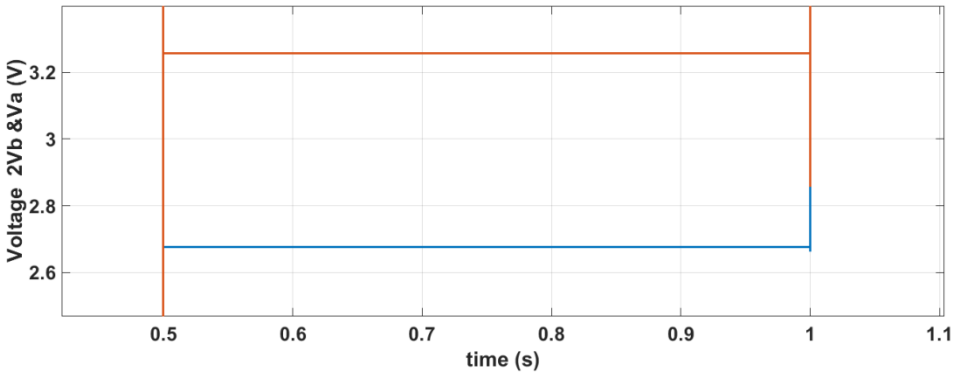

Fig 5. 14: Voltages at the output of op-amp2 and node Va

The op-amps in section 1, 3 and 4 are used to achieve a gain 20 & offset of -7. The differential Op-amp in section 1 (purple) is used to subtract V_a from $2V_b$ (V_{ce}) and apply a gain of 10 by choosing R_5 and R_7 to be 10,000Ω and R_6 and R_8 to be 100,000Ω. This means, considering equation (5.23) the output of op-amp 1(purple) will gain by 10.

$$V_{out} = V_{ce} = 2V_b\left(\frac{R_6}{R_5 + R_6}\right)\left(\frac{R_7 + R_8}{R_7}\right) - V_a\left(\frac{R_8}{R_7}\right) \quad (5.\ 23)$$

Only a gain of 10 is applied in section 1 because a non-inverting amplifier in section 4 is used to apply the offset of -7. Since the gain of a non-inverting amplifier will always be greater than 1, a gain of 2 is applied to get a gain of 20 in total. The equation for the output of op-amp 4 (red) can be written as:

$$V_{out} = Gain * V_c + (1 - Gain)V_{offset} \quad (5.\ 24)$$

From equation (5.24) the part (Gain*V_c) of the equation contains the product of collector-emitter voltage, the gain of the differential amplifier (op-amp1-purple) which is 10 and the gain (Gain) of op-amp 4 (red) which is 2; the second part ((1-Gain)* V_{bias}) gives -7. The bias is applied by the use of a potentiometer using a voltage follower (op-amp 3-blue) to apply the reference voltage on the inverting input of op-amp 4. This is done so that the gain of the op-amp 4 (red) is not affected. Hence a gain of 20 and an offset of – 7 are achieved. The two diodes D5 and D4 are used as protection in case of any

voltage spikes to protect the op-amp 2. The simulation output of the measurement circuit can be seen in Fig 5. 15. This gives an accurate result of 4.596V which is the same as (Vce*20)-7, where Vce is 0.579834V.

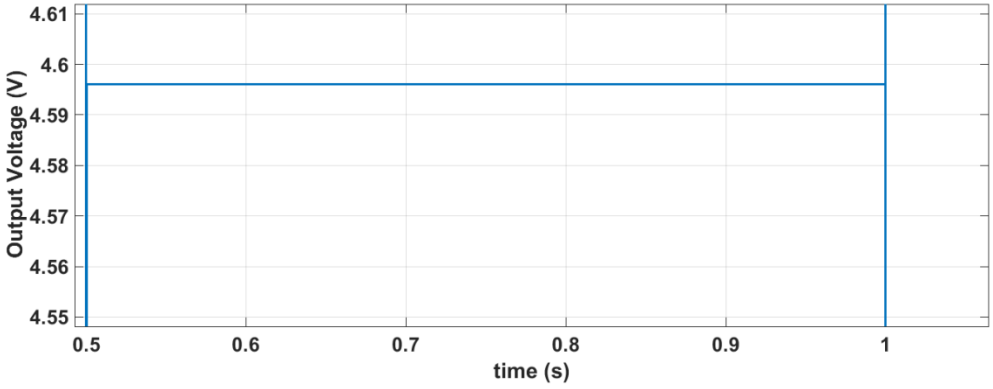

Fig 5.15: Output of the measurement circuit

5.5.1 Protection Board

The reference point of the measurement circuit is the IGBT emitter. Since this is floating, there is a need for galvanic isolation between the measurement circuit and the FPGA board. A high speed isolation amplifier is used to isolate the emitter of the power device from a direct connection to the FPGA. The isolation amplifier used here is the Analog devices AD215BY 120 kHz bandwidth, low distortion, isolation amplifier. One of the applications the isolation amplifier is designed for is high speed data acquisition which is important in this work in order not to lose valuable data. The unity gain configuration of the op-amp for signals within the range ±10 is used (measurements range between ±5V) and can be seen in Fig 5.16. On the output of the isolation amplifier a voltage follower is used with a ±5V supply to limit the output voltage so as to match the limits of the input of the A/D converter.

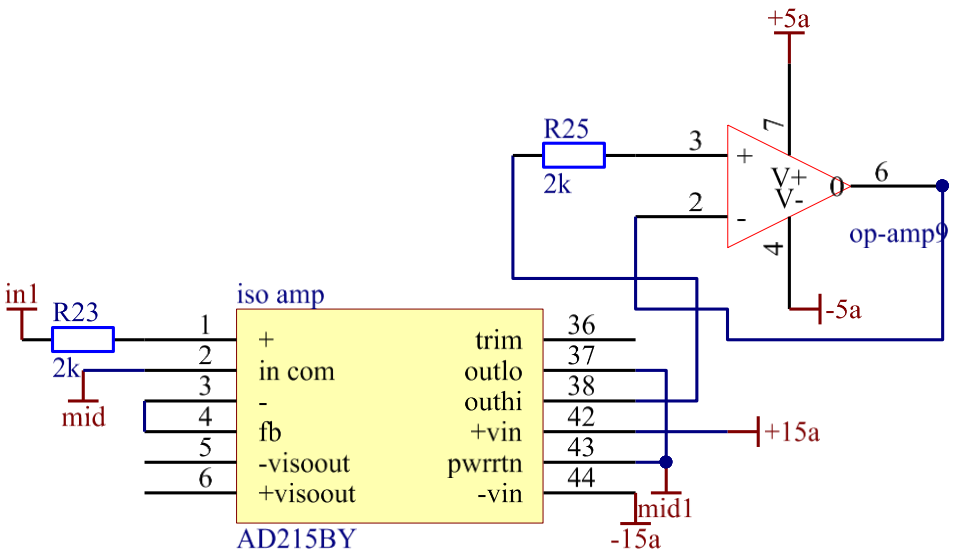

Fig 5.16: Schematic of the isolation board

An image of the measurement board and the isolation board can be seen in Fig 5.17. The diodes used to extract Vce D1 and D3 is the BY203 diodes which have a blocking capability of 2kV. A DC-DC converter is used to supply the op-amps and isolation amplifier with a ±15V. The buffer op-amp the output is supplied by a DC-DC converter of ±5V. Capacitors are also applied to the supply for each op-amp to ensure a smooth DC supply.

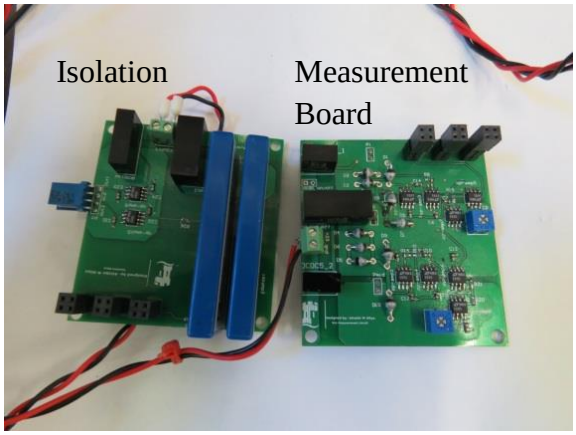

Fig 5.17: Image of measurement circuit and isolation board

A simple test was carried out using the measurement circuit to test the accuracy. At room temperature the voltage of the power device was measured using both the measurement circuit and an accurate digital multi-meter. The measurement circuit is read by the host PC as seen in Fig 5.18. The mean value

of the measured signal is derived to be 5.238V which matches the value on the digital multi-meter. The device was then heated by supplying a current pulse of a few second to test the capability to measure temperature change. The voltage after the heating pulse is removed can be seen in Fig 5. 19. The voltage is then converted to temperature using equation (5.25) as can be seen in figure Fig 5. 20. Equation (5.25) has been derived from the experimental calibration process performed in Chapter 4 involving a hot plate and accurate temperature measurement. The results indicate that the measurement circuit is functioning well.

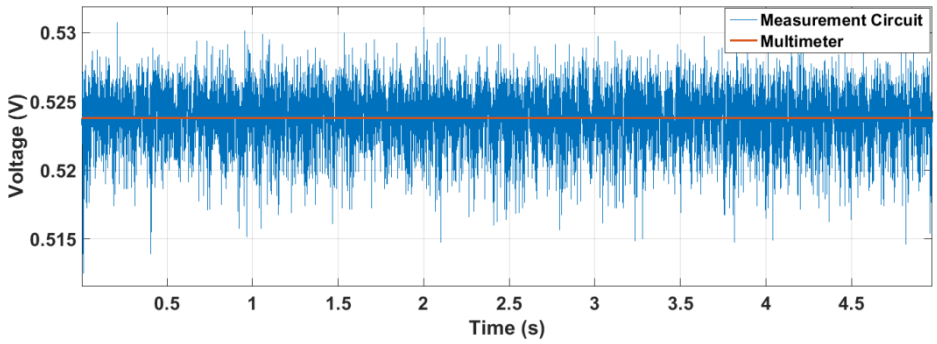

Fig 5. 18: Constant voltage measurement using digital multimeter and measurement circuit

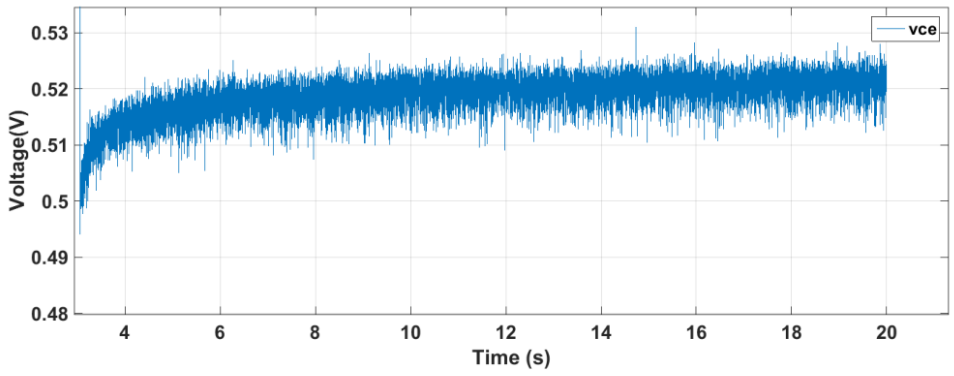

Fig 5. 19: Voltage measurement after the heating pulse

$$Temperature = (voltage * (-496.88)) + 278.64 \qquad (5.25)$$

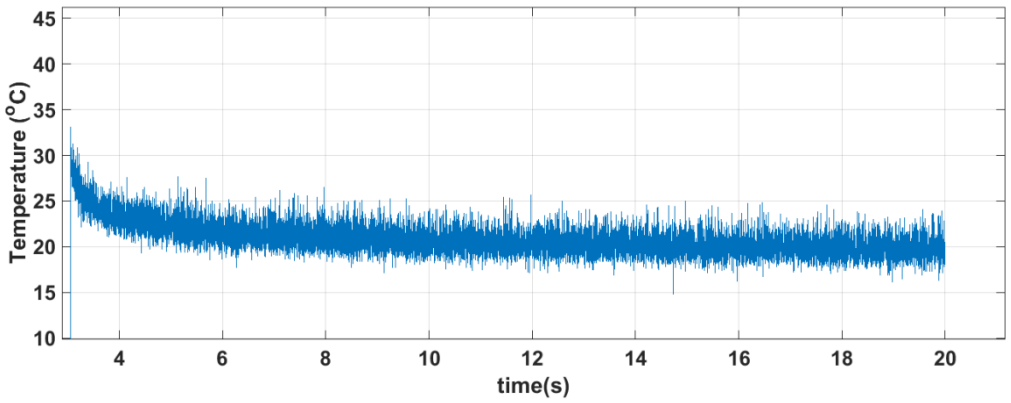

Fig 5. 20: Temperature change after heating pulse

5.6 Conclusion

This chapter has given an overview of the experimental set-up and the equipment used. It has presented the design and consideration made for the measurement circuit and the isolation board. The gate drive design has also been presented. The power converter design, modulation technique (Space Vector Modulation) and control design have also been explained.

Chapter 6: Proof of Concept Demonstration

6.1 Introduction

In the previous chapters, the following have been discussed: power module structure, failure mechanisms and reliability, derivation of the thermal impedance and structure function, on-board temperature acquisition, and implementation of the on-board methodology. The culmination of the aforementioned aspects is the presentation of the results. Before acquiring the results however, some challenges were met in relation to obtaining temperature after heating process. The challenges are first discussed along with the solution devised. Finally the results validating the proposed methodology (use of structure function) are presented. Results showing the implementation of the on-board methodology which is carried out on a module, where measurements were taken before and after cycling is also presented.

6.2 Structure Function Capability

Two diodes were soldered onto a substrate to test if a purposely introduced difference in the solder layer can be identified. One of the diodes was soldered as best as possible with a 100μm solder mask onto the substrate; the second diode had voids intentionally induced by using a quarter of the amount of the solder used in the first sample. The solder when put in the oven spread leaving voids due to insufficient amount of solder. A scanning acoustic microscope (SAM) scan of the solder layer between the chip and the substrates is presented in Fig 6.1(a). The SAM uses sound to obtain the images of the internal parts of an object in a non-destructive fashion by focusing sound waves on small segment of test object. The sound after hitting the test object is reflected, absorbed or scattered, the resultant waves picked up by the sensor is used to determine the material used. An image of the two diodes on a substrate is shown in Fig 6.1(b).

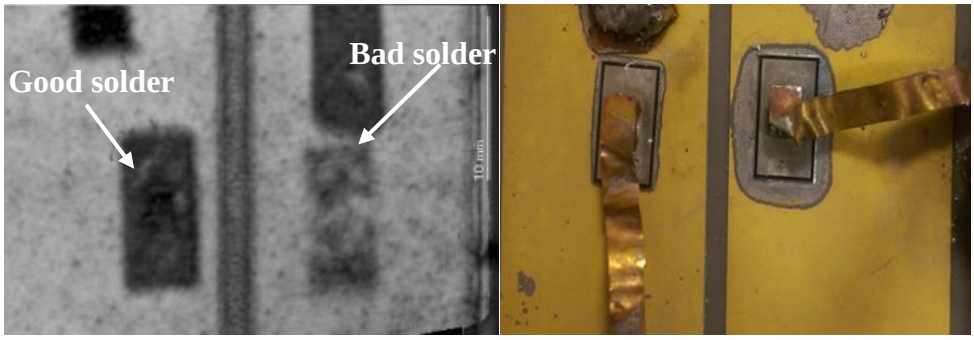

Fig 6.1: (a) Acoustic scan of solder layer (b) camera image

The thermal transients of the two diodes were then derived and are presented in Fig 6.2. Although the thermal transient curves show there is a difference in the thermal path characteristics, it is hard to relate the change to a precise structural feature and make sense of it. Therefore the structure functions are used to process the results.

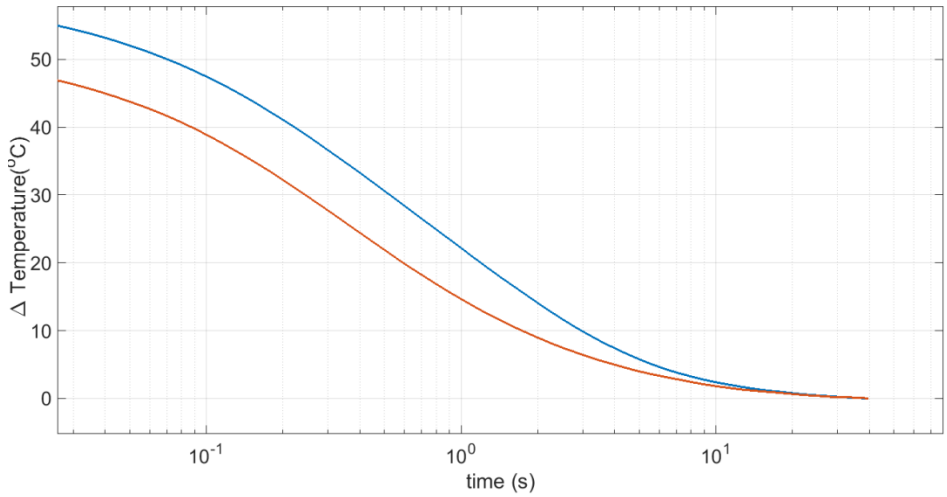

Fig 6.2: Experimental thermal transients for good and bad diode

The differential structure function was used to check the difference in the solder layer between the two test diodes in Fig 6.1(a) & (b). In Fig 6.3(a) the shift in thermal resistance between the well soldered (blue) and badly soldered (orange) diode is noticed at a thermal resistance of less than 0.1K/W. This indicates the difference occurs in the die region as the thermal resistance is proportional to the distance into the device from top to bottom as shown in the cross-section.

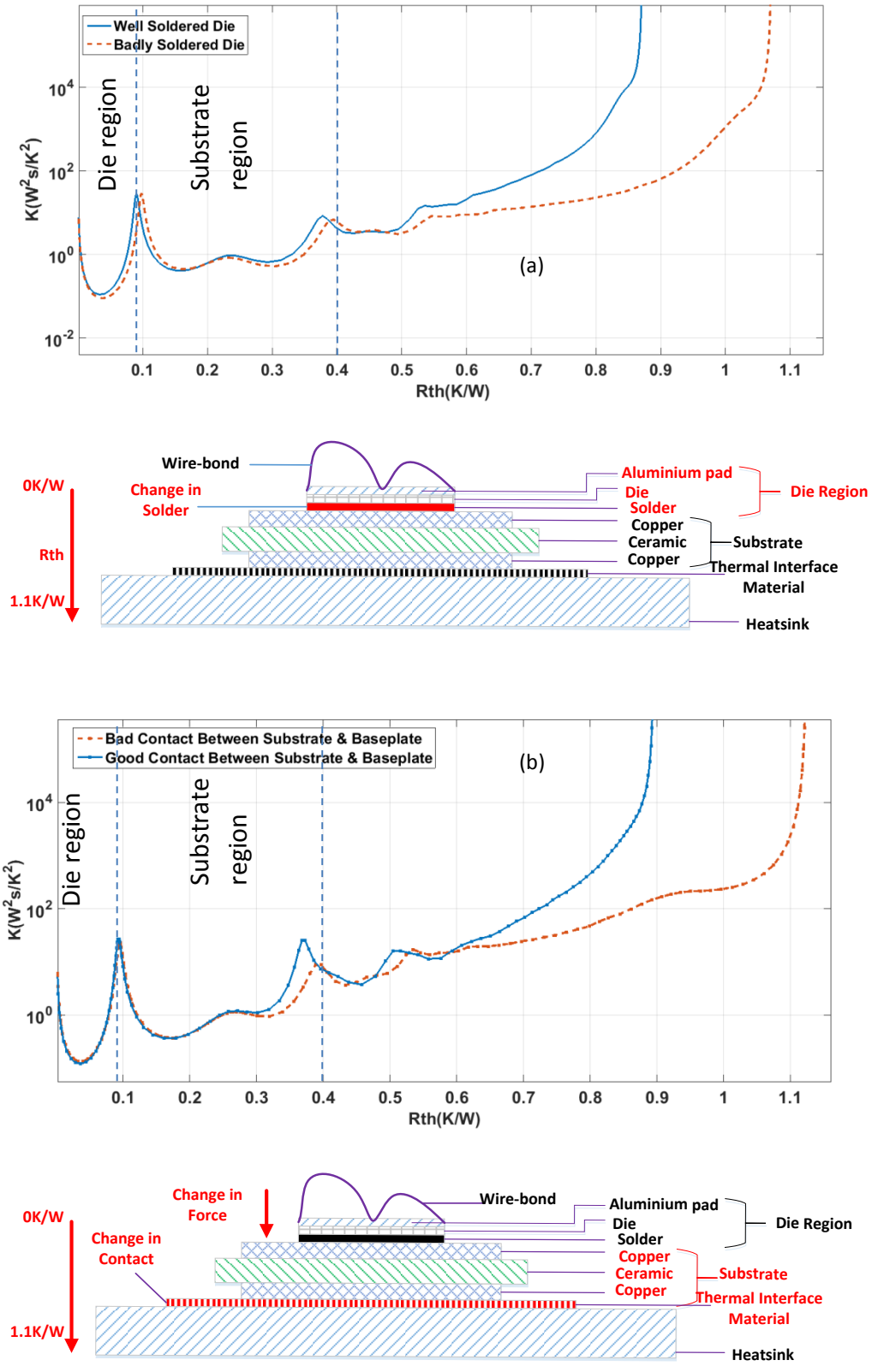

Fig 6. 3: Differential structure function of the (a) solder layer (good and bad) (b) same device with difference at the substrate

Clamps were used to ensure a good contact between the substrate and the heatsink. Therefore by measuring the same diode but changing the force of contact at the bottom of the substrate shows a difference at a higher thermal resistance as seen in Fig 6.3(b). This indicates that not only the change in thermal resistance can be obtained but its location in the die attach or the solder between the substrate and baseplate. A preliminary knowledge of how the device type/batch is structured (number of layers) aids in identifying the peaks accurately. Hence the results and challenges of its implementation on the inverter set-up will be presented in the next sections.

6.3 Inverter Measurements

With the structure function validated in its capabilities, the measurements need to be carried out on realistic inverter driving an induction motor (system). The design parameters listed in Table 6.1 were chosen because test was designed with traction systems in mind. 700V DC was chosen because this is a common voltage for city trams. The current reference of 7A is based on the maximum magnetising current for the induction motor. The test has been carried out successfully at different switching frequencies.

The heating period was determined by first carrying out a full thermal transient test and based on this, it was established that the optimal cooling duration was 100s. The thermal transient obtained gives an idea of the time needed for the temperature to reach steady value. After the heating period of the devices, the cooling curve needs to be measured by passing the low current used to calibrate the device. This is carried out by switching on one of the heated devices and the others off as shown in Fig 6.4. The first attempt at acquiring the cooling curve is given in Fig 6.5, which shows a noticeable distortion in the measurements in the initial instants.

Table 6.1: Set-up parameters

Parameter	Value
DC link Voltage	700V
Phase Current	7A
Switching Frequency	2kHz-20kHz

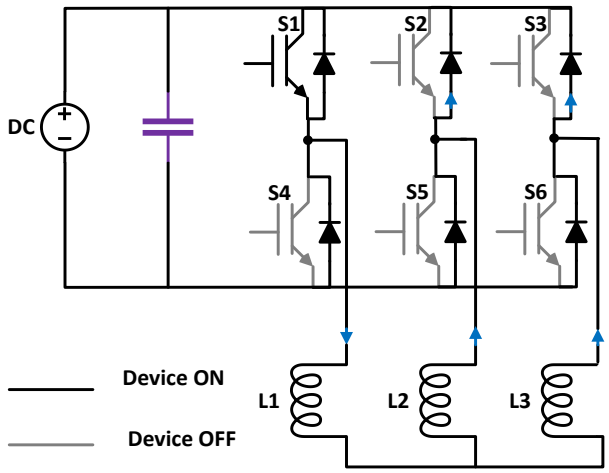

Fig 6.4: Inverter during measurement phase (free-wheeling)

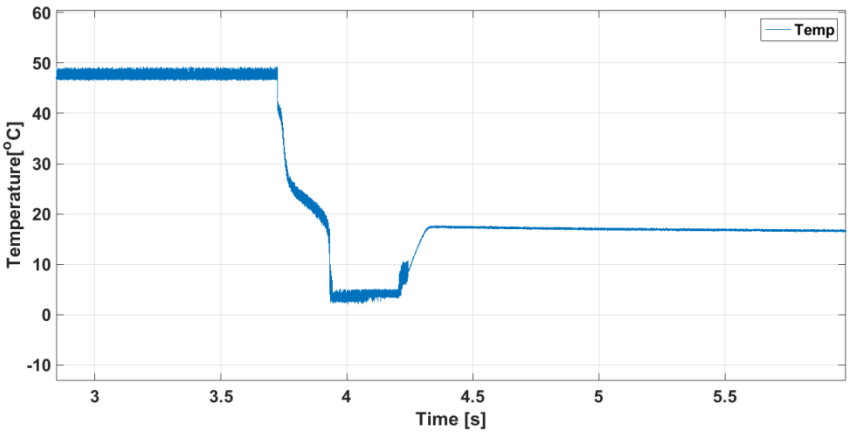

Fig 6.5: First attempt at measurement

The distortion in measurement is due to the energy stored in the motor inductance which is as a result of the heating currents. Magnetising current (i_{sd}) is applied to the motor with no torque current (i_{sq}) in order to keep the motor still. When the heating current is turned off, the current free wheels through the

devices switched on for measurement and the top 2 diodes in the 2 other phases as shown in Fig 6.4. This means that the low current measurement cannot be carried out during the free-wheeling period due to high current flowing in the device meant for measurement in this period. A voltage (collector-emitter) and current measurement of the device was carried out at this stage and it can be seen in Fig 6.6 that the device current takes up to 1s to decay to zero.

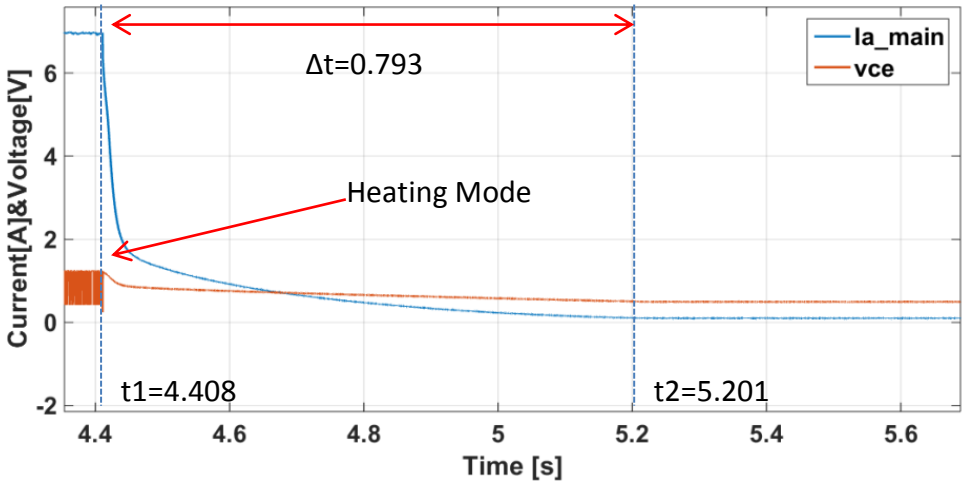

Fig 6.6: Current and voltage (collector-emitter) of DUT

From Fig 6.6, it can be observed that it takes approximately 0.8s for the current to reach the level of the measurement current. If the measurement is to start 0.8s after turn-off, the most important part of the information about the structure of the device is lost as the die, solder and substrate have smaller time constants. The data sheet gives information about the junction to case thermal resistance of the device [97] which is around 0.2 °C/W. By matching this information to the derived normalized temperature (thermal impedance) shown in Fig 6.7, the approximate time constant from the junction to the case can be obtained. In this case, the obtained time constant from the graph is 0.2512 seconds. This means that any cooling measurement that starts past this time constant contains structural information only of the heat sink. Therefore any degradation present in the solder layer between the substrate and the baseplate device will not be recorded.

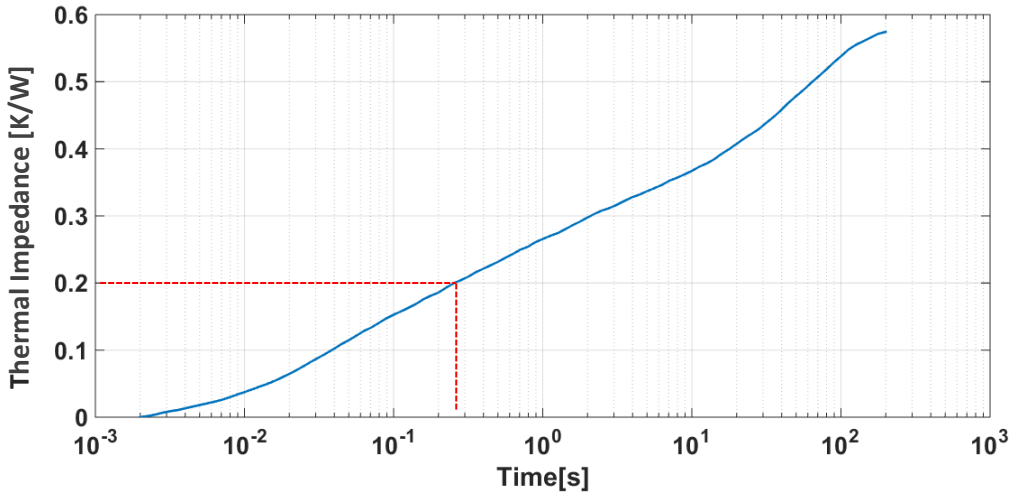

Fig 6.7: Thermal Impedance curve

Since the current stored in the inductor flows through the DUT and the collector-emitter voltage is always measured, the collector current against the collector emitter voltage (I-V curves), that is the output characteristics at different temperatures can be used to estimate the temperature by creating a look-up table. The output characteristics were measured using a curve tracer [98]. In Fig 6.8 the voltage and current passing through the device is measured during turn-off. It can be observed from Fig 6.8 that the measured current and voltage does not fall within the expected temperature range after heating (25°C -125°C) above the cross-over point (inflexion point). The curve indicates the temperature is below 25°C. In Fig 6.9 it can be observed the reference point for the measurement circuit is a floating point and varies from one potential to another. This leads to the possibility of encountering common mode issues. In this work the Linear Technology LT 1001 precision op-amp [99] is used in the measurement circuit explained in chapter 5. By looking up the common mode rejection ratio (CMMR) graph in the data sheet, the issue of collector current and the collector-emitter voltage of the device not corresponding to the temperature range of 25°C -125°C is found to be due to the CMRR for the LT 1001 with respect to frequency. The CMMR starts to drop off just above 10Hz which is quite low, as the drop of the collector–emitter voltage after the device is switched off is quite fast.

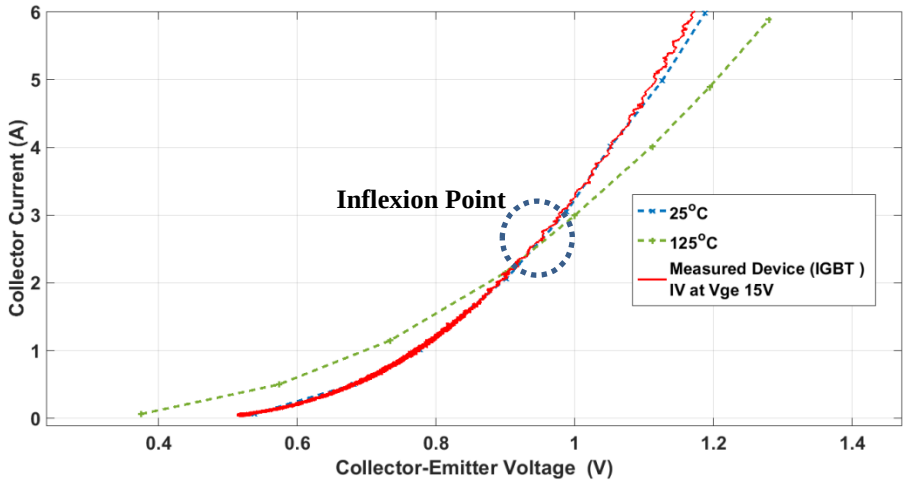

Fig 6.8: Measured curves and IV curves using LT1001

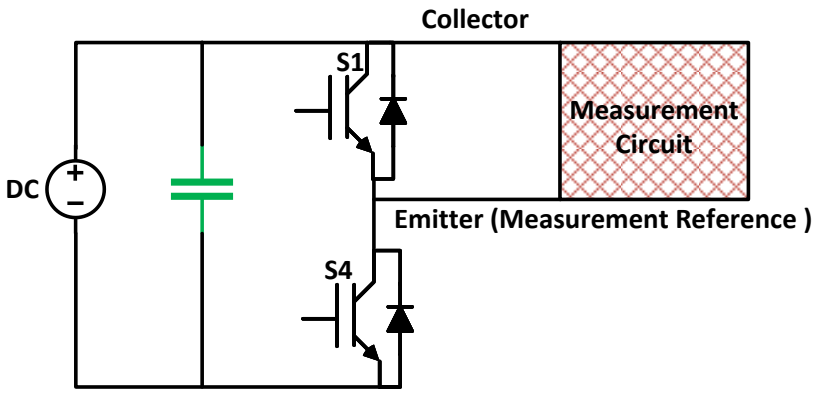

Fig 6.9: Measurement circuit reference point

To solve this issue, an op-amp LT1360 [100] with a better CMMR performance is used as a replacement for the LT1001. The IV curve measurement is carried out with the replacement op-amp LT1360. The result of this measurement can be seen in Fig 6.10 with the measured IV positioned between the 75°C curve and the 50°C curve above the inflexion point and on the 50°C curve below the inflexion point. Therefore this gives the possibility of obtaining the temperature during the transient period whose measurement is distorted.

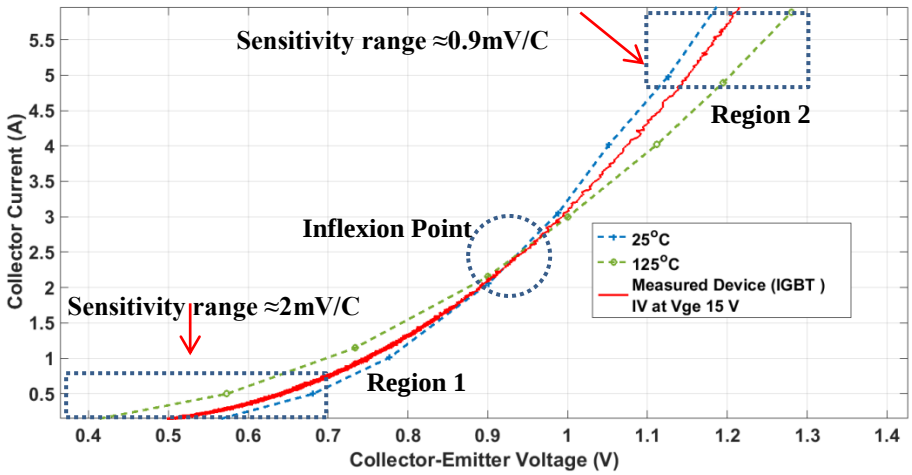

Fig 6.10: I-V curves and measured device current and voltage (LT1360)

However this measured current and voltage of the device passes through a point on the I-V curves where there is no difference in voltage and current for all the temperatures. This means that it is impossible to measure at this point (inflexion point). But above and below this point the sensitivity gradually decreases. The highlighted area in Fig 6.10 below the inflexion point has a lower sensitivity (to noise) of about 2mV/°C, whereas the highlighted area above this region has a higher sensitivity (to noise) of 0.9mV/°C. Since Region 1 is also associated with low self-heating in the device it is preferable to use this region for measurement.

The options to increase di/dt in order to measure immediately after heating are to reduce the inductance or increase the voltage. To reduce the inductance is impractical. To increase the voltage is possible but limited by the system design. The other option is to increase di/dt by changing the current reference of the current controller from the heating current to the measurement current in order to exploit Region 1.

The methodology used to solve this problem is to use the current controller, which was used to heat the devices to force the current, to a low value. As illustrated in Fig 6.11, the reference is changed from 7A to a low value 0.2A in this case. The current changes faster (from 7A to 0.2A in 2ms) than in the previous case. This means that the self-heating is negligible, also faster time constants will be recorded. In this case the measurement starts when the

current falls below 1A. The sensitivity (to noise) of the IV curve reduces as the current approaches zero therefore less error in the measurement.

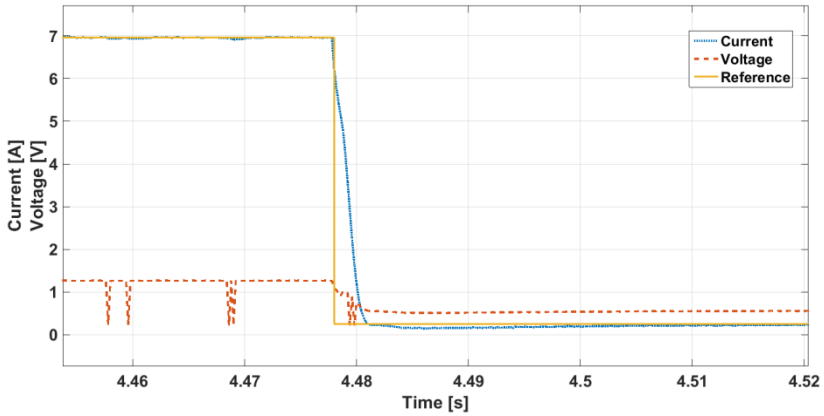

Fig 6.11: Collector current and collector emitter voltage during measurement using vector control.

The junction temperature measurements taken in this case are shown in Fig 6.12 which means that measurement is acquired the very first moments after the heating. The thermal transient measurement (cooling) is affected by noise as illustrated in Fig 6.12, therefore proper filtering needs to be applied in other to make use of the thermal transient curve for further processing. In this work, the filtering technique used is a numerical average of every point on the thermal transient. This is carried out by obtaining multiple thermal transients from the system to ensure that no information regarding the thermal transient is altered during filtration. The filtered curves are obtained using equation (6.1). Where T is the average temperature at a certain time instance, t is the total duration of the thermal transient (or last time instance/point), n is the number of curves to be averaged and a,b,c are the temperatures at a certain time instance, for a single measured curve.

$$Temp_{filtered} = \left[T_1 = \frac{1}{n}\sum_{i=1}^{n} a_i, T_2 = \frac{1}{n}\sum_{i=1}^{n} b_i, \ldots\ldots\ldots\ldots\ldots T_t = \frac{1}{n}\sum_{i=1}^{n} c_i \right] \qquad (6.1)$$

Two filtered curves are presented here to show that this process is repeatable and reliable. This is important because the whole process is done to check for degradation in power modules. The structure function is used to process the

two curves obtained from the inverter. The structure function is used as it provides a comprehensive graphical representation of what is going on in the device. The structure function of the two measured cooling curves can be seen in Fig 6.13. A small difference can be seen in the structure function between two different measurements. The measurements of the thermal transients as presented in Fig 6.12 are distorted by noise. The noise in the measurement can cause artefacts, false peaks in the function. The measured signals undergo an extensive data processing. To obtain the Foster network, the time constant needs to be derived from the thermal transient. This is carried out using numerical deconvolution. The Bayes iteration number determines the quality of numerical deconvolution. A higher Bayes iteration number results in better resolution but also leads to enhancement of noise. The optimal Bayes iteration number of 1000 is chosen for this work. The difference in the two differential structure function curves in Fig 6.13 is due to noise artefacts. This can be differentiated from actual degradation by observing the rest of the differential structure function after a shift in peak occurs. In this case the two curves remain the same even after a shift in peak, while in the case of actual degradation the difference is translated to the end of the structure function curves.

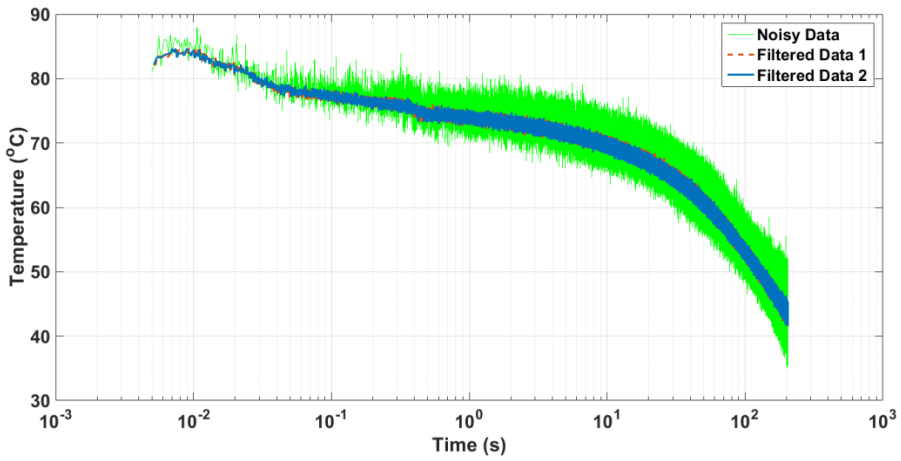

Fig 6.12: Junction temperature curves showing good repeatability

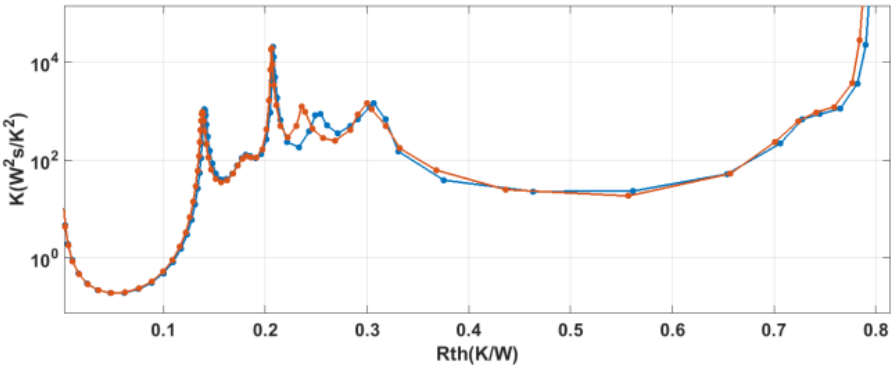

Fig 6. 13 Differential structure function showing repeatability of this process

This methodology is used to check for degradation in the DUT [97]. The module was power cycled using constant current with a current of 52A. An on time 50s and an off time of 60 seconds are used (45.45% duty cycle). The minimum junction temperature and the maximum junction temperature can be seen in Fig 6.14. The minimum junction temperature during cycling is 6°C and the maximum junction temperature is 137°C before initiation of degradation process. Degradation can be seen in the maximum junction temperature curve after 8000 cycles. This is also the case with the ΔTj because the minimum junction temperature is constant as shown in Fig 6.15. The initial ΔTj before degradation was chosen in order to accelerate the cycling process. The maximum ΔTj is chosen that will not exceed device maximum operating temperature by choosing the appropriate cycling current and duty cycle.

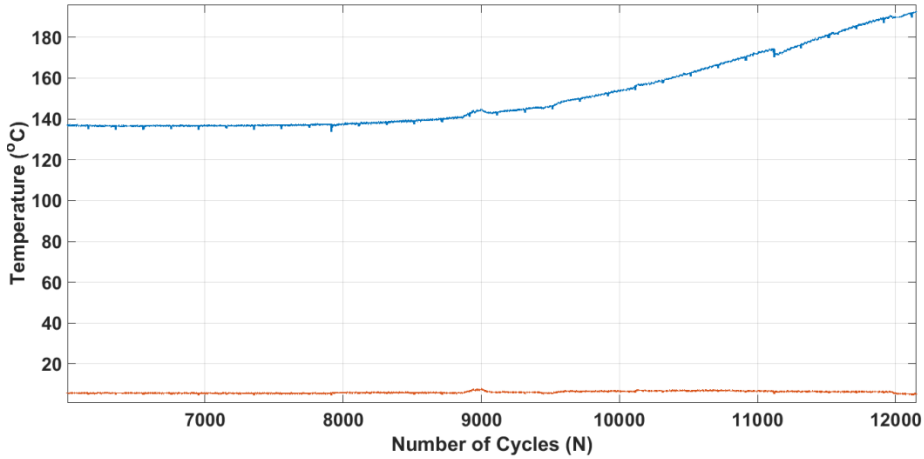

Fig 6.14: Minimum junction temperature (orange) & maximum junction temperature (blue)

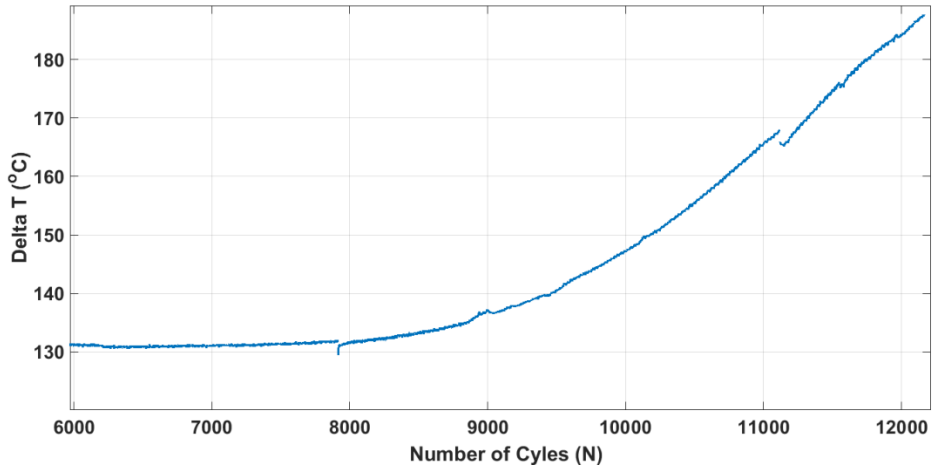

Fig 6.15: Variation of ΔT over cycles showing degradation starting after 8000 cycles

Before the cycling process started initial tests were carried out for the sake of comparison. An acoustic scan of the power device solder layer between the substrate and baseplate was carried out as can be seen in Fig 6.17(a). The differential structure function of the power device was also measured. The differential structure function was validated with the datasheet[97]. Structure function measurements were carried out at the beginning; a film was placed between the baseplate and the heatsink in one measurement, and the other measurement with no film. The differential structure function can be seen in Fig 6.16 (a). The typical junction to case temperature according to the data sheet is 0.25°C/W, this matches the differential structure function as the difference starts to occur at that thermal resistance value on the structure function.

After the degradation was observed by the acoustic scan in Fig 6.17(b) the shift in thermal resistance indicating degradation can be seen in earlier peaks indicating degradation in the solder layer in Fig 6.16 (b). This means that with this methodology the structure function of the power devices can be measured to indicate degradation in inverter setups.

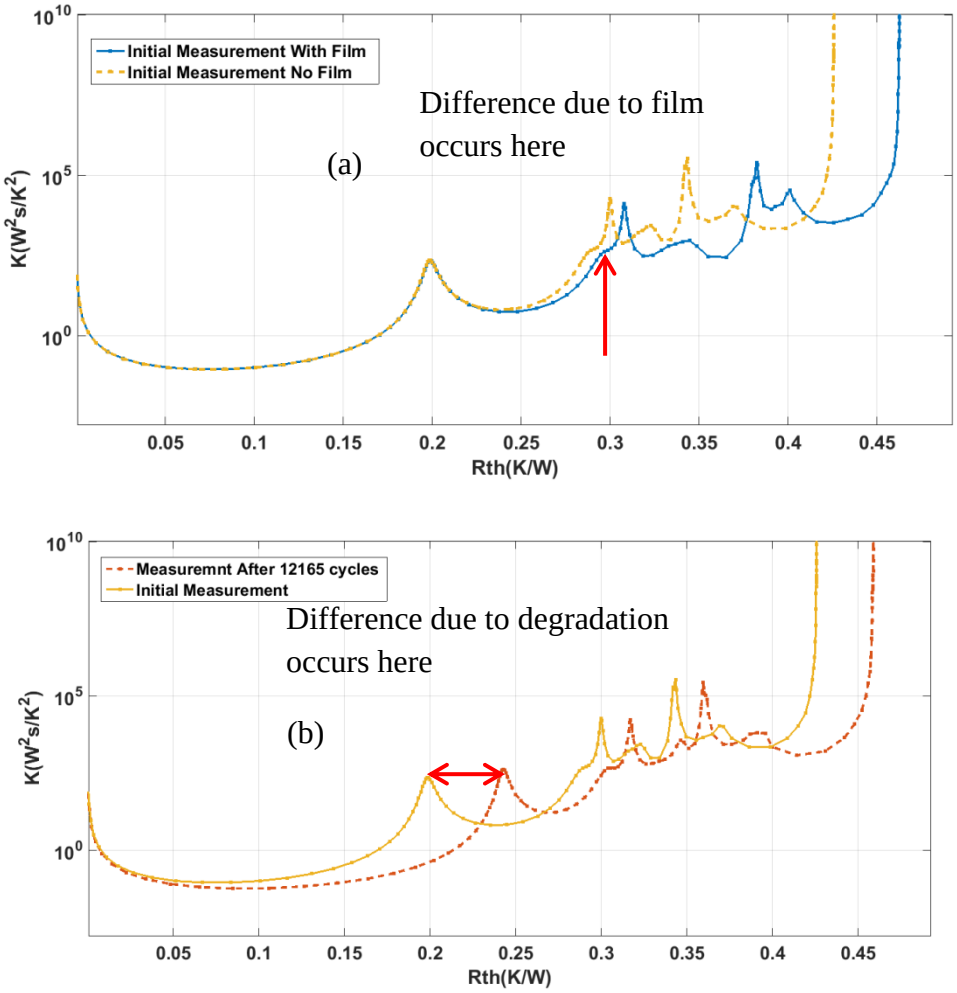

Fig 6.16: Differential structure function (a) before cycling with the same module and including a film between baseplate & heat-sink (b) comparing initial measurement with no film to measurement after cycling

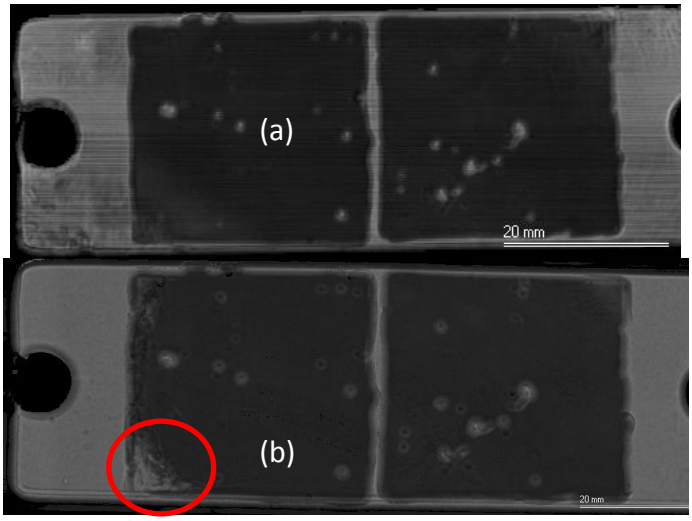

Fig 6. 17: (a) Scanning acoustic microscope at time 0 (b) after 10000 cycles

6.4 Conclusion

This chapter has shown that degradation in power modules can be measured using the structure function in both discrete samples and in an inverter set-up. The challenges in obtaining the structure function on an inverter set-up have been outlined. The methodology used in this work to overcome the challenge has been presented. The ability to detect the region where degradation occurred has also been shown by intentionally inducing degradation between the substrate and the baseplate for the discrete samples. This has also been successfully implemented on the inverter setting by measuring the difference in the solder layer between the substrate and the baseplate supported by SAM images.

Chapter 7: Conclusion

7.1 Summary

This thesis has demonstrated a technique used to check the health of modules used in induction motor drives. The power modules experience temperature swings which lead to stressing of the device especially between the substrate and the baseplate. The structure function was used for successfully tracking the magnitude and location of degradation in power modules. The structure functions are obtained by direct mathematical transformations from the heating or cooling curves. The ability to detect the region where degradation occurred has been demonstrated by intentionally inducing degradation between the substrate and the baseplate and by measuring degradation after cycling. An on-board heating technique using vector control with indirect flux rotor orientation to make the induction motor stationary while passing current through the switches in the power module in order to obtain thermal transients has been demonstrated experimentally. This has given rise to the means of checking the health of power modules regularly on-board without additional high current sources to prevent unforeseen failures during operation. As vector control is used for the heating; the existing software only needs a simple modification. The measurement circuit can also be included on the gate driver board.

7.2 Contribution

An original approach in this thesis is the implementation of a test routine (on-board) which can be carried out between operational phases of the equipment, such as in trains once a week/month in the depot for maintenance routines using vector control. The two aspects to obtaining the structure function are, heating the power device and measurement. In this thesis, the overall approach used to derive the structure function is presented. This entails the theory behind the structure function and how it can be obtained. Also, the heating methodology which makes use of vector control has been elaborated. The

amalgamation of the heating and measurement system with the challenges encountered have been presented along with the results validating the on-board measurement methodology.

7.3 Future Work

Before this method can be widely used, further research needs to be done to investigate the following aspects:

- Possibility to detect wire-bond lift off and die attach degradation
- Application to other power module technologies such as press pack modules
- Monitoring of health of antiparallel diodes
- Application to wide bandgap devices
- Other inverter topologies (multilevel inverters)

7.4 Application to Other Inverter Topologies

Multi-level converters are widely used in medium-voltage drives (MVDs) for industry (e.g., rolling mills, fans, pumps, and conveyors), marine appliances, mining, and traction [101]. The use of multi-level converters in critical applications makes degradation monitoring in these topologies very important. Recently wide-band gap devices in dc/dc converters and dc/ac inverters have been widely introduced. Various converters with different application conditions show the potential of achieving very high efficiencies with WBG devices under a wide operating range [102]. This makes WBG devices favourable for most applications, consequently making monitoring the health of the devices a very important aspect of operation. Simulations to implement the methodology in this thesis using a multi-level converter topology are carried out using an active neutral point clamped (ANPC) as a case study.

As mentioned in Chapter 6, the freewheeling current disrupts the measurement of temperature after the heating current is switched off as shown in Fig 7.1. The control scheme implemented in this thesis to ensure that measurement starts early enough only measures the solder between the substrate and the baseplate. The application of this methodology in multi-level converters provides the potential to enhance measurements and capture small time constants such as the solder layer (die-attach). For example the use of ANPC

will enable measurement that captures faster time constants due to opportunity to isolate the DUT from freewheeling current.

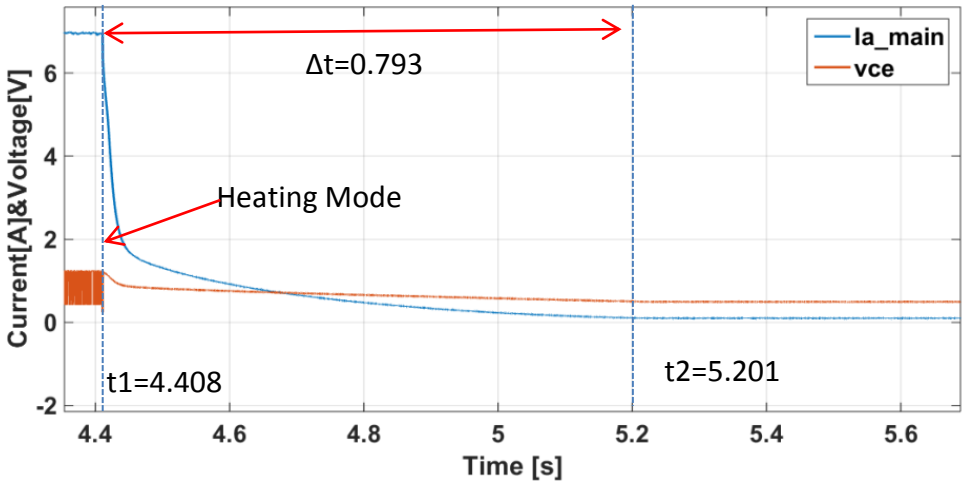

Fig 7.1: Current and Voltage (collector-emitter) of DUT

The ANPC inverter has 6 switches in a single phase as shown in Fig 7.2 which are used to obtain a 3-level output phase voltage with respect to the neutral point. Different modulation strategies exist for the ANPC. One of these modulation strategies based on the reverse conduction capability of SiC MOSFETs is shown Fig 7.3.

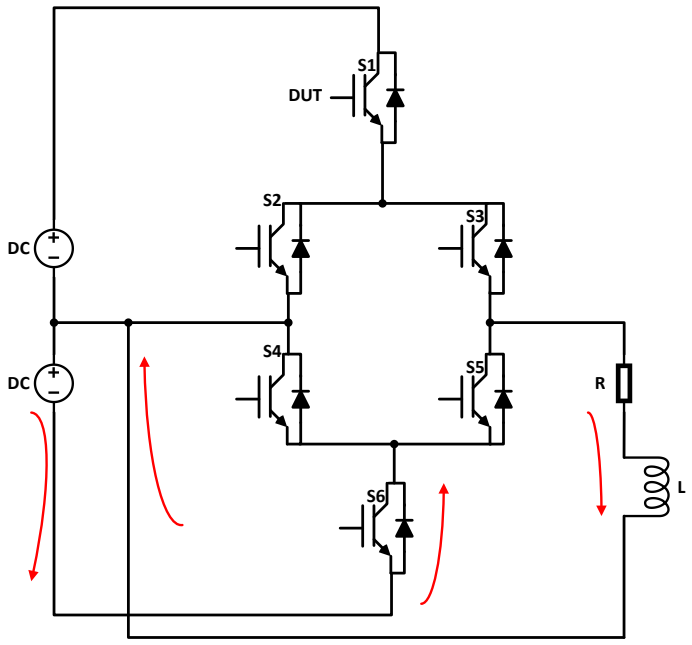

Fig 7.2: Single phase ANPC inverter

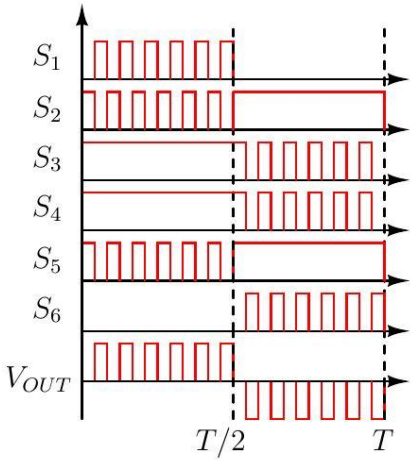

Fig 7.3: Switching Sequence and output voltage of a single phase of ANPC [103]

For the maintenance routine, the circuit is simulated in the same way the single phase converter in this thesis is operated and with the same control technique. The two switches S1, S3 are driven by the same control signal and S5, S6 are driven with the opposite signal while S2 and S4 remain completely off. Hence the ANPC operates as a single phase of a 2 level converter.

A heating current reference of 20 A is applied for 5s. After the 5s heating period all the switches were turned off with the exception of the DUT (S1). The output current is shown in Fig 7.4, with the freewheeling current flowing through the phase, after all the devices except S1 have been switched off. The freewheeling current path is illustrated in Fig 7.2 with the current flowing through the load, then the lower DC link, then the anti-parallel diodes of S6 and S5. This means that during measurement no load current flows through the DUT (S1). The current that flows through the DUT is shown in Fig 7.5. It can be seen that in the simulation the current goes to 0 instantaneously. In experiment the initiation of measurement is only limited to the device transient as opposed to the freewheeling current.

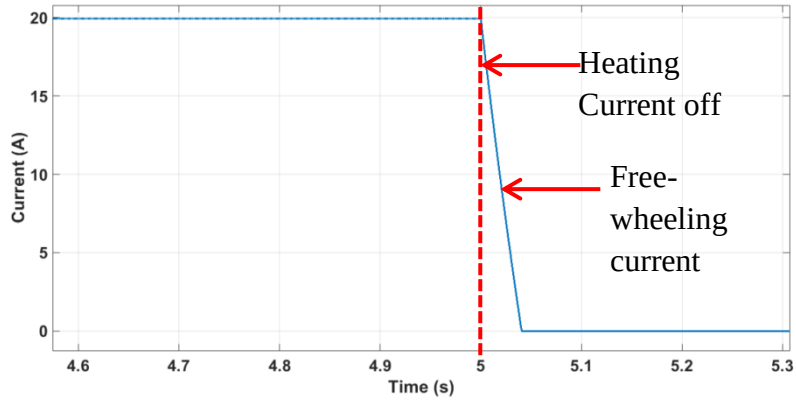

Fig 7.4: Simulation output current ANPC inverter during maintenance routine

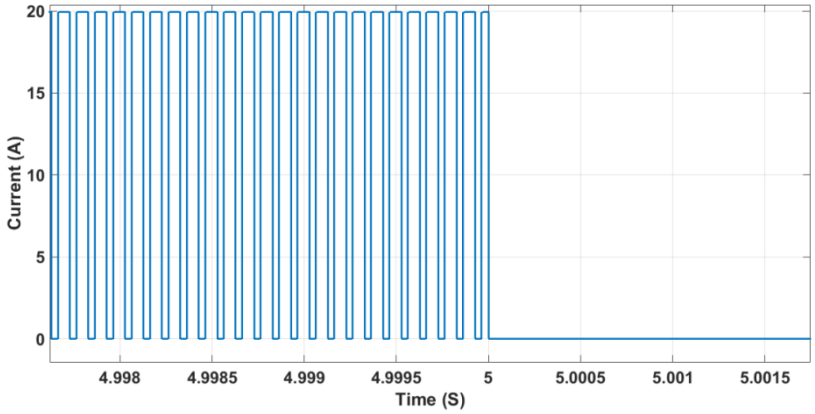

Fig 7.5: Simulation of current through DUT during maintenance routine

Application of this technique provides an opportunity to make accurate thermal characterisation of the devices used in various multilevel converters. There is also a possibility of including bond wire measurements. These can be carried out by obtaining the voltage when the high current is passed through the device as was presented in [23]. The voltage measurement is already implemented in this system; hence no added complexity is needed. The voltage drop across the bond wires is relatively insignificant compared to the voltage across the p-n junction when measuring at low currents as stated earlier. This means that a significant number of bond wires need to lift off before this phenomenon can be observed with low current measurement. If the voltage measurement at both high current and low current are utilised measuring both the wire bond lift off and the degradation in the structure becomes a possibility. This gives rise to the potential of on-board monitoring of power devices in different multilevel applications using WBG devices such as automotive, traction and aerospace.

Appendix 1

A1.1 1D Heat Conduction

The assumption is that the temperature is a function of only the x coordinate and time; that is T=T(x,t) and the conductivity λ, density ρ, and the specific heat capacity c of the solid are all constant. The principle of conservation of energy for the volume, surface area A, and thickness Δx, of Fig 1A.1 can be stated as in [26].

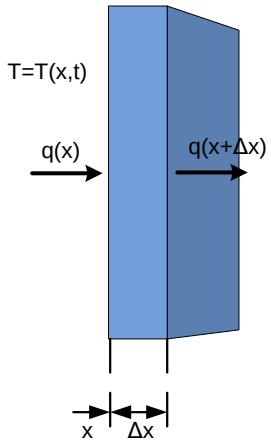

Fig 1A.1: Illustration of One Dimensional Heat Flow

$$\begin{array}{c}\text{Rate of heat conduction}\\ \text{into control volume}\\ +\\ \text{Rate of heat generation}\\ \text{inside control volume}\end{array} = \begin{array}{c}\text{Rate of heat conduction}\\ \text{out of control Volume}\\ +\\ \text{Rate of energy storage}\\ \text{inside control volume}\end{array} \qquad (1A.1)$$

The above can be expressed as:

$$-\lambda A\frac{\partial T}{\partial x}(x)+HA\Delta x=-\lambda A\frac{\partial T}{\partial x}(x+\Delta x)+\rho A\Delta x c\frac{\partial T(x+\Delta x/2,t)}{\partial t} \qquad (1A.2)$$

Dividing (2A.3) by the volume AΔx and rearranging the following is obtained:

$$\lambda\frac{\left(\frac{\partial T}{\partial x}(x+\Delta x)\right)-\left(\frac{\partial T}{\partial x}(x)\right)}{\Delta x}+H=\rho c\frac{\partial T(x+\Delta x/2,t)}{\partial t} \qquad (1A.3)$$

The first term on the left side of (1A.3) can written as

$$\frac{\partial T}{\partial x}(x+\Delta x)=\frac{\partial T}{\partial x}(x)+\frac{\partial}{\partial x}\left(\frac{\partial T}{\partial x}(x)\right)dx=\frac{\partial T}{\partial x}(x)+\frac{\partial^2 T}{\partial x^2}(x)dx \qquad (1A.4)$$

The right hand side of (1A.3) can be expanded in Taylor series centred on x.

$$\frac{\partial T}{\partial t}\left[\left(x+\frac{\Delta x}{2}\right),t\right]=\frac{\partial T}{\partial t}(x)+\frac{\partial^2 T}{\partial x \partial T}(x)\frac{\Delta x}{2}+..... \qquad (1A.5)$$

In the limit as $\Delta x \rightarrow 0$ only the first term in the Taylor series is used and the subsequent terms are ignored. Substituting the results from (1A.4) and (1A.5) in (1A.3):

$$\lambda\frac{\frac{\partial T}{\partial x}(x)+\frac{\partial^2 T}{\partial x^2}(x)dx-\left(\frac{\partial T}{\partial x}(x)\right)}{\Delta x}+H=\rho c\frac{\partial T}{\partial t}(x) \qquad (1A.6)$$

$$\lambda\frac{\partial^2 T}{\partial x^2}+H=\rho c\frac{\partial T}{\partial t} \qquad (1A.7)$$

The first term on the left hand side represents the net rate of heat conduction into the control volume per unit volume. The second term on the left side is rate of energy generation per unit volume inside the control volume. The right side represents the rate of increase in internal energy inside the control volume per unit volume[26].

Appendix 2

A2.1 Derivation of convolution form equation

The thermal transient can be written as

$$a(z) = \int_{-\infty}^{\infty} R(l)\left(1 - e^{\left(-e^{(z-1)}\right)}\right)dl \tag{2A.1}$$

Differentiating both sides with respect to z where

$$f(z,l) = R(l)\left(1 - e^{\left(-e^{z-l}\right)}\right) \tag{2A.2}$$

$$\frac{da(z)}{dz} = \frac{d}{dz}\int_{-\infty}^{\infty} f(z,l)dl \tag{2A.3}$$

Using Leibniz principle to differentiate the right hand side.

$$\frac{d}{dz}\left(\int_{-\infty}^{\infty} f(z,l)dl\right) = \left(\int_{-\infty}^{\infty} \frac{\partial}{\partial z} f(z,l)dl\right) \tag{2A.4}$$

Where

$$\frac{\partial}{\partial z} f(z,l) = \frac{\partial}{\partial z}\left(R(l) - R(l)e^{\left(-e^{z-l}\right)}\right) \tag{2A.5}$$

The chain rule is used to find the partial derivative of the exponential term

$$\frac{d\, e^{u(z)}}{dz} = \frac{d\, e^{u(z)}}{du(z)} \times \frac{du(z)}{dz} \tag{2A.6}$$

The partial derivative of (2A.5) is then

$$\frac{\partial}{\partial z} f(z,l) = R(l) \times \left(e^{-e^{(z-l)}} \times e^{z-l}\right) \tag{2A.7}$$

(2A.3) can then be written as

$$\frac{da(z)}{dz} = \int_{-\infty}^{\infty} R(l) \times W(z-l)dl \tag{2A.8}$$

Where

$$W(z-l) = \left(e^{-e^{(z-l)}} \times e^{z-l}\right) \tag{2A.9}$$

(2A.8) is a convolution type equation and can be written as

$$\frac{da(z)}{dz} = R(z) \otimes W(z) \qquad (2A.10)$$

A2.2 MATLAB code for transforming Foster network to a Cauer network

```
%----------------------------------Foster---------------------------------%

%    data from curvefitter (For 2 components. Be sure to put the number of Rs and Cs you
require)
      T1 = 0.002965;

      T2 =0.3714;


      R1 =       0.06217 ;

      R2 =        0.1379 ;


      C1 =       T1/R1 ;

      C2 =       T2/R2 ;

 %Defining 's' as a transfer function
   format long
   s=tf('s');
% foster Equation gives the z in the transfer function format

z=R1/(1+(s*R1*C1))+R2/(1+(s*R2*C2))

 %put the coefficients from Z back in A(Denominator) and B(Numerator)
 A=[0.001101
    0.3744
    1];

 B=[0.0235
```

```
    0.2001];
%--Runs until there are no coefficients left(Long division)----------
while ~isempty(A)
 format long
%gives thermal Capacitance
 ca1=A(1)/B(1);
 cth=abs(ca1)
 %Calculates the numerator of the remainder
 y1=(A(1:(end-1)))-((B(1:end)).* abs(ca1));

 %B taken from previous step to calculate resitor
 ra1=B(1)/y1(2);
 rth=abs(ra1)
 %puts zero in non existing element of array
 fox=padarray(y1,[1,0],1,'post');
%taken from z1 from element 2 to end because first element is zero

z1=(B(1:end))-( (fox(2:end)).* abs(ra1));
 %thermal resistance calculated
 %  putting back the one taken off in are=B(1:end-1);
A=fox(2:end);
B=z1(2:end);
end

% ------------------------------------------------------------------------------------------
```

A2.3 An example of Foster to Cauer Conversion

A cooling curve is used to derive the time constants below. Below we have a foster network with two thermal resistances and capacitances.

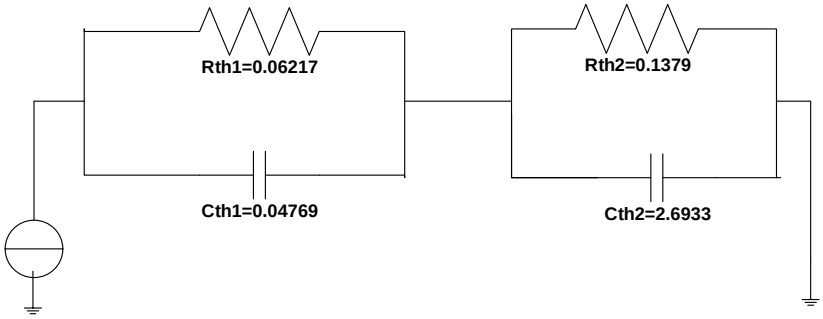

Figure 2A.1 Foster Network with RC Values

The total thermal impedance is

$$Z_{in}(s) = \frac{0.06217}{1 + s0.002965} + \frac{0.1379}{1 + s0.3714} \tag{2A.11}$$

Rearranging

$$Z_{in}(s) = \frac{s0.0235 + 0.2001}{1 + s(0.3744) + s^2(0.0011)} \tag{2A.12}$$

To obtain the thermal capacitances and the resistance for the Cauer network equation 2A.12 needs to be written in the form

$$\frac{1}{Z_i(s)} = s C_i + Y_i \tag{2A.13}$$

$$\frac{1}{Y_i(s)} = R_i + Z_{i+1} \tag{2A.14}$$

The process of polynomial long division is used. To start this process the thermal capacitance needs to be derived first therefore equation (2A.12) should be in the form of admittance.

$$\frac{1}{Z_i(s)} = Y_i(s) = \frac{s^2(0.0011) + s(0.3744) + 1}{s0.0235 + 0.2001} \tag{2A.15}$$

$$s0.0235 + 0.2001 \overline{)\; s^2(0.0011) + s(0.3744) + 1} \quad \Big| \; 0.0468s$$

$$\text{.....} - s^2(0.0011) \text{.....} s(0.0094)$$

$$\text{.....} = 0 + s(0.3650) + 1$$

$$\frac{1}{Z_i(s)} = quotient + remainder \tag{2A.16}$$

$$\frac{1}{Z_i(s)} = 0.0468s + \frac{s(0.3650) + 1}{s(0.0235) + 0.2001} \tag{2A.17}$$

Therefore from equation (2A.17)

$$C_1 = 0.0468 \text{ J/K}$$

And the remainder is equal to the admittance

$$Y_i(s) = \frac{s(0.3650)+1}{s(0.0235)+0.2001} \tag{2A.18}$$

Therefore

$$\frac{1}{Y_i(s)} = Z_i(s) = \frac{s(0.0235)+0.2001}{s(0.3650)+1} \tag{2A.19}$$

Using the same long division as above

$R_1 = 0.0644\ K/W$

And

$C_2 = 2.6898\ J/K$

$R_2 = 0.1357$ K/W

So now that the thermal resistances and capacitances have been deduced from the foster network, these values can be used in a simulation to see how much the thermal curve of the foster network differs from the Cauer network. The result is shown in figure 2A.2 the curves are have a little variation and can hardly be noticed. The green line as shown in the legend represents the Cauer network and the red line represents the Foster network. A cursor was places at certain point and the difference of 0.0274 Degrees C was obtained. This shows this is a reliable way of obtaining the cauer network from the foster network.

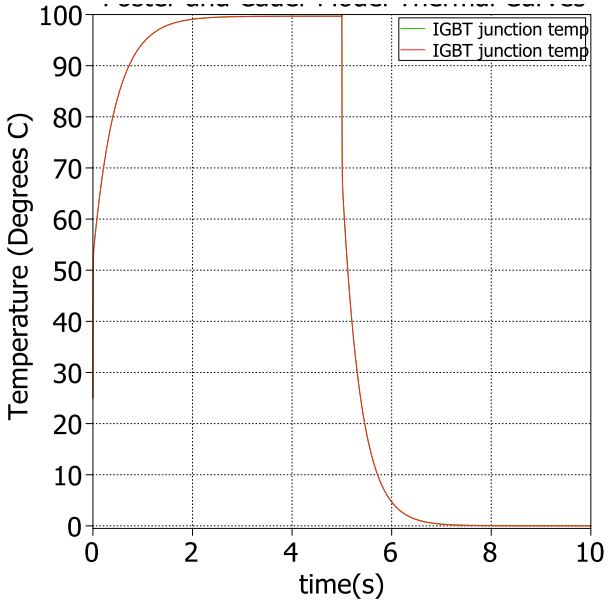

Figure 2A.2 Foster and Cauer Thermal Transients (Overlapping)

Appendix 3

A3.1 Clarke's Transformation

Space vectors can be used to express three phase components in a more convenient manner. With current voltage e.t.c

$$\vec{\imath}sum = \vec{\imath}u + \vec{\imath}v + \vec{\imath}w = iue^{j0} + ive^{j\frac{2\pi}{3}} + iwe^{j\frac{4\pi}{3}} \quad (3A.1)$$

Using Euler formula in

$$\vec{\imath}sum = \left(iu - \frac{1}{2}iv - \frac{1}{2}iw\right) + j.\left(\frac{\sqrt{3}}{2}iv - \frac{\sqrt{3}}{2}iw\right) \quad (3A.2)$$

The real and imaginary parts can be re-written as

$$i\alpha = Re(\vec{\imath}sum) = \frac{2}{3}\left(iu - \frac{1}{2}iv - \frac{1}{2}iw\right) \quad (3A.3)$$

$$i\beta = Img(\vec{\imath}sum) = \frac{2}{3}\left(0 + \frac{\sqrt{3}}{2}iv - \frac{\sqrt{3}}{2}iw\right) \quad (3A.4)$$

This is called Clarke Transformation. This transformation also known as the αβ coordinate system is in the following figure. In Fig 3A.1 the α-axis coincides with the u-vector and the β-axisis perpendicular to the α-axis. For an electric machine this is fixed on the stator.

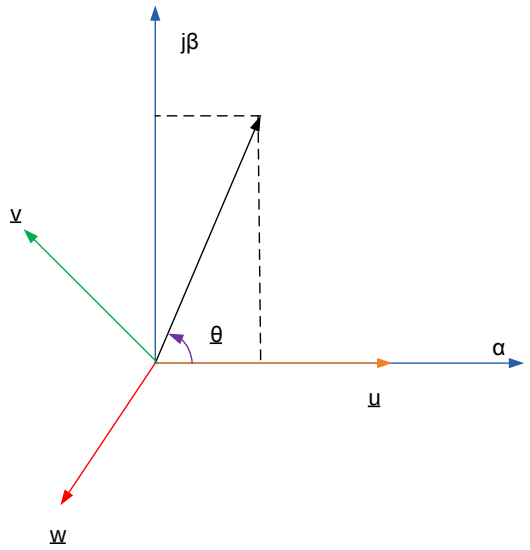

Fig 3A.1: Space vector in αβ-coordinate system

A3.2 Principles of an Induction Motor

A three phase motor has a stator and a rotor. The stator coils are physically spaced 120 degrees from each other. The rotor is inserted in the spacing between the stator. From Faraday's law any change in the magnetic environment of a coil of a wire will cause a voltage (EMF) to be "induced" in the coil. No matter how the change is produced, the voltage will be generated. The change could be produced by changing the magnetic field strength, moving a magnet toward or away from the coil, rotating the coil relative to the magnet and so forth.

In a three system the sinusoids develop a changing pattern in the magnetic field which creates a rotating magnetic field. For a motor to function there needs to be a rotating magnetic field. The rotating magnetic field induces EMF on the rotor which produces a current of its own. This current then creates its own magnetic field, which interacts with that of the stator to produce torque.

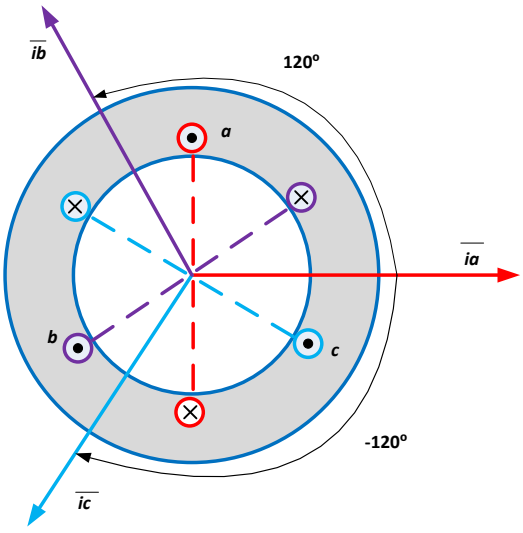

Fig 3A.2: Windings in an induction motor

Three stator windings are organized with 120° angle difference in the physical space between each other as seen in Fig 3A.2. The arrowed lines define the directions of the currents in the windings in a form of vector. The three currents are named as $\overline{i_a}$, $\overline{i_b}$ and $\overline{i_c}$. The vector magnitudes are equal to the

current magnitudes respectively, with the dotted lines indicating the direction of the corresponding magnetic field. This configuration changes direction and magnitude with time. The sum of vector currents can be considered as:

$$\overline{i_{sum}} = \overline{i_a} + \overline{i_b} + \overline{i_c} = i_a e^{j0} + i_b e^{j\frac{2\pi}{3}} + i_c e^{j\frac{4\pi}{3}} \tag{3A.5}$$

Using Euler formula in

$$\overline{i_{sum}} = \overline{i_a} + \overline{i_b} + \overline{i_c} = i_a e^{j0} + i_b e^{j\frac{2\pi}{3}} + i_c e^{j\frac{4\pi}{3}} \tag{3A.6}$$

$$\overline{i_{sum}} = \left(i_a - \frac{1}{2} i_b - \frac{1}{2} i_c \right) + j\left(\frac{\sqrt{3}}{2} i_b - \frac{\sqrt{3}}{2} i_c \right) \tag{3A.7}$$

The transformation of space vector is directly derived from the sum of the vectors. The αβ based coordinate system is obtained from (3A.7). Further information on this can be found in section A3.1. Based on the equation above, a coefficient 2/3 is applied to $\overline{i_{sum}}$, in order to keep constant magnitude of the vectors during the transformation. The space vector transformation is thus defined below

$$\overline{i_s} = \frac{2}{3}\overline{i_{sum}} = \frac{2}{3}\left(i_a + a * i_b + a^2 * i_c\right) = i_s e^{j\theta} \tag{3A.8}$$

According to the electric machine theory, rotating magnetic fields will be generated in the stator if sinusoidal currents flow in the windings. In this section it will be shown that this is true using space vector. The currents in the windings at time, *t*, could be presented with the following equations:

$$i_a = I_o \cos\left(\omega t + \varphi_o\right) \tag{3A.9}$$

$$i_b = I_o \cos\left(\omega t + \varphi_o - \frac{2\pi}{3} \right) \tag{3A.10}$$

$$i_c = I_o \cos\left(\omega t + \varphi_o + \frac{2\pi}{3} \right) \tag{3A.11}$$

$$\overline{i_{sum}} = \frac{2}{3}\left(\overline{i_a} + \overline{i_b} + \overline{i_c}\right) = \frac{2}{3} I_o \left(\cos(\omega t + \varphi_o) + j \sin(\omega t + \varphi_o)\right) = \frac{2}{3} I_o e^{j(\omega t + \varphi_o)}$$

(3A.12)

It can be seen from (3A.12) that the current space vector has constant amplitude and rotates at an angular speed ω which is shown in Fig.3A.3. Ampere's law states that the magnetic field in space around an electric current is proportional to the electric current which serves as its source. Since the magnetic field is directly generated with currents, it is obvious that the magnetic field in the stator also has a constant magnitude and a constant angular speed, which is equal to ω.

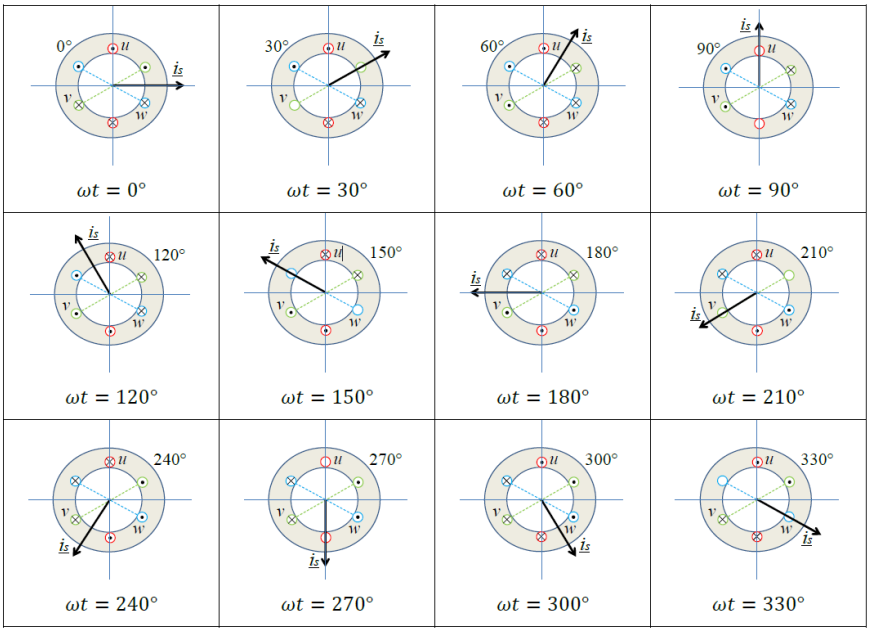

Fig 3A.3: Chart showing the rotation of the current space vector [104]

A3.3 Park's Transformation

Sometimes it is more convenient to analyze the machine in a rotation coordinate system as shown in Fig 3A.3. The dq coordinate system rotates around a common coordinate origin which is the same u coordinate used in the αβ coordinate system. At a point in time the d-axis has an angular relativity with to the stationary u-vector.

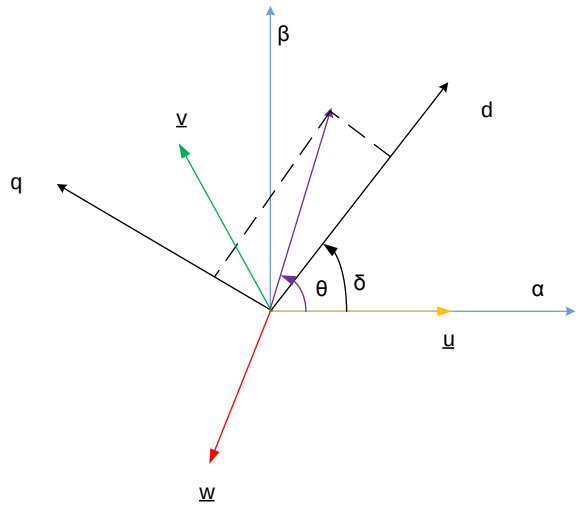

Fig 3A.4: Space vector in ***dq***-coordinate system

The dq expression of the space vector is derivable from the Clarke's transformation:

$$id = i\alpha * cos\delta + i\beta * sin\delta \quad (3A.13)$$

$$iq = -i\alpha * sin\delta + i\beta * cos\delta \quad (3A.14)$$

Alternatively, the d and the q components of the space vector could be directly derived from the space vector definition. If the d-axis has an angle δ compared to the fixed u-axis at a certain time, a rotation operator $e^{-j\delta}$ will transform the space vector from the fixed coordinate system in the dq-system as

$$\vec{\imath}sum, dq = \frac{2}{3}\left(iu + ive^{\frac{j2\pi}{3}} + iwe^{\frac{-j2\pi}{3}}\right) * e^{-j\delta} \quad (3A.15)$$

Using Euler's formula

$$Re(\vec{\imath}sum, dq) = i\alpha * cos\delta + i\beta * sin\delta = id \quad (3A.16)$$

$$Im(\vec{\imath}sum, dq) = -i\alpha * sin\delta + i\beta * cos\delta = iq \quad (3A.17)$$

A3.4 Indirect rotor flux orientation

The angle can be calculated by the integral of the electric speed. The process used is shown below

$$\lambda = \int \omega e \, dt = \int \omega r + \omega sl \, dt = \int (\omega r + \frac{isq}{\tau r \ imrd}) \, dt \qquad (3A.18)$$

where

$$\frac{Lr}{Rr} = \tau r \qquad (3A.19)$$

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