High Power Modular Converters for Grid Interface Applications

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Abstract

Scientists at European Organization for Nuclear Research (CERN) are currently conducting feasibility studies for the Compact linear collider (CLIC); their proposed next experimental setup for gathering information on the fundamental particles of matter. This experiment will involve the simultaneous pulsing of 1300 klystron modulators to produce a 140 μs, 39 GW pulse with a 50 Hz repetition rate. This proposal presents many demands for the connected power system as an effort is made to "hide" this pulse from the local distribution network - instead drawing only the constant average power of approximately 300 MW. This challenge is considered in this work.

In order to understand the optimal approach both the power system architectures and power electronics interfaces must be considered simultaneously. An approach to the optimisation of the power system architecture is described in this thesis. It is clear from this exercise that the optimum power converter topology for the interface between the electricity distribution network and the klystron modulators is the Modular Multilevel Converter (MMC). This converter is mainly used in modern HVDC transmission circuits as a result of its high efficiency and ability to produce high quality AC waveforms.

Pulsing of the klystron modulators does however create further challenges for the inner control loops of an MMC. The placement of the pulse can create imbalances in the DC capacitors of the MMC submodules which may result in tripping of the converter if not corrected. This thesis proposes three arm balancing solutions to be applied together with the decoupled AC and DC side controller designed for the specified application.

These proposed solutions to the aforementioned problems are successfully validated using simulation work in PLECS and using data from a laboratory scale prototype of one of the MMC interface power converters.

To my parents

- whose love travels thousands of miles -

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List of Terms

Abbreviations

CERN - Conseil Europeen pour la Recherche Nucleaire

CLIC - Compact Linear Collider

RF - Radio Frequency

EDF - Electricite de France

MMC - Modular Multilevel Converter

NPC - Neutral-Point Clamped

CHB - Cascaded H-Bridge

FC - Flying Capacitor

DCC - Diode-Clamped Converter

VSC - Voltage Source Converter

HVDC - High Voltage Direct Current

LCC - Line-Commutated Converters

XLPE - Cross-Linked Polyethylene

EMI - Electromagnetic Interference

STATCOM - Static Synchronous Compensator

AF - Active Filter

FACTS - Flexible AC Transmission Systems

UNIFLEX-PM - Universal Flexible Power Management system

CMC - Cascaded Matrix Converter

ANPC - Active Neutral-Point Clamped

MLC^2 - Multilevel-Clamped Multilevel Converter

MMSPC - Modular Multilevel Series Parallel Converter

AAC - Alternate Arm Converter

PH-M2C - Parallel Hybrid Modular Multilevel Converter

LV - Low Voltage

MV - Medium Voltage

HV - High Voltage

SVC - Static VAR Compensator

LMV - Lower Medium Voltage

CSA - Cross Section Area

TE - Top Event

BE - Basic Event

MCS - Minimum Cut Set

VDE - Verband der Elektrotechnik, Elektronik und Informationstechnik

ESR - Equivalent Series Resistance

SHE - Selective Harmonic Elimination

NLC - Nearest Level Control

SVM - Space Vector Modulation

PWM - Pulse Width Modulation

PD - Phase Disposition

POD - Phase Opposite Disposition

APOD - Alternate Phase Opposite Disposition

PLL - Phase Locked Loop

PCC - Point of Common Coupling

DDSRF - Decoupled Double Synchronous Reference Frame

FLL - Frequency Locked Loop

DSOGI - Decoupled Second-Order Generalised Integrator

ISR - Interrupt Service Routine

Nomenclature

V_{DC}, v_{DC} - Converter DC voltage mean and instantaneous value

ΔV, ΔV^{max} - DC voltage droop and its maximum value

P_{peak} - Klystron modulator peak power

T_{pulse} - Pulse duration

f_{rep} - Pulse repetition frequency

T_{rep} - Pulse repetition period

v_{s_AC} - Grid RMS line to line voltage

k_{AC} - Converter DC to AC voltage ratio

P_{rated}, $P_{nominal}$ - Power system component rated and nominal power

n - Number of power system components on a common bus bar

U_{fault}, U_{nom} - Equivalent and nominal voltage at the fault location

$Z_{0,1,2}$ - Impedance towards the grid: 0 - zero, 1- positive, 2 - negative sequence

$I_K^{''}$ - Sub-transient fault current

P_{top} - Probability of the top event

P_{MCS} - Probability of the MCS

E_{stored} - Energy stored in all cell capacitors

P_{rat} - Converter rated power

E_{arm} - Energy stored in one arm inductor

L_{arm} - Arm inductance

i_{DC}, I_{DC} - Converter DC current instantaneous and mean value

$k_{1,2}$ - Coefficients for the energy stored in the converter arm inductors

C_{DC} - DC link capacitance

E_{DC} - The energy stored in the DC link capacitors

N - Number of cells per MMC arm

$v_{s\_A,B,C}$ - Grid/source voltage of the phase A, B or C

$i_{A,B,C}$ - Converter and grid current of the phase A, B or C

$v_{A,B,C}$ - Converter AC voltage of the phase A, B or C

C_{cell} - Cell capacitance

L_{ph} - Phase inductance

$i_{up\_A,B,C}$ - Upper arm chain-link current of phase A, B or C

$i_{lo_A,B,C}$ - Lower arm chain-link current of phase A, B or C

$v_{up\_A,B,C}$, ${v_{up\_A,B,C}}^{ref}$ - Upper arm chain-link voltage and its reference of phase A, B or C

$v_{lo\_A,B,C}$, ${v_{lo\_A,B,C}}^{ref}$ - Lower arm chain-link voltage and its reference of phase A, B or C

$v_{Cup\_A,B,Ci}$ - Capacitor voltage of i^{th} cell in the upper arm of phase A, B or C

$v_{Clo\_A,B,Ci}$ - Capacitor voltage of i^{th} cell in the lower arm of phase A, B or C

$i_{circ\_A,B,C}$, ${i_{circ\_A,B,C}}^{ref}$ - Circulating current and its reference of phase A, B or C

${v_{DC}}^{+}$, ${v_{DC}}^{-}$ - DC link positive and negative voltage potential

$v_{AC\_A,B,C}$, ${v_{AC\_A,B,C}}^{ref}$ - AC part of the arm voltage and its reference of phase A, B or C

$v_{DC\_A,B,C}$, ${v_{DC\_A,B,C}}^{ref}$ - DC part of the arm voltage and its reference of phase A, B or C

V_{sm} - Grid voltage amplitude

I_m - Phase current amplitude

ω - Grid radial frequency

f - Grid frequency

$p_{s\_A,B,C}$, $P_{s\_A,B,C}$ - Grid/source instantaneous and average power of the phase A, B or C

ϕ_i - Phase shift between grid voltage and phase current vector

ϕ_v - Phase shift between grid voltage and converter AC voltage vector

V_m - Converter voltage amplitude

p_{AC}, P_{AC} - Overall grid AC side instantaneous and average (active) power

Q_{AC} - Overall grid AC side reactive power

p_{DC}, P_{DC} - Converter DC side instantaneous and average power

v_C, V_C - Average cell capacitor voltage in a chainlink and its nominal value

E_{cl} - Overall energy of a chainlink

P_{cl} - Average chainlink power

$p_{up\_A,B,C}$, $P_{up\_A,B,C}$ - Upper arm instantaneous and average power

$p_{lo\_A,B,C}$, $P_{lo\_A,B,C}$ - Lower arm instantaneous and average power

EP - Capacitance constant

L_{arm_res} - Resonance value of arm inductance

α - Fault DC current rise rate

θ - Phase angle of the grid voltages

$v_{s\_\alpha,\beta}$ - Grid voltage α or β component

$i_{\alpha,\beta}$ - Phase current α or β component

$v_{AC\_\alpha,\beta}$ - AC part of the arm (converter) voltage α or β component

$v_{s\_d,q}$ - Grid voltage d or q component

$i_{d,q}$, ${i_{d,q}}^{ref}$ - Phase current d or q component and its reference

L_{eq} - Equivalent phase inductor

$v_{AC\_d,q}$ - AC part of the arm (converter) voltage d or q component

τ_i - Time constant of d, q current controller

k_{dq_p}, k_{dq_i} - Proportional and integral gain of the d, q current controller

τ_{i_circ} - Time constant of circulating current controllers

k_{circ_p}, k_{circ_i} - Proportional and integral gain of circulating current controllers

i_{load} - Load current

v_{tot}, V_{tot}, ${V_{tot}}^{ref}$ - Sum of all cell capacitor voltages, its average value and reference

$v_{tot\_A,B,C}$, $V_{tot\_A,B,C}$, ${V_{tot\_A,B,C}}^{ref}$ - Sum of phase A, B or C cell capacitor voltages, its average value and reference

$P_{A,B,C}$ - Power added to the phase A, B or C

$\Delta I_{circ\_A,B,C}$ - Phase balancing correction to the circulating current reference of phase A, B or C

$\Delta P_{arm\_A,B,C}$ - Difference between arm powers of phase A, B or C

$I_{circ50\_A,B,C}$ - Circulating current 50 Hz component amplitude of phase A, B or C

$DEN_{A,B,C}$ - Ratio describing how the circulating current amplitude (or x parameter) affects the arm powers difference of phase A, B or C

v_{DC50}, V_{DC50} - DC voltage 50 Hz component ripple and its amplitude

ϕ_{DC50} - DC voltage 50 Hz component ripple angle

$\phi_{circ50\_A,B,C}$ - Circulating current 50 Hz component angle

$NUM_{A,B,C}$ - The amount of imbalance between arm powers of phase A, B or C

$x_{A,B,C}$ - Parameter x for phase A, B or C

Z_{arm} - Equivalent arm impedance amplitude

$\Delta\phi_{circ50}$ - Equivalent arm impedance angle

I_{peak} - Peak load current

T_s - Sampling time

f_s - Sampling/switching frequency

L_{load} - Load inductance

C_{load} - Load capacitance

R_{load} - Load resistance

v_{out} - Output load voltage

λ - Load dumping factor

R_M - Burden resistor

T - Grid period

I_{load50} - Load current 50 Hz component amplitude

I_{DC50} - DC current 50 Hz component amplitude

ϕ_{load50} - Load current 50 Hz component angle

ϕ_{IDC50} - DC current 50 Hz component angle

t_{start} - Time when the pulse starts with respect to the phase A grid voltage positive gradient zero crossing

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Chapter 1

Introduction

1.1 Motivation for the research project

Scientists at the European Organization for Nuclear Research (french: Conseil Europeen pour la Recherche Nucleaire, CERN) are aiming to achieve higher energy particle collisions in order to produce the basic constituents of matter - the fundamental particles. This requires building high-luminosity colliders that usually process very high input powers in order to achieve the required centre-off-mass energy collisions. Processing high powers demands very efficient, high availability power electronics. In addition, acceleration cavities often require pulsed power sources, and the grid interface power electronics in that case ideally acts as a firewall, blocking the effect of the pulsed operation from reaching and impacting the electricity network.

1.1.1 Compact linear collider

The Compact linear collider (CLIC) is a high energy linear accelerator under feasibility study at CERN [3]. It is aimed for high-luminosity electron-positron collisions reaching the centre-of-mass energy of 3 TeV. Achieving high collision energy requires

high acceleration gradients, that are in the case of CLIC provided by a two-beam acceleration principle [3, 4]. This principle requires a drive beam that runs through the power extraction and transfer structures, producing high radio frequency (RF) power pulses used for the main beam acceleration. The drive beam is usually accelerated in a traditional way, i.e. by klystrons, reaching the energies of a couple of GeV. The initial layout of the CLIC is presented in Fig. 1.1. In order to reach the energy of 3 TeV two main beams are placed in approximately 50 km long tunnel, while two drive beams are required for their acceleration. Drive beams are 2 - 2.5 km long and their parallel placement gives an opportunity to place the klystrons used for acceleration of the both beams along 2 - 2.5 km, as suggested in [5].

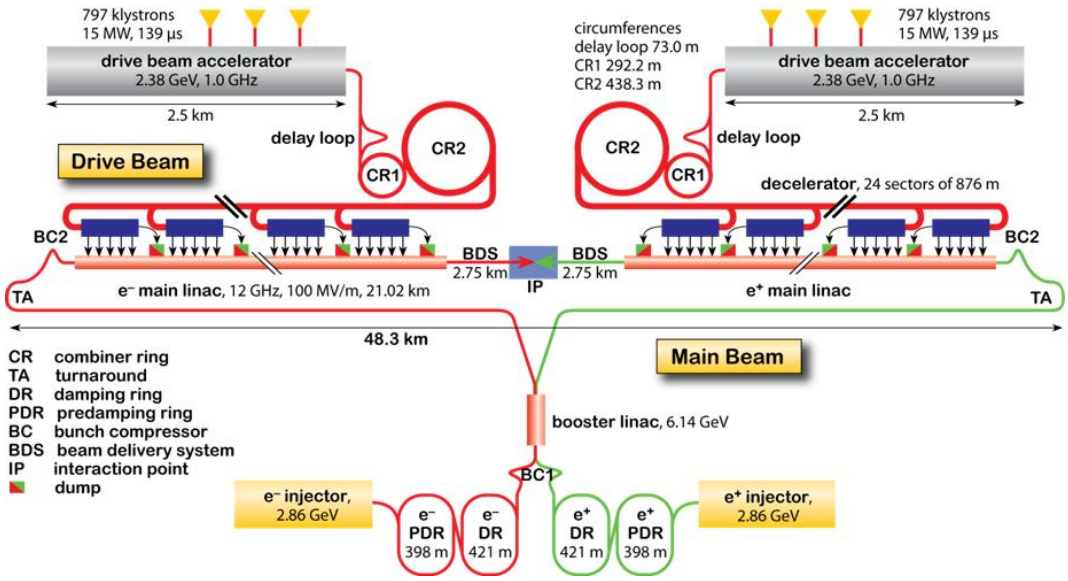


Figure 1.1: Initial CLIC layout overview aimed for 3 TeV centre-of-mass energy. The figure is taken from [1].

Klystrons are the most efficient linear acceleration tubes, using DC voltage to accelerate electrons that are modulated by an RF sinusoidal signal [6]. In order to reduce the power consumption, klystrons aimed for the drive beam acceleration are operated with a pulsed supply instead of the DC voltage [7]. Therefore, the drive beam klystrons require short, high voltage pulses, with the very tight specifications on the

pulse quality (flat top stability, rise and fall times, etc.) as given in [4]. The drive beams acceleration power is therefore pulsed in nature, with a 39 GW peak power for 140 μs of pulse length and a repetition rate of 50 Hz [4].

Initially, as presented in Fig. 1.1, approximately 1600 klystrons were required to accelerate both drive beams. During the scope of this research, the klystron supply voltage was re-optimised and new pulse parameters [8] were obtained. The new parameters indicate the peak pulse power of nearly 29 MW per klystron, which reduced the required number of klystrons to approximately 13 hundred in total.

Klystron modulators are used to produce a voltage pulse to be applied at each klystron. In the CLIC application the output pulse voltage is approximately 180 kV. The input modulator voltage is usually in the medium voltage range (1-35 kV), requiring a modulator ability to step-up voltage. In [4] various modulator topologies are considered, but considering the pulse rise and fall times, as well as the quality of the flat top, the solutions with a pulsed transformer are the most preferable. This topology comprises a capacitor bank which is discharged through a high voltage pulse transformer via the use of a solid state switch [4].

1.1.2 Requirements for the grid interface to the klystron modulators

The grid interface of klystron modulators should recharge the capacitor banks between pulses and ensure that a constant average power of approximately 280 MW is drawn from the grid despite the pulsed nature of the klystron modulators. The grid interface (charger) to approximately 1300 klystron modulators is presented in Fig. 1.2. The expected grid voltage, capacitors bank voltage v_{DC} and the modulator output voltage for the system presented in Fig. 1.2 are shown in Fig. 1.3.

The klystron modulators draw a short high current pulse when the solid state switch is closed and the capacitor voltage is transferred to the primary winding of the pulse

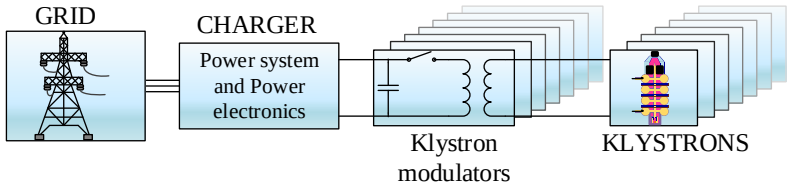


Figure 1.2: Grid interface to the drive beam klystron modulators.

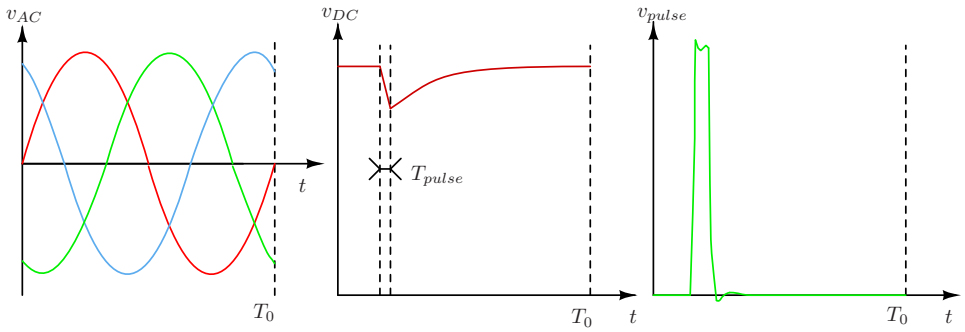


Figure 1.3: From left to right: the expected grid voltage, DC voltage and the final modulator voltage.

transformer. The pulse current causes a voltage droop on the main capacitor bank voltage v_{DC}, which requires a compensation to avoid the presence of the voltage droop on the transformer secondary side. Without this compensation the droop would have an adverse effect on the output pulse flat top stability. The voltage droop compensation is carried out on the primary side of the transformer, by a high bandwidth active bouncer [9] capable of compensating a maximum voltage droop of 1 kV which is between 5 % and 20 % of the nominal DC voltage [4]. The parameters of the klystron modulator are given in Table 1.1. The repetition rate of the pulses indicates the presence of the 50 Hz component in the DC voltage ripple.

CERN uses the French electricity provider (french: Electricite de France, EDF) grid connection at the transmission voltage level with the grid parameters given in Table 1.2. The grid connection is approximately 500 m away from the klystron modulators,

Table 1.1: Parameters of klystron modulators

Parameter	**Label**	**Value**
Nominal DC voltage [kV]	V_{DC}	5 - 20
Maximum voltage droop [kV]	ΔV^{max}	1
Peak pulsed power [MW]	P_{peak}	29
Pulse duration [μs]	T_{pulse}	140
Repetition rate [Hz]	f_{rep}	50

distributed along 2 - 2.5 km. The design of a dedicated power system is required to meet the connection requirements at both grid and modulator side, while maximising the overal efficiency and availability [4, 5].

Achieving low AC power fluctuation (bellow 2 %, Table 1.2) is one of the biggest challenges for the power electronics used as a grid interface to the klystron modulators, considering their synchronous pulsation with the total peak power of nearly 39 GW.

Table 1.2: Parameters of the grid (EDF)

Parameter	**Value**
Grid voltage [kV]	400
Available power [MW]	400
Maximum fault power [MVA]	14000
Resistance/reactance ratio	0.07
Zero sequence impedance ratio	0.822
Power fluctuation [%]	<2

The voltage droop (at the capacitor bank) is limited by selection of the appropriate capacitance of the capacitor bank, which is already attenuating power fluctuation at the DC side by 80-90 % [5]. Grid interface power electronics used as a charger of the capacitor bank should be able to further suppress pulsed effects in order to achieve low AC power fluctuation. Considering the voltage ratings and the requirement for high efficiency and good AC waveform quality, multilevel topologies are foreseen as being more suitable than the standard 2-level topologies [5, 7].

1.2 Project objectives

Based on the presented challenges from the previous section, the objectives of the research work addressed in this thesis are defined. The main project objectives are following:

- Review existing multilevel topologies and discuss their benefits and drawbacks for the CLIC application. This includes both AC/DC and DC/DC topologies.
- Analyse different power system design architectures in order to meet all the requirements and design practices at CERN. The selection of the power system layout is coupled with the converter topology selection.
- Perform an optimisation of the power system in order to select the most suitable voltage levels, as well as the number of converters and their power and voltage ratings.
- Identify all the possible effects of the klystron modulators, on the selected converter/power system topology.
- Design a closed-loop control strategy to achieve low AC power fluctuation despite the pulsation present on the modulator side, as well as regulating the DC voltage.
- Validate proposed control algorithms on the selected converter topology through simulation modelling.
- Build an experimental prototype including the converter and a pulsed DC load capable of emulating the klystron modulators.
- Verify the proposed control algorithms experimentally.

1.3 Organisation of the thesis

The second chapter presents the literature review of the multilevel topologies, since they are recognised as the most suitable for the CLIC application. The chapter discusses the features of the most commonly used topologies for different applications.

The following chapter presents the challenges for the utility interface, by discussing all the power system structures considered with regard to converter topologies, voltage levels and number of required stages of power conversion. The single-stage power system architecture, utilising only AC/DC power converters and step down transformers is recognised as the suitable architecture, given that the AC power fluctuation can be minimised regardless of the klystron modulator features. The most suitable topology is a Modular Multilevel Converter (MMC), and the further analysis is based on this topology. The chapter presents the power system optimisation results, by finding the most suitable converter voltage and power ratings that minimise the overal system cost and losses.

Chapter 4 highlights the features of the MMC topology. It presents the review of the modulation methods for multilevel topologies, with the focus of their application on an MMC. The energy stored in the converter is distributed in the converter arms, that are used for multilevel waveform generation. Having such a structure, provides an ability to decouple the converter AC and DC sides which is an important characteristics for the CLIC application.

In Chapter 5, the control strategy for a grid connected MMC with a pulsed DC load emulating the klystron modulators, is developed. The pulsed DC load with a repetition rate of 50 Hz is a constant source of imbalances between converter arms, making the requirement for arm balancing controllers. The chapter presents three arm balancing methods, one that was already reported in the literature and two developed during this research.

The following chapter validates the proposed control algorithms from Chapter 5

through simulation modelling. The ability to achieve low AC power fluctuation is verified for all proposed arm balancing methods, and the success of those methods is discussed for various pulse positions (with respect to the grid voltages).

Chapter 7 presents laboratory scale experimental prototype, including the 9-level 7 kV MMC and pulsed load emulation circuit drawing 3.3 kA short current pulse. The chapter also discusses the implementation issues related to the control platform, data acquisition and switching between different modes of operation (precharge, grid synchronisation, pulsed load conditions).

In Chapter 8, experimentally obtained results are presented. All the concepts proposed in Chapter 5 and validated by numerical simulations in Chapter 6, are experimentally verified on the small scale prototype.

Finally, Chapter 9 gives the conclusions on the presented work and summarises the contributions of this thesis.

Chapter 2

Multilevel converters - Literature review

2.1 Introduction

In recent years, multilevel converters have dominated the market of high voltage, high power converters due to the various benefits they offer with respect to traditional two-level topologies [10, 11, 12]. The main principle of the multilevel converters is based on the careful insertion of additional voltage levels in the AC voltage signal, which naturally leads to better AC waveform quality [10, 13]. The first multilevel topologies were patented in 1971, as a stepped-wave converter circuit [14] and a transformer-less power supply [15]. Shortly after, a neutral-point clamped (NPC) converter was proposed [16]. In the following years many publications about these three topologies were made, leading to their current forms and names. The stepped-wave converter is currently known as a Cascaded H-bridge (CHB) converter [17]. The transformer-less power supply has evolved into flying capacitor (FC) converter [18]. Finally, the 3-level NPC converter has later evolved to a diode-clamped converter (DCC) which can be extended to have an increased number of levels. These three topologies are nowadays considered as classic multilevel topologies [11]. There are

various comparisons of the classic multilevel topologies based on different features and applications [19, 20, 21, 22].

Despite the early discovery, their application was possible only after they were studied in detail [23] and after other technology advances were made, such as a development of IGBTs [24], increased computational power of the controller units, etc. The application of the multilevel topologies has advanced with the use of the voltage source converters (VSCs) in high voltage direct current (HVDC) applications [13].

The development of HVDC technology is presented in [13, 25]. The initial HVDC stations were built using two-level current source line-commutated converters (LCC), which evolved with advances in controlled semiconductors [26, 27]. Today LCC is considered a mature classic HVDC topology utilising series connection of the switches (thyristor valves) or multiple three-phase converters (6-pulse converters) in order to build-up higher DC link voltages. This include 12-pulse converters and series connection of 12-pulse converter groups [25]. Such topologies require fairly expensive and bulky transformers, AC filters and power factor correction circuits [13, 28]. The development of voltage source converters brought benefits of using fully controlled semiconductors and independent active and reactive power control. Additionally, in the case of VSCs the change of the power flow direction does not require the change of the polarity in the DC voltage, which is the case with the current source converters, enabling the use of modern infrastructure such as cross-linked polyethylene (XLPE) insulated cables [13]. However, usage of two-level VSC in HVDC system still requires large and expensive filters. In addition, the series connection of the switches (IGBT valves) is required in order to reach high voltage levels, which together with high switching frequencies has an adverse effect on converter efficiency [28]. The invention of the modular multilevel converter initially proposed in [29] has made a breakthrough in modern VSC based HVDC systems [30, 31]. This is due to the ability to extend it to an arbitrary number of levels by simply adding identical converter cells.

The demand of high power and high voltage converters, requiring high efficiency and power density, initiated two pathways for the development of modern power

conversion [10]. One is improvement of the switches, in terms of the voltage and current ratings and reduction of the switching and conduction losses. The other direction is towards new topologies, such as multilevel topologies, primarily based on low switching frequency and the ability to reach high voltage and power levels with traditional switches.

The increase in the number of voltage levels, provides the ability to create more sinusoidal waveforms that can be synthesized with lower switching frequencies. This reduces filtering requirements [10], which in the case of LCC HVDC systems have the biggest footprint and most significant cost [13, 28]. Additionally, reduction of the switching frequency lowers the switching losses and therefore increases the converter efficiency. Having multiple intermediate voltage levels, rather than DC bus voltage levels only, reduces the voltage stress on the switches $\frac{dv}{dt}$, reducing the problems related to electromagnetic interference (EMI) [13]. Multilevel topologies also offer a redundancy in switching states generating the same voltage level, allowing application of different control methods, usually having a goal to control the voltages and current distribution on the passive components, generally present in multilevel topologies [10, 32]. Additionally, a redundancy in some topologies provides a possibility to develop a fault tolerant operation since the malfunctioning device can be bypassed [11].

2.2 Multilevel topologies

The DCC and FC converter theoretically can be extended to the any number of levels, but practically this includes an increase in control and design complexity. These two topologies are also referred to as monolithic [13], since the extension to the higher voltage levels requires a series connection of switches or diodes to provide high blocking voltage capabilities. In the case of the NPC converter, the extension to higher number of levels (DCC) includes balancing of more DC link capacitor voltages. Additionally, the number of clamping diodes per phase increases with the increase of

the number of levels n as $(n-1)\cdot(n-2)$ [33]. A single phase of a 3-level and 5-level DCC are presented in Fig. 2.1.

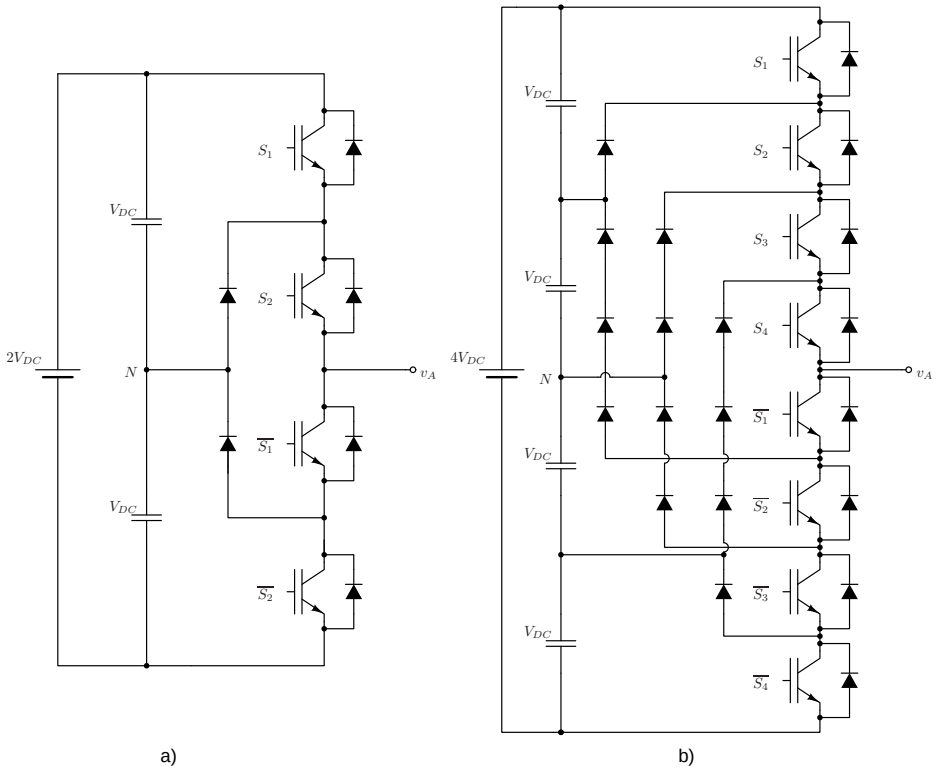


Figure 2.1: Phase A representation of the a) 3-level and b) 5-level diode clamped converter.

The FC converter has a modular structure [10], but an extension to a higher number of levels, requires the addition of another FC cell with increased capacitor voltage rating (cells are not rated at the same voltage levels). An alternative would be to use a stack of capacitors with the same rating, as suggested in [34]. Due to the issues with the extension to the higher number of levels, those two topologies are mostly used in industry in their 3-level (NPC converter) and 4-level (FC converter) configurations [11], in particular for MV drives applications [34].

The CHB converter features cascaded modular structure, that can be extended to any number of levels by adding additional, identical or asymmetrical converter cells.

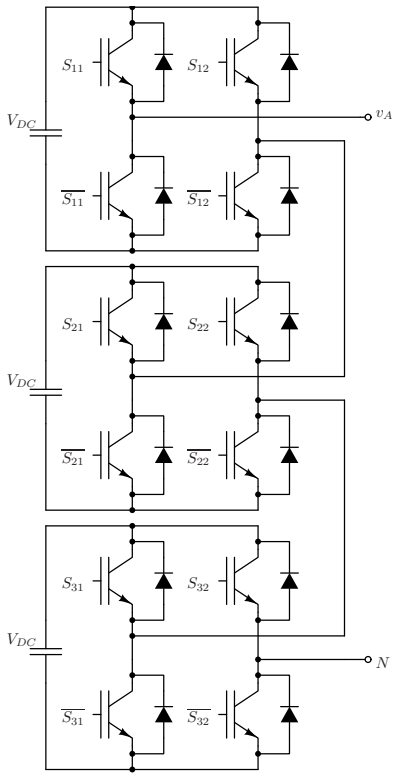


Figure 2.2: Phase A representation of 7-level cascaded H-bridge converter.

The basic unit is a full bridge cell, as presented in Fig. 2.2. In the inverter configuration, the CHB requires multiple isolated DC sources or a complex phase-shifting transformer when applied with a multi-pulse diode rectifiers [11, 34]. However, this topology has made a breakthrough in the power system applications such as static synchronous compensator (STATCOM), active filters (AFs) and other parts of flexible AC transmission systems (FACTS) [10, 11]. Those systems process reactive power, therefore there are no issues related to the capacitor voltages balancing and providing additional DC voltage sources, in the cases of both CHB and NPC converters [11, 23]. Nevertheless, the capacitor voltages balancing mechanism has to be implemented if the asymmetry is present in converter cells or modulation strategy. The CHB converter played a major role in the Universal Flexible Power Management system (UNIFLEX-PM), as an interconnection converter between different AC grids [35, 36].

The summary of all the applications in power system, motor drives, energy generation and transmission of the three classical topologies is given in [11]. The development of the multilevel topologies has not stopped at the classical topologies. These three topologies have triggered development of various hybrid topologies, such as H-NPC combing H-bridge and NPC, cascaded matrix converter (CMC) combining H-bridge cells in matrix converter, active neutral-point clamped (ANPC) converter, T-type converter, etc. [11]. ANPC features the possibility to control the neutral current path, and therefore to solve the problems of uneven loss distribution present in NPC [11, 25, 34]. In [37] multilevel-clamped multilevel converters (MLC^2) are introduced. Those topologies are based on generating the clamping voltage levels (as in DCC) with additional multilevel converters. One of the proposed topologies uses a single phase 3-level NPC converter to generate clamping voltage levels and three phase 3-level NPC converter to generate output waveforms [37]. This way a 5-level MLC^2 is generated with lower component count when compared to 5-level NPC. In addition to those, some asymmetric topologies have been proposed, such as a CHB with unequal cell capacitor voltages [38]. The concept of asymmetric DC voltages is especially interesting in multilevel configurations for open-end machines [39].

In [40] a generalised multilevel topology has been proposed that features the possibility to extend to any number of levels together with balancing of all DC link capacitors voltages. The converter can use different building blocks, such as P2 cells (half bridge), P3D cells (3-level NPC converter) and P3C cells (3-level FC converter). Starting from the generalised topology based on the P2 cells, the majority of multilevel converters can be derived, by simply removing some diodes or switches or capacitors [40, 41]. One of the topologies that can be generated from the generalised topology is a zigzag cascaded converter, requiring only one DC source without capacitors balancing problems [42]. This generalised topology offers a possibility to realise a DC-DC converter topologies as well, such as a magnetic-less DC-DC converter [23, 43], suitable for low voltage applications.

A discovery of a modular multilevel converter [29] succeeded after a principle of converters with distributed energy storage has been patented [44]. The principle

behind this idea is to replace the switches in a half-bridge converter with the so-called "chainlinks" which are a series of cascaded half-bridge cells [13, 29] and to build up a single DC source converter with the distributed energy storage elements. This converter features the ability to extend to any number of levels, thanks to its modular structure and more importantly it is developed using standard low voltage devices, which increases the converter availability [29]. Unlike a two-level converter, arm currents in the MMC converter are not chopped but continuous [30], since there is a current path regardless of the cell control signals and current sign. In the early publications, the converter arms included the chainlink only (without arm inductor) and such a topology can be derived from the generalised multilevel topology [23]. The need of having an inductor when connecting a VSC to the AC grid, has lead to the inductor insertion in the converter arms without affecting the converter performance [2]. The significance of those chokes in the converter arms was first addressed in [30, 2], suggesting that they limit the arm currents ripples and the DC fault current. With the development of closed-loop methods controlling both circulating currents and phase currents [45, 46], the arm inductors became crucial for the circulating current control [47]. A single phase representation of the MMC converter with two half-bridge cells in a chainlink is presented in Fig. 2.3(a).

The idea of a chainlink converters propagated not only to inverter and rectifier topologies, but also to AC-AC converters [48], DC-DC converters [49] and STATCOM applications in a star or delta configurations (in the same arrangements that CHB converters can be used) [45]. Due to possibility to scale to any number of levels and achieve high DC link voltage, without the need for DC link capacitor, MMC became emerging topology for the HVDC systems [50].

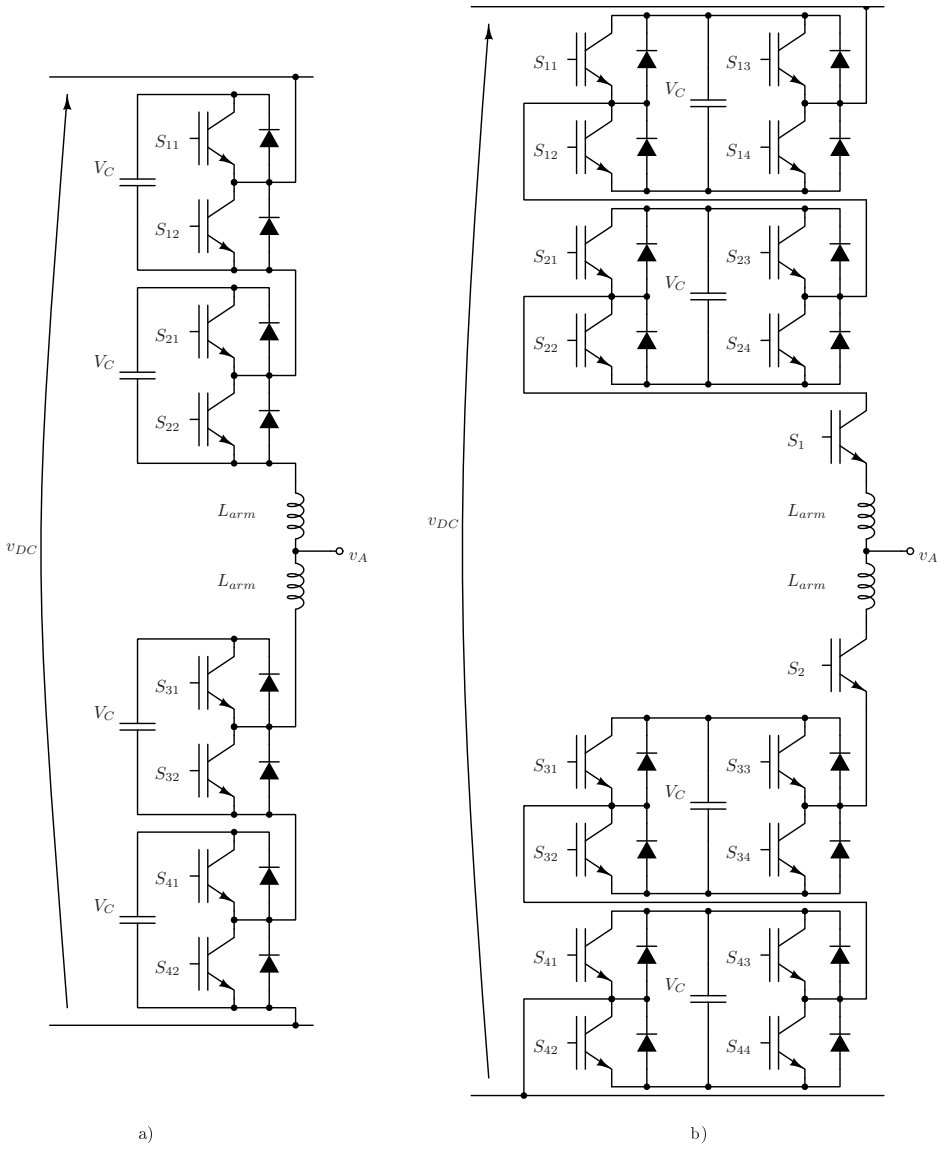


Figure 2.3: Phase A representation of the 2 cell per arm a) MMC utilising half bridges and b) AAC utilising full bridges.

A MMC with half-bridge cells in the chainlinks is the cheapest and the most efficient modular cascaded converter, but it does not have a fault ride-through capability when it comes to a short circuit DC bus fault [51]. To provide the DC link fault ride-through capabilities, cells with a bipolar operation can be employed. One of the candidates is a H-bridge cell that performs bipolar operation. However, this means

an increased component count and doubled semiconductor losses under the normal operation [51]. The alternative are cells that combine the benefits of unipolar and bipolar operation, by providing different current paths for normal and fault conditions [13, 51]. Additionally, multilevel converter cells can be realised as FC cell, T-type NPC cell, etc. [13, 52, 53]. These kind of cells do not provide bipolar operation, but they provide a larger number of converter levels with a smaller number of cells. Based on the standard MMC topology, a modular multilevel series parallel converter (MMSPC) is proposed in [54]. This topology features the ability to connect the submodules in series (as traditional MMC) and also in parallel, by using a 4-terminal cell. The submodules that would be bypassed in a main MMC operation can take over current from the active modules via parallel current path and this way actively participate in capacitor voltage balancing [54].

Various hybrid converter topologies have been proposed that use a combination of monolithic and modular (chainlink, cascaded) topologies [13]. Some of those are with director switches and the series wave-shaping circuit on the AC side, or the wave-shaping circuit on the DC side [55]. Those kind of topologies usually have monolithic director switches that are switched at the fundamental frequency and possibly under zero voltage conditions across the switch (zero voltage switching) [13]. Usually, they have either a lower component count, reduced losses, possibility of a DC fault ride-through while keeping some of disadvantages of monolithic topologies. In the case that chainlinks need to produce bipolar voltages, bipolar cells are required, such as full-bridge cells [13]. One of those topologies is an alternate arm converter (AAC) [55, 56], which has DC fault ride-through capabilities. A single phase representation of an AAC with two full-bridge cells per arm is presented in Fig. 2.3(b). Another interesting topology is a CHB-NPC converter [57] with the series connection of CHB cells and the NPC converter operated at fundamental frequency. Additionally, there are topologies with H-bridge director switches, such as a parallel hybrid modular multilevel converter (PH-M2C) [58]. This topology offers very high efficiency due to the zero-voltage switching of the H-bridge director switches, but requires inductive filtering of the DC link and also isolation transformers on the AC side. A PH-M2C with the input isolation transformer and DC link filtering, is presented in Fig. 2.4.

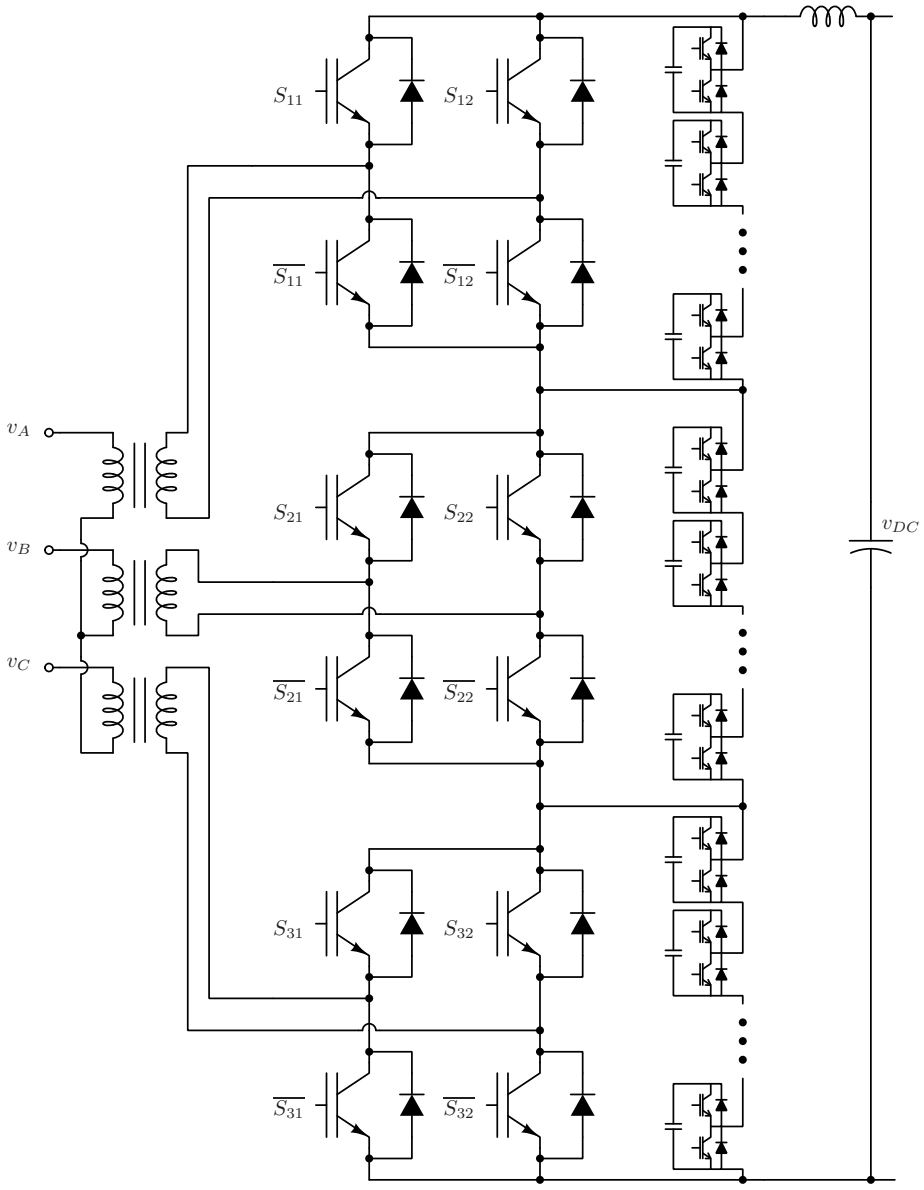


Figure 2.4: Three phase parallel hybrid modular multilevel converter with the input transformer and DC link filter.

2.3 Summary

Multilevel topologies have benefits of good AC waveform quality and harmonic performance, which can be achieved even with low switching frequencies. Reduction in switching frequency leads to an increase of the converter efficiency which makes multilevel topologies particularly interesting for high power applications. In the grid-interface applications, the good AC waveform quality and high efficiency are crucial.

Multiple voltage levels reduce the stress on the devices by reducing $\frac{dv}{dt}$, which is important for diminishing the EMI related issues. Usually, the same AC waveform can be generated with multiple switching sequences. Those redundant states provide a degree of freedom that can be used for implementing additional control loops. In modular converter structures, the converter cells are symmetrical, which brings a redundancy in hardware. Therefore, the extra cells can be added to the structure, in order to allow fault-tolerant operation.

Various multilevel topologies have been presented, starting from the three classic topologies, and leading to some modular and hybrid solutions. The topologies can be classified as monolithic, modular and hybrids of monolithic and modular topologies. Monolithic topologies can not be easily extended to an arbitrary number of voltage levels. Modular topologies can be extended to any number of levels, and they are composed of a number of cascaded identical converter cells.

Depending on the application, power and voltage level, different multilevel topologies can be selected. Monolithic topologies are dominant in the low voltage (LV) and medium voltage (MV) range. Modular multilevel topologies are particularly interesting for MV and high voltage (HV) applications due to the ability to reach any voltage level with standard LV components. One of the topologies, the MMC, had a great influence on the development of modern VSC HVDC transmission links, thanks to the various benefits in high voltage rectifier/inverter operation.

Chapter 3

Power system design

3.1 Introduction

This chapter presents the work carried out on the power system interface for the CLIC facility. In particular it discusses the challenges for the utility interface such as the power system structure and grid interface converters with regards to required functionality, efficiency, etc. The chapter proposes a systematic approach for finding an optimal power system design by considering various possible architectures and analysing their compatibility with the system specifications and technical limitations. Power system design includes global integration, selection of the number of converters, transformers and other power system components, and the most suitable AC and DC voltage levels for distribution. Optimisation parameters driving the design are, for example, overall efficiency, cost and the reliability/availability of the accelerator.

The next section gives an introduction to the power system components, nomenclature and voltage levels. The third section presents the background of all the power system structures considdered and the converter topologies. The features of all the solutions are discussed in order to narrow down the scope of candidates before performing multidimensional optimisation. The following section is focused on the power

system representation and evaluation of different power system parameters, obtained by modelling the system components and also by evaluating the power system as a whole. The fifth section relates to the optimisation, with the target to meet both the grid and klystron modulator requirements by selecting the most suitable number of transformers, converters, etc. and the AC and DC voltage levels.

3.2 Power system components and nomenclature

The power system comprises multiple sources and loads, typically connected to the points of fixed voltage levels (bus bars). A power system is usually not autonomous, i.e. it is connected to the grid at the transmission voltage level (110 kV and above) via transmission lines [59]. Aside from the grid, the power system can have other energy sources, so-called dispersed generation units, such as alternative energy sources, or energy storage elements that can be used as both sources and loads depending on the direction of power flow [60]. Those kind of sources are typically integrated in the power system at distribution voltage level (from 7.2 kV to 36 kV depending on the country) [60]. The power system loads can be various, belonging to industrial, residential, transportation, commercial, etc. consumption groups that can also be integrated in the power system at different voltage levels. Transformers provide a voltage step-down between the transmission and distribution voltages. Transformer windings can be connected in three ways: star, delta or zig-zag, that are assigned with Y, D, Z, respectively. Uppercase letters are used at the transformer primary side, while the lowercase letters are used on the secondary side [61]. In addition, when 4 wire connection is available, N (n) is added to assign a neutral, while in the case of delta connection, a number from 0 to 11 is added to indicate the phase shift (from 0 ° to 270 °) between the primary and the secondary windings.

Every voltage level is assigned a bus bar, which is a low resistance conductor bar capable of carrying high currents without significant voltage drop. The power system components are connected to the bus bars via various breaking equipments, such as

circuit breakers, mechanical switches, fuses, disconnectors, etc. Bus bars are typically contained in enclosed switchgear that also includes breaking equipment. Switchgear is mainly used in the low voltage and distribution voltage range and their technology is addressed in [62].

In the case that the power taken from the power system is not of a good quality, in the sense of power factor and total harmonic distortion, additional power system components are used. Those include active and passive filters, static VAR compensators (SVCs), STATCOM, to name a few.

Here, the voltage ranges for the transmission and distribution are introduced. However, power system components are often rated at high, medium and low voltages, therefore those voltage levels have to be defined. According to the standard IEC 60038 [63] a high (and extra high) voltage corresponds to voltages above 35 kV, medium voltage corresponds to the voltage range from 1 kV to 35 kV, while low voltage is below 1 kV.

3.3 Background on possible power system structures

The grid connection at CERN is at the transmission voltage level of 400 kV, while the klystron modulator input voltage is in the range from 6 kV to 20 kV. Approximately 1300 klystrons are distributed along a 2 - 2.5 km path, thus a well-structured power system must be designed considering both spatial and electrical distribution constraints. Klystron modulators have a capacitor at their input used to limit the voltage droop to the specified range, between 5 % and 20 % of the nominal DC voltage value. The power system used as a grid interface for the klystron modulators is also referred to as a capacitor charger (main capacitors bank) [4, 7]. In [7] various charger architectures were presented considering both a classical approach with a low voltage AC/DC and DC/DC converter per klystron modulator and a single medium

voltage charger AC/DC converter supplying a DC voltage bus-bar feeding all klystron modulators with or without intermediate DC/DC converters. The classical approach is studied in more detail together with the matrix pulse transformer based klystron modulator design in [64]. Here, the general charger infrastructure will be studied for the case of capacitor pulse discharge klystron modulators [9].

In general, all power system architectures can be classified as either single-stage or double-stage on the basis of how many stages of power conversion there is. Single-stage conversion systems include only AC/DC converters used for charging the main capacitor bank. Double-stage conversion includes both AC/DC and DC/DC converters, which decouple the pulsed load effects at the modulators side from the utility grid. Multilevel topologies are naturally suitable for the CLIC application since all the voltage levels are at MV range or higher. Therefore, the multilevel topologies presented in Chapter 2 are considered as candidate topologies in both single- and double-stage conversion systems.

Both single- and double-stage solutions start with a grid connected VSC aimed at active power transfer from the grid to the klystron modulators or intermediate DC/DC converters. A voltage source converter, presented in Fig. 3.1, is connected to the grid via a dominantly inductive impedance (resistance is neglected here). In that case, if the converter draws purely active power, the amplitude of the converter phase voltage should be higher than the grid phase voltage amplitude, to allow for the voltage drop across the phase inductance. This is analysed in more detail in subsection 4.4.1, and concluded with the (4.28). Considering three phase AC to single DC bus converter topologies, such as NPC, FC, T-type converter and MMC, the maximum AC phase voltage is equal to the one half of the DC link voltage. In the case of hybrid topologies such as AAC and PH-M2C the maximum phase voltage is $\frac{2}{\pi}V_{DC}$ and $\frac{\pi}{6}V_{DC}$, respectively [56, 58]. A particular case is a CHB converter, utilised as a three-phase AC to multiple DC bus converter, where the maximum phase voltage is equal to $N \cdot V_{DC}$ where N is the number of cascaded cells per phase and V_{DC} is the nominal cell output voltage. Based on the previous discussion, the maximum RMS line to line grid AC

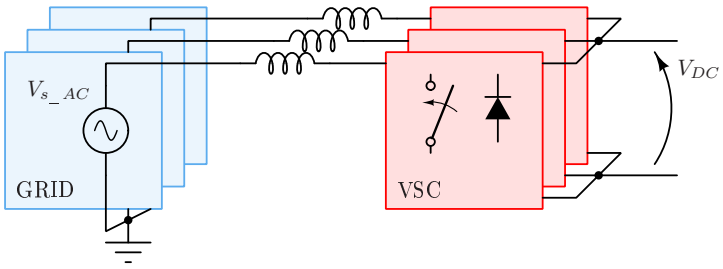


Figure 3.1: Grid connected voltage source converter.

voltage is described by:

$$V_{s\_AC} \leq \frac{\sqrt{3}}{\sqrt{2}} k_{AC} \cdot V_{DC} \tag{3.1}$$

where k_{AC} depends on the converter type, being $\frac{1}{2}$, $\frac{2}{\pi}$, $\frac{\pi}{6}$ and N for MMC, AAC, PH-M2C and CHB converter, respectively. If there is a single stage of conversion, for all converter types, apart from CHB converter, the AC voltage will be in the range of 3 kV (MMC, NPC, T-type converter, etc producing 6 kV DC voltage) to 15 kV (AAC producing 20 kV DC voltage) depending on the DC voltage level and the selected topology. Those voltage levels all belong to the MV range and the grid connection point is at 400 kV, therefore step-down transformers are used to provide the specified AC voltage. Due to the large step-down ratios (30-130 times) two stages of step-down transformers have to be utilised. Fig. 3.2 shows an example of a single stage power conversion system with two low frequency transformer stages. Note that in order to distinguish between the two MV levels in the second transformation stage, the lower voltage is now termed lower MV (LMV). In the case of CHB converter, the AC voltage range is defined with the number of cells and the DC voltage level and it can belong to either medium or high voltage range. Hence, in the case of CHB converter one stage of step-down transformers might be sufficient.

In double-stage conversion systems, DC/DC converters can provide a voltage step-down, therefore eliminating the need for one step-down transformer stage. A double stage conversion example is presented in Fig. 3.3. The DC/DC converters are based on the dual active bridge concept where the individual bridges can be standard two-

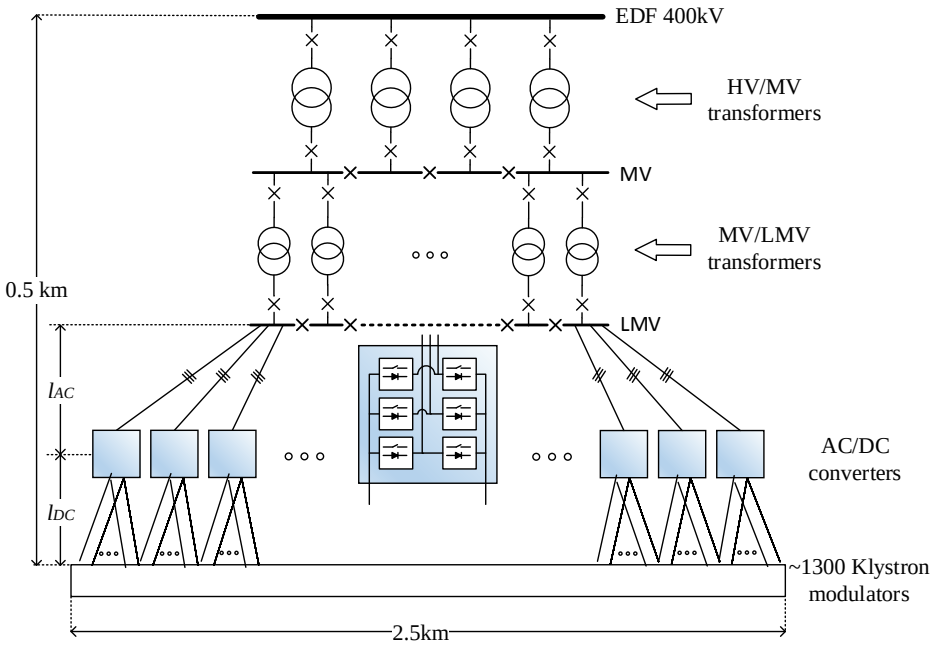


Figure 3.2: Single-stage conversion example.

or three-level or MMC based [49] with an inductive element between them used to control power flow [65]. The inductive element can be a transformer which in that case provides both insulation and a step-down in voltage. This avoids the problem of trying to achieve a large ratio via modulation alone which is very inefficient.

In the case when a CHB converter is used in a single-stage architecture, it provides multiple DC outputs that are floating with respect to the AC neutral and ground potential. In this case the inputs of the modulators are floating at the potentials reaching $(N-1)V_{DC}$ (medium or high voltage range). The active bouncer as a part of a klystron modulator [9] would require high isolation of the utilised electronics (a few of tens of kV). Also the DC voltage distribution would be done at floating voltage levels, which is not preferable. This solution restricts the modulator design, and therefore it is not suitable for the CLIC application. The solution with a CHB converter also requires an insulation stage providied by an isolated DC-DC converter per CHB converter cell, in the same manner as in UNIFLEX [35]. This solution

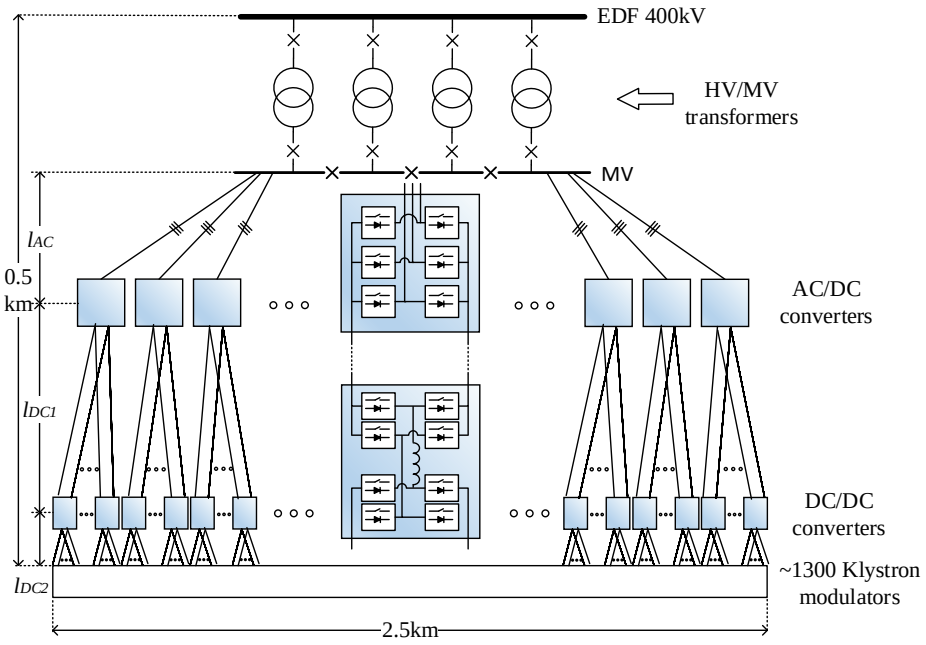


Figure 3.3: Double-stage conversion example.

apart from requiring transformers in the isolated DC/DC converters, also requires two capacitor banks, one at the modulator input and one on the converter cells.

In [66] the scope of possible power system structures in terms of the number of transformers and converters is presented for the case of a modulator input voltage fixed at 10 kV. The study presented relays the current infrastructure used at CERN, including the 66 kV and 18 kV voltage distribution system [5]. However, building a new linear accelerator will involve complete rebuilding of the power system, allowing different distribution voltage levels and therefore in the study that follows a number of other possibilities is considered. The scope for number of transformers and converters is derived on the basis of rated power at the specified voltage levels. Similarly the maximum converter current is limited to 1 kA, due to the maximum current ratings of MV cables and selected switches [66].

The possible voltage levels are defined by the available cable and switchgear ratings.

The medium voltage cable catalogues offer the cable parameters for the discrete voltage levels, presented in Table 3.1. In addition, corresponding switchgear voltage levels are given. The selected voltage levels should be close to the rated levels of the cables, in order to fully utilise their insulation potential. The information provided in Table 3.1 is based on the medium voltage cables produced by Nexans and General Electric switchgear components [67, 68].

Table 3.1: Cable and switchgear voltage ratings

Cable voltage rating phase/line (maximum)	Switchgear voltage rating
1.8/3 (3.6) kV	3.3 kV
3.8/6.6 (7.2) kV	7.2 kV
6.35/11 (12) kV	12 kV
8.7/15 (17.5) kV	17.5 kV
12/20 (22) kV	24 kV
19/33 (36) kV	38 kV

Based on the possible voltage levels from Table 3.1 and the relation between AC and DC voltage (3.1), candidate distribution voltage levels can be selected. The relation (3.1) is dependent on converter topologies, due to different values of k_{AC}.

Double-stage conversion power system architectures are assumed to be more expensive and less efficient than single-stage architectures. The challenge for a single stage system architecture is to achieve a low power pulsation at the AC grid given the pulse nature of the DC load. There are many benefits from adopting a single-stage architecture if this problem can be solved. Therefore this thesis assumes the adoption of a single-stage power system architecture and solving the power fluctuation problem to make this feasible is a main objective of the work carried out on the conversion stage, as documented in Chapter 5.

In [66], where the DC voltage is specified to be 10 kV, the topologies considered were modular multilevel, hybrid multilevel and classic monolithic topologies. The multilevel topologies are used in the higher power range, while in the lower power

range monolithic topologies such as NPC and FC converter are used. Use of multilevel topologies in the case of a single converter per klystron modulator (rated power of 200 kW) would be cost inefficient. In the case of NPC or an FC converter operating at a 10 kV DC bus voltage, a series connection of low voltage switches or usage of the MV switches is required, which together with increased switching frequency leads to increased losses. As a design rule for the optimisation stage, a decision on converter topology is done on the basis of the DC voltage, where for voltages of 10 kV and above, modular multilevel topologies are used, while for the lower voltage range monolithic topologies are selected [69].

Figs. 3.2 and 3.3 present the example of both the electrical and spatial distribution. The transformer stages are placed in proximity to the EDF connection, while a larger distance is assumed for LMV AC cables and DC cables. However, the spatial distribution has to be decided by the design rules, set to minimise the losses and maximise the availability of the power sistem. Availability and reliability of the power system is increased by providing a defined amount of redundancy, and using proven technologies for the power system and power electronics components.

3.4 Power system representation

The chosen power system structure has two stages of step-down transformers and AC/DC converters. Radially distributed bus bars are present at every voltage level. An example of such a system is presented in Fig. 3.2.

This section presents the design rules and the power system limitations and based on them derives the power system structure. Depending on the number of bus bars, transformers, converters, etc. all system components ratings will be known and therefore it is possible to model them. The following subsections present the models of the power system components and evaluation parameters of the system as a whole.

3.4.1 Design rules and CERN specific limitations

The design rules include a set of assumptions made in a design and optimisation process that are fixed for all considered solutions. Design rules, together with the number of power system components fully define the power system layout. The set of rules is listed below:

- *The longest cables are at the highest AC voltage levels* - Transmission and distribution at higher voltage levels, requires less current at the same power level, which reduces the losses in cables. In addition, the DC voltage is controlled on the converter DC side, therefore the shortest possible DC voltage cables enhance the DC voltage quality at the modulator inputs.

- *Fault currents are within the interruption capabilities of standard breaking equipment* - Based on the equipment currently used at CERN, the prices of breaking equipment, such as medium voltage switchgear, significantly increase when the fault currents go beyond 20 kA. Therefore, the power system topological selections are done to ensure the fault currents at the MV and LMV bus bars are lower than 20 kA.

- *A defined amount of redundancy is provided at every voltage level* - This involves paralleling transformers and converter outputs in order to provide reconfigurability of the network in the case of a fault. The power system and power electronics components are rated at higher powers (or voltages) than nominal and some additional transformers, cells, connections, etc. are added to provide redundancy.

- *Usage of standard low voltage IGBTs* - To provide high reliability and availability of the accelerators, proven and available technologies are used at CERN. Therefore use of standard 1.7 kV IGBTs is suggested even for medium voltage converters. In addition, the nominal suggested switch voltage is 1 kV, due to the high risk of ionizing radiation failures under overvoltage and high electric field, typically leading to loss of switch gate control.

- *Halogen free cables* - At CERN medimum voltage cables used are halogen free, XLPE single-core copper conductors. The maximum cable cross section used is 400 mm^2, due to the size of standard switchgear cable sockets and banding issues typical for higher cross section conductors. Cables are placed in surface galleries, where the current capacity de-rating factor is set to be 0.7. The grid connection at the transmission voltage level is provided by aluminum conductor overhead cables [59].

- *HV substations are outdoor while MV substations are indoors* - HV substations include overhead cables and oil-insulated HV/MV transformers that are typically outdoors. MV substations include MV bus bars realised with the enclosed switchgear, typically located indoors, and dry-type MV/LMV transformers.

3.4.2 Power system design

The power system layout supporting the given design rules is shown in Fig. 3.4. The 400 kV to MV conversion is achieved with an outdoor substation and in general, there can be more than one. Under these circumstances, the distribution (long cables) is performed at 400 kV. Additionally, MV bus bars (enclosed switchgears) are distributed along 2 km drive beam, so that the MV cables are longer than the LMV or DC cables. This way the HV/MV substations and MV bus bars are placed in proximity to the klystron modulators. The system starting from the MV bus bars to the klystron modulators can be divided into equivalent sectors, each of them is associated to one MV bus bar. One of the sectors is presented in Fig. 3.4 where there are 4 MV bus bars, therefore 4 equivalent sectors.

Redundancy is achieved by parallel connection of transformers (or converter outputs) to a common bus bar. In the case when n parallel components are needed to support the power rating, one spare component is added to achieve $(n + 1)$ redundancy. In this case the rated and nominal power of the parallel components are different and

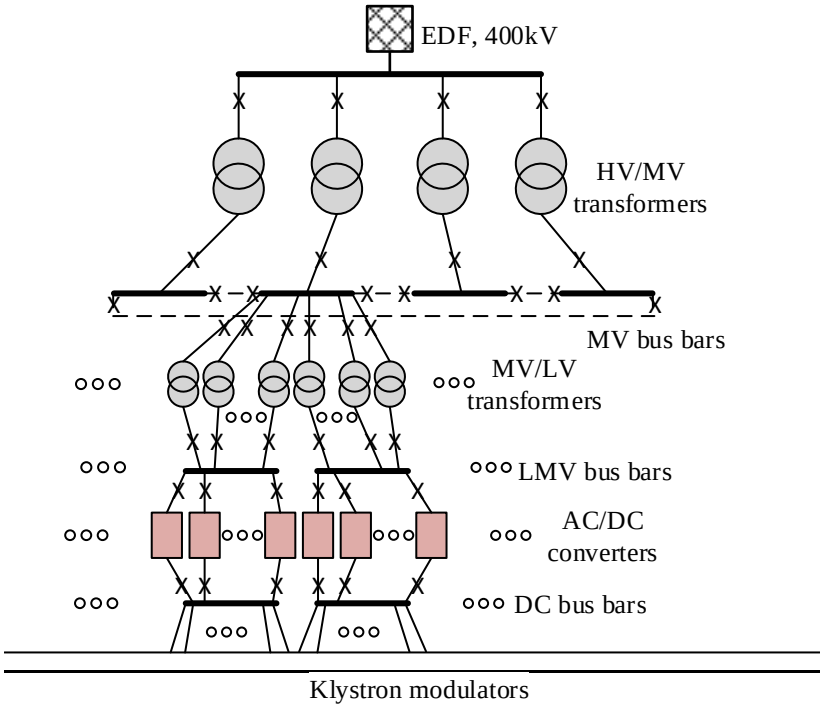


Figure 3.4: An example of a power system layout with radially distributed bus bars.

described by:

$$P_{rated} = \frac{P}{n}, \quad P_{nominal} = \frac{P}{n+1} \tag{3.2}$$

where, P is the power rating of the common bus bar. Since the grid source is quite close to the drive beam, maximum fault currents are foreseen to be higher than the breaking currents of standard equipment. In order to increase impedance, and reduce the fault current at MV level, two HV/MV transformers in normal operation are never operated in parallel. Thus, there is only one HV/MV transformer per MV bus bar and the redundancy must be provided from the MV side, by connecting the bus bars (Fig. 3.4). In the case of transformer failure the power will be supplied from two neighboring bus bars and all HV/MV transformers are rated at 3/2 of the nominal power. This way in the case of failure of one cable, transformer, circuit beaker, or a converter per bus bar, there will be a way to reconfigure a system and supply a bus bar with the nominal power, providing fault tolerant operation.

In the case of a bus bar failure, all loads corresponding to that bus bar will not

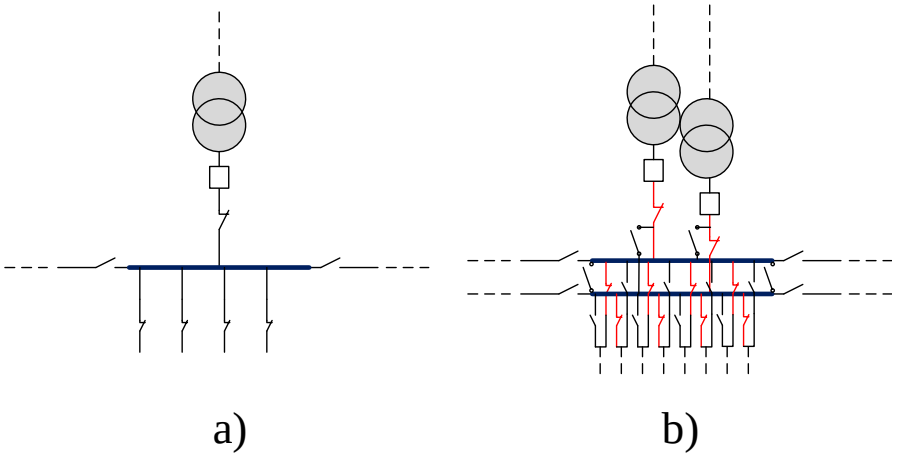


Figure 3.5: A comparison of a) single and b) parallel bus bars design principle.

be supplied. The bus bar failure rate is much lower than those of transformers, switchgears, cables and converters. However, two approaches are possible: the first one, with radial distribution of bus bars was already explained; and a second one with parallel bus bars. The illustration of single and double bus bar principle in case of MV bus bars is presented in Fig. 3.5. In the second case, all loads and feeders associated with one bus bar have the potential to be connected to a parallel bus bar. Also, parallel bus bars can be connected amongst themselves as a support when there is a lack of power on one of them. For the case of double bus-bars, transformers are rated at twice the nominal power. The DC bus bar will remain single (without parallel pair) due to the large number of connections (≈1300). Having double bus bars would certainly increase the power system and accelerator availability, but the cost increase would be significant, as well.

From the power electronics point of view, paralleling converter outputs on a common DC bus bar might add extra control complexity. In the case of an MMC, a current contribution of each phase its controlled and delivered to the DC link without any inductive filtering. Therefore, the equal current sharing among different converter phases is provided without significant increase of control complexity [70]. Both PH-M2C and AAC require some inductive filtering, therefore making a requirement for

DC current sharing control. The situation might be easier for the AAC whose structure is very similar to MMC. The AAC has some benefits when compared to MMC, such as DC fault ride-through ability and higher coefficient k_{AC}. However, the AAC requires full-bridge cells and director switches, which brings additional cost. PH-M2C has a hybrid structure, with coupled AC and DC side control. The benefit with respect to MMC is smaller number of cells required with somewhat increased losses and reduced modularity. Therefore, considering all the aspects of the given application, the MMC offers the best efficiency, availability, control complexity, cost compromise. Still, in the voltage range below 10 kV, some simpler converter solutions such as NPC or FC converters are considered.

Based on Table 3.1, in the case of a single-stange conversion system, utilising converters with $k_{AC} = \frac{1}{2}$, there are six potential cases for the distribution voltage ratings, as described by Table 3.2.

Table 3.2: Possibilities for the power system voltage ratings

HV/MV transformer primary/secondary (ratio)	**MV/LMV transformer primary/secondary (ratio)**	**Converter AC/DC**
400 kV/33 kV (12.1)	33 kV/3.3 kV (10)	3.3 kV/6 kV
400 kV/33 kV (12.1)	33 kV/6 kV (5.5)	6 kV/10 kV
400 kV/33 kV (12.1)	33 kV/10 kV (3.3)	10 kV/20 kV
400 kV/20 kV (20)	20 kV/3.3 kV (6.1)	3.3 kV/6 kV
400 kV/20 kV (20)	20 kV/6 kV (3.3)	6 kV/10 kV
400 kV/20 kV (20)	20 kV/10 kV (2)	10 kV/20 kV

The first three cases from Table 3.2 have more uniform distribution of the step-down ratios between the two stages of transformers. In addition, at the higher voltage ratings the maximum fault currents are expected to be lower. Therefore, the first three cases are selected for the optimisation. The voltages given in Table 3.2 are approximate, to satisfy the cable technology of 3.6 kV, 7.2 kV, 12 kV, 22 kV and 36 kV from Table 3.1.

3.4.3 Cable models

Current and voltage ratings are the main parameters for cable selection. Current rating is dominantly determined by conductor cross section area (CSA) and material, but is also influenced by the number of cores, and the environment in which the cables are placed, such as in the ground, in galleries, in ducts underground, in air, etc. The data provided by the manufacturer specifies current ratings considering a specific installation environment, but in the ideal case (specific air/ground temperature, depth in ground, ground resistivity and single cable). In the case of multiple cables or deviation from the "ideal" environment de-rating factors should be applied. The cable CSA selection is based on the rated RMS value of the cable current. A de-rating factor of 0.7 is selected for the surface galleries, while the maximum CSA is $400\,\mathrm{mm}^2$. In the case of higher current ratings requiring higher CSA, paralleling of the cables is done.

Resistance, inductance and capacitance per unit of length are also provided by the manufacturer. Resistance is predominantly determined by the conductor properties, and temperature. Capacitance depends on the cable dimensions and the insulation permitivity. Inductance is also dependent on the cable dimensions. For the exact calculation of cable losses and current rating, all the formulas and information is defined by standard IEC 60287-1-1 [71]. However, for the purpose of loss estimation of cables (as a part of CLIC distribution), cable resistance will suffice. Having the current rating (nominal current RMS value), cable length and resistance, the ohmic losses are obtained. The losses are multipled by three in the case of AC distribution, when cable AC resistance is used. Similarly the losses are multiplied by two in the case of DC distribution when cable DC resistance is used. For the purpose of fault current calculation, both cable resistance and reactance are used. Cable length is defined by the spatial distribution of the cable galleries connecting the bus bar (switchgear) to the power system components such as transformers or converters (see Appendix A).

The cost of cables is driven by the cost of copper, and it increases with the voltage level due to the higher insulation requirement. The prices used in the final optimi-

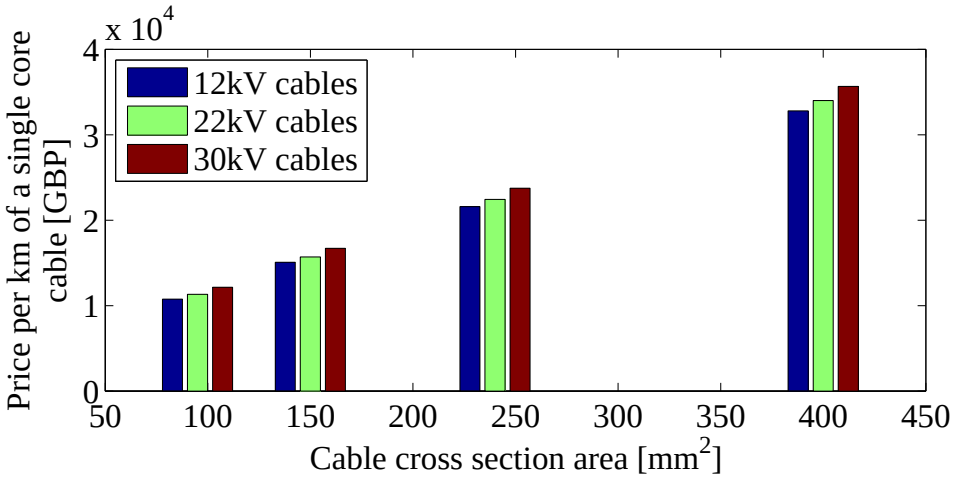


Figure 3.6: Cable prices in GBP for the MV cables depending on the voltage rating and conductor cross section.

sation, taken from the internal CERN data (SolidAl condutores electricos, S.A.) are presented in Fig. 3.6. It can be seen that cable prices increase with the cross section and voltage rating almost linearly.

3.4.4 Transformers

There are two stages of step-down transformers, first from 400 kV to 33 kV and second from 33 kV to either 3.3, 6 or 10 kV. The first stage requires oil insulated transformers, while the transformers operated at MV are dry, typically cast resin insulated. The intermediate voltage level of 33 kV was selected to belong to the MV region, to allow the use of dry transformers in the second stage, since they are significantly cheaper than oil insulated ones. The power range for the HV/MV transformer is between 50 MW and 150 MW, while the MV transformer power range is assumed to be between 2 MW and 12 MW.

Transformer windings can be connected in any of the three possible ways. The arrangement of the windings affects the propagation of different sequence components in the case of a short-circuit fault, therefore affecting the maximum fault current. For

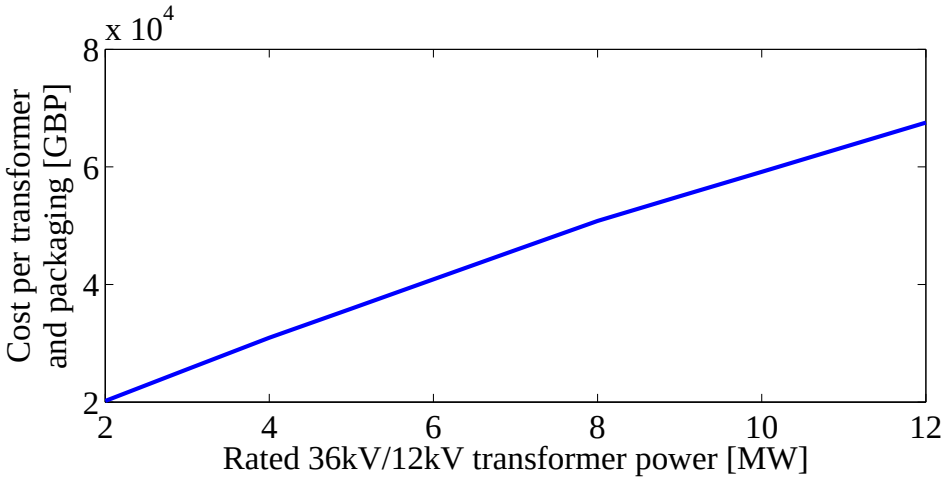


Figure 3.7: Transformer (and packaging) price in GBP vs. rated power

the purpose of fault current calculation transformer impedances are used. Typical per unit impedance voltage drop for the given primary voltage and rated power are obtained from [72]. The per unit impedance voltage drop u_k and resistance voltage drop u_r for the HV/MV transformers, are in the range of (10, 16) and (0.15, 0.5), respectively. Per unit impedance and resistance voltage drop of MV/LMV transformers for the given power range, are in the range (6.1, 9.1) and (1.525, 2.124), respectively.

For the purpose of efficiency calculation, two types of losses have to be taken into account: no-load losses, related mainly to the core losses; and full load losses related to both copper and core losses. Details of transformer full load losses and no-load losses, in the case of 36 kV primary, and different secondary voltages (6 and 12 kV) are taken from CERN internal data. The same source is used for estimating MV transformer price and its dependence on the rated power as presented in Fig. 3.7.

3.4.5 Fault Currents

The maximum fault current in the system should not exceed 20 kA which is the breaking current of standard MV interruption devices. Usage of standard equipment lowers the price and also improves the overall availability of the system. The fault currents

are calculated by using an equivalent circuit containing the impedances towards the grid and an equivalent voltage source at the fault location. The equivalent voltage source U_{fault} as a function of nominal voltage U_{nom} at the fault location is given by:

$$U_{fault} = c_{max}\frac{U_{nom}}{\sqrt{3}} \approx 1.1\frac{U_{nom}}{\sqrt{3}} \tag{3.3}$$

where, c_{max} is the voltage factor for calculating maximum fault current [72]. Typically, the three phase fault is the most severe, i.e. causing the maximum fault currents. However, the maximum fault current can correspond to some other fault type, depending on the impedance ratios. The fault current is the highest in the sub-transient period [72], therefore those currents are observed. Table 3.3, shows the sub-transient fault currents (initial short circuit current) for different fault types. Z_1, Z_2 and Z_0 denotes positive, negative and zero sequence impedance, respectively. In the case of transformers and cables, positive and negative sequence impedances are equal, while the zero sequence impedance is given by impedance ratio, in the case of a transformer, and the DC impedance, in the case of cables. The three phase to ground fault is considered a symmetrical type of fault, producing only positive sequence currents and requiring calculation of only positive sequence impedances. In cases of some asymmetrical faults, e.g. two phases to ground, zero and negative (equal to positive sequence) sequence impedances have to be obtained.

Table 3.3: Maximum fault currents depending on the fault type

Fault description	**Sub-transient fault current**
Three phase short circuit to ground or free of ground	${I_{K3}}'' = \frac{1.1 \cdot U_{nom}}{\sqrt{3}\lvert Z_1 \rvert}$
Two phases short free of ground	${I_{K2}}'' = \frac{1.1 \cdot U_{nom}}{\lvert Z_1 + Z_2 \rvert}$
Two phases short to ground	${I_{KE2E}}'' = \frac{1.1 \cdot \sqrt{3} \cdot U_{nom}}{\lvert Z_1 + Z_0 + Z_0 \frac{Z_1}{Z_2} \rvert}$
One phase short to ground	${I_{K1}}'' = \frac{1.1 \cdot \sqrt{3} \cdot U_{nom}}{\lvert Z_1 + Z_2 + Z_0 \rvert}$

To decide on delta or star connection of the transformers, the current network infrastructure at CERN is used as an example. HV/MV transformers are YNynd0 type,

so that the zero sequence current can pass from primary to secondary, through the zero sequence transformer impedances and neutral grounding impedances. Thus, zero sequence current exists in the case of some asymmetrical faults on the MV level. Currently used MV/LMV transformers are YNd11, that are blocking the zero sequence fault current on the LMV connection [73].

A fault at the MV level has an equivalent impedance calculated from the sum of the cable impedances, the impedance of the HV/MV transformer and the grid. The grid maximum fault power and impedance ratios, given in the Table 1.2, are used for estimating the minimum grid resistance and reactance for the positive and zero sequence. Similarly, overhead lines and cable impedances are estimated. Per unit impedance voltage drop u_k and per unit resistance voltage drop u_r ranges taken for the manual are used for estimation of resistive and reactive part of the transformer impedance for specific voltage and power rating [72]. Those per unit values have to be recalculated for the base voltage equal to the nominal voltage at the fault location. Faults at the LMV level, have an equivalent impedance equal to the sum of impedances of the parallel MV/LMV transformers, cables, the impedance of one HV/MV transformer and the grid. The impedance of parallel connections of transformers includes the reduction of transformer impedance by the number of transformers (per LMV bus bar).

The number of HV/MV transformers and MV bus bars influences the fault current at the MV voltage level in the same way for all analysed layouts. The minimum number of the MV bus bars that guarantees the fault current within the breaking capabilities of the MV equipment is 4. In the case of three MV bus bars, the fault current at 30 kV is 20.6 kA and it is caused by the symmetrical 3 phase fault. On the other hand, the maximum fault current at the LMV bus bar is influenced by both voltage level and the number of power system components. At this stage, due to the MV/LMV transformers type chosen, only symmetrical fault types are considered. The obtained results for the lowest AC voltage (3.3 kA) indicate that the fault currents are always beyond 20 kA. For the other two voltage levels, the maximum fault current at the LMV bus bars can be lower than 20 kV but it is sensitive to the number of

transformers and bus bars used. The maximum fault current, considering both MV and LV bus bars is analysed in detail in section 3.5.

3.4.6 Availability

Reliability is the probability that a component performs its intended operation for a specified period of time under normal operating conditions [74]. On the other hand, a failure rate is a probability that the device will fail to perform its intended operation in the next time unit, while until that moment operation was normal. Availability is given as a percentage or proportion of time in which the device operates properly. Unavailability is also given as a percentage or proportion of time in which the device does not operate properly (availability and unavailability sum up to 1 or 100 %). In the following study both availability and unavailability are given in min/year.

In order to estimate power system availability certain assumptions are required. A failure that will not cause a system outage due to the ability to reconfigure the power system is not considered a fault. These failures might require the system to power off and restart, but to simplify the analysis, they are not considered a fault. A fault is only a failure (or combination of failures) that can not be corrected by system reconfiguration.

A fault tree analysis algorithm is applied for the unavailability probability calculation. Fault tree analysis is based on the collection of all combinations of basic events that lead to the top event [75]. The top event (TE) is being considered as the most undesirable event. Failure of any component is considered to be a basic event (BE). A combination of basic events that lead to a top event is called a minimum cut set (MCS). Any of the MCSs can cause the top event, which is in that case described by:

$$TE = \sum_i MCS_i = \sum_i \Big(\prod_j BE_j \Big)_i \tag{3.4}$$

In this case the top event is failure to deliver power to a certain number of klystron modulators. Failure to deliver power at any voltage level will, as a consequence, lead

to the TE. If every voltage level has a top event (failure to deliver power at that level) and if those top events are not mutually dependent, the probability of the global top event is the sum of probabilities of each of the local top events. To calculate the probability of the top event at the specified voltage level, all minimum cut sets need to be identified as a collection of basic events. Taking this into account the probability of the top event on a specific voltage level can be calculated by:

$$P_{top} = \sum_{i} P_{MCS_i} - \sum_{i<j} P_{MCS_i \cap MCS_j} + \sum_{i<j<k} P_{MCS_i \cap MCS_j \cap MCS_k} - ... \tag{3.5}$$

Minimum cut sets are usually a combination of a feeder failure and the failure of the connecting switches and cables needed for reconfiguration, or a bus bar failure without an option to reconnect the loads. On the bus bars where $(n+1)$ redundancy is applied, the top event occurs if two or more feeders on the common bus bar fails and reconfiguration is not possible.

For the probability (to fail) calculation, the data for all the basic event probabilities must be known. This data is usually statistical based on experience of the cables, switchgear, circuit breakers, transformers, and disconnector failure rates. The data is obtained from the German Association for Electrical, Electronic & Information Technologies (german: Verband der Elektrotechnik Elektronik Informationstechnik e.V, VDE) that collected the failure rates for the transmission and distribution network components [76]. Obtained data relates to the period from 2004 to 2011 and it is described with the number of failed components, failure frequency [1/year], average interruption duration [h] and probability of component unavailability [min/year]. The converter unavailability is not modelled in detail and a constant unavailability is assumed for all the converters being approximated at 15 min/year. This value is derived on the basis of an approximated converter failure rate of $30 \cdot 10^{-6}$ 1/h and interruption of 1 h. The failure rate here is an average value for the converter topologies analysed in [77] based on the military standard from 1995 [78] (this standard is nowadays considered obsolete therefore this estimation might be inaccurate, but is the best available without significant extra work beyond the scopes of this thesis).

The typical unavailability of a power system with single radially distributed bus bars

is around 180 min/year. At the same time, the typical unavailability of the power system with the parallel bus bars is around 20 min/year. Variation of the number of power system components does not significantly affect the power system unavailability when the assumed redundancy design rules are followed. Parallel bus bars have higher reconfigurability which provides higher availability. However, some reconfigurations require system shut down which decreases availability. If this is taken into account, the expected difference in availability will be smaller. The final design will be a trade-off between cost and availability.

3.4.7 Power electronics parameters

Power electronic components have to be modelled in terms of efficiency, cost and size. The converter efficiency is mainly dependent on the topology used, but there are some variations depending on the converter power and voltage ratings, requiring different ratings of the switches and passive components. The cost and size are mainly related to the converter ratings, while some variation in power density is expected for different topologies.

The MMC sizing is presented in detail in section 4.5, where the number of converter cells, size of cell capacitance and arm inductance are addressed. The NPC converter does not have passives, but the ratings of the switches has to be selected. This topology is a candidate for 3.3 kV AC to 6 kV DC converter, and if 1.7 kV IGBTs are used, every switch (Fig. 2.1a)) has to be replaced by series connection of three switches.

The losses in the converter are divided into losses in passive components (capacitors and inductors in the case of MMC) and losses in the active components (IGBTs and diodes). The losses of the active components are further divided into switching and conduction losses that are estimated using the methodology from [2] and verified through the simulation. Conduction losses are computed considering the linearised relation between the switch turn on voltage, and on-state resistance, approximated

from a v_{CE}-i_C curve available in the datasheet. Switching losses are estimated on the basis of IGBT turn-on and turn-off energies, and the diode reverse recovery energy available in the datasheet for the rated switch voltage and current. In [2], MMC current waveforms and uniform switching among cells is assumed, so that averaged currents of all switches and diodes can be derived. In a similar way, a semi-analytical approach can be derived, where the instantaneous currents are integrated by numerical simulations. This methodology can be applied to some other topologies, where internal currents have more complex harmonic content.

Switching frequency directly affects the switching losses. The switching frequency of the 10 kV DC voltage MMC is set to 6500Hz (650 Hz equivalent cell switching frequency), where, the switching frequency of the 20 kV DC converter is 5000 Hz (250 Hz equivalent switching frequency of the cell). The selected values follow the switching frequency of the similar scale HVDC prototypes [79]. In the case of an NPC converter, the selected switching frequency is 2500 Hz (this is already a high frequency for an NPC converter [11] and the expected AC waveform quality and available bandwidth are not comparable with those provided by an MMC). The losses are dependent on the converter rated and nominal power and rated voltage, and the characteristics of the semiconductors used.

For the purpose of modelling the losses in the capacitance, an equivalent series resistance (ESR) of 1 mΩ (this follows the ESR values of the film capacitors for given voltage/capacitance range [80]) is assumed to be the only source of losses. The arm inductor is modelled as air cored inductor, known as Brooks coil [81], using copper bar. The series resistance is estimated on the basis of copper resistance.

The comparison of the converter efficiency, for the converter operation at the rated power is given by Fig. 3.8. The DC current is limited to 200-1000 A, and the NPC converter is used when the DC voltage is about 6 kV while MMC is used when the DC voltage is 10 kV and higher. The parameters of the 1.7 kV switches, are taken from a Dynex module datasheet [82].

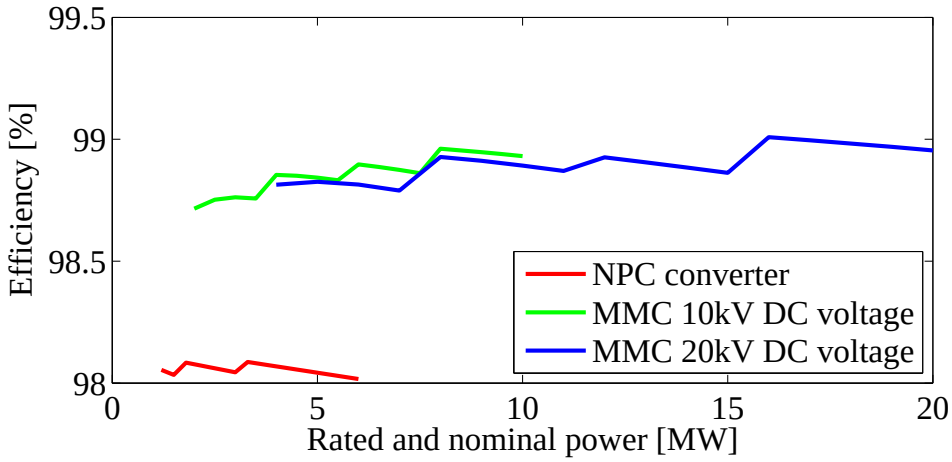


Figure 3.8: Converter efficiency vs. rated power for different voltage ratings, estimated using the methodology from [2].

The price of the IGBTs and cell capacitors are based on the available catalogue data (Dynex and NWL) [82, 83], while the price of the arm inductors is estimated on the basis of the current price of copper. An estimation of capacitors cost is 0.1 \$ per 1 μF for the film capacitor rated at 1 kV, which is suitable for the MMC cell capacitors. The converter hardware cost is estimated to be 30 % higher than the sum of all semiconductors and passive components. The manufacturing cost has not been considered.

From section 4.5 (4.38), it can be concluded that the energy stored in the cell capacitors (E_{stored}) is proportional to the converter power (P_{rat}), meaning that the energy stored in all converters in the system would be proportional to the overall rated power. In that sense, if the price of capacitors is proportional to the energy stored in them, the price of all cell capacitors in the system should be similar regardless of the converter power and voltage ratings, when MMC based solutions are considered. The differences come due to the converters overrating (to provide redundancy) and availability of only discrete values of capacitances (E12 series). Similar conclusions can be drawn about the energy stored in the arm inductors, where arm inductance is given by (4.40). The nominal current of an arm inductor is one third of the DC

current, so the nominal energy stored in arm inductors is given by:

$$6 \cdot E_{arm} = \frac{6}{2} L_{arm} (\frac{I_{DC}}{3})^2 \approx \frac{1.3}{3} k_1 \frac{{V_{DC}}^2 \cdot {I_{DC}}^2}{P_{rat}} = k_2 \cdot P_{rat} \tag{3.6}$$

Where k_2 is a constant parameter. Considering this, the energy stored in all the inductors of all MMCs in the system would be proportional to the system rated power, and it should not vary with the converter ratings. However, some differences in the inductor prices are present as a consequence of the inductor designs and converter overrating.

3.5 Power system optimisation

The power system is optimised to ensure the best trade-off between system efficiency, cost and accelerator availability. The solution should be feasible, i.e. within technical constraints, such as maximum fault currents, maximum cable cross sections, etc.

The power system optimisation diagram is presented in Fig. 3.9. At the initial stage topological selections to satisfy the basic requirements at the grid and modulators sides were made. This selection includes the the design rules and considerations presented in section 3.4. Then, the first verification of the system is done by observing the system availability, efficiency and fault currents, for the first three candidate structures from Table 3.2, as presented in [69]. For the purpose of validating the power system performance, the models from section 3.4 are used, and the system is described for all possible voltages and quantity of power system components. All possible number of outdoor substations, MV bus bars, HV/MV transformers, LMV bus bars, MV/LMV transformers and converters that satisfy the maximum bus bar currents, transformer power ratings and converter current ratings were considered. Here the maximum bus bar current is set to 3 kA.

The analysis of the maximum fault currents at MV and LMV bus bars, has shown that there is a minimum required number of HV/MV transformers and minimum required LMV voltage, in order to limit the fault currents to 20 kA. Figs. 3.10 and 3.11 present

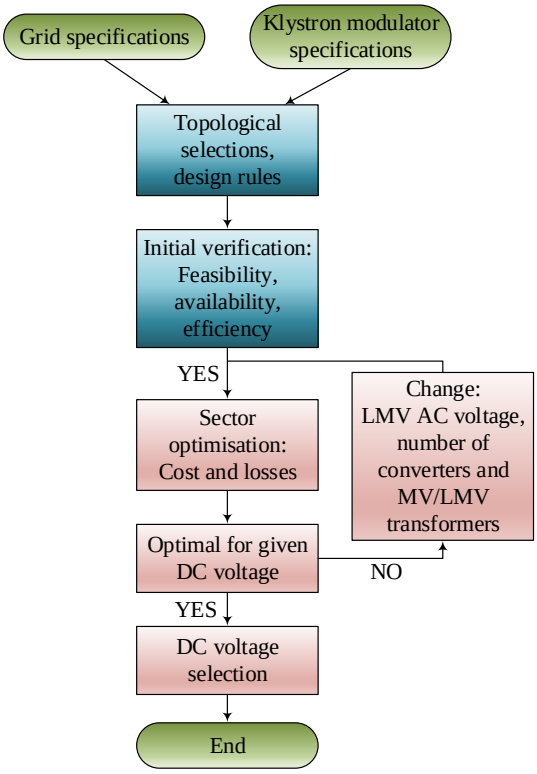


Figure 3.9: Power system optimisation diagram.

maximum fault currents for different power system structures delivering 10 kV and 20 kV DC voltage. Note that in Figs. 3.10 and 3.11 all generated possibilities relate to one, two, three or four HV outdoor substations, depending on the number of MV bus bars (4 MV bus bars can correspond to either 1, 2 or 4 outdoor substations). All the solutions with the LMV being 3.3 kV have maximum fault current above 24 kA, while for the other two cases, the possible number of HV/MV transformers (and MV bus bars) is 6 and 7. In the case of LMV bus bars voltage of about 6 kV, two LMV bus bars are needed to transmit the power associated to one MV bus bars. In the case of 10 kV LMV bus bars, one MV bus bar feeds one LMV bus bar.

The next stage of the power system optimisation from Fig. 3.9 is the sector optimisation with the goal to minimise the cost and the losses. At this point either 6 or 7 sectors can be selected, starting with the MV bus bars and delivering power to the

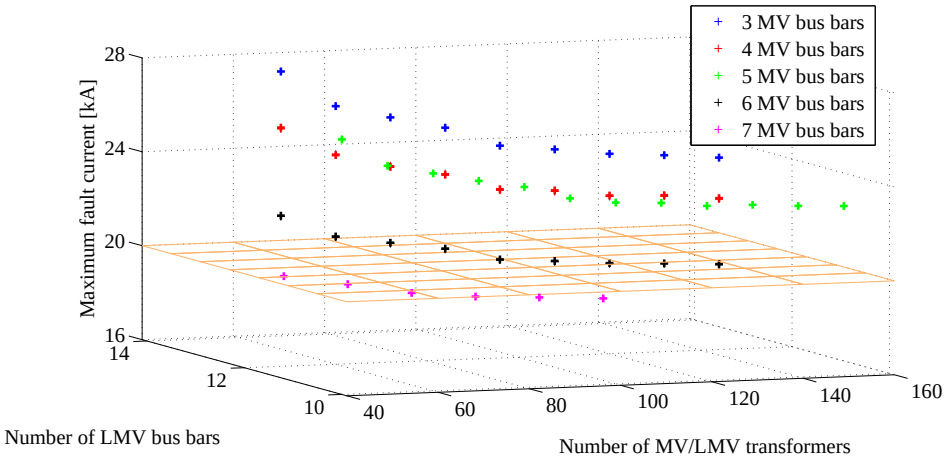


Figure 3.10: Maximum fault currents in the case of LMV at 6 kV and the final DC voltage about 10 kV.

corresponding number of klystron modulators. The number of sectors is selected to be 6, since it can be realised in more ways (1, 2 or 3 outdoor substations). Having 7 sectors would involve the same optimisation procedure and lead to similar optimisation results. Two different sector architectures are possible due to the two different DC voltage ranges, as presented in Fig. 3.12.

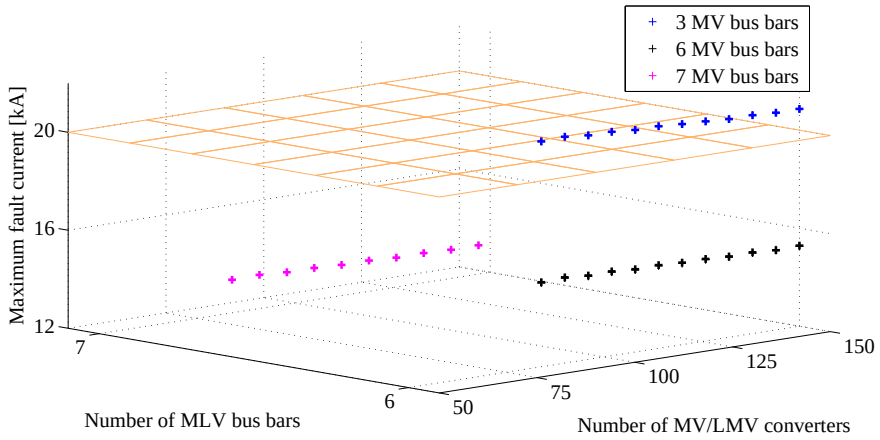


Figure 3.11: Maximum fault currents in the case of LMV at 10 kV and the final DC voltage about 20 kV.

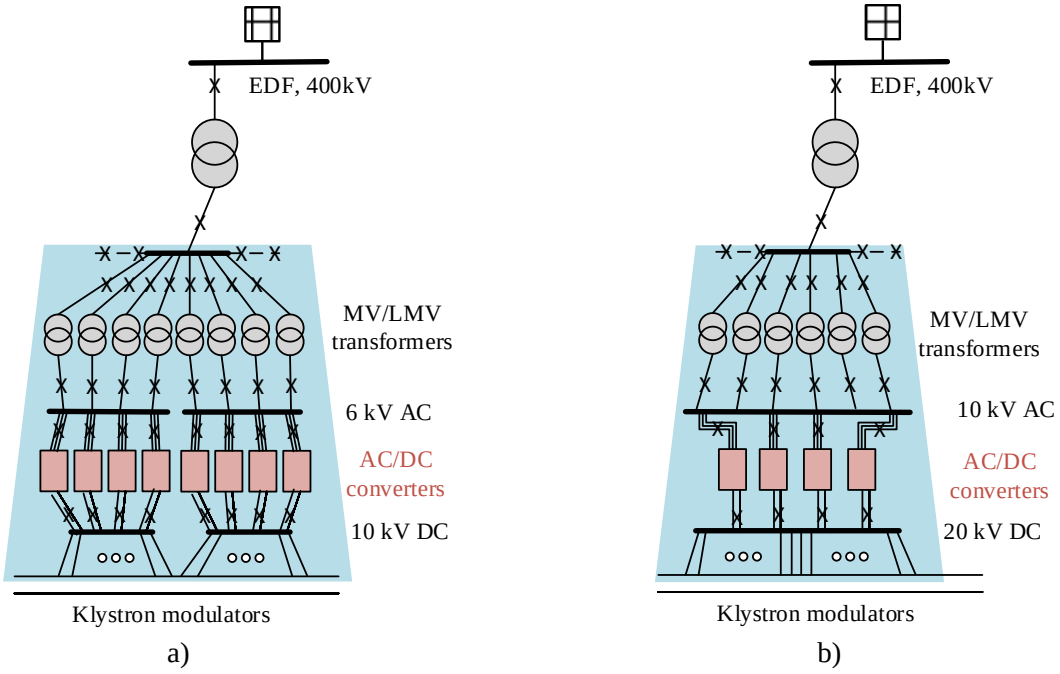
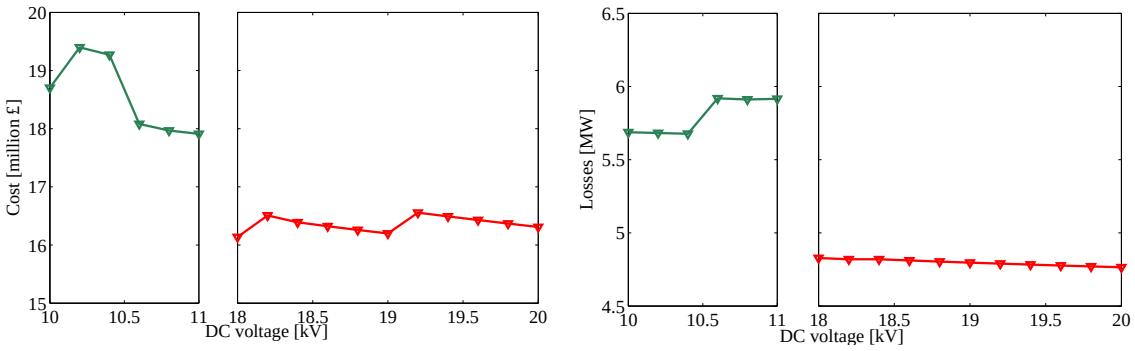


Figure 3.12: Two different sector architectures delivering a) 10 kV, b) 20 kV DC voltage.

Both price and losses should be minimised, so they are both normalised with their

minimum values for the given voltage range and then weighted with the same coefficient. For each of the possible MLV and DC voltage levels, the optimal number of transformers and converters is selected. The losses are estimated on the bases of losses and efficiencies of power system components as presented in section 3.4. Cost models of power system components are also presented in section 3.4, while the cost of the civil engineering is based on the CERN internal data and assumptions of the converters, switchgears, and transformer sizes, as presented in Appendix A. Cost of the bus bars or enclosed switchgears was not included in the optimisation (the data was not available).

Fig. 3.13 shows optimisation results in terms of cost and losses of all 6 sectors, as a function of the final DC voltage level. The DC voltages between 11 and 18 kV are not observed, since there are no suitable cable and switchgear options for both LMV and DC voltage (Table 3.1).

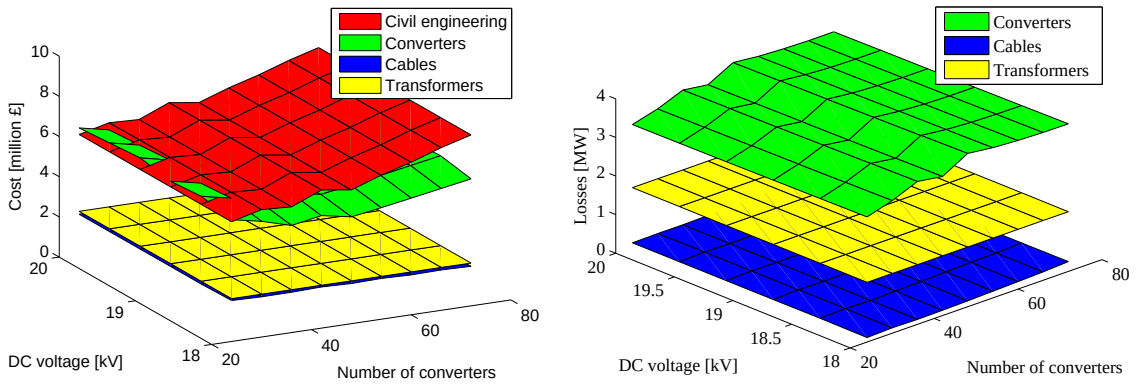


(a) (b)

Figure 3.13: Total a) cost and b) losses of the 6 sectors optimisied to deliver specified DC voltage bellonging to the 10 kV (green) and 20 kV (red) voltage range.

As presented, both cost and losses are lower in the higher voltage range, i.e. when the DC voltage is from 18 to 20 kV (22 kV cables), when compared to lower voltage range (DC voltage between 10 and 11 kV, corresponding to 12 kV cables). In the higher voltage range, the optimal number of converters is 24 yielding that one DC bus bar is fed by 4 converters and it supplies about 220 modulators. Each converter is rated

at 16.6 MW and nominally operates at 12.5 MW. In the higher voltage range, the influence of the DC voltage and number of converters on overall cost and losses in the case of 36 MV/LMV transformers and fixed LMV voltage at 10.5 kV is presented in Fig. 3.14.



(a) (b)

Figure 3.14: Break down of the total a) cost and b) losses of the 6 sectors vs. the DC voltage and number of converters.

Fig. 3.14 indicates that most of the power system cost is in the converters and civil engineering, and the number of converters influences both the power electronics and civil engineering cost, while the influence of the DC voltage is not significant. The majority of losses also relates to converters, followed by the losses in the MV/LMV transformers. Having the DC voltage set at 20 kV, and the number of converters to 24, the overall system losses are estimated to be 6.9 MW, corresponding to the efficiency of 97.7 %. The break down of the losses is given in Table 3.4.

Table 3.4: Break down of the overal power system losses.

Losses	HV/MV transformers	MV/LMV transformers	Converters	Cables	**Total**
Absolute [MW]	1.5075	1.5472	3.1814	0.6592	6.8953
Relative	0.005	0.0052	0.0106	0.0022	0.023

In the presented optimisation algorithm, the cost and losses of the load, i.e. klystron modulators, were not taken into account. As previously mentioned the DC voltage droop ΔV is limited to 1 kV, due to the compensation limits of the active bouncer [9]. To limit the droop to the absolute value of 1 kV different sizes of the main capacitor banks at the modulator inputs are required in the cases of the DC voltage being around 10 kV and 20 kV. The required energy to be stored in the main DC capacitor bank is discussed in [84]. The capacitance of the main bank (converter output capacitance) required to limit the voltage droop to the value of ΔV is given by:

$$C_{DC} = \frac{P_{rat} \cdot T_{rep}}{\Delta V \cdot V_{DC}} \tag{3.7}$$

where T_{rep} is the load pulse repetition frequency. The required energy to be stored in the main capacitor bank, is therefore given by:

$$E_{DC} = \frac{P_{rat} \cdot T_{rep}}{2 \cdot \Delta V} \cdot V_{DC} \tag{3.8}$$

From (3.8), assuming the same load profile, rated power and DC voltage droop (1 kV), the case with the DC voltage range of 20 kV requires almost twice as much energy to be stored in main capacitor as the solution with the DC voltage range of 10 kV. Therefore, an increase in cost of the main capacitor bank is expected. However, the capacitor bank is assumed to be a part of the klystron modulators, and their size should be optimised when the moduator is optimised, i.e. pulsed isolated transformer, disconnector switch, active bouncer, etc. In [84], the size of the main capacitor bank and the DC voltage droop is analysed from the aspect of the power electronics and reducing AC power fluctuation. The analysis in [84] indicates that the AC power quality is similar in the cases of 10 kV and 20 kV DC voltage MMC only if the size of the relative voltage droop is the same. In the case of fixed relative voltage droop, for instance to 10 % of the nominal DC voltage, the energy stored in the main capacitor bank is the same (3.8).

3.6 Summary

The power system optimisation requires respecting both the grid requirements and the klystron modulator requirements. The grid connection is at the transmission voltage level, while the klystron modulators require DC voltage in a medium voltage range. Therefore, this chapter presented a generlised approach to the power system design, analysing potential converter topologies, and power system architectures. Additionally, the possibilities for the intermediate voltage levels and the final DC voltage levels were analysed. An optimisation goal to achieve the specified power system functionalities while optimising the parameters such as cost and losses was set. The optimisation required multiple stages to narrow the scope of possible solutions, on which the final cost and losses optimisation is performed.

The optimisation is based on the available data on the power system components, as well as experiences and design practices from CERN. It is based on many assumptions, and therefore the presented results are not absolute, but rather approximated values. The power electroncs contribute to the majority of system losses and cost and they were analysed in more detail [84]. Improved optimisation results could be obtained by using more detailed models of the power system components (which were not available during the scope of the study). Additionally, including the prices of bus bars, breaking equipment or switchgears in the optimisation might affect the final result.

The presented optimisation results however, favour multilevel topologies due to their high efficiency, contributing to high overal efficiency. In addition, the highest possible DC voltage level was selected as the most suitable, while the minimum cost and losses are obtained with the smallest number of converters (highest possible power). Therefore, the modular multilevel converter, with the ratings from Table 3.5 is selected for further analysis. This includes the design of the control approach for the MMC under pulsed DC load, presented in Chapter 5, as well as verification by the simulation (Chapter 6) and experimentally (Chapter 8). An important part of the following work deals with minimising the AC power fluctuation, on which the feasibility of the single-

stage power system architectures considered is critically dependent.

Table 3.5: Modular multilevel converter ratings.

Variable	**Value**
DC voltage	20 kV
AC voltage	10.5 kV
Rated power	16.6 MW
Num of cells per arm	20

Chapter 4

Modular multilevel converter

4.1 Introduction

This chapter focusses on the modular multilevel converter, in the form presented in [44, 2]. In the previous chapter, the MMC has been recognised as the most suitable candidate for the specified application. Therefore, the following section highlights the features of the selected topology. The third section presents modulation methods suitable for all multilevel topologies, using the example of an MMC where the modulation algorithm provides gating signals for all the cells in a chainlink based on the chainlink voltage reference. The selected modulation method ensures the capacitor voltages balance for the cells within a chainlink. The fourth section presents converter models and equations that are useful for understanding the converter operation and also for designing the control loops in Chapter 5. Finally, the sizing of the passives, such as arm inductors and cell capacitors, is explained.

4.2 MMC features

Each MMC phase leg consists of two arms of cascaded submodules connected in series with a small inductor, as shown in Fig. 4.1. For the purpose of this analysis the phase and arm inductors are assumed to be ideal, i.e. any resistance is neglected since it is not relevant for the analysis. The switching cell (submodule) in such a converter is a simple half bridge converter (shown in Fig. 4.1) using a capacitor as a storage element. Assuming the number of cells in one arm is N ($2 \cdot N$ cells in one phase), depending on a modulation method, $(N + 1)$ or $(2 \cdot N + 1)$ voltage levels can be generated in the phase voltage waveform [85]. Each cell capacitor can be included in the current path ($S_1 = 1$ and $S_2 = 0$) yielding a cell voltage equal to the cell capacitor voltage, or excluded from the current path ($S_1 = 0$ and $S_2 = 1$) when the cell voltage is zero.

Some of the most important features of the MMC are listed below:

- *It can be extended to any number of levels* - converter arms can comprise any number of submodules connected in series. The high number of levels gives the possibility to decrease the switching frequency (even to the fundamental), while maintaining good AC waveform quality and harmonic performance. The only limitation is the increase of control complexity in terms of signals to be processed and generated. To cope with this issue, in terms of converter simulation, various methods to reduce the simulation time are proposed [86]. In terms of experimental prototypes there are several reported methods to estimate cell capacitor voltages in order to reduce the number of sensors [87, 88]. Additionally, the control of a high voltage MMC can use a distributed architecture, where submodules have their local control unit and health monitoring that works together with the centralised controller (master) [89].

- *High efficiency* - Low switching frequencies can be used due to the large number of levels. The overall converter efficiency is estimated to be higher than 98 % for a full scale implementation [2].

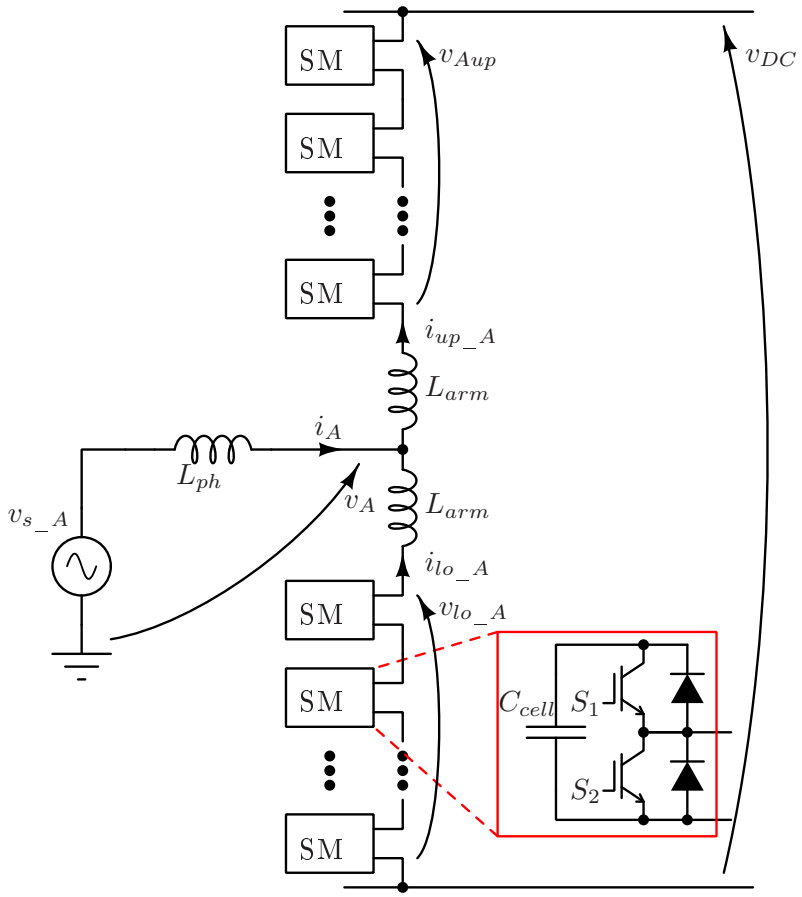


Figure 4.1: A single-phase representation of a modular multilevel converter.

- *High availability, modularity, redundancy* - the converter utilises identical submodules, based on low voltage proven semiconductor devices. Due to the modular stricture, additional modules can be added to increase the converter redundancy [53]. In the case of module failure, that module can be bypassed and repaired without interrupting converter operation.

- *Internal arm currents are not chopped but continuous* - The arm currents comprise both a DC and a fundamental component part [30], with low $\frac{di}{dt}$. Note here that high $\frac{di}{dt}$ is contained within a submodule, which with the proper design mitigates the EMI problems. Both arm currents quantities can be controlled [45, 90, 91].

- *Voltage balancing can be done with slower dynamics than the converter control*

- The balancing is done on much larger time scale than the sampling period and the current control time constant.

- *There is no need for a bulk DC link capacitor* - Both DC voltage and current are smooth, therefore there is no need for additional filters. However, in the specified application, the klystron modulators require input DC bus capacitors in order to limit the voltage droop to a values that can be compensated by the active bouncer circuit [9].

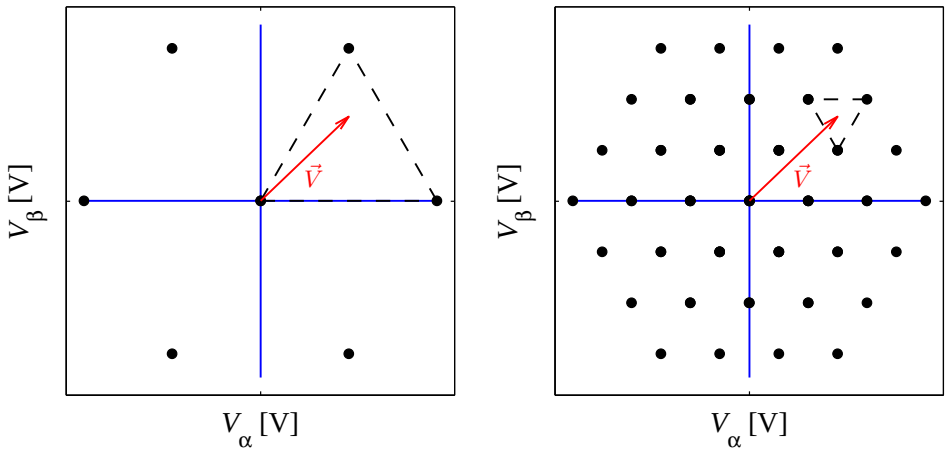
The following sections give an overview of how it is possible to achieve the aforementioned characteristics. To fully understand the converter behaviour and internal and external waveforms, modulation methods and converter models for different purposes are presented in detail.

4.3 Modulation methods

Modulation techniques are a mechanism for appropriate control of the switches (signals S_1 and S_2 of each cell) that will enable the AC voltage to follow the reference provided by the converter control algorithm. Assuming the switch control signals for one cell are represented as binary values (S_1 and S_2, Fig. 4.1), they should be complementary ($S_1 = \overline{S_2}$). Only one of them completely describes whether the cell capacitor is included or excluded from MMC current path, thus the modulation strategy should provide one control signal for each converter cell. Of course, in practice, a small deadtime ($S_1 = 0$ and $S_2 = 0$) must be inserted to avoid shoot through. However, for the purposes of analysis, the influence of that is assumed to be negligible.

4.3.1 Background on classic multilevel modulation methods

Classification of modulation techniques for cascaded multilevel inverters is presented in [10, 92, 93]. These modulation techniques can be applied to all cascaded multi-



(a) Two-level (b) Four-level

Figure 4.2: SVM diagram for three-phase converter.

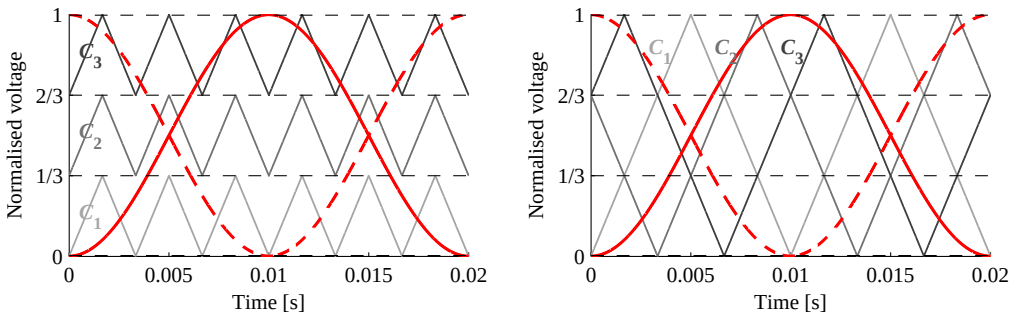
level converters, with small variations in the switch control signal generation. Selective harmonic elimination (SHE) and staircase modulation are techniques that provide switching at the fundamental frequency (frequency of the reference). The SHE method involves pre-calculation of the turn-on angles of the switches that optimise the harmonic profile of the AC voltage. The staircase method is also referred to as nearest level control (NLC) and it considers simple comparison of the reference with the possible voltage levels, giving the control signals that provide a voltage level closest to the reference level. Carrier based modulation techniques and multilevel space vector modulation (SVM) operate at higher frequencies than fundamental frequency. SVM for multilevel 3-phase converters works on the same principle as for the case of SVM for 2-level 3-phase converters, but the number of possible switching vectors (states) increases, together with the number of sectors. This is illustrated with Fig. 4.2 for 2-level and 4-level converters. SVM is a common modulation technique for industrial a 2- and 3-level converters, however its application has spread to multilevel topologies with a growth of microprocessor capability. SVM has the potential of exploiting redundant voltage levels present in multilevel topologies [11], for instance for the purpose of controlling the common mode voltage [29].

Carrier based modulation techniques relay on the pulse width modulation (PWM) principle, where the switching signal sequence is obtained by simple comparison of carriers and reference signals. In general, there is one reference signal for a chainlink and one carrier signal per converter cell. Since the MMC has two arms in each leg, the modulation strategy can be achieved with two reference signals and N carriers.

Carrier based techniques can be further divided into those with level-shifted and phase-shifted carriers. Level-shifted carrier based PWM for MMC has N level-shifted carriers, with an amplitude equal to $\frac{1}{N}$, that completely cover the range of 0 to 1 (or the carrier amplitude can be 1, covering range 0 to N, in the case of that convention). Reference signals are typically sinusoidal signals with the DC offset normalised to fit the range of 0 to 1. Depending on the phase shift among the level-shifted carriers there are three types of level-shifted PWM technique: in phase disposition (PD), phase opposite disposition (POD) and alternate phase opposite disposition (APOD) [10]. PD level-shifted PWM is illustrated in Fig. 4.3(a) in the case of a four-level MMC (3 cells in a chainlink) with two reference signals and three carriers. The carriers C_1, C_2 and C_3 correspond to first, second and third cell in a chainlink (upper and lower arm), respectively. If the reference is higher than the carrier of each cell, the capacitor of that cell should be included in the circuit. Based on the amount of switching events occurring, the equivalent (average) cell switching frequency is N times lower than the carrier frequency.

Phase-shifted carrier based PWM considers N phase-shifted carriers, amplitude equal to 1, covering the range from 0 to 1 (again the convention can be that the carriers cover the range from 0 to N). Each carrier corresponds to one cell and the phase shift between them is $\frac{2\cdot\pi}{N}$ rad. Phase-shifted carrier based modulation for a four-level MMC is illustrated in the Fig. 4.3(b). The three carriers correspond to the three cells in each arm. The control signal generation is provided by a simple comparison of each cell carrier and the reference. In this case the equivalent switching frequency of each cell is equal to the carrier frequency.

For the same equivalent switching frequency of a converter cell when carrier-based



(a) Level-shifted (b) Phase-shifted

Figure 4.3: Carrier based modulation technique for 3 cell per arm MMC, where full line presents the reference for the lower arm, whist the dashed line reference signal is a reference of the upper arm.

methods are applied (N times higher switching frequency of the level-shifted carriers when compared to phase-shifted) the PD level-shifted carrier method performs the best in terms of waveform harmonics [93]. The phase-shifted carrier based modulation produces identical AC waveform as APOD level-shifted carriers modulation. However, in terms of capacitor voltage balancing, phase-shifted and level-shifted carrier based PWM algorithms perform very differently. If we focus on one chainlink at Fig. 4.3(a), the first cell (corresponding to C_1) will be included in the current path for the majority of the reference period, while the third (C_3) will be excluded from the current path for the majority of the time. At the same time, from Fig. 4.3(b) it can be seen that all cells will be included/excluded from the current path more uniformly. Therefore, the phase-shifted carrier based algorithm provides more uniform switching of the cells, leading to natural cell capacitor voltage balancing in the case of the FC and CHB converter [18, 94], while the level-shifted algorithm requires capacitor voltage balancing.

4.3.2 Modulation methods for MMC

The previously described modulation techniques are applicable for all multilevel topologies, and are therefore applicable to the MMC. Which modulation technique is most appropriate in a given situation depends on a specific application requirements and the MMC characteristic.

Although the MMC was first proposed together with SVM [29], this kind of modulation is not commonly applied to the MMC. The number of sectors dramatically increases with the number of levels, making the sector identification computationally demanding. Therefore, SVM is applied to the MMCs with low number of levels, typically used in low and medium voltage applications [95]. Additionally, there are methods for optimised selection of the sectors, and one of them is a generalised space vector modulation method that provides some flexibilities in control implementation [96].

A review of the most commonly used modulation techniques for the MMC is presented in [53]. Those are carrier based and low frequency methods and require some modification specific for the MMC. Phase-shifted and level-shifted carrier based modulation techniques require capacitor voltage balancing. In [31], a level-shifted carrier based method with an integrated capacitor voltage balancing algorithm is proposed. The algorithm suggests that the level-shifted carriers are used to determine the insertion index of an arm, being the sum of all control signals generated by the comparison of reference and carriers. Based on the arm current sign the capacitors are sorted in ascending or descending order and according to the insertion index, specific cells capacitors are selected to be included/excluded in/from the current path. This way, during one switching period, some cells are included in the current path, some cells are excluded, while only one cell performs PWM. The same principle in [97] is referred to as a nearest level and PWM (NLC+PWM) control. In that case, the nearest (lower) integer to the insertion index is the number of cells to be included and the residue of the insertion index is used as a duty-cycle of the cell performing PWM. Another alternative of this algorithm is presented in [98] where based on the sorting

order of the cell capacitor voltages, carriers from 4.3(a) are dynamically assigned to different cells in the chainlink.

NLC and SHE methods switch each cell at the fundamental frequency and therefore have reduced switching losses. The NLC typically induces low frequency switching harmonics in the output waveform, but the spectrum improves with the number of levels [97]. Therefore, in the case of an MMC with a high number of levels, a good waveform quality is guaranteed even when the switching is performed at the fundamental frequency. In [99] an overview of low switching frequency modulation methods is presented. SHE methods can cancel some of the low frequency harmonics or optimise other parameters such as THD, switching losses, etc. [99]. SHE methods are applied to the MMCs with a target to provide capacitor voltage balancing while canceling low order harmonics in the AC waveforms [100].

Sorting algorithms are used in conjunction with level-shifted carrier based algorithm and nearest level control [97] to provide cell capacitor voltage balancing. In both cases, there are issues with unnecessary switching occurring with rotation of the cells at every update of the voltage reference. This occurs when the insertion index does not change much (integer part unchanged), but the cell that performs PWM and the cells that are included in the current path are changed, in order to perfectly balance cell capacitor voltages. There are various ways to reduce the unnecessary switching while maintaining capacitor voltage balancing and good AC waveforms. Some of those methods are presented in [53], and they include sorting the cell capacitor voltages of only a portion of the cells [101], capacitors voltage ripple control [102], less frequent sorting of all the cell capacitor voltages [98], etc.

All of the carrier based algorithms produce $(N + 1)$ levels in the chainlink voltage, however, in the case of PD level-shifted carriers, the converter AC waveform has $(2 \cdot N + 1)$ levels, while in the case of APOD (or phase-shifted carriers) the number of levels is $(N + 1)$ [85]. Therefore, using PD enhances the AC waveform quality while increasing the harmonic content in the DC current (and circulating currents).

Phase-shifted carrier based modulation can be used in the case of distributed control, since the specific carrier is always related to the specific converter cell [53, 97]. However, in the case of an MMC, natural balancing of the cells capacitors does not occur, requiring a balancing algorithm. In the case of phase-shifted carrier based modulation implemented on the local cell controller, each cell has its own voltage reference, including the AC part, DC part, arm balancing part and internal cell capacitor voltage control part [46, 96]. Phase-shifted carriers of one arm cover a $2 \cdot \pi$ rad angle, but their distribution in this region does not need to be fixed (such as a phase shift of $\frac{2 \cdot \pi}{N}$ rad among subsequent cells). In [98] a dynamic allocation of the phase-shifted carriers is suggested in order to provide voltage balancing, in the case of centralised MMC control.

A scaling of the arm or cell reference has to be done in order to bring the maximum reference level to the maximum carrier level in the case of carrier based modulation techniques. Similarly, the reference has to be scaled to get the insertion index to fit the range 0 to N in NLC techniques. In the case of an MMC the reference and the carriers can be scaled to belong the 0 - 1 region, but they can also be scaled to belong to 0 - N region. The first case is typically used for distributed phase-shifted carrier based control, where the cell reference is normalised with the cell capacitor voltage. In the second case, the insertion index is a reference for the N level-shifted carriers covering 0 - N region, or it can be rounded to select the number of included cells in NLC. To fit this region, the arm reference is normalised with the average cell capacitor voltage (of all cells in that arm). Normalisation can be performed as a division with the nominal cell voltage value, or with the cell capacitor voltage measurements, or with a hybrid of the two accounting for the low harmonic ripple present in the cell capacitor voltages. Normalisation with the cell capacitors voltage measurement (the average of all chainlink cells) is classified in [53] as a closed-loop control that must be applied together with the arm balancing methods.

In this thesis, the NLC+PWM (or level-shifted carrier based method with sorting of cell capacitor voltages) is applied [31, 97] and it allows cell capacitor voltage balancing. The modulation method is illustrated in Fig. 4.4 for the upper arm phase A chainlink.

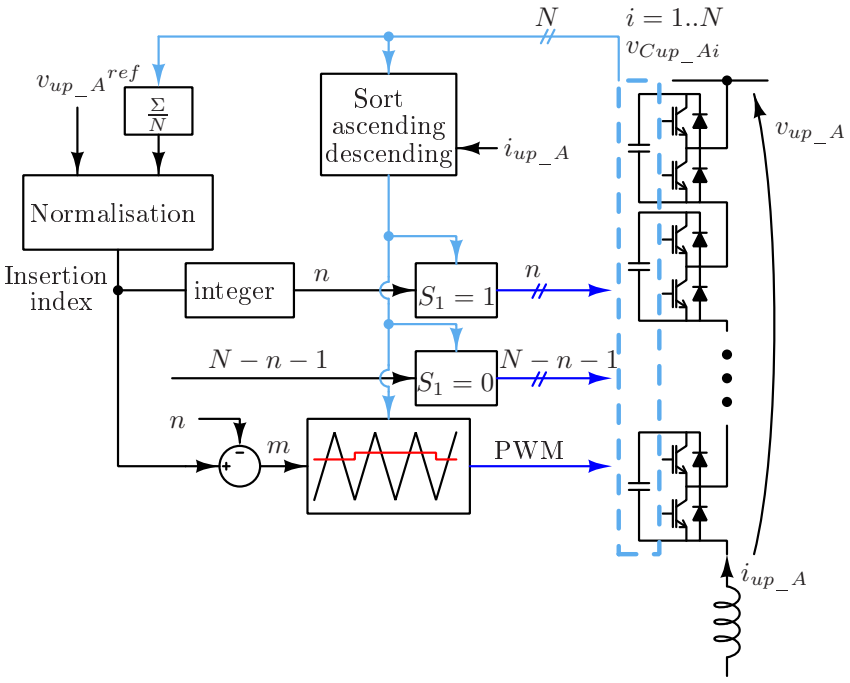


Figure 4.4: Modulation algorithm with cell capacitor voltages balancing feature, on the example of the upper arm chainlink of phase A.

In order to reduce unnecessary switching, the sorting is performed every N carrier frequency cycles, to comply with the equivalent switching frequency being N times lower in the case of level-shifted carrier based modulation. Since the carriers are in phase, a $(2 \cdot N + 1)$ level is generated in the AC waveform. The scaling of the reference signal is done to fit the region of 0 to N, by normalising the arm reference with the average of the measured cell capacitor voltages within that arm.

4.4 Converter models

Fig. 4.5 presents a simplified diagram of a grid connected modular multilevel converter. Each converter phase has upper and lower arms, made up of MMC chainlinks

(half-bridges connected in series) and an arm inductor L_{arm}. The half-bridge cells store a certain amount of energy in the cell capacitance C_{cell}. Controllable voltage sources in Fig. 4.5 represent the chainlink voltages.

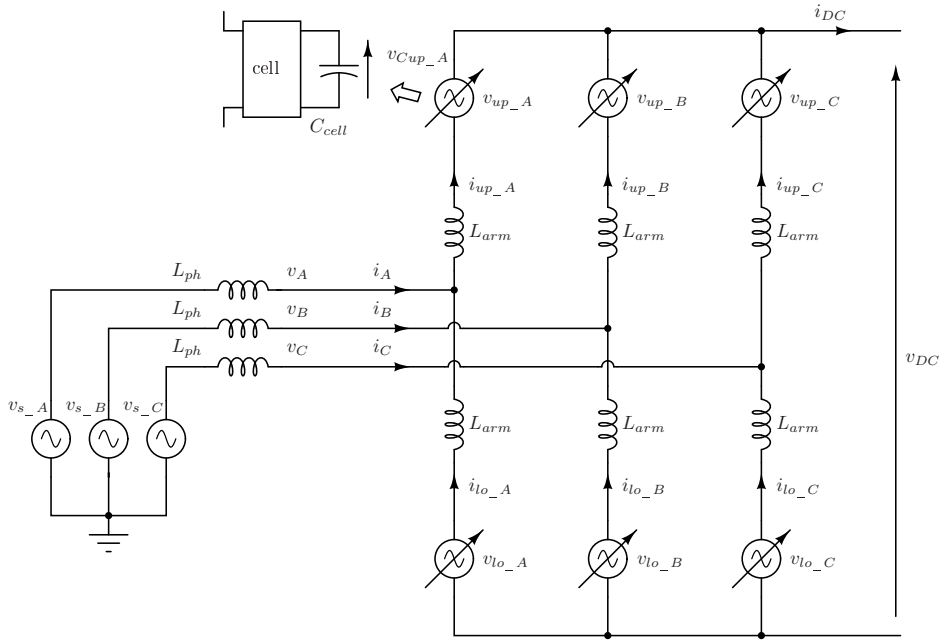


Figure 4.5: Grid connected MMC simplified schematics.

Seen from the AC side, the relation between phase current and voltage is given by:

$$v_{A,B,C}(t) = v_{s\_A,B,C}(t) - L_{ph}\frac{di_{A,B,C}(t)}{dt} \tag{4.1}$$

where L_{ph} is phase inductance, $v_{s\_A,B,C}(t)$ is phase voltage (A, B or C) at the point of common coupling (source/grid), $i_{A,B,C}(t)$ is source and converter AC current, and $v_{A,B,C}(t)$ is the converter phase (A, B or C) voltage. The phase current is divided between the upper and lower arms as described by:

$$i_{A,B,C}(t) = i_{up\_A,B,C}(t) - i_{lo\_A,B,C}(t) \tag{4.2}$$

At the same time the DC current is related to the upper and lower arm currents as described by:

$$i_{DC}(t) = i_{up\_A}(t) + i_{up\_B}(t) + i_{up\_C}(t) = i_{lo\_A}(t) + i_{lo\_B}(t) + i_{lo\_C}(t) \tag{4.3}$$

where $i_{DC}(t)$ denotes converter DC current. The amount of the current that each phase contributes to the DC current together with the current that circulates among phases is called the circulating or differential current. The circulating current is fictitious current calculated as:

$$i_{circ\_A,B,C}(t) = \frac{i_{up\_A,B,C}(t) + i_{lo\_A,B,C}(t)}{2} \tag{4.4}$$

In the literature there are two conventions about the circulating current, one considers only the current circulating among phases without contributing to the DC current [31, 53, 86], while the other is as previously defined by (4.4) and will be used in this thesis [45, 103, 104].

Ideally, the AC current is evenly shared between the upper and lower arms, while the DC current is evenly shared between the phases. In that case the arm currents have an equal DC component, as described by equations (4.5) and (4.6):

$$i_{up\_A,B,C}(t) = i_{circ\_A,B,C}(t) + \frac{1}{2}i_{A,B,C}(t) = \frac{1}{3}i_{DC}(t) + \frac{1}{2}i_{A,B,C}(t) \tag{4.5}$$

$$i_{lo\_A,B,C}(t) = i_{circ\_A,B,C}(t) - \frac{1}{2}i_{A,B,C}(t) = \frac{1}{3}i_{DC}(t) - \frac{1}{2}i_{A,B,C}(t) \tag{4.6}$$

Here the assumption that the part of arm currents that circulates among phases is zero is made.

The converter AC voltages are described by equations (4.7) and (4.8):

$$v_{A,B,C}(t) = {v_{DC}}^{+}(t) - v_{up\_A,B,C}(t) + L_{arm}\frac{di_{up\_A,B,C}(t)}{dt} \tag{4.7}$$

$$v_{A,B,C}(t) = {v_{DC}}^{-}(t) + v_{lo\_A,B,C}(t) - L_{arm}\frac{di_{up\_A,B,C}(t)}{dt} \tag{4.8}$$

where ${v_{DC}}^{+}(t)$ denotes positive potential of the DC voltage, and ${v_{DC}}^{-}(t)$ denotes negative potential of the DC voltage, i.e. $v_{DC}(t) = {v_{DC}}^{+}(t) - {v_{DC}}^{-}(t)$. It is assumed that, due to the symmetry, only switching frequency components exist between the central point of the DC link and the supply neutral, as given by:

$${v_{DC}}^{+}(t) = -{v_{DC}}^{-}(t) = \frac{v_{DC}(t)}{2} \tag{4.9}$$

By adding (4.7) and (4.8) and substituting (4.2), the following relation applies:

$$v_{A,B,C}(t) = \frac{v_{lo\_A,B,C}(t) - v_{up\_A,B,C}(t)}{2} + \frac{L_{arm}}{2}\frac{di_{A,B,C}(t)}{dt} \tag{4.10}$$

When (4.7) and (4.8) are subtracted and (4.4) is applied, the DC voltage is derived:

$$v_{DC}(t) = v_{up\_A,B,C}(t) + v_{lo\_A,B,C}(t) - 2 \cdot L_{arm}\frac{di_{circ\_A,B,C}(t)}{dt} \tag{4.11}$$

By combining (4.1) and (4.10), the half of the difference of upper and lower arm voltages is derived:

$$\begin{aligned}\frac{v_{lo\_A,B,C}(t) - v_{up\_A,B,C}(t)}{2} &= v_{s\_A,B,C}(t) - (L_{ph} + \frac{L_{arm}}{2})\frac{di_{A,B,C}(t)}{dt} \\ &= v_{AC\_A,B,C}(t)\end{aligned} \tag{4.12}$$

and assigned to the new variable $v_{AC\_A,B,C}$.

Similarly, the sum of upper and lower arm chainlink voltages, is given by:

$$v_{lo\_A,B,C}(t) + v_{up\_A,B,C}(t) = v_{DC}(t) + 2 \cdot L_{arm}\frac{di_{circ\_A,B,C}(t)}{dt} = v_{DC\_A,B,C}(t) \tag{4.13}$$

and assigned to a variable $v_{DC\_A,B,C}$.

Equations, (4.12) and (4.13) represent a decoupled AC and DC side converter model, used to develop AC and DC (circulating) current controllers. Considering those equations, the upper and lower arm voltages are typically represented by equations (4.14) and (4.15):

$$v_{up\_A,B,C}(t) = \frac{v_{DC\_A,B,C}(t)}{2} - v_{AC\_A,B,C}(t) \tag{4.14}$$

$$v_{lo\_A,B,C}(t) = \frac{v_{DC\_A,B,C}(t)}{2} + v_{AC\_A,B,C}(t) \tag{4.15}$$

The newly introduced variables $v_{AC\_A,B,C}$ and $v_{DC\_A,B,C}$ correspond to the AC and DC parts of the arm voltages for phase A, B or C. Generating the chainlink voltages couples the AC and DC side converter models, since the reference quantities for both sides contribute to the chainlink voltage.

4.4.1 Grid connected converter power

The grid voltages $v_{s\_A,B,C}$, in the case of grid represented as ideal voltage sources, contain only positive sequence 50 Hz voltages as given by:

$$\begin{aligned} v_{s\_A}(t) &= V_{sm} \cdot \sin(\omega \cdot t) \\ v_{s\_B}(t) &= V_{sm} \cdot \sin(\omega \cdot t - \frac{2 \cdot \pi}{3}) \\ v_{s\_C}(t) &= V_{sm} \cdot \sin(\omega \cdot t - \frac{4 \cdot \pi}{3}) \end{aligned} \tag{4.16}$$

where $V_{sm}(t)$ is peak grid phase to neutral voltage and $\omega = 2 \cdot \pi \cdot f$ is the grid radial frequency, corresponding to $f = 50\,\text{Hz}$ grid frequency.

Without loosing generality a phase shift of ϕ_i is assumed between source voltage and phase current. The phase currents are given by:

$$\begin{aligned} i_A(t) &= I_m \cdot \sin(\omega \cdot t + \phi_i) \\ i_B(t) &= I_m \cdot \sin(\omega \cdot t - \frac{2 \cdot \pi}{3} + \phi_i) \\ i_C(t) &= I_m \cdot \sin(\omega \cdot t - \frac{4 \cdot \pi}{3} + \phi_i) \end{aligned} \tag{4.17}$$

where $I_m(t)$ is peak phase current.

Converter AC power is equal to the sum of the powers delivered to each of the three phases. The instantaneous power delivered to phase A, is described by:

$$p_{s\_A}(t) = v_{s\_A}(t) \cdot i_A(t) = \frac{V_{sm} \cdot I_m}{2}(\cos(\phi_i) - \cos(2 \cdot \omega \cdot t + \phi_i)) \tag{4.18}$$

The average power is calculated as the mean value of the instantaneous power over the fundamental period T. The average power delivered from phase A is given by:

$$P_{s\_A} = \overline{p_{s\_A}(t)} = \frac{1}{T}\int_t^{t+T} p_{s\_A}(\tau) \cdot d\tau = \frac{V_{sm} \cdot I_m}{2}\cos(\phi_i) \tag{4.19}$$

Similarly, the instantaneous and average powers for phase B and C can be derived. The overall instantaneous power is constant, as given by:

$$p_{AC}(t) = \frac{3 \cdot V_{sm} \cdot I_m}{2}\cos(\phi_i) \tag{4.20}$$

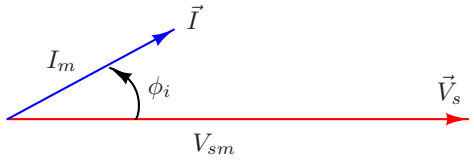


Figure 4.6: Voltage and current vector, with the phase shift displacement.

The average power is therefore equal to the overall instantaneous power:

$$P_{AC} = \overline{p_{AC}(t)} = p_{AC} \tag{4.21}$$

The average converter power is also called the active power or real power. If the voltage and current are represented as vectors (Fig. 4.6), the active power is calculated as a dot product of the two vectors:

$$P_{AC} = \frac{3}{2}\vec{I} \cdot \vec{V_s} = \frac{3 \cdot V_{sm} \cdot I_m}{2} \cos(\phi_i) \tag{4.22}$$

where $\vec{V_s}$ and $\vec{I}$ are voltage and current vectors with amplitudes V_{sm} and I_m, respectively. The phase displacement of the current ϕ_i is the phase shift between two vectors.

The reactive power is calculated as the cross product of the current and voltage vectors, thus the reactive power Q_{AC} is given by:

$$Q_{AC} = \frac{3}{2}\vec{I} \times \vec{V_s} = -\frac{3 \cdot V_{sm} \cdot I_m}{2} sin(\phi_i) \tag{4.23}$$

In the CLIC grid-interface application, the converter should draw only active power, while the reactive power should be zero. In that case the current and voltage vectors are aligned, i.e. the phase shift between them is zero. This guarantees the maximum power, for a given current amplitude, as described by:

$$P_{AC} = \frac{3 \cdot V_{sm} \cdot I_m}{2} \tag{4.24}$$

Since there is no phase shift in this case ($\phi_i = 0$), ϕ_i can be neglected from the previous equations. In that case, the current, grid voltage and converter voltage vectors, based

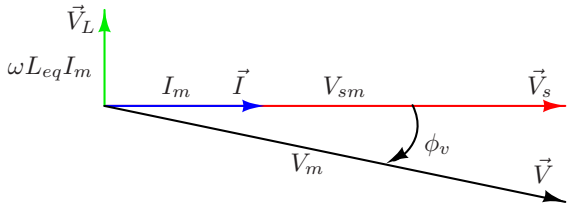


Figure 4.7: Phase current and grid and converter voltage vectors.

on equation (4.1), are presented in Fig. 4.7. The converter AC voltages measured with respect to the grid neutral, are given by:

$$\begin{aligned} v_A(t) &= V_m \cdot \sin(\omega \cdot t + \phi_v) \\ v_B(t) &= V_m \cdot \sin(\omega \cdot t - \frac{2 \cdot \pi}{3} + \phi_v) \\ v_C(t) &= V_m \cdot \sin(\omega \cdot t - \frac{4 \cdot \pi}{3} + \phi_v) \end{aligned} \tag{4.25}$$

The converter active and reactive powers are calculated as the dot and cross product of phase current and converter voltage, respectively:

$$P_{AC} = \frac{3}{2}\vec{I} \cdot \vec{V} = \frac{3 \cdot V_m \cdot I_m}{2} \cos(\phi_v - \phi_i) = \frac{3 \cdot V_m \cdot I_m}{2} \cos(\phi_v) \tag{4.26}$$

$$Q_{AC} = \frac{3}{2}\vec{I} \times \vec{V} = \frac{3 \cdot V_m \cdot I_m}{2} sin(\phi_v - \phi_i) = \frac{3 \cdot V_m \cdot I_m}{2} sin(\phi_v) \tag{4.27}$$

Since the inductor active power is zero (90° angle between voltage and current) the converter AC power should be equal the active power taken from the grid, and the converter reactive power should be opposite to the reactive power of the phase inductors. Considering equations (4.22) and (4.26) the relation between the converter and the grid peak voltage is given by:

$$V_m \cdot \cos(\phi_v) = V_{sm} \tag{4.28}$$

If ideal converter waveforms are assumed, the DC voltage and DC current are equal to their mean values. The DC side power is therefore given by:

$$p_{DC}(t) = v_{DC}(t) \cdot i_{DC}(t) = V_{DC} \cdot I_{DC} = P_{DC} \tag{4.29}$$

If the switches, cell capacitors, arm and phase inductors are assumed to be lossless, the AC and the DC powers are equal.

4.4.2 Energy stored in converter chainlinks

Each chainlink consists of N half-bridge cells with the cell capacitor as a storage element. The overall energy E_{cl} of a chainlink is given by:

$$E_{cl}(t) = \frac{1}{2} N \cdot C_{cell} \cdot v_C(t)^2 \tag{4.30}$$

where C_{cell} represents cell capacitance, and $v_C(t)$ is the average voltage on the cell capacitors within a chainlink. In general, the voltages on different cell capacitors of one chainlink are balanced if voltage balancing is included into the modulation strategy. The nominal cell capacitor voltage V_C in the MMC converter is N times smaller than the nominal DC voltage [29], as given by:

$$V_C = \frac{V_{DC}}{N} \tag{4.31}$$

The cell capacitor voltages oscillate during the period of the AC voltage, but the average value over a period, i.e. the mean value of the energy stored should be constant from period to period. Keeping the chainlink energy constant (the average cell capacitor voltages at the nominal value) is one of the control requirements, and it is ensured by maintaining zero average chainlink power. The relation between average chainlink power $P_{cl}(t)$ and change of average cell capacitors voltage is:

$$P_{cl}(t) = \frac{dE_{cl}(t)}{dt} = N \cdot C_{cell} \cdot v_C(t) \frac{dv_C(t)}{dt} \tag{4.32}$$

The instantaneous upper arm chainlink power $p_{up\_A,B,C}(t)$ is given by:

$$p_{up\_A,B,C}(t) = -v_{up\_A,B,C}(t) \cdot i_{up\_A,B,C}(t) \tag{4.33}$$

By substituting equations (4.5) and (4.14) in (4.33) and applying the averaging over the fundamental period, the average upper arm chainlink power, $P_{up\_A,B,C}$, is derived as:

$$\begin{aligned} P_{up\_A,B,C} &= -\overline{(\frac{v_{DC\_A,B,C}(t)}{2} - v_{AC\_A,B,C}(t))(i_{circ\_A,B,C}(t) + \frac{1}{2} i_{A,B,C}(t))} \\ &= -\overline{(\frac{V_{DC}}{2} - v_{AC\_A,B,C}(t))(\frac{1}{3} I_{DC} + \frac{1}{2} i_{A,B,C}(t))} \end{aligned} \tag{4.34}$$

Here, a constant value for the DC voltage and current are assumed. Also, if the circulating current is constant and equal to $\frac{1}{3}I_{DC}$, the DC part of the chainlink voltages, $v_{DC\_A,B,C}$, is equal to the DC voltage (4.13).

Equation (4.34) has 4 cross products, however, since $v_{AC\_A,B,C}$ and $i_{A,B,C}$ are 50 Hz sinusoids, only two cross products have a non-zero mean value. The average upper arm power is therefore computed as:

$$P_{up\_A,B,C} = -\frac{V_{DC} \cdot I_{DC}}{6} + \overline{\frac{1}{2} v_{AC\_A,B,C}(t) \cdot i_{A,B,C}(t)} \tag{4.35}$$

By substituting (4.12) in (4.35), and taking into account that there is no average power dissipation in the arm and phase inductor, the previous equation becomes:

$$\begin{aligned} P_{up\_A,B,C} &= -\frac{V_{DC} \cdot I_{DC}}{6} + \overline{\frac{1}{2} v_{s\_A,B,C}(t) \cdot i_{A,B,C}(t)} = \\ &= -\frac{P_{DC}}{6} + \frac{P_{AC}}{6} \end{aligned} \tag{4.36}$$

Based on this, the average upper arm power is equal to zero if the AC and the DC powers are equal. The average lower arm power is given by equation 4.37.

$$\begin{aligned} P_{lo\_A,B,C} &= -\overline{(\frac{v_{DC\_A,B,C}(t)}{2} + v_{AC\_A,B,C}(t))(i_{circ\_A,B,C}(t) - \frac{1}{2} i_{A,B,C}(t))} = \\ &= -\frac{P_{DC}}{6} + \frac{P_{AC}}{6} \end{aligned} \tag{4.37}$$

Equations (4.36) and (4.37), under the specified assumptions, describe the energy stored in the upper and lower arm chainlinks that can be used for cell capacitor voltage regulation. Based on these expressions the power of all the converter chainlinks can be computed, and therefore the dynamics of the energy stored in the converter cells can be related to the converter voltage and current references. This provides a possibility to maintain the energy stored in the converter cells and a similar approach can be used for maintaining the energy stored in the converter phases and arms.

4.5 MMC sizing

An MMC provides a multilevel AC waveform by relying on the distributed energy stored in the cell capacitors [29, 105]. Therefore, to provide an energy transfer at certain voltage ratings, there is a minimum of energy storage required to ensure correct converter operation [105, 106]. Additionally, energy stored in the cell capacitors has the biggest influence on the converter size, cost and weight [106]. Hence, dimensioning the cell capacitors plays major role in the converter design, especially in cost-sensitive applications. The required energy per chainlink, as given by (4.30), is defined by the cell capacitance, number of cells and nominal cell capacitor voltage (or nominal DC voltage).

Dimensioning of an MMC includes selection of the number of cells, cell capacitance, arm inductance and voltage and current ratings of semiconductor devices. The number of cells is predefined with the nominal DC voltage and the voltage rating of the switches. If 1.7 kV IGBTs are utilised, the nominal cell voltage is about 1 kV, and since an arm should be able to generate the full DC voltage, defining the nominal number of cells per arm is simple. For instance if the DC voltage is set at 20 kV, the number of cells per MMC arm is going to be 20.

The cell capacitance is dimensioned with respect to how much energy is needed to be stored in the converter to correctly operate at a certain power level. Correct operation requires limited cell capacitor voltage ripple, in order to be able to generate arm voltage references. In [107], the converter capacitance constant EP is defined as the energy-power ratio, as described by:

$$EP = \frac{E_{stored}}{P_{rat}} = \frac{3 \cdot C_{cell} \cdot V_{DC}^2}{N \cdot P_{rat}} \tag{4.38}$$

The capacitance constant has a dimension of time. In [107] suggested values for the capacitance constant is in the range of 10 - 50 ms. The capacitance constant has a direct effect on the amount of ripple in the cell capacitor voltages. In [45] the selected value for capacitance constant is 115 ms. In [105, 106] the minimum required energy to be stored in the converter cells is analysed in different conditions. In

[106] a normalised rated energy storage [kJ/MVA], which corresponds to capacitance constant in [ms], is analysed for different modulation indices and power angles, on the basis of maximum allowed capacitor voltages ripple. For the capacitor voltage ripple of $\pm 10\,\%$ in the case of active power transfer, a rough estimation of the minimum capacitance constant EP is between 20 and 30 ms. Under the same conditions, the authors in [105] suggest a capacitance constant of 39 ms. The values considered in this theses are about 40 - 60 ms which corresponds to a cell capacitor voltage ripple of approximately 10 - 15 %. For the same DC voltage and capacitance constant, the capacitance is directly proportional to the rated power (4.38).

The circulating current, if it is not controlled, has a negative-sequence second harmonic component [47, 86] due to the arm power oscillation described by (4.33) when both arm current and arm voltage have DC and 50 Hz components. The arm inductance is selected either to limit the second harmonic in the circulating current or to reduce $\frac{di}{dt}$ in fault conditions, such as a short circuit of the DC link [47, 107]. In [47] an algorithm to select arm inductance, when the maximum second harmonic circulating current amplitude is known, for the given power and voltage ratings, is suggested. Similarly, in [107] it is suggested that the arm inductance should be selected to avoid a resonance with the cell capacitances at the critical frequencies. A resonance between the arm inductance and cell capacitance happens for the specified value of arm inductance L_{arm_res} given by:

$$L_{arm\_res} = \frac{N}{C_{cell}(2 \cdot \pi \cdot f)^2} \frac{2(h^2-1) + m^2 \cdot h^2}{8 \cdot h^2(h^2-1)} \tag{4.39}$$

where f is fundamental frequency, h is the harmonic order and m is the modulation index [107]. The critical harmonics are even: 2, 4, etc. The values of L_{arm} and C_{cell} should be selected to avoid resonance, since at the resonance points, the cell capacitor voltages have significantly higher ripple. In this thesis, the arm inductance is selected to have a somewhat higher (30 %) inductance than the resonance inductance (4.39) at second harmonic frequency ($h = 2$ and $f = 50\,\text{Hz}$). When equation (4.38) is solved for C_{cell} and the value is substituted in (4.39) a simplified expression for the arm inductance is obtained:

$$L_{arm} = 1.3 \cdot L_{arm\_res} \approx k_1 \frac{{V_{DC}}^2}{P_{rat}} \tag{4.40}$$

where k_1 is a constant parameter (approximately 80 μs for the capacitance constant of 50 ms, fundamental frequency of 50 Hz and modulation index of 1). The selected arm inductance is directly proportional to the square of the DC voltage, and inversely proportional to the rated power. According to [47], the fault current rise rate, α, can be computed as:

$$\alpha = \frac{V_{DC}}{2 \cdot L_{arm}} \tag{4.41}$$

which in the case of multilevel topologies is less than 10 A/μs. For the above selected values and converter ratings from Table 3.5, the fault current rise rate is approximately 5.2 A/μs.

The peak switch current is equal to the maximum arm current, which is the sum of $\frac{1}{3}$ of the DC current and $\frac{1}{2}$ of the AC current amplitude (when second harmonic in circulating current is suppressed). The peak current is used for selecting the semiconductor devices. Since the pulsed load requires an arm balancing method with a 50 Hz component in the circulating current (section 5.6), the peak switch current will be somewhat higher, requiring more tolerance in the switch selection.

4.6 Summary

This chapter presented the MMC topology, which has been chosen for the grid interface to the klystron modulators. In general terms, the main converter features were reviewed, including high AC waveform quality, possibility to extend to any number of levels, modularity and availability. The possibility to operate the converter without the DC link capacitors made a topology breakthrough in the HVDC applications. However, this feature is not utilised in the application of interest due to necessity for the DC link capacitors responsible for limiting the DC voltage droop caused by load pulses.

There are various modulation methods used in multilevel topologies, applicable on the MMC, as well. However, some modifications of those are necessary to achieve full

topology potential. There is always a compromise between the switching frequency and AC waveform quality, however, when it comes to large number of levels it is possible to reduce the switching losses while providing good AC waveform quality. The application, control dynamics and number of levels determine the most suitable modulation method. The selected modulation method is (NLC+PWM) that can be used with the centralised controller, and it is therefore suitable for the MMC in the MV range (moderate number of levels). This method provides cell capacitor voltage balancing, by including the cell capacitors in the current path according to the sorting order.

The MMC features decoupling between AC and DC side, provided by the internal distributed energy storage elements. Due to this, converter AC and DC currents can be independently controlled. This chapter presented converter models, used to characterise converter internal and external waveforms. Based on the models, the AC current is fully described with the grid voltages, phase and arm impedance and the AC part of the arm voltage references. Similarly, the DC side model is defined through the circulating current model, defined by the DC voltage, arm impedance and the DC part of the arm voltage references. The coupling of the two sides comes with the modulation signal generation which includes both AC and DC parts of the arm voltage references. Therefore, the decoupling is only provided if the arm voltage is following its reference, i.e. if modulation works correctly, and the capacitor voltages are close to their nominal value. The presented models are used in Chapter 5 for the purpose of phase current and circulating currents controller design.

The modulation method provides balancing of cell capacitors within an arm, but it does not guarantee that cell capacitors are at the correct voltage level or balancing between arms and phases. To make sure that the cell capacitors of all the arms are at the correct voltage level, each converter arm is represented by the energy stored in the arm. This energy can be corrected by acting on the average arm power. In this chapter, the relation between converter average arm power and the converter waveforms is derived. In the ideal situation, the average arm powers are zero, but in reality when a system contains various disturbances, the energy stored in an arm

has to be controlled. The models from this chapter are used for design of converter energy, phase balancing and arm balancing controllers in Chapter 5.

Converter operation relies on the distributed energy storage providing additional voltage levels, therefore the converter can operate correctly only it has been sized for the specified voltage, current and power levels. The parameters such as converter cell dimensions, arm inductance, etc. have a huge influence on converter models and controller parameters.

Chapter 5

Control of VSC with a pulsed load

5.1 Introduction

This chapter presents the control challenges of a grid connected modular multilevel converter with a pulsed DC load that emulates klystron modulators. The chapter starts with the general background on grid connected converter power control. The AC side converter transfer function, together with the controller design is addressed. In the following section the decoupled AC and DC side control approach is reviewed and recognised as the most favourable MMC operational mode. The section proposes the control system structure based on the decoupled AC and DC side controller, in order to meet the application requirements. The DC side equivalent circuit and so called circulating current controller design are also presented. The fourth section focuses on the voltage controllers, including cell capacitor voltages and the DC link voltage control. The influence of the pulsed DC load operated at the fundamental grid frequency on the MMC performance is analysed in the fifth section. The pulsed load effects highlight the importance of balancing the converter arms, and this section proposes two novel arm balancing methods and reviews one method previously published in the literature. Finally, the operation of the grid synchronisation and precharge stages are presented.

5.2 General background on VSC control

This section focuses on the power control of a grid connected MMC based voltage source converter (VSC). In the case of three-phase converters, the control is typically phasor based. The phasors are obtained by applying well known Clarke's and Park's transformations [108, 109]. After applying Clarke's transformation on phase A, B and C quantities, two coordinates are derived in the stationary α, β reference frame. Upon applying Park's transformation on the α, β coordinates, two coordinates in synchronous d, q reference frame are derived. The Park's transform requires the phase of the grid voltage θ, so that the d, q frame can rotate with the same speed as the grid voltage vectors. Obtaining the phase angle of the grid voltages is presented in the separate section dedicated to phase locked loop (PLL), see section 5.7. In the case of three-phase system, the coordinates in synchronous reference frame are constant. Thus, the power control is based on the d, q current control, by making AC current components follow the constant current references. Current references are calculated on the basis of power demand. The equivalent of the equations (4.22) and (4.23), in the d, q system are equations (5.1) and (5.2), respectively:

$$P_{AC} = \frac{3}{2}(V_{s\_d} \cdot i_d + V_{s\_q} \cdot i_q) \tag{5.1}$$

$$Q_{AC} = \frac{3}{2}(-V_{s\_d} \cdot i_q + V_{s\_q} \cdot i_d) \tag{5.2}$$

where $V_{s\_d,q}$ and $i_{d,q}$ are grid voltages and phase currents in the d, q frame, respectively. Usually, PLLs track the voltage phasor angle, so that the grid voltage has only d component, i.e. q component is equal to zero. In that case, to ensure reactive power equal to zero, the q component of the AC current should be also fixed at zero, while the d current directly affects the transmitted power. Having the active power reference, the current references ${i_{d,q}}^{ref}$ are calculated as:

$$\begin{aligned} {i_d}^{ref} &= \frac{2 \cdot P_{AC}}{3 \cdot V_{s\_d}} \\ {i_q}^{ref} &= 0 \end{aligned} \tag{5.3}$$

The equivalent schematics of grid connected MMC is presented in Fig. 5.1. The schematics corresponds to the equation (4.12). Voltages $v_{s\_A,B,C}$ are grid voltages

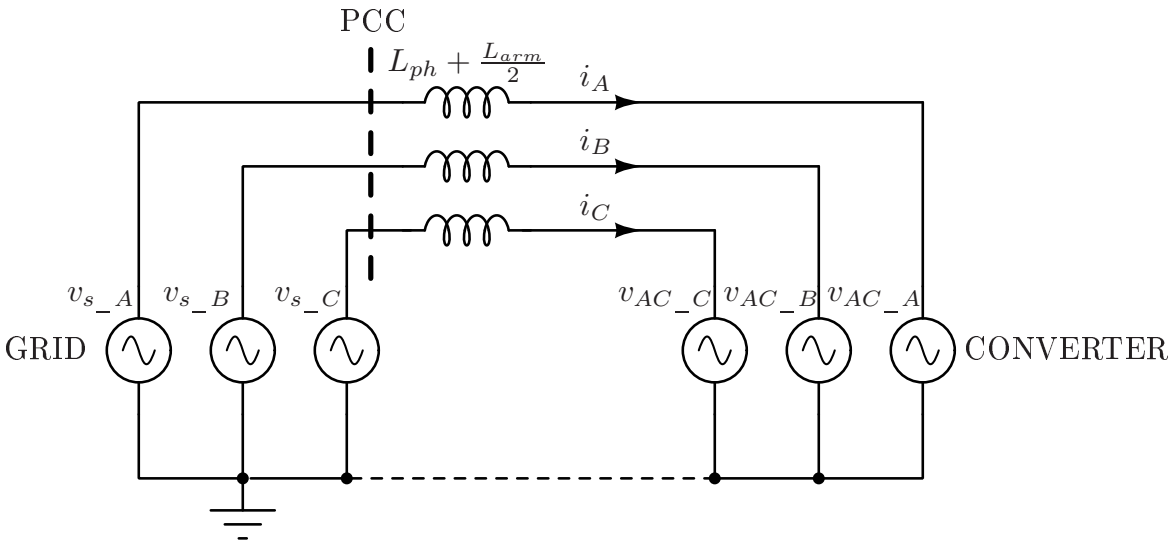


Figure 5.1: Equivalent AC circuit of grid connected MMC converter.

at the point of common coupling (PCC), $v_{AC\_A,B,C}$ are AC components of chainlink voltages, while the inductance in between L_{eq} is the sum of phase inductance and half of arm inductance. By applying the Clarke's transformation on equation (4.12), (5.4) is derived for the stationary reference frame:

$$v_{s\_\alpha,\beta}(t) - (L_{ph} + \frac{L_{arm}}{2})\frac{di_{\alpha,\beta}(t)}{dt} = v_{AC\_\alpha,\beta}(t) \tag{5.4}$$

The matrix representation of the same equation is:

$$\begin{bmatrix} v_{s\_\alpha} \\ v_{s\_\beta} \end{bmatrix} - (L_{ph} + \frac{L_{arm}}{2})\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} v_{AC\_\alpha} \\ v_{AC\_\beta} \end{bmatrix} \tag{5.5}$$

By applying the Park's transformation on the (5.5), the coupling factor between d and q coordinates appears:

$$\begin{bmatrix} v_{s\_d} \\ v_{s\_q} \end{bmatrix} - L_{eq}\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega \cdot L_{eq}\begin{bmatrix} i_q \\ -i_d \end{bmatrix} = \begin{bmatrix} v_{AC\_d} \\ v_{AC\_q} \end{bmatrix} \tag{5.6}$$

To simplify the transfer function, a new control variable, u, is introduced and its representation in the d, q coordinate system is given by (5.7):

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = L_{eq}\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{5.7}$$

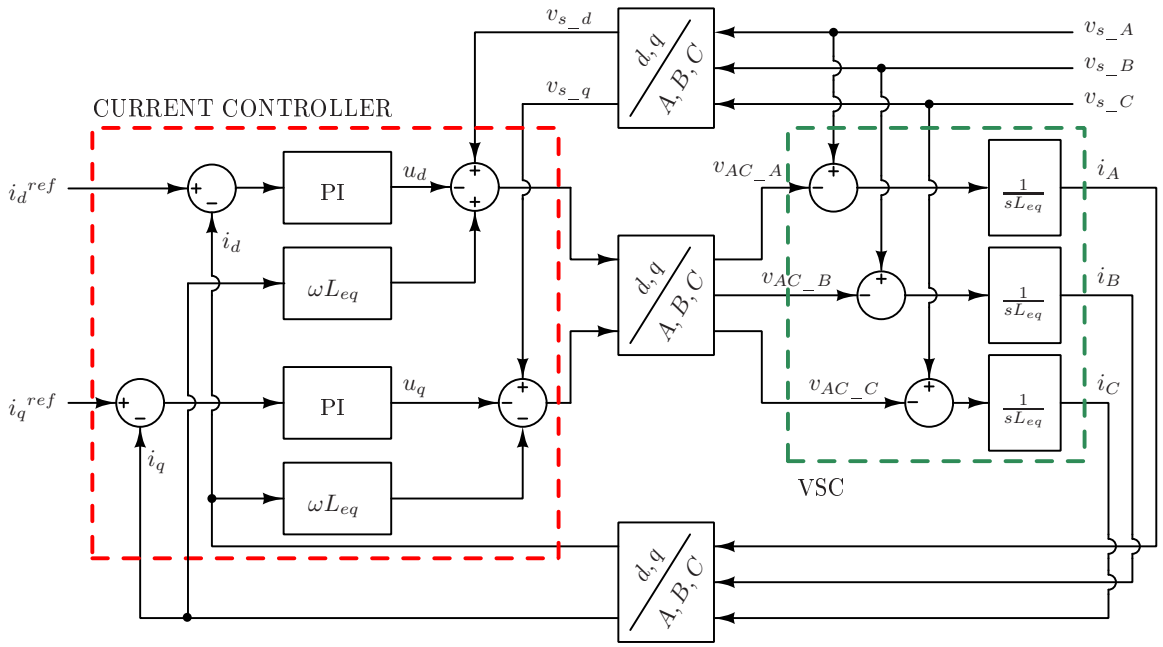


Figure 5.2: PI based d, q axis current controller.

The AC component of the chainlink voltage reference is described by (5.8):

$$\begin{bmatrix} v_{AC\_d} \\ v_{AC\_q} \end{bmatrix} = \begin{bmatrix} v_{s\_d} \\ v_{s\_q} \end{bmatrix} - \begin{bmatrix} u_d \\ u_q \end{bmatrix} + \omega \cdot L_{eq} \begin{bmatrix} i_q \\ -i_d \end{bmatrix} \tag{5.8}$$

The current-mode control in the d, q coordinate system is presented in Fig. 5.2. The coupling between the d and q quantities on the converter side needs to be taken into account when the controller is designed, so the decoupling is present in the controller. The controller compensates for the voltage drop on the equivalent inductor, by producing $u_{d,q}$ variable which is further used for forming the AC part of the voltage reference.

The converter transfer function in the Laplace domain is $\frac{1}{s \cdot L_{eq}}$, which represents the idealised case when there is no series resistance in the grid. This case is in agreement with Fig. 5.1 and derived equations. In reality, some non-zero resistance is present, which shifts converters pole from zero to a small negative value. The low frequency pole would cause the loop gain to drop from a relatively low frequency, therefore the

plant pole should be cancelled with the controller zero [110]. The PI regulator is used as a compensator, since the controller zero is used to compensate the converters pole. The controller pole at zero provides zero-error in the constant reference tracking. In this case, the closed-loop transfer function for tracking both current references has the same expression, given by:

$$\frac{i_{d,q}}{{i_{d,q}}^{ref}} = \frac{1}{\tau_i \cdot s + 1} \tag{5.9}$$

where τ_i is the time constant of the new closed-loop system. The time constant is chosen to make a controller fast enough to track the current reference, but slow enough to provide a cut-off frequency lower than one half of the sampling frequency. Depending on the application, the time constant of current mode controllers τ_i is between 0.5 ms and 5 ms [110]. The controller gains are in that case described by

$$k_{dq\_p} = \frac{L_{eq}}{\tau_i}, \quad k_{dq\_i} = \frac{R_{eq}}{\tau_i} \tag{5.10}$$

where R_{eq} is non-zero series resistance. In the modelled case $R_{eq} = 0$ and the integral parameter is calculated so that $\frac{k_{dq\_i}}{k_{dq\_p}} \ll \frac{1}{\tau_i}$. Therefore, the controller bandwidth is regulated with the proportional gain only.

5.3 Decoupled AC and DC side control

Initial publications of MMC suggested the open-loop control that included only VSC control and calculation of the AC voltage (AC part of the arm voltage) [29, 111]. In that case, the DC part of the arm reference is always equal to the half of the DC voltage. Additionally, the circulating current naturally has a second harmonic component causing an increase of cell capacitor voltages ripple [86, 112]. This kind of control does not leave a possibility of capacitor voltage balancing and control. Some open-loop control systems use an estimation of the energy stored in cell capacitors to generate arm references, providing a capability of cell capacitors balancing [113, 114]. A closed-loop control proposed in [45] opens a possibility for DC current control and regulating cell capacitor voltages at the correct level.

The closed-loop control takes into account of both AC and DC terminals and it is based on the MMC AC and DC side equations (4.12) and (4.13) and a decoupled converter model [90]. An extended decoupled model of the converter, considering the input, output, common mode and circulating current (authors consider circulating current only the current flowing among phases) is reported in [115, 116]. All those current components exhibit decoupled dynamics, given that the cell capacitors are properly balanced. In this thesis, a circulating current includes both output current (contributing to the DC current) and current circulating among phases. In the case when there is no connection between the grid neutral and the mid point of the converter DC link rails, common mode current is not present in the system [115].

Depending on the application, the control of an MMC might require regulation of multiple variables, such as the cell capacitor voltages, DC voltage, converter power, etc. For the given application, two current controllers are applied. One is aimed at controlling the phase (input) currents, as presented in previous section while the second control the circulating currents. The first controller is responsible for the AC part of the voltage reference for the converter arms. The circulating current controllers produce the DC part of the converter arms voltage reference. This provides the decoupling of the AC and DC side of the circuit and reduction of the mutual influence. The PI controllers used for this purpose can be tuned separately, since the dynamics of the currents is decoupeld [91]. However, decoupling of those controllers is possible only if the capacitor voltage balancing is ensured [117].

5.3.1 Control strategy

The application of a grid connected MMC, as an interface to the klystron modulators, requires regulation of both AC power and DC voltage. Since the pulsed DC load causes various harmonics in the DC voltage and current ripple, a decoupled AC and DC side controller is essential. In order to have a decoupled dynamics of these two sides, the regulation of cell capacitor voltages is necessary. In literature there are various control approaches used for the cell capacitors balancing and voltage

regulation. Some of those methods act on the specific cell modulation signal [45, 46, 91, 103, 115], while the others act on the circulating current reference in order to balance the cell capacitors [117, 118]. In [46, 103] the importance of arm balancing is highlighted and its effect on the converter stability is studied. The modification of the circulating current reference affects the energy stored in the chainlink, but not the energy distribution between cell capacitors inside the chainlink. The balance of the capacitors inside the chainlink is in that case provided by the modulation algorithm [31, 119].

Since the energy stored in the converter has to be maintained, an energy controller has to be included in the design, as well. The total stored energy, described by the sum of all cell capacitor voltages, is dependent on the difference between converter input and output power. Therefore, the sum of all cell capacitor voltages is controlled by modifying the power reference. In [45] the energy stored in each converter phase is used for generation of the circulating current reference. Such an algorithm is typically used when MMC is operated as an inverter, i.e. when the DC side is the input side. When MMC is operated as a rectifier, the control of energy stored in the phase (the sum of all cell capacitors of that phase) can be implemented to modify circulating current reference for the purpose of phase balancing. The balancing terms used to control overall converter energy, energy stored in converter phase and energy stored in converter arms have slower dynamics and therefore are used as outer control loops. Modifications of the decoupled control methodology including energy balancing (the sum of all cell capacitor voltages), phase balancing (the sum of cell capacitor voltages of one phase) and arm balancing (the sum of cell capacitors of one arm) application has been reported in literature [116].

For the given DC voltage, the klystron modulators draw a certain amount of power, depending on the pulse duration. The converter DC power is imposed by the load, thus the energy controller should correct the AC power reference accordingly. Therefore, the energy controller is used as an outer loop with respect to the AC power and phase current references.

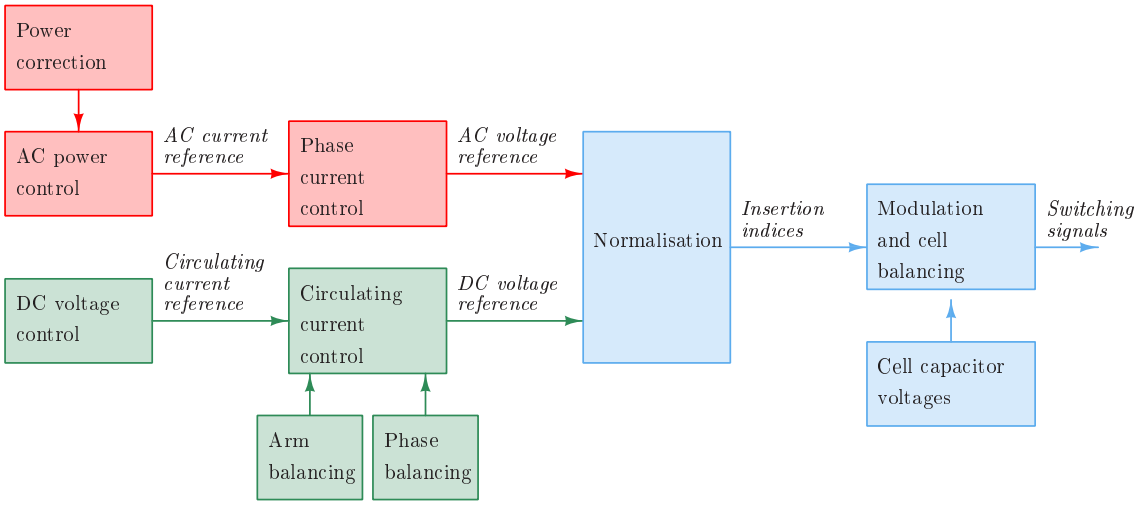


Figure 5.3: Decoupled AC and DC side controller strategy for the specified application.

The droop in the DC voltage is limited by the DC link capacitors. Those capacitors should be recharged after the pulse, requiring a DC voltage controller. The DC voltage is regulated by controlling the DC current. In the case of an MMC, the DC current is controlled indirectly by controlling the composing quantities, i.e. circulating currents. If the peak DC voltage should be followed, the bandwidth of the controller has to be very high. If only the average DC voltage should be controlled, the dynamics are slower and the DC voltage controller can be used as an outer loop of the circulating current controller.

Phase balancing and arm balancing are also provided by modifying the circulating current references. The circulating current controllers provide DC parts of the arm voltage references. The proposed control strategy employed is depicted in Fig. 5.3. The MMC converter together with the control strategy from Fig. 5.3 is presented in Fig. 5.4.

The particularity of the application is a fundamental frequency component in the DC voltage ripple which causes the imbalances of the converter arms. Imbalanced converter arms lead to the reduction of the cell voltages of one arm, which results

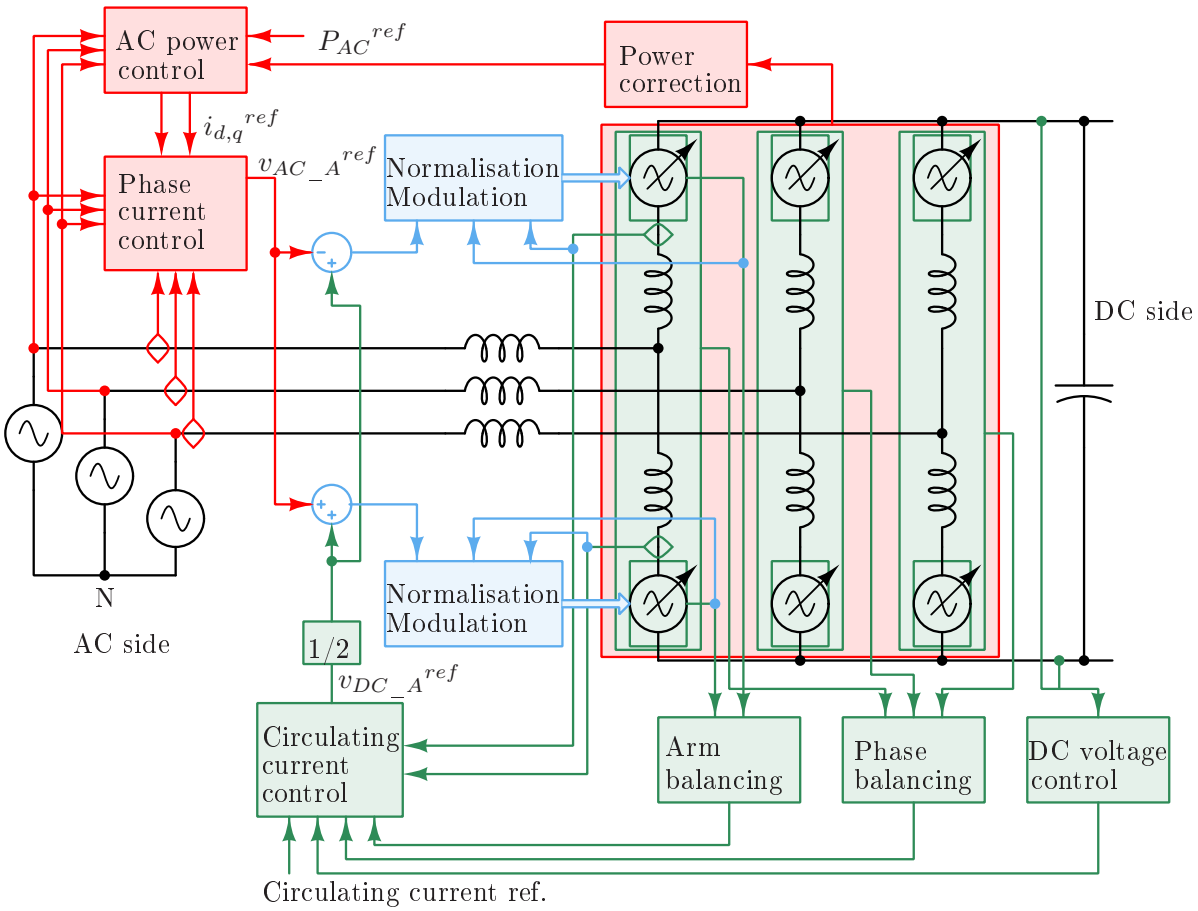


Figure 5.4: The control strategy applied on the MMC converter, with the focus on one converter phase.

in the overmodulation of that arm. Overmodulation causes low frequency distortion, which is hard to filter and leads to an increased AC power fluctuation [112, 117]. Thus, the arm balancing controller is discussed in more detail in the following sections.

5.3.2 Circulating current control

The circulating current controller is based on the equivalent DC side circuit presented in Fig. 5.5 for the case of phase A. The DC part of the reference for the upper and

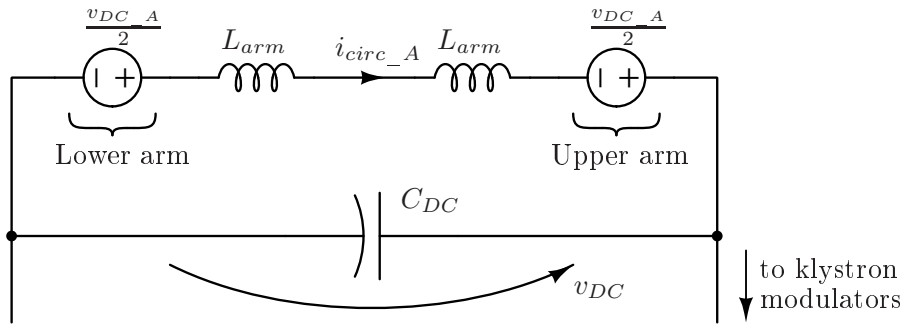


Figure 5.5: Equivalent DC side circuit of phase A of an MMC converter.

lower arm chainlinks is provided by the circulating current controller that compensates for the voltage drop across the two arm inductors. The equivalent DC side equation is given by (4.13).

The circulating current reference is essentially generated from the DC voltage controller, which is a slower outer loop in the control system. One third of the DC current reference is set as a circulating current reference of each of the phases. In addition, the reference can be modified with the arm and phase balancing controllers (Fig. 5.3).

The circulating current reference is ideally constant, which leaves a possibility for PI regulators to track it without steady-state error. Similarly to the d, q current controllers, the PI based compensator, compensates for the voltage drop on the two arm inductors, to provide the overall DC part voltage reference on the two chainlinks of the same phase. The controller diagram is presented in Fig. 5.6, where phase A is used as an example.

The open-loop transfer function has a pole at zero (or close to zero in the case of a lossy inductor), thus a simple PI controller is sufficient to compensate this pole. The closed-loop transfer function, with the correct choice of controller gains can be

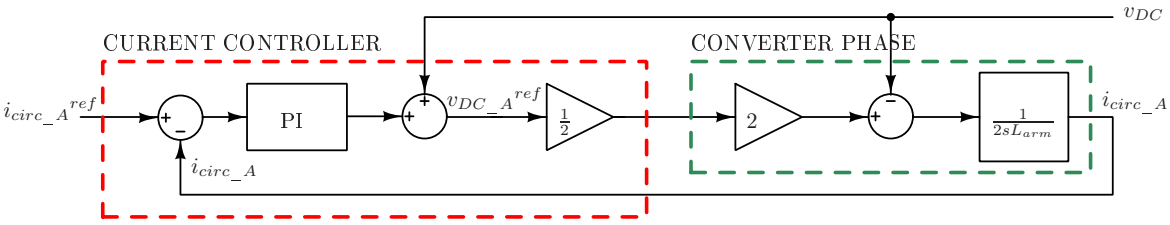


Figure 5.6: Circulating current controller for the phase A.

simplified to the equation (5.11):

$$\frac{i_{circ\_A,B,C}}{i_{circ\_A,B,C}{}^{ref}} = \frac{1}{\tau_{i\_circ} \cdot s + 1} \tag{5.11}$$

Where τ_{i_circ} is the time constant of the circulating current controller. The controller gains and time constant are chosen in a similar way to the d, q current controllers. The relation between controller gains and the time constant is in that case described by:

$$k_{circ\_p} = \frac{2 \cdot L_{arm}}{\tau_{i\_circ}}, \quad \frac{k_{circ\_i}}{k_{circ\_p}} \ll \frac{1}{\tau_{i\_circ}} \tag{5.12}$$

since zero series resistance is assumed.

In the case of circulating current reference not being constant, some other type of controller, such as proportional-resonant controller [120] able to track specific harmonic components, would be a more suitable solution. However, if the PI controller has enough bandwidth to track low frequency references with small steady-state error, it can be used as a circulating current compensator, accepting a non-zero tracking error. Additionally, if the circulating current controller is used only to suppress the second harmonic circulating among phases (which is not the case in the specified application), a circulating current components in a d, q reference frame rotating at $-2 \cdot \omega$ can be controlled to zero by providing a DC voltage reference correction [86]. In the specified application, the circulating current would have only DC current component and the 50 Hz component which will be controlled utilising a PI controller, as presented in Fig. 5.6.

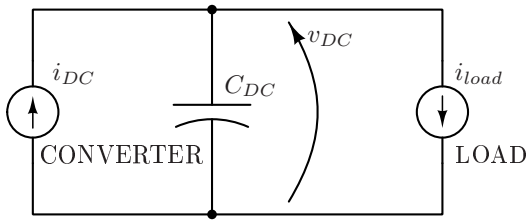


Figure 5.7: Equivalent circuit on the DC link side.

5.4 Voltage controllers

This section is focused on the design of slow controller loops used for generating the d, q axis and circulating current references. These controllers are used for the purposes of cell capacitor voltage regulation and the DC voltage control. Those controller loops regulate the mean value of the capacitor voltages and thus are based on the capacitor voltages averaged over a 20 ms period. Therefore, the time constant of the closed-loop controller should be significantly higher than 20 ms.

The first subsection is focused on the DC voltage controller that regulates the average DC voltage at the nominal level. This is important to provide approximately the same pulsed current from pulse to pulse. The following subsection discusses cell capacitors control including the overall energy control, phase balancing and arm balancing. The converter models for the purpose of controller design are presented, as well.

5.4.1 DC voltage controller

The DC link capacitor is charged by the converter and discharged by the periodical pulses of the load. The equivalent equation for the DC voltage and the equivalent circuit around the DC link capacitor is given by:

$$C_{DC}\frac{dv_{DC}(t)}{dt} = i_{DC}(t) - i_{load}(t) \tag{5.13}$$

and Fig. 5.7, respectively.

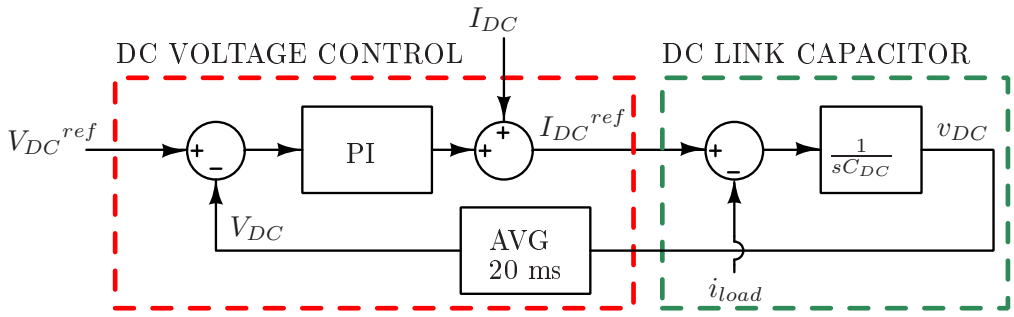


Figure 5.8: DC voltage controller used for the DC current reference generation.

The output current is pulsed, but its average value over 20 ms period is constant in regular operation. The converter DC current should have the same average value and the DC voltage controller is used to correct the DC current reference to this value. Again, the controller can be based on the averaged DC voltage and slow PI controller. The controller diagram is given by Fig. 5.8. The DC current reference has a DC current nominal value as a feed-forward term and a correction generated by the PI controller in order to maintain the average DC voltage level. The same control diagram can be used on a non-averaged DC voltage. In that case the DC current reference would not be constant over a 20 ms period and would have some 50 Hz component. This would affect the arm balancing method that will be discussed in detail in section 5.6. In any case, the cut-off frequency of the closed-loop controller has to be significantly lower than the cut-off frequency of the circulating current controller.

At the initial stage of this research one of the specifications was achieving high before-pulse DC voltage repeatability [4] since the voltage at the begining of the pulse influences repeatability of the pulses produced by klystron modulators. Further research about the klystron modulator repeatability performance suggests that the low frequency non-reapeatability sources can be compensated [121]. Thus, the focus of the research moved from the peak DC voltage control. However, the DC voltage controllers can be designed to track the peak voltage rather than average. In that case

the charging DC current might not be constant, requiring adjustments from the arm balancing methods.

5.4.2 Cell capacitor voltages and their control

This section relates to the regulation of the cell capacitor voltages. The need of maintaining the energy stored in the converter is essential for any operation of the MMC [112, 113]. At the same time, cell capacitor voltages balancing is needed only in the cases where there are sources of imbalance between converter phases and converter arms. The sources of imbalances might be transients, unsymmetrical converter cells, arm inductors, phase inductors etc. Pulsed DC load causes imbalance between converter arms, which makes arm balancing crucial for this application. The imbalance between cells within one arm is always present as a consequence of different gating signals, thus balancing of the capacitors within an arm is essential. This is provided by the modulation algorithm and it will not be the topic of this section.

The equation (4.32) shows the relation between power delivered to the converter arm and the average cell voltage of that arm. If the cells within one arm are well balanced and the average cell voltage is close to its reference V_C, while the capacitors voltage ripple is negligible, their instantaneous voltage can be substituted with the V_C. The following equation is derived:

$$P_{cl}(t) = N \cdot C_{cell} \cdot V_C \frac{dv_C(t)}{dt} \tag{5.14}$$

The relation between the chainlink power and the sum of the capacitor voltages within the chainlink v_{cl} is:

$$P_{cl}(t) = C_{cell} \cdot V_C \frac{dv_{cl}(t)}{dt} \tag{5.15}$$

Based on this equation the relation between the additional power added to the converter arm with respect to the sum of capacitor voltages within the arm can be estimated.

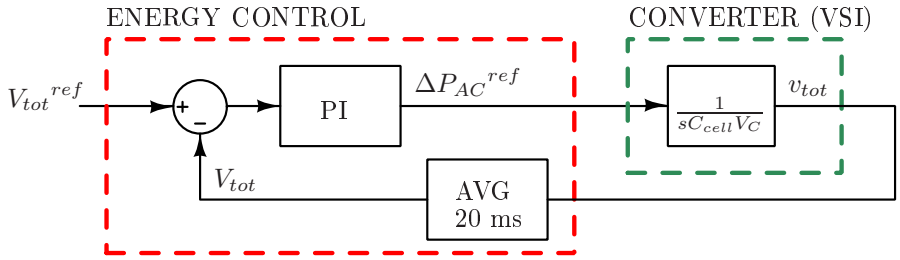


Figure 5.9: Converter total cell capacitor voltage controller.

5.4.2.1 Energy controller

The energy controller is used to correct the AC power reference in order to maintain the energy stored in the converter, i.e. the sum of all cell capacitor voltages, at the nominal level. By applying (5.15) to all six converter chainlinks, the amount of power ($\Delta P_{AC}(t)$) to be added to the AC power reference to maintain the converter energy is:

$$\Delta P_{AC}(t) = C_{cell} \cdot V_C \frac{dv_{tot}(t)}{dt} \tag{5.16}$$

An open-loop transfer function of the total cell voltages in the converter over the additional AC power reference is derived and a suitable PI controller is designed (Fig. 5.9). The controller is designed to have a low cut of frequency, since it is used as the outer loop for the d, q current controller and it is applied on the average of the sum of cell capacitor voltages over the period of the fundamental.

The reference for the sum of the cell capacitor voltages $V_{tot}{}^{ref}$ is set to achieve the nominal voltage on each cell capacitor and it is equal to $6 \cdot N \cdot V_C$. The sum of cell capacitor voltages in the converter is controlled by acting at the AC power reference and indirectly d, q current references.

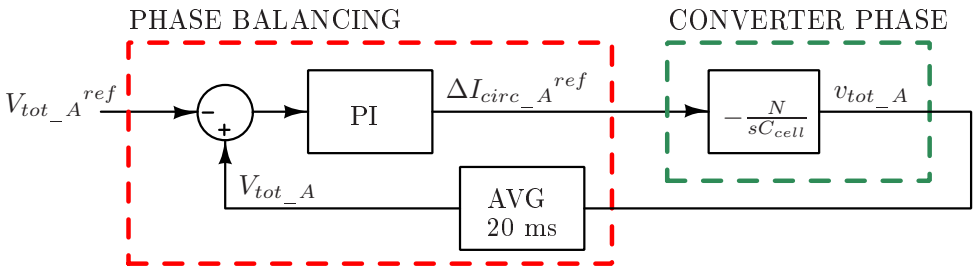


Figure 5.10: Phase A total cell capacitor voltage controller.

5.4.2.2 Phase balancing control

The amount of power to be added to converter phase to maintain the total cell capacitors voltage within that phase is given by:

$$P_{A,B,C}(t) = C_{cell} \cdot V_C \frac{dv_{tot\_A,B,C}(t)}{dt} \tag{5.17}$$

Starting from (4.34) and the sum of upper and lower arm powers (4.36) and (4.37), the derivative of power added to the phase with respect to the corresponding phase circulating current is:

$$\frac{dP_{A,B,C}(t)}{di_{circ\_A,B,C}(t)} = -v_{DC}(t) \tag{5.18}$$

The total sum of cell capacitor voltages in a phase should be controlled by acting on the circulating current reference. The amount of current ($\Delta I_{circ\_A,B,C}$) to be added to the circulating current reference to maintain the total cell capacitor voltages of a phase is:

$$\Delta I_{circ\_A,B,C}(t) = -\frac{C_{cell} \cdot V_C}{v_{DC}(t)} \frac{dv_{tot\_A,B,C}(t)}{dt} \approx -\frac{C_{cell}}{N} \frac{dv_{tot\_A,B,C}(t)}{dt} \tag{5.19}$$

Based on the (5.19), by applying a Laplace transformation, a transfer function of a total cell voltages within one phase over the circulating current is obtained and suitable PI controller is designed. A controller design for the phase A is presented in Fig. 5.10.

The closed-loop transfer function has a single pole at a very low frequency, since it should be significantly slower than the inner loop (circulating current controller)

and also should have a time constant much higher than 20 ms. The controller from Fig. 5.10 can be used for the purposes of phase balancing, i.e. ensuring even energy sharing among phases, but also for the purpose of controlling the energy stored in the converter phase as in [45, 115, 122]. When the controller is used for phase balancing purposes, the reference ${V_{tot\_A,B,C}}^{ref}$ is given as average value of the sum of cell voltages of the three phases. In that case each phase circulating current reference is corrected by a small DC offset, that together add up to zero $\Delta I_{circ\_A} + \Delta I_{circ\_B} + \Delta I_{circ\_C} = 0$. The presented controller does not ensure that the cell capacitor voltages follow the nominal value, but it ensures that the capacitor voltages are equal among the phases. In that case, the energy controller ensures that cell capacitors follow the nominal voltage reference.

When the same control structure is used to control the phase and overall energy, the reference for the sum of capacitors within one phase is equal to $2 \cdot N \cdot V_C$. This is typically used when the converter is operated as an inverter or in the precharge stage that will be discussed in section 5.8.

5.4.2.3 Arm balancing control

For the purpose of arm balancing controller, the relation of the difference of arm powers and the difference of total upper and lower arm voltages has to be derived. Based on the (5.15), the difference between upper and lower arm powers is given by

$$\Delta P_{arm\_A,B,C}(t) = C_{cell} \cdot V_C \frac{d\Delta v_{arm\_A,B,C}(t)}{dt} \tag{5.20}$$

where $\Delta v_{arm\_A,B,C}$ denotes the difference between the sum of cell capacitor voltages in upper and lower arm. This voltage should follow the zero reference, which would mean balanced upper and lower arms. The arm balancing is provided by editing circulating current reference. In particular, to provide arm balancing, a 50 Hz component is added to the circulating current reference producing a non-zero active power when multiplied with the AC part of the arm voltage reference. To provide the difference in power needed to balance the arm voltages, a corresponding amplitude of the 50 Hz

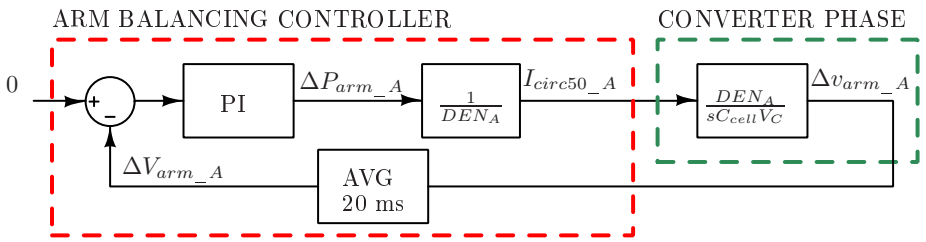


Figure 5.11: Arm balancing controller.

component current $I_{circ50\_A,B,C}$ is given by equation:

$$I_{circ50\_A,B,C}(t) = \frac{C_{cell} \cdot V_C}{DEN_{A,B,C}} \cdot \frac{d\Delta v_{arm\_A,B,C}(t)}{dt} \tag{5.21}$$

where the $DEN_{A,B,C}$ is a voltage and it is the first derivative of the average arm powers difference with respect to the circulating current 50 Hz component amplitude. The value of the denominator depends on the phase angle of the 50 Hz component in the circulating current and it will be discussed in following sections.

A PI controller can be designed to provide the amplitude of the 50 Hz component in the circulating current reference, as in Fig. 5.11. Again, the controller should have low cut-off frequency as an outer loop to the circulating current controller and considering its application on the averaged cell capacitor voltages.

5.5 Pulsed load effects

Assuming that the modulation works properly (the $v_{DC\_A,B,C}$ and $v_{AC\_A,B,C}$ follow ${v_{DC\_A,B,C}}^{ref}$ and ${v_{AC\_A,B,C}}^{ref}$, respectively) normal operation of control algorithms is provided and $i_{circ\_A,B,C}$ and $i_{A,B,C}$ follow their references. Normally, the MMC is operated with constant DC current demand that in the application of interest would uniformly recharge the DC link capacitor back to the specified voltage. In that case, the circulating current is constant and the DC voltage reference ${v_{DC\_A,B,C}}^{ref}$ is approximated with v_{DC} (4.13), even though some higher frequency switching ripple is present. Since $v_{AC\_A,B,C}$ and $i_{A,B,C}$ have only 50 Hz (plus higher frequency switching

noise) they would make a non-zero average power only in combination with 50 Hz current and voltage, respectively. Thus, it is important to highlight the mean value and 50 Hz component of DC voltage as:

$$v_{DC} = V_{DC} + v_{DC50} \tag{5.22}$$

where V_{DC} is the mean value and v_{DC50} is 50 Hz component of DC voltage ripple, caused by the pulsed load. Any other harmonics are ignored here since they do not contribute to the average power.

Starting from the (4.33), the average power of the upper arm of the phase A, B or C, $P_{up\_A,B,C}$, is given by:

$$P_{up\_A,B,C} = -\frac{V_{DC} \cdot i_{circ\_A,B,C}}{2} - \frac{\overline{v_{DC50} \cdot i_{A,B,C}}}{4} + \frac{\overline{v_{AC\_A,B,C} \cdot i_{A,B,C}}}{2} \tag{5.23}$$

If we assume that the overall converter energy is maintained, i.e. energy controller is applied and converter has negligible losses, input and output powers are equal $P_{AC} = P_{DC} = P$. Hence, the following relation applies:

$$\frac{V_{DC} \cdot i_{circ\_A,B,C}}{2} = \frac{P}{6} = \frac{\overline{v_{AC\_A,B,C} \cdot i_{A,B,C}}}{2} \tag{5.24}$$

By applying (5.24) to (5.23), the average power of the upper arm of phase A, B or C is given by (5.25). Similarly, the average power of the lower arms is described by:

$$P_{up\_A,B,C} = -\frac{\overline{v_{DC50} \cdot i_{A,B,C}}}{4} \tag{5.25}$$

$$P_{lo\_A,B,C} = \frac{\overline{v_{DC50} \cdot i_{A,B,C}}}{4} \tag{5.26}$$

The previous equations imply that in the case of non-zero 50 Hz component in the DC voltage, there will be an imbalance between the upper and lower converter arm average powers, i.e. total available arm voltages. Having different arm powers, the cell voltages of two arms diverge until overmodulation occurs in the arm with the lower cell capacitor voltages. Overmodulation can be a consequence of increased cell capacitor ripple, causing low frequency distortion, as it is adressed in [112]. The AC power has increased fluctuation once the overmodulation happens, as presented in

Fig. 5.12. The sum of all capacitor voltages (available voltage) in upper and lower arm chainlinks, together with the corresponding modulation signals are presented in Fig. 5.13. This is an example relating to 20 cells per arm converter operating at 16 MW and 20 kV DC voltage under pulsed load. At 0.35 s the overmodulation occurs in the lower arm, causing distortion of the waveforms that leads to the spikes in the AC power. Once the overmodulation happens the arm capacitor voltages of both arms reach new steady state values, i.e. the total available voltages stop drifting one from another. In the new steady state, upper and lower arm average powers are equal to zero, with the constant difference among cell capacitor voltages of upper and lower arm and distorted AC currents.

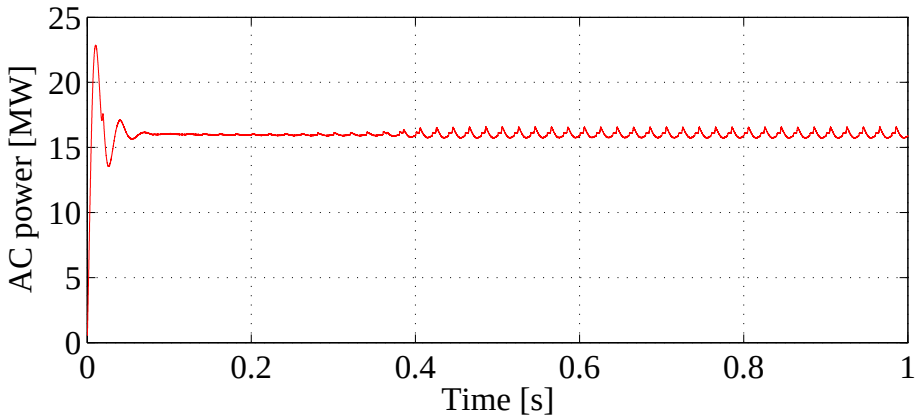


Figure 5.12: AC side power of the converter with pulsed DC load and constant circulating currents.

Since the pulsed load operates at 50 Hz, the DC voltage ripple has a 50 Hz component that affects two arm powers in the opposite way. This effect is present in all phases, but different, depending on the phase shift between phase current and the DC voltage 50 Hz component phase angle, according to (5.25) and (5.26). If the pulse takes place twice in the fundamental period, the effect of the DC voltage ripple on the average arm powers of the same phase would be the same. In that case, only the imbalance in the cell capacitor voltage ripples would be appearing between phases. Additionally, if the repetition frequency of the pulses is 300 Hz, the pulse has the same effect on all converter arms, thus maintaining the energy stored in the converter cells and ensuring

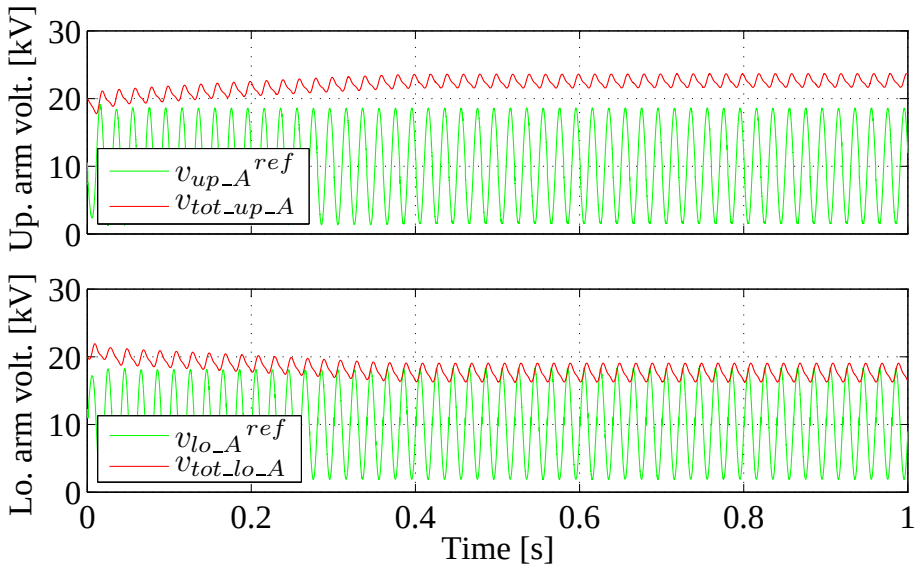


Figure 5.13: The modulation signal (green) and total available voltage (red) of upper (top) and lower (bottom) arm voltages in the imbalanced condition.

balanced cell voltages.

5.6 Arm balancing under pulsed DC load

In order to achieve low distortion of the AC currents and low AC power fluctuation, the AC references have to be followed. Hence, overmodulation should not occur. The first subsection focuses on the novel arm balancing method under pulsed DC load, by inserting a 50 Hz component in the circulating current references. This method ensures successful arm balancing for the majority of possible pulse positions with respect to grid voltages. However, this method is sensitive to pulse position.

The second subsection reviews the idea of inserting a 50 Hz component in the circulating current, but in phase with the AC voltage reference [70]. This method has been introduced for the normal operation of MMC, but it is also applicable for the pulsed load condition.

The third subsection focuses on the novel arm balancing method based on the change in a modulation scheme which ensures a low AC power fluctuation regardless the load pulse position. The method is based on modulation signal redistribution between converter arms while maintaining the correct AC waveforms.

5.6.1 Analytical solution for the circulating current reference

If the modulation algorithm is unchanged, the only way to balance arm voltages is to act on circulating current reference, since the AC quantities can not be changed to maintain a low total AC power fluctuation. Such an algorithm corresponds to a class of capacitor voltage control where the voltage balancing between two arms is achieved by changing the current references while the balancing of the capacitor voltages in one arm is achieved by sorting capacitor voltages [31, 119, 123]. The modification of the circulating current reference based on evaluating the oscillating energy/power in the arms is presented in [118, 124]. For the purpose of balancing the cell capacitor voltages between two arms of the same phase, the circulating current modification has to be based on average energy/power evaluation.

In order to balance the arm capacitor voltages and upper and lower arm average powers, a 50 Hz component must be added to the circulating current. The circulating currents of phases A, B and C are given by:

$$i_{circ\_A,B,C} = I_{circ\_A,B,C} + i_{circ50\_A,B,C} \tag{5.27}$$

where $I_{circ\_A,B,C}$ is the DC component and $i_{circ50\_A,B,C}$ is 50 Hz component of phase A, B and C circulating current. The ${v_{DC\_A,B,C}}^{ref}$ are no longer equal to v_{DC} (here agian the focus is on the average value and 50 Hz component of the ripple), as described by:

$${v_{DC\_A,B,C}}^{ref} = v_{DC} + 2 \cdot L_{arm} \cdot \frac{d}{dt} i_{circ50\_A,B,C} \tag{5.28}$$

Following the same procedure as in the previous section, the average upper and lower arm powers can be described by (5.29) and (5.30):

$$\begin{aligned} P_{up\_A,B,C} = &- \frac{\overline{v_{DC50} \cdot i_{circ50\_A,B,C}}}{2} - \frac{\overline{v_{DC50} \cdot i_{A,B,C}}}{4} \\ &- \overline{L_{arm} \cdot \frac{d}{dt} i_{circ50\_A,B,C} \cdot \frac{i_{A,B,C}}{2}} + \overline{v_{AC\_A,B,C} \cdot i_{circ50\_A,B,C}} \end{aligned} \tag{5.29}$$

$$\begin{aligned} P_{lo\_A,B,C} = &- \frac{\overline{v_{DC50} \cdot i_{circ50\_A,B,C}}}{2} + \frac{\overline{v_{DC50} \cdot i_{A,B,C}}}{4} \\ &+ \overline{L_{arm} \cdot \frac{d}{dt} i_{circ50\_A,B,C} \cdot \frac{i_{A,B,C}}{2}} - \overline{v_{AC\_A,B,C} \cdot i_{circ50\_A,B,C}} \end{aligned} \tag{5.30}$$

The only way both upper and lower arm powers are equal to zero at the same time, is if following equation applies:

$$\frac{\overline{v_{DC50} \cdot i_{circ50\_A,B,C}}}{2} = 0 \tag{5.31}$$

The relation (5.31) is possible only if the phase angles of 50 Hz component of the DC voltage ripple and the circulating current are shifted by $\frac{\pi}{2}$ rad. In that case, based on the amplitudes and phase angles of all variables from (5.29) and (5.30), amplitudes of the 50 Hz component of the circulating currents ($I_{circ50\_A,B,C}$) can be computed. The labels for the phase angle and amplitudes of the 50 Hz components of relevant signals are given by Table 5.1.

Table 5.1: Amplitudes and phase angles of 50 Hz components.

Signals	Amplitude labels	Phase labels
$i_{A,B,C}$	I_m	$\phi_{i\_A,B,C}$
$v_{AC\_A,B,C}$	V_m	$\phi_{v\_A,B,C}$
v_{DC50}	V_{DC50}	ϕ_{DC50}
$i_{circ50\_A,B,C}$	$I_{circ50\_A,B,C}$	$\phi_{circ50\_A,B,C}$

The difference between the upper and lower arm average powers is described by following equation:

$$\begin{aligned}\Delta P_{arm\_A,B,C} = &- \frac{V_{DC50} \cdot I_m \cos(\phi_{DC50} - \phi_{i\_A,B,C})}{4} \\ &- \frac{L_{arm} \cdot \omega \cdot I_{circ50\_A,B,C} \cdot I_m \cos(\phi_{circ50\_A,B,C} + \frac{\pi}{2} - \phi_{i\_A,B,C})}{2} \\ &+ V_m \cdot I_{circ50\_A,B,C} \cos(\phi_{circ50\_A,B,C} - \phi_{v\_A,B,C})\end{aligned} \tag{5.32}$$

When the phase angle of the circulating current of phases A, B and C is fixed to $\phi_{circ50\_A,B,C} = \phi_{DC50} - \frac{\pi}{2}$, the amplitude of 50 Hz component of the circulating current is calculated as:

$$\begin{aligned}I_{circ50\_A,B,C} &= \frac{NUM_{A,B,C}}{DEN_{A,B,C}} = \\ &= \frac{\frac{V_{DC50} \cdot I_m \cos(\phi_{DC50} - \phi_{i\_A,B,C})}{4}}{V_m \cos(\phi_{DC50} - \frac{\pi}{2} - \phi_{v\_A,B,C}) - \frac{L_{arm} \cdot \omega \cdot I_m \cos(\phi_{DC50} - \phi_{i\_A,B,C})}{2}}\end{aligned} \tag{5.33}$$

where ω is the angular frequency of the grid, while $NUM_{A,B,C}$ and $DEN_{A,B,C}$ denote the numerator and the denominator of the circulating current 50 Hz component amplitude for the phases A, B and C. Here, it can be seen that the amplitude of the 50 Hz component in the circulating currents can be both positive and negative, where negative value would indicate a phase angle shifted by π.

Based on the pulse position and the phase angle of the DC voltage ripple 50 Hz component, the circulating current will have different amplitudes in the case of different phases. Both pulse position and the DC voltage ripple angle are measured with respect to the phase A grid voltage positive gradient zero crossing. Even though, the position of the pulse has crucial influence to the DC voltage ripple angle, the influence

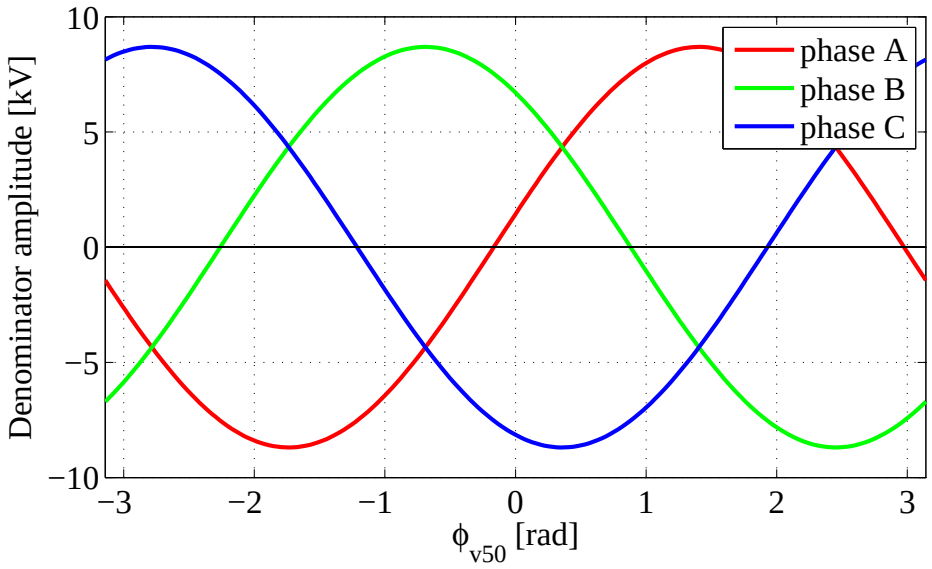


Figure 5.14: Analytically derived denominator values vs. the DC voltage ripple phase angle.

of the DC current is present as well. This is due to the fact that the resulting DC current, as a sum of the circulating currents, might have a non-zero 50 Hz component.

Additionally, depending on the pulse position (and DC voltage ripple phase angle), the denominator $DEN_{A,B,C}$ of the (5.33) can be positive, negative or zero. Obviously, in the case of the denominator being zero, there are issues related to calculation of the right amplitude of the 50 Hz component in the circulating current. In the cases when the denominator value is small (close to zero, positive or negative) the amplitude of the circulating current is higher and this is when the pulsed load significantly affects that particular phase. Fig. 5.14 shows waveforms that the denominators of phases A, B and C would have, as a function of the DC voltage ripple phase angle. These waveforms are generated assuming ideal AC voltages and currents, for the converter rated according to the Table 3.5, equation (5.33) and the derivation presented in Appendix B. In total there are 6 zero crossings of the denominators of all three phases, within one fundamental period.

Assuming that the DC voltage ripple has a phase angle that makes a non-zero denominator values in all three phases, (5.33) can be used as a feed-forward term for the

circulating current amplitude generation working together with the arm balancing controller. Additionally, on the basis of Fig. 5.11 and (5.32) the controller can be designed to ensure arm balancing.

A correction to the precalculated amplitude is provided by a PI controller, as presented in Fig. 5.15. NUM_A and DEN_A denote numerator and denominator of the phase A circulating current 50 Hz component amplitude from (5.33).

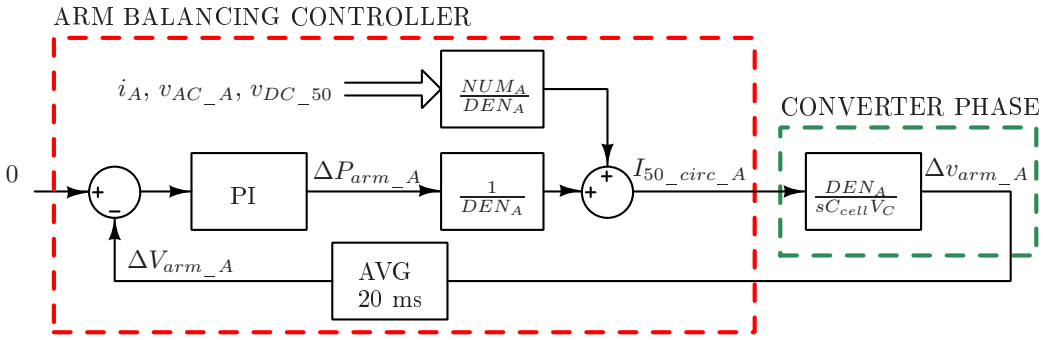


Figure 5.15: Arm balancing under pulsed DC load on the example of phase A.

The circulating currents 50 Hz components of all three phases are in phase or in phase opposition, thus the sum of the currents, i.e. 50 Hz component ripple of the DC current might not be zero. Based on equation (5.33) and the model from the Appendix B the amplitude of the DC current ripple versus the DC voltage ripple phase angle, is given in Fig. 5.16. The sum of the circulating currents 50 Hz component is dependent on the pulse position and it is higher in the pulse position for which any of the denominators is close to zero (or have small amplitude). Also there are pulse positions in which the DC current has zero DC current ripple.

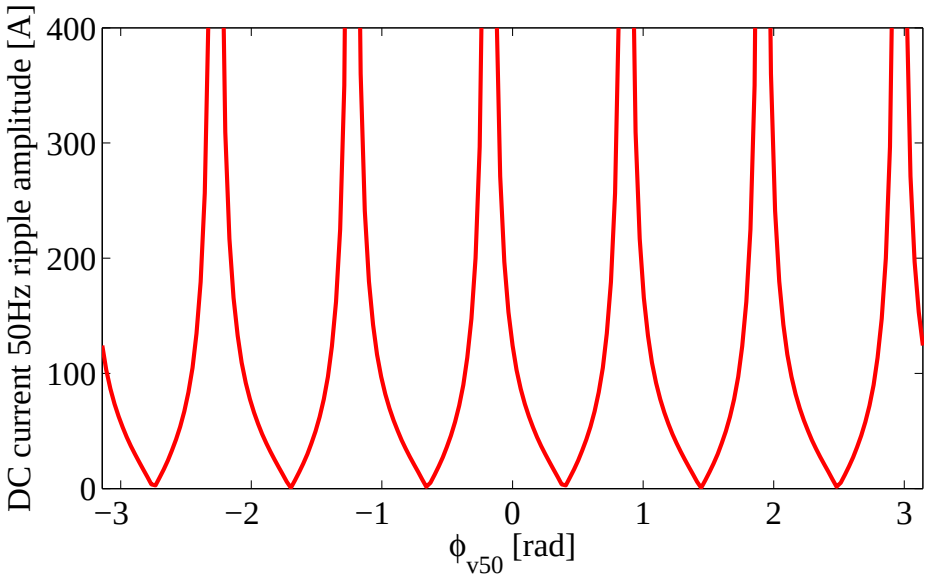


Figure 5.16: Analytically derived DC current 50 Hz component amplitude vs. the DC voltage ripple phase angle.

Additionally, if the DC voltage controller is not giving the constant DC current reference (Fig. 5.8), but it provides a reference that contains 50 Hz component, the generation of the circulating current reference needs to be modified. This includes taking into account the amount of 50 Hz component already present in the circulating current reference, as one third of the DC current reference. Hence, the circulating current reference generated by the arm balancing controller, has to be reduced for the sine-wave representation of the 50 Hz component induced by the DC current reference. Since the 50 Hz component of the DC current is not known during the current control period, the waveform from the previous period is used.

Different pulse positions will result in different amplitudes of the DC current ripple, as presented in Fig. 5.16. The pulse positions for which the sum of circulating currents has zero 50 Hz ripple provide uniform charging of the DC link capacitors.

5.6.2 Circulating current reference regardless of DC load type

In [70], the arm balancing with the 50 Hz circulating current in phase or in phase opposition with the AC reference voltage has been suggested. It is suggested that only a proportional gain should be applied to $\Delta v_{arm\_A,B,C}$ to cope with a transient imbalances, meaning that in steady state amplitude of circulating currents is zero. A pulsed DC load operated at 50 Hz causes constant imbalances in the average arm powers. Therefore, a PI controller should be used. In [125] a similar concept is introduced, where the circulating current is in phase or in phase opposition with the grid voltage by controlling the difference of energy stored in two arms to zero. In [125] it is suggested that the 50 Hz component in the circulating current can be adjusted either by keeping the phase angle constant and controlling the amplitude or by keeping the amplitude constant and adjusting the phase angle. However, aligning the current with the AC voltage is the most efficient method since in the power cross-product lower amplitude of current can be used to produce the same power with the same AC voltage.

When the circulating current is aligned with the AC voltage reference, the phase angles are equal, i.e. $\phi_{v\_A,B,C} = \phi_{circ50\_A,B,C}$. By applying that relation to the (5.32), the circulating current amplitude in the steady state is given by equation:

$$I_{circ50\_A,B,C} = \frac{NUM_{A,B,C}}{DEN_{A,B,C}} = \\ = \frac{\frac{V_{DC50} \cdot I_m \cos(\phi_{DC50} - \phi_{i\_A,B,C})}{4}}{V_m - \frac{L_{arm} \cdot \omega \cdot I_m \cos(\phi_{v\_A,B,C} + \frac{\pi}{2} - \phi_{i\_A,B,C})}{2}} \tag{5.34}$$

In the (5.34) the denominator is always positive and approximately equal to the AC voltage reference amplitude. Thus, for the same power correction ($NUM_{A,B,C}$) the current amplitude is smaller when compared to the previous method. Also, the denominator does not depend on the pulse position meaning that the stability of the control loop is not affected.

However, the equations for averaged arm powers (5.29) and (5.30) are not equal to

zero with given angle of the circulating current. The offset present in both arm powers is equal, therefore it can be controlled with the phase balancing loop and energy maintaining loop.

The controller structure can stay the same as the one in Fig. 5.15, with the difference in calculating the circulating current angle and different denominator value. The performance of the controller is less affected by the position of the pulse, which makes all pulse positions suitable for achieving low AC power fluctuation. Also the amplitudes of circulating currents are much lower, giving lower DC current ripple and lower DC power fluctuation. In this case, the DC current has the same non-zero amplitude of the 50 Hz ripple for all pulse positions, which is estimated in Appendix B based on the (5.34). In the case of the DC voltage controller providing a non-constant DC current reference, the circulating current references need to be corrected for one third of the 50 Hz DC current reference ripple.

5.6.3 Change in the modulation scheme to achieve arm balancing

In the previous analysis, the generation of the modulation signal for the converter arms considered equal distribution of the DC voltage reference and opposite AC voltage references with the same magnitude. An alternative way to avoid overmodulation and ensure low AC power fluctuation is to redistribute the modulation signal in such a way that the AC part of the voltage reference and AC current are not distorted, i.e. that the equations (4.4) and (4.12) are satisfied. The distribution of the DC voltage reference should remain unchanged, to avoid zero sequence components in the converter AC voltages. On the other hand, distribution of the AC part of the reference can be changed. In that case the references for the upper and lower arm are given by following equations, instead of equations (4.14) and (4.15), respectively.

$$v_{up\_A,B,C}(t) = \frac{v_{DC\_A,B,C}(t)}{2} - (1 + x_{A,B,C}) v_{AC\_A,B,C}(t) \tag{5.35}$$

$$v_{lo\_A,B,C}(t) = \frac{v_{DC\_A,B,C}(t)}{2} + (1 - x_{A,B,C}) v_{AC\_A,B,C}(t) \tag{5.36}$$

Where $x_{A,B,C}$ is a parameter that describes redistribution of the AC part of the reference between arms of the phase A, B or C. This way, both AC and DC voltage references are followed, which provides low AC power fluctuation.

The simplified converter diagram in the case of phase A is given in Fig. 5.17. It can be seen that $x_{A,B,C} \cdot v_{AC\_A,B,C}$ does not affect the AC side equivalent circuit, but only the DC side equivalent circuit. Thus, uneven distribution of the AC reference between two arms do not cause uneven distribution of the phase current between the two arms. However, the non-zero parameter $x_{A,B,C}$ causes appearance of the 50 Hz component in the circulating current, acting as a disturbance for the circulating current controller which normally tries to maintain a constant reference. The equivalent DC side circuit (with the focus on 50 Hz disturbance) is presented in Fig. 5.18.

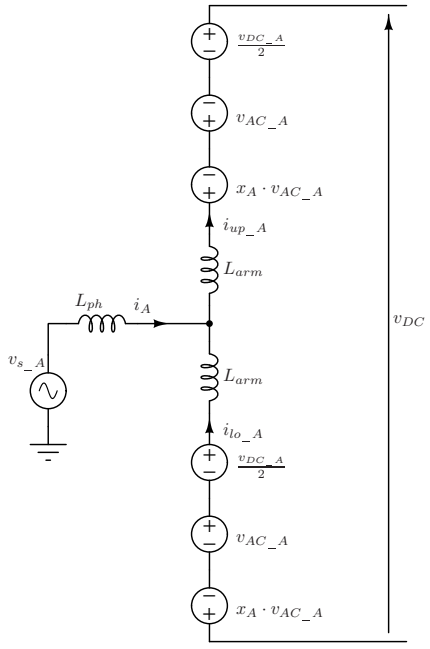


Figure 5.17: Simplified schematics of the phase A of an MMC with uneven distribution of AC voltage reference.

Since the circulating current would have a 50 Hz component, the circulating current controller will have a non-zero error in steady state, with the mean value following the

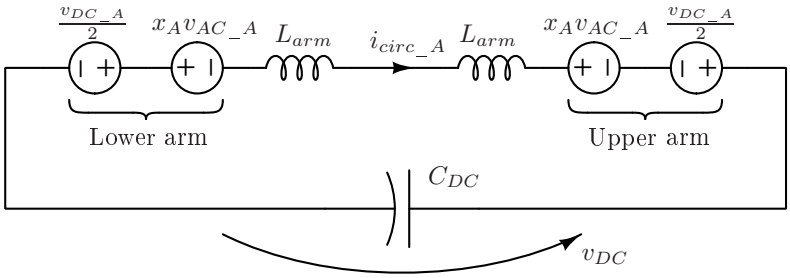


Figure 5.18: Equivalent DC side circuit of phase A of an MMC with uneven AC reference distribution.

reference. Thus, the DC reference, comprised of the DC voltage feed-forward term and the PI controller output is a function of the circulating current 50 Hz component. Considering the PI controller parameters (proportional gain k_{circ_p} and integral gain k_{circ_i}), the DC voltage reference can be approximated as:

$$\begin{aligned} {v_{DC\_A,B,C}}^{ref}(t) = v_{DC}(t) + {v_{DC\_A,B,C}}^{0} \\ - k_{circ\_p} \cdot i_{circ50\_A,B,C}(t) - k_{circ\_i} \int_0^t i_{circ50\_A,B,C}(\tau) d\tau \end{aligned} \tag{5.37}$$

where ${v_{DC\_A,B,C}}^{0}$ ensure that the mean values of circulating currents follow their constant references.

In steady state, the voltage over two arm inductors is compensated by the DC reference correction and $2 \cdot x_{A,B,C} \cdot v_{AC\_A,B,C}$. From the (5.37) and the DC equivalent circuit from Fig. 5.18, it can be concluded that the DC reference correction can be modelled as a series connection of a resistor with the resistance of k_{circ_p} and capacitor with the capacitance of $\frac{1}{k_{circ\_i}}$, as shown in Fig. 5.19.

Based on the equivalent circulating current 50 Hz component circuit, it can be seen that the circulating current is in a counter phase with the $2 \cdot x_{A,B,C} \cdot v_{AC\_A,B,C}$ and also that the equivalent impedance is dominantly real. Namely, the PI controller is designed as described in the section 5.3 and it has a k_{circ_p} proportional to arm inductance (5.12). Therefore, the resistance is significantly higher than the two arm inductance impedance at 50 Hz. Also, the capacitor has a complex impedance of

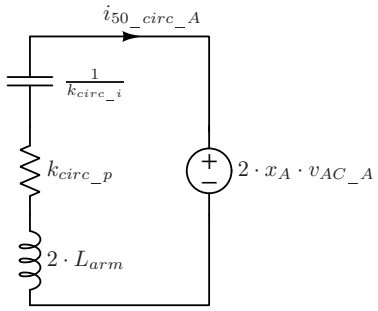


Figure 5.19: Circulating current 50 Hz component equivalent circuit in the case of uneven AC reference distribution, assuming PI based circulating current controller.

opposite sign, which makes imaginary part of the impedance lower. The circulating current 50 Hz component can be described by the following equation:

$$i_{circ50\_A,B,C}(t) = -\frac{2 \cdot x_{A,B,C} \cdot V_m}{Z_{arm}} \cos(\omega \cdot t + \phi_{v\_A,B,C} + \Delta\phi_{circ50}) \tag{5.38}$$

where Z_{arm} and $\Delta\phi_{circ50}$ correspond to the impedance amplitude and phase angle from the Fig. 5.19, respectively. The angle is typically only a few degrees positive or negative, depending on the circulating current controller parameters. Thus, this method has almost the same performance as the method from the previous subsection, i.e. the circulating current is almost aligned with the AC voltage reference.

The averaged upper and lower arms power and the difference between them satisfy equations (5.29), (5.30) and (5.32), even if the starting expressions for upper and lower arms voltages are not the same. By applying equation (5.38) to the (5.32), the nomianal value of parameter $x_{A,B,C}$ is given by:

$$\begin{aligned} x_{A,B,C} &= \frac{NUM_{A,B,C}}{DEN_{A,B,C}} = \\ &= \frac{\frac{V_{DC50} \cdot I_m \cos(\phi_{DC50} - \phi_{i\_A,B,C})}{4}}{-\frac{2 \cdot {V_m}^2 \cdot \cos(\Delta\phi_{circ50})}{Z_{arm}} + \frac{L_{arm} \cdot \omega \cdot V_m \cdot I_m \cos(\phi_{v\_A,B,C} + \Delta\phi_{circ50} + \frac{\pi}{2} - \phi_{i\_A,B,C})}{Z_{arm}}} \end{aligned} \tag{5.39}$$

The denominator describes how the parameter $x_{A,B,C}$ influences the average power difference between arms and it is always negative, meaning that the increase of $x_{A,B,C}$, causes the decrease of the power difference, which causes the decrease of the difference of upper and lower arm cell voltages. The benefit of this method is that it directly

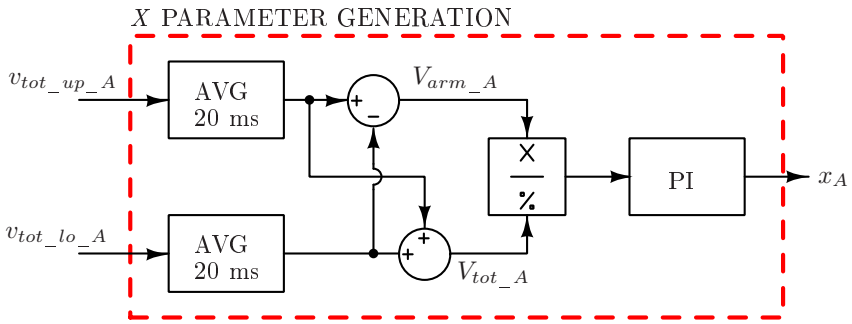


Figure 5.20: Parameter x_A generation on the basis of cell capacitor voltages on the example of phase A.

acts on the references to avoid overmodulation in the arms. Additionally, there is no need for generation 50 Hz component of the circulating current references and their correction in the cases when the DC current reference, produced by the voltage controller, is not constant.

The parameter $x_{A,B,C}$ is directly derived from the imbalance between the capacitor voltages of the upper and lower arms, meaning that the arm with lowest available voltage will have the lower amplitude of the modulation signal. The derivation of the parameter $x_{A,B,C}$ is presented in Fig. 5.20. Even if imbalances are present the overmodulation can be avoided by reducing the amplitude of the arm with lower capacitor voltages.

This way, the further divergence of the voltages is stopped and also the imbalance is removed. In other words, the PI controller ensures a zero steady state error and proper voltage balancing. The arm balancing controller from the Fig. 5.20 is included in the overall control diagram, as presented in Fig. 5.21. The difference from the general decoupled AC and DC side controller (Fig. 5.3) is in the arm balancing that is directly acting on the arm voltage references generation.

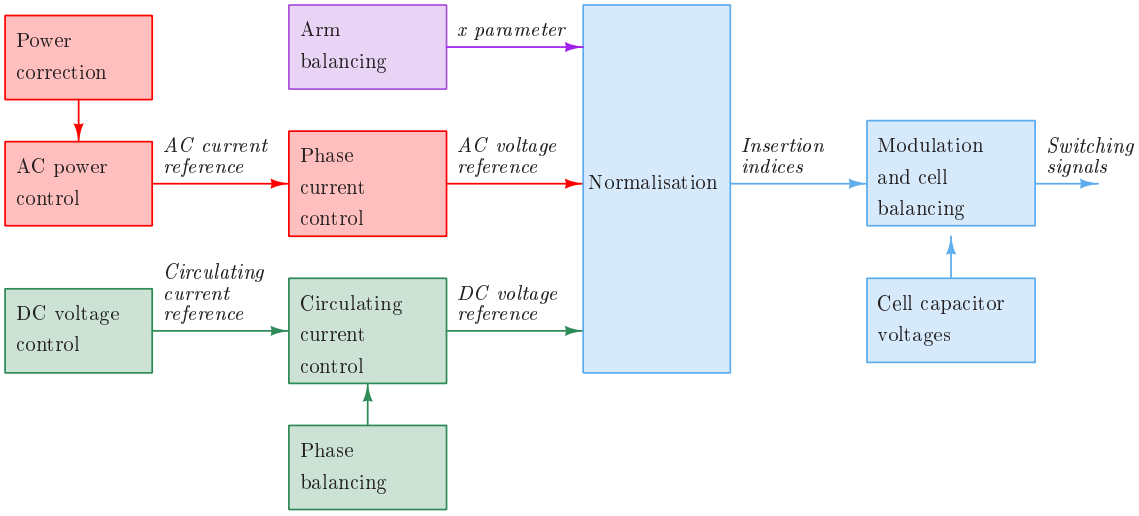


Figure 5.21: Controller strategy with the redistributed AC reference for the application of interest.

From the simulation results for the case of 10 % voltage droop on the DC side, the values of parameter $x_{A,B,C}$ are below 2 %. The amplitudes of the circulating currents and other waveforms will be discussed in more details in the simulation and experimental results chapters.

5.7 Grid synchronisation

In order to provide power control in the synchronous reference frame domain, the angle of stationary reference frame, θ, is needed. The synchronous reference frame should have the rotating speed equal to the angular grid frequency, so the information about the angle and the frequency has to be extracted from the grid. The most popular and the easiest way for phase extraction is the PLL. The basic principle of a d, q axis based PLL is shown in Fig. 5.22 and it is used for the grid-connected converters [110, 126] and in drives applications [127]. Since the power is usually controlled at the PCC of converter and the grid, the grid voltage is used as a reference for positioning of

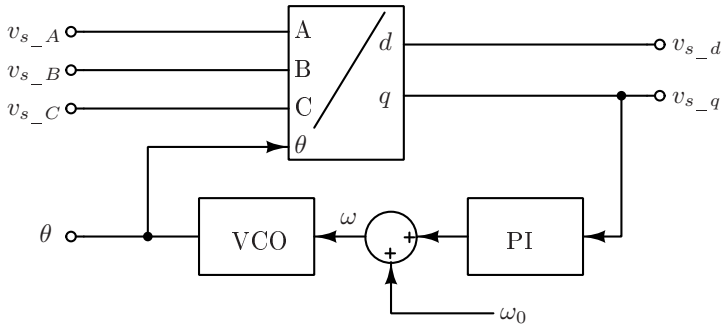


Figure 5.22: PLL applied on grid voltages, to provide grid phasor angle.

the synchronous frame. This means that the reference frame, besides rotating at the same speed as grid voltages, has d component aligned with the grid voltage phasor.

In the Fig. 5.22 the transformation of the grid voltages from A, B and C coordinates to d, q coordinates is presented. Since the fundamental grid frequency is well known for being 50 Hz (or 60 Hz in USA), this value is tracked using the PLL, accounting for any frequency variations. In this case, the voltage controlled oscillator (VCO) is basically an integrator. By integration of the frequency, the phase of the grid voltage phasor is extracted.

The basic PLL is a good solution if there are minor disturbances in the grid voltages amplitudes or frequencies. However, if there is some type of fault in the grid, there are some components on positive or negative multiples of fundamental grid frequency and the basic PLL is not able to provide adequate d, q components. Faults are usually caused by short-circuit events from phase to phase, or phase to ground, or many phases together. All those faults will cause negative or/and zero sequence component in voltages at PCC and changes in positive sequence component [128]. One possible solution for grid synchronisation under faults is to employ a PLL in the so-called decoupled double synchronous reference frame (DDSRF) [128]. Aside from the amplitude of the voltages, their phase angles also change, once a fault takes place. The most stable variable in a grid system is the grid frequency [128]. Closing the frequency loop, i.e. usage of a frequency locked loop (FLL), can also

be used for splitting grid voltages into sequence components. The algorithm that is utilised together with a FLL in order to provide voltage separation into sequences is the decoupled second-order generalised integrator (DSOGI). Both DDSRF and DSOGI are analysed in detail in [128], together with the power control methods under unbalanced grid conditions.

5.8 Control algorithms for soft-start and precharge

The previously described control approaches assume a start-up condition of the MMC being connected to the grid with already precharged cell capacitors. However, in the experimental verification of the converter, a controlled way of precharging the converter cells and synchronising the converter to the grid has to be developed. This sections describes the control approach of the precharge mode, suitable for the small scale experimental prototype.

In typical MMC applications the rail-to-rail DC bus capacitor is not used, so it is possible to charge submodule capacitors with the DC source rated at the nominal cell voltage. The conventional precharge methods reported in literature apply this feature, by charging cells sequentially [29] or in parallel [129]. Those methods require an additional DC source and contactors (or other types of switches) in order to connect/disconnect the auxiliary charging circuit to/from the DC bus. However, in the case of the MMC with a DC link capacitor, charging with a low voltage is not possible since the DC link capacitor should be precharged, as well. Thus, two precharge methodologies are considered; one where the precharge is done from the AC side and the other where the precharge is performed from the DC side. In both cases, the converter goes through the uncontrolled and controlled stage. Those concepts are analysed for the HVDC systems with two back-to-back MMCs in [130].

Precharge from the AC side starts with an uncontrolled stage where the whole MMC is behaving as a diode-bridge rectifier. In that stage the DC link is precharged to voltage lower than nominal (in the case of 10kV AC voltage, to 13.5kV DC voltage)

which would be shared equally among $2 \cdot N$ cells (not N as in the case of normal MMC operation). From that point, the controlled stage starts with the goal to precharge and maintain cell capacitor voltages and DC link capacitor voltage at the nominal voltage level. The controlled stage requires careful design of the control loops, since initial errors are quite high and overshoot in waveforms and overmodulation is likely to happen. One method to perform the controlled stage, in the case of precharge from the AC side, is reported in [131] and it requires changes in arm reference generation.

The precharge from the DC side, also comprises of two stages, the uncontrolled and controlled one. In this case an additional DC source rated at the nominal DC voltage is needed. During the uncontrolled stage, the number of included cells in both upper and lower arms is equal to $\frac{N}{2}$, providing that the cell capacitors and the DC link capacitor are precharged to their nominal value. The insertion of the cells according to previously explained modulation algorithm, is performed so that capacitor voltages balancing within an arm is ensured. This way, the controlled stage starts with the capacitors charged to nominal voltages and the only goal is to maintain cell capacitor voltages. In that case, in the controlled stage, MMC is operated as a conventional inverter with zero AC reference voltages.

For the rated voltages from Table 3.5 and the grid connected MMC, precharging from the AC side would be better solution since it does not require an additional DC source. The precharge from the DC side is suitable for the drives applications, since a DC source is available. For the smaller scale converter, aimed as an experimental prototype, precharge from the DC side is simpler and more practical. In this case, once the precharge stage is finished, the precharge circuit (additional DC source) is disconnected from the DC bus so that the AC terminals are connected to the grid. However, this approach requires another mode, so-called synchronisation to the grid in order to allow smooth grid connection.

5.8.1 Precharge from the DC side

In order to avoid the inrush current, the precherge circuit either has a series resistance [131] or the ability to slowly increase the DC link voltage in order to provide a soft-start. Here, the auxiliary DC source under analysis contains a three-phase diode bridge and a variable AC source only, since the DC link capacitor is already present on the MMC DC side. The MMC with the precharge circuit is presented in Fig. 5.23.

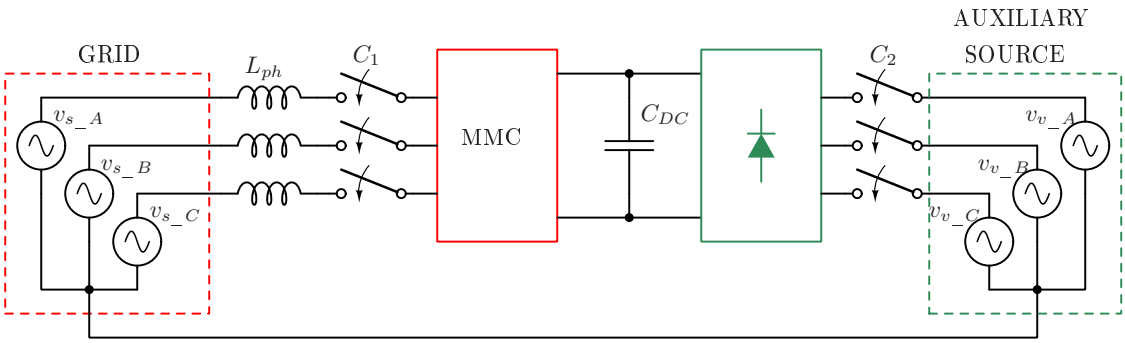


Figure 5.23: The grid connected MMC with the precharge circuit attached to the DC side.

Soft-start is performed with the slow increase of the auxiliary AC source voltage, while the uncontrolled operation of the converter is applied. The uncontrolled stage means including $\frac{N}{2}$ cell capacitors of each arm in the current path, with the selection of capacitors that ensure capacitor balancing (section 4.3). The AC terminals of the converter are disconnected from the grid (C_1 is open, C_2 is closed, Fig. 5.23). Once the DC link and cell capacitor voltages reach their nominal voltages, the controlled stage starts. The increase of the AC voltage can stop here, although further variations would affect the DC voltage only while the cell capacitor voltages are regulated. The controlled stage has a goal of maintaining the energy stored in each of converter phases, through the circulating current control (Fig. 5.6). The controller produces the DC voltage reference for the arms, while the AC reference is fixed to zero. The control diagram for one converter phase is presented at Fig. 5.24.

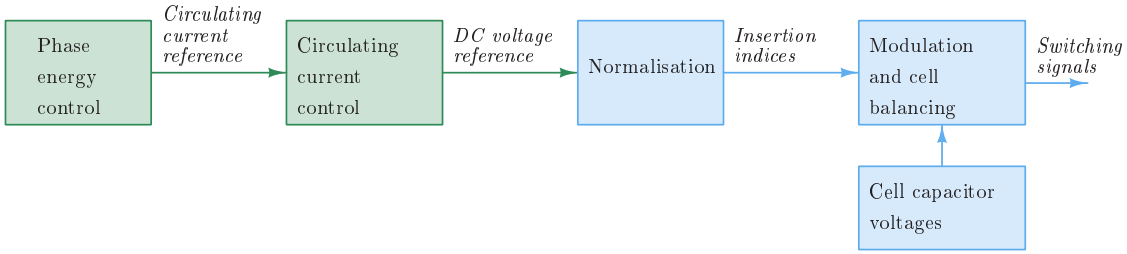


Figure 5.24: Controller strategy for the controlled stage of the precharge regime.

The control strategy from 5.24 has only one inner loop, related to the circulating current controllers and one outer loop used to regulate the energy stored in the converter phase. The phase energy controller has the same architecture as the phase balancing controller from Fig. 5.10, but with the ${V_{tot}}^{ref} = 2 \cdot N \cdot V_C$. Hence, this controller is used to maintain the energy stored in the converter phase at the nominal value.

To prepare the converter for the grid connection, the voltage produced on the AC terminals can be synchronised to the grid, in that case the AC reference is equal to the grid phase voltages. To be able to have a grid connection under zero voltage conditions between converter terminals and the grid (across phase inductors) the neutral point of two AC sources (the grid and the auxiliary precharge source) should be at the same voltage potential, as presented in the Fig. 5.23). At this point PLL can be used, in order to have the grid angle ready for the mode when the precharge circuit is disconnected and the converter is connected to the grid.

5.9 Summary

This chapter summarises the basis of VSC power control applied on the MMC converter, which together with circulating current controllers provide decoupled AC and DC side MMC control. Additionally, the outer voltage control loops, aimed for the

capacitor voltage balancing and DC voltage control are presented. These loops are slower and applied on voltage quantities averaged over the one fundamental period.

The control structure for the MMC, used as a grid interface to the pulsed DC load, is proposed. The controller for the overall energy stored in the converter is correcting the AC power reference, whilst the DC voltage controller, phase and arm balancing loops are affecting the circulating currents references and their control. The described control system allows controllability of both the AC power and DC voltage while maintaining the correct energy distribution amongst the converter cells.

The pulsed load effects on the MMC are analysed and the main feature is constant imbalance source for the average arm powers caused by the 50 Hz DC voltage ripple. Unbalanced converter arms shortly lead to an overmodulation of the arm with lower capacitor voltages causing AC power distortion. Three methods for the arm balancing for the MMC converter under pulsed DC load are analysed and all of them are characterised with the appearance of 50 Hz component in the circulating currents and DC current.

The first method is based on the analytical calculations for the circulating current references. Its performance is highly affected by the pulse position with the respect to grid voltages. For some, less suitable pulse positions the controller is not stable and the amplitudes of the 50 Hz components of circulating current and DC current are too high. However, for the most of pulse positions the controller performs arm balancing and for some of them, the resulting DC current has no 50 Hz ripple component.

The second method ensures arm balancing by producing the circulating current references in phase with an AC voltage reference of each phase. This method results in a lower 50 Hz component in the circulating current and a certain amount of DC current ripple regardless the pulse position. The balancing is successful for all pulse positions.

The third method is not based on the generating circulating current references, but on the redistribution of the AC voltage references between two arms of the same phase.

This way the overmodulation is avoided by reducing the amplitude of the arm voltage reference for the arm with lower capacitor voltages. This method also leads to the appearance of a 50 Hz component in the circulating currents and the DC current. The method performance is very similar to the second method since the 50 Hz component of the circulating currents has a small phase shift with respect to the corresponding AC voltage references.

Finally, the grid synchronisation and converter start-up techniques are presented. The precharge of the cell capacitors and the DC link capacitor is crucial for normal operation of MMC. Thus, the precharge techiques were analysed, including the decision on the precharge from the AC or DC side of the converter. Due to the simpler controlled stage of the precharge regime, the precharge from the DC side is selected for the laboratory prototype.

Chapter 6

Simulation results

6.1 Introduction

This chapter presents the validation of proposed converter topology and control strategies, using numerical simulations. Simulation models are built in the PLECS simulation package [132]. The simulation model is based on a 20 kV DC voltage, 16.6 MW medium voltage MMC under pulsed DC load. The pulsed DC load emulates a certain number of klystron modulators, corresponding to converter rated power by drawing an ideal constant current pulse. The converter ratings are given in Table 3.5. The DC voltage droop is set to 10 % of a nominal DC link voltage, to account for the worst case scenario if the power system optimisation results favoured the lower DC voltage range (10 kV DC voltage).

In Chapter 5, three arm balancing methods for an MMC under pulsed DC load are presented, and each of them is validated by simulation. To simplify the results presentation and comparison of the converter performance with different arm balancing methods, they are assigned as method one, two and three. Here, the method based on analytical solution for the circulating current reference from section 5.6 is referred to as method one. The method where the circulating current reference is aligned with

the AC voltage reference of that phase is referred to as method two. The method based on the change in the AC reference distribution among converter arms is named as method three.

The converter waveforms and control variables are dependent on the pulse position with respect to the AC voltages and currents. The pulse position is measured with respect to phase A grid voltage positive gradient zero crossing. The majority of the presented results in this chapter relate to the pulse position of 0.534 rad (approximately 1.7 ms after phase A voltage zero crossing), and unless otherwise specified this pulse position is assumed. In addition, performance of all three arm balancing methods is observed for different pulse positions, covering one third of the grid voltage period.

At the moment when the simulation starts, all capacitors are precharged and the AC power reference is set to the nominal value, while the pulsed load is enabled. This means that when simulation starts current controllers enter a transient in achieving nominal power transmission from the grid to the load.

The next section relates to the simulation model implementation, by covering both the converter and load parameters and the implementation of the control loops. The following section presents the performance of the PLL and the pulsed load. The pulsed load repetition frequency of 50 Hz produces a 50 Hz component in the DC voltage ripple.

The fourth section presents validation of all control loops introduced in Chapter 5 for the pulse position of 0.534 rad. The highlight is on the phase currents and AC power quality as well as the different waveforms for the circulating currents obtained for different arm balancing methods. The following section analyses the performance of the control system with each of the arm balancing controllers and for a range of pulse positions.

6.2 Simulation model implementation

This section covers both the hardware and the control implementation of the converter under pulsed DC load. The implementation of the converter and the load relates to the component ratings and characteristics. The implementation of the control loops presents the controller gains, based on the theory presented in Chapter 5.

6.2.1 Converter and load implementation

The converter and the load parameters, based on the optimisation result from Chapter 3 and converter sizing from section 4.5, are listed in Table 6.1. The simulation model of a three-phase 20 cell per arm modular multilevel converter is built on the basis of Fig. 4.1. Each cell is a modelled as a half bridge with ideal switches, i.e IGBT and an anti-parallel diode assumed to be either ON (0 V across the switch) or OFF (zero current through the switch), and a cell capacitor, precharged at nominal voltage V_C. In addition, the DC link capacitor is assumed to be precharged at V_{DC}. The arm inductors and phase inductors are assumed to be lossless. The grid is represented with a positive sequence ideal AC sources. The load is represented as an ideal periodical current pulse, with the pulse duration of 140 μs and pulse period of 20 ms.

Table 6.1: Simulation model parameters.

Parameter	Label	Value
DC voltage	V_{DC}	20 kV
AC voltage amplitude	V_{s_m}	8.57 kV
Rated power	P	16.6 MW
Cell voltage	V_C	1 kV
Cell capacitance	C_{cell}	13.8 mF
Arm inductance	L_{arm}	1.8 mH
Phase inductance	L_{ph}	3.5 mH
DC link droop	ΔV	2 kV
DC link capacitor	C_{DC}	8.3 mF
Peak load current	I_{peak}	118.57 kA

6.2.2 Implementation of the control algorithms and modulation scheme

The control loops presented in Chapter 5, are implemented in the simulation model of an MMC under pulsed DC load descrabed by Table 6.1. The control loops in Chapter 5 are presented by their Laplace domain equivalent diagrams and transfer functions, which can be implemented in PLECS environment. However, to make the simulation environment more similar to the experimental implementation, discrete current controllers are used. Discrete controllers are applied on the discrete signals, sampled at the sampling frequency f_s, with the controller gains obtained from the Laplace transfer function models. If trapezoidal integration is assumed and a sampling period is T_s, the discrete integrator is described by:

$$Int(z) = \frac{T_s}{2}\frac{z+1}{z-1} \tag{6.1}$$

In the simulation model the pulse duration is set to 140 μs, therefore to ensure at least one of the samples during the pulse and enough bandwidth for the current controllers,

sampling frequency is set to 10 kHz. The PI controller gains used in the simulation model are presented in Table 6.2. The trapezoidal integration rule (6.1) guaranties the same behaviour of the continuous and discrete controllers only if the ratio between sampling frequency and the closed-loop bandwidth is higher than 35 [133]. In the case of the current controllers, for the selected bandwidth values from Table 6.2, the stable controller behaviour is guaranteed while the response might not be identical with the continuous controller alternatives. Nevertheless, the fast current controller responses are confirmed, as documented in section 6.4.

Table 6.2: Controller gains used for the purpose of verification by simulation.

Controller	Gain label	Gain value	Gain unit	Bandwidth
Phase currents	k_{dq_p}	8.87	$\mathrm{V \cdot A^{-1}}$	$2000\,\mathrm{rad \cdot s^{-1}}$
	k_{dp_i}	887	$\mathrm{V \cdot A^{-1} \cdot s^{-1}}$	
Converter energy	k_{en_p}	138	$\mathrm{W \cdot V^{-1}}$	$10\,\mathrm{rad \cdot s^{-1}}$
	k_{en_i}	69	$\mathrm{W \cdot V^{-1} \cdot s^{-1}}$	
Circulating currents	k_{circ_p}	15	$\mathrm{V \cdot A^{-1}}$	$3750\,\mathrm{rad \cdot s^{-1}}$
	k_{circ_i}	532	$\mathrm{V \cdot A^{-1} \cdot s^{-}1}$	
DC voltage	k_{dc_p}	0.083	$\mathrm{A \cdot V^{-1}}$	$12.7\,\mathrm{rad \cdot s^{-1}}$
	k_{dc_i}	0.83	$\mathrm{A \cdot V^{-1} \cdot s^{-1}}$	
Phase balancing	k_{pb_p}	0.014	$\mathrm{A \cdot V^{-1}}$	$20\,\mathrm{rad \cdot s^{-1}}$
	k_{pb_i}	0.007	$\mathrm{A \cdot V^{-1} \cdot s^{-1}}$	
Arm balancing	k_{ab_p}	69.2	$\mathrm{W \cdot V^{-1}}$	$8\,\mathrm{rad \cdot s^{-1}}$
	k_{ab_i}	692	$\mathrm{W \cdot V^{-1} \cdot s^{-1}}$	
Parameter x	k_{x_p}	0.3		$6.9\,\mathrm{rad \cdot s^{-1}}$
	k_{x_i}	1	s^{-1}	
PLL	k_{pll_p}	10	$\mathrm{rad \cdot s^{-1} \cdot V^{-1}}$	$86000\,\mathrm{rad \cdot s^{-1}}$
	k_{pll_i}	500	$\mathrm{rad \cdot s^{-2} \cdot V^{-1}}$	

A very high bandwidth value for the PLL loop is not driven by the application requirements, and would not be appropriate for the non-ideal grid voltages. However, in the ideal simulation environment, the selected PI controller parameters provide perfect grid voltages angle tracking and decomposition to the d and q axis voltages.

The DC voltage reading is used as a feed-forward term in the circulating current controllers (Fig. 5.6, Chapter 5). If one sample delay compensation is not applied during the pulse instant, a spike will be present in the DC current and circulating currents. This is due to an error in the DC voltage reference being roughly 1.4 kV during the whole switching period. Even though this spike is present, the converter AC side would not be affected, thus achieving low AC power fluctuation. However, to avoid the spike in the DC current, the droop in the DC voltage reading is shifted one sample forward.

The modulation is performed with the same switching frequency, i.e. the frequency of the carrier is equal to 10 kHz, while each cell switches at lower frequency. As described in section 4.3, in the case of NLC + PWM method, the sorting at every sampling instant causes unnecessary switching. Therefore, to reduce the switching frequency of each cell, the sorting is performed every 20th (number of cells) sampling period, i.e. at 500 Hz. In this condition, the cell capacitor voltages of 20 cells within an arm might not be perfectly balanced and the assumption that all cell capacitor voltages can be approximated with the average cell capacitor voltage is not correct. To get the modulation working correctly, the algorithm from Fig. 4.4 (section 4.3) has to be modified. As suggested in [98], instead of normalising the reference with the average voltage of all cells in an arm, the carrier amplitudes (or the potential levels) can be scaled up with the cell capacitors voltages according to the sorting order.

6.3 Performance of the PLL and klystron modulator emulation

In order to set the grid connected converter control in the d, q reference frame, the information about grid phase angle is necessary. Therefore the PLL waveforms are presented first. The grid phase A voltage and grid voltages d and q components and phase angle are given in the Fig. 6.1. The simulation starts at $t = 0$ s and the d, q axis voltages are established shortly after.

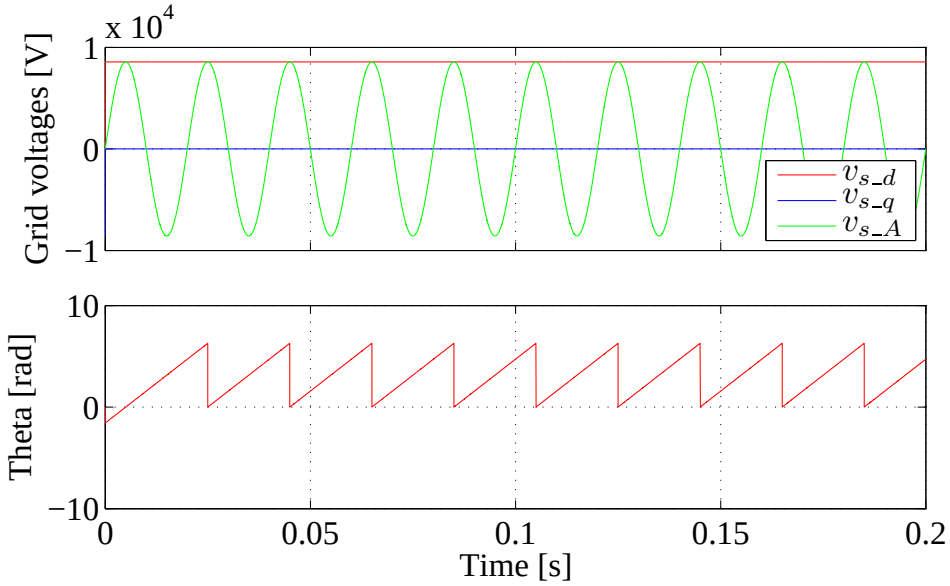


Figure 6.1: Grid voltages and phase angle in transient when the simulation starts.

The klystron modulators draw short high current pulses in order to provide high voltage pulse on the klystron inputs. By doing so, a DC link capacitor is discharged and a voltage droop is present in the DC voltage. Before validating a converter under such kind of load, it is important to present the load characteristics.

The pulsed load current and the DC voltage are observed under steady state conditions when arm balancing method one is applied. Fig. 6.2 presents pulsed load characteristics, showing the periodical discharge of the DC link capacitor by a high pulsed current. Peak pulse current of the numerous klystron modulators corresponding to the converter rated power is approximately 120 kA.

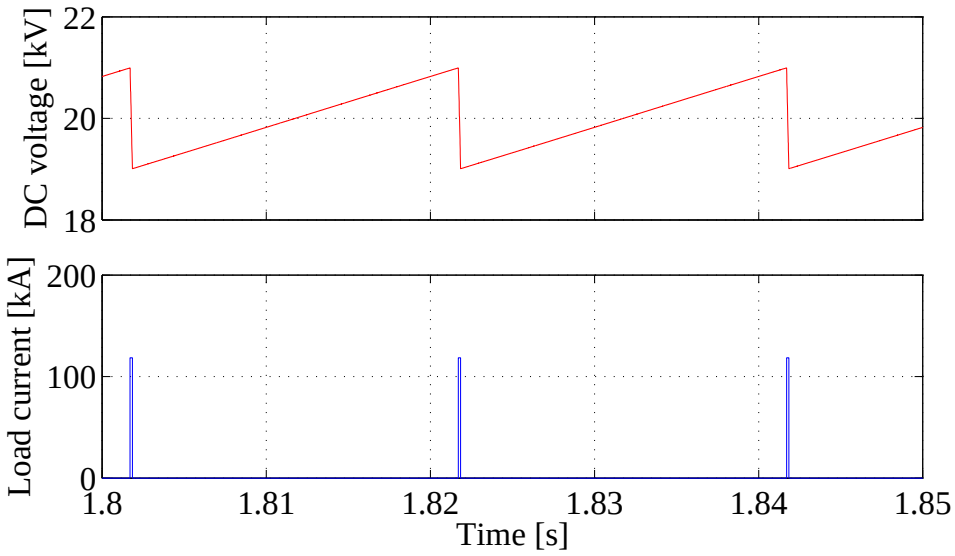


Figure 6.2: Pulsed load characteristics: DC voltage and load current under steady state conditions.

The actual load current might not be constant during the pulse, however this idealised case is a simple way to model the pulsed load while providing the similar effects on the DC voltage as the effects produced by klystron modulators. From the perspective of controller design verification and converter behaviour, the DC voltage waveform is more important than the load current shape. The DC voltage ripple harmonics are presented in Fig. 6.3. As discussed in Chapter 5, the significant amplitude of 50 Hz component is present since the pulse repetition rate is 50 Hz.

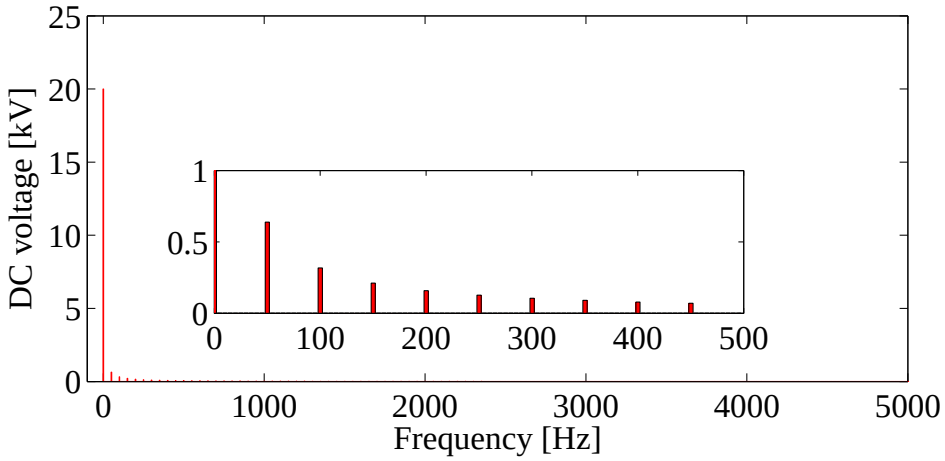


Figure 6.3: DC voltage harmonics under steady state conditions when arm balancing method one is applied.

6.4 Validation of control loops

The aim of this section is to present the characteristic waveforms relevant to all controllers from Chapter 5. The highest importance is given to the phase and circulating current controllers. The quality of the AC currents directly influence the grid power quality, therefore they are analysed for all the arm balancing methods. In addition circulating current controller references are particular for every arm balancing method, thus requiring the circulating current analysis for all of them. The phase current and circulating current controllers have the same gains for all arm balancing methods, hence the PI variables are presented only in the case of arm balancing method one. In addition the validation of the slow voltage controllers, including energy, DC voltage and phase balancing controllers is presented only for the case of arm balancing method one.

6.4.1 Phase current controller

When the simulation starts the AC power demand is set to 1.66 MW, and the d, q axis current references are computed according to the power demand and grid d, q axis voltages. The d, q axis currents start following their references, as it is presented in Fig. 6.4 for the case of arm balancing method one. The d, q axis currents have a small overshoot, and approximately 20 ms after the simulation starts they reach their references.

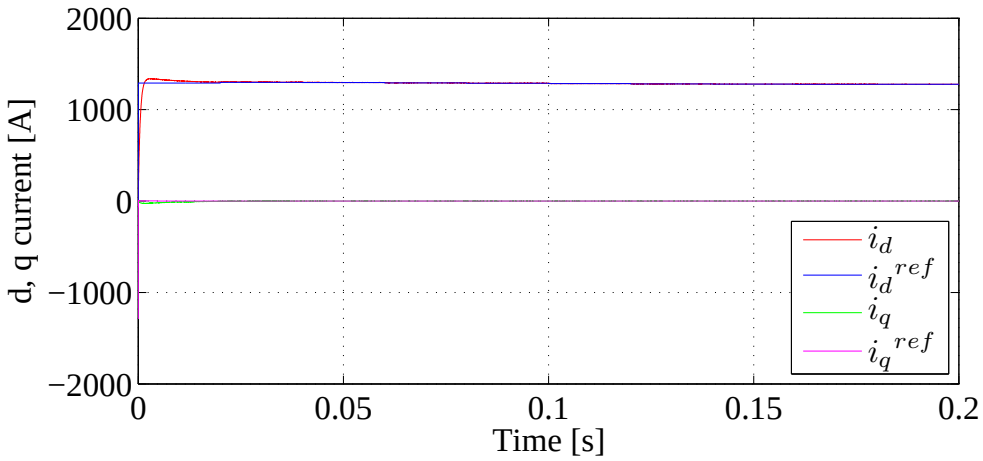


Figure 6.4: The d, q current controller reference tracking during transient in the case of arm balancing method one.

The generation of the d, q component of the AC voltage reference, is based on the feed-forward grid voltage components and the d, q current controller output (Fig. 5.2), as presented in Fig. 6.5. Since there is no resistance in the phase and arm inductors, the d axis component of the grid and converter AC voltage is almost equal, while the converter voltage has q component associated with the voltage drop across the inductors.

The grid active power and its reference during transient are presented in Fig. 6.6. The AC power reference is constant over a 20 ms period, since it is corrected by the converter energy controller. Similarly to the d, q axis currents, a small overshoot is

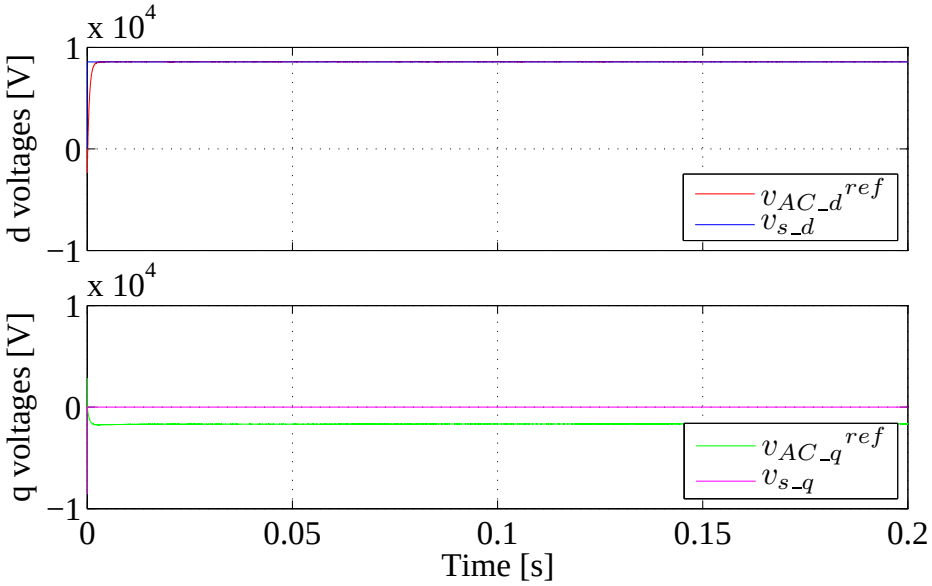


Figure 6.5: Grid voltage and the converter AC voltage d, q components during transient in the case of arm balancing method one.

present, while the settling time is approximately 20 ms.

The performance of the d, q axis current controller under steady state conditions is presented in Fig. 6.7. The current references are followed and the same amount of ripple (approximately 2 A) is present in both d and q axis current components.

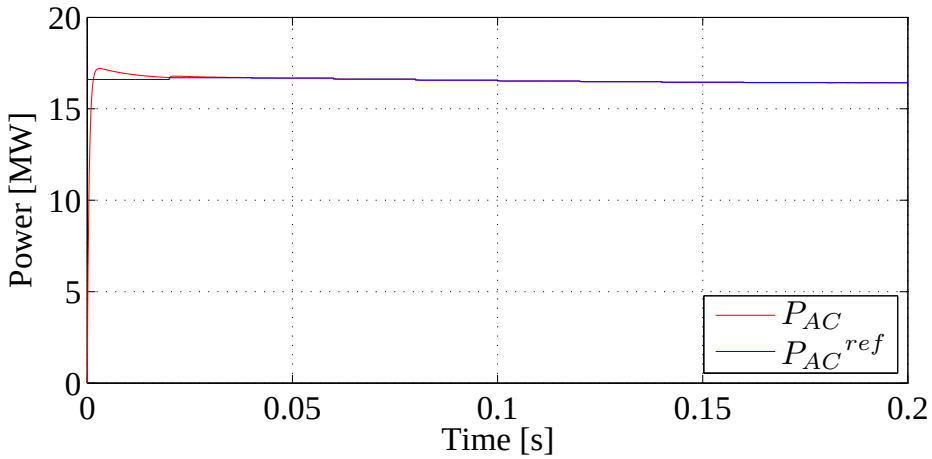


Figure 6.6: Grid active power and its reference during transient in the case of arm balancing method one.

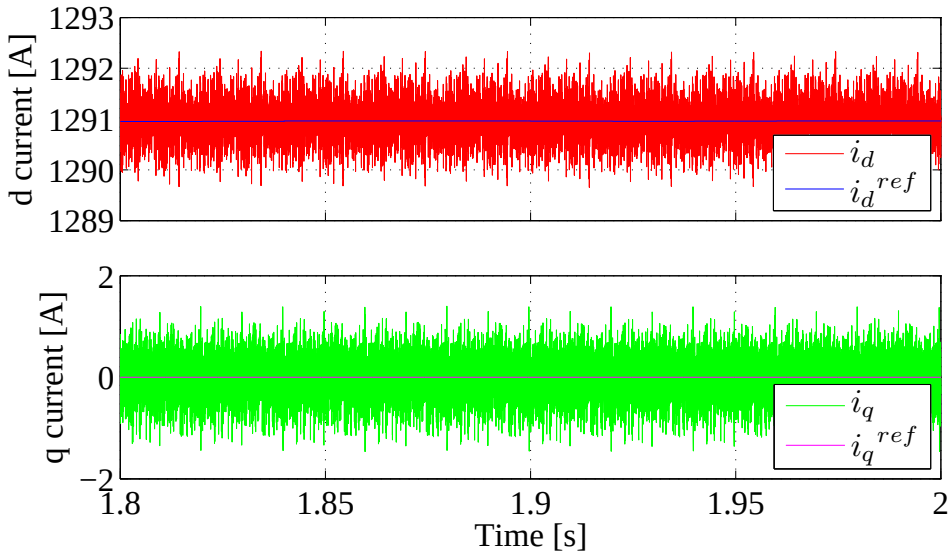


Figure 6.7: The d, q current controller reference tracking under steady state conditions with pulsed load when arm balancing method one is applied.

Fig. 6.8 shows grid instantaneous power and its reference and DC power delivered to the load under steady state conditions with the pulsed DC load. The presented case corresponds to the arm balancing method one. The amount of AC power ripple

is approximately 30 kW which considering rated power of 16.6 MW, corresponds to 0.18 %. At the moment of the pulse occurrence, there is no distortion present in the AC power, although the DC power reflects pulsed load behaviour.

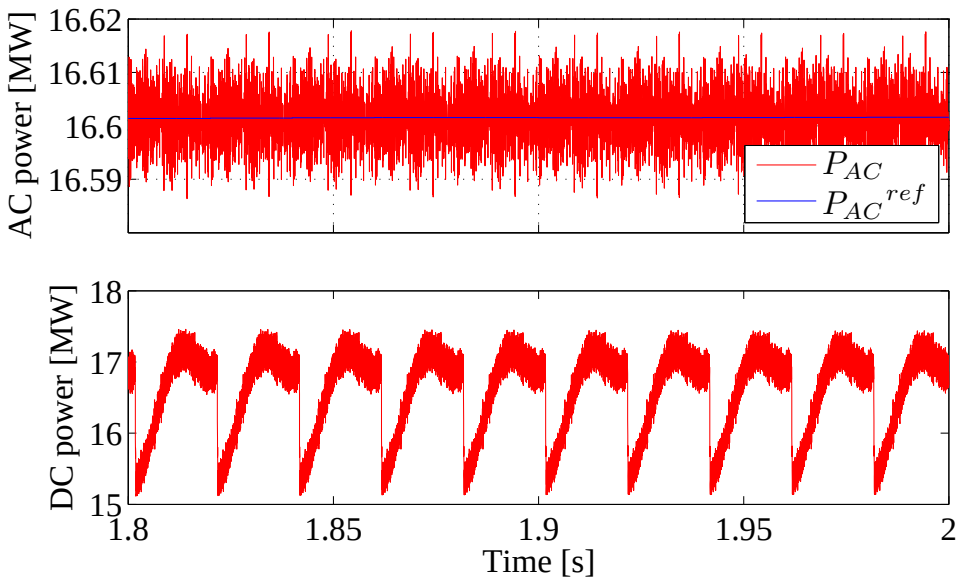


Figure 6.8: Grid active power and its reference and the converter DC power under steady state conditions with pulsed load when arm balancing method one is applied.

The grid power harmonics are observed in order to check the low harmonic content which is hard to filter out. Fig. 6.9 presents the grid power harmonics with the emphasis to the low frequency region where non of the amplitudes is higher than 0.006 % of the nominal power.

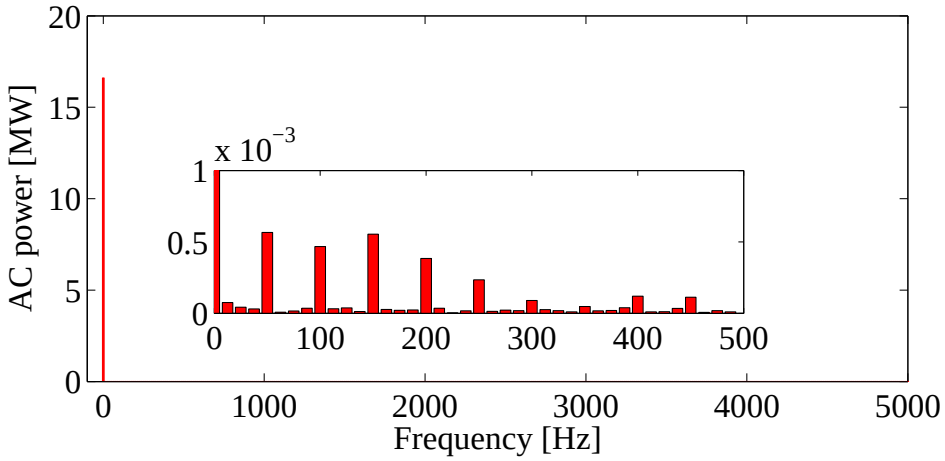


Figure 6.9: Grid active power harmonics under steady state conditions with pulsed load when arm balancing method one is applied.

6.4.1.1 Phase current waveform quality

The waveforms of the three phase AC currents are analysed together with their low fequency spectrum as a measure of grid current quality. Figs. 6.10 and 6.11 present the phase currents and their spectrum under steady state conditions with the pulsed DC load when arm balancing method one is applied.

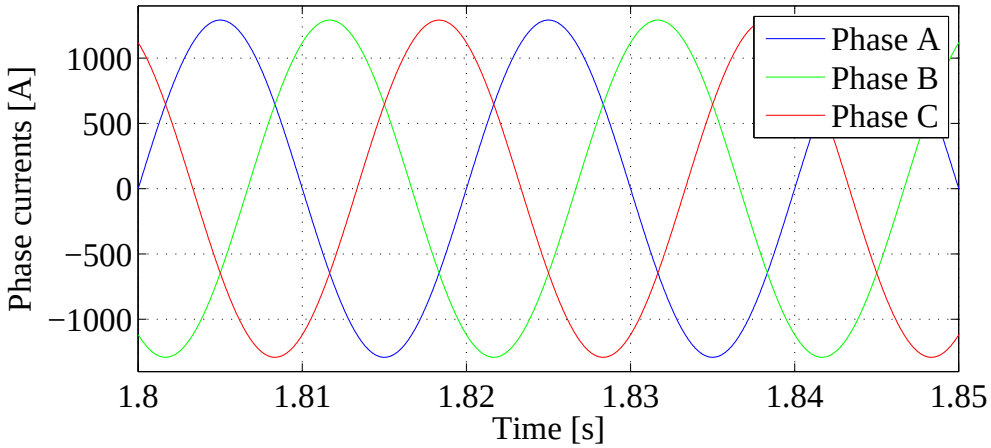


Figure 6.10: Phase/grid currents under steady state conditions with pulsed DC load, when arm balancing method one is applied.

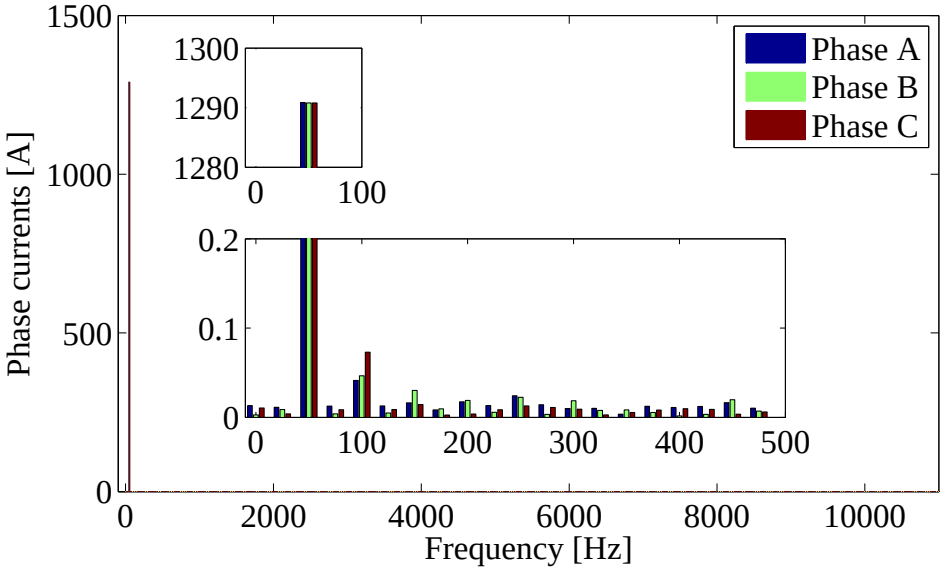


Figure 6.11: Phase/grid currents spectrum under steady state conditions with pulsed DC load, when arm balancing method one is applied.

From Fig. 6.11 it can be seen that the fundamental component of all three phases is equal, meaning that the phases are perfectly balanced. The low frequency spectrum contains only components with amplitudes below 0.1 A, giving very low THD of approximately 0.19 %.

Figs. 6.12 and 6.13 present the phase currents and their spectrum under steady state conditions with the pulsed DC load when arm balancing method two is applied.

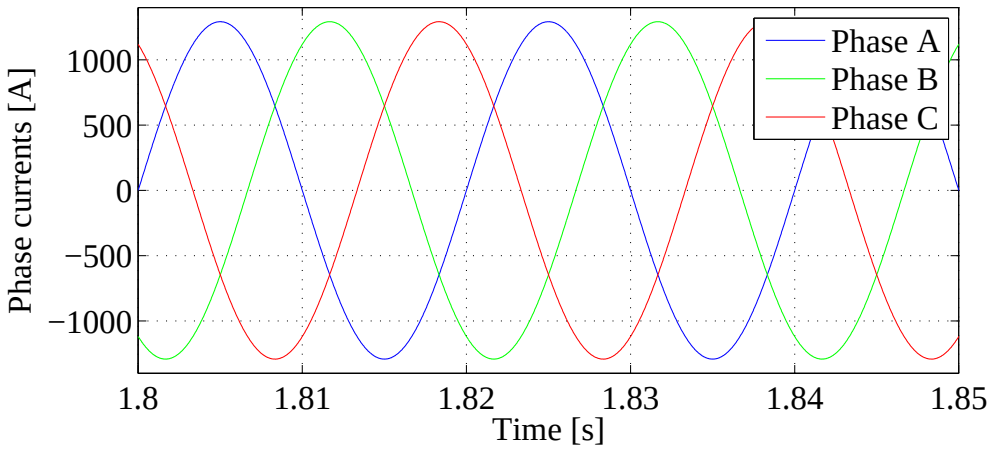


Figure 6.12: Phase/grid currents under steady state conditions with pulsed DC load, when arm balancing method two is applied.

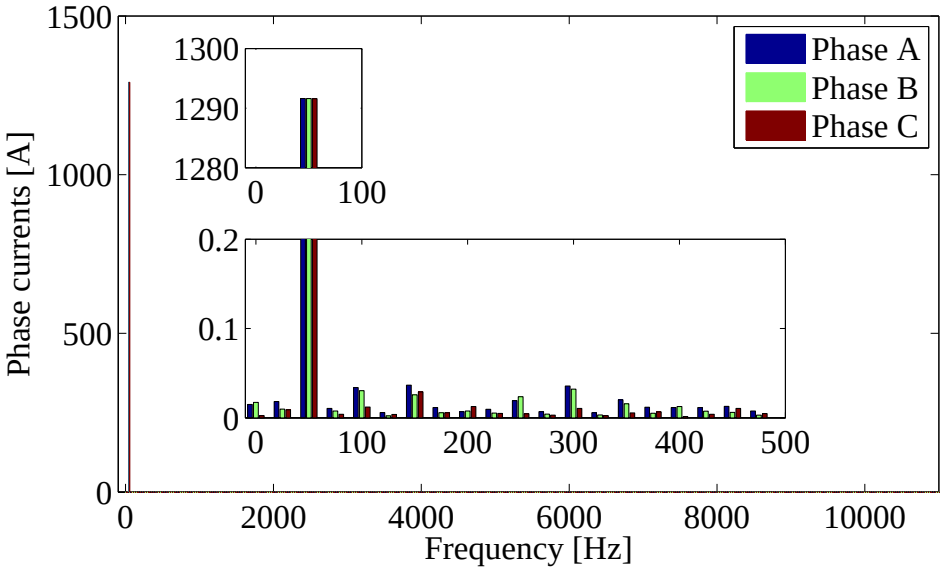


Figure 6.13: Phase/grid currents spectrum under steady state conditions with pulsed DC load, when arm balancing method two is applied.

In the case of arm balancing method two, the low harmonic spectrum is similar to

the case of arm balancing method one, with the components lower than 0.1 A. The obtained THD is approximately 0.19 %.

The phase currents and their harmonic spectrum for the converter with the pulsed DC load when arm balancing method three is applied are presented in Figs. 6.14 and 6.15, respectively. The presented waveforms are obtained under steady state conditions.

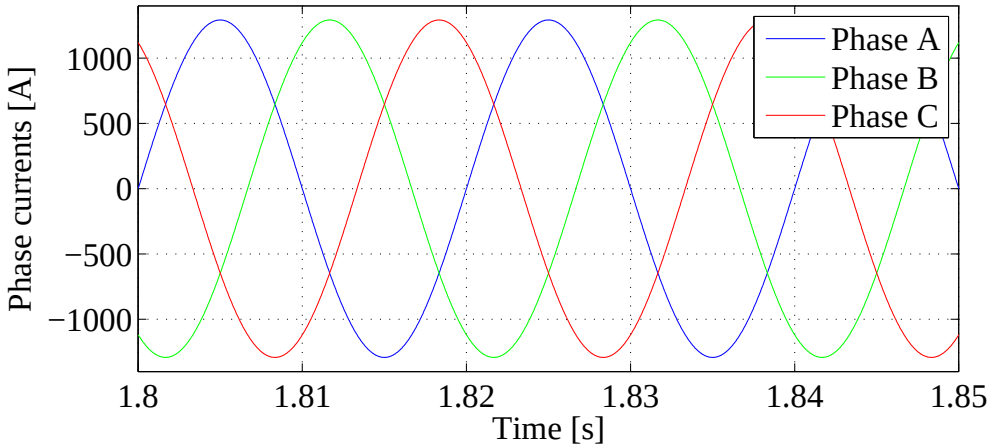


Figure 6.14: Phase/grid currents under steady state conditions with pulsed DC load, when arm balancing method three is applied.

The obtained spectrum of the phase currents when the arm balancing method three is applied is similar to the spectrum in the cases of methods one and two. The obtained THD is somewhat lower than in the previous two cases; approximately 0.15 %.

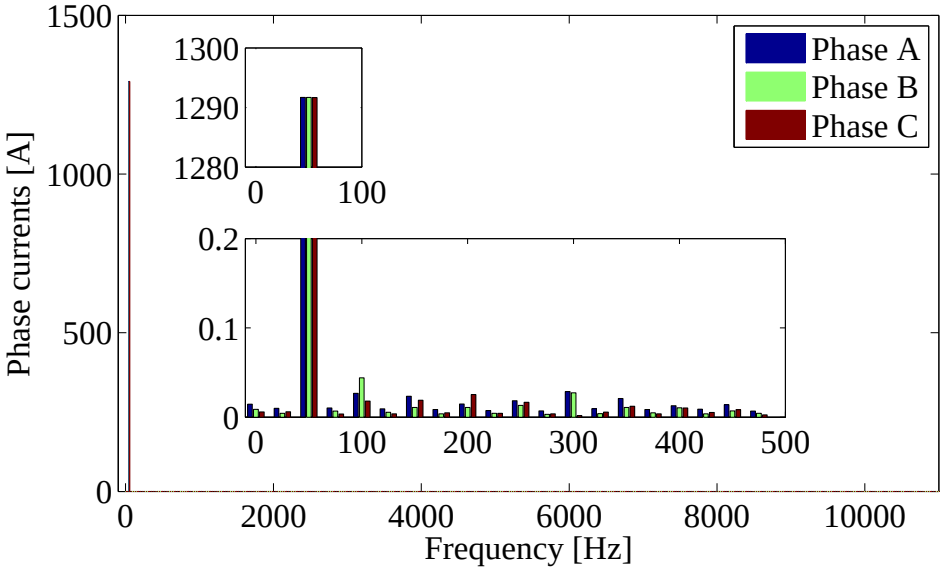


Figure 6.15: Phase/grid currents spectrum under steady state conditions with pulsed DC load, when arm balancing method three is applied.

6.4.1.2 Energy control

Fig. 6.16 presents the PI controller waveforms used for the control the sum of all cell capacitor voltages, i.e. the energy stored in the converter. The presented waveform relate to the transient when simulation starts, for the converter with pulsed DC load, when arm balancing method one is applied.

The sum of all cell capacitor voltages and its reference is presented in the Fig. 6.17. The sum of all cell capacitors reaches its reference at approximately $t = 1\,\mathrm{s}$.

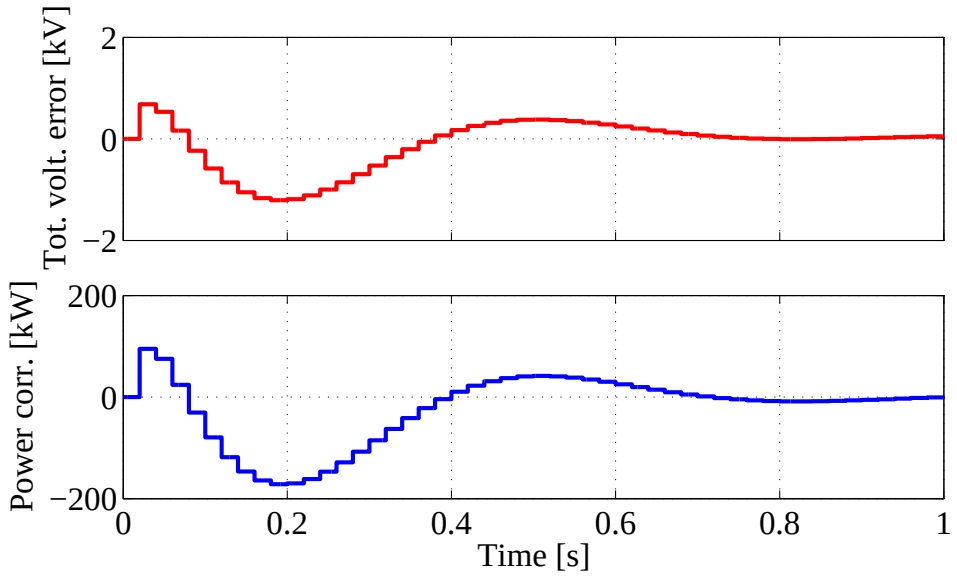


Figure 6.16: The converter energy controller waveforms during transient when the simulation starts.

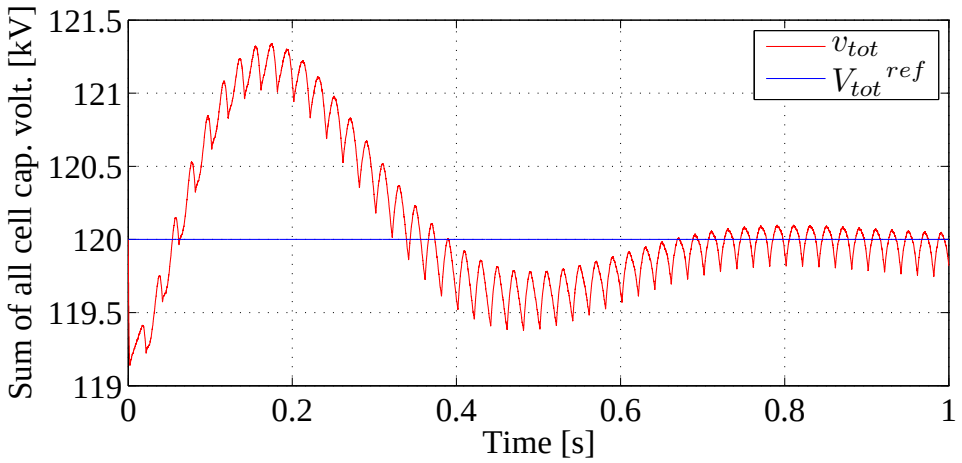


Figure 6.17: Sum of all cell capacitor voltages and its reference during transient when the simulation starts.

6.4.2 Circulating current controller

The circulating current and its reference during transient when the simulation starts (from zero current to the nominal current with the 50 Hz arm balancing component) when arm balancing method one is applied is presented in Fig. 6.18.

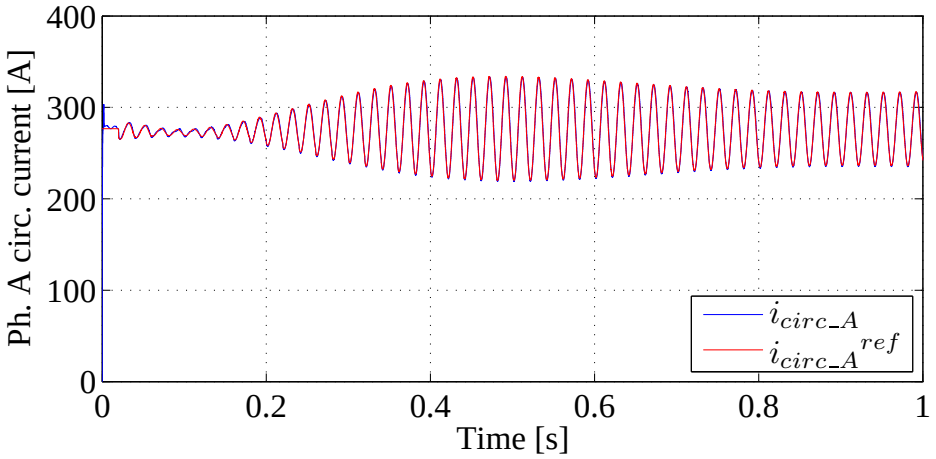


Figure 6.18: Phase A circulating current and its reference when arm balancing method one is applied during transient when the simulation starts.

The circulating current controller is used to generate the DC part of the voltage reference of the particular phase. The DC voltage reading (compensated for the one sample delay) is fed-forward in order to generate the DC part of the reference. In the case of arm balancing method one, the DC part of the arm voltages reference of the phase A together with the DC voltage is presented in Fig. 6.19.

6.4.2.1 Circulating current waveforms

The spectrum of the phase A circulating current and its reference is shown in Fig. 6.20 for the arm balancing method one. The DC part of the circulating current is equal in all the phases, while the 50 Hz component is produced by the arm balancing controller and is different in phases A, B and C. It can be seen that the circulating

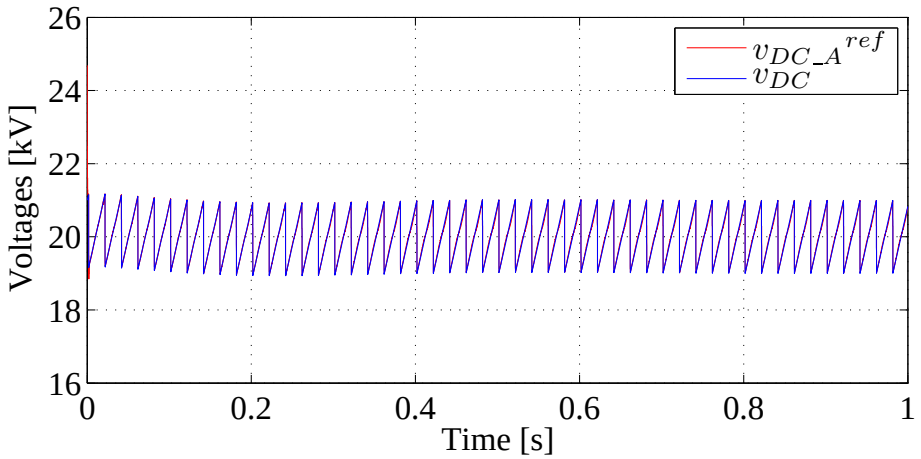


Figure 6.19: Phase A DC part of the reference and DC voltage during transient when the simulation starts.

current follows its reference with the very small delay in 50 Hz component tracking, due to the use of high bandwidth PI (not resonant controller).

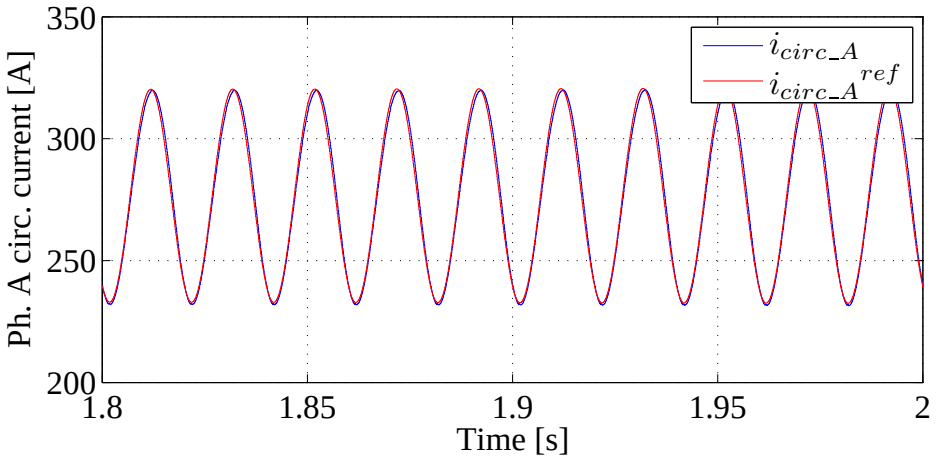


Figure 6.20: Phase A circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method one is applied.

Fig. 6.21 presents the phase A circulating current and its reference spectrum in the case when arm balancing method one is applied. As it is presented both the mean value and the 50 Hz component of the circulating current follow their references.

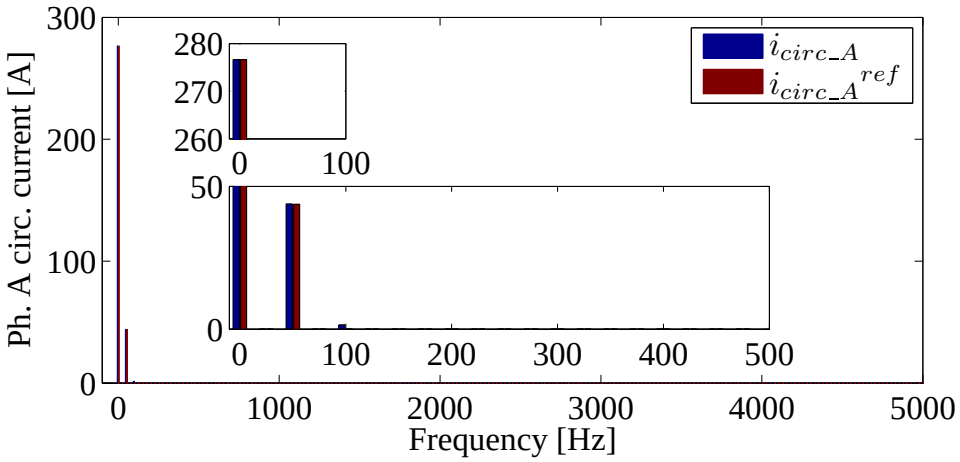


Figure 6.21: Spectrum of the circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method one is applied.

In addition, there is a low amplitude 100 Hz component present, which does not contribute to the arm or phase cell capacitor voltages imbalance.

Fig. 6.22 presents the phase A circulating current and its reference in the case when arm balancing method two is applied. The amplitude of the 50 Hz component in the circulating current is smaller when compared to the case with arm balancing method one. The circulating current is following its reference, and again a small delay is present.

The spectrum of the phase A circulating current and its reference in the case of arm balancing method two, is shown in Fig. 6.23. The tracking of the reference mean value and 50 Hz component is clear. There is a small 100 Hz component in the circulating current (which is not present in the reference) with the same amplitude as in the case of arm balancing method one.

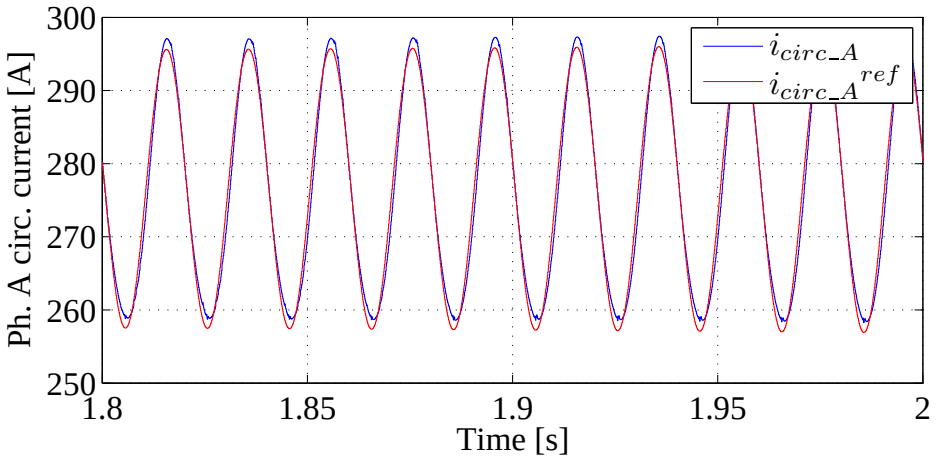


Figure 6.22: Phase A circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method two is applied.

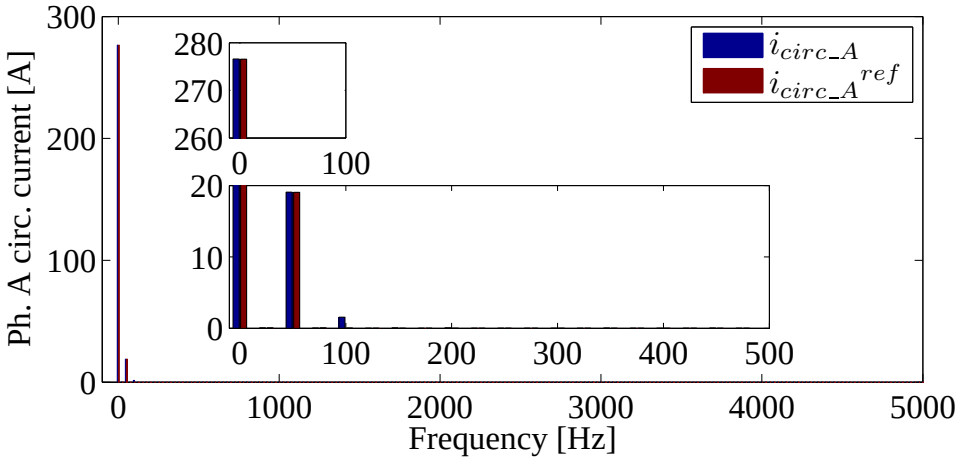


Figure 6.23: Spectrum of the circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method two is applied.

Fig. 6.24 presents the phase A circulating current and its reference in the case when arm balancing method three is applied. In this case the circulating current reference is constant, while the 50 Hz component in the circulating current is present due to the uneven distribution of the AC part of the reference among converter arms.

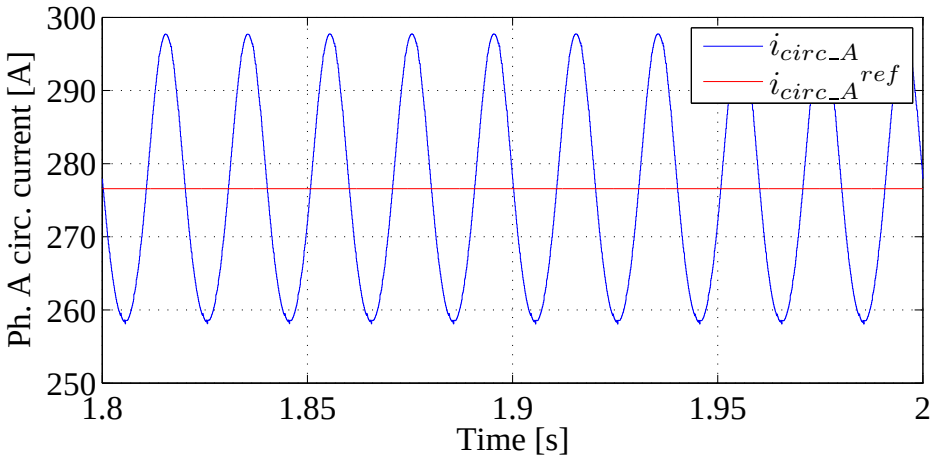


Figure 6.24: Phase A circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method three is applied.

The spectrum of the phase A circulating current and its reference in the case of arm balancing method three, is presented in Fig. 6.25. The mean value of the circulating current is following its reference. The 50 Hz component of the circulating current is somewhat higher than in the case of the arm balancing method two. The 100 Hz component in the circulating current has a similar amplitude as in the case of both arm balancing methods one and two.

6.4.2.2 DC voltage controller

The DC voltage controller is producing a DC current reference in order to keep the average DC voltage at the correct level (Fig. 5.8). The controller output together with the nominal DC current (830 A) as a feed-forward term is set as a DC current reference. The produced reference is constant and it corresponds to the DC current average value. The DC current might have additional 50 Hz ripple as a consequence of the arm balancing controllers.

The DC voltage PI controller waveforms are presented in Fig. 6.26 during the transient when the simulation starts. The DC voltage error, i.e. the difference between the

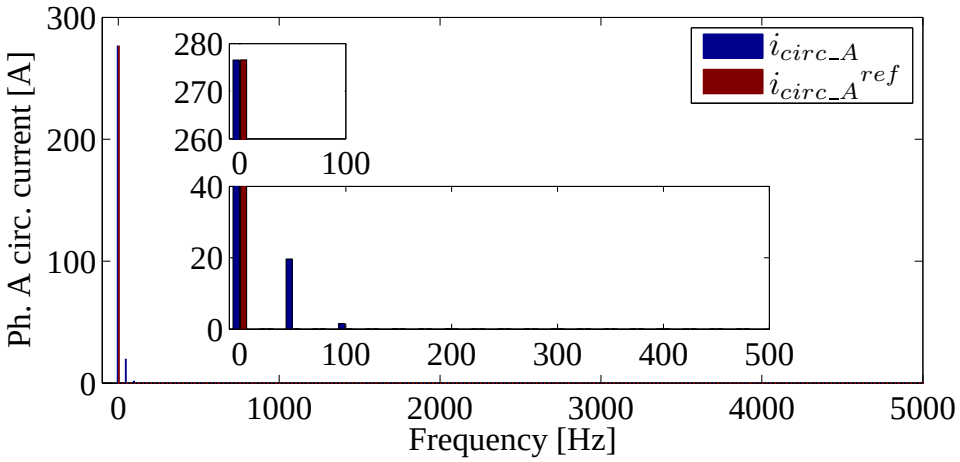


Figure 6.25: Spectrum of the circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method three is applied.

DC voltage reference and the DC voltage averaged over 20 ms period, is converging towards zero in approximately 1 s.

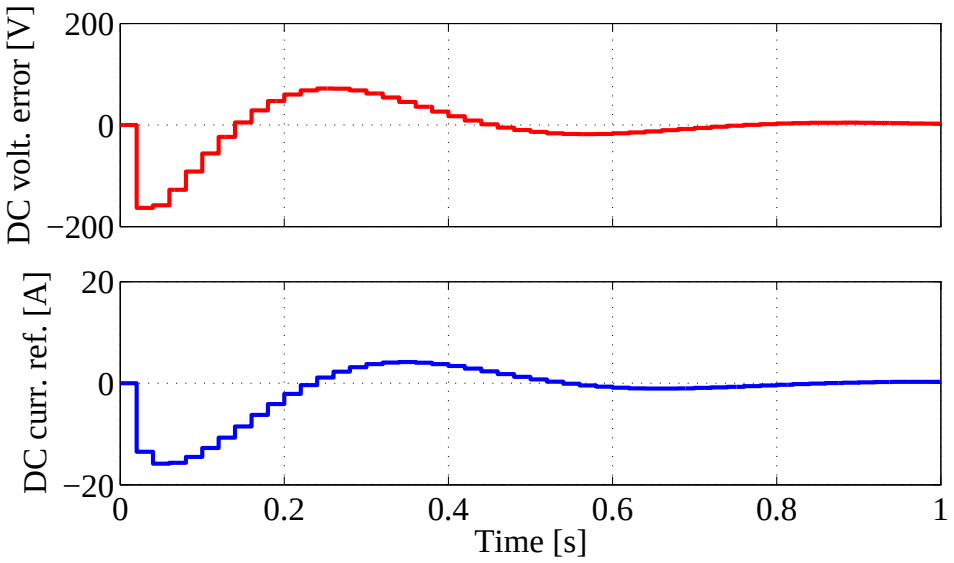


Figure 6.26: DC voltage error and controller output correcting DC current reference during transient when simulation starts.

The DC voltage and its reference are presented in Fig. 6.27 during the transient when

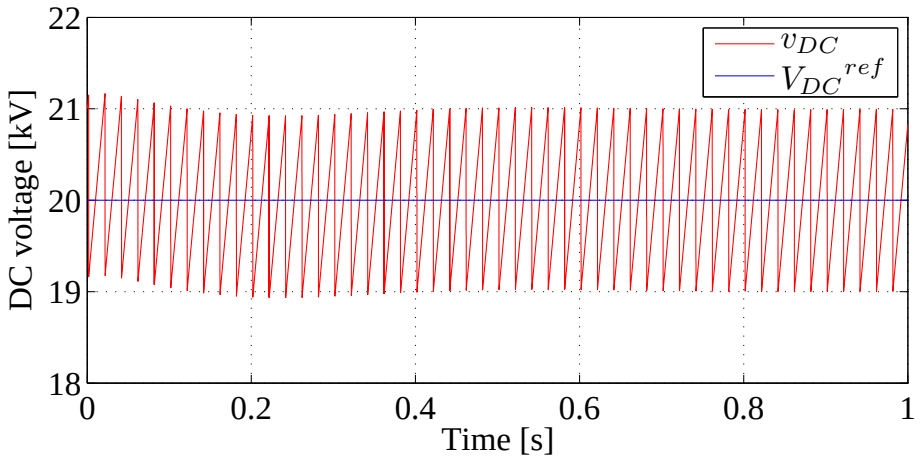


Figure 6.27: Converter DC voltage and its reference during transient when simulation starts.

the simulation starts. The DC voltage was precharged to the nominal average value, but due to the transient in phase and circulating current controllers and depending on the pulse position, there is a transient in the DC voltage.

The DC current waveforms for the three arm balancing methods, under steady state conditions with the pulsed DC load is presented in Fig. 6.28. For the given pulse position, the resulting 50 Hz component of the DC current ripple is significantly lower in the case of arm balancing method one when compared to arm balancing methods two and three.

6.4.2.3 Phase balancing

Phase balancing loop ensures equal distribution of the energy stored in the converter cell capacitors among converter phases. Equal stored energy corresponds to equal sum of cell capacitors voltages in all three phases. The performance of the phase balancing controller from Fig. 5.10 is presented in Fig. 6.29 during the transient when the simulation starts.

For the purpose of phase balancing, the reference for the sum of all cell capacitor

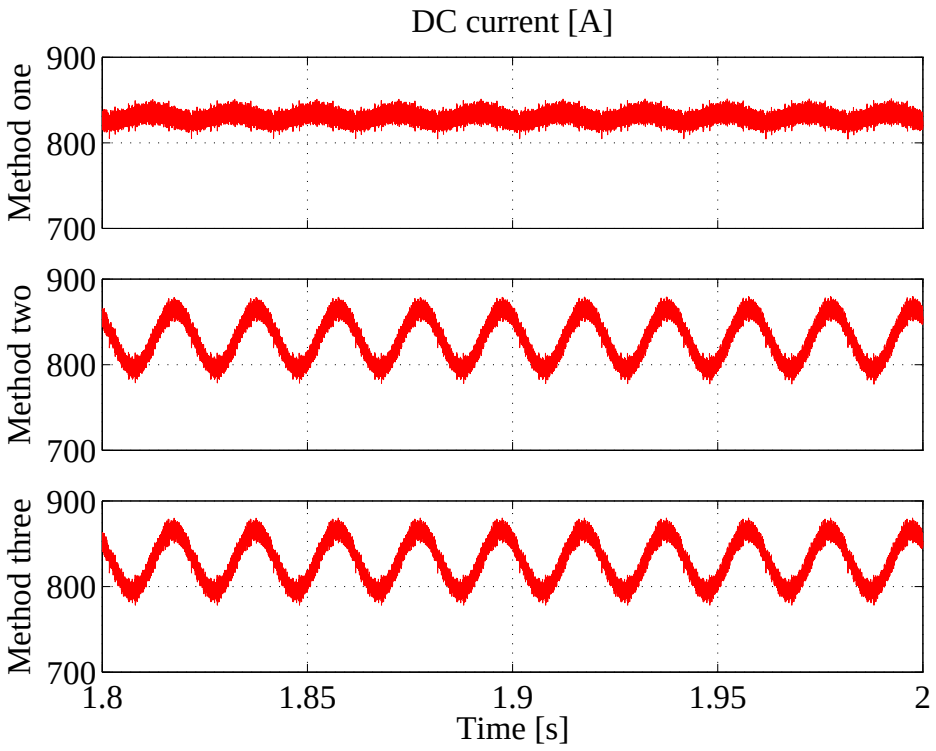


Figure 6.28: Converter DC current under steady state conditions for three arm balancing methods.

voltages of one phase is set to the average value of the sum of the cell capacitor voltages of the three phases. This way each circulating current reference is corrected only for the small DC offset, and the sum of the DC offsets of the three phases results in zero offset in the DC current. The sum of all cell capacitor voltages of phase A, its average value over 20 ms and its reference during the transient is presented in Fig. 6.30.

The transient presented in Fig. 6.30 is mainly related to the transient of the overall energy stored in the converter, while the converter phases are well balanced among each other (the average value of the sum of all cell capacitors is close to its reference).

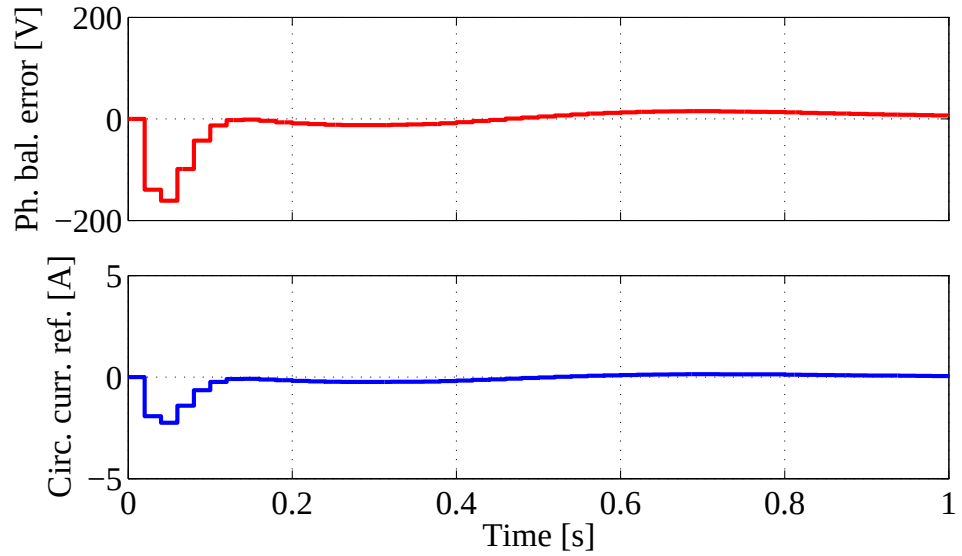


Figure 6.29: Phase balancing error and controller output correcting phase A circulating current reference during transient when the simulation starts.

6.4.2.4 Arm balancing

Since the pulsed DC load has a repetition rate of 50 Hz, the converter DC voltage has a 50 Hz component in its ripple which is a constant source of imbalance between converter arms.

The arm balancing controllers of the methods one and two are based on the PI controller producing the power on its output to compensate for the imbalance induced by the DC voltage ripple. The performance of the arm balancing controller, given with the difference of the sums of cell capacitor voltages of phase A upper and lower arm (as an error) and the compensated imbalance power is presented in Fig. 6.31. The settling time is somewhat longer than 1 s.

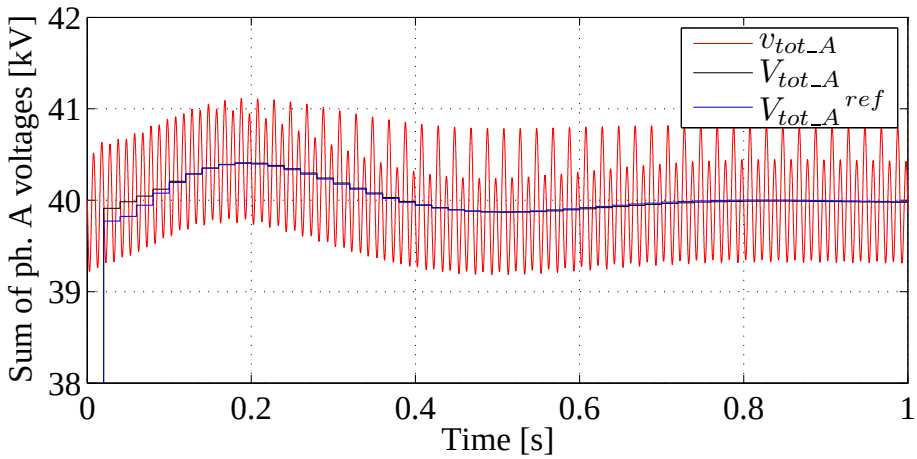


Figure 6.30: Sum of the phase A cell capacitor voltages, average value and the reference during transient when the simulation starts.

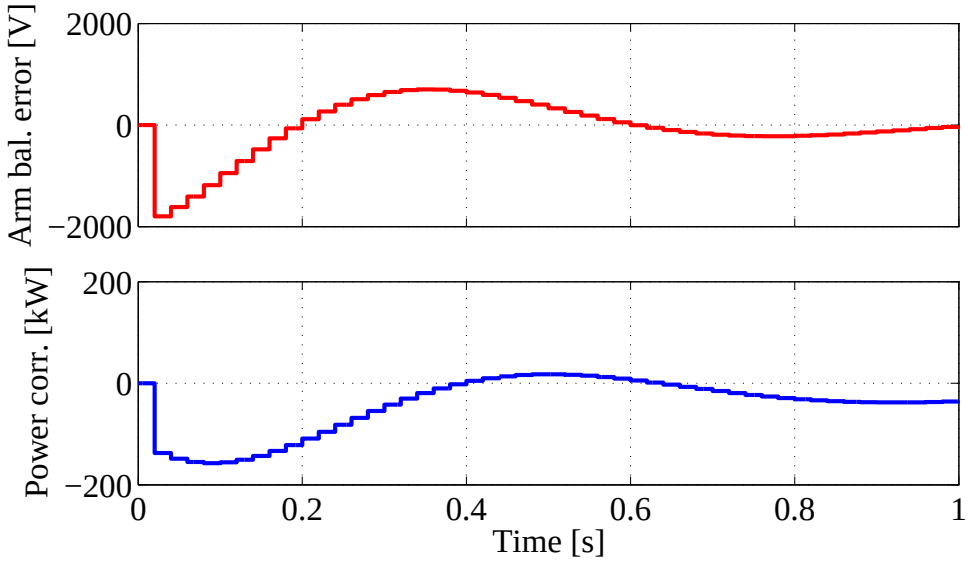


Figure 6.31: Arm balancing error and controller output being the compensated power used for generation of circulating current reference 50 Hz component during transient when the simulation starts.

The sum of cell capacitors of upper and lower arm of phase A under steady state conditions when arm balancing method one is applied, are presented in Fig. 6.32.

The cell capacitors of the two arms are not having equal ripple amplitude, but their average values over 20 ms period are well balanced.

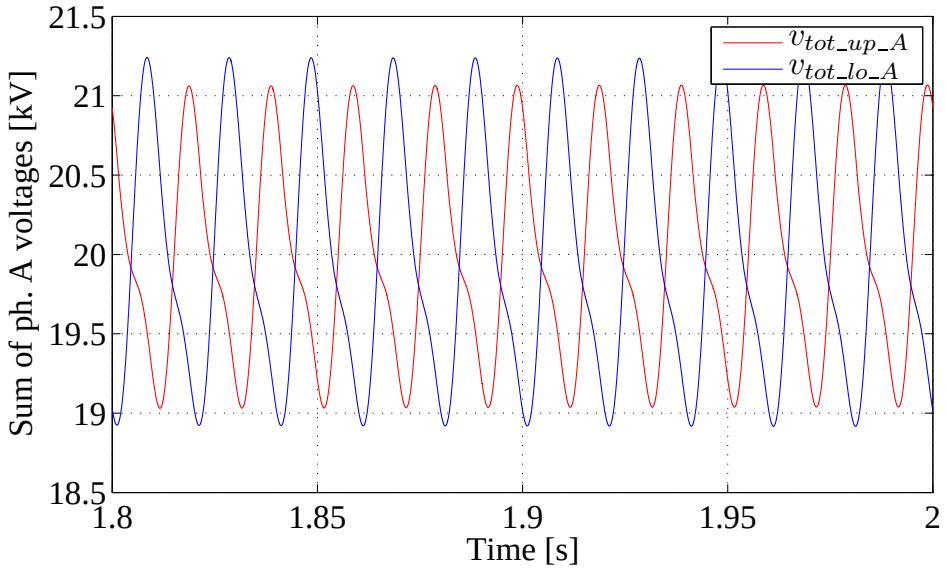


Figure 6.32: Sum of the phase A upper arm and lower arm cell capacitor voltages under steady state conditions when method one is applied.

In the case of arm balancing method one, the three circulating current reference 50 Hz components are in phase (or having opposite phase), with different amplitudes defined by the pulse position. For the presented case, i.e. the pulse position of 0.534 rad, the three circulating current references are presented in Fig. 6.33. For the given pulse position, none of denominators (Fig. 5.14, section 5.6) is close to zero, giving moderate amplitudes of the circulating current that result in the DC current with a very low 50 Hz component (Fig. 6.28).

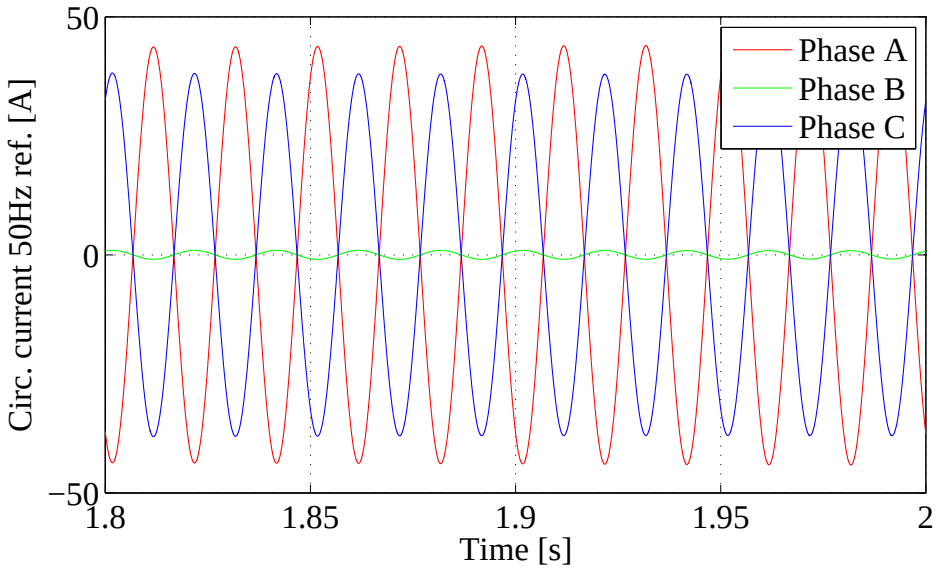


Figure 6.33: Circulating current reference 50 Hz component used for arm balancing under steady state conditions when method one is applied.

Fig. 6.34 presents the sum of the cell capacitor voltages of the phase A upper and lower arm under steady state conditions when arm balancing method two is applied. The average of the two sums is well balanced regardless of the higher ripple in cell capacitor voltages of the lower arm.

Circulating current references required to balance the converter arms, for phase A, B and C, under steady state conditions when arm balancing method two is applied are presented in Fig. 6.35. In this case the 50 Hz components of circulating currents are in phase (or in opposite phase) with the AC voltage reference. The sum of the three references will result in non-zero 50 Hz component of DC current ripple. The presented case relates to the pulse position of 0.534 rad, but the similar amount of the DC current ripple is expected in all pulse positions.

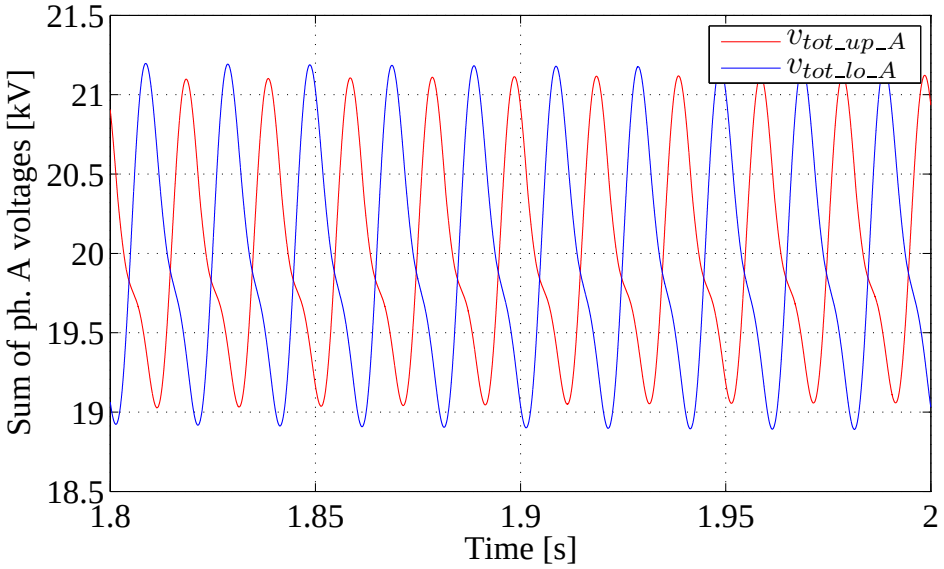


Figure 6.34: Sum of the phase A upper arm and lower arm cell capacitor voltages under steady state conditions when method two is applied.

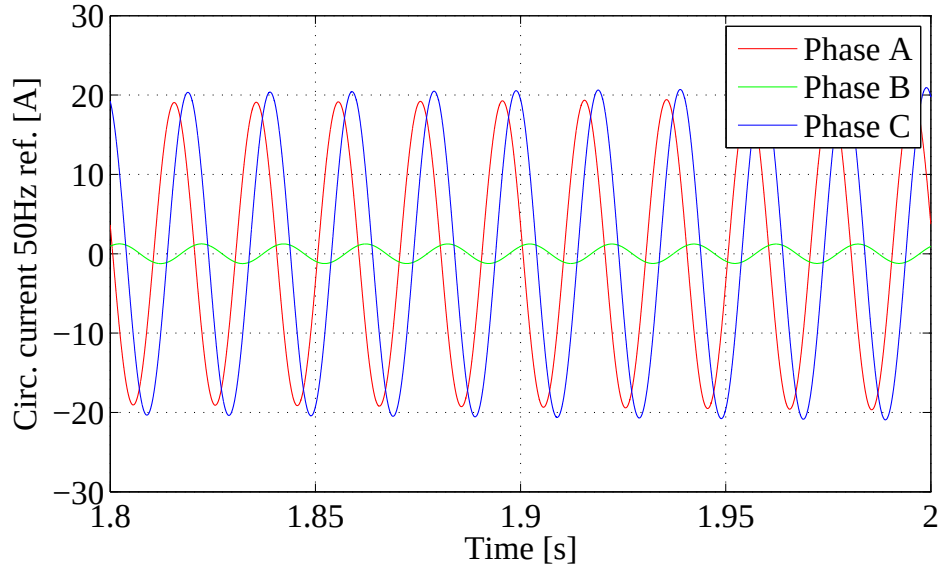


Figure 6.35: Circulating current reference 50 Hz component used for arm balancing under steady state conditions when method two is applied.

Fig. 6.36 presents the sum of the cell capacitor voltages of the phase A upper and

lower arm under steady state conditions when arm balancing method three is applied.

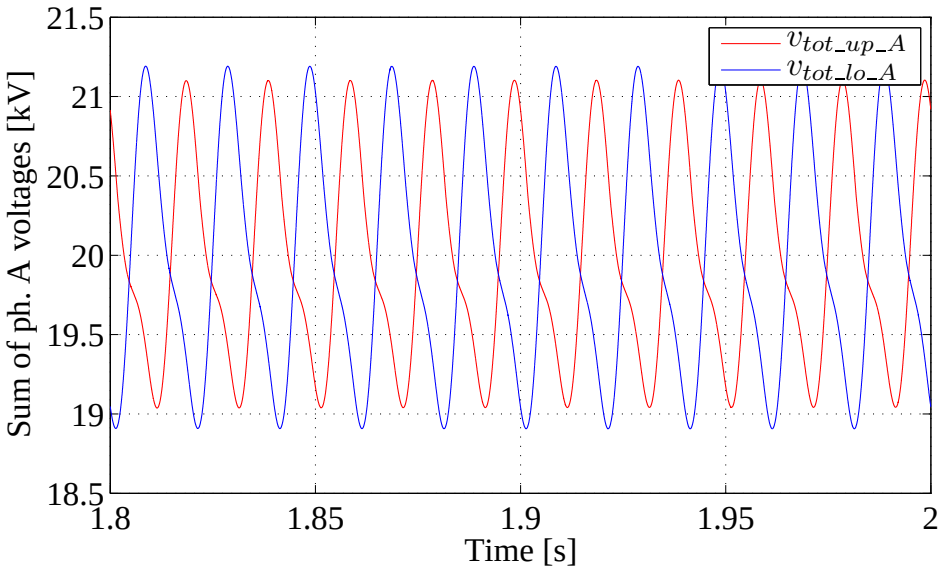


Figure 6.36: Sum of the phase A upper arm and lower arm cell capacitor voltages under steady state conditions when method three is applied.

The values of the x parameter obtained under steady state conditions for the pulse position 0.534 rad are presented in Fig. 6.37. As presented, for the given pulse position, $x_{A,B,C}$ are lower than 0.02, meaning that the AC reference redistribution is less than 2 %. Non-zero values of parameter x mean non-zero 50 Hz component in the circulating current and non-zero amplitude of the 50 Hz component in the DC current.

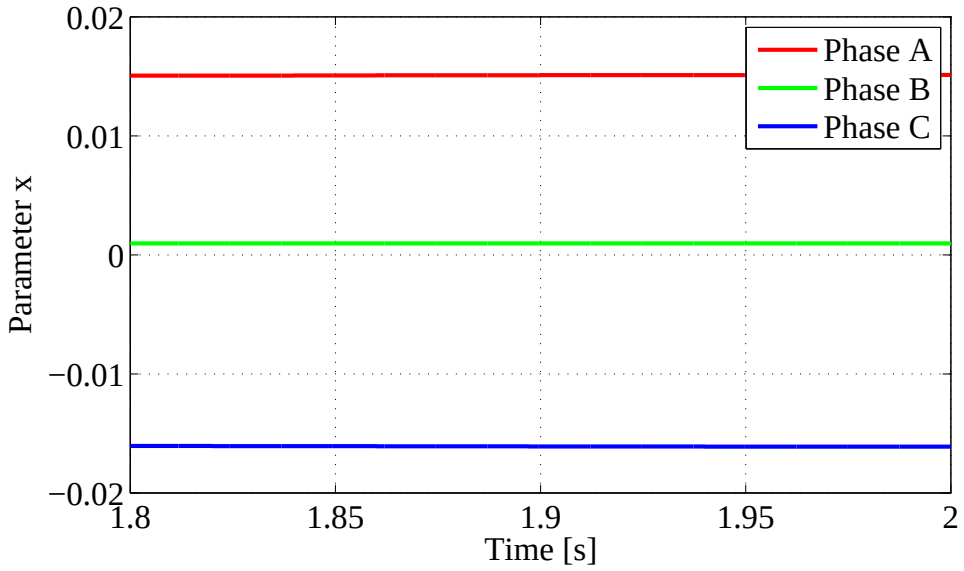


Figure 6.37: Paramter x values used for arm balancing in steady state when method three is applied.

6.4.3 Disabling arm balancing controller

Here, the waveforms of the converter with the pulsed DC load are presented in the case when arm balancing controller is omitted. Since the DC voltage ripple has a 50 Hz component, it affects average arm powers (of the same phase) in an opposite way which causes divergence of cell capacitors voltages of the two arms. The extent in which the pulsed load affects the converter arms is different for different phases, depending on the pulse position (with respect to that phase AC waveforms).

For the given pulse position of 0.534 rad, the phases A and C are more affected than the phase B, causing faster divergence of the cell capacitors voltages in phases A and C with respect to phase B. The divergence of the cell capacitor voltages of the converter arms caused by the pulsed DC load is presented in Fig. 6.38.

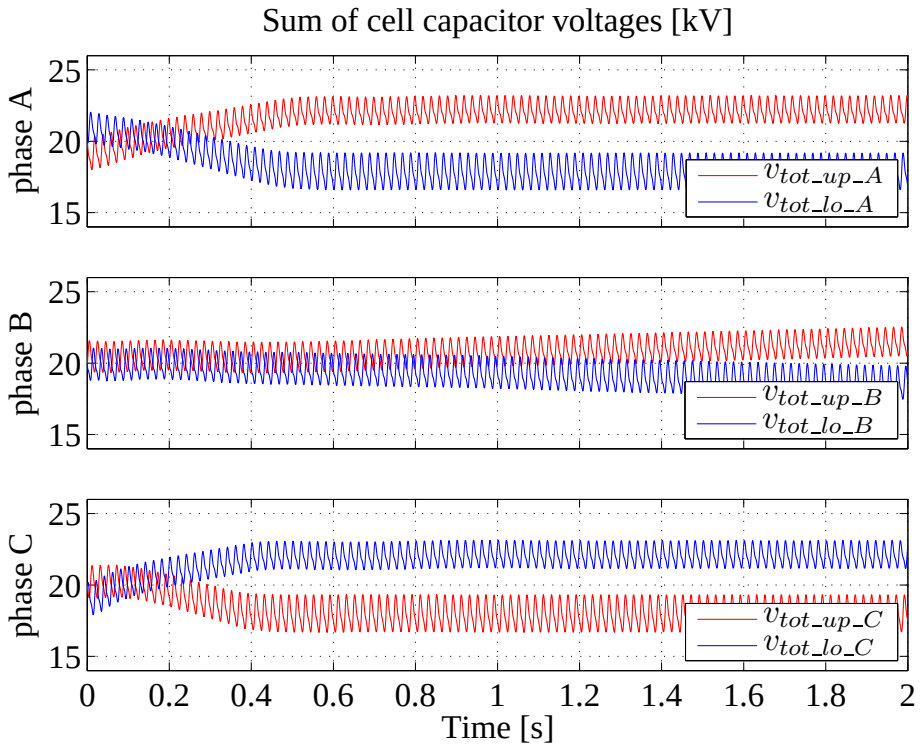


Figure 6.38: The sum of cell capacitor voltages of converter arms when arm balancing controller is disabled.

Once the sum of cell capacitors voltages of any of the arms becomes lower than its reference signal (arm voltage reference) the overmodulation of that arm occurs. At the specific moment, overmodulation brings average arm powers to zero, and the divergence of the arm voltages stops. For phase A this happens at $t = 0.5\,\mathrm{s}$, while for phase C it happens approximately at $t = 0.4\,\mathrm{s}$, as presented in Fig. 6.38. The overmodulation causes notches in the arm voltages at the points where reference is higher than the available voltage of that arm (sum of all cell capacitors of that arm), as presented in Fig. 5.13, Chapter 5. The converter phase voltages with respect to the grid neutral, 1.8 s after the simulation starts are presented in Fig. 6.39. At this point the overmodulation has already occurred in phases A and C, but not in phase B.

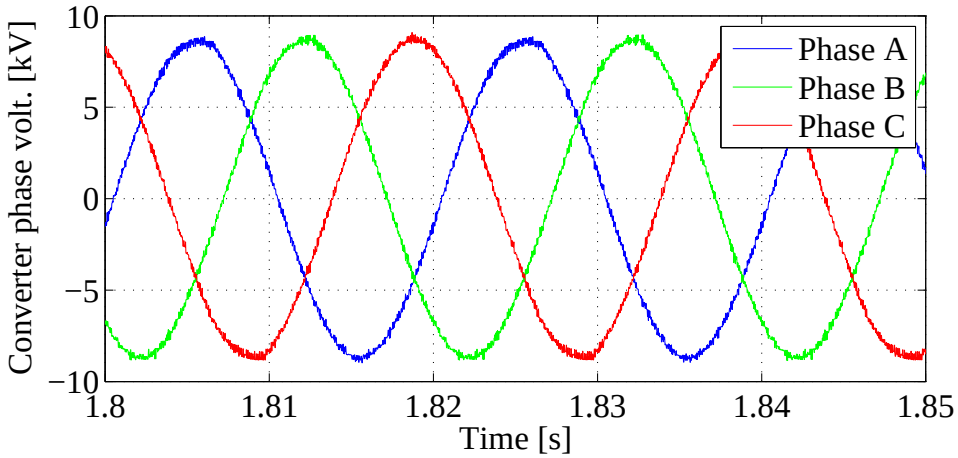


Figure 6.39: Phase voltages when the arm balancing controller is disabled.

The harmonic spectrum of the phase voltages from Fig. 6.39 are presented in Fig. 6.40. Regardless the fact that the overmodulation is not present in the phase B, all three phases have similar amplitudes of low frequency harmonics.

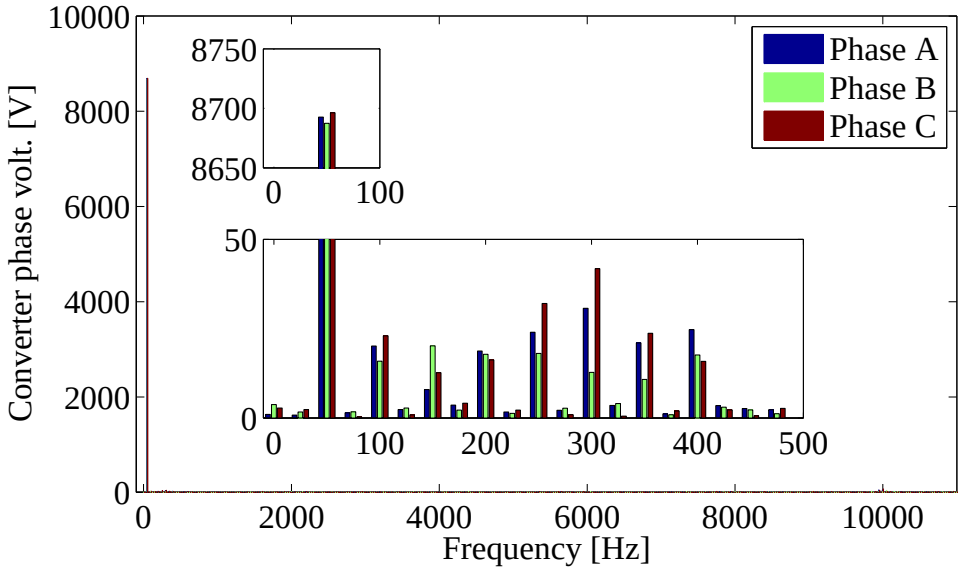


Figure 6.40: Phase voltages spectrum when the arm balancing controller is disabled.

Fig. 6.41 shows phase current waveforms 1.8 s after the simulation starts when the

arm balancing controller is disabled. Some distortion is noticeable, which was not the case in the phase currents from Figs. 6.10, 6.12 and 6.14. The THD of the currents is also increased, and it is the highest in phase C, approximately 0.96 %.

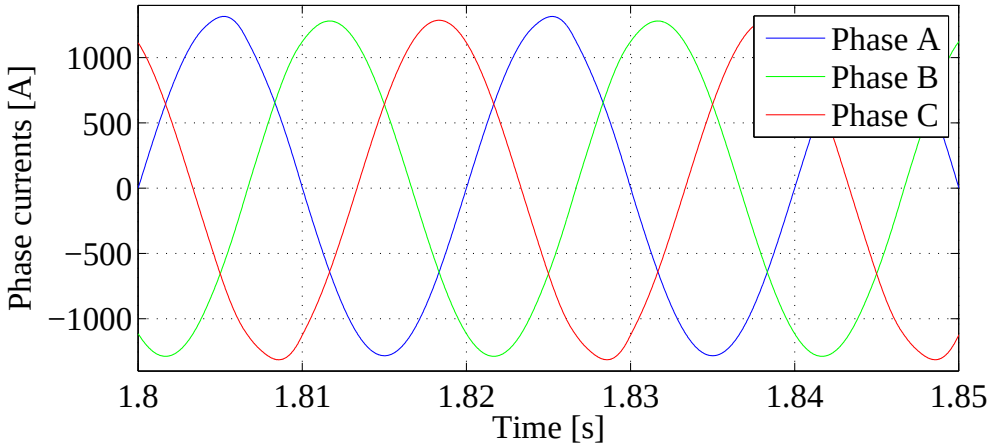


Figure 6.41: Phase/grid currents when the arm balancing controller is disabled.

The spectrum of the phase currents for the converter under the pulsed DC load without arm balancing controller is presented in Fig. 6.42. The low frequency harmonic components are present in the similar amounts in all three phases regardless of the fact that the overmodulation has not occurred in the phase B. When compared to Figs. 6.11, 6.13 and 6.15 the amplitude of the low frequency components starting at 100 Hz was increased approximately 50 times.

The converter AC power and its reference in the case when overmodulation is present in phases A and C is shown in Fig. 6.43. Two notches corresponding to the overmodulation of the two phases are clearly present in the AC power. The AC power fluctuation in this case is about 3.6 % which is beyond the specification.

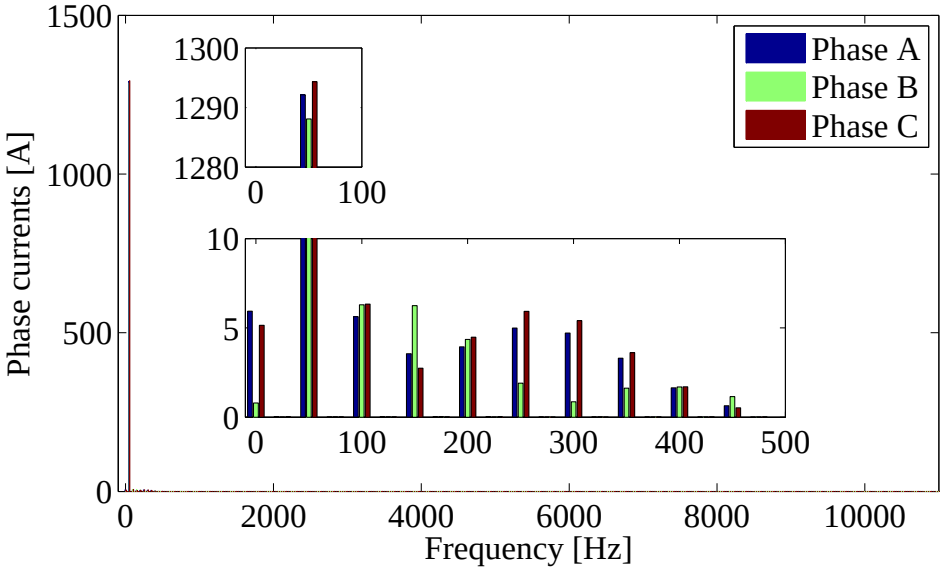


Figure 6.42: Phase/grid currents spectrum when the arm balancing controller is disabled.

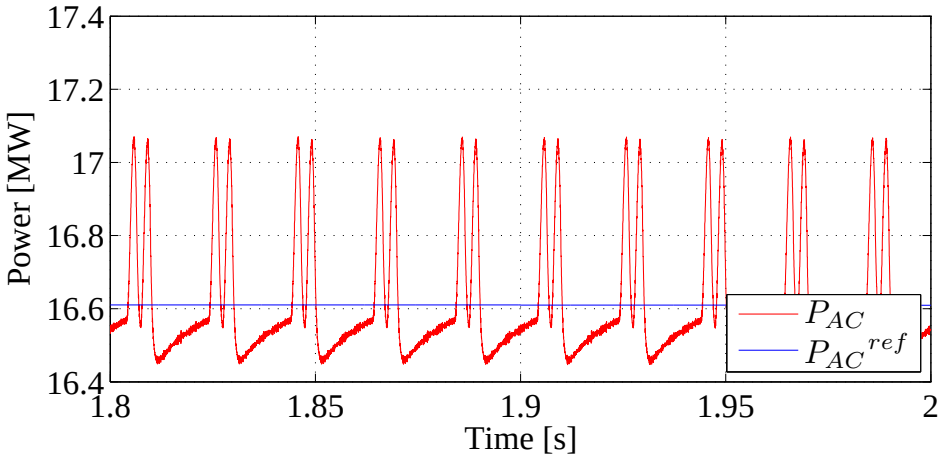


Figure 6.43: Converter AC power and its reference when arm balancing controller is disabled.

The AC power harmonics when the overmodulation is present in two converter phases are presented in Fig. 6.44. The low harmonics spectrum starting at 50 Hz is presented for the amplitudes of 200 kW which is significantly higher than in the case when there

is no overmodulation and arm balancing method one is applied (Fig. 6.9).

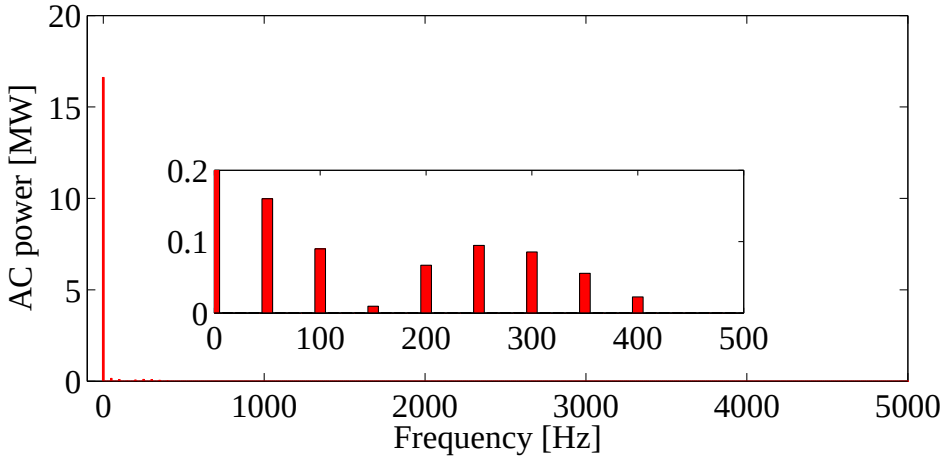


Figure 6.44: Converter AC power harmonic spectrum when arm balancing controller is disabled.

The imbalance of the converter arms happens due to the 50 Hz component in the DC voltage ripple. If the pulsed load has the same pulse length but a repetition rate of 100 Hz the DC voltage ripple does not have 50 Hz component. In that case there is not any source of imbalance between the converter arms. Therefore, overmodulation is not present and the AC power fluctuation is low. In that case the pulse happens twice in the grid period, affecting both arms equally (they have the same insertion indices at the two pulse instances). However, the arm power oscillation will be different in different phases, leading to different amplitudes of the cell capacitor voltages. In the case of a pulse repetition rate of 300 Hz all converter phases and arms would be affected equally.

Fig. 6.45 presents the sum of cell capacitors of converter arms when both phase and arm balancing controllers are disabled, with the pulsed DC load having a repetition rate of 100 Hz. The pulse occurs twice in the fundamental period, 1.7 ms after phase A grid voltage zero crossing.

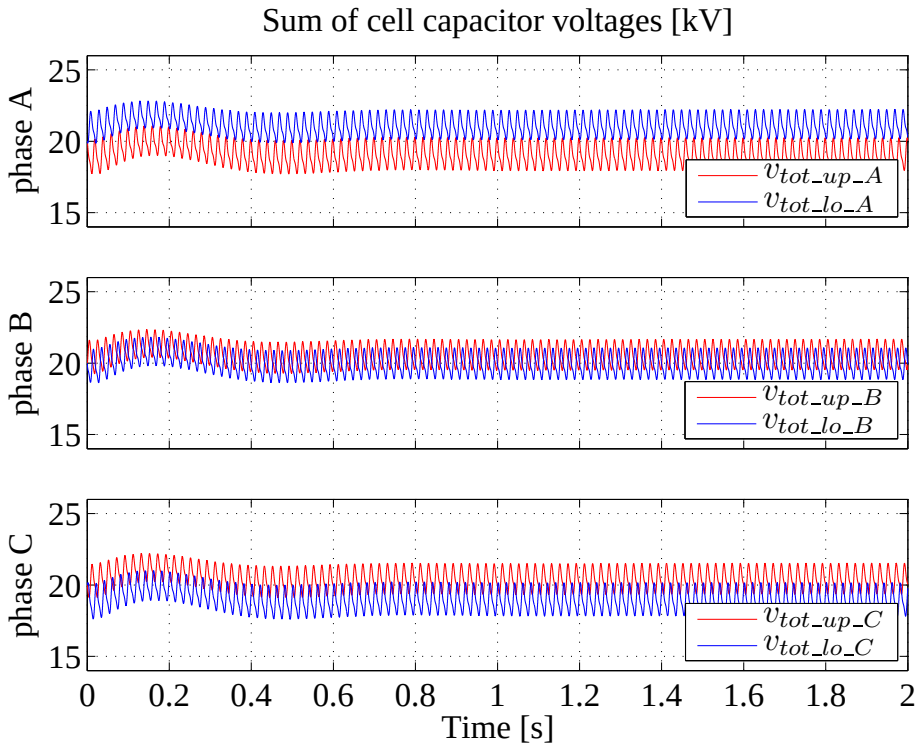


Figure 6.45: The sum of cell capacitor voltages of converter arms when arm balancing controller is disabled.

As presented, there is an initial imbalance of the converter arms caused by transient, and pulse happening under not identical conditions for upper and lower arms during transient. However, once the nominal power is reached, the pulse always affects both arms in the same way, and further divergence is stopped, i.e. average arm powers are zero. The observed converter AC power fluctuation is about 0.18 %.

6.4.4 General converter waveforms

In order to fully present the converter operation, additional internal and external converter waveforms are presented. Those waveforms are not relevant for the pulsed load, but are necessary for validating converter operation.

Fig. 6.46 presents cell capacitor voltages of all 20 cells in upper and lower arm of the phase A under steady state conditions when arm balancing method one is applied. Since the sorting frequency is 500 Hz, imperfect balancing of the cells at every switching instant is present. However, the mean values of the cell capacitor voltages are equal.

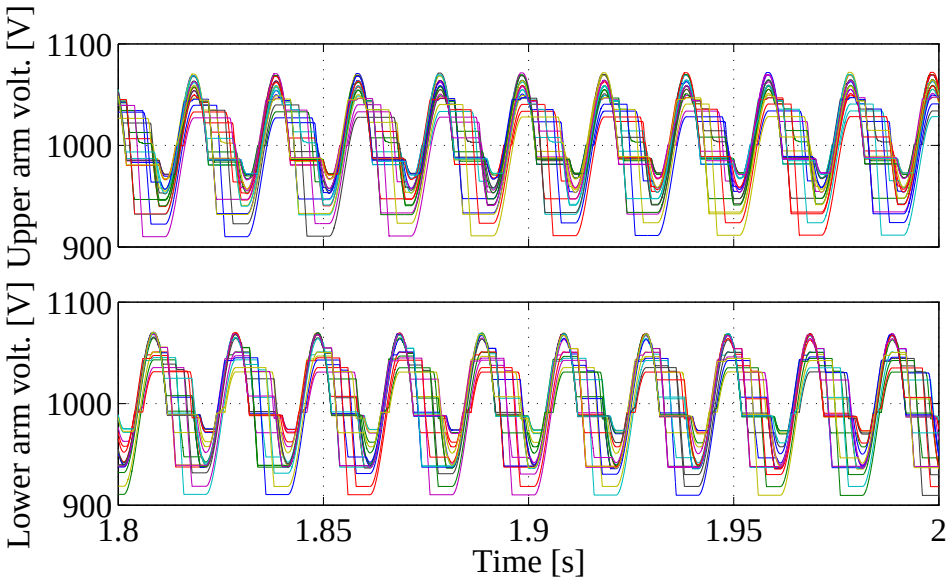


Figure 6.46: Phase A cell capacitor voltages under steady state conditions.

The phase A arm currents and circulating current are presented in Fig. 6.47. The presented case relate to steady state conditions when arm balancing method one is applied, for the pulse position of 0.534 rad. As shown, the arm currents do not have equal 50 Hz components due to the presence of 50 Hz component in the circulating current.

Converter phase voltages, with respect to the AC source neutral, under steady state conditions with pulsed DC load are presented in Fig. 6.48. Due to large number of cells per arm and $(2 \cdot N + 1)$ modulation, the converter AC voltage looks like a pure sine wave, without visible staircase structure.

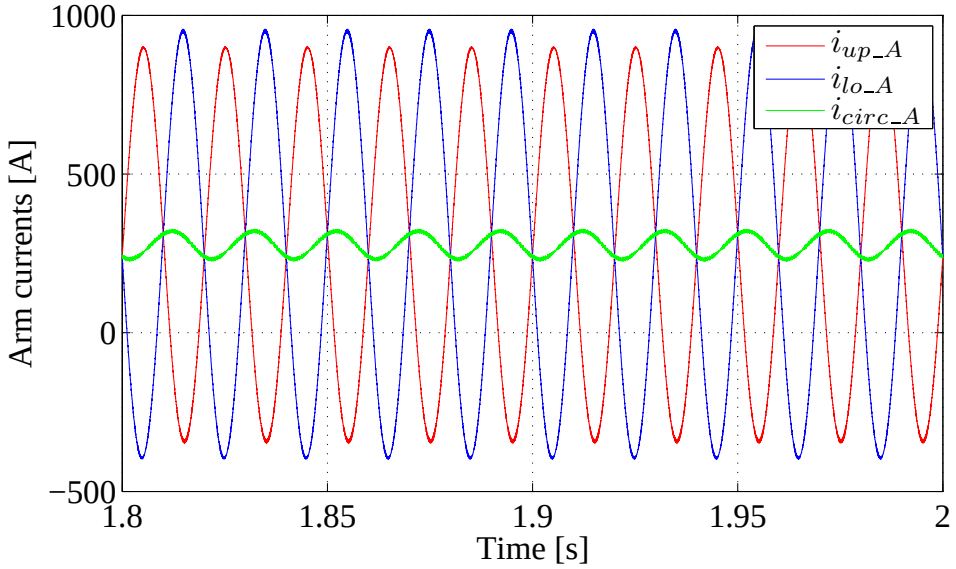


Figure 6.47: Phase A arm currents and circulating current under steady state conditions when arm balancing method one is applied.

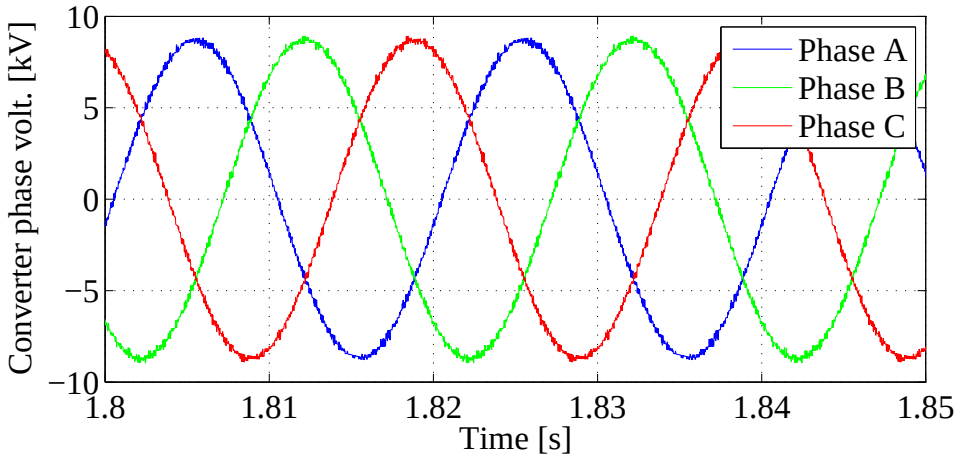


Figure 6.48: Phase voltages under steady state conditions, when arm balancing method one is applied.

The spectrum from Fig. 6.49 corresponds to the converter phase voltages from Fig. 6.48. Low frequency harmonics are present and the most dominant is at 350 Hz and 400 Hz with the amplitude below 0.2 % of the fundamental.

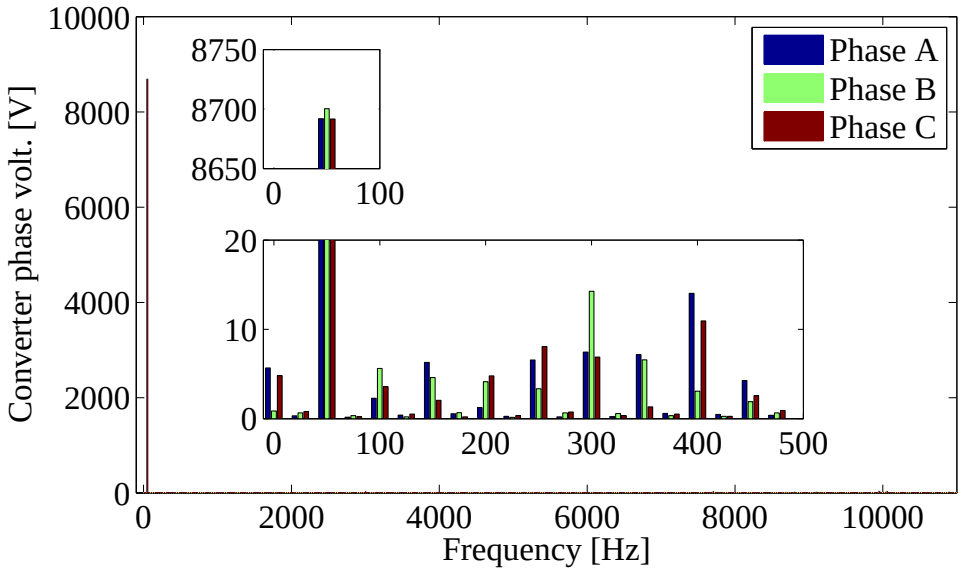


Figure 6.49: Phase voltages spectrum under steady state conditions, when arm balancing method one is applied.

6.5 Performance of the control system for different pulse positions

This sections presents the performance of arm balancing controllers for different pulse positions, covering one third of the fundamental period. The pulse positions are observed with respect to the rising slope zero crossing of the phase A grid voltage. The observed pulse positions are placed between phase A and phase B grid voltage zero-crossings, therefore symmetrical behaviour of the converter and controller waveforms is expected in the other two thirds of the fundamental period (since converter phases are symmetrical).

6.5.1 Arm balancing method one

Fig. 6.50 shows the amplitudes of circulating currents 50 Hz component vs. the pulse position in the case of arm balancing method one. The amplitude here can be negative if the same phase angle is assumed for all the phases. An alternative would be having a phase angle shifted by π rad and positive amplitude. For the two out of 21 observed pulse positions in the presented region $(0, \frac{2\pi}{3})$ rad, 50 Hz amplitudes of the circulating current were not converging to constant values. Those two points belong to so-called critical regions in which one of the denominators (section 5.6, Fig. 5.14) is crossing zero. The critical region for phase A is around 0.1 rad, while for the phase C is in the middle of the observed region, i.e. around $\frac{\pi}{3}$ rad. The critical region for the phase B is just after $\frac{2\pi}{3}$ rad, so it is not covered in Fig. 6.50.

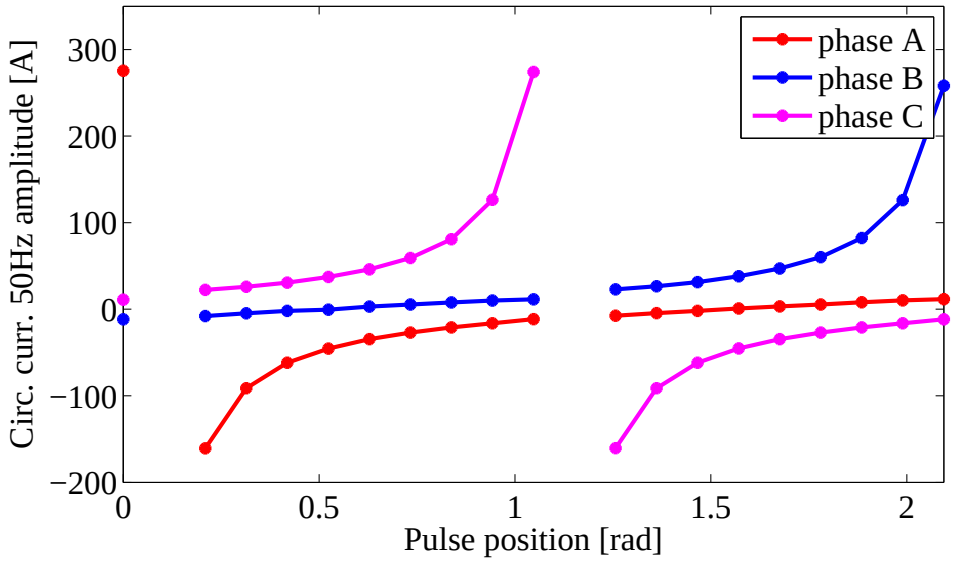


Figure 6.50: Amplitude of the circulating current reference (assuming the phase angle lagging $\frac{\pi}{2}$ rad behind DC voltage ripple) vs. the pulse position.

The obtained AC and DC power fluctuation vs. pulse position when arm balancing method one is applied are presented in Fig. 6.51. The AC power fluctuation is approximately 0.2 % for all non-critical pulse positions, while the DC power fluctuation

is significantly affected by the pulse positions. With the pulse positions approaching the critical ones, the amount of 50 Hz component in the most affected phase circulating current reference increases, causing an increase of the 50 Hz component in the DC current ripple.

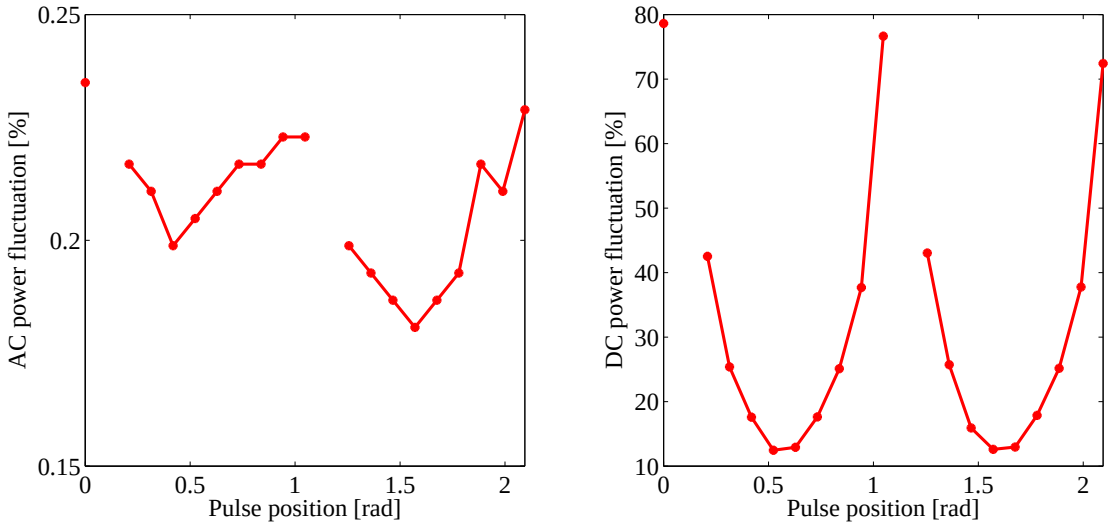


Figure 6.51: AC and DC power fluctuation vs. the pulse position when the arm balancing method one is used.

The amplitude of the DC current vs the angle of the DC voltage ripple 50 Hz component is presented in Fig. 6.52. This figure shows a perfect match with the analytical model in Appendix B and Fig. 5.16 (Chapter 5). As the pulse position moves from 0 rad to $\frac{2\cdot\pi}{3}$ rad region, the DC voltage ripple angle moves from π rad to $\frac{\pi}{3}$ rad.

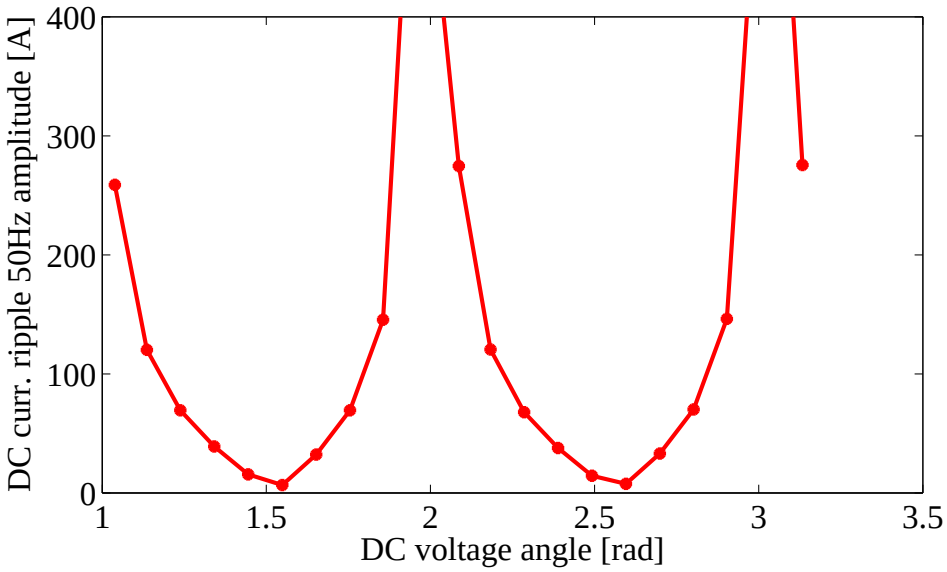


Figure 6.52: The DC current ripple 50 Hz component ripple amplitude vs. the DC voltage ripple 50 Hz component angle when the arm balancing method one is applied.

6.5.2 Arm balancing method two

Arm balancing method two uses the circulating current 50 Hz component aligned (or in counter phase depending on the pulse position) with the AC voltage reference.

Fig. 6.53 shows the amplitudes of circulating currents 50 Hz component vs. the pulse position. The amplitude here can be negative if the phase angle is assumed to be the same as the angle of that phase AC reference.

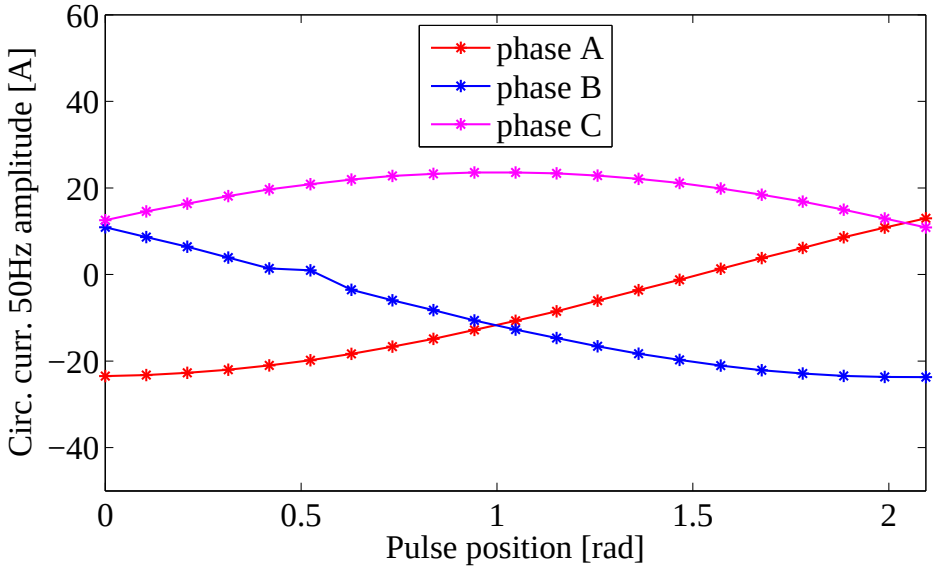


Figure 6.53: Amplitude of the circulating current reference (assuming the phase angle being the same as the AC voltage reference) vs. the pulse position.

The obtained AC and DC power fluctuation vs. pulse position when method two is applied are presented in Fig. 6.54. The AC power fluctuation is approximately 0.2 %, while the DC power fluctuation is about 18 %. The nearly constant DC power ripple indicates similar amplitudes of the 50 Hz component in the DC current despite the pulse position.

6.5.3 Arm balancing method three

The values of $x_{A,B,C}$ parameter obtained for different pulse positions are presented in Fig. 6.55. The values of the parameter x are always below 2 % for the voltage droop of 10 %.

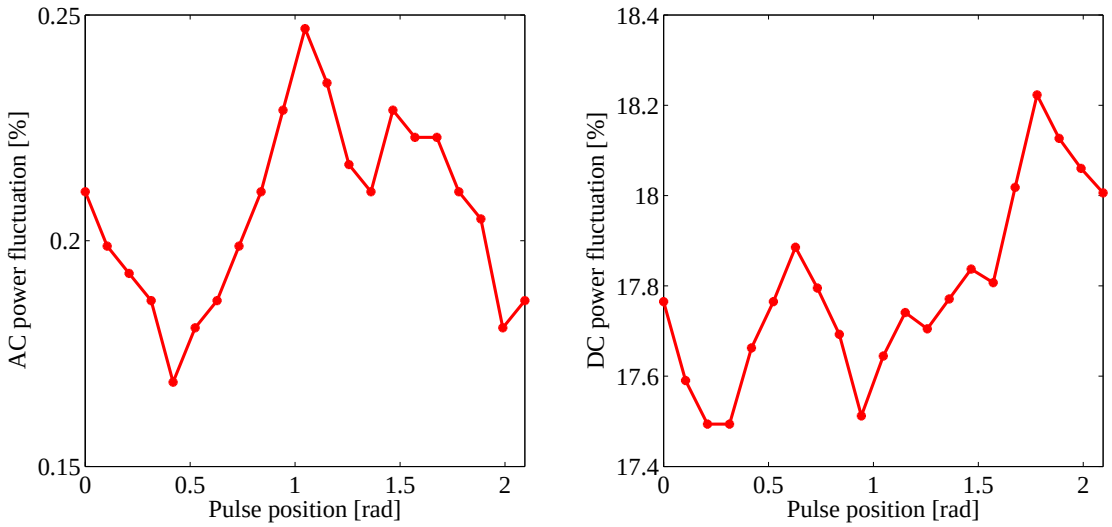


Figure 6.54: AC and DC power fluctuation vs. the pulse position when the arm balancing method two is used.

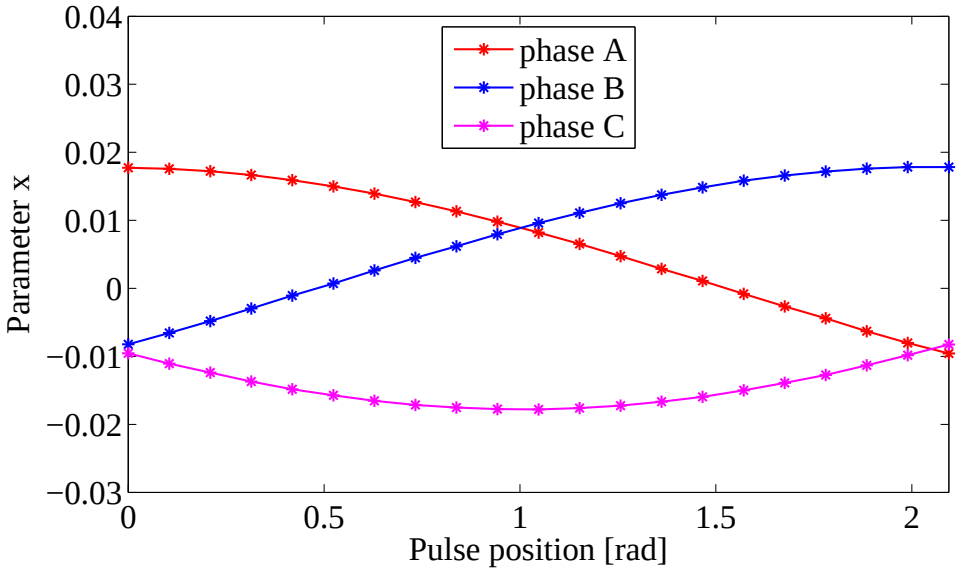


Figure 6.55: Parmeter $x_{A,B,C}$ vs. the pulse position.

The obtained AC and DC power fluctuation vs. pulse position when method three is applied are presented in Fig. 6.56. The AC power fluctuation is approximately 0.2 %,

while the DC power fluctuation is about 18 %.

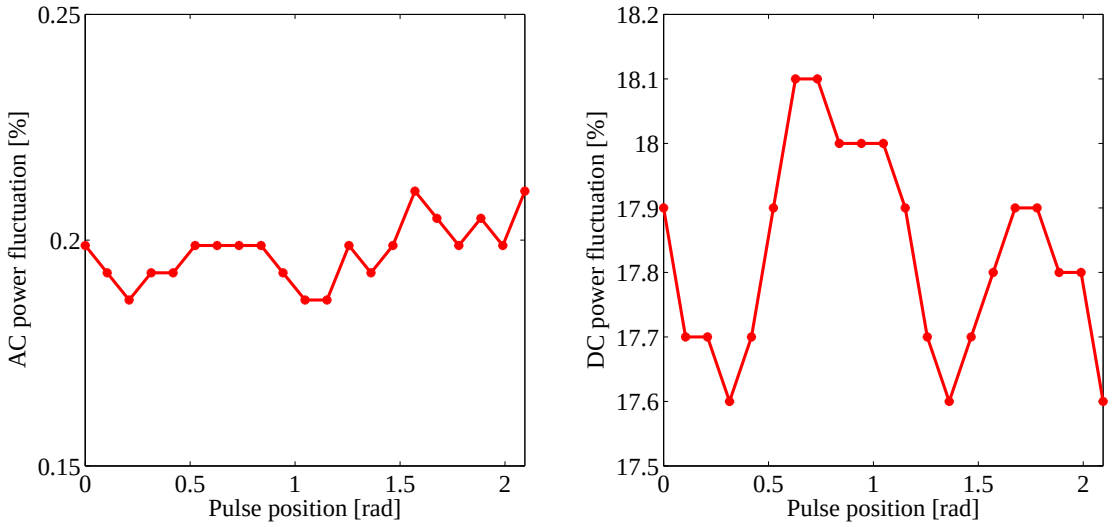


Figure 6.56: AC and DC power fluctuation vs. the pulse position when the arm balancing method three is used.

The method three has the similar performance to the method two, giving approximately the same AC and DC power ripple, for all pulse positions.

6.6 Summary

Based on the simulation model of an MMC under pulsed DC load emulating klystron modulators, a feasibility of achieving low AC power fluctuation is confirmed. All the presented control loops from Chapter 5 are validated on a 20 cell par arm converter model, which despite the pulsed nature of the DC load provided high quality AC currents.

Three arm balancing methods are verified for the fixed pulse position of 0.534 rad and the similar quality of the AC power is achieved for all of them. However, the

arm balancing method one is sensitive to the pulse positions, meaning that in some critical positions arm balancing can not be achieved, and the AC power is beyond the specifications. If the pulse is synchronised to the grid, the arm balancing method one can be utilised and the pulse position can be chosen to guarantee constant DC current (no 50 Hz component in the DC current). The arm balancing methods two and three, are suitable for all pulse positions, therefore they can be applied even if the pulse is synchronised to some other 50 Hz periodical source rather than grid. However, a certain amount of the DC current 50 Hz ripple is always present when arm balancing methods two and three are used.

The main reason for the imbalances present among converter arms is the load repetition rate equal to the grid frequency. The use of different load frequency, such as 100 Hz or 300 Hz, would mean no imbalance between converter arms. In that case there is no need for the arm balancing and phase balancing controllers, assuming fully symmetrical converter cells and arms.

Chapter 7

Experimental rig

7.1 Introduction

This chapter presents the design of the small scale grid connected MMC under pulsed DC load. The experimental prototype has been constructed in order to validate the behaviour of the converter and the control techniques developed in this thesis. The chapter discusses the structure of the converter, precharge circuit and the load emulation circuit. The pulsed load is emulated with a resonant L-C converter, which will be described in following section.

The third section focuses on the control platform, comprising a DSP board and 4 FPGA cards, used to control the experimental converter. Converter measurements are obtained by data acquisition boards that are connected to the A/D channels of the FPGA boards. The following section presents the control software which allows the safe converter operation through the different modes, such as precharge, grid synchronisation, pulsed load, etc.

7.2 Prototype design

This section focuses on a prototype design that is suitable for validating the theoretical and simulation results previously obtained for the modular multilevel converter used as a grid interface for klystron modulators. The simulation results were based on an MMC with 20 cells per arm, a 20 kV DC bus voltage and a rated power of 16 MW, since these ratings were selected as optimal in the power system optimisation process. Due to the laboratory limitations, a scaled converter prototype has been designed. A 4 cell per arm, 400 V DC bus voltage, 7 kW modular multilevel converter is proposed for validation. Although these ratings are not suitable for supplying klystron modulators, they are considered appropriate to validate the converter behaviour under the pulsed load, with a 50 Hz repetition rate. Furthermore, the presented control methodologies can be validated on the smaller scale prototype.

In addition to the converter design, the prototype includes the load and precharge circuit design. The load circuit should emulate the behavior of a klystron modulator rated at the converter DC voltage and power. The load is scaled down with the same scaling factor as the converter, while maintaining the pulse length and repetition rate. The load is realised through a resonant L-C circuit, providing sinusoidal pulsed current as will be described below. The precharge from the DC side has been already discussed in the Chapter 5, but its hardware and operation will be discussed below, as well.

The prototype hardware is given in Fig. 7.1. The 4 cell per arm MMC, together with the precharge circuit, contactors and the resonant load, is presented.

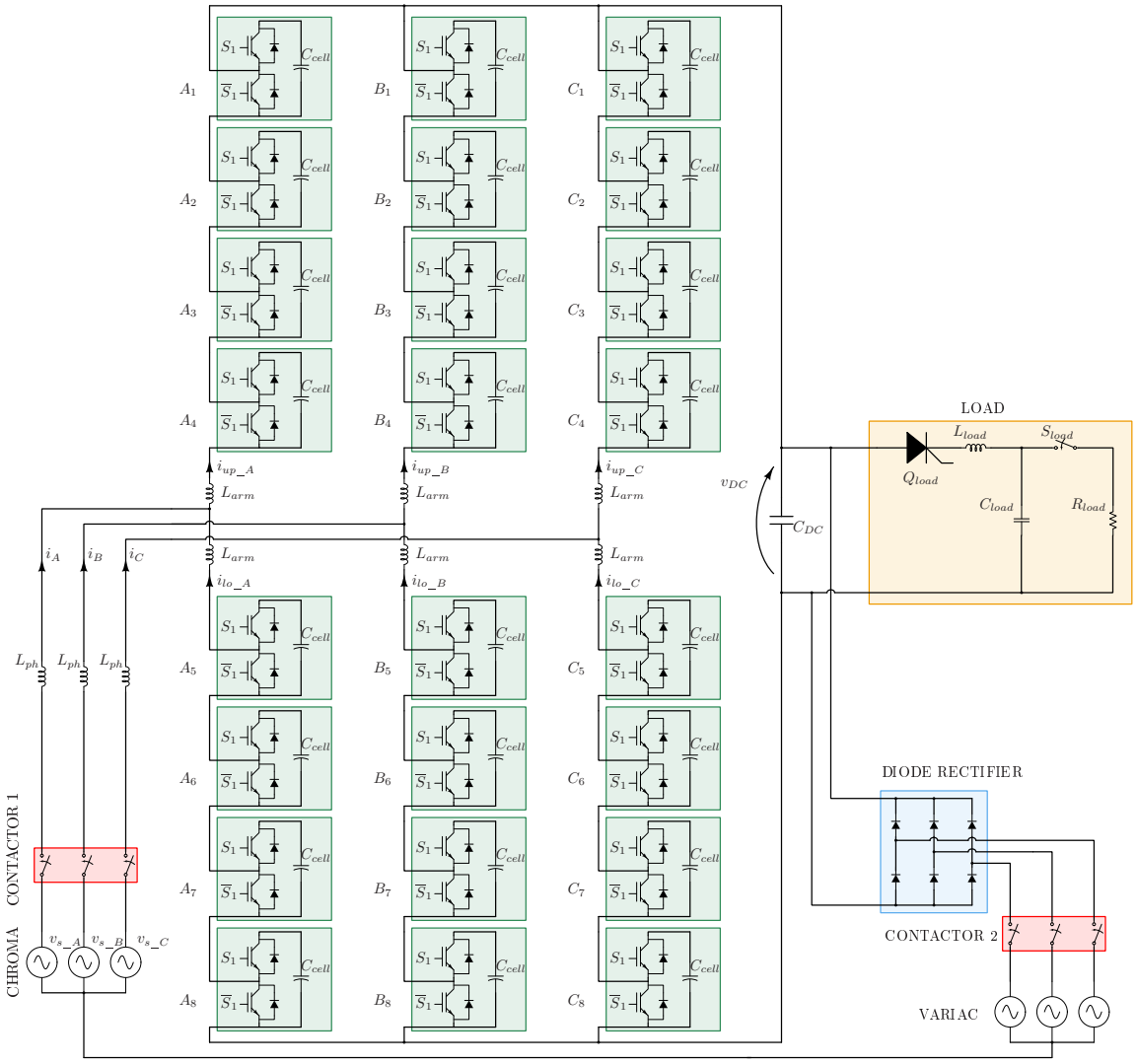
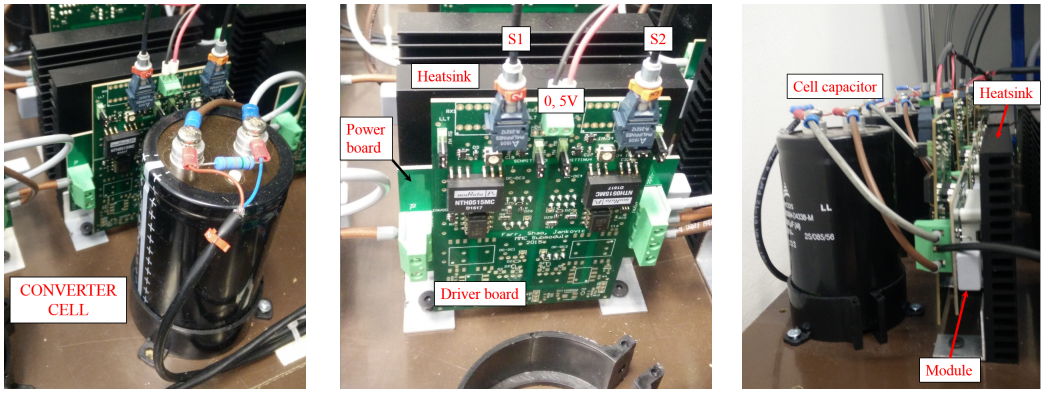


Figure 7.1: Schematics of the experimental prototype.

7.2.1 Converter design

The 4 cell per arm converter, with a DC bus voltage of 400 V would require half-bridge cells with a nominal DC voltage of 100 V. However, the cell design has been inherited from the previous research efforts in multilevel converters within the research group, and therefore is overrated for this application. The cell is designed as a full-

bridge converter (H-bridge) using an Infineon 600 V, 50 A full-bridge module (F4-50R06W1E3). The photographs of the converter cell are presented in the Fig. 7.2. A gate driver board is directly connected to a power board containing the IGBT module. For the purpose of this project only two gate drivers are populated, and only one module leg is used in order to make a half bridge cell. However, both driver board and the power board can be fully populated for the full-bridge operation. This, together with the overrated cell voltage and current allows converter use for future research projects.



(a) Front view, whole cell (b) Front view, PCBs (c) Side view

Figure 7.2: One half-bridge converter cell.

The gate drive control signal is carried via the fibre optics cable, where the light means logic '1' and it is recived by fibre optic reciever, that inverts the logical zero, i.e. in the case of light the receiver output is '0'. Since the light in the fibre cable should turn on the switch, the signal from the fibre receiver should be inverted to polarise the gate. The gate driver circuit is presented in Fig. 7.3. A delay of the rising edge of PWM signal is provided by R-C circuit, and the resulting signal is additionally shaped by a Schmitt trigger inverter, in order to increase the dead-time between upper and lower switch gating signals. The gating signal is isolated from the 5 V power supply through an optocoupler, while an additional isolated DC-DC converter is used to provide the gating voltage levels for every switch. The IGBT is driven with ± 15 V (while the emitter is at 0 V), meaning that the logic 'one' corresponds to the voltage of 15 V and the logic 'zero' corresponds to -15 V.

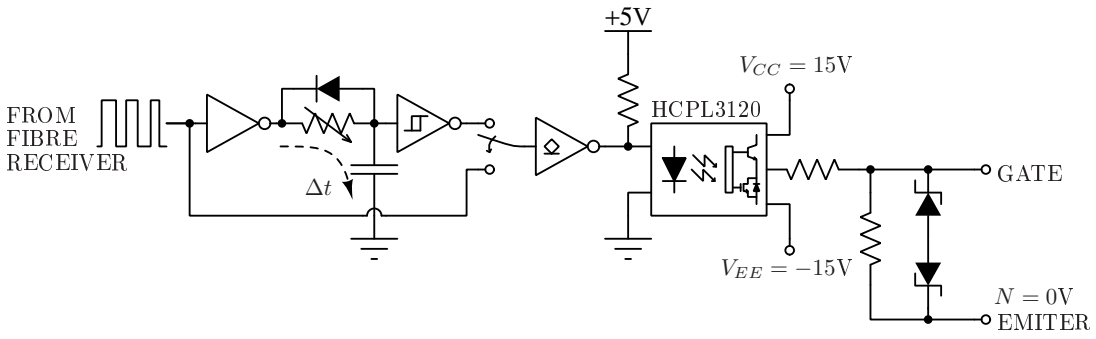
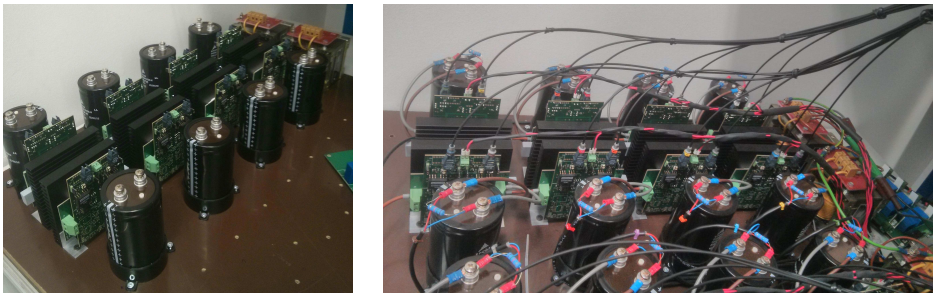


Figure 7.3: Gate drive schematics used for gating the cell switches.

Cell capacitance is selected according to the available E12 series and the capacitance constant previously considered in section 4.5 by equation (4.38). For the experimental converter (rated power 7 kW, 4 cells per arm and DC voltage of 400 V), the cell capacitance of 3.3 mF corresponds to the capacitance constant of 56.57 ms. The chosen capacitor voltage rating is 350 V which is significantly larger than the rated 100 V, to provide headroom for using the converter at higher voltage ratings. The discharge resistor is selected as a compromise of high resistance (to be neglected in the converter models) and relatively low time constant (to minimise the discharge time, i.e. the time between two subsequent converter runs). The selected resistance of 15 kΩ corresponds to the time constant of approximately 50 s.

The arm inductance value is selected from the E12 series, to avoid the resonance with the equivalent arm capacitance as given by (4.39) in section 4.5. The second harmonic resonance occurs at 1.18 mH, thus the selected inductance is 1.5 mH (approximately 30 % higher). The rated current of the inductor is 21 A which is close to rated arm currents.

Converter phase A is presented in the photographs of Fig. 7.4. At the side, next to phase A, is phase B, followed by phase C. The whole three-phase MMC is presented in Fig. 7.5.



(a) Unconnected (b) Connected

Figure 7.4: Photographs of the one converter phase.

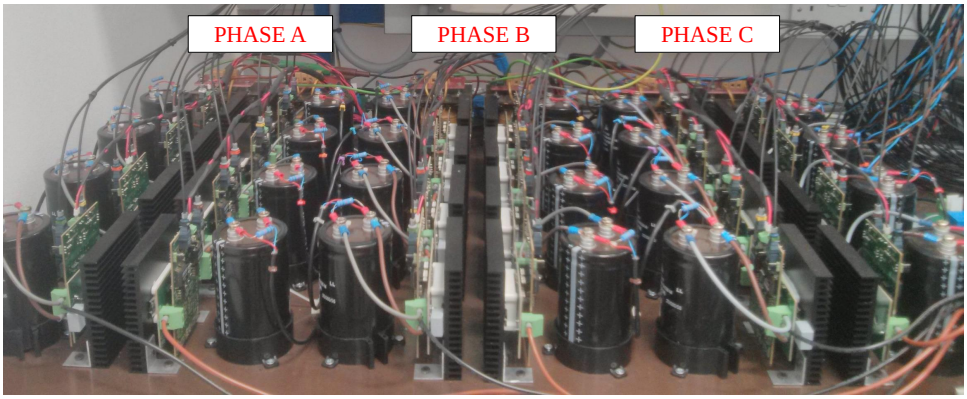


Figure 7.5: Photograph of the three-phase MMC.

The DC link capacitors are located in proximity to the load, and they are used to limit the DC voltage droop. The size of the DC link capacitor is defined by the rated load power and the size of the voltage droop, as given by (3.7) where $\Delta V = 0.1 \cdot V_{DC}$ corresponds to 10 % voltage droop. The selected capacitance for the rated power (6.6 kW) is 8.5 mF. The capacitance is realised with the parallel connection of three capacitors, one of 1.5 mF and two 3.5 mF. Both capacitors are rated at 1 kV which is significantly higher than the nominal DC link voltage. Similarly to the selection of discharge resistors for the cell capacitors, discharge resistors for the DC link capacitors are selected to provide the discharge time constant in the range of minutes. Three 18 kΩ resistors are used, each in parallel with one capacitor, and the obtained time constant is 51 s.

The grid connection is realised through the three-phase inductor with the inductance of 3 mH, which is approximately twice the arm inductance. The rated current should be higher than the rated AC currents which is 18 A RMS in the case of full converter power (∼26 A peak current). The grid is emulated with a Chroma programmable AC power source 61511. The AC voltages have a peak RMS value of 130 V phase to neutral (184 V peak).

7.2.2 Pulsed load design

The load circuit that emulates the klystron modulators behaviour for the purpose of experimental verification is presented in Fig. 7.6. The thyristor gate is triggered with a short pulse to initiate the current pulse, with the repetition rate, f_{rep}. When the thyristor is conducting, a portion of energy from the DC link capacitor is transferred to the load capacitor through the load inductor, which forms a resonant circuit. The current shape is a half sinusoid, since the thyristor turns off when the current falls to zero. The average current and the pulse duration can be designed by selecting appropriate circuit elements in order to emulate a klystron modulator (scaled power and DC voltage). The circuit behaviour is dominantly defined by the values of C_{load} and L_{load}, but it is also affected by the damping factor λ, the DC link capacitance and the thyristor Q_{load} reverse recovery (energy Q_{rr}).

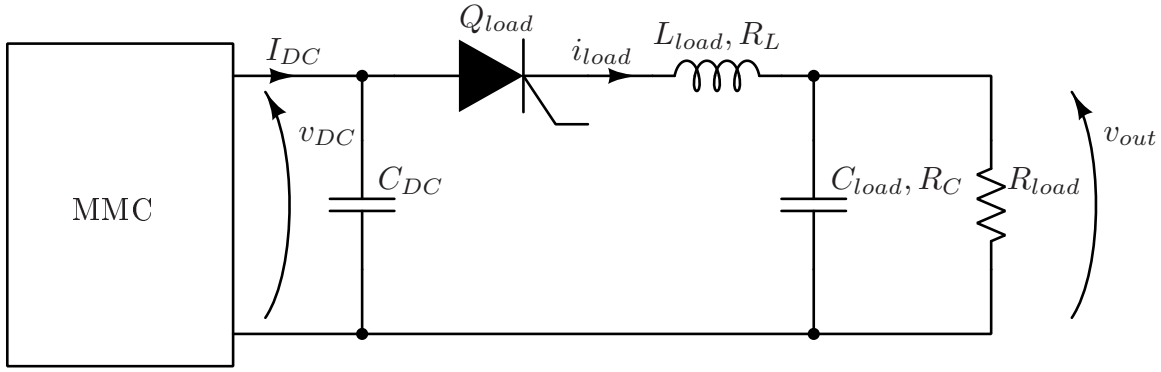


Figure 7.6: Resonant pulsed load design.

Since the DC current and the current through the discharge resistor R_{load} are significantly lower than the pulsed current (during pulse) they are not considered in following analysis. Also the Q_{rr}, reverse recovery energy of the thyristor, hasn't been considered in the analysis. The damping factor is proportional to the series resistance present in the load inductance and the load capacitance as given by:

$$\lambda = \frac{R_L + R_C}{2 \cdot L_{load}} \tag{7.1}$$

Having assumed a certain amount of λ and knowing that the DC power is P_{DC}, the load capacitance can be computed as:

$$C_{load} = \frac{1}{(1 + e^{-T_{pulse} \cdot \lambda}) \frac{{V_{DC}}^2}{T_{rep} \cdot P_{DC}} - \frac{1}{C_{DC}}} \tag{7.2}$$

where T_{pulse} is pulse duration, which is $140\,\mu$s. For given pulse duration, damping factor and selected capacitance, the load inductance is computed as:

$$L_{load} = \frac{\frac{1}{C_{DC}} + \frac{1}{C_{load}}}{(\frac{\pi}{T_{pulse}})^2 + \lambda^2} \tag{7.3}$$

Since the value of the damping factor is not a priori known, but it is also dependant on the value of load inductance and series resistances, the equations (7.2) and (7.3) can not be computed analytically. If zero damping factor is assumed, these equations are simplified and they can be analytically computed. For the power ratings of 6.6 kW, the calculated values for C_{load} and L_{load} are $433\,\mu$F and $4.8\,\mu$H, respectively.

The peak current of the resonant load is computed by:

$$I_{peak} = \frac{V_{DC} \cdot T_{pulse}}{\pi \cdot L_{load}} \tag{7.4}$$

For given parameter values, the peak current is 3.714 kA. This peak value correspond to the average current of 16.5 A and the RMS current of 218 A.

Practically, the exact values of inductance and capacitance computed above cannot be obtained. The actual parameters of the resonant load elements are given in Table 7.1. The arm inductance is air-cored since any core material would saturate at the high peak currents considered. The arm inductors are designed on the brooks-coil

Table 7.1: Load parameters measured at 1 kHz.

Rated power	L_{load}	R_L	C_{load}	R_C	R_{load}
6.6 kW	5.26 μH	3.64 mΩ	435.5 μF	8.8 mΩ	10 Ω

principle [81], with the conductor rated on the basis of the RMS load current. The achieved inductor parameters are given in the Table 7.1.

The load capacitor also needs to withstand the RMS current and the pulse current, therefore the parallel connection of film capacitors is done. The capacitance of 440 μF is realised with four 50 μF capacitors and twelve 20 μF capacitors. To ensure even current distribution among parallel capacitors, they are distributed in a circle connected to two parallel copper plates. The capacitor parameters are also provided in Table 7.1.

The load resistance is selected to discharge the load capacitor before the next pulse. Thus, the time constant should be at least 5 times smaller than the pulse period. The selected resistance is provided in Table 7.1. Also the rated power of the load resistance should be higher than the rated DC power P_{DC} since all power transmitted to the load gets dissipated on the load resistor.

The measured value of series resistance (excluding connections) is about 12.4 mΩ which gives the λ value of 1182.5 s^{-1}. This λ value does not have a significant effect to the equations (7.2) and (7.3), and the assumption of a small λ value is therefore justified.

The pulsed load prototype rated at the power of 6.6 kW when the DC voltage is 400 V is shown in Fig. 7.7. The figure shows the DC bus capacitors, positioned in proximity to the load, thyristor with the heatsink, air-cored load inductor, and the load capacitors realised with 16 capacitors in parallel.

The thyristor should be capable of conducting the peak load current, and also satisfy maximum $\frac{di}{dt}$. The selected component is a Dynex DCR960G26 which is supplied

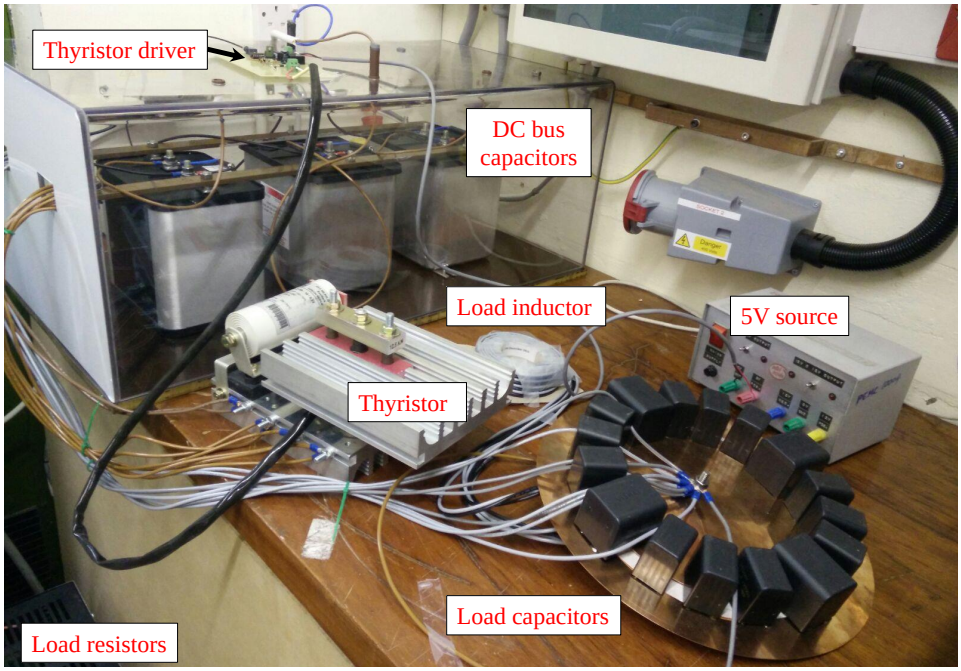


Figure 7.7: Pulsed load experimental prototype.

with a parallel snubber circuit (0.22 μF, 111 Ω). The thyristor gate driver is designed with respect to the gate V_{GT} - I_{GT} characteristics provided in the datasheet. Based on those curves the gating voltage and the output resistance of the gate driver are selected. In this particular case the gating voltage is 24 V, while the output resistance R_{out} is 10 Ω. The driving circuit is presented in Fig 7.8.

The thyristor driver requires an additional isloated DC-DC converter providing a 24 V (V_{CC2}) for driving the thyristor gate. Also, in order to provide enough drive current, a circuit with a MOSFET is used, as presented in Fig 7.8. The selected MOSFET requires driving voltage up to 10 V meaning that it can not be driven with the already available 24 V. Thus, another isolated DC-DC converter (providing V_{CC1}) is used for driving the MOSFET, with the source potential ($N = 0$) being isolated from the digital logic and fibre receiver with the optocoupler.

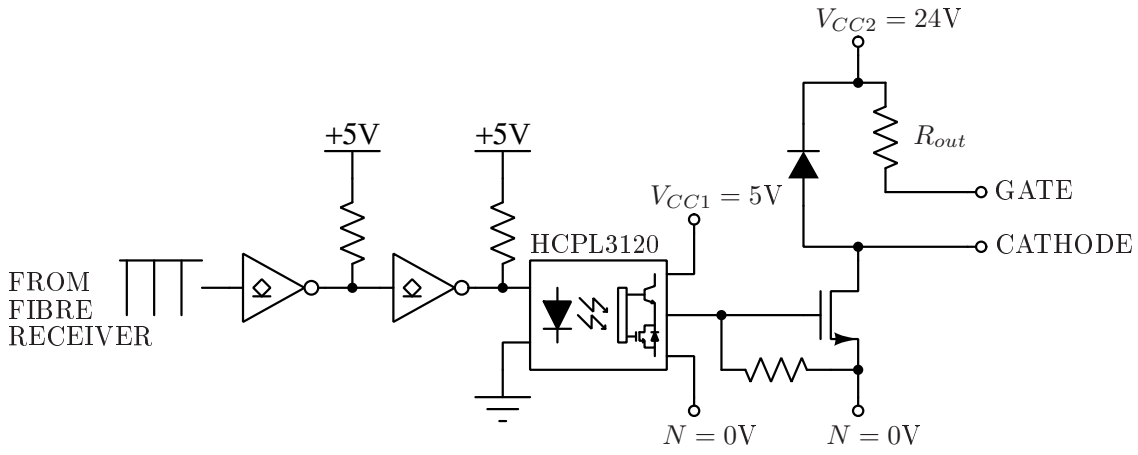


Figure 7.8: Thyristor gate drive schematics.

7.2.3 Precharge circuit

The precharge circuit has been already discussed in Chapter 5 (Fig. 5.23), which covered the control aspects of the precharge regime. The precharge circuit includes an additional variable AC source, a three phase diode bridge rectifier and a contactor for connecting and disconnecting this auxiliary circuit. The additional capacitors for smoothing the rectifier voltage are not needed since the converter already has a DC link capacitor.

A variable autotransformer (variac) provides a scaled voltage of the three-phase voltages available in the laboratory (240 V RMS phase voltage). In order to provide the nominal DC voltage on the DC link capacitor the variac voltage should be slowly increased from 0 V to approximately 173 V RMS phase voltages corresponding to 72 % of the actual grid voltage.

The diode bridge should be capable of blocking the total DC voltage, while the current rating should not be critical, since the slow increase of the variac voltage guaranties charging the DC link with the low currents. The selected module VS-36MT60, has rated current of 35 A and 600 V blocking voltage.

The contactor is used to connect or disconnect the precharge circuit to the converter DC bus. The contactor can be placed either on the DC connection (DC contactor) or at the variac connection (AC contactor). For the simplicity reasons the contactor is placed at the three-phase system, between the variac and the diode bridge. The selected model LC1D32-BL is driven with 24 V DC, and its rated current is 32 A. The contactor is controlled with a fibre optic signal sent from the digital control unit, which will be described in more detail in the following section. The contactor closing time is approximately 77 ms, while the opening time is 135 ms.

Since the precharge regime should not overlap with the grid connection regime, another contactor is placed on the converter grid connection, and these two contactors should not be closed at the same time. Fig. 7.9 presents the control circuit of the two contactors, C_2 which connects the precharge circuit, and C_1 which connects the converter to the grid. Both contactors and their control circuits are equivalent, with the difference that grid connection has a manual switch enable (together with the fibre optic signal).

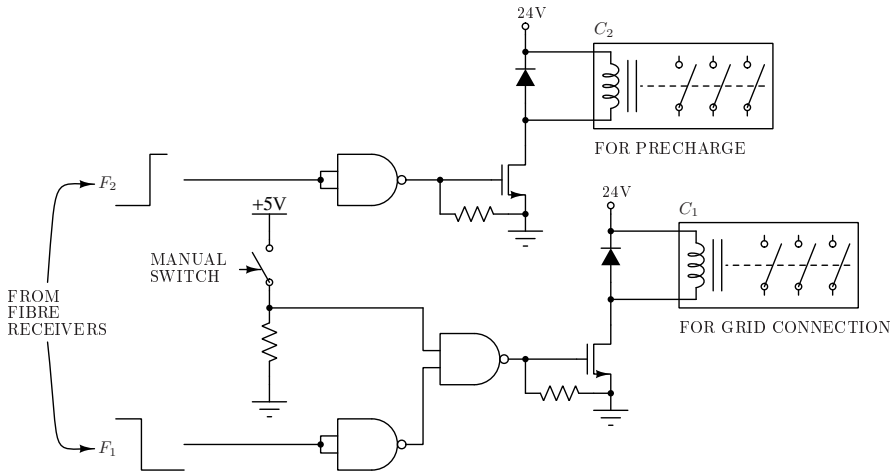


Figure 7.9: Contactor control circuit.

The contactor control circuit requires an additional 24 V DC voltage source with respect to the common control logic ground (5V power supply ground). For this

purpose an isolated DC-DC converter 5V to 24V (isolation was not required) is used. The MOSFET provides additional current capacity for magnetising the contactor coil.

7.3 Control hardware

The control hardware is used for the implementation of safe and correct operation of the experimental converter and the load. The control hardware includes the acquisition system needed for reading the converter signals, such as relevant voltages and currents, the digital control that process the readings and based on those provides the control signals, that are further transmitted to the gate drivers and contactors control circuits. The control hardware, as a part of the experimental rig, provides the ability to switch between different modes of the operation, such as precharge, inverter operation, rectifier operation, no-load condition, and the pulsed load condition. All control signals are transmitted via the fibre optic cables in order to minimise the noise and EMI effects on the system.

7.3.1 Data acquisition

The data acquisition system provides the relevant converter signals to the FPGA board, carries out the A/D conversion and transfers the data to the digital processing unit. The acquisition is done by the sensor boards equipped with the current and voltage transducers for reading specified converter voltages and currents.

For the presented converter, all cell capacitor voltages should be measured together with the arm currents in order to perform the sorting algorithms and capacitor balancing within one arm. The arm currents can also be used for calculating phase current, circulating current and the DC current which are needed for current control loops. Therefore, the number of readings required per phase is ten - eight cell capacitor voltages and two currents, and it is equal to number of A/D channels available

on one FPGA board. For this purpose, a PCB is designed to collect the one phase internal readings. Each of those PCBs is attached to one FPGA board, implying the need for three FPGA boards for the three-phase converter.

Further measurements include the grid AC voltage, converter DC voltage, AC currents and the DC current; needed for the purpose of grid synchronisation, power control, and output control. Another PCB is designed for the purpose of monitoring those external signals, and it is presented in Fig 7.10. As already mentioned the phase currents and the DC current can be calculated, based on the arm currents. However, the fourth FPGA card needs to be used for the data acquisition of the external signals, so the current transducers are included as well.

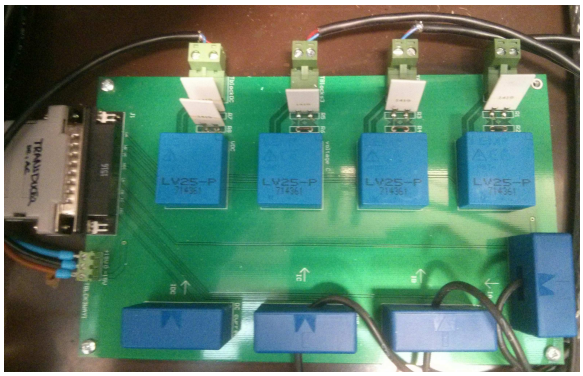


Figure 7.10: An example of the data acquisition PCB.

7.3.1.1 Voltage and current transducers

Both current and voltage transducers are produced by LEM and are equipped with a Hall effect closed-loop current sensor. These sensors measure the input current and provide the output current proportional to the input current whilst providing galvanic isolation. Both current and voltage transducers require an additional $\pm 15\,\mathrm{V}$ voltage source, with respect to the control system $0\,\mathrm{V}$ potential.

Voltage sensor LV 25-P is used, and its application is presented in Fig. 7.11. As previously mentioned, the transducer still measures the current, so a resistor R_{in} is

needed to transfer the measured voltage into a current. The selecton of input resistor depends on the nominal voltage to be measured and the datasheet information about nominal input current.

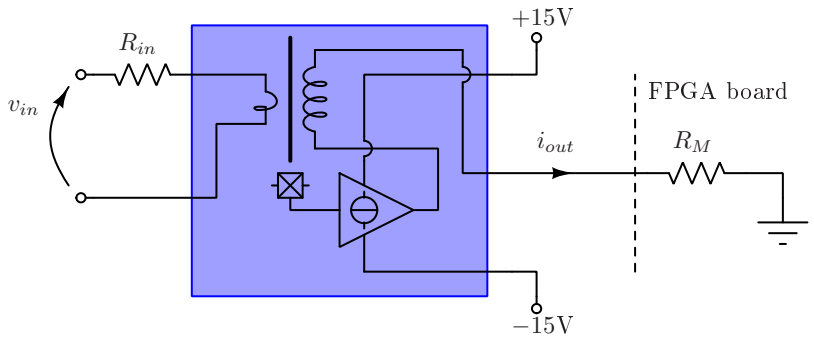


Figure 7.11: LV 25-P voltage transducer application circuit.

The selected resistor in that case is a 20 kΩ, 5 W thick film resistor, which gives a nominal measurement point at 200V. In order to transform the output sensor current to a voltage, a so-called burden resistor R_M is used. These resistors are placed on the FPGA board where their voltage is processed with operational amplifiers and forwarded to the A/D converters. The voltage on the burden resistors should be limited to ±5 V which is the supply voltage level at the FPGA board. The burden resistor in this case is 200 Ω. The same combination of input resistor and burden resistor can be used for reading the phase voltages. The DC voltage has a nominal value of 400 V, and thus input resistor used is 40 kΩ (two 20 kΩ resistors in series). The burden resistor in that case is again 200 Ω.

Current sensor LA 55-P is used, and its concept is presented in Fig. 7.12. The cable with the measured current is passed through the hole in the transducer in order to make a turn (one or more turns). The nominal current of all turns together is 50 A and the output current is in the range of ±50 mA. The burdern resistor selected is 100 Ω in order to limit the voltage on the FPGA board. All current sensors use a single turn through the transducer.

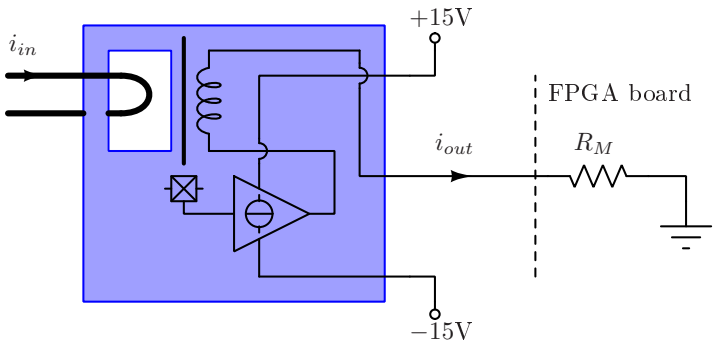


Figure 7.12: LA 55-P current transducer application circuit.

Knowing the resistor values, transducer characteristics and A/D converter characteristics, the approximate transfer function from the measured signal to the read 14 bit integer can be calculated. However, this would be inaccurate, since the resistor tolerances, transducer tolerances, and temperature effects haven't been taken into account. Therefore, the sensor should be calibrated with the precise voltage and current sources, to get the relation between readings and the measured signals. After calibration in the ranges of interest, a linear equation is derived that translates 14 bit integer into the actual voltage and current. With the increased temperature and time, the characteristic of the sensor changes, meaning that the process of calibration needs to be carried out multiple times.

7.3.2 Digital control

The digital control software consists of Actel FPGA board designed within the research group and the DSP board C6713 DSK by Texas Instruments. In this application 4 FPGA boards are stacked to the DSP board. The number of FPGA boards was selected on the basis of number of available A/D channels, even if the processing power of four FPGAs was not necessary. The DSP board is additionally equipped with a HPI daughtercard which is used for communication, downloading DSP code,

and online monitoring of the converter variables on the PC.

7.3.2.1 FPGA board and control signals generation

The FPGA board has been designed within the research group and it features the Proasic3 FPGA chip by Actel. The FPGA board is presented in Fig. 7.13.

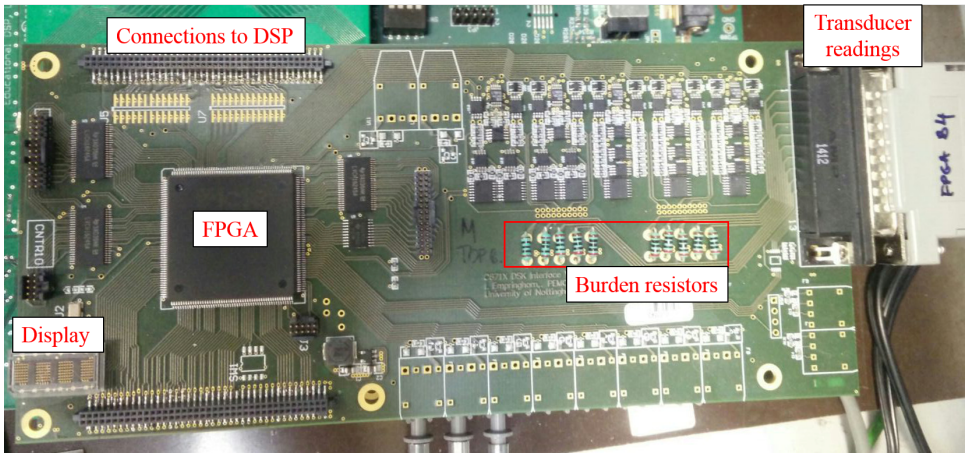


Figure 7.13: FPGA board designed within PEMC research group.

The implemented design includes 21 registers used to store the relevant settings and data, such as the interrupt period, enable bits, trip status register, A/D readings, space vectors, etc. The DSP can write to or read from those registers. In the configuration where multiple FPGA boards are used, the FPGAs, as external memories of the DSP, are using the same parallel port to communicate with the DSP. In that case, one FPGA is a master, and it is responsible for the interrupt generation, while the other boards are synchronised to this interrupt. Once the DSP receives the interrupt, the interrupt routine is executed, and this will be the topic of the control software subsection. Also, the master board receives the manual enable signal which enables the PWM and other control signals outputs.

The FPGA board has a 50 MHz clock, which is used for main operations such as

interrupt generation, A/D channels reading, and PWM generation. Additionally, there are 10 MHz and 3 MHz clocks used for less demanding and smaller priority tasks, such as display refreshing. A display is used to show the information about board operation, such as enable, disable and trip messages.

The PWM vectors for driving converter cells, are serviced through the first in first out (FIFO) block, which displays vectors subsequently. Each vector has a data part and the time part, as presented in Fig.7.14. The time part indicates for how many clock cycles should one vector be applied. In this arrangement, the data bits refer to the converters cells status.

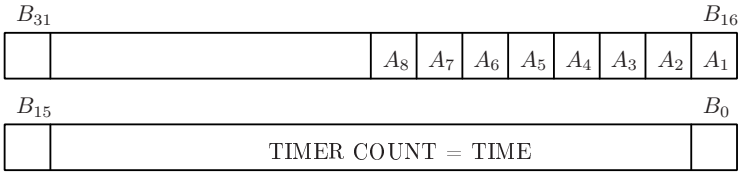


Figure 7.14: FIFO based vector for PWM signal generation in the case of phase A.

Bits B_{16} - B_{23} relate to the cells of the phase A according to the Fig. 7.1. For instance, if the bit B_{16} is "1", the first cell in the upper arm should be included in the current path for the given time period. If the value was zero, that cell should be bypassed. From this one bit, two opposite gating signals are produced, for the upper and lower switch of the half bridge, with insertion of the deadtime specified with the DSP. The deadtime is stored in one of the FPGA registers and the same value applies to all PWM signals produced by that FPGA. At every instant the insertion index of upper and lower arm is between 0 and 4, meaning that the integer part of the insertion index indicates how many cells are included in the current path, while the fractional part presents the duty ratio of one cell in the arm that performs PWM (application of the algorithm from Fig. 4.4). This means, that in one interrupt period maximum two cells (one in the upper arm and one in the lower) in the phase perform PWM. In the case that insertion index of the upper arm is 0.8, 3 cells of upper arm are always bypassed, while one (for instance A_2) performs 80 % PWM. At the same time, if the

insertion index of the lower arm is 3.2, 3 cells of the lower arm are always included in the current path, while the fourth cell (for instance A_8) performs PWM with the duty ratio of 20 %. In that case 5 switching vectors should be sent to FIFO register during one interrupt routine, as it is depicts in the Fig. 7.15. The bits B_{16}, B_{18} and B_{19} are '0', while bits B_{20}, B_{21} and B_{22} are "1" in all of these five vectors.

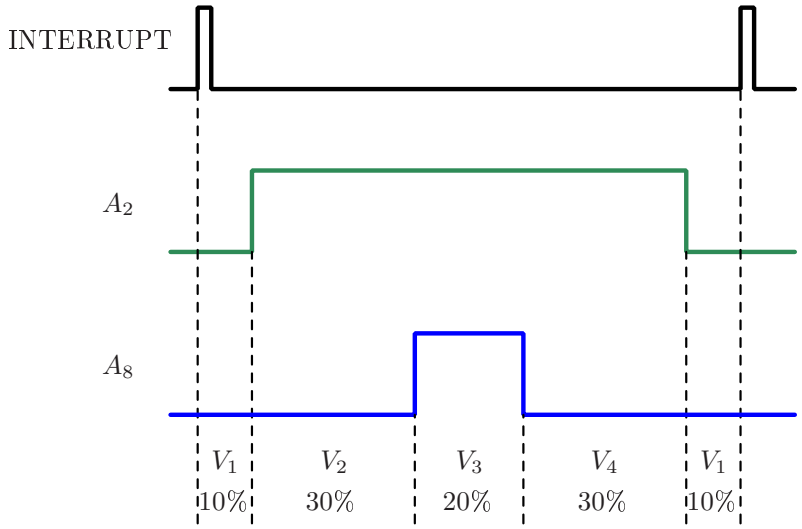


Figure 7.15: PWM vectors generation in the case of modulation indices 0.8 and 3.2.

To control three phases, with the given vector arangements, three FIFO registers are needed. This can be provided by using only one FPGA (a master FPGA board) that will provide 48 gating signals. However, the FPGA board has an interface to maximum 10 fibre optic receivers or transmitters, so an extension board needs to be used. This board accesses the 48 buffers on the FPGA board and transfers the data to the fibre optic transmitters.

The control signals for the protection (contactors) and pulsed load (thyristor gating signal), are produced by another FPGA board. Again a FIFO register is used, even though the gating signals are constant over the interrupt period. This means that once in the interrupt routine an information about these three signals is written to one FIFO register. Based on that register, three bits are outputted to the fibre optic

transmitters that are placed at the FPGA board. Contactors are never closed at the same time, and which control signal is "1" depends on the operating regime. The thyristor gate is triggered (by the *Pul* bit) in duration of one interrupt cycle, and for the rest of the pulse period, this bit is "0".

Each FPGA board features 10 A/D converters, and it is also possible to set the trip levels for all of those channels. In the case when some of the measured signals is beyond the trip level, the trip signal is sent to the FPGA and the trip information is written in the trip status register. The trip status register also contains the information about trips generated by software. Once a trip occurs all control outputs are disabled ("0"), and the DSP can write a trip information message on the display of the FPGA board.

7.3.2.2 DSP board

The C6713 DSK board is presented in Fig. 7.16 and it features a high precision, 225 MHz TMS320C6713 DSP. The board includes the JTAG interface, which allows programming and debugging via USB. By using this feature the code execution can be debugged directly from Code Composer Studio, together with the monitoring of the variables, registers and memory locations. By adding a DSK6XXXHPI Daughtercard from Educational DSP (Fig. 7.16), the downloading of the code is possible through the HPI port of the DSK and also, a serial USB communication allows the PC to monitor the variables in a real time. The host interface for the HPI is a graphical interface (Matlab based) developed within the research group and it provides the ability of plotting real time variables in Matlab and also online control of system variables.

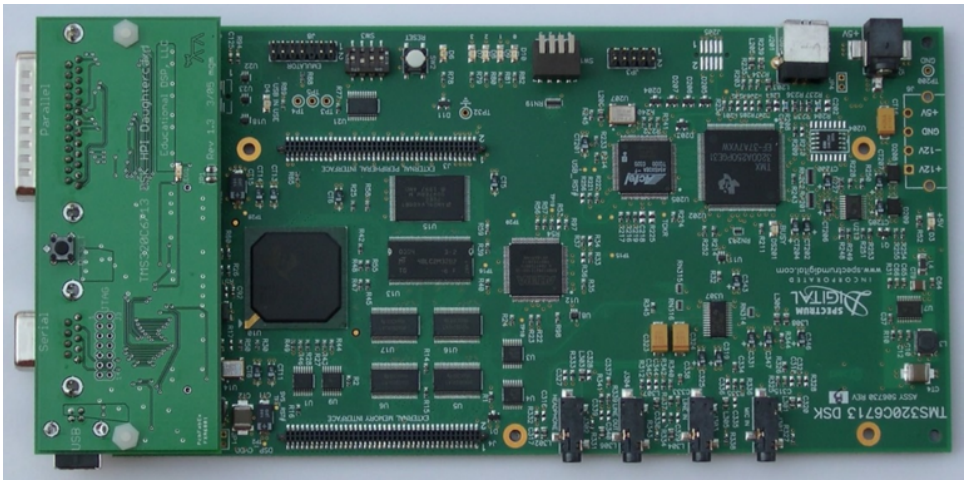


Figure 7.16: DSP board C6713 DSK by Texas Instruments together with the HPI Daughtercard from Educational DSP.

The DSP "sees" FPGA boarads (registers) as an external memory with the 32-bit parallel comunication link used for the adressing and the data. The FPGA boards registers are placed at location 0xA0000000, with separated memory spaces for different FPGA boards. The DSP writes to the FPGA registers after reset in order to make initial settings. After that, the master FPGA produces periodical interrupt signals, which lead to the execution of the interrupt routine on the DSP. This routine reads the measured signals, processes the data and executes the control algorithms. At the end a certain number of vectors is generated and written to the FIFO registers of the FPGA.

7.4 Control software

The control software is implemented on the DSP with the goal to provide safe operation and control of the experimental rig under various modes. At first initial settings need to be set, such as variable values, references and constants, including sensors gains and offset; the DSP settings, such as clock, and external memory interface;

the FPGA settings, such as swtiching period, deadtime, hardware trips, etc. When the initial settings are made, the master FPGA starts generating an interrupt signal which triggers the interrupt service routine (ISR) (this is executed periodically). This section focuses on the actions undertaken by the ISR through different operation modes. The second part of the section discusses the implementation of PI based controllers and their gains, with respect to Chapter 5.

The structure of the ISR algorithm is presented in Fig. 7.17. The ISR starts by taking the A/D readings and checking the existence of any software trips. In the case of the trip, the bit corresponding to that trip is set in the trip status register and all control outputs on the FPGA boards are disabled. Then the manual enable is checked and if it is not present, again all control outputs are disabled. If the manual enable is present, certain control methods should be applied and the control signals sent to the hardware.

By default the precharge mode is selected and contactor C_2 is closed. Also, by default converter should not produce any waveforms at the AC outputs. At first an uncontrolled precharge mode is applied, while the variac voltage is increased and the cell capacitors are charging, as has been described in section 5.8. Once the cell capacitors are charged to their nominal voltage, the variable that indicates the controlled precharge state is set. Having those settings, the ISR executes the code algorithm from Fig. 5.24. The phase balancing and other operations marked with red in Fig. 7.17 are not executed every time ISR is run but only once in 20 ms period. Also, these operations are applied on the average capacitor voltages as described in section 5.4. In this regime, from the HPI interface in Matlab a control signal *Sine_out* can be set in order to prepare the converter for the synchronisation to the grid. Upon receiving this signal, the PLL is synchronised, and the converter references are set to replicate the grid voltages on the converter AC outputs. Upon confirming that the converter output voltages are the same as the fundamental harmonic of the grid voltage, the contactor C_1 is manually enabled.

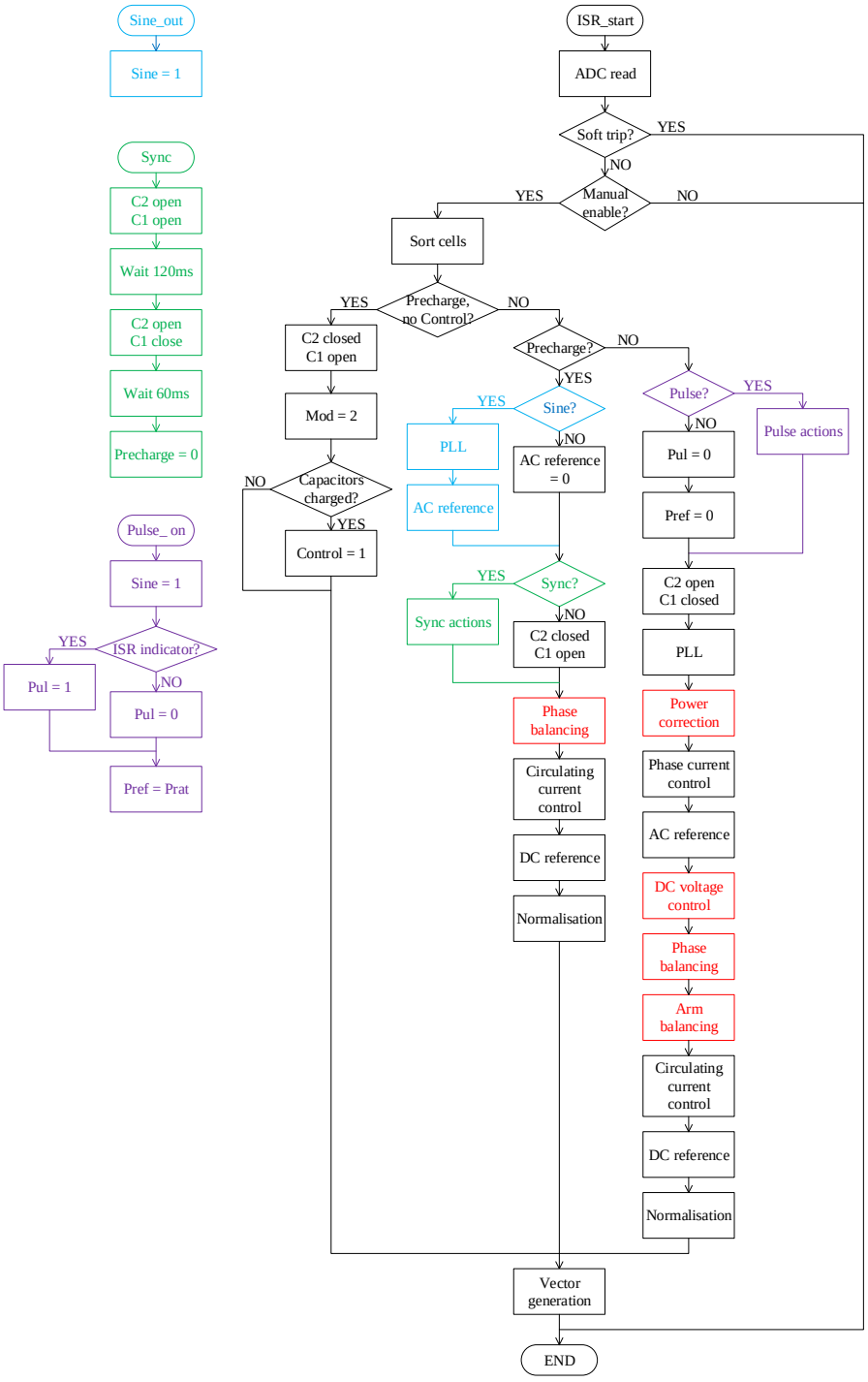


Figure 7.17: Structure of the ISR algorithm.

Again, a synchronisation signal can be sent through the HPI in order to end the precharge mode and start a grid connected operation. When this is received, the signal to open contactor C_2 is sent, than after 120 ms the signal to close contactor C_1 is sent, and after another 60 ms the precharge mode is finished. These timings are selected considering the finite contactors opening and closing times.

In the rectification mode, the nominal power drawn from the grid is zero, even though a certain power is needed to compensate for the losses and discharge resistors power. In this mode the algorithm from the Fig. 5.3 is executed. Similarly the algorithm with the x parameter arm balancing controller can be implemented (Fig. 5.21).

A signal that triggers pulse load operation can be sent from the HPI. In that case the power reference should be changed to the nominal pulsed load power reference, while the thyristor control signal should be generated during one interrupt period, once in the grid period. As it is presented in the Fig. 7.17, when the interrupt routine indicator matches the selected one (this can be varied with the respect to the grid voltages) the thyristor gate is triggered (Pul bit in the FIFO register).

7.4.1 Implementation of the control loops

The dynamics of the controllers is defined by the controller proportional and integral gains. The gain values used in the experimental implementation of control algorithms from Chapter 5 are presented in Table 7.2.

The presented gain values correspond to the controllers in Laplace domain (continuous), while their implementation on a digital control platform, requires discretisation. The sampling and switching frequency is set to 10 kHz. Similarly to the simulation model, a trapezoidal integration is assumed. The integrator has to be implemented and this requires an adaptation of controller gains. Based on the sampling frequency,

Table 7.2: Controller gains used for the purpose of the experimental rig control

Controller	Gain label	Gain value	Gain unit	Bandwidth
Phase currents	k_{dq_p}	10	$\mathrm{V \cdot A^{-1}}$	$2670\,\mathrm{rad \cdot s^{-1}}$
	k_{dp_i}	2000	$\mathrm{V \cdot A^{-1} \cdot s^{-1}}$	
Converter energy	k_{en_p}	2.76	$\mathrm{W \cdot V^{-1}}$	$8.8\,\mathrm{rad \cdot s^{-1}}$
	k_{en_i}	8.28	$\mathrm{W \cdot V^{-1} \cdot s^{-1}}$	
Circulating currents	k_{circ_p}	15	$\mathrm{V \cdot A^{-1}}$	$5000\,\mathrm{rad \cdot s^{-1}}$
	k_{circ_i}	750	$\mathrm{V \cdot A^{-1} \cdot s^{-}1}$	
DC voltage	k_{dc_p}	0.12	$\mathrm{A \cdot V^{-1}}$	$14.2\,\mathrm{rad \cdot s^{-1}}$
	k_{dc_i}	0.12	$\mathrm{A \cdot V^{-1} \cdot s^{-1}}$	
Phase balancing	k_{pb_p}	0.1	$\mathrm{A \cdot V^{-1}}$	$120\,\mathrm{rad \cdot s^{-1}}$
	k_{pb_i}	0.02	$\mathrm{A \cdot V^{-1} \cdot s^{-1}}$	
Arm balancing	k_{ab_p}	3.45	$\mathrm{W \cdot V^{-1}}$	$10.5\,\mathrm{rad \cdot s^{-1}}$
	k_{ab_i}	1.725	$\mathrm{W \cdot V^{-1} \cdot s^{-1}}$	
Parameter x	k_{x_p}	0.3		$6.1\,\mathrm{rad \cdot s^{-1}}$
	k_{x_i}	1	s^{-1}	
PLL	k_{pll_p}	2	$\mathrm{rad \cdot s^{-1} \cdot V^{-1}}$	$427\,\mathrm{rad \cdot s^{-1}}$
	k_{pll_i}	500	$\mathrm{rad \cdot s^{-2} \cdot V^{-1}}$	

the controller gains are modified as given by:

$$\begin{aligned} k_{pi\_1} &= \frac{T_s}{2} k_i + k_p \\ k_{pi\_2} &= \frac{T_s}{2} k_i - k_p \end{aligned} \tag{7.5}$$

where k_p and k_i are original gains of continuous controller and k_{pi_1} and k_{pi_2} are newly derived gains used to implement a PI controller as described by:

$$PI_{out} = PI_{out\_prev} + k_{pi\_1} \cdot err + k_{pi\_2} \cdot err_{prev} \tag{7.6}$$

where controller error err and output PI_{out} relate to the current sampling instant, while err_{prev} and PI_{out_prev} relate to the previous sampling instant. In the case of voltage controllers that are applied on the averaged waveforms, fundamental period T is substituted in (7.5) instead of T_s, while (7.6) is executed once in a fundamental period (previous values in that case relate to the previous execution of the equation).

7.5 Summary

A construction of a small-scale laboratory prototype including the 9-level MMC converter and a resonant DC load, with the goal to validate the application of a MMC as a grid interface of the pulsed DC load, has been discussed. The design consideration in terms of component slection, driving circuits, and protection and precharge circuit are presented in detail. Additionally, the control hardware including DSP-FPGA platform and control software used for operating the rig are described.

The presented experimental rig will be used for generation of experimental results which are the topic of the next chapter.

Chapter 8

Experimental results

8.1 Introduction

This chapter presents the most relevant experimental results based on the converter and the load described in section 7.2. Performed experiments had a task to prove the concepts presented by theoretical analysis and simulation. A grid-connected MMC under the pulsed DC load requires multiple control loops to provide safe converter operation and satisfy the specifications related to the low AC power fluctuation. Chapter 5 presented the control strategy for such an application, including decoupled AC and DC side control, where AC side is controlled by the phase currents (d, q) control and DC side is controlled by circulating current controllers. Additionally, there are outer control loops with slower dynamics that regulate DC voltage level, the amount of energy stored in the converter and the sharing of the stored energy among phases and arms of the same phase. The pulsed DC load is a constant source of the imbalance between the arms of the converter phases. Therefore, arm balancing controllers are crucial for proper converter operation ensuring low AC power fluctuation. The section 5.6 presented three arm balancing methods and all of them are experimentally verified. Other control loops remain unchanged while the arm balancing controllers are alternating.

The next section relates to the validation of precharge and PLL algorithms. Obviously, the success of those algorithms is crucial for obtaining all experimental results. Therefore, the presentation of those provides a complete validation of the experimental rig.

The third section relates to the waveforms relevant for the pulse load, such as the DC voltage, load output voltage and the load pulsed current.

The following section presents the relevant experimental results used for the validation of the control loops presented in Chapter 5. As in Chapter 6, the most important results related to the power quality and AC currents, as well as the circulating current waveforms, are presented for all arm balancing methods. The same nomenclature as in Chapter 6 is used, i.e. arm balancing methods from section 5.6 are termed arm balancing method one, two and three. DC voltage controller, energy controller, and phase balancing loop would exhibit the same behavior with all arm balancing methods, hence they can be analysed only for the arm balancing method one. All presented data relates to the pulse position of 1.7 ms after phase A grid voltage positive gradient zero crossing, which corresponds to the pulse position angle of 0.534 rad. This pulse position is suitable for the analytical arm balancing solution (arm balancing method one), which is sensitive to different pulse position.

Finally, all three arm balancing methods were evaluated for different pulse positions, covering one third of the grid voltage period. The amount of the AC and DC power fluctuation together with the arm balancing controller parameters are presented for different pulse positions. The acquired results are compared with the results obtained by simulation.

Some of the results presented in this chapter are recorded by the HPI graphical interface in Matlab. The waveforms recorded through the HPI are sampled at 10 kHz, which is the equivalent switching frequency. Hence, current readings obtained by HPI do not have a switching ripple. However, high frequencies are already aliased in the phase currents thanks to the arm and phase inductors. The other results are

obtained by 200 MHz oscilloscope using current probes (30 A, 100 kHz, 1 % tolerance) and voltage probes (700 V, 70 MHz, 2 % tolerance). For the pulsed load current measurement a Rogowski probe (6 kA, 16 MHz) is used.

8.2 Evaluation of the precharge and PLL

In the controlled precharge mode, upon sending the *Sine_out* signal (Fig. 7.17), the controller performs a PLL to track the grid angle and also provide converter AC references in phase with the grid voltages. At that point converter is operated as an inverter, with open AC terminals. Figs. 8.1 - 8.4 are captured by the HPI.

The grid phase A voltage and gird voltages d and q components and phase angle are given in the Fig. 8.1. The signal *Sine_out* is sent at 0 s.

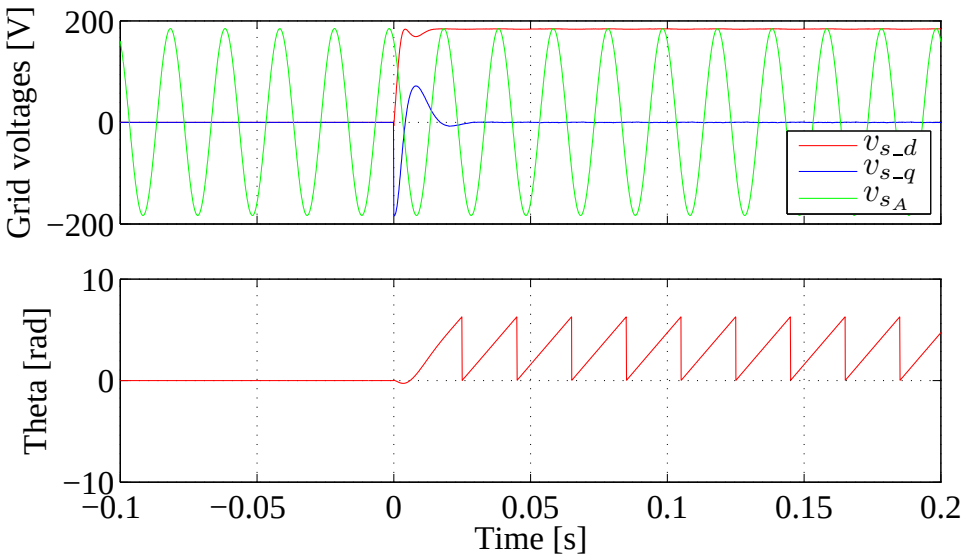


Figure 8.1: Grid voltages and phase angle when AC waveforms output is enabled in controlled precharge mode.

At that point the arm balancing is not applied, only the energy stored within phases

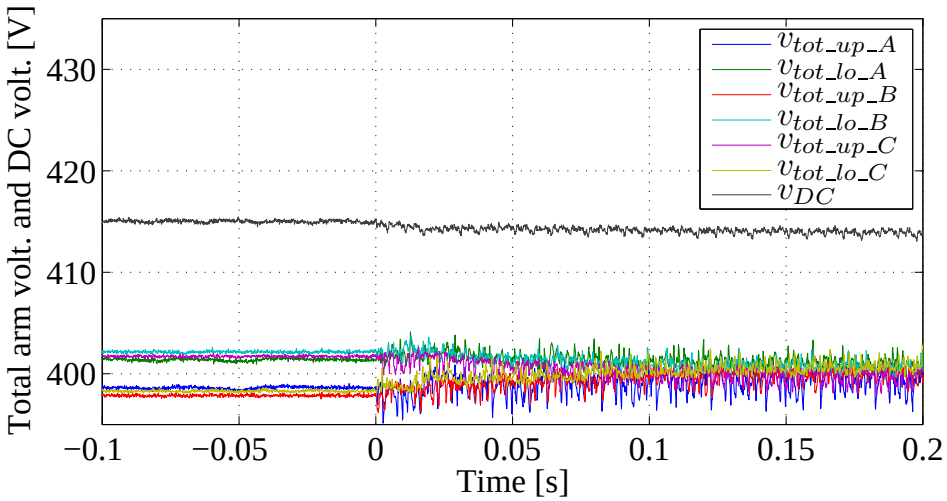


Figure 8.2: Total arms voltages and the DC voltage when AC waveforms output is enabled in controlled precharge mode.

is controlled. Fig. 8.2 shows the sum of all cell capacitor voltages of each arm and the DC voltage. The DC voltage is higher than nominal and it is not controlled in the precharge mode.

The insertion indices for all converter arms are presented in Fig. 8.3. Once the AC output is enabled the arm voltages references contain the AC part, as well as the insertion indices.

After it has been confirmed that the converter outputs correct AC waveforms, the contactor C_1 is manually enabled. However, it remains open until it is enabled by software. At 0 s *Sync* signal is sent (Fig. 7.17), to open contactor C_2 and after a defined amount of time close C_1. Fig. 8.4 shows the sum of all cell capacitor voltages of each arm and the DC voltage. Since here the precharge mode ends, the DC voltage is controlled and it shortly reaches the nominal level.

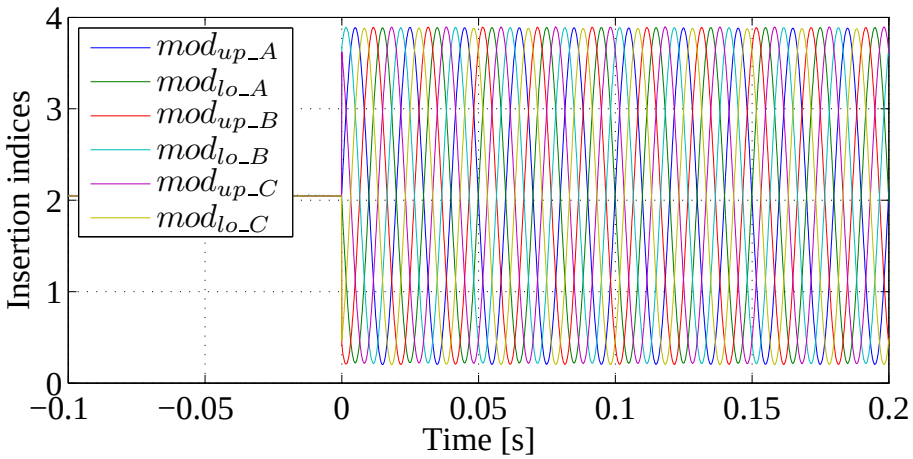


Figure 8.3: Insertion indices for all converter arms when AC waveforms output is enabled in controlled precharge mode.

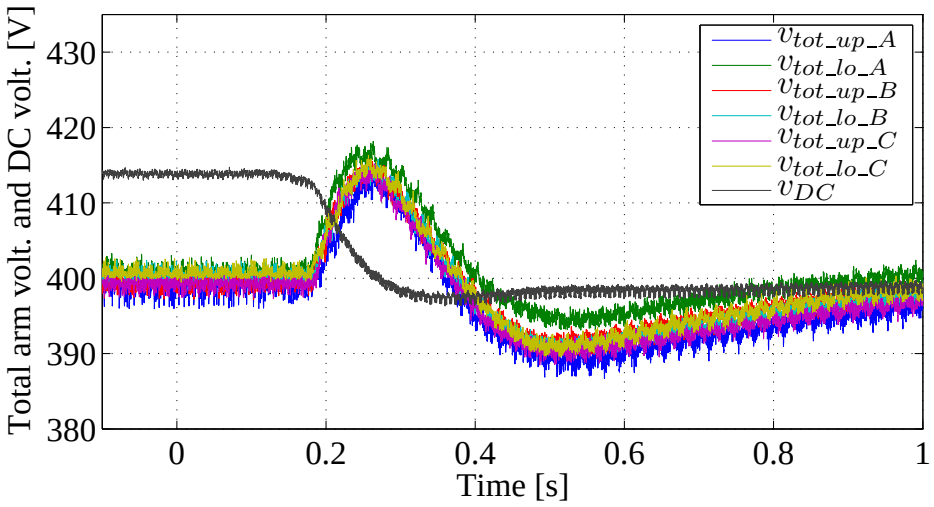


Figure 8.4: Total arms voltages and the DC voltage when synchronisation to the grid is enabled.

Fig. 8.5 presents phase A grid and converter voltage (measured with respect to the grid neutral) and the phase current after synchronsiation to the grid and before enabling the pulsed load. The converter draws small current and low power, since it is in a no-load condition. After the grid synchronisation the converter is ready for

the pulsed load.

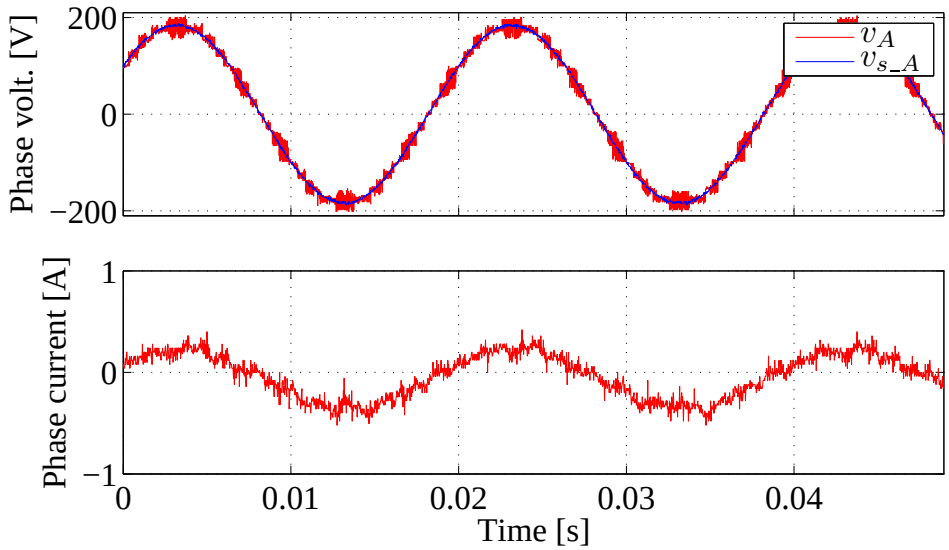


Figure 8.5: Grid and converter phase A voltage and phase A current when converter is synchronised to the grid in no-load condition.

8.3 Pulsed load waveforms

The pulsed load current, DC voltage and output voltage (Fig. 7.6) are observed under steady state conditions when arm balancing method one is applied. Fig. 8.6 presents pulsed load characteristics, showing the periodical discharge of the DC link capacitor by a high pulsed current. Fig. 8.7 presents the pulsed load characteristics by focusing on one current pulse. As it is presented, the load current has a duration of approximately 150 μs and the peak value of 3.35 kA, which is slightly lower than theoretically predicted value (7.4). The effect of the thyristor reverse recovery is visible in the current shape. The DC voltage droop is approximately 40 V which corresponds to 10 % of the nominal value.

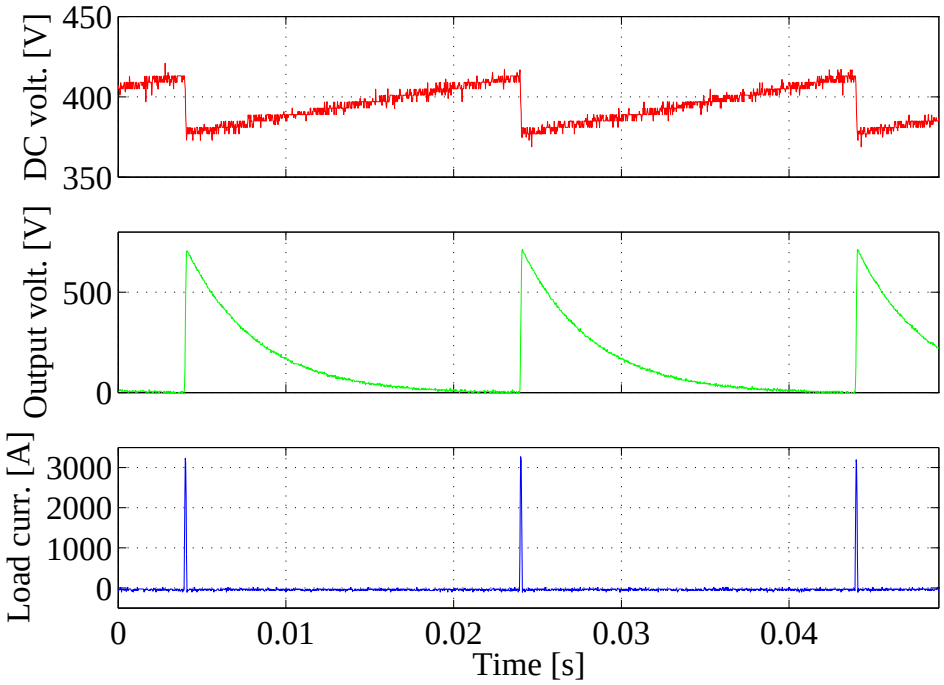


Figure 8.6: Pulsed load characteristics: DC voltage, output voltage and load current under steady state conditions.

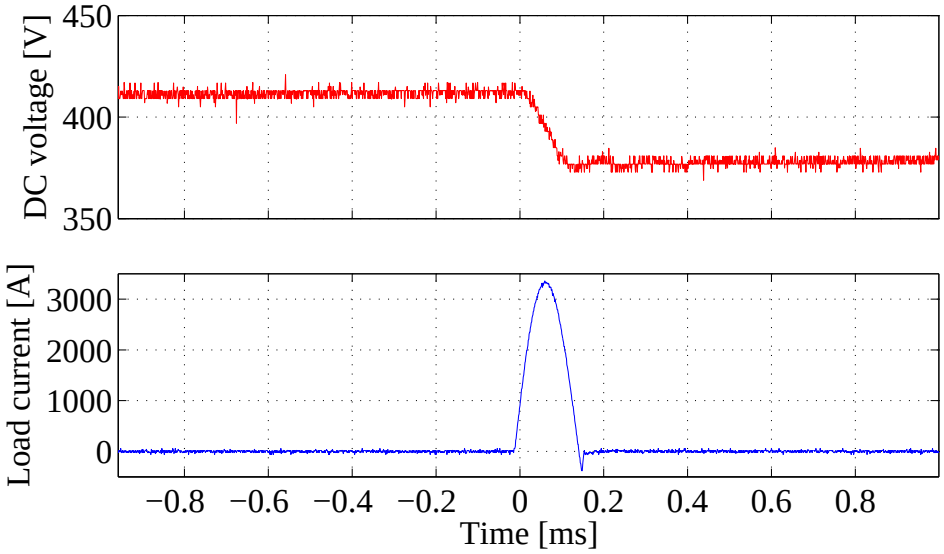


Figure 8.7: Pulsed load characteristics: DC voltage and load current, with the focus on one current pulse.

8.4 Validation of the control loops

This section is focused on the validation of the control loops presented in detail in Chapter 5. The focus is on the two main current controllers used as inner loops and slow voltage controllers used as outer loops to the current controllers.

8.4.1 Phase current control

The following figures are captured to evaluate AC side controller performance, including the d, q current controller providing AC power control, and energy balancing controller. Figs. 8.8 - 8.13 were captured and generated on the basis of HPI data. Those figures relate to the arm balancing method one.

Upon grid synchronisation the converter draws low power of approximately 100 W to compensate for the losses and the power dissipated on the discharge resistors. Once the pulsed load is enabled, the AC power reference is set to 6.9 kW. This step increase of the power, translated to the d, q current controller is presented in Fig. 8.8 for the case of arm balancing method one.

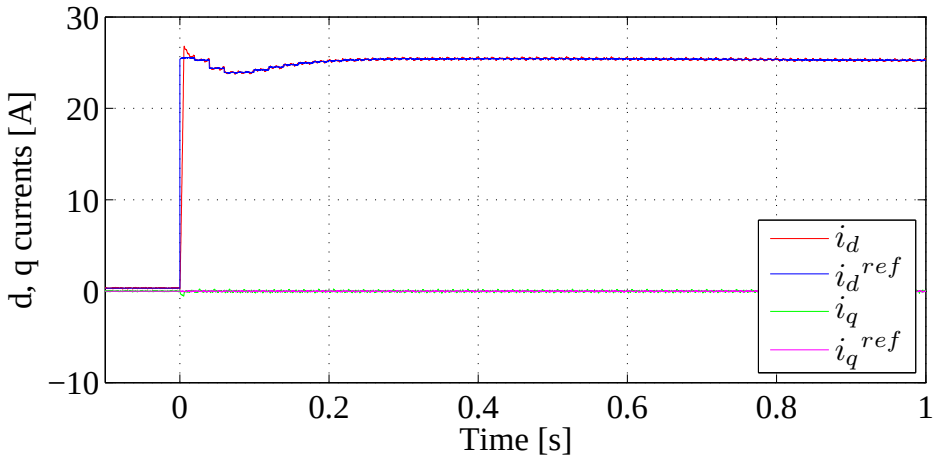


Figure 8.8: The d, q current controller reference tracking during transient when pulsed load is enabled.

The generation of the d, q component of the AC voltage reference, on the basis of the feed-forward grid voltage components and the d, q current controller output (Fig. 5.2) is presented in Fig. 8.9.

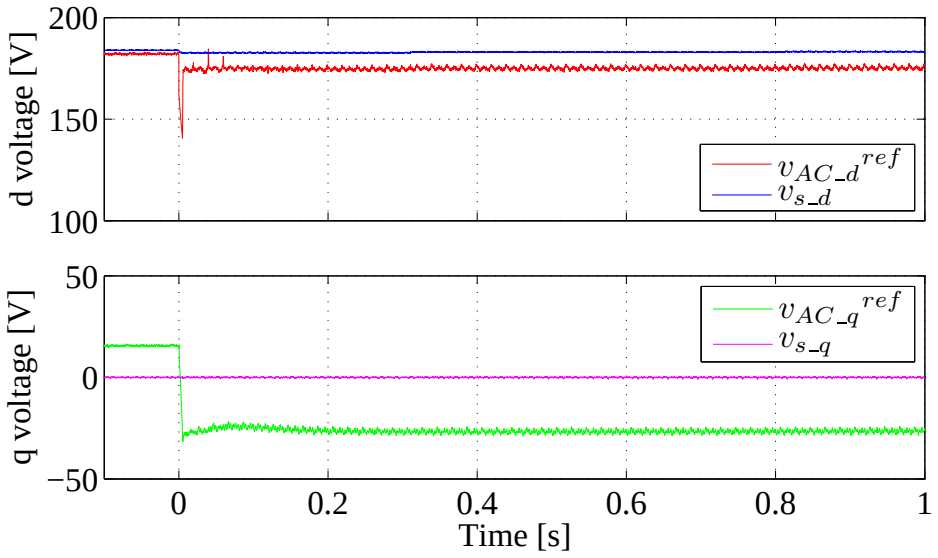


Figure 8.9: Grid voltage and the converter AC voltage d, q components during transient when pulsed load is enabled.

The grid active power and its reference during transient are presented in Fig. 8.10. The power is computed on the basis of the grid voltages and currents d, q components, as given by (5.1). The AC reference is constant over 20 ms period, since it is corrected by the converter energy controller.

The ripple of the measured d, q axis currents is visible in Fig. 8.11. The amplitude of this ripple in the phase current d, q components is approximately 0.3 A. The ripple has a certain amount of 50 Hz component, which indicates the presence of either zero or 100 Hz components in the grid/phase currents. The zero sequence component can not exist, since 3 wire AC system is used. However, inaccurate sensor readings might induce some DC offsets. A 100 Hz component might be present in actual phase current waveforms, as a consequence of system non-idealities, and propagation of the disturbances. Note here, that the d, q axis current references are not constants even

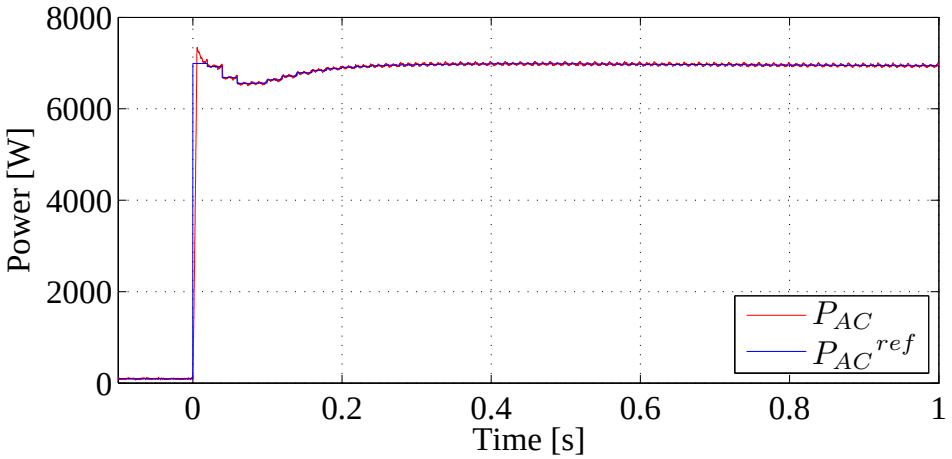


Figure 8.10: Grid active power and its reference, during transient when pulsed load is enabled.

though the AC power reference is constant. This is due to imperfect grid voltages generated by the AC source, and limited accuracy of the voltage sensors.

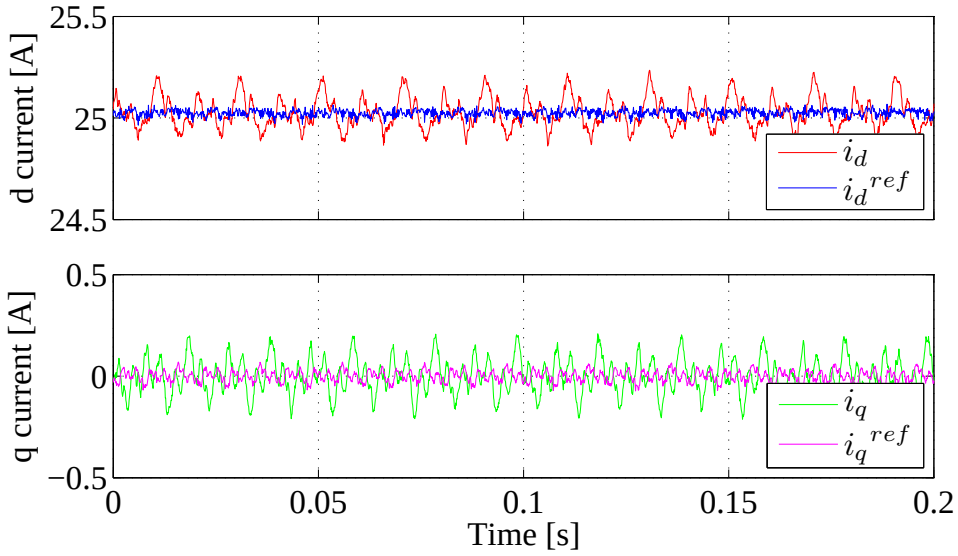


Figure 8.11: The d, q current controller reference tracking under steady state conditions with pulsed load.

The AC power drawn by the converter and the DC power delivered to the load under

steady state conditions with pulsed DC load are presented in Fig. 8.12. Since this result is obtained by the HPI interface, the switching harmonics in AC currents are neglected, providing lower AC power fluctuation (compared to reality). The AC power fluctuation is approximately 100 W which corresponds to 1.45 %. A certain amount of 50 Hz component ripple is present in the active power, which is a consequence of the non-zero 100 Hz component or DC offset in phase currents. At the moment of the pulse instant there is no distortion in the AC power waveform, while the DC power clearly indicates the presence of the pulsed load.

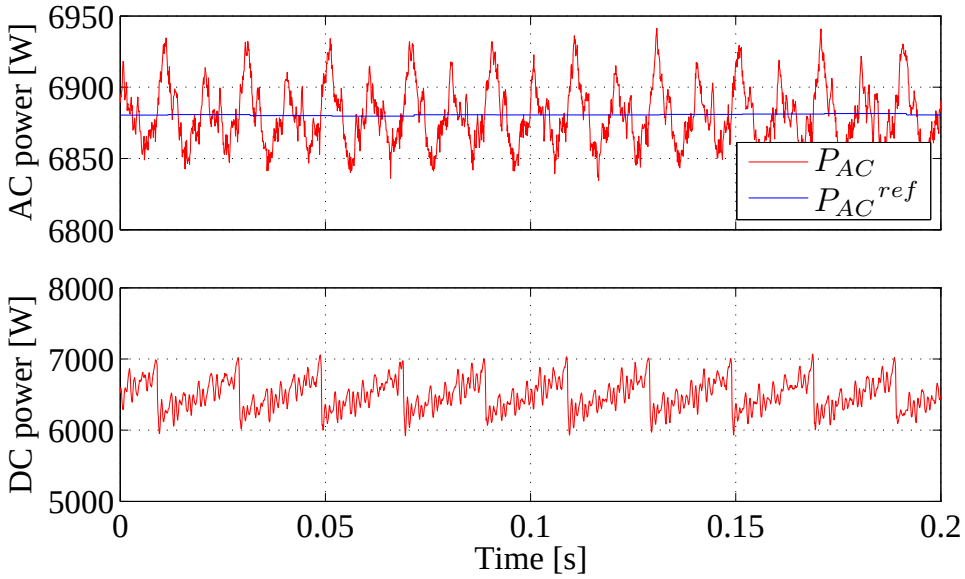


Figure 8.12: Grid active power and its reference and the converter DC power under steady state conditions with pulsed load.

The AC power harmonics are presented in Fig. 8.13. The dominant harmonic in the AC power ripple is at 100 Hz indicating the potential imbalance in powers between phases, i.e. not equal amplitudes of 50 Hz components of phase voltages or currents. This might be a consequence of inaccurate transducer gains.

Converter AC currents, captured by the oscilloscope in the transient from no-load to the pulse load condition, are presented in Fig. 8.14. Before the pulse starts

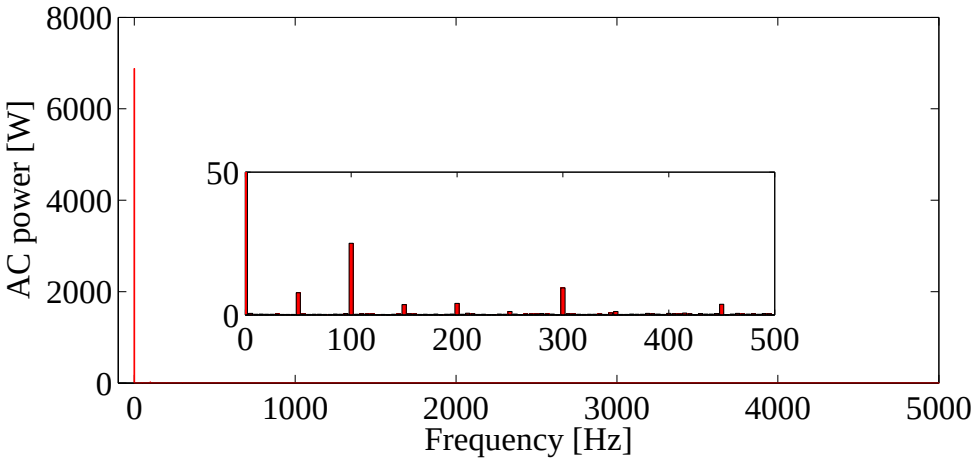


Figure 8.13: Grid active power harmonics under steady state conditions with pulsed load.

converter draws approximately 0.4 A, while when the pulse starts the peak current is approximately 25 A. The captured results relate to arm balancing method one.

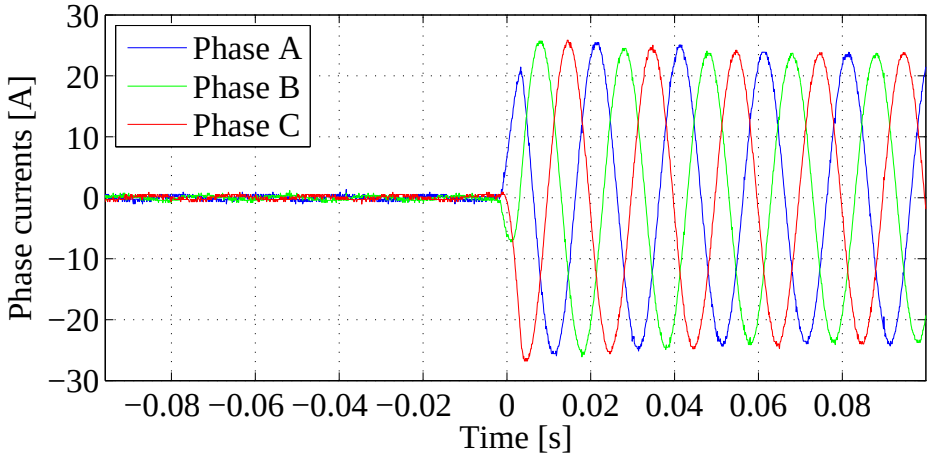


Figure 8.14: Phase/grid currents during transient when pulsed load is enabled.

8.4.1.1 Phase currents in the cases of different arm balancing methods

The following figures show phase currents and their harmonic spectrum under steady state conditions for all three arm balancing methods. Figs. 8.15 and 8.16 present the phase currents and their spectrum in a steady state under pulsed DC load when arm balancing method one is applied.

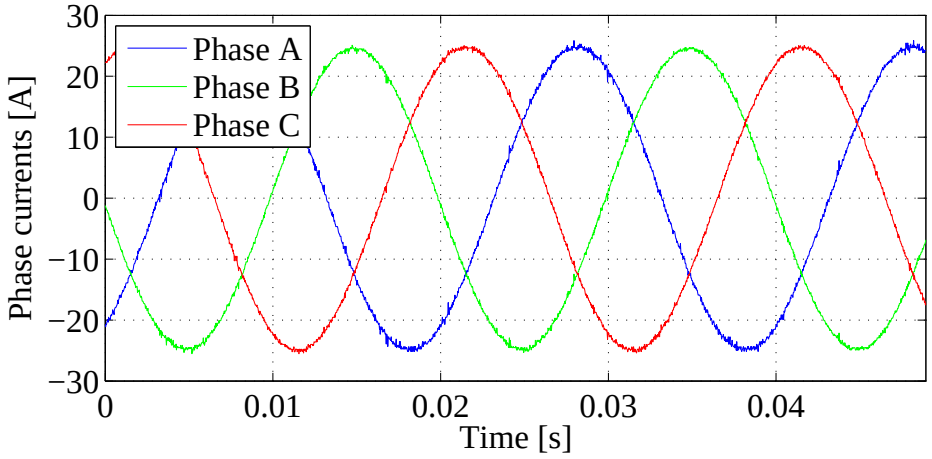


Figure 8.15: Phase/grid currents in steady state under pulsed DC load, when arm balancing method one is applied.

The spectrum from Fig. 8.16 indicates a certain amount of imbalance of the fundamental current component. Phase B has a lower amplitude of the fundamental, when compared to phase A and C. This might ba a consequence of a uneven gains of the current transducers or the oscilloscope probes. A presence of the 100 Hz component in the AC power indicated uneven amplitudes of the fundamental component in phase currents. Other harmonic components mainly relate to the presence of the non-zero average current, and 100 Hz, 350 Hz, etc. All harmonic components apart from the fundamental have an amplitude lower than 0.1 A, providing relatively clean phase current waveforms (Fig. 8.15).

The phase currents do not have significant switching frequency harmonics (around 10 kHz), meaning that the currents obtained by the HPI are very similar to those

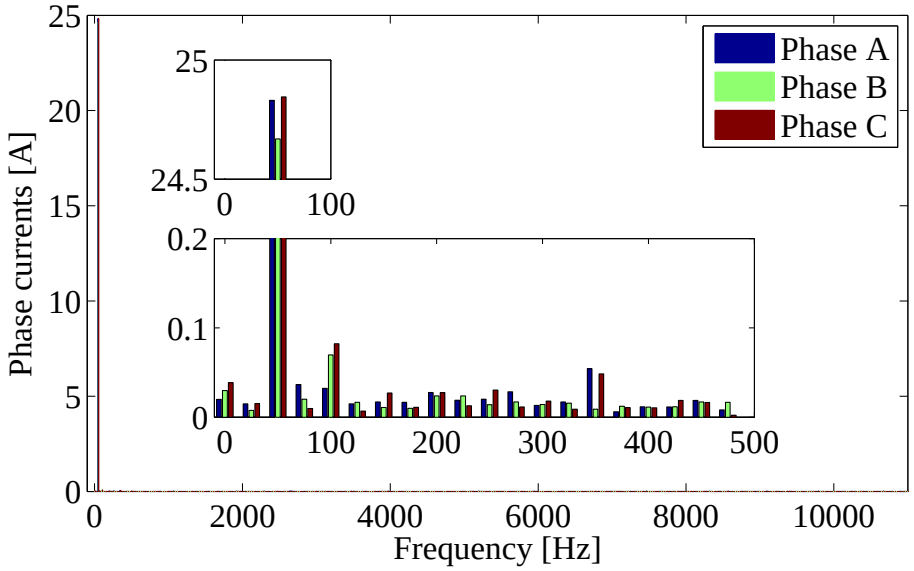


Figure 8.16: Phase/grid currents spectrum in steady state under pulsed DC load, when arm balancing method one is applied.

captured by the oscilloscope. Therefore, the AC power fluctuation computed from the HPI captured d, q voltage and currents, should not have a significantly lower value when compared to reality.

Figs. 8.17 and 8.18 present the phase currents and their spectrum under steady state conditions with the pulsed DC load when arm balancing method two is applied. The harmonic spectrum (Fig. 8.18) is similar to the case when arm balancing method one is applied. The same amount of imbalance is present in the fundamental currents component. Additionally, the average value and low frequency harmonics all have an amplitude below 0.1 A. The switching harmonics at 10 kHz are negligible.

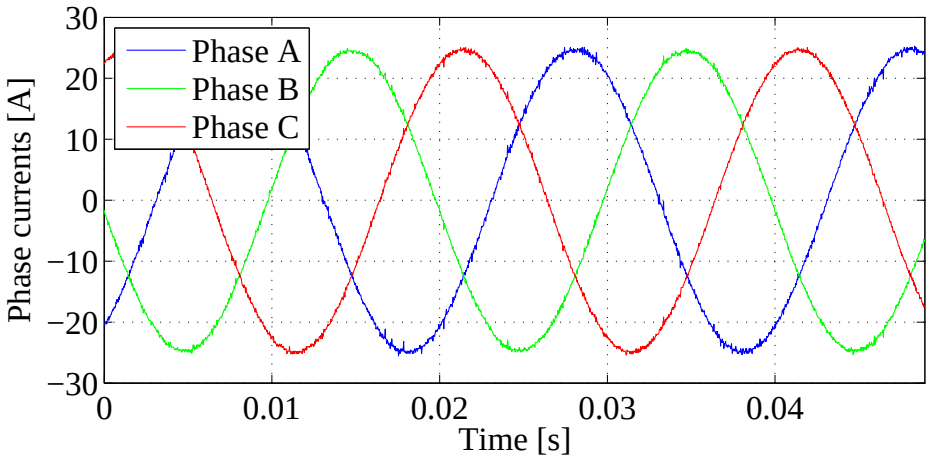


Figure 8.17: Phase/grid currents in steady state under pulsed DC load, when arm balancing method two is applied.

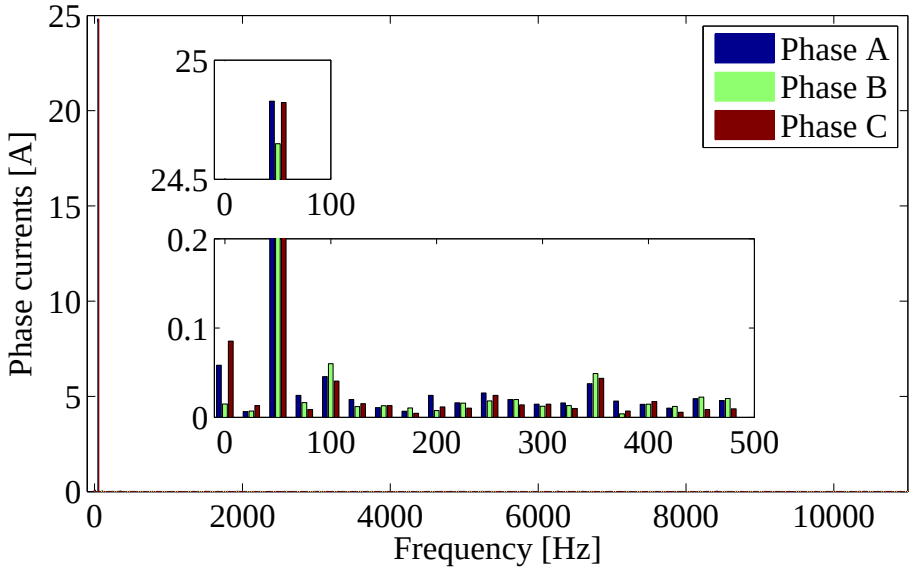


Figure 8.18: Phase/grid currents spectrum in steady state under pulsed DC load, when arm balancing method two is applied.

Figs. 8.19 and 8.20 show phase currents waveforms and their spectrum under steady state conditions with the pulsed DC load when arm balancing method three is applied. Again, obtained waveforms and current harmonics are similar to the results when

balancing methods one and two are applied. Some low order harmonics with the amplitude below 0.1 A and imbalance in the fundamental component indicates very similar performance. Again, the region around the equivalent switching frequency does not contain harmonics of significant amplitude.

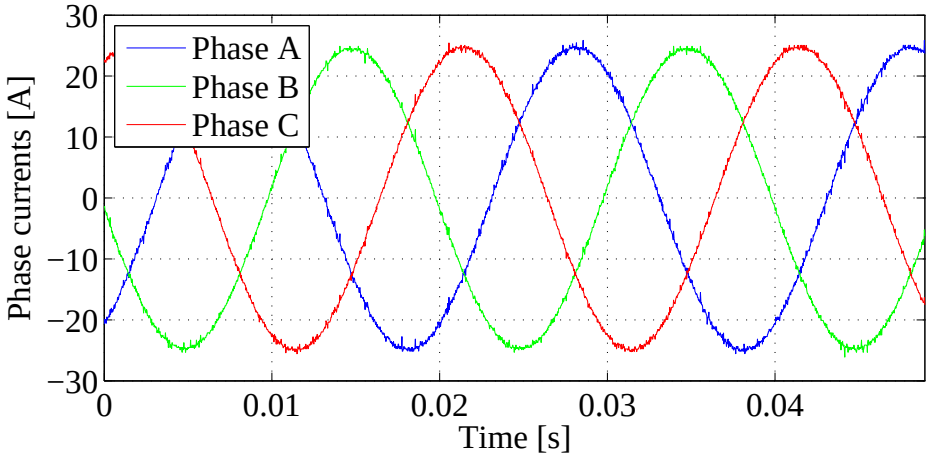


Figure 8.19: Phase/grid currents in steady state under pulsed DC load, when arm balancing method three is applied.

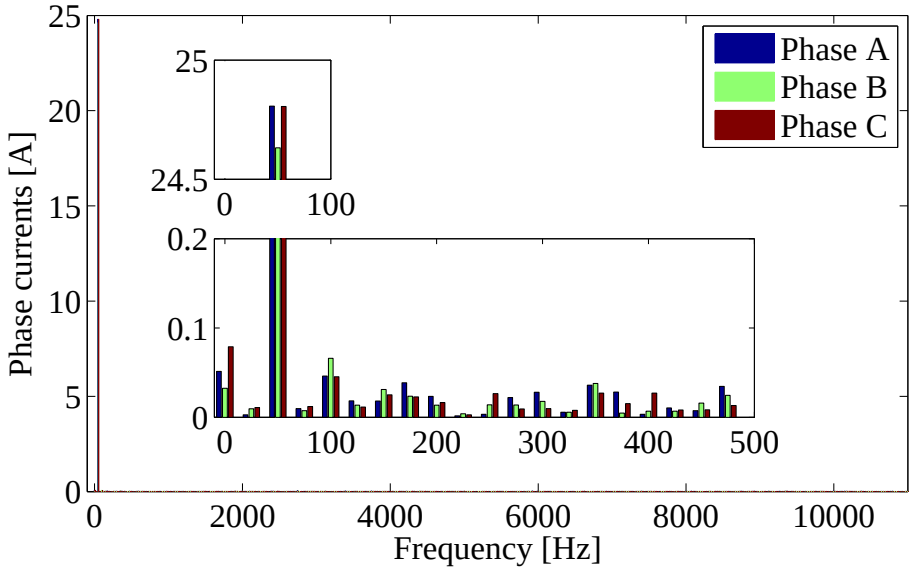


Figure 8.20: Phase/grid currents spectrum in steady state under pulsed DC load, when arm balancing method three is applied.

8.4.1.2 Energy control

The converter energy control loop is validated by the waveforms obtained by the HPI interface. Figs. 8.21 and 8.22 are recorded for the arm balancing method one, while the similar waveforms are expected for other arm balancing methods. The Fig. 8.21 presents input and output signal of the PI based converter energy controller (Fig. 5.9) during transient from no-load to pulsed load condition. The input signal is the error in the sum of all cell capacitor voltages, while the output is a power correction to be added to the AC power reference.

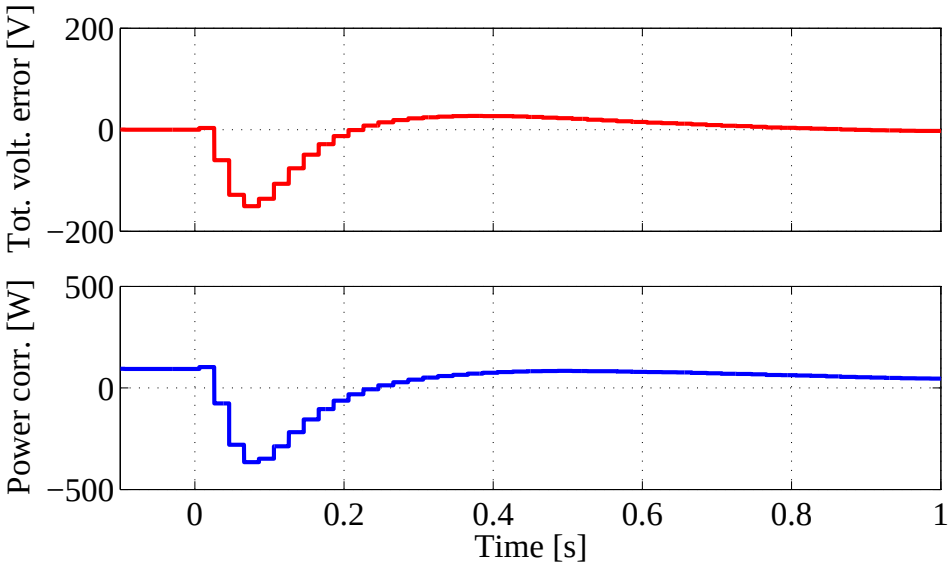


Figure 8.21: The converter energy controller waveforms during transient when pulsed load is enabled.

The sum of all cell capacitor voltages and its reference is presented in the Fig. 8.22. The sum of all capacitor voltages reaches its reference about one second after the pulsed load is enabled.

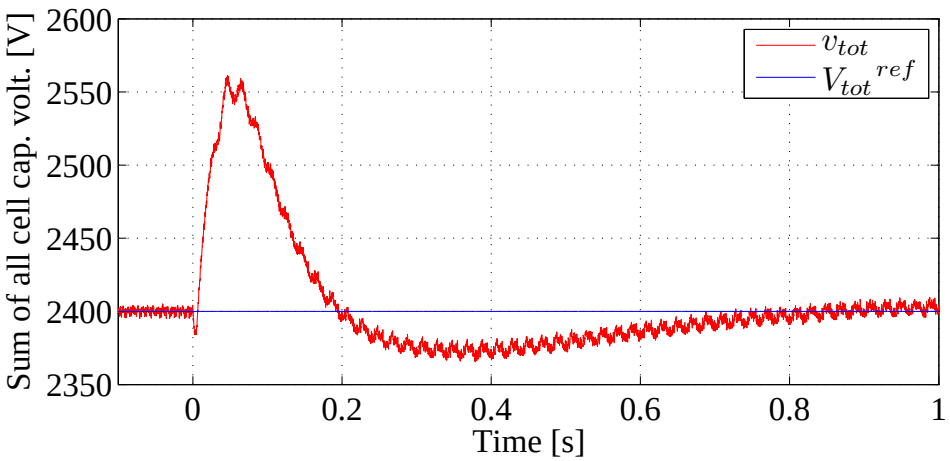


Figure 8.22: Sum of all cell capacitor voltages and its reference during transient when pulsed load is enabled.

8.4.2 Circulating current control

This section relates to the validation of the circulating current controllers and the voltage controllers used as outer loops to those controllers. The circulating current reference comprises of one third of the DC current reference, a component generated by the phase balancing loop and a component generated by the arm balancing loop (in the case of arm balancing methods one and two). Since all arm balancing methods provide different circulating current references, the detailed results will be presented for all arm balancing methods.

The following figures relate to the circulating current controller and they are captured by the HPI interface. The circulating current and its reference during transient from no-load to pulsed load condition when arm balancing method one is applied is presented in Fig. 8.23.

The circulating current controller together with the DC voltage as a feed-forward term generates DC part of the arm voltages references. In the case of phase A, the DC part of the reference together with the DC voltage is presented in Fig. 8.24.

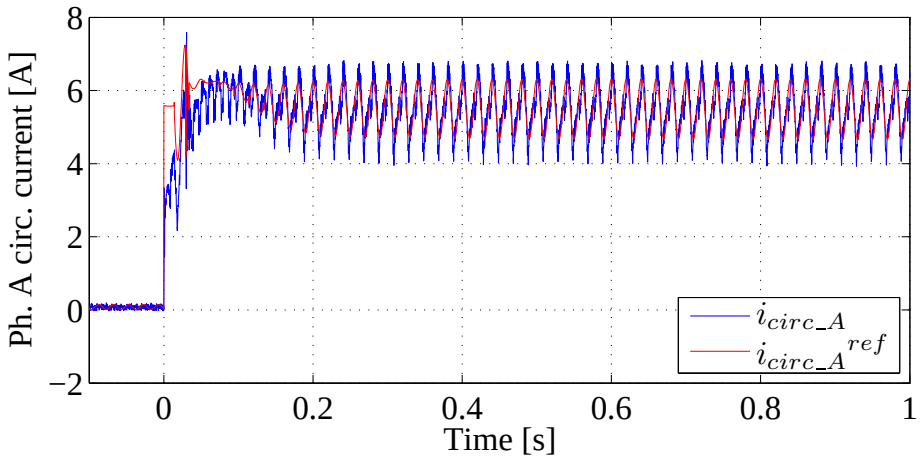


Figure 8.23: Phase A circulating current and its reference during transient when pulsed load is enabled.

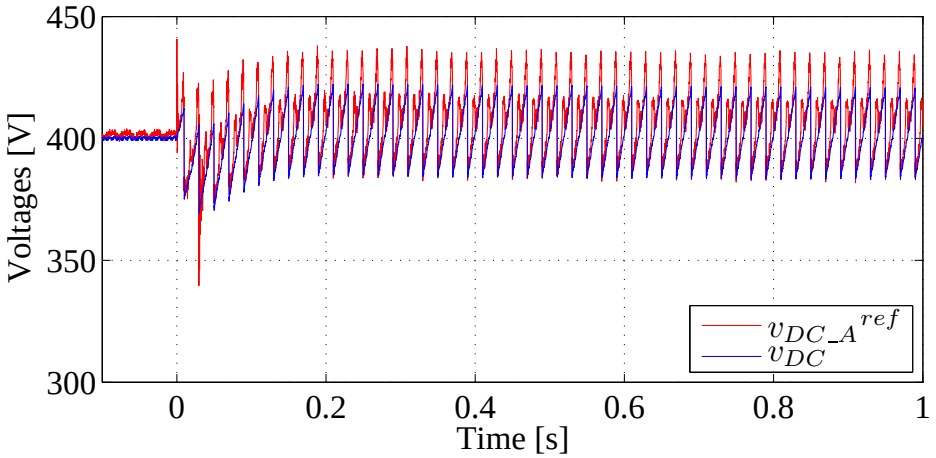


Figure 8.24: Phase A DC part of the reference and DC voltage during transient when pulsed load is enabled.

If the DC voltage is fed without any modification, a huge current spike will be present in the DC current and circulating currents during and after pulse. This is a consequence of delays present in the system, including sampling, calculation and application delay. In order to avoid a current spike, which might trip the circuit protection elements, two sample delay compensation is applied on the DC voltage. This in-

cludes empirical droop emulation in the DC voltage reading two samples before the DSP would actually "see" it. It has been proven in simulation (where one sample delay compensation is needed) that the AC waveforms would still be clean even if delay compensation is not applied.

8.4.2.1 Circulating current in the cases of different arm balancing methods

Fig. 8.25 shows the phase A circulating current and its reference in the case of arm balancing method one. It can be seen from the figure that the circulating current follows the reference but that there is a significant distortion occurring twice in the fundamental period. This can be related either to the arm currents zero crossing or rounding of the insertion indices. Namely, when the arm currents are crossing zero, the conduction device in the converter cells is changed from diode to switch and vice versa. Also, the decision on the switching pattern in the modulation block is based on the current sign. The possible issue with the insertion indices is when both upper and lower arm indices are in the region of small or big modulation index. In that case the PWM is not performed and the insertion index is rounded to the closest integer. In both scenarios the sum of the two arms voltages does not result in the DC voltage reference, which is a disturbance to the circulating current controller.

Fig. 8.26 shows the spectrum of the phase A circulating current and its reference in the case of arm balancing method one. The circulating current reference has only DC part and the 50 Hz component, and both of these quantities are perfectly followed. However, the distortion is also present and it is dominant at 100 Hz (it happens twice in the period) and at multiples of 100 Hz.

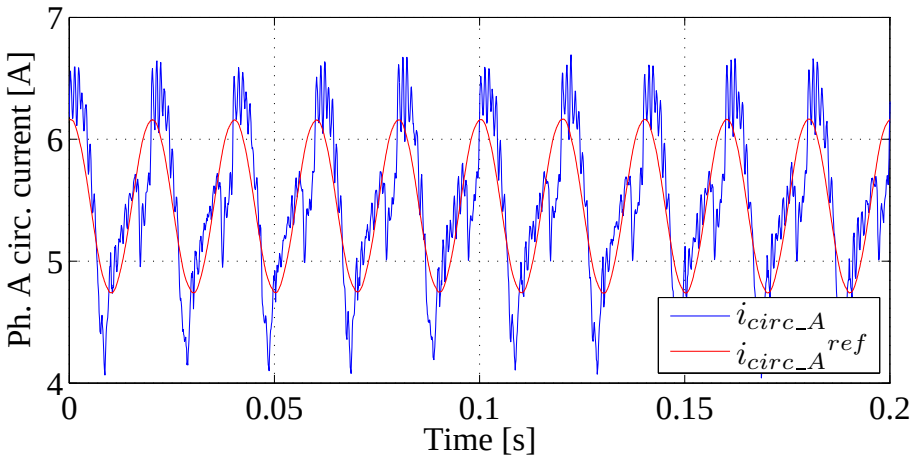


Figure 8.25: Phase A circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method one is applied.

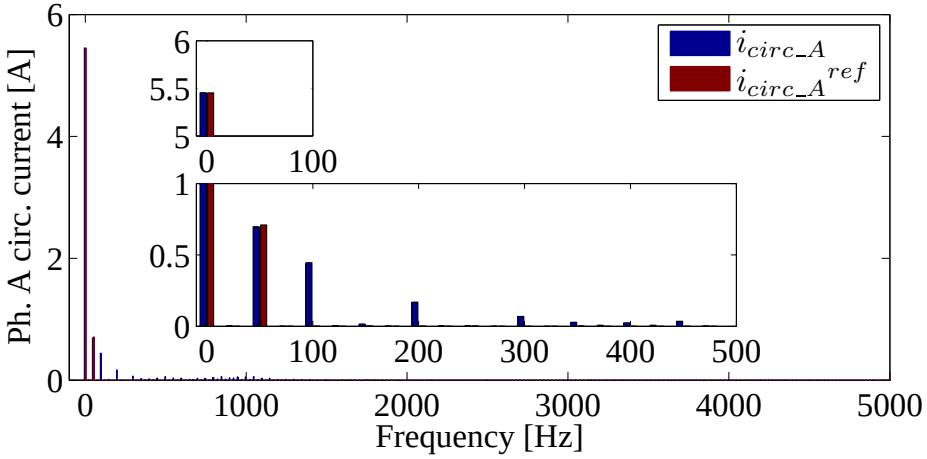


Figure 8.26: Spectrum of the circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method one is applied.

Fig. 8.27 presents the phase A circulating current and its reference in the case when arm balancing method two is applied. Again, there is a distortion in the circulating current occurring two times in the fundamental period.

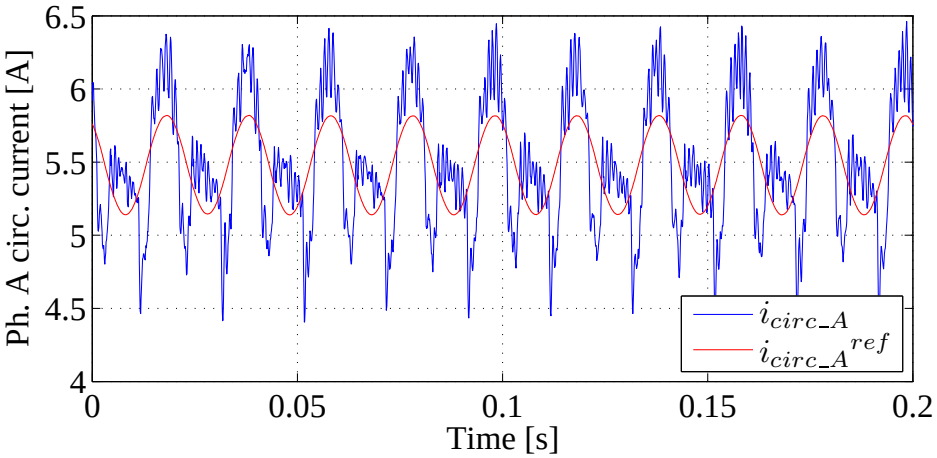


Figure 8.27: Phase A circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method two is applied.

The spectrum of the phase A circulating current and its reference is shown in Fig. 8.28. The tracking of the reference mean value and 50 Hz component is perfect. However, the harmonics at 100 Hz component and the multiples of 100 Hz are present with the similar amplitudes as in the case of arm balancing method one.

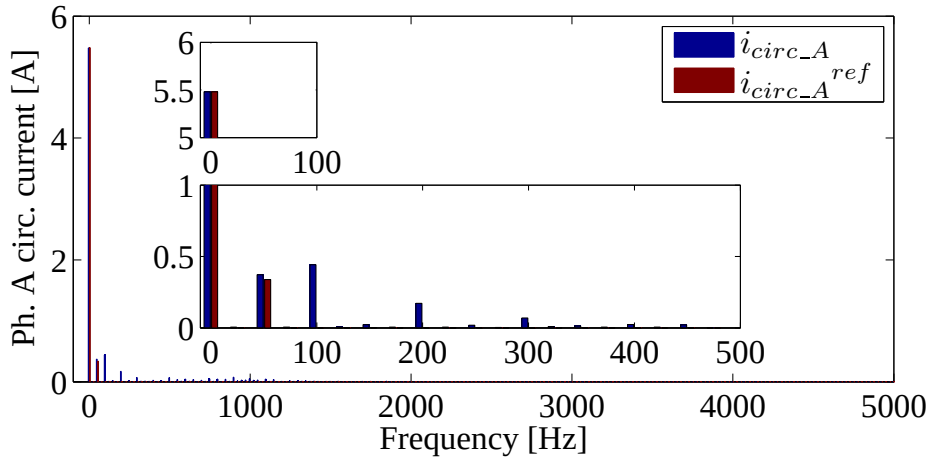


Figure 8.28: Spectrum of the circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method two is applied.

The phase A circulating current and its reference in the case of arm balancing method three are shown in Fig. 8.29. The circulating current waveform contains a 50 Hz component and a distortion at 100 Hz.

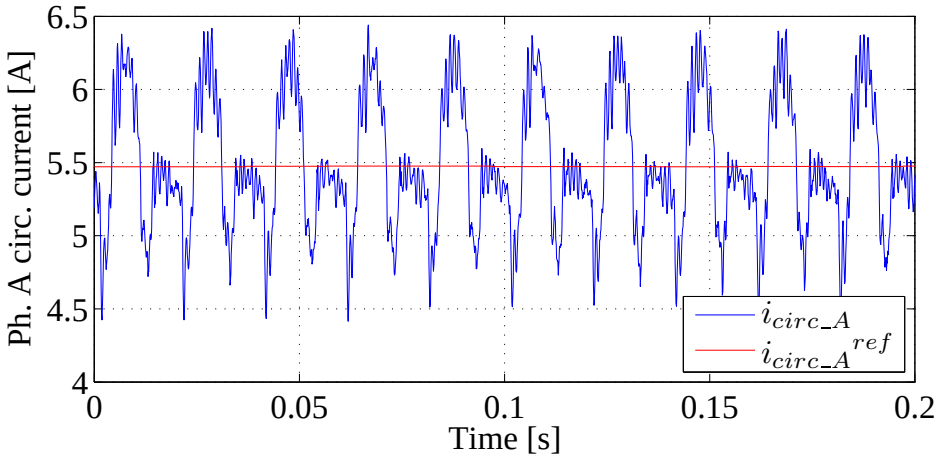


Figure 8.29: Phase A circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method three is applied.

Fig. 8.30 shows the spectrum of the circulating current and its constant reference in the case when method three is applied. The circulating current mean value follows the reference, but there is a 50 Hz component present and the distortion at multiples of 100 Hz. The amount of 50 Hz component is similar to the case of arm balancing controller two, while distortion harmonics have the same amplitude in all three cases.

8.4.2.2 DC voltage controller

The focus of the following subsection is on the verification of the DC voltage controller used to ensure that the average DC voltage follow its reference. When the pulsed load is enabled, the DC current reference is set at 16.5 A as a feed-forward term. The DC voltage controller provides a correction of the DC current reference (Fig. 5.8).

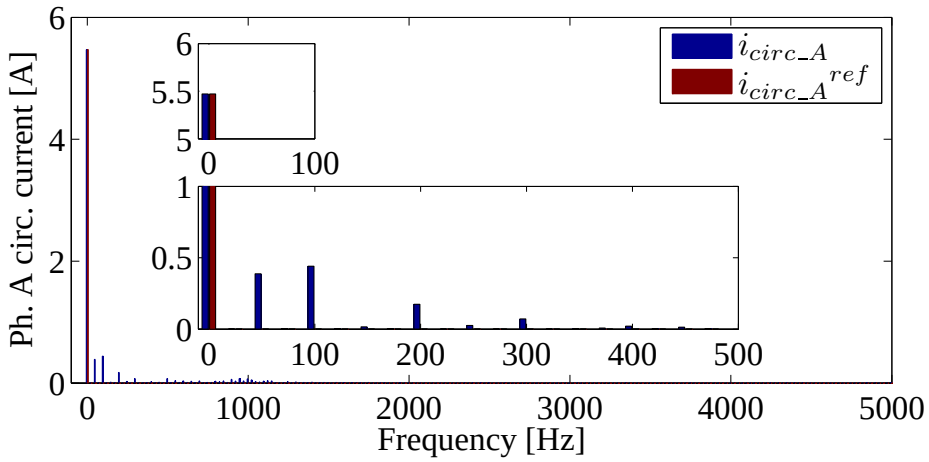


Figure 8.30: Spectrum of the circulating current and its reference under steady state conditions with pulsed DC load when arm balancing method three is applied.

Figs. 8.31 and 8.32 are captured though the HPI interface. Fig. 8.31 presents the error of the average DC voltage value, and the controller output during the transient when pulsed load is enabled. The DC voltage settling time is longer than 1 s due to the slow controller dynamics.

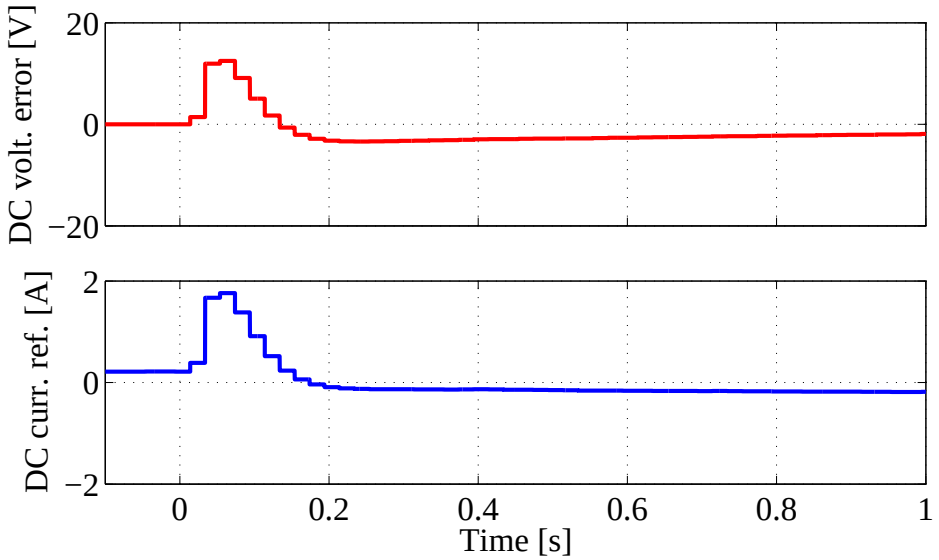


Figure 8.31: DC voltage error and controller output correcting DC current reference during transient when pulsed load is enabled.

The DC voltage and its reference are presented in Fig. 8.32 during the transient when the pulsed load is enabled.

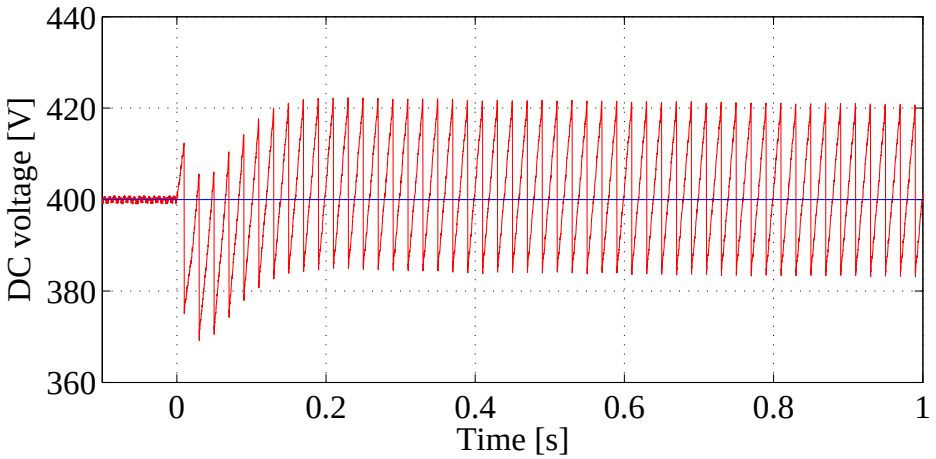


Figure 8.32: Converter DC voltage and its reference during transient when pulsed load is enabled.

8.4.2.3 DC current in the cases of different arm balancing methods

Even if the DC voltage controller provides constant DC current reference, the presence of different amplitudes of 50 Hz component in the circulating currents implies a certain amount of 50 Hz component in the DC current. Depending on the pulse positions and the arm balancing method used, different amplitudes are present (Appendix B). Also the shapes of the DC voltage ripple vary, but this effect is not significant. Figs. 8.33 - 8.35 are based on the DC currents measured by the oscilloscope.

Fig. 8.33 presents the DC currents under steady state conditions for two different pulse positions in the case when method one is applied. In the case of method one, the DC current has a different amplitude depending on the pulse position, therefore in addition to the pulse position of 0.534 rad in which the DC current reference is nearly constant, the pulse position of 0.88 rad is presented since it is closer to the critical region. The second pulse position features significantly higher DC current amplitude meaning higher DC power fluctuation.

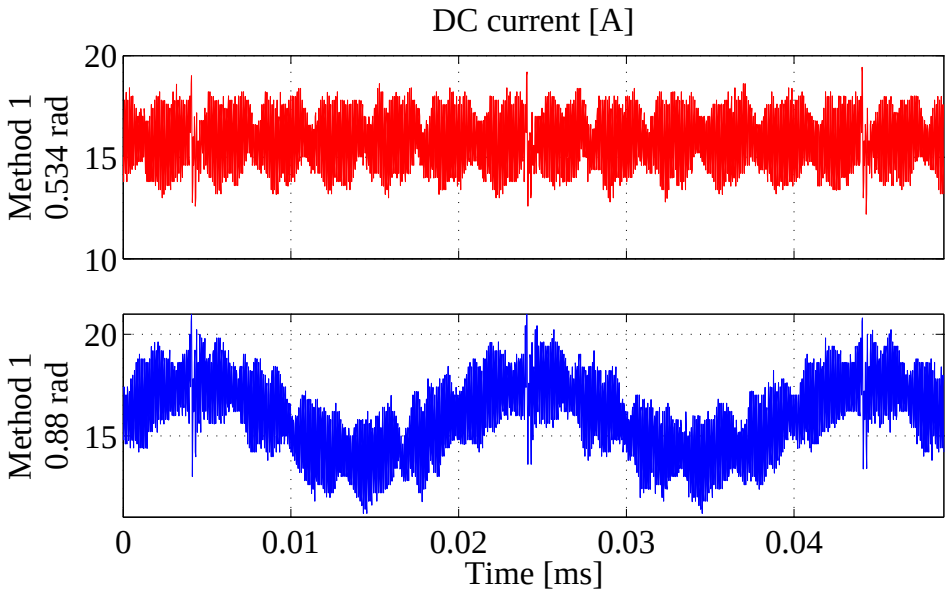


Figure 8.33: DC currents under steady state conditions with pulsed load for pulse positions of 0.534 rad and 0.88 rad when arm balacing method one is applied.

Fig. 8.34 presents the DC currents under steady state conditions for arm balancing methods two and three and the pulse position of 0.534 rad. As expected the performance of the two controllers is similar, having a certain amount of 50 Hz component in the DC current ripple. Those two methods feature the same amplitude of the DC current ripple for all possible pulse positions.

Fig. 8.35 shows harmonic spectrum of four different DC currents addressed in Figs. 8.33 and 8.34. The amount of 50 Hz ripple is the lowest in the case of method one and pulse position of 0.534 rad. If the pulse can be set with respect to the grid voltages (which was done in this experiment), it can be positioned so that the DC current has no 50 Hz component when method one is applied. Methods two and three would have a 50 Hz component of approximately 0.6 A which corresponds to 4 % of the nominal value. This amplitude would be more or less the same regardless the pulse position. Method one for the pulse position of 0.88 rad induces a 50 Hz component of 1.9 A which corresponds to 12 % of the fundamental.

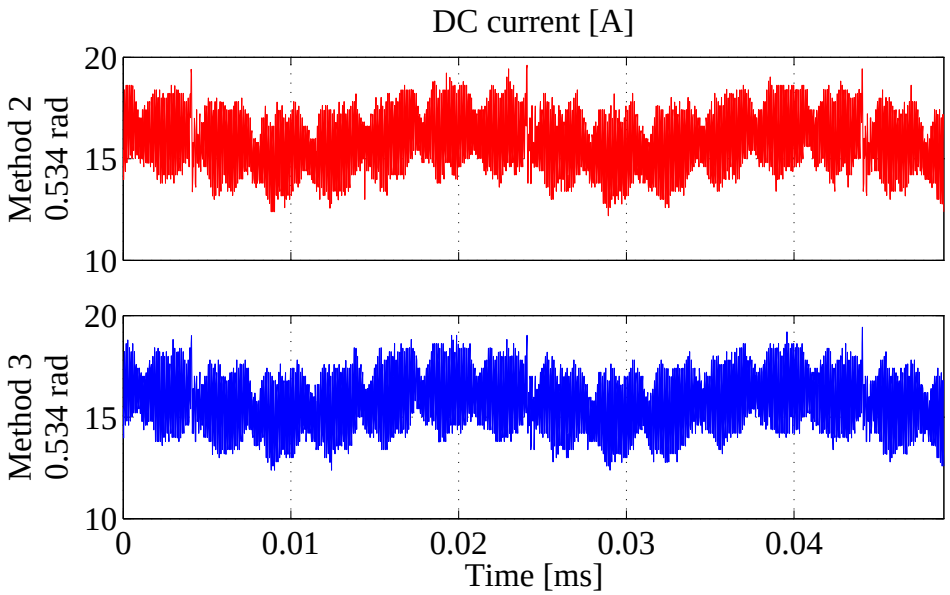


Figure 8.34: DC currents under steady state conditions with pulsed load (pulse position is 0.534 rad) for arm balancing methods two and three.

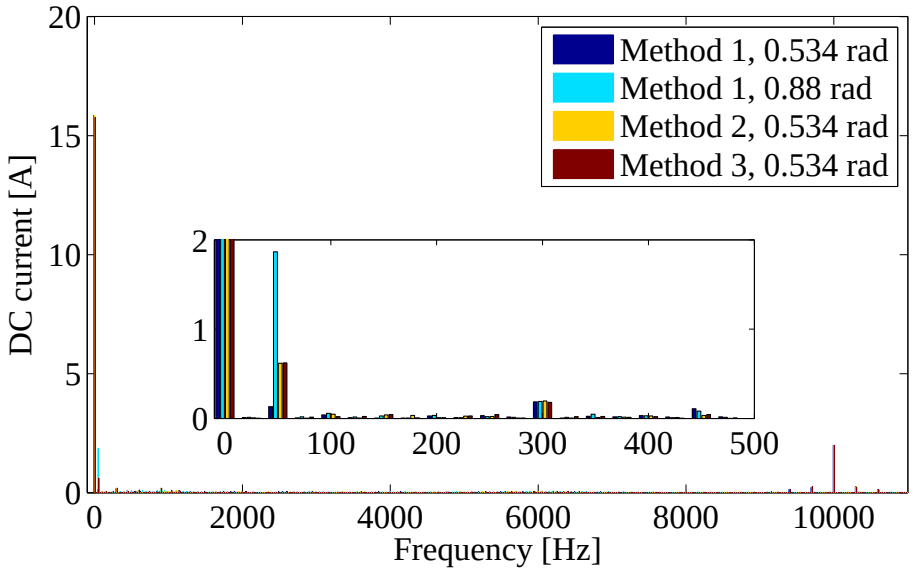


Figure 8.35: DC current harmonics comparison for different arm balancing methods.

The switching harmonics at 10 kHz are visible in the DC current spectrum, since the filtering inductance is significantly smaller than the equivalent inductance at the AC

side, and also because of $(2 \cdot N + 1)$ modulation [85]. This means that the DC power fluctuation obtained by the HPI will be lower than in reality, due to the neglected switching harmonics.

8.4.2.4 Phase balancing

This loop behaves the same regardless the type of arm balancing controller used. Therefore, the results are presented only for the case of arm balancing method one. Figs. 8.36 and 8.37 are captured by the HPI interface. Fig. 8.36 presents error of the sum of all cell capacitor voltages within converter phase A and a small DC offset used to correct circulating current reference (Fig. 5.10) during the transient when the pulsed load is enabled. The voltage error of one phase is the difference between the sum of all cell capacitors of that phase and the average value of this sum for all three phases.

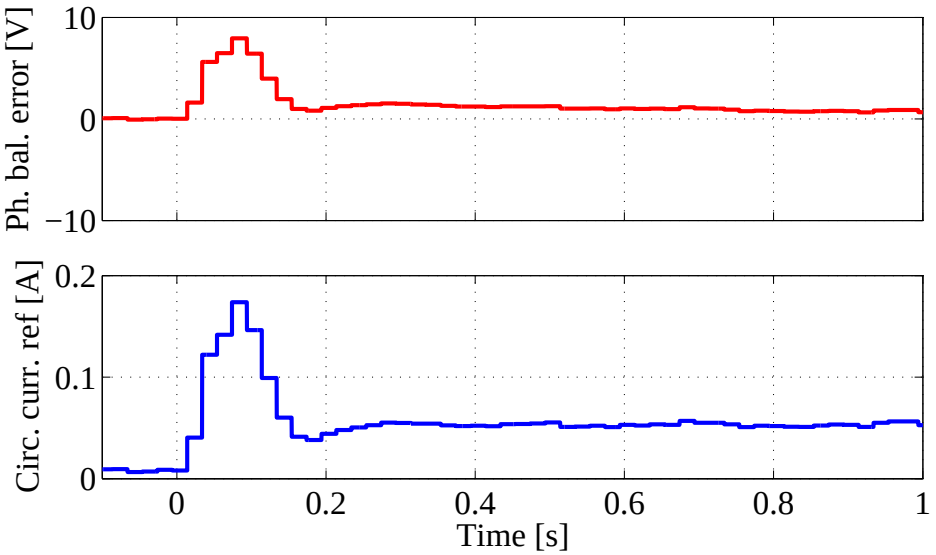


Figure 8.36: Phase balancing error and controller output correcting phase A circulating current reference during transient when pulsed load is enabled.

The sum of all cell capacitors, its average value over 20 ms and its reference during

transient is presented in Fig. 8.37.

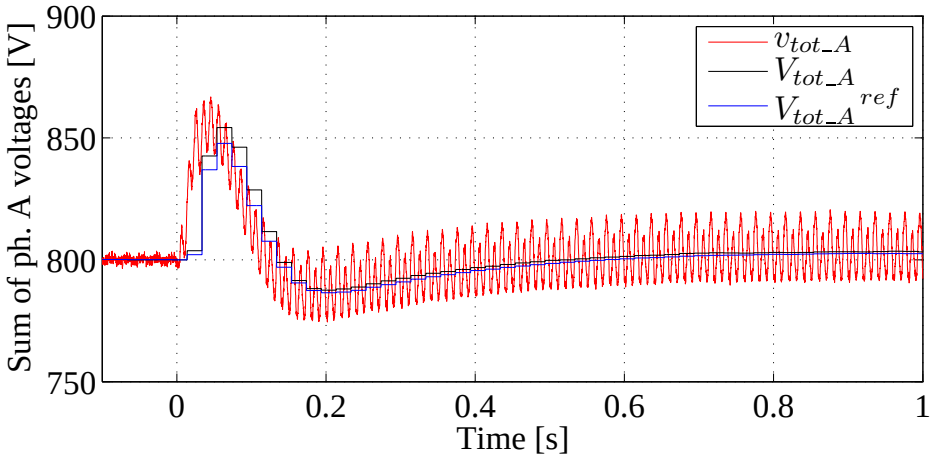


Figure 8.37: Sum of the phase A cell capacitor voltages, average value and a reference during transient when pulsed load is enabled.

8.4.2.5 Arm balancing

Due to internal converter imbalances, such as unequal cell capacitors, arm inductors, semiconductors characteristics and also measurements inaccuracy, arm balancing is necessary even if converter is under no-load or resistive load conditions. In ideal environments, such as those emulated by simulations, the imbalance between arms exists only if there is a constant source of imbalances, such as the pulsed DC load. In simulations, a small imbalance might be present during transients, but the divergence of capacitor voltages of the two arms of the same phase does not persist after the transient. However, in the experiments, if arm balancing is not applied, the cell capacitor voltages of two arms keep diverging until overmodulation of one arm happens and system reaches a new equilibrium.

In the conditions before pulsed load is enabled, the arm balancing methods two and three can be used. The arm balancing method one is applicable only to pulsed load condition, i.e. a condition in which the DC voltage ripple has a 50 Hz component. Therefore, when the method one was examined, the method two was applied before

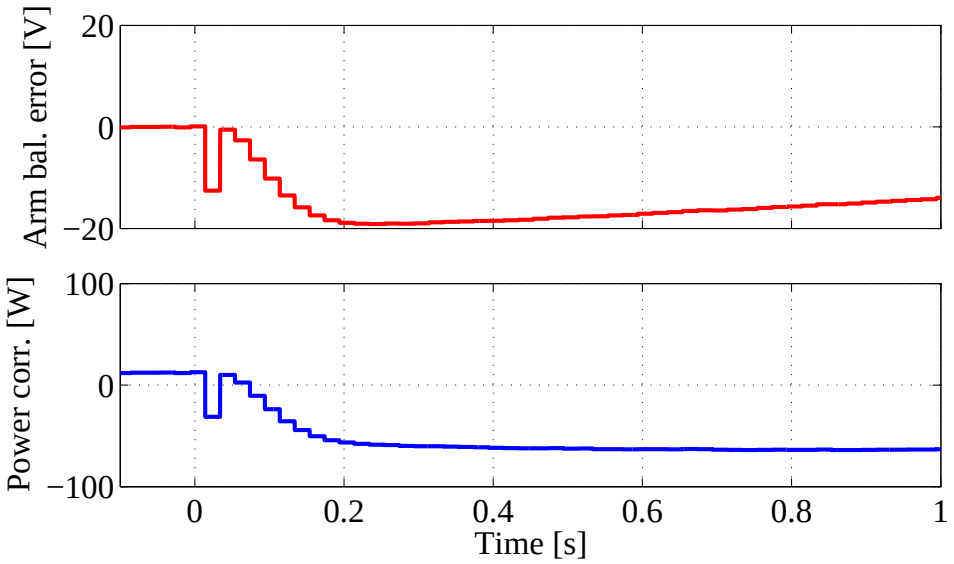


Figure 8.38: Arm balancing error and controller output being balancing power between arms of phase A during transient when pulsed load is enabled.

the pulse, while method one is applied during the pulse.

The following figures are captured through the HPI interface, with an aim to validate the performance of arm balancing controllers. Fig. 8.38 presents the difference in sum of cell capacitors of phase A upper and lower arms, and a power correction used to balance those arms. The figure is related to the transient when the pulsed load is enabled. Fig. 8.38 shows that a certain amount of power imbalance exist before pulsed load is enabled, as a consequence of internal converter sources of imbalances.

Fig. 8.39 shows the sum of cell capacitor voltages of phase A upper and lower arm under steady state conditions in the case of arm balancing method one. The arms are perfectly balanced, but the cell capacitor voltages ripple is not the same due to the 50 Hz in the circulating current, causing different arm current amplitudes.

Under state conditions the arm balancing controller compensates for a certain amount of power imbalance in every phase. The compensated powers are -62.2 W, -3.563 W and 82.16 W, for phases A, B and C, respectively. This amount of power imbalance

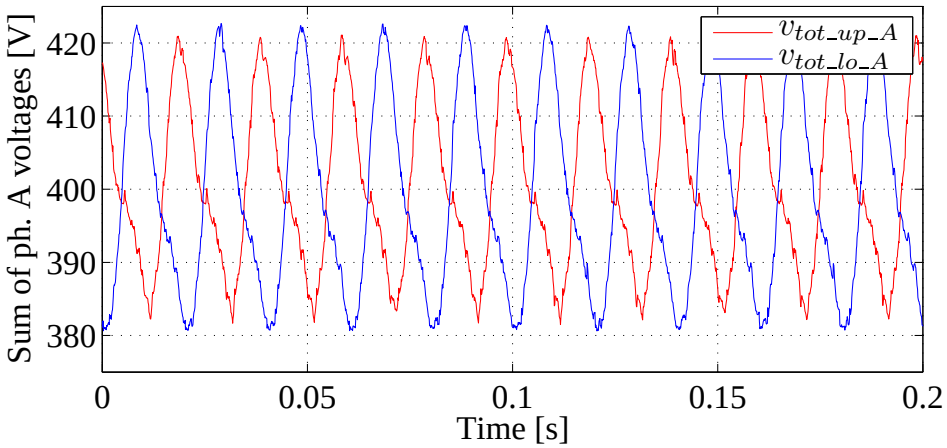


Figure 8.39: Sum of the phase A upper arm and lower arm cell capacitor voltages under steady state conditions when method one is applied.

is mainly a consequence of the pulsed load. However, a certain amount of it can be associated to the internal imbalance being present without pulsed load.

The circulating current 50 Hz component references under steady state conditions when arm balancing method one is applied are shown in Fig. 8.40. The references of all three phases are in phase or in counter phase which is the characteristics of method one. For this pulse position the sum of the three references is close to zero, meaning constant DC current reference.

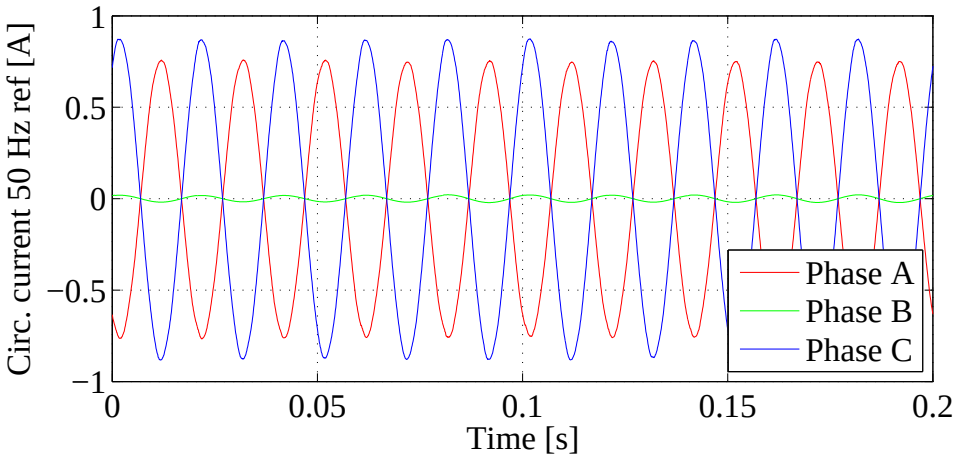


Figure 8.40: Circulating current reference 50 Hz component used for arm balancing under steady state conditions when method one is applied.

Fig. 8.41 presents the sum of cell capacitor voltages of phase A upper and lower arm under steady state conditions in the case of arm balancing method two.

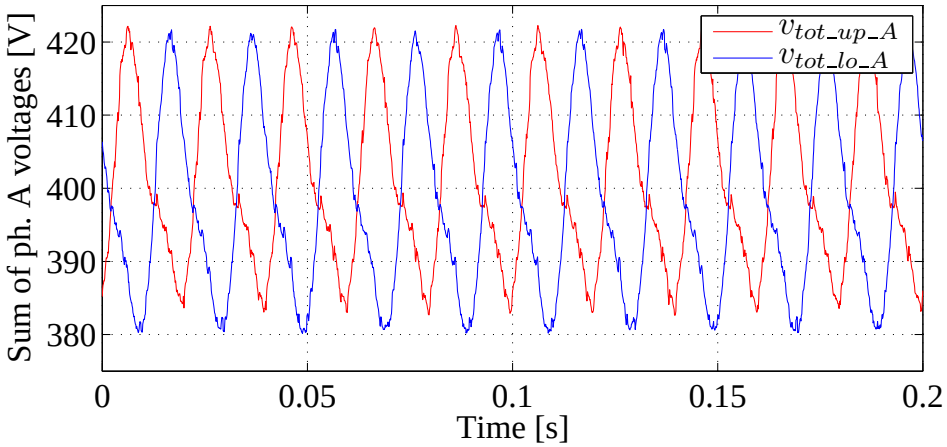


Figure 8.41: Sum of the phase A upper arm and lower arm cell capacitor voltages under steady state conditions when method two is applied.

Since the pulse position is the same as in the case when method one is applied, it is expected that arm balancing controller compensates for the same imbalance powers.

The expected variation is in the variation of internal imbalance present before the pulsed load was enabled. The compensated powers in this case are -63.8 W, -5.5 W and 82 W from phases A, B and C, respectively. However, the circulating current references are different with respect to arm balancing method one. Fig. 8.42 presents the phases A, B and C circulating current reference 50 Hz component, under steady state conditions when method two is applied. The references of phases A and B are in counter phase with their AC voltage references while phase C is in phase with corresponding AC voltage reference.

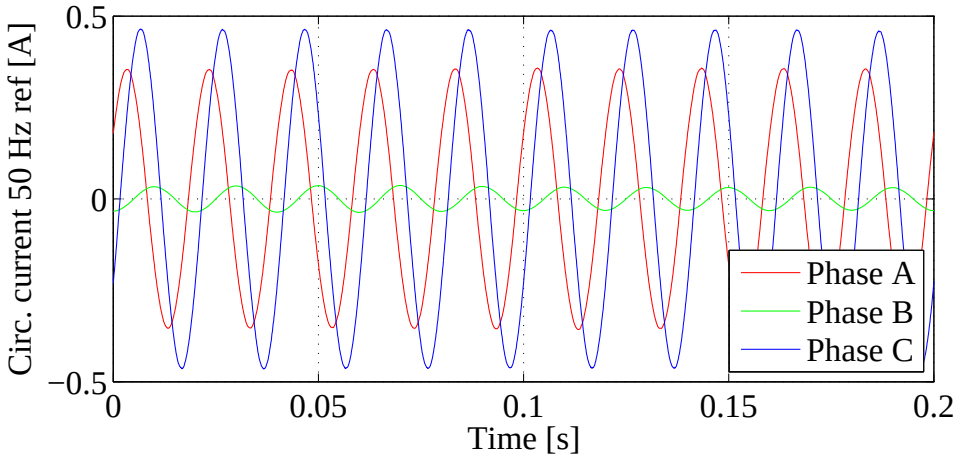


Figure 8.42: Circulating current reference 50 Hz component used for arm balancing under steady state conditions when method two is applied.

Fig. 8.43 presents the sum of cell capacitor voltages of phase A upper and lower arm under steady state conditions in the case of arm balancing method three.

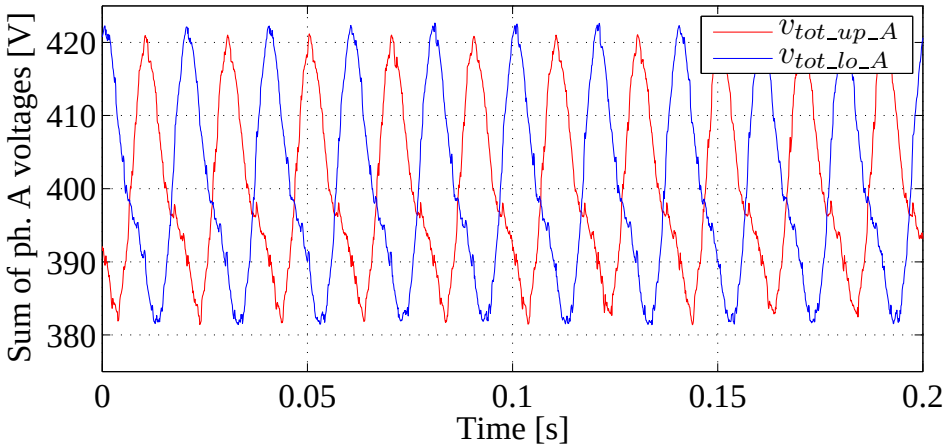


Figure 8.43: Sum of the phase A upper arm and lower arm cell capacitor voltages under steady state conditions when method three is applied.

The steady state values of the $x_{A,B,C}$ parameters are presented in Fig. 8.44. For the given pulse position, the AC voltage reference for converter arms in all the phases is adjusted to less than 2 % with respect to the nominal amplitude the AC reference.

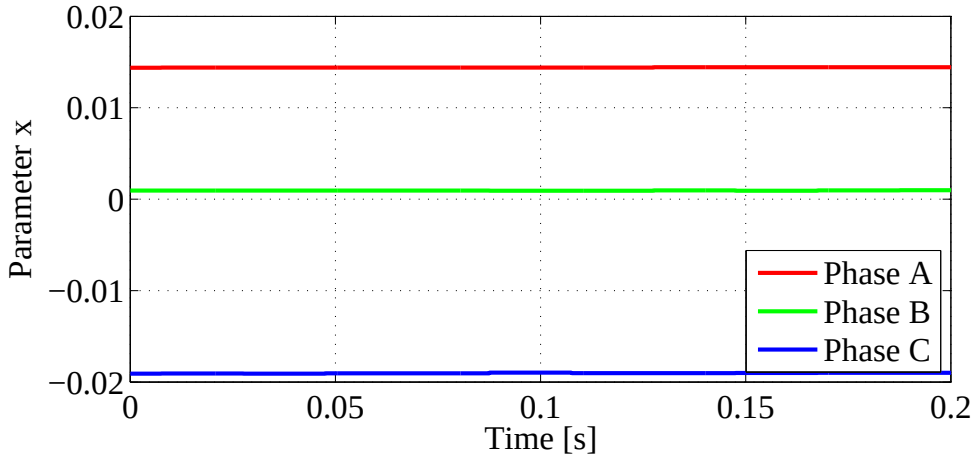


Figure 8.44: Paramter x values used for arm balancing under steady state conditions when method three is applied.

8.4.3 Disabling arm balancing controller

This sections is highlighting the importance of the arm balancing controllers when MMC is operated under pulsed DC load. For the demonstration purpose method one is applied, and then the arm balancing is disabled for 0.4 s, to see the effects on the converter waveforms. Figs. 8.45 - 8.49 represent the HPI captured waveforms before and after the arm balancing controller is disabled and after re-enabling the controller. At 0 s the arm balancing controller is disabled, at 0.4 s it is re-enabled.

Fig. 8.45 shows the behaviour of cell capacitor voltages of converter arms under steady state conditions, after disabling the arm balancing controller, and after re-enabling the arm balancing controller. The sum of cell capacitor voltages in each of the converter arms is presented. Before 0 s all converters arms are perfectly balanced. At 0 s the arm balancing is disabled, and the cell voltages of converters arms of the same phase start diverging. The pulse position of 0.534 rad affects the most phases A and C while phase B is not significantly affected. At 0.4 s the arm balancing is re-enabling and the cell capacitor voltages of two arms of the same phase start re-converging.

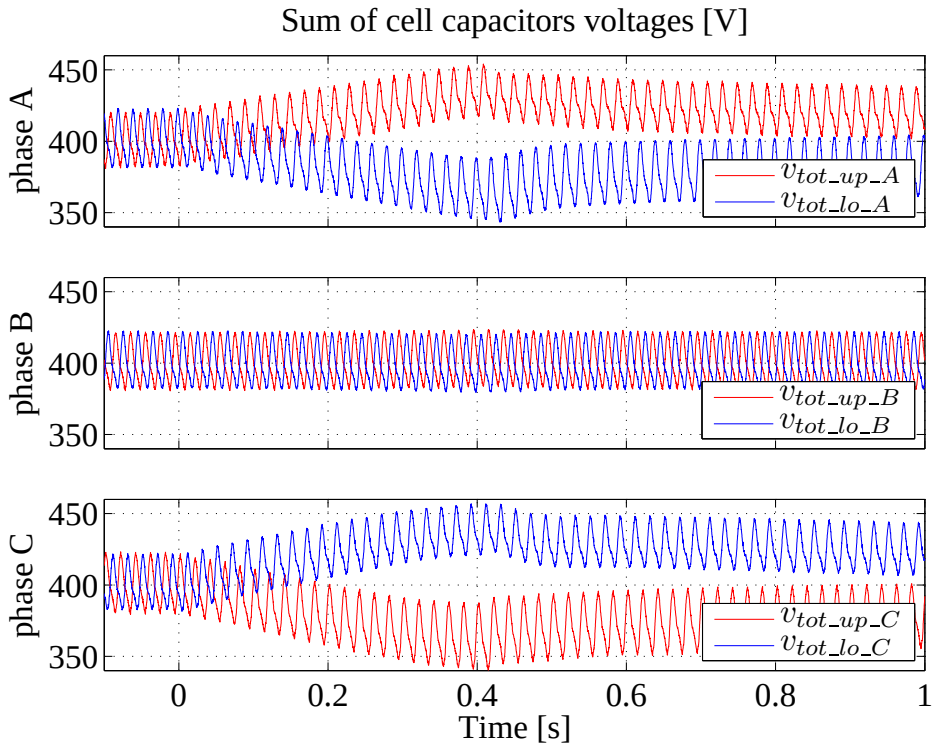


Figure 8.45: Sum of the upper arm and lower arm cell capacitor voltages when disabling and re-enabling of arm balancing controller is done.

Fig. 8.46 presents phase d, q currents and their references in steady state, after disabling arm balancing controller and after re-enabling arm balancing controller. The d, q currents do not have increased ripple until the overmodulation of the arm with lower cell capacitor voltages happen. The overmodulation starts happening around 0.35 s and effects of it increase as cell capacitor voltages diverge. The d, q axis current ripple decreases only after re-enabling arm balancing controller. Once the sum of cell capacitor voltages of particular arms ($v_{tot\_lo\_A}$ and $v_{tot\_up\_C}$) is above the reference signal, d, q axis current ripple is reduced to its steady state value (at approximately 0.48 s).

The ripple in d, q axis currents directly affects AC power fluctuation. The AC power and its reference are presented in Fig. 8.47 in steady state, after disabling arm

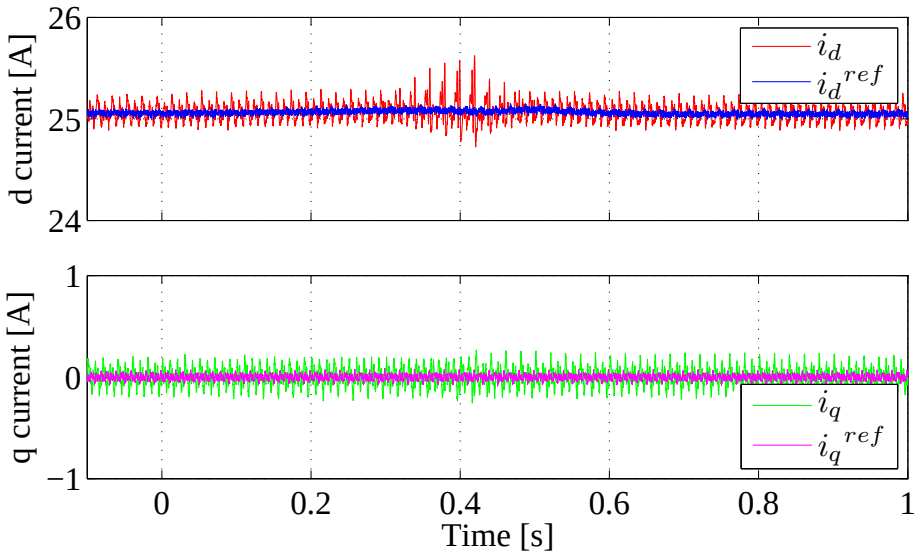


Figure 8.46: Phase/grid d, q currents when disabling and re-enabling of arm balancing controller is done.

balancing controller and after re-enabling arm balancing controller. The AC power has increased fluctuation when overmodulation occurs in any of the converter arms, which corresponds to time 0.35 s - 0.45 s. AC power fluctuation is increased from approximately 100 W in steady state to about 250 W during overmodulation. The increased power fluctuation correspond to 3.5 % which is far beyond the specification.

Fig. 8.48 presents phase A circulating current and its reference under steady state conditions, after disabling and re-enabling the arm balancing controller one. When the arm balancing controller is disabled, the circulating current has no 50 Hz component, but the 100 Hz distortion is present.

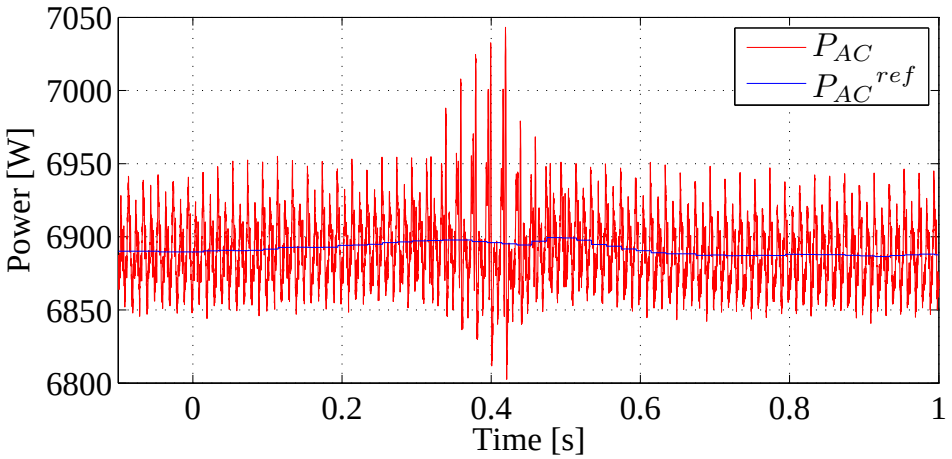


Figure 8.47: AC power and its reference when disabling and re-enabling of arm balancing controller is done.

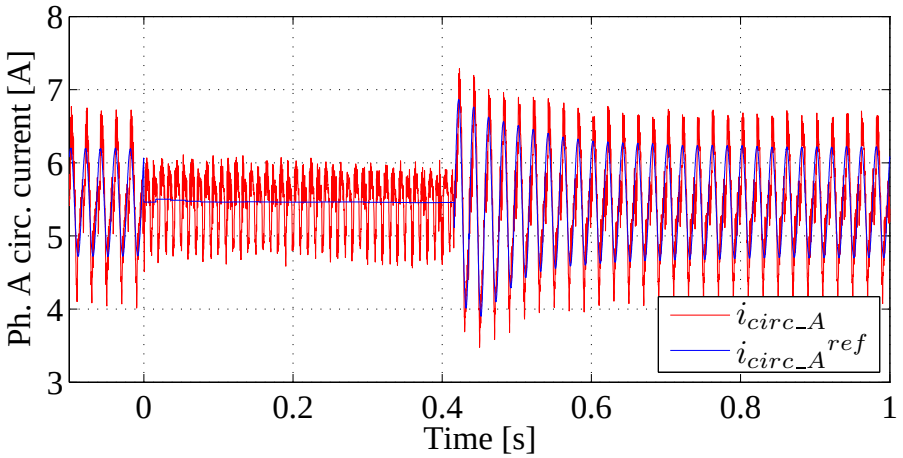


Figure 8.48: Phase A circulating current when disabling and re-enabling of arm balancing controller is done.

Fig. 8.49 shows circulating currents 50 Hz component references under steady state conditions, after disabling and re-enabling the arm balancing controller one. When the arm balancing controller is disabled, the circulating current references have zero 50 Hz component.

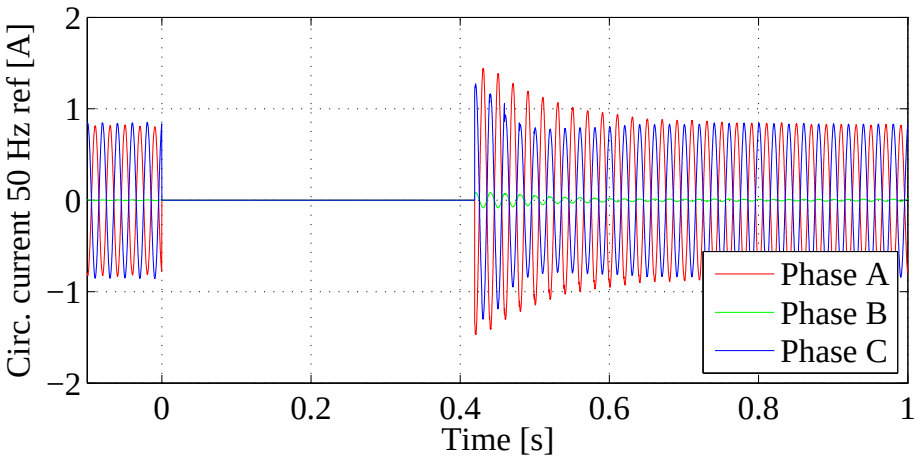


Figure 8.49: Circulating currents 50 Hz component references (in the case of arm balancing method one) when disabling and re-enabling of arm balancing controller is done.

The following figures show the consequences of overmodulation on the phase currents and active power. Namely, the arm balancing controller was disabled for longer period, and it has been observed that after 0.4 s phases A and C reach a new equilibrium where cell capacitors stop diverging (the overmodulation in phase B happens later). Therefore, it was possible to record phase currents by the oscilloscope under new steady state conditions of phases A and C as a consequence of overmodulation. The phase currents waveforms are presented in Fig. 8.50.

The harmonic spectrum (Fig. 8.51) is more polluted with the low frequency harmonics, similarly to the case in Fig. 6.42.

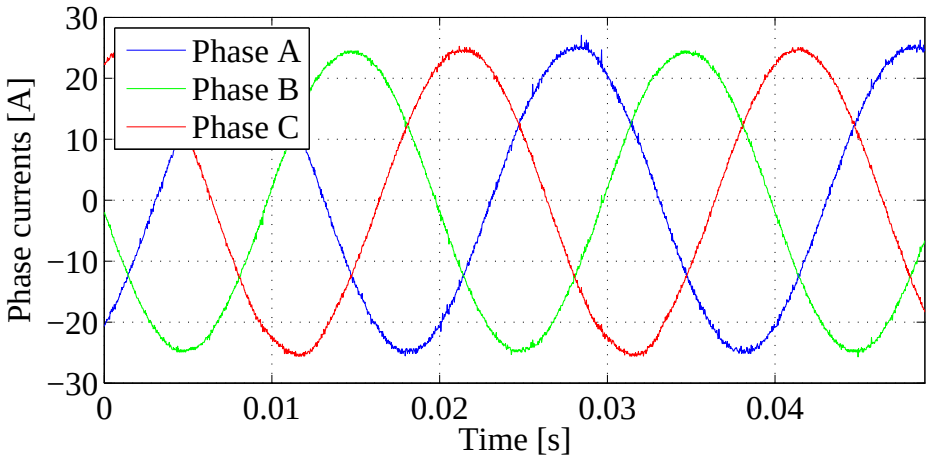


Figure 8.50: Phase/grid currents of the converter with pulsed DC load, when arm balancing is disabled.

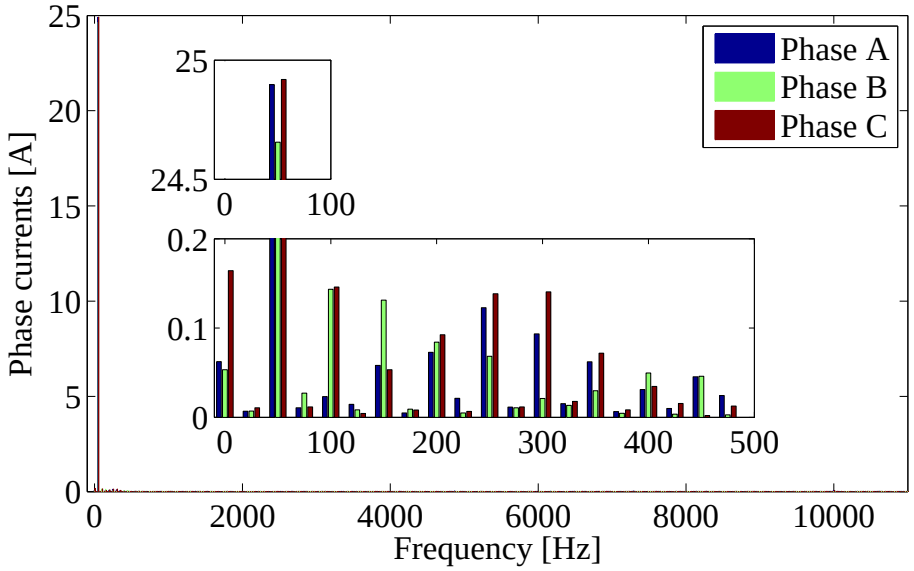


Figure 8.51: Phase/grid currents spectrum of the converter with pulsed DC load when arm balancing is disabled.

Figs. 8.52 and 8.53 are generated from the HPI captured waveforms. Grid active power and its reference, while some of converter arms are overmodulated, is presented in Fig. 8.52.

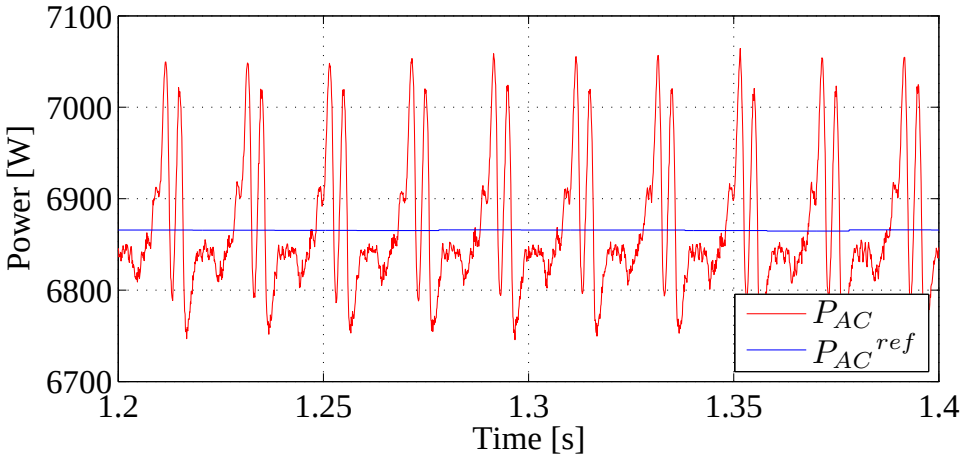


Figure 8.52: Grid active power and its reference, under steady state conditions with pulsed load when arm balancing is disabled.

The AC power harmonics are presented in Fig. 8.53. When compared to the spectrum from Fig. 8.13, significantly higher amplitudes of low frequiency components is present. The power spectrum is very similar to the one obtained by simulation (Fig. 6.43) with the low frequency components starting at 50 Hz.

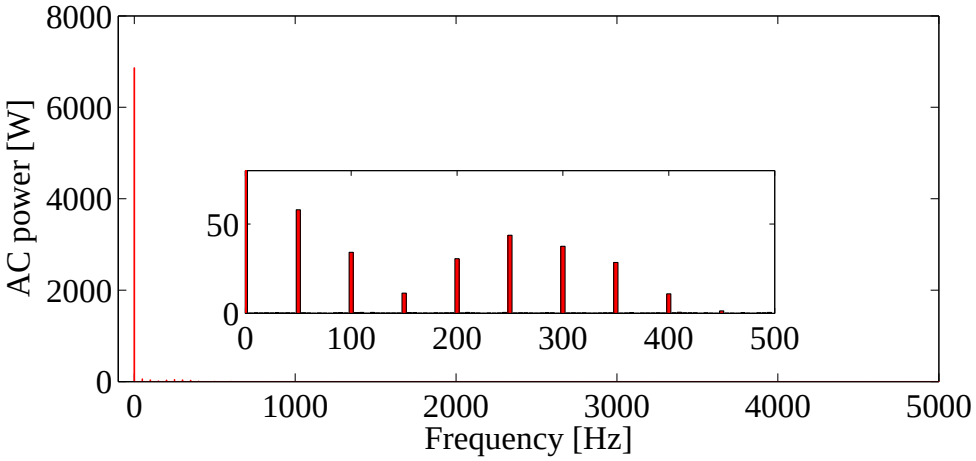


Figure 8.53: Grid active power harmonics, under steady state conditions with pulsed load when arm balancing is disabled.

8.4.4 General converter waveforms

This subsection relates to the converter inner and outer waveforms to prove the correct operation of the converter. Figs. 8.54 - 8.56 are captured by the HPI interface and relate to the converter inner signals.

The modulation algorithm (Fig. 4.4) is responsible for balancing of the cell capacitors inside an arm. All cell capacitor voltages of phase A are presented in Fig. 8.54. All cell capacitors of both upper and lower arms are perfectly balanced, and regulated at mean voltage level of 100 V. The amplitudes of upper and lower arm cell capacitor voltages are not equal due to different amplitude of arm currents as a consequence of 50 Hz component in the circulating current.

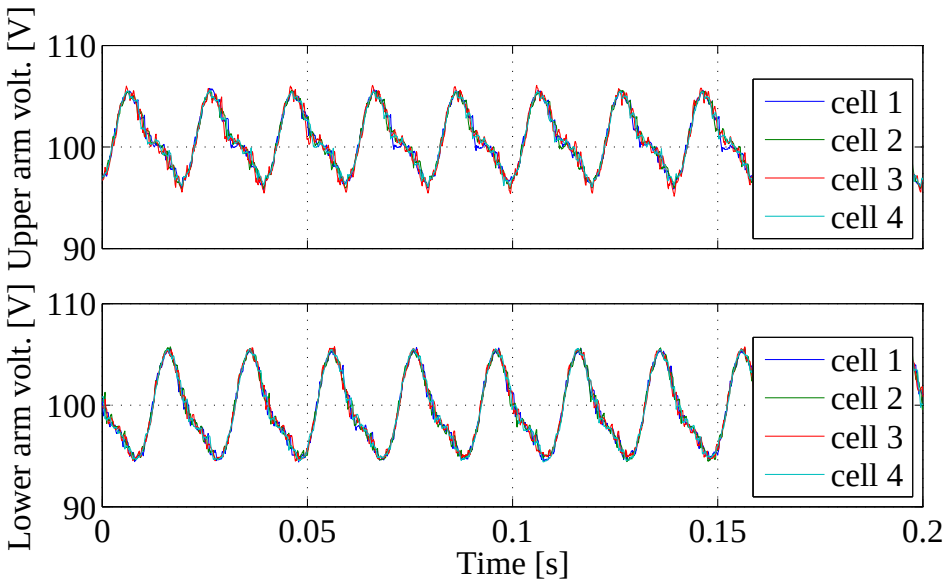


Figure 8.54: Phase A cell capacitor voltages under steady state conditions.

The phase A arm currents and the circulating current under steady state conditions with pulsed load when arm balancing method one is applied are presented in Fig. 8.55. The distortion present in the circulating current, is not obvious in the arm currents waveforms. The reason for this distortion might be a zero crossing of arm currents, when a current sign decides the switching algorithm and commutation devices during

deadtime. Another reason might be rounding of the insertion indices.

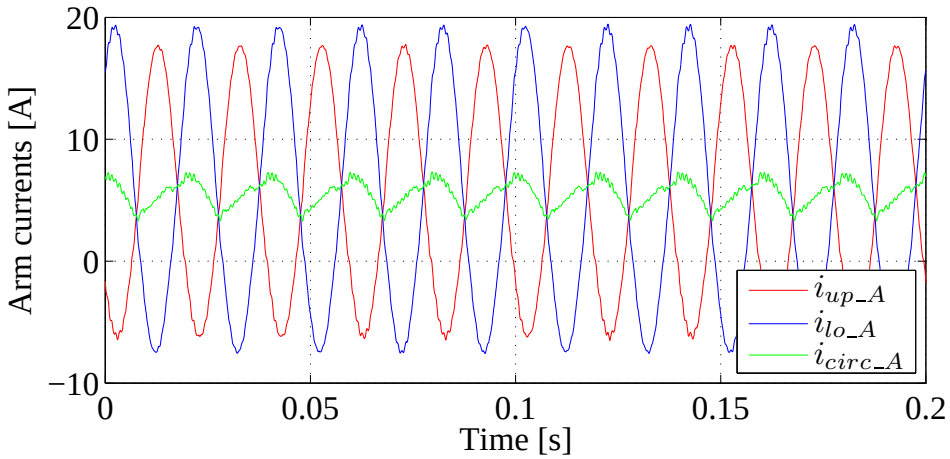


Figure 8.55: Phase A arm currents and circulating current under steady state conditions when arm balancing method one is applied.

The modulation signals, i.e. insertion indices of phase A upper and lower arm are presented in Fig. 8.56.

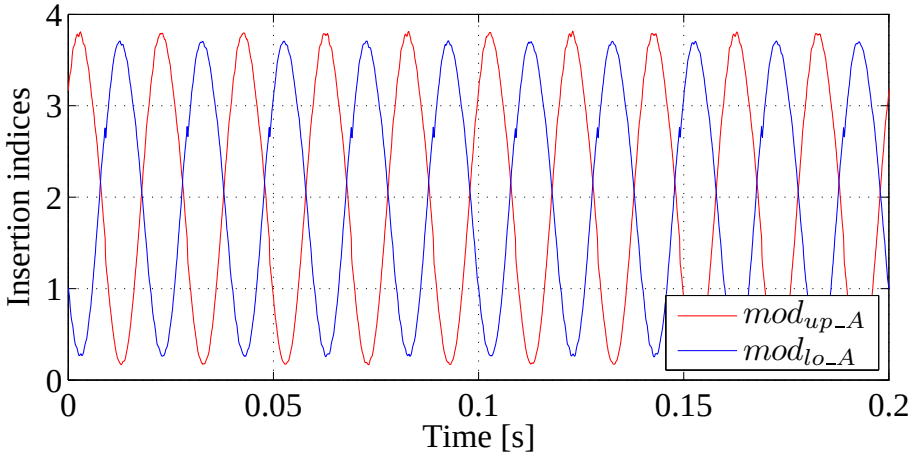


Figure 8.56: Phase A upper and lower arm insertion indices under steady state conditions when arm balancing method one is applied.

Converter phase voltages, measured from the converter AC terminals to the AC source

neutral, under steady state conditions with pulsed DC load are presented in Fig. 8.57.

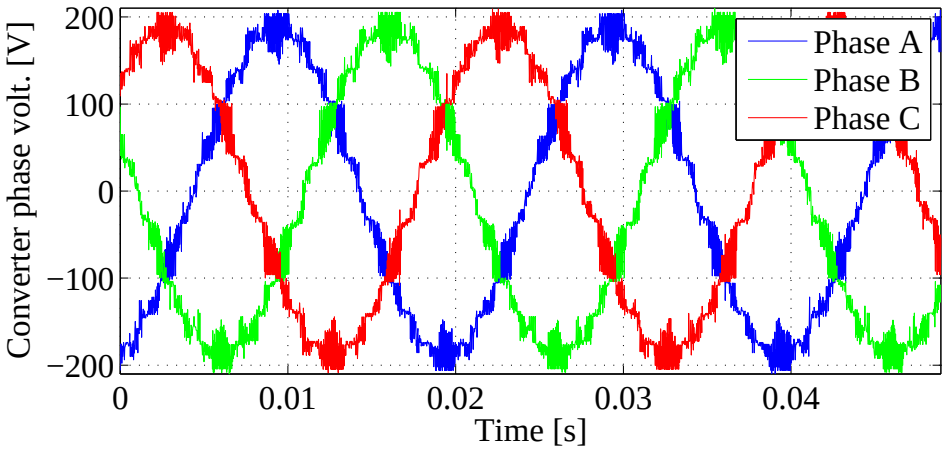


Figure 8.57: Phase voltages under steady state conditions with pulsed DC load, when arm balancing method one is applied.

The spectrum from Fig. 8.58 corresponds to the converter phase voltages from Fig. 8.57. Low frequency harmonics are present (those are present in phase current) and the most dominant is at 350 Hz with the amplitude below 1.5 % of the fundamental. Also in the area around 10 kHz the switching harmonics can be observed. Those harmonics are completely filtered in phase currents.

Fig. 8.59 shows phase A grid and converter voltage together with the phase current. As it is shown the converter voltage lags the grid voltage, while grid voltage and current seem to be perfectly aligned.

Based on the fundamental components of the waveforms from Fig. 8.59 phase shifts between each of them can be determined. If a fundamental of the grid voltage has a phase angle 0 rad, the phase angles of the converter voltage and phase current are -0.1886 rad and -0.0069 rad, respectively. This phase shift between the grid voltage and current corresponds to power factor of 0.99998.

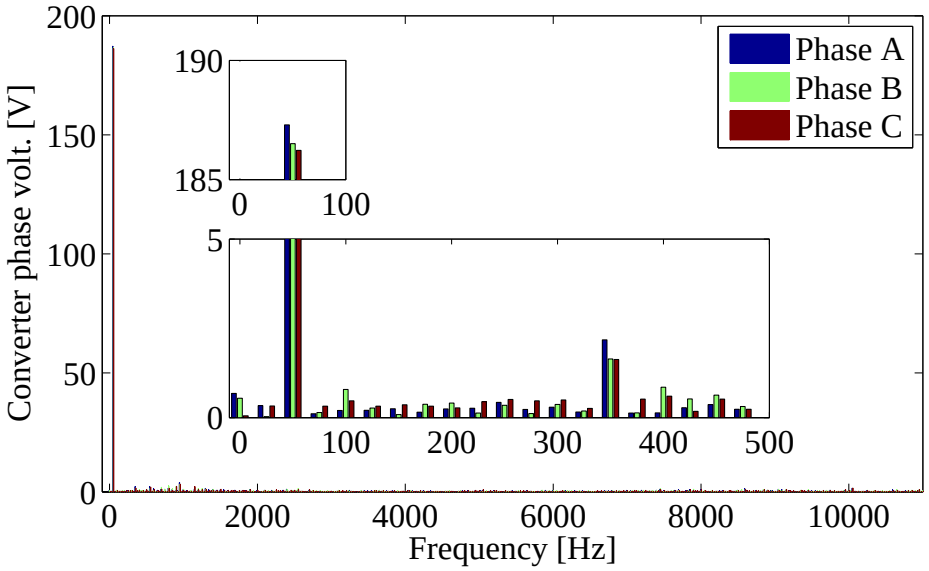


Figure 8.58: Phase voltages spectrum under steady state conditions with pulsed DC load, when arm balancing method one is applied.

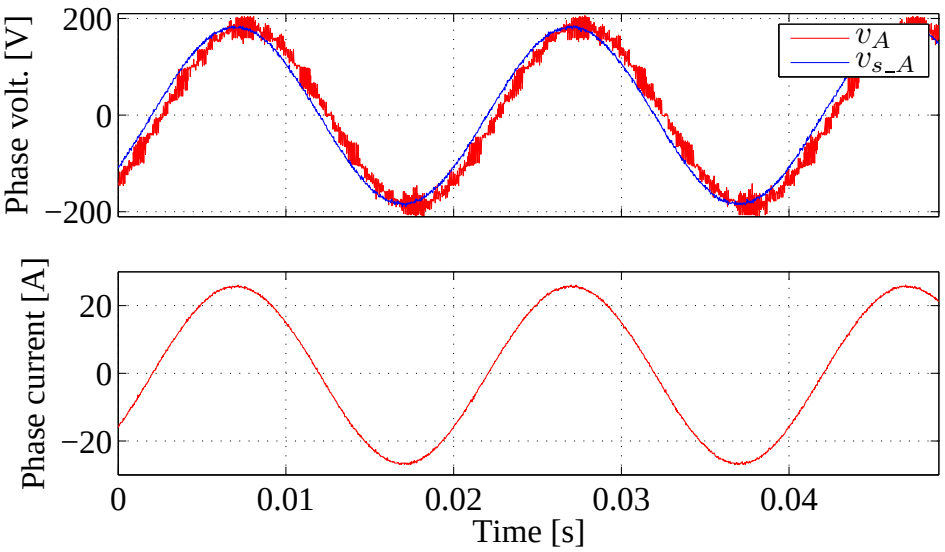


Figure 8.59: Phase voltages under steady state conditions with pulsed DC load, when arm balancing method one is applied.

8.5 Performance of the control system for different pulse positions

This section is focused on evaluating controller performance for different pulse positions. The pulse positions between phase A and phase B positive gradient zero crossing, which corresponds to one third of grid period, were analysed. A step in pulse positions used in this analysis is 0.09425 rad. The similar behaviour is expected for the pulse positions outside the observed region. However, some variance is expected due to the internal imbalances caused by the unsymmetrical converter arms. The internal imbalance sometimes acts to reduce the pulsed load effects, for instance when the pulse position is such that the upper arm gets more power than the lower arm (of a specific phase), and the internal imbalance puts more power in the lower arm than the upper. Having the pulse position exactly π rad apart from that position, would mean that the internal imbalance adds up with the imbalance caused by the pulsed load. At that position, both internal imbalance and pulsed load imbalance would add up and induce more power in the lower arm. Therefore, rather than having the same amplitudes of circulating current at those two positions, somewhat higher amplitude is expected in the second case. Internal imbalance is not dependent on the pulse position but it varies with temperature causing different before pulse conditions for different experiments.

The pulse position effects are examined for three arm balancing methods, in order to evaluate the achieved power fluctuation and parameters used for arm balancing (circulating current 50 Hz component and x parameter values).

All of the results presented in this section are derived from the HPI captured waveforms.

8.5.1 Arm balancing method one

The arm balancing method one corresponds to the analytical solution for the circulating current reference, presented in section 5.6. This method is characterised with the six critical regions for pulse positions in a grid voltages period, while each phase has two critical regions. As the pulse position approaches the critical region, the 50 Hz component of the amplitude of the circulating current reference of that phase increases (amplitude of the arm currents increases). Due to the arm inductors peak current limitaiton, a circulating current amplitude is limited to 3 A. This made the critical region wider, since at all the pulse positions demanding higher circulating current reference, the arm balancing wasn't possible. Hense, the presented results relate only to pulse positions in which safe converter operation was possible and the circulating current amplitude is limited to 3 A.

Fig. 8.60 shows the amplitudes of circulating currents 50 Hz component vs. the pulse position. The amplitude here can be negative if the same phase angle is assumed for all the phases. An alternative would be having a phase angle shifted by π and positive amplitude. The critical region for the phase C is in the middle of the observed region, i.e. around $\frac{\pi}{3}$ rad, while the critical region for the phases A and B are around 0 rad and $\frac{2\pi}{3}$ rad, respectively. The presented results match the results obtained by simulation (Fig. 6.50).

The compensated power used to correct arm powers imbalance is presented in Fig. 8.61. To find the amount of compensated power associated with the pulsed load, the balancing power before pulse and during pulse has been recored. Their difference is assumed to be used for balancing the disturbance induced by the pulsed load. The difference in powers should be symmetrical in the regions outside the analysed region and also among phases. At the same time the compensated power during the pulsed load won't be symmetrical since it has an internal imbalance effect.

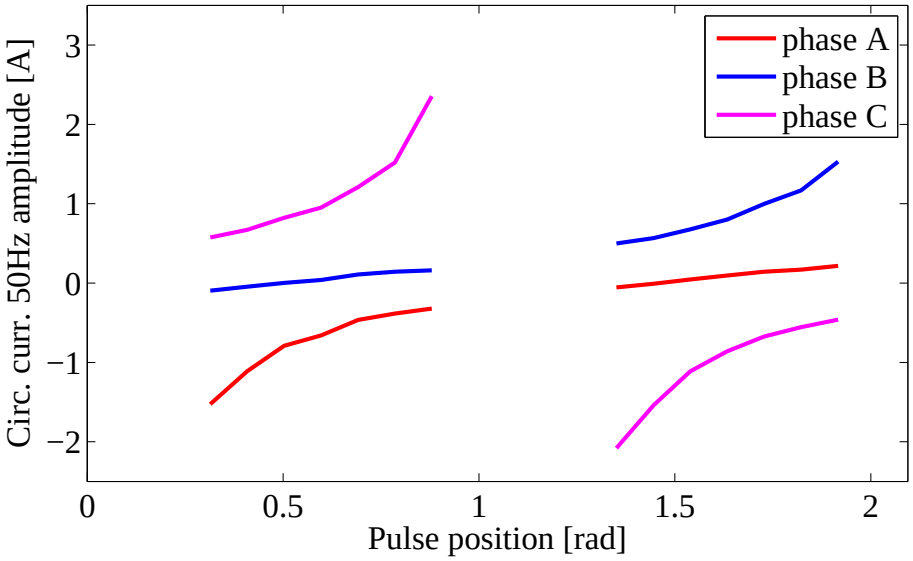


Figure 8.60: Amplitude of the circulating current reference (assuming the phase angle lagging $\frac{\pi}{2}$ rad behind DC voltage ripple) vs. the pulse position.

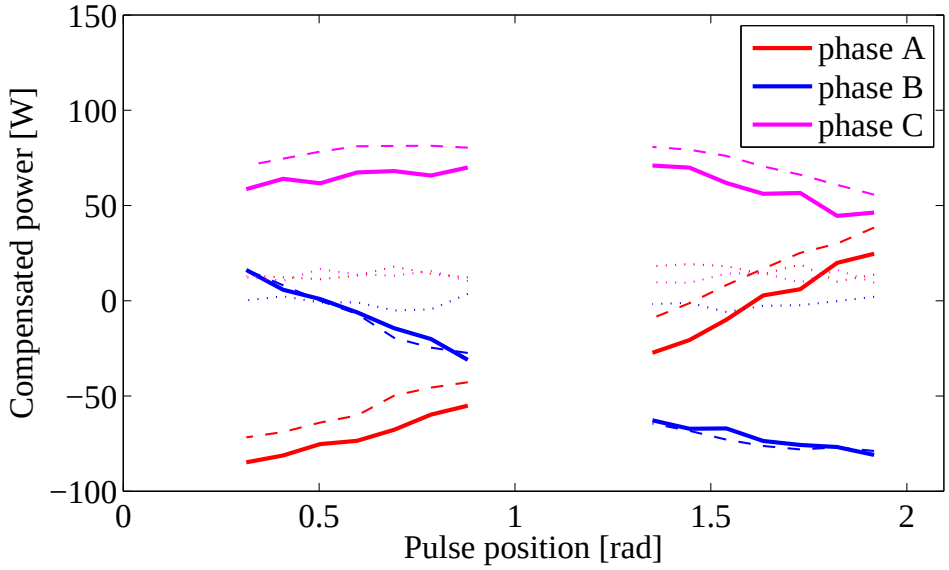


Figure 8.61: Balancing power before pulse (dotted lines), during pulse (dashed lines) and the difference (full line associated with the pulsed load only) vs. the pulse position when the arm balancing method one is used.

It can be seen from Fig. 8.61, that the internal imbalance acts to increase pulsed load caused imbalance in phase C for those pulse positions. At the same time, the internal imbalance reduces the pulsed load imbalance in phases A. The internal imbalance of phase B is fairly low and it does not affect balancing power significantly.

The AC and DC power fluctuation vs. the pulse position are presented in Fig. 8.62. For all analysed pulsed positions, the converter AC power fluctuation is between 1.4 and 1.6 %, while the DC power fluctuation varies from 15 to 40 %. The DC power fluctuation follows the pattern from the simulations (Fig. 6.51), i.e. it increases as the pulse positions are approaching the critical regions.

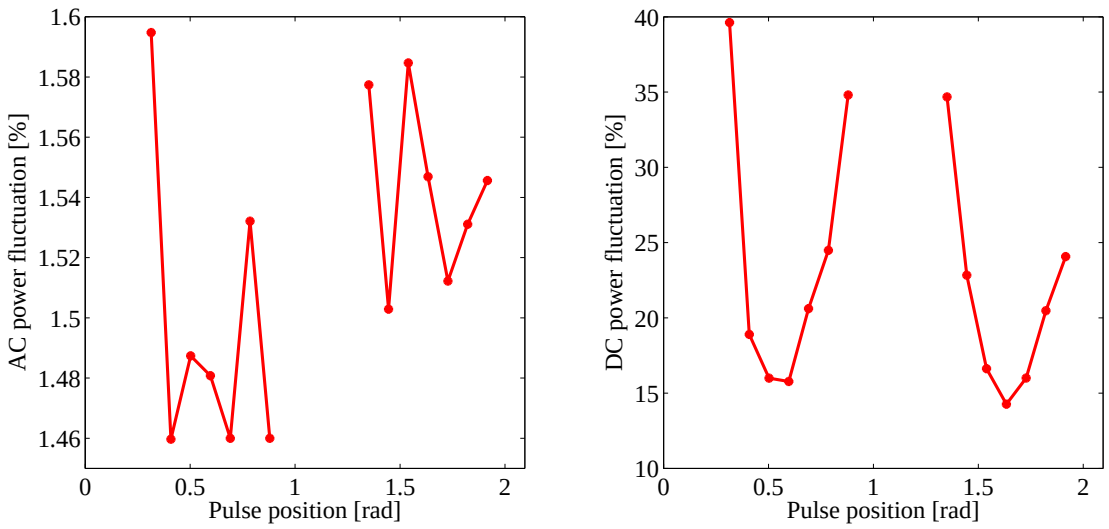


Figure 8.62: AC and DC power fluctuation vs. the pulse position when the arm balancing method one is used.

8.5.2 Arm balancing method two

Arm balancing method two uses the circulating current 50 Hz component aligned (or in counter phase depending on the pulse position) with the AC voltage reference.

Since this method can be applied for all pulse positions, the whole region of one third of the fundamental period is covered.

Fig. 8.63 shows the amplitudes of circulating currents 50 Hz component vs. the pulse position. The amplitude here can be negative if the phase angle is assumed to be the same as the angle of that phase AC reference.

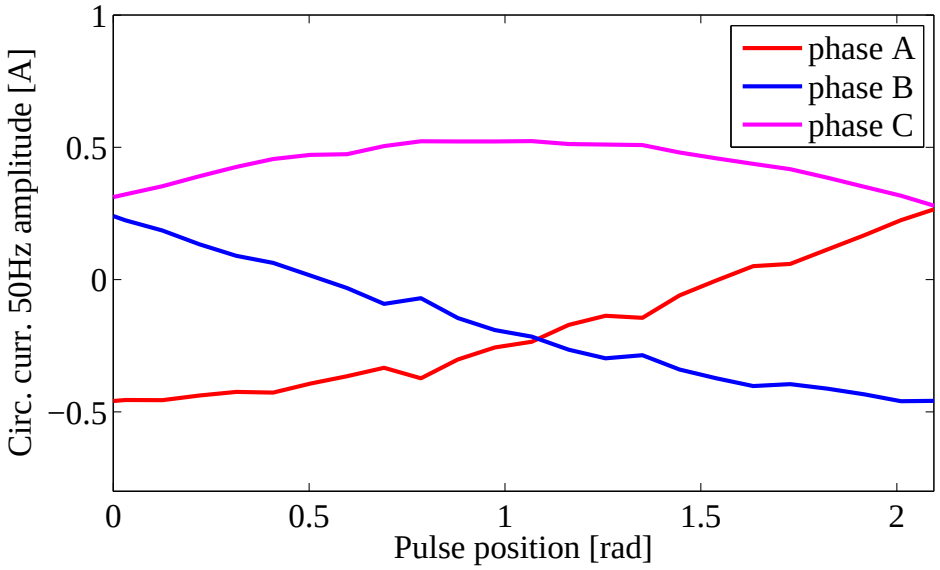


Figure 8.63: Amplitude of the circulating current reference (assuming the phase angle being the same as the AC voltage reference) vs. the pulse position.

The compensated power used to correct arm powers imbalance is presented in Fig. 8.64. Again, the balancing power before pulse, during pulse and their difference are observed. The powers from Fig. 8.61 have very similar waveforms, and any difference is caused by the internal imbalance. The significant difference is in internal imbalance of phase A, which is negligible when the results for method two were recorded.

The AC and DC power fluctuation vs. the pulse position are presented in Fig. 8.65. For all analysed pulsed positions, the converter AC power fluctuation is between 1.35 and 1.75 %, while the DC power fluctuation is approximately 21 %. All pulse positions should result in the same DC current amplitude (DC power fluctuation).

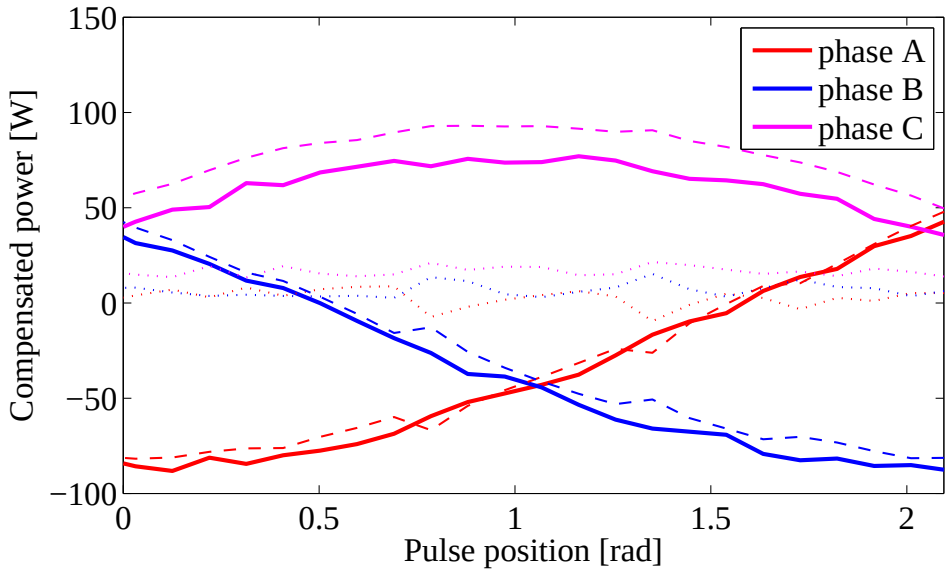


Figure 8.64: Balancing power before pulse (dotted lines), during pulse (dashed lines) and the difference (full line associated with the pulsed load only) vs. the pulse position when the arm balancing method two is used.

However, some variation can be expected due to internal imbalances that vary with the temperature causing different conditions for different pulse positions.

8.5.3 Arm balancing method three

Arm balancing method three considers a tailored distribution of the AC reference signal among arms of the same phase, described by the constant parameter $x_{A,B,C}$. The method can be applied to all pulse positions, and its performance is observed for pulses belonging to one third of the grid voltage period.

The values of $x_{A,B,C}$ parameter before pulse and during pulse were observed, and their difference is supposed to be associated with the pulsed load only. Fig. 8.66 presents $x_{A,B,C}$ parameters values in those conditions vs. the pulse position. The values of the parameter x are always below 2.5 %. The obtained dependence of the parameter $x_{A,B,C}$ on pulse positions is matching the dependence obtained by simulation (Fig.

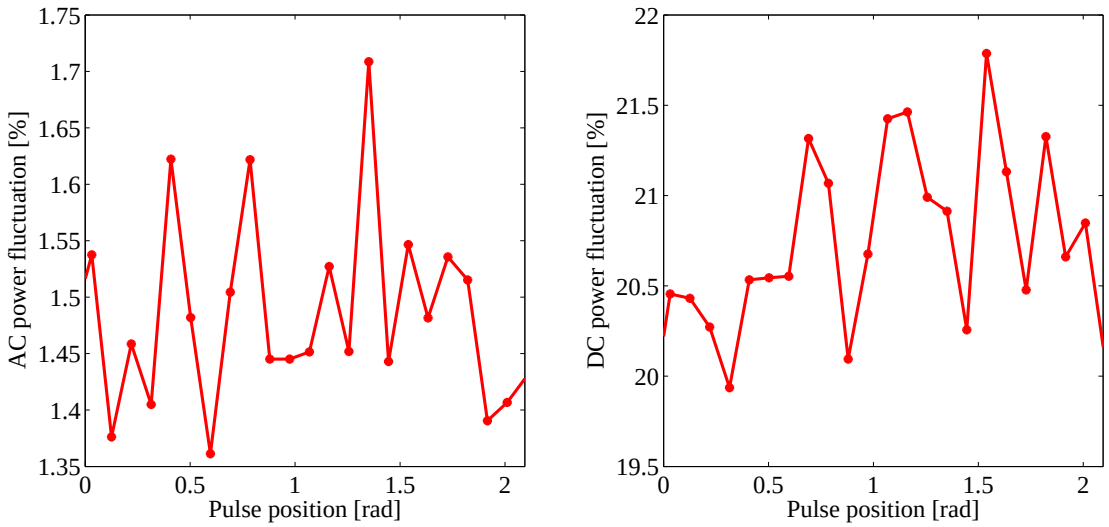


Figure 8.65: AC and DC power fluctuation vs. the pulse position when the arm balancing method two is used.

6.55).

The obtained AC and DC power fluctuation vs. pulse position when method three is applied are presented in Fig. 8.67. The AC power fluctuation is between 1.4 and 1.7 %, while the DC power fluctuation is about 21 %. The obtained DC power fluctuation is similar to the case of the arm balancing methods two, since for both methods a defined amount of the 50 Hz component in the DC current ripple is present regardless of the pulse position.

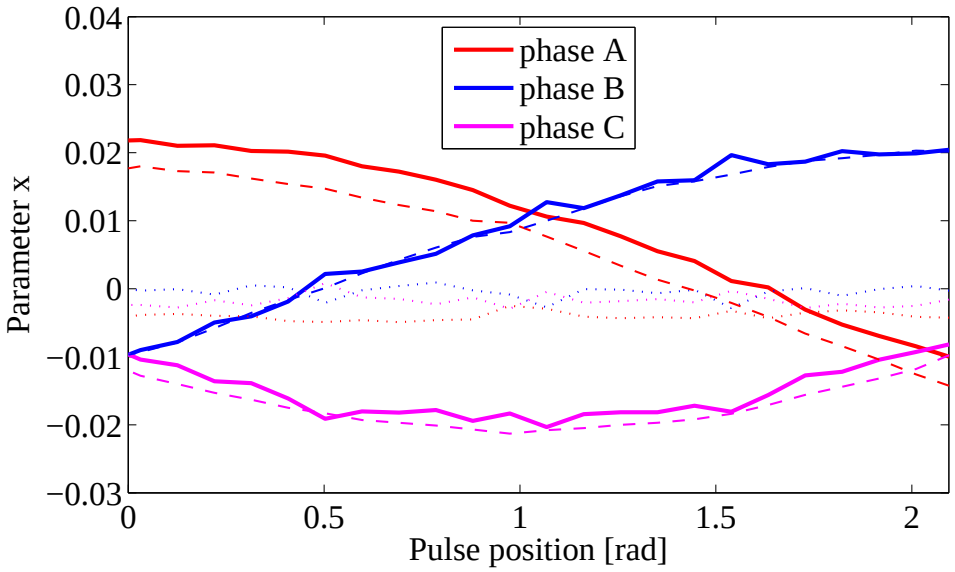


Figure 8.66: Parmeter $x_{A,B,C}$ before pulse (dotted lines), during pulse (dashed lines) and the difference (full line associated with the pulsed load only) vs. the pulse position.

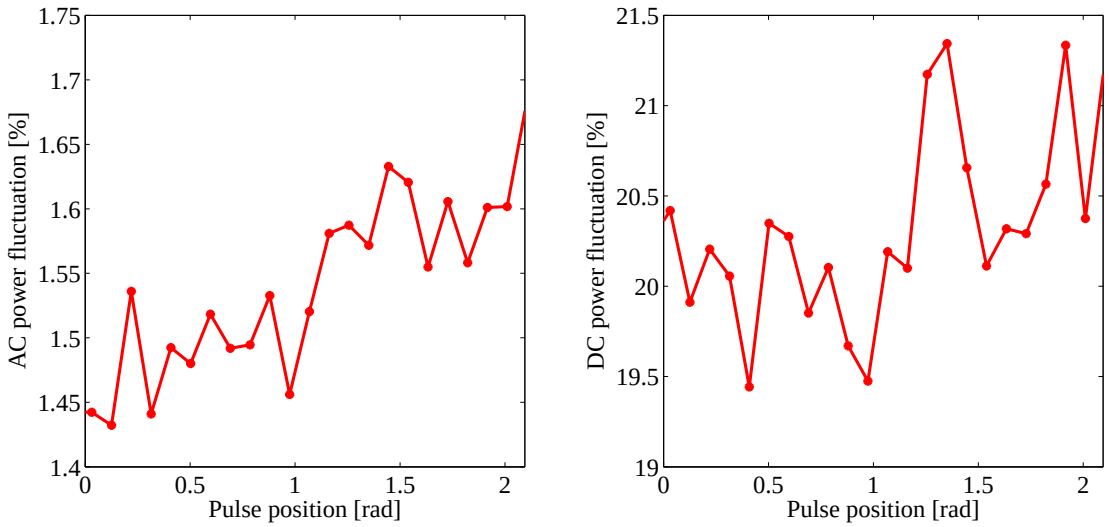


Figure 8.67: AC and DC power fluctuation vs. the pulse position when the arm balancing method three is used.

8.6 Summary

This chapter has presented the results taken at the experimental rig comprising a 9-level modular multilevel converter and its pulsed DC load, drawing a 3.3 kA peak current. The MMC used as a grid interface to the pulsed DC load has issues of the imbalances between converter arms. In the scope of this research three arm balancing methods were developed and analysed. Those three methods were validated experimentally and their performance is in agreement with the analysis and simulation results.

Aside of the arm balancing method performance of the overall control system has been verified. The performance of all control loops has been validated. Some of them were analysed for all arm balancing methods, while others perform exactly the same for all the methods and presenting one of them was sufficient.

The main specification to achieve was low AC power fluctuation. The AC power fluctuation below 1.7 % is achieved for all three arm balancing methods, when switching ripple is neglected. In addition, phase currents do not have significant switching ripple, meaning that the HPI based AC power fluctuation estimation is accurate. The arm balancing method one was performed for a limited number of pulse positions, since it is sensitive to the pulse position. Additionally, the limitation of the rig was the amplitude of the arm currents which extended the critical regions. However, if the pulse position can be chosen with respect to grid voltages the arm balancing method one can perform the intended operation with the constant DC current (and switching ripple). The other two methods ensure low AC power fluctuation regardless the pulse position, with a constant 50 Hz component present in the DC current ripple.

A defined amount of imbalance between converter arms is present even without pulsed DC load, i.e. for the case of no-load or resistive DC load. Therefore, arm balancing controllers happen to be necessary even in those conditions. Arm balancing methods two and three can be used in those cases. Arm balancing method one cannot, since the circulating current references computation is dependant on the DC voltage ripple

50 Hz component.

A distortion in the circulating current has been observed, occurring twice in the fundamental period. This distortion does not depend on the arm balancing method, but it is caused by the distortion in the modulation process, resulting in the phase DC voltage reference not being followed. This is either the issue of the arm currents zero crossing or rounding of the modulation signals. Further investigation and solution would be an interesting topic for the future work.

The converter operation when arm balancing is disabled has been presented as well. This has shown that the overmodulation of converter arms causes the imbalances on the AC side that lead to increased AC power fluctuation. In addition, the performance of the precharge mode and grid synchronisation has been presented in order to complete the rig validation.

Based on the presented results, all theoretical aspects of the control system from Chapter 5 have been proven. The presented results are in agreement with the results obtained by simulation.

Chapter 9

Conclusions

The Compact Linear Collider is a next generation accelerator being proposed at CERN for reaching centre-of-mass energy of 3 TeV. A key component of the overall installation is the RF generation system employing klystron modulators. Given the complexity of the system and the high power levels involved (39 GW peak pulsed power, 300 MW overall average power) the grid interface system requires very detailed consideration. This thesis has addressed research into the grid interface for the CLIC klystron modulators from both the power system and the power electronics conversion points of view. The klystron modulators operate synchronously producing a peak power of approximately 39 GW with the repetition rate of 50 Hz. Such an amount of power requires the design of a highly efficient power system and very good power quality drawn at the grid. This challenge has been approached by analysing possible converter topologies and power system architectures that would satisfy the requirements at both the grid connection point and the klystron modulator inputs. Building a new accelerator demands multiple feasibility and optimisation studies in terms of cost, consumed power, availability, outcomes, etc. and the results presented in this thesis are the contribution to those studies.

Two main power system architectures were considered: single-stage and double-stage conversion. Single stage-power system architectures comprise two low frequency

transformer stages and one AC/DC conversion stage. The double stage conversion architectures include one stage of step-down transformers and both AC/DC and DC/DC converters. Taking into account the grid voltage level and the final DC voltage range, various potential solutions for the intermediate (AC or DC) voltages and final DC voltage is considered. Due to the candidate DC/DC converter voltage ratings, the double-stage conversion architectures are assumed to be less efficient and more expensive than single-stage conversion solutions. Two stages of conversion are usually considered if suppression of the power pulsation is not feasible with the AC/DC converter alone. In this thesis, the feasibility of achieving low AC power fluctuation despite significant DC power fluctuation is assumed (and verified), leading to the selection and demonstration of a feasible single-stage power system architectures.

The power system design respects a set of rules and assumptions that are applied to all potential single-stage conversion architectures. Those include, for example, the application of $(n + 1)$ redundancy in order to achieve higher system availability, selection of cable and transformer ratings and use of standard proven technologies in terms of switches, switchgear and other breaking equipment. The potential voltage levels are selected in order to fully utilise the cables and the switchgear isolation capabilities. Based on this, there are various candidate solutions, characterised by different voltage levels and number of power system components such as converters, transformers, bus bars, etc. For instance, there are three possible DC voltage levels - 6 kV, 10 kV and 20 kV.

Various converter topologies were considered. All potential voltage levels belong to the MV range and higher, which are suitable for multilevel topologies, due to their ability to reach higher voltage levels with standard (lower voltage) components. The multilevel topologies benefit from higher AC waveform quality with reduced switching frequency yielding higher converter efficiency. The choice of the specific topology is done on the basis of the DC voltage rating, where voltages of 10 kV and above are suitable for modular multilevel topologies and lower voltages correspond to simpler topologies, such as the NPC converter.

The power system optimisation required modelling of the power system components with regard to their efficiency and cost; and also modelling the system as a whole with respect to the overall unavailability and fault currents. The unavailability analysis did not indicated any serious sensitivity on the optimisation variables, whilst the maximum fault current analysis eliminated the lowest DC voltage solution (6 kV), while imposing the minimum number of HV/MV transformers and MV bus bars. Further optimisation was done on a sector basis, where each sector is a part of the power system from one MV bus bar to the corresponding klystron modulators. The optimisation is performed to minimise the sector cost and losses while varying the number of power system components for the two DC voltage levels. The power system optimisation results favoured the 20 kV DC voltage region. However, in the higher voltage region, more energy needs to be stored in the klystron modulator capacitor banks for the same DC voltage droop. In that case the relative voltage droop is lower, which improves the AC power fluctuation. The optimisation selects 24 converters for the entire system, where each converter is rated at 16.6 MW and operated at 12.5 MW.

The selected converter topology is the modular multilevel converter, that is composed of 6 symmetrical converter arms, each comprising an arm inductor and a series connection of the submodules. In an MMC the building block is a half-bridge based submodule, where the number of levels in the AC voltage waveform as well as the converter redundancy increases with an addition of a submodule. This feature provides a possibility to bypass a submodule under failure while maintaining normal converter operation. The other benefits particularly important for the CLIC application are high efficiency and AC voltage quality and the ability to separate AC and DC side control. The last feature allows blocking the propagation of the pulsed effects from the DC side to the grid.

For the MMC used as a grid interface to the klystron modulators, closed-loop control is required. The control of both AC power and the DC voltage is required. Due to the decoupled AC and DC side models, the phase current and circulating current controllers are designed independently. The phase current controller is used for generation of the AC part of the arm voltage reference, while the circulating current

controller is responsible for the DC part of the reference, for each of the phases. The phase current controller is used for controlling the AC power, whilst the DC voltage is controlled via the circulating current control. The design of the controllers that maintain the overall energy stored in the converter and those that control the distribution of the stored energy among converter phases and arms is also provided.

The effects of a pulsed DC load, representing the klystron modulator behaviour, on the MMC operation are analysed. Having a pulsed DC load with a repetition rate of 50 Hz is identified as a constant source of imbalance among the converter arms of each phase. The DC voltage ripple has a 50 Hz component that creates non zero arm powers of opposite signs in the two arms of the same phase. Furthermore, the amount of this imbalance power is different for different converter phases due to the different phase shift between the DC voltage ripple 50 Hz component and the converter AC current. To overcome those issues, an arm balancing controller has to be used.

The thesis proposes three arm balancing controllers: one previously reported in the literature, and two newly proposed. Arm balancing method one, is a novel analytical solution for generating the circulating current reference that provides zero average arm power for all the converter powers. This method results in the circulating currents having a 50 Hz component shifted by $\frac{\pi}{2}$ rad from the DC voltage ripple 50 Hz component. A PI controller is designed to regulate the arm imbalance by providing the power compensation (opposite to the imbalance power) based on which the circulating current amplitude is derived. Arm balancing method two, has already been reported in the literature and requires 50 Hz components in the circulating currents that are in phase or in counter phase to the AC voltage references, depending on the sign of the compensated power. The same PI controller can be implemented, as in the case of arm balancing method one. Finally the third method, does not impose the 50 Hz component in the circulating current, but the 50 Hz component appears as a consequence. The method is based on an augmented modulation strategy, with a tailored distribution of the modulation signals between the arms within a phase, to ensure low AC power fluctuation. This way, in the equivalent DC circuit a component proportional to the AC voltage reference is inserted, causing an occurrence of

the 50 Hz component in the circulating current, regardless of its constant reference. The phase angle of those current components is based on the properties of the PI circulating current controller. For high bandwidth circulating current controller, the 50 Hz component in the circulating current has very small phase shift with respect to the AC voltage reference, which leads to similar controller behaviour as in arm balancing method two. Since there is a 50 Hz component present in the circulating current, for any of the arm balancing methods, the resulting DC current has a 50 Hz component.

The control approach and arm balancing methods are verified on a 20 cell per arm converter model with the ratings defined by the power system optimisation result. The pulsed load is emulated with a constant current pulse, discharging the DC link capacitance by the 10 % of the nominal DC voltage. An AC power fluctuation of approximately 0.2 % can be achieved with the proposed control strategy using any of the arm balancing methods.

Since the pulse position has an effect on the amount of the imbalance between the converter arms, the performance of the proposed control strategy is verified in conjunction with any of the proposed arm balancing methods for various pulse positions. Method one is sensitive to pulse position and it has 6 critical regions in which the arm balancing and low AC power fluctuation can not be achieved. In addition, the amplitude of the 50 Hz component in the DC current ripple is dependent on the pulse position, being zero for the most suitable ones, and reaching significant amplitudes in critical points. In the case of arm balancing methods two and three, the balancing is successful for all pulse positions and the amount of AC power fluctuation and the DC current ripple is not sensitive to the pulse position. However, a certain amount of DC current ripple is always present.

A small scale experimental prototype has been built to validate the MMC operation under pulsed DC load. This includes building a 4 cell per arm 7 kW converter, providing a 400 V DC voltage to the pulsed load. The pulsed load has been emulated with a resonant circuit, drawing a 3.3 kA peak current pulse, shaped as a half sine

wave lasting approximately 150 μs. The effect of this current on the DC voltage is similar to the ideal case modelled in the simulation, causing a droop of approximately 10 % of the nominal voltage. Both the converter voltage and current ratings are scaled with the same factor with respect to the values used in simulation.

The effects of the pulsed load, predicted analytically and verified by simulation, are observed on the experimental prototype. The control strategy proposed has been verified experimentally. All proposed arm balancing controllers are validated on the experimental rig, and their performance is observed for different pulse positions. Arm balancing method one has the limitations related to the critical pulse positions in which the arm balancing can not be achieved and low AC power fluctuation can not be guaranteed. For the pulse positions outside this region, the arm balancing is successful and a low AC power fluctuation is guaranteed. Arm balancing methods two and three are successful for all pulse positions, and they provide very similar performance. The control strategy applying any of the three arm balancing methods, given that the arm balancing is successful, ensures AC power fluctuation of approximately 1.5-1.7 %. The DC current 50 Hz component amplitude can be minimised only by choosing a suitable pulse position in the case of arm balancing method one, while for the other two arm balancing methods this amplitude is always approximately 4 % of the nominal DC current.

Arm balancing method one, requires the pulsed DC load to be synchronised to the grid, so that the pulse starts at a suitable moment with respect to the grid voltages. The grid frequency typically oscillates around 50 Hz, meaning that in the case the load is synchronised to some other very accurate timer, the performance of arm balancing method one can not be guaranteed.

Due to the constant source of imbalance between the converter arms, for all presented arm balancing methods, the circulating currents (and the DC current) always have non-zero 50 Hz component, causing an increase of the converter losses and also the need for overrating the current of the switches, arm inductors and cell capacitors. This can be avoided by selecting a different pulse repetition rate, such as 100 Hz or

300 Hz. However, this decision, as well as the decision on pulse synchronisation is to be made by the global CLIC management, by taking into account the operation of the klystron and klystron modulators.

9.1 Summary of achievements and contribution

The achievements and contributions of the presented work are following:

- The review of the multilevel topologies, with the regard to their ability to extend to higher number of levels (AC waveform quality), modularity, efficiency - important parameters for the CLIC application.
- The structured design and optimisation of the power system used as a grid interface for the CLIC klystron modulators. This included various design considerations with respect to the power system architecture, components selection and converter topology selection.
- The controller design for an MMC used in the CLIC application. The review of the topology features and the most frequently used modulation methods. Development of the converter models, on which a decoupled AC and DC side closed-loop control strategy is based and designed.
- The analysis of the pulsed DC load effects on the MMC operation. The load repetition rate of 50 Hz is a constant source of imbalance between the converter arms. Therefore, constant operation of arm balancing controllers is required to actively produce arm balancing variables, which is not the case in typical MMC applications and it has not been analysed in the literature before.
- Two novel arm balancing methods are proposed. Arm balancing method one is a novel analytically based solution for this kind of DC load. Arm balancing method three is a novel augmented modulation strategy that provides the arm balancing given that a PI based circulating current controller is used.

- The evaluation of arm balancing method two, already proposed in the literature, on the MMC with a pulsed DC load.
- The evaluation of the MMC, proposed control strategy and all three arm balancing methods through the numerical simulation. The obtained AC power fluctuation is approximately 0.2 % despite higher DC power fluctuation (10 % and above). The limitations of the proposed algorithms are given by analysing their effectiveness for different pulse positions within the grid voltage period.
- The experimental evaluation of the MMC, proposed control strategy and all three arm balancing methods experimentally. This includes building an experimental rig comprising 7 kW, 400 V DC voltage MMC and a resonant pulsed load with the 3.3 kA peak current; and implementing proposed control algorithms on the DSP/FPGA platform.

The list of the papers published based on the achievements presented in this thesis is given in Appendix C.

9.2 Plans for improvement

Future work includes various improvements that can be made with respect to both the power system optimisation and the power electronics and control part. Some of the objectives for the future work are the following:

- Improved optimisation results can be obtained by using more detailed modelling of the power system components and also by taking into account the economic and other details of the bus bars.
- An optimisation including both the klystron modulators and the power system used as a charger might give different optimisation results. It has already been discussed, that if the DC voltage droop is kept at its maximum value, the

relative droop is smaller with the higher DC voltage, leading to higher energy storage requirements.

- Development of arm balancing methods that would not result in an increase of the DC current 50 Hz component ripple with respect to the ripple induced by the DC voltage controller. Additionally, the success of the balancing methods and the AC power controller should not be dependent on the pulse position.

- Development of a DC voltage controller capable of controlling the peak voltage regardless of the energy taken from the pulse, and pulse duration.

- Better understanding of the cause of internal imbalances present in the experimental prototype even when there is no pulsed DC load (i.e. no-load and resistive load conditions).

- Understanding the cause of the notches in the circulating current obtained experimentally. Removing those notches so that the circulating currents do not have 100 Hz component ripple, would be the next step.

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Appendix A

Civil engineering cost

A.1 Introduction

This appendix presents the distribution of the switchgear, converters and transformers within the sector, and estimation of the civil engineering infrastructure cost. The sector delivering 20 kV is used as an example. Cost of the buildings and cable galleries are estimated on the basis of CERN internal data. The size of the MV/LMV transformers, converters, and switchgear is assumed and the relevant data is presented here.

A.2 Spatial distribution and estimation of civil engineering cost

Fig. A.1 presents the spatial distribution of a single sector delivering 20 kV DC voltage. As previously mentioned, MV bus bars are already distributed along the drive beam fairly close to the klystron modulators. The length of the bus bar is estimated on the basis of number of connections per length. It has been assumed that one

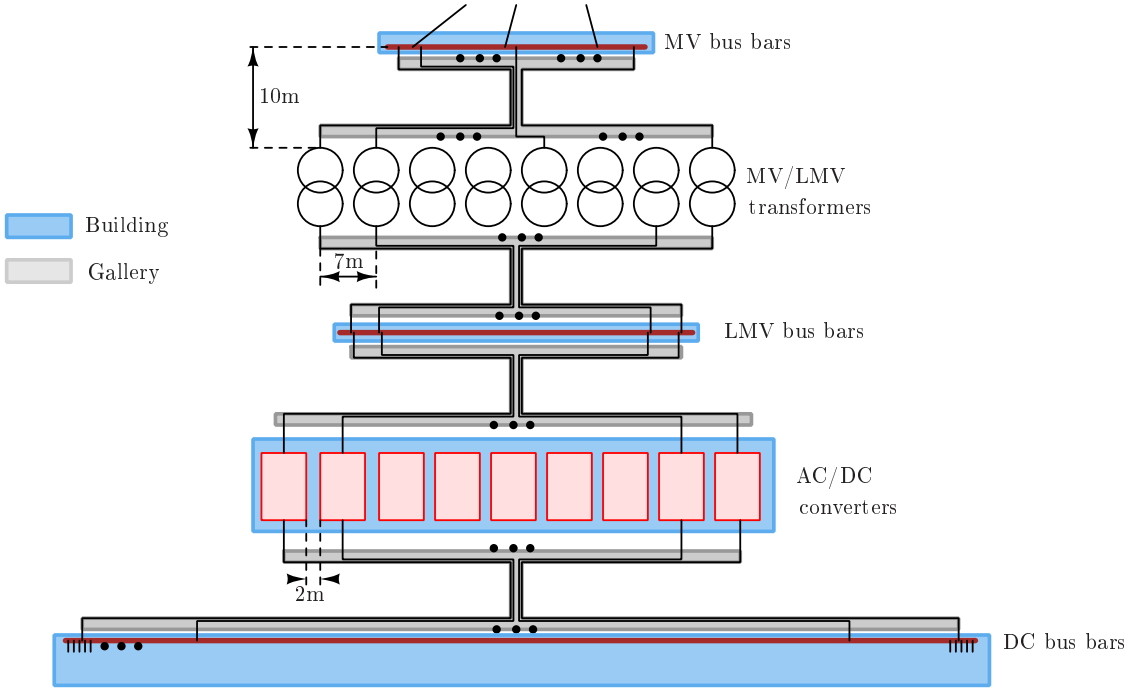

Figure A.1: One sector spatial distribution and civil engineering infrastructure.

switchgear, 1 m long, has two three phase connections. Therefore, the length of the enclosed switchgear racks is assumed to be proportional to the number of connections of both feeders (connections to the HV/MV bus bars) and loads (connections to the MV/LMV bus bars). Here, in the case of current ratings requiring paralleling of the cables, the number of connections is increased. Similarly the size of the LMV bus bars and DC bus bars is derived. The MV bus bars and LMV bus bars are placed in separate buildings, with the dimension of bus bar length multiplied by 10 m, one floor (4 m high). The cost of a two-floor building (8 m tall) is assumed to be 1650 GBP per meter square.

The minimum distance between bus bars (building) and transformers or bus bars and converters (building) is assumed to be 10 m. All buildings are placed in parallel to the drive beam, while the 10 m distance is assumed in orthogonal direction, as presented in Fig. A.1.

The size of the transformers is assumed to be fixed regardless of different power ratings. They are placed 7 m apart from each other (this follows standard practice design at CERN). This corresponds to the typical size of a cast-resin insulated transformers with the rated power in a MW range.

Based on the electrical connections of an MMC from Fig. 4.1, the physical representation of an MMC with N submodules per arm is presented in Fig. A.2. The MMC size is estimated on the basis of the size of converter cell, dominated by the energy storage element. The dimensions of a 3 mF, 1 kV capacitor is assumed to be 30 cm×30 cm×30 cm (based on the similar components available in the laboratory) and based on the capacitance one coordinate is scaled. The dimension of half bridge and drivers is assumed to be the same, while the dimension of an arm inductor is assumed to be 30 cm×30 cm×20 cm. The approximated structure considers three converter phases in a row, 2 m apart, while all converters belonging to one DC voltage bus bar are distributed in columns and fitted to a single building. Converters are assumed to be fitted in two-floor buildings, and in the cases their height is higher than 8 m the cost of the building is scaled accordingly.

The cables do not follow the shortest paths, but the paths defined by the gallery in which the cable is placed. The cable galleries are typically 2 m×2 m tunnels where cables can be placed in a form of a matrix. The price of the cable gallery per unit of length is assumed to be 2310 GBP, and the maximum number of cables to be placed inside is assumed to be 96 (32 three phase cables). In this case the distance between cables is about 20 cm. In the case that not all the cables following the cable path can fit to one of the galleries, a larger gallery is assumed with the price scaled up with respect to additional cables (additional cross section of the gallery) to be placed. The distribution of cable galleries is presented in Fig. A.1.

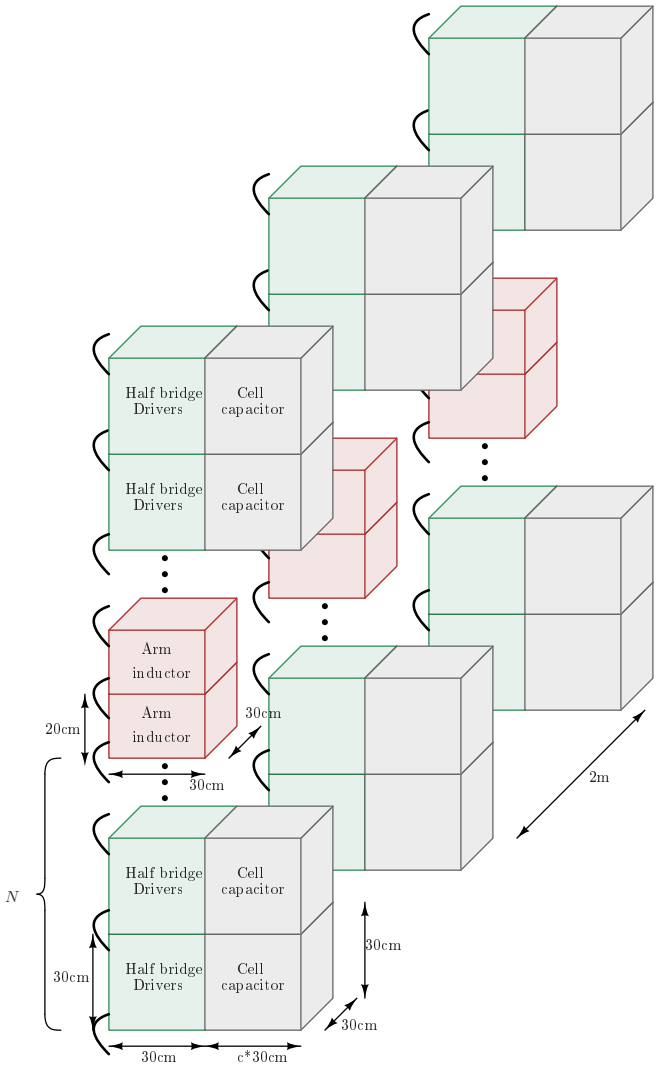

Figure A.2: MMC converter physical model.

A.3 Summary

The spatial distribution of one sector delivering 20 kV is presented. Based on the presented assumptions, the requirements for the sizes and cost of buildings storing enclosed switchgear and converters are estimated. In addition, sizes and cost of the galleries are also estimated on the basis of spatial distribution and the amount of cables they need to fit. The spatial distribution also defines cable lengths used in the cable losses and cost estimation in section 3.4.

The presented derivation required multiple assumptions with regard to sizing of converter, transformers, switchgear. The approximate values used, might not provide the exact estimation of the system cost, but they show a trend of dependence on different power ratings of power system components. For instance gallery cost dependence on the number of cables or converter size (building size) dependence on the cell capacitance.

In the case of sectors used to deliver 10 kV DC voltage, two groups of MV/LMV transformers, LMV bus bars, converters and DC bus bars are required. In that case the number of cable galleries and buildings increases, but they are shorter when compared to the previously presented case.

Appendix B

Modelling converter waveforms for different pulse positions

B.1 Introduction

This appendix considers the derivation of the DC current and other converter waveforms for different pulse positions through numerical simulation in Matlab. The models are derived for arm balancing methods one and two, for which the circulating current 50 Hz component reference is known.

B.2 Waveforms modelling

In order to understand the dependence of circulating currents and DC current waveform on the DC voltage phase angle, a constant amplitude of the DC voltage ripple 50 Hz component ${V_{DC50}}^1$ is assumed, with the phase angle ϕ_{DC50} varying from $-\pi$ to π rad. The ideal converter AC waveforms are also assumed, based on the converter parameters from Table 6.1. Under these circumstances, the parameters of the AC

Table B.1: Amplitudes and phase angles of AC waveforms and DC voltage.

Signals	Amplitude	Phase angle
i_A	1.29 kA	0 rad
v_{AC_A}	8.57 kV	-0.2 rad
v_{DC50}	${V_{DC50}}^1$	$(-\pi, \pi)$ rad

waveforms are given by Table B.1. The angles of phases B and C are shifted with respect to phase A for $-\frac{2\cdot\pi}{3}$ and $-\frac{4\cdot\pi}{3}$, respectively.

First, arm balancing method one is assumed and the amplitude of the circulating current references for phases A, B and C are given by (5.33), Chapter 5. Based on this equation and the values from Table B.1, the denominator dependence on the DC voltage phase angle is obtained, as presented in Fig. 5.14, Chapter 5.

The circulating and DC current amplitudes are dependent on V_{DC50}, while the DC current amplitude affects the amplitude of the DC voltage ripple V_{DC50}. Therefore, in order to obtain the absolute values, first an assumption of ${V_{DC50}}^1 = 0.1 \cdot V_{DC}$ is made. The DC current amplitude, ${I_{DC50}}^1$, is then computed (sum of circulating current amplitudes) assuming the phase angle is equal to $\phi_{DC50} - \frac{\pi}{2}$. The amplitude of the DC current ripple is proportional to the DC voltage ripple.

The load current also has a 50 Hz component, shifted by $\frac{\pi}{2}$ with respect to the DC voltage 50 Hz component ripple (Fig. 5.7, Chapter 5). The vector diagram of the load current, DC current and DC voltage 50 Hz component is presented in Fig. B.1. The load current 50 Hz component, is equal to the first harmonic of the periodical pulsed signal, as given by:

$$I_{load50} = \frac{I_{peak} \cdot 2}{\pi} \sin(\pi \frac{T_{pulse}}{T_{rep}}) \approx \frac{I_{peak} \cdot 2}{\pi} \cdot \pi \frac{T_{pulse}}{T_{rep}} = 2 \cdot I_{DC} \tag{B.1}$$

where I_{DC} is nominal DC current. Due to the short pulse duration when compared to the pulse period, an assumption that a $\sin(\alpha) \approx \alpha$ for the small angle α, is applied.

Based on Fig. B.1 the relation between the 50 Hz component of the DC current and

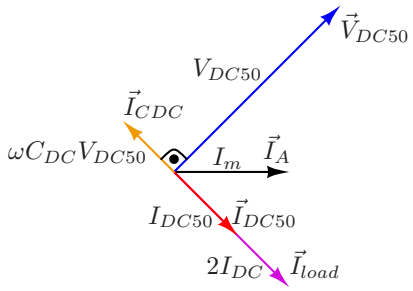

Figure B.1: Equivalent vector diagram for the 50 Hz component of the DC link related waveforms when arm balancing method one is used.

the DC voltage, can be derived as:

$$(2 \cdot I_{DC} - I_{DC50}) \frac{1}{\omega \cdot C_{DC}} = V_{DC50} \tag{B.2}$$

Knowing that the 50 Hz component ripple of the DC current is linearly dependent on the DC voltage ripple, the amplitude of the DC current (lagging by $\frac{\pi}{2}$ behind the DC voltage) is computed as:

$$I_{DC50} = \frac{2 \cdot I_{DC}}{\omega \cdot C_{DC} \frac{V_{DC50}{}^{1}}{I_{DC50}{}^{1}} - 1} \tag{B.3}$$

The absolute value of the DC current ripple 50 Hz component is presented in Fig. 5.16, Chapter 5. Very similar dependence is obtained by simulation and is presented in Fig. 6.52. Similarly to the DC current amplitude, the circulating current amplitudes, originally computed with $V_{DC50}{}^{1}$, can be scaled to obtain their characteristics for the real DC voltage amplitude ripple, V_{DC50}.

The angle of the load current, when the pulse delay of t_{start} is taken into account, is given by:

$$\phi_{load50} = \phi_{load50}{}^{0} - 2 \cdot \pi \frac{(t_{start} + \frac{T_{pulse}}{2})}{T_{rep}} \tag{B.4}$$

where $\phi_{load50}{}^{0}$ corresponds to the angle of 50 Hz component of load current when there is no delay ($t_{start}{}^{0} = -\frac{T_{pulse}}{2}$) which is equivalent to a cosine with zero phase shift. However, in this model and simulation model (Chapter 6) the phase current with a zero phase shift is associated with the sine, providing $\phi_{load50}{}^{0} = \frac{\pi}{2}$. The DC voltage

angle is leading by $\frac{\pi}{2}$ load current (Fig B.1), giving the relation of the pulse position ($2 \cdot \pi \frac{t_{start}}{T_{rep}}$ in radians) and the DC voltage angle presented in Fig. B.2.

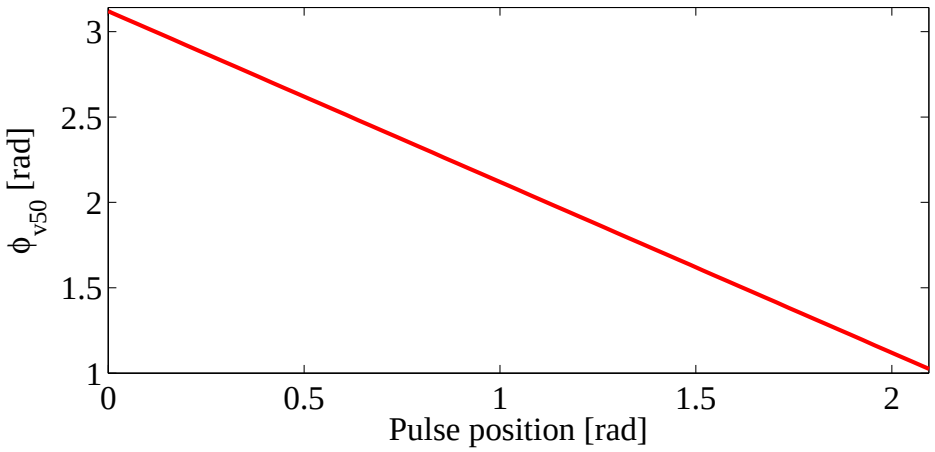

Figure B.2: DC voltage ripple 50 Hz component phase angle vs. the pulse position in the case of arm balancing method one.

In the case of arm balancing method two, the 50 Hz component of circulating current references is described by (5.34), Chapter 5. In that case the denominator of all three phases is equal and not dependent on pulse positions. However, the amplitudes of circulating currents are dependent on pulse position and linearly dependent on the amplitude of the DC voltage ripple 50 Hz component. Again, the amplitude of the DC voltage ripple 50 Hz component is assumed to be ${V_{DC50}}^1 = 0.1 \cdot V_{DC}$. The circulating current references are aligned with the corresponding AC voltage references. They can be projected on the phase A AC voltage vector and an orthogonal vector (lagging $\frac{\pi}{2}$ behind the AC voltage vector). In that case the amplitude of the DC current can be computed as:

$$ {I_{DC50}}^1 = \sqrt{({I_{circ50\_A}}^1 - \frac{1}{2}({I_{circ50\_B}}^1 + {I_{circ50\_C}}^1))^2 + (\frac{\sqrt{3}}{2}({I_{circ50\_B}}^1 - {I_{circ50\_C}}^1))^2} \tag{B.5} $$

where ${I_{circ50\_A,B,C}}^1$ are for the assumed DC voltage ripple 50 Hz component amplitude. The phase angle of the DC current is not dependent on the DC voltage ripple

amplitude, and it is computed as:

$$\begin{aligned}\phi_{IDC50} &= \phi_v - \text{atan2}(\frac{\sqrt{3}}{2}({I_{circ50\_B}}^1 - {I_{circ50\_C}}^1), {I_{circ50\_A}}^1 - \frac{1}{2}({I_{circ50\_B}}^1 + {I_{circ50\_C}}^1)) \\ &= \phi_v + \phi_{DC50}\end{aligned} \tag{B.6}$$

The equivalent vector diagram of the 50 Hz components of the DC side voltages and currents in the case of arm balancing method two is presented in Fig. B.3. The same pulse position is assumed as in Fig. B.1, giving the same relative position of the load current vector with respect to the phase A current.

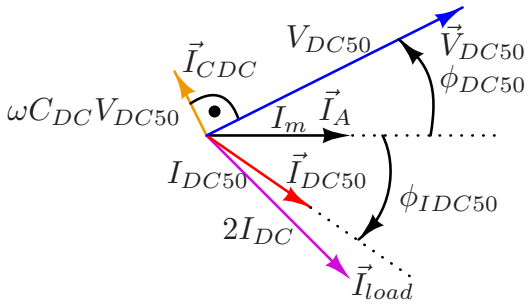

Figure B.3: Equivalent vector diagram for the 50 Hz component of the DC link related waveforms when arm balancing method two is used.

The phase shift between the DC voltage vector and the DC current vector is constant for all pulse positions and it is equal to $-\phi_v$, and the angle between the DC capacitor current and the DC current is therefore equal to $\frac{\pi}{2} - \phi_v$. Both, DC link capacitor current and the DC current ripple 50 Hz component amplitude are proportional to the DC voltage ripple amplitude, while the load current amplitude is fixed to $2 \cdot I_{DC}$ (B.1). Based on the currents triangle the actual DC voltage ripple 50 Hz component V_{DC50} can be found and the computed DC current amplitude ${I_{DC50}}^1$ scaled to its actual value. The DC current amplitude is computed by:

$$I_{DC50} = \frac{2 \cdot I_{DC}}{\sqrt{1 + (\omega \cdot C_{DC} \frac{{V_{DC50}}^1}{{I_{DC50}}^1})^2 - 2 \cdot \omega \cdot C_{DC} \frac{{V_{DC50}}^1}{{I_{DC50}}^1} \cdot \cos(\frac{\pi}{2} - \phi_v)}} \tag{B.7}$$

and it is not dependent on the pulse position. The DC current ripple 50 Hz component amplitude obtained by (B.7) and by simulation (Section 6) is presented in Fig. B.4.

The amplitudes obtained by simulation are matching the analytically obtained ones.

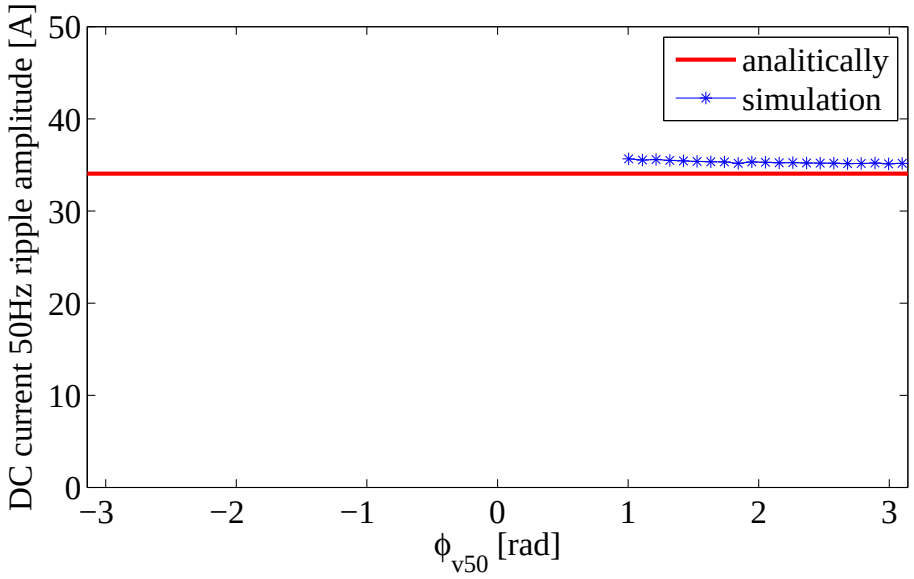

Figure B.4: DC current ripple 50 Hz component vs. the DC voltage ripple phase angle in the case of arm balancing method two.

Similarly to the case with arm balancing method one, the phase angle of the load current 50 Hz component is known (B.4), and the phase shift between this current and the DC voltage ripple can be found. Based on this dependence of the DC voltage ripple angle on pulse position in radians can be found. Again the as the pulse position moves from 0 rad to $\frac{2\cdot\pi}{3}$ rad, the DC voltage angle moves from 3.079 rad to 1.005 rad, linearly.

B.3 Summary

The arm balancing method one has the denominator of equation (5.33) dependent on the pulse position. Furthermore, the DC current ripple 50 Hz component is also dependent on the pulse position. The DC current ripple amplitude varies from zero, in 6 pulse positions, to infinity in critical 6 pulse positions. The angle of the DC

current ripple is always shifted by $\frac{\pi}{2}$ from the DC voltage ripple. On the contrary, in the case of arm balancing controller two, both the denominator of (5.34) and the resulting DC current amplitude are constant regardless of the pulse position. The phase shift between the DC voltage ripple and the DC current ripple 50 Hz component is also constant and it is defined by the phase shift between converter AC voltage and current.

Appendix C

Publication list

The following publications presented at international conferences are results of the research investigations directly related to this thesis:

1. M. Jankovic, A. Watson, J. Clare, P. Wheeler, and D. Aguglia, "Grid Interface Challenges and Candidate Solutions for the Compact Linear Collider's (CLIC) Klystron Modulators," in *Pulsed Power Conference (PPC), 2013 19th IEEE*, pp. 1-6, June 2013.

2. M. Jankovic, A. Watson, J. Clare, P. Wheeler, and D. Aguglia, "Optimal Power System and Grid Interface Design Considerations for the CLICs Klystron Modulators," in *Power Modulator and High Voltage Conference (IPMHVC), 2014 IEEE International*, pp. 83-88, June 2014.

3. M. Jankovic, A. Watson, J. Clare, P. Wheeler, and D. Aguglia, "Grid Interface Design for the Compact Linear Collider (CLIC)," in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, pp. 1-10, Sept. 2015.

4. M. Jankovic, A. Costabeber, A. Watson, and J. Clare, "Control of a Grid Connected Modular Multilevel Converter under Pulsed DC Load," in *Industrial*

Electronics Society, IECON 2015 - 41st Annual Conference of the IEEE, pp. 2526-2531, Nov. 2015.

5. M. Jankovic, A. Watson, A. Costabeber and J. Clare, "Control of a Modular Multilevel Converter with Pulsed DC Load," in *in Energy Conversion Congress and Exposition (ECCE), 2016 IEEE*, CD-ROM paper, Sept 2016.