DC Fault ride through operation of a Full bridge MMC converter

Yixue Feng MSc.

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Abstract

In recent years the growth of renewable energy has encouraged the development of HVDC grids. One challenge of building HVDC grids is the power converter response to DC side faults. The full-bridge Modular Multilevel Converter (MMC) is a desired power converter topology which is used in HVDC grids due to its scalability, modularity and capability of blocking DC side faults.

Post fault operation of the full-bridge MMC requires the control of power flow, the energy of each sub-module capacitor and the elimination of circulating harmonic current to reduce power loss while DC line-to-ground or DC line-to-line faults exist.

This thesis presents a post fault operation method for a full-bridge MMC in order to transmit partial power after a DC line-to-ground fault and provides reactive power after DC line-to-line fault. Simulated results are provide from a point-to-point HVDC system which consists of two eleven-level full-bridge MMC.

Acronyms

HVDC High Voltage Direct Current. 2

IPD In-Phase Disposition. 95

LCC Line Commutated Converter. 2

MMC Modular Multilevel Converter. 3

PR Proportional Resonant. 114

VSC Voltage Source Converter. 2

List of Terms

C Sub-module capacitance. 57

ΔW_C Energy stored in upper arm minus energy stored in lower arm. 62

f Fundamental frequency. 58

I_{ac} AC side current. 56

i_{cu} upper arm capacitor current. 58

I_{dc} DC side current. 56

I_{diff} Circulating current of one phase. 62

I_l Lower arm current. 56

I_n Circulating current. 56

$I_{reactive}$ Reactive current. 71

I_{real} Active current. 71

I_u Upper arm current. 56

I_{valve} Arm current. 101

L_c Arm inductance. 62, 116

N Sub-module number in one arm. 54

N_c Currently inserted sub-module number. 101

N_l Lower arm inserted sub-module number. 54

n_l Lower arm insertion index. 54

N_s Modulation number of inserted sub-module. 98

N_u Upper arm inserted sub-module number. 54

n_u Upper arm insertion index. 54

P_{CD} Conduction power loss of Diode. 81

P_{CT} Conduction power loss of IGBT. 81

P_e Real power proportion on the upper arm. 70

P_l Power flow through lower arm. 61

P_u Power flow through upper arm. 61

R_c Arm resistance. 116

R_u Reactive power proportion on the upper arm. 71

ΣW_C Energy stored in one phase-leg. 62

v_0 Average voltage of sub-module capacitor. 65

V_{abc} Three phase voltage in Cartesian coordinate system. 107

V_{ac} AC side voltage. 54

v_c Sub-module capacitor voltage. 49

V_{cl} Lower arm sub-module capacitor voltage. 55

V_{cu} Upper arm sub-module capacitor voltage. 55

V_{dc} DC side voltage. 54

V_{diff} Voltage across arm inductor. 62

V_{dq} Three phase voltage in dq0 coordinate system. 108

V_l Lower arm voltage. 53, 57

V_{ph} Phase-leg voltage. 57

V_{sm} Sub-module voltage. 49

V_u Upper arm voltage. 53, 57

W_l Energy stored in lower arm. 61

W_u Energy stored in upper arm. 61

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Chapter 1

Introduction

1.1 Objectives and motivation of the thesis

Multi-terminal high voltage direct current (HVDC) grids are a technically and economically viable solution for future bulk power transmission for the development of large scale renewable energy. By connecting different power sources such as wind, hydro and solar, HVDC grids have advantages of flexibility and reliability. The renewable energy power source such as offshore wind power farms are usually located in remote areas. Compare to an AC system, HVDC is more economic for transmission over long distance, especially when using cable to transmit the power.

Currently HVDC system exist mostly point-to-point systems with Line Commutated Converter (LCC) or Voltage Source Converter (VSC). VSC is more suitable for HVDC grids since it does not need to reverse voltage polarity to change power lower direction. As one of the topologies of VSC, Modular

Multi-level Converters (MMC) could provide high voltage, high performance waveforms with a low switching frequency. Its modularity allows the increase of the voltage rating of converter by adding more sub-modules.

One of the challenge of building a HVDC system is how it would react to a DC side fault. For example, it would take about two month to fix a submarine cable. During the repair time, the transmission between the onshore and offshore system are cut. MMC with full-bridge sub-modules is able to continue to produce the rated AC waveform up to a complete reversal of the DC-Link voltage, as such it has a DC fault blocking response. And after DC fault, full-bridge MMC can partially transmit power.

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The main aim of this project is to research full-bridge MMC post DC fault operation. The advantage of the full-bridge sub-module is that it could provide negative voltage and lead to arm voltage range increase to $[-V_{dc}, V_{dc}]$. It assumes that in a symmetric monopole point-to-point HVDC system, two full-bridge MMC converters are connected through two power cables. After a DC line-to-ground fault, both converters have one pole connected to ground. One possible operation method is that the faulted pole arm could provide the voltage as AC voltage V_{ac}, and the other arm provide voltage as $\frac{1}{2}V_{dc} - V_{ac}$. Then on DC side the voltage is $\frac{1}{2}V_{dc}$ so that the point-to-point system could

continue to transfer half rated power. There are also other possible post line-to-line fault operation methods. After DC line-to-line fault, both converters have two pole connected with ground. One arm could provide the voltage as AC voltage V_{ac}, and the other arm provide voltage as $-V_{ac}$. Then on DC side the voltage is 0, but on AC side the converters can still provide reactive power.

The full-bridge modular multilevel converter can only operate correctly when all the sub-module capacitor voltage are controlled. Also, energy inside the sub-modules in one arm have to be evenly distributed. The harmonic circulating which is caused by interaction between arm inductor and sub-module capacitors should be eliminated to reduce power loss.

This thesis provides post fault operation method and the control schemes which include power flow control, energy inside sub-modules control and proportional resonant control. All these methods and control schemes allow the full-bridge MMC continue to transfer half rated power after DC line-to-ground fault, and provide reactive power to each side AC system after DC line-to-line fault.

The objectives of this thesis are:

- To evaluate the current research into full-bridge modular multilevel converters, in an effort to show the advantages of this topology in order to response to DC side fault.

- Research a post fault operation method which enable the HVDC system transmit partial rated power after DC side line-to-ground fault and provide reactive power after line-to-line fault.

- To simulate a point-to-point system with 11-level full-bridge modular multilevel converter to investigate the post fault operation method.

1.2 Statement of originality

The author believes that the originality presented in this thesis lies in the following:

- The new management algorithm for the full-bridge MMC such that it can continue to transmission power with one cable grounded after a dc side line-to-ground fault. The operation can be extended to minimize voltage stress on the ac side transformer. The MMC has to operate asymmetrically to remove voltage stress on transformer, thus the second harmonic circulating current and the sub-module capacitor voltage need to be controlled.

- The new management scheme can eliminate second harmonic arm current for post fault operation.

- The new management scheme can control the total energy of one phase and can control the energy difference in the upper and lower arms, to balance sub-modules energy of the upper and lower arms for asymmetric post fault operation.

1.3 Outline of the thesis

Chapter two provides an overview of the HVDC grids and the DC grid power flow control schemes. An overview of different voltage source converter topologies are then given. The background of HVDC cables and circuit breaker are provided.

Chapter three presents analysis of full-bridge modular multilevel converter in normal operation. The second harmonic circulating current and sub-module capacitor voltage estimation are investigated. The post fault operation modes are presented in order to enable the converter continue operation after DC side line-to-ground fault or line-to-line fault. The best post line-to-ground fault mode is given from the power loss point of view.

Chapter four presents the control schemes of full-bridge modular multilevel converter in normal and post fault operation condition. The sub-module balancing scheme is based on level-shifted PWM, and the rotation speed depends on the carrier wave frequency. The rest control schemes AC, DC current control, second harmonic circulating current elimination and the energy of sub-module capacitor voltage.

Chapter five presents the overview of CIGRE DC grid system. It provides the reference for the parameters of simulated full-bridge modular multilevel converter. The scaling method for the simulation circuit is also provided. The advantages and disadvantages of different cable modelling methods are

presented. A non-switching model of MMC converter is presented in order to reduce the simulation computation time.

Chapter six presents the simulation results obtained by using Matlab/Simulink. Evaluation of the post fault operation schemes and MMC control schemes are presented.

Chapter seven gives the conclusions for the work as a whole and is followed by several appendices containing information on the power loss calculation of post fault operation.

Chapter 2

Literature Review

This chapter presents a review of HVDC system grid. The chapter begins with a general introduction to HVDC system configurations and grid topologies. Power flow control schemes are then presented, including the advantages and disadvantages of each scheme. A brief introduction of the available converter topologies is provided, which classified into modular and non-modular structures. Background information on HVDC cables and DC circuit breaker topologies are then presented.

2.1 HVDC grids

Multi-terminal high voltage direct current (HVDC) grids are a technically and economically viable solution for future bulk power transmission required due to the development of large renewable energy installation [1–6]. The reason for considering an HVDC system is that it has lower cost for long

distance power transmission compared to an HVAC system. The break-even distance, which is when cost of HVDC system and HVAC system are equal, for an overhead line is 500-800 km [7–9], for a cable is 50 to 80 km [10–13].

HVDC converters can be classified as Line-Commutated Converters (LCC also called Current-source converters) and Voltage-Source Converters (VSC). The LCC, which is thyristor-based, is also known as the classic HVDC or traditional HVDC converter since it has been used from 1972 [14]. The main difference between LCC and VSC is that the VSC uses semiconductor devices such as IGBT, which can be controlled to turn on and turn off. Meanwhile LCC uses thyristor, which can only be controlled to turn on with turn off relies on the external circuit. This freedom gives the VSC advantages such as black start capability and reactive power control [15]. Most importantly, the VSC changes the power flow direction by changing the current direction, maintains the voltage polarity the same. This makes it more suitable for multi-terminal HVDC transmission [16].

Up to now, HVDC systems mainly has been point-to-point connections. Instead of connecting these point-to-point systems, an HVDC grid has less converters, and as a result the investment cost and conversion loss will lower. Moreover, an HVDC-VSC grid is more flexible for power flow and energy trading, and will increase grid security [17]. The configurations of HVDC-VSC system are given in the following subsections.

2.1.1 HVDC system configuration

The arrangement of VSC converters for HVDC power transmission can be classified into the following types, asymmetric monopole, symmetric monopole and bipole [15, 18]. Here a brief description of each type of system is presented.

Asymmetric monopole configuration

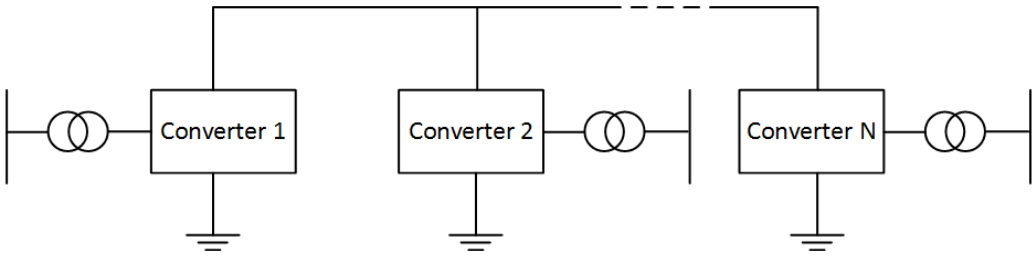


Figure 2.1: The configuration of Asymmetric monopole HVDC grid with earth return

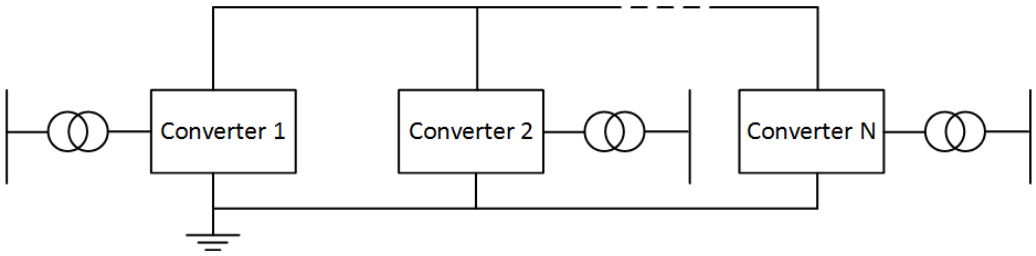


Figure 2.2: The configuration of Asymmetric monopole HVDC grid with metallic return

Figure 2.1 shows the configuration of an asymmetric monopole HVDC grid with earth return. Figure 2.2 shows the configuration of an asymmetric monopole HVDC grid with metal return. The common conception between

them is that they both have a single HVDC converter connected via a single conductor at the full HVDC voltage. The advantages of earth return are reduced cable investment cost and relatively less transmission loss [3]. However, the metallic return is essential when the continuous current flow through earth is not permitted [3].

Symmetric monopole configuration

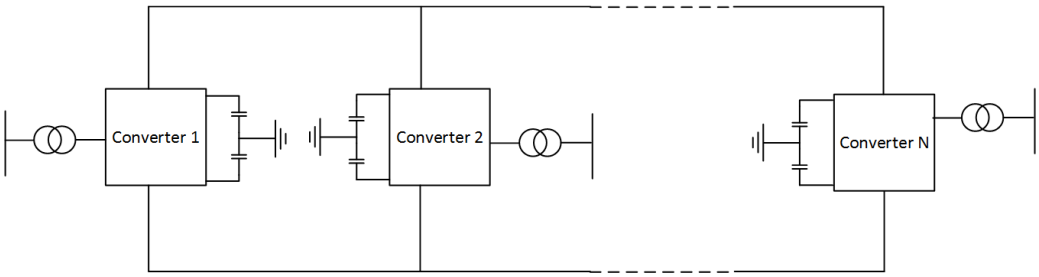


Figure 2.3: The configuration of Symmetric monopole HVDC grid

The configuration of a symmetric monopole HVDC grid is shown in figure 2.3. Unlike the asymmetric monopole, it features a single HVDC converter with two conductors, and the grounding is at the middle of the DC side. This increases the power transmission compare to asymmetric monopole configuration since the DC side voltage doubled, and in normal operation, no current flows through the earth [3].

Bipole configuration

As shown in figure 2.4, the configuration of a Bipole HVDC grid consists of two HVDC converters connected in series and grounded in the middle. The

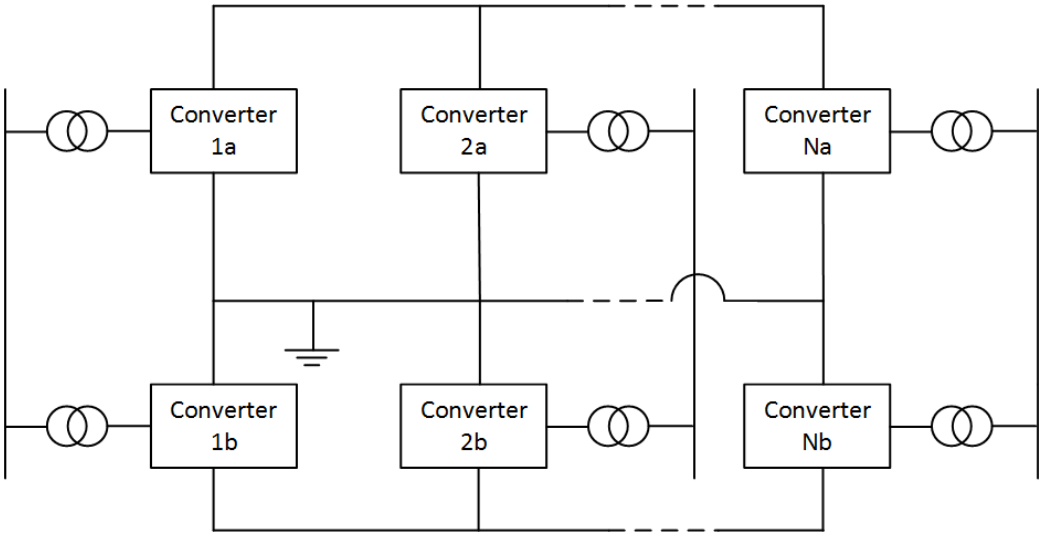


Figure 2.4: The configuration of Bipole HVDC grid

most attractive point about the Bipole configuration is that with one cable fault. It is shall possible to operate the system at reduced power [18].

Mixed configuration

In order to build DC Grids, it is important that all the readily existing HVDC systems can be connected into the grid. As long as the DC voltages are the same, the three types of HVDC system configuration can be connected together. Figure 2.5 shows one example of a configuration mixing three types. Converter 1 is a bipolar structure. Converter 2 is asymmetric monopolar with metallic return, with the grounding point at converter 1. Converter 3 is a symmetric monopole configuration.

If the number of terminals in Figure 2.5 is increased, there are many possibilities for interconnection between the terminals. The topology of the

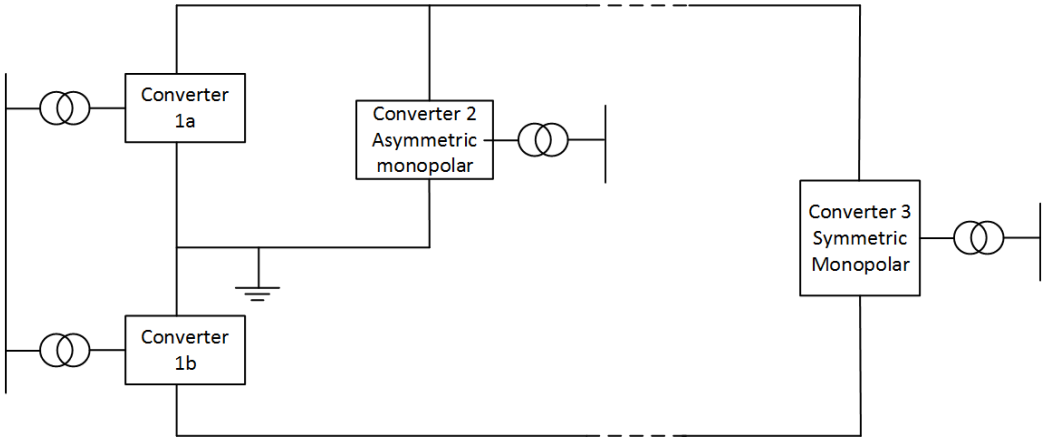


Figure 2.5: The configuration of Mix HVDC grid

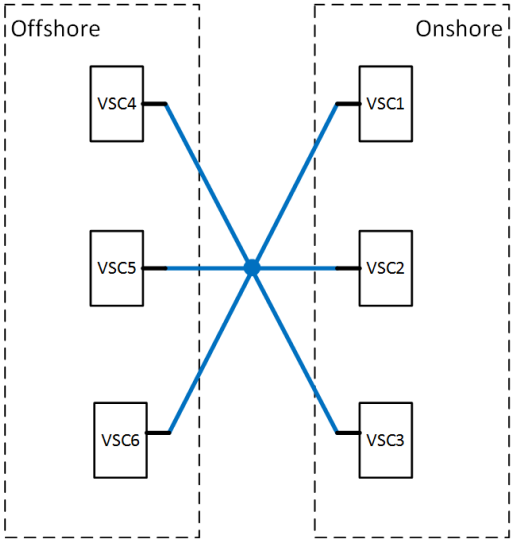
multi-terminal HVDC grid has an impact on the steady state system losses and grid reliability [19]. Different topologies of HVDC grid are discussed in the next subsection.

2.1.2 HVDC grids topology

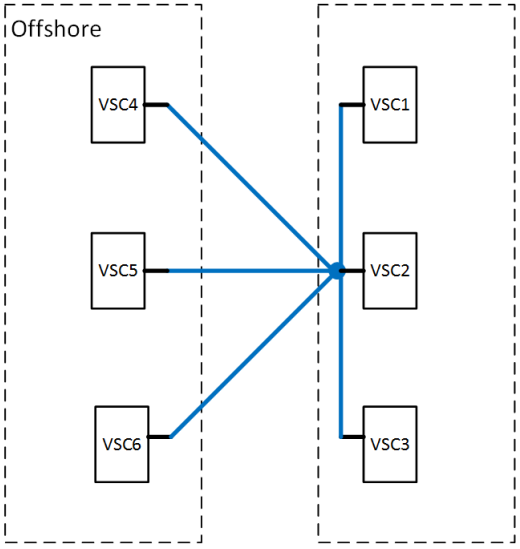
There are three HVDC grid topologies are considered here: star topology, ring topology and meshed topology [19–21]. We take a 6 terminal HVDC system as an example, assuming 3 of them are onshore substations and the other 3 are offshore wind farms. The pros and cons of each topology are demonstrated below.

Star topology

Two star topologies are shown in Figure 2.6. The central point could be on an offshore platform or on an onshore substations, respectively as illustrated



(a) Star topology with central node



(b) Star topology with central substation

Figure 2.6: Star topology of HVDC grids

in 2.6a and 2.6b. Either way the terminals are connected at one central node.

The advantages of star topology are: first, the topology structure is simple; second, the cost of this topology is low since the cable rating of the transmission lines is same as the rating of the corresponding terminal. The disadvantage is that if a fault occurs at the central node the whole grid goes down. When a DC fault occurs on a cable, and if the DC fault is permanent, which is highly possible, the corresponding wind farm or substation is lost. This causes the reliability of the star topology to be low [19, 20].

Ring topology

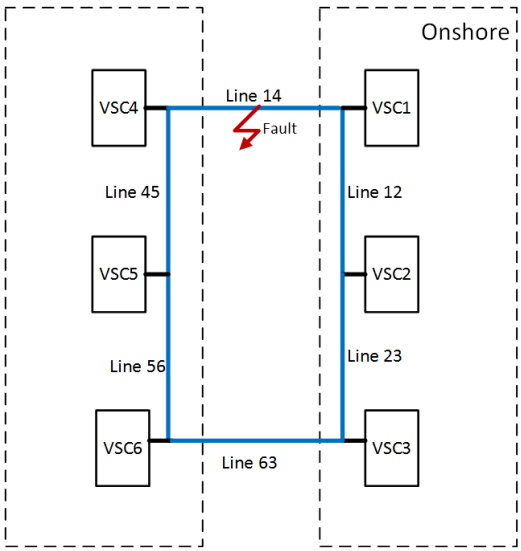


Figure 2.7: Ring topology of HVDC grids

Figure 2.7 shows a ring topology HVDC grid. The terminals are connected as a closed loop. This topology has more reliability and flexibility

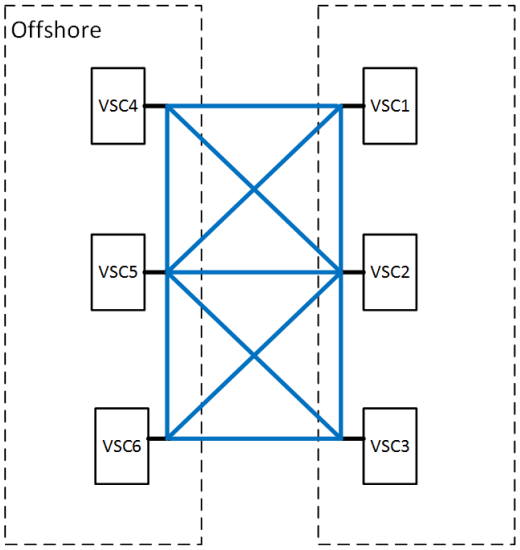


Figure 2.8: Mesh topology of HVDC grids

than the star topology [19, 20].

The absence of a central node avoids the whole grid to go off due to a simple fault. Also when a DC fault occurs, for example at line 14, the open loop is able to operate without losing wind farm 4. However, this also lead to a disadvantage of the ring topology which is that the cable rating need to be higher than in a star topology. In the above example, after line 14 is disconnected, the power from wind farm 4 has to go through line 45, line 56 and line 63 to be transferred to onshore. As a result, the rating of line 63 is at least the sum of the power rating of wind farm 4,5 and 6. This increases the investment cost [20].

Meshed topology

The mesh topology is presented in figure 2.8. It is an extreme case in that all terminals are connected with each other. The purpose is to show the advantages and disadvantages of the mesh topology clearly.

The benefits of a meshed topology is that the reliability and flexibility is increased [19]. If the line between terminal 1 and 4 is disconnected as in the ring topology example, the power from wind farm 4 has more choices to be transferred onshore. The drawback is that the increased connections use more cables than the star or ring topologies. As stated before, connecting all terminals with each other may not be necessary in practice, so the cost will a trade off between reliability and cable cost. Anyhow, the high reliability and flexibility make the mesh topology more suitable to meet future HVDC grids requirements than the others [19].

The topology of an HVDC grid can be a mix of the above. For example, the wind farms could be connected to onshore first, with a subsequent increase in connections from a star or ring to a mesh by adding cables. The grid building could be a gradually growing process. The optimal topology depends on the terminal locations and power flow scenarios. The power flow control methods of multi-terminal HVDC grids is introduced next.

2.2 Literature review of published power flow control schemes

There are two types of methods to control multi-terminal HVDC grid power flow: by adding a device such as a voltage source at the end of lines, and by power flow control schemes. The published power flow control schemes can be classified into three types: Master-slave control [16, 22, 23], voltage margin control [24–26] and voltage droop control [27–31].

2.2.1 Device power flow controller

In multi-terminal HVDC VSC grids, the flow of current in the transmission lines depend on the voltage difference of the two ends and the impedance. Although in theory the line current can be controlled by adding resistance, steady state loss would be increased significantly. On the other hand, if an auxiliary dc voltage controller is added on one end of the line, the power flow on the line can be controlled by introducing a voltage source [32]. The loss then will then depend on the efficiency of this device. Up to now, three topologies of device are proposed: Thyristor power flow controller [33], DC/DC device [34] and current flow controller [35].

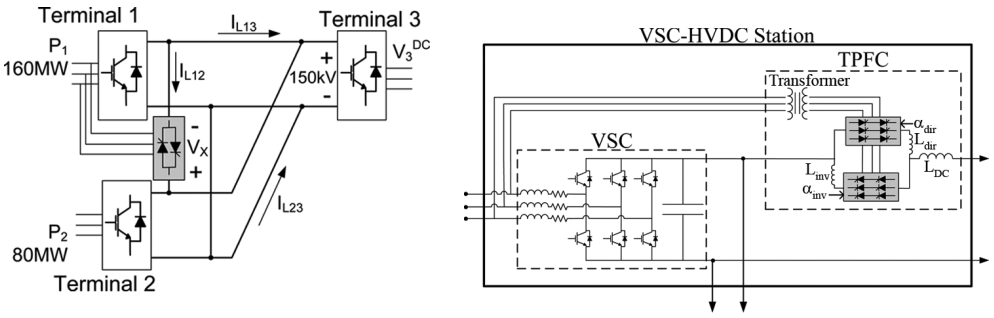


Figure 2.9: The structure of thyristor power flow controller [33]

Thyristor power flow controller

The structure of a thyristor power flow controller is shown in figure 2.9. It is inserted in series in the dc transmission line and it consists of two 6-pulse thyristor bridges to have four-quadrant operation. The rating of this thyristor controller is expected to be 10% of the connected VSC converter [33].

DC/DC device

Since a DC/DC converter can produce a voltage difference, it can be placed at the end of line to control current flow. There are many topologies for a DC/DC converter which could be used to connect different HVDC grids [36–38]. Figure 2.10 shows the structure of a bipolar DC/DC converter. In [34], a voltage control ratio $1\% - 20\%$ for the DC/DC device when used in power flow control is considered to be optimal.

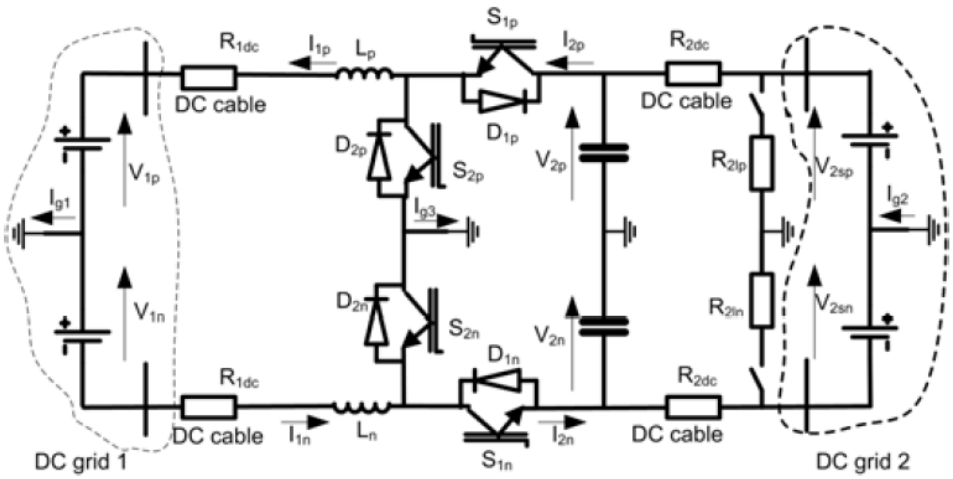


Figure 2.10: The structure of bipolar DC/DC covnerter [34]

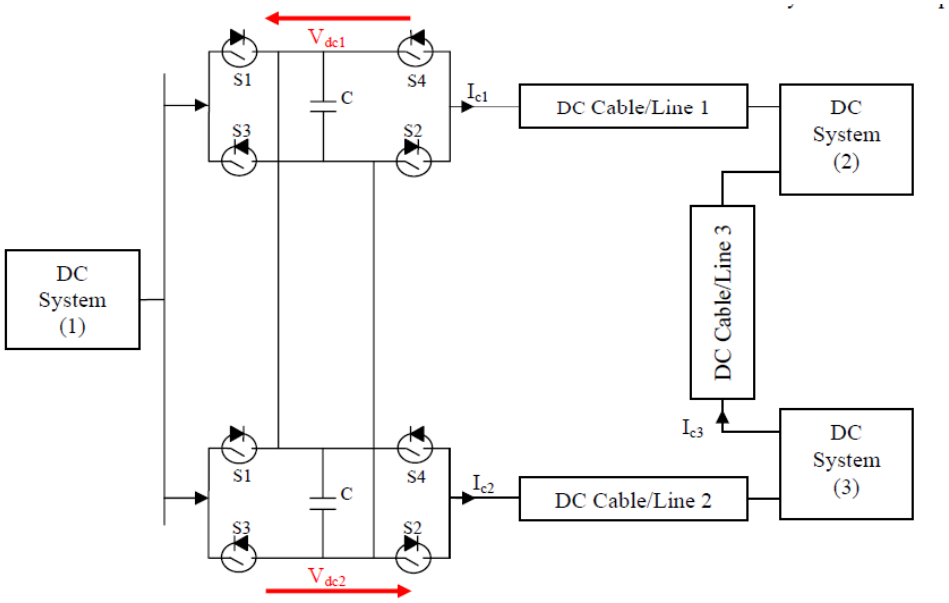


Figure 2.11: The structure of Current Flow Controller [35]

Current flow controller

Figure 2.11 illustrates the structure of a current flow controller. Both the thyristor power flow controller and this CFC are connected in series with

cables. The difference is that in order to reduce power loss, the thyristor PFC transfers the power draw from the DC cable to an AC side through a transformer, while the CFC transfers this power to another cable. As a result, the AC transformer rating of the thyristor PFC has to be the DC system voltage, meanwhile the rating of this CFC can be the insertion voltage which is much smaller than DC system voltage [35].

All three devices introduced above are theoretically able to control the power flow of HVDC grids. They could increase the DC grid power flow flexibility by assisting the other multi-terminal HVDC power flow control schemes which are discussed next. However, the investment cost and efficiency of these devices still need to be investigated [35].

2.2.2 Master-slave control

In point-to-point HVDC systems, one converter controls the DC voltage and the other converter controls the power flow. The same control can be used in a multi-terminal system, where one converter controls the DC voltage and the others control the power flows [22]. The converter controlling the DC voltage acts as master controller, and its power flow depends on the rest of the converters.

The master converter has to be able to provide and absorb a large power when necessary. For example, when a converter is lost or there is an increased

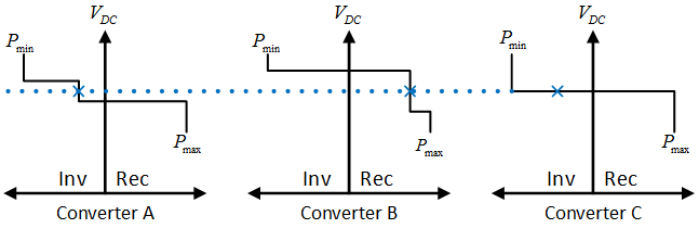
demand from one terminal. The worst case happens when the master converter fails since the whole system will go off. Consequently, for a mesh HVDC grid, master-slave control is not very suitable [23].

2.2.3 Voltage margin control

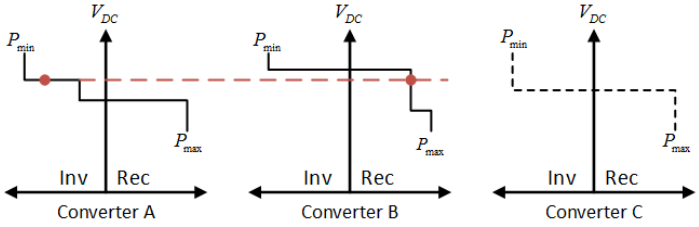
In voltage margin control, each converter is given a DC voltage offset. The difference between the converter offsets is defined as the voltage margin [24, 25]. The DC voltage offset can be set in 2-stages to reduce the reliance on the communications between terminals [26].

Compared to Master-slave control, the advantage of Voltage margin control is that when the converter controlling the DC voltage is lost, a new equilibrium point (power balance point) will be reached automatically and another converter will regulating the DC voltage.

Figure 2.12 shows an example of 2-stage voltage margin control of three terminals A,B and C. When all the three converters are in operation as in figure 2.12a, terminal C controls the DC voltage. After terminal C is lost, as shown in figure 2.12b, the system reaches a new balance where terminal A controls the DC voltage.



(a) An example voltage margin control of HVDC grids with three terminals

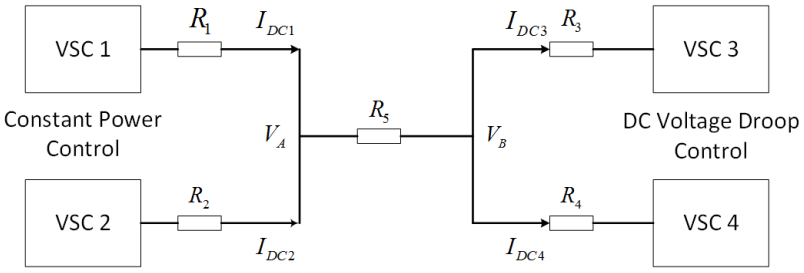


(b) An example voltage margin control of HVDC grids with three terminals while terminal C is outage

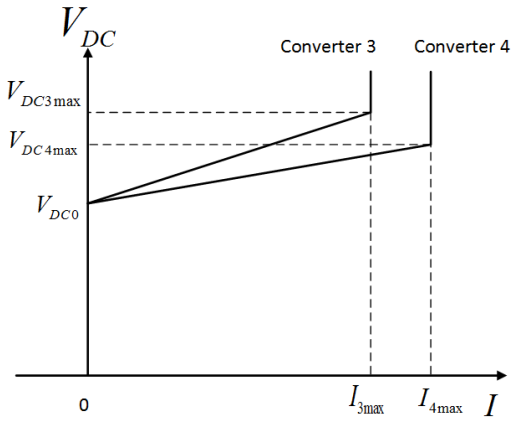
Figure 2.12: An example voltage margin control of HVDC grids [24]

2.2.4 Voltage droop control

Another control method is named voltage droop control. It regulates the DC voltage based on the relation between voltage and power or current. An example of the Voltage-Power characteristic or Voltage-current characteristic of one converter is illustrated in Figure 2.13 [16, 27, 29]. The limits on voltage and current are determined by the terminal converter. The DC voltage reference will be calculated according to the droop characteristics.



(a) An example of HVDC grids with four terminals



(b) Voltage droop control characteristics of terminal 3 and 4

Figure 2.14: An example voltage droop control of HVDC grids [30]

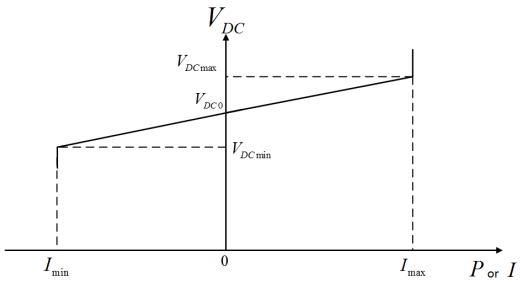


Figure 2.13: An example of Voltage-Power characteristic or Voltage-current characteristic of one converter

Simplified four terminal HVDC grid is shown in Figure 2.14a. Assume VSC 1 and 2 are offshore wind farms and they are provide constant power; VSC 3 and 4 are onshore substations and they both implement voltage droop

control. The resistors represent the impedance of the cables. Define the V/I characteristic slope of VSC 3 as $k_3 = \frac{V_{DC3max} - V_{DC0}}{I_{DC3max}}$ and the slope of VSC 4 as $k_4 = \frac{V_{DC4max} - V_{DC0}}{I_{DC4max}}$. Then the DC voltages of VSC 3 and 4 are:

$$\begin{aligned} V_{DC3} &= V_{DC0} + k_3 I_{DC3} \\ V_{DC4} &= V_{DC0} + k_4 I_{DC4} \end{aligned} \tag{2.1}$$

According to the grid structure, the voltage at V_B is:

$$V_{DC3} + R_3 I_{DC3} = V_{DC4} + R_4 I_{DC4} \tag{2.2}$$

Substituting (2.1) to (2.2) yields

$$\begin{aligned} k_3 I_{DC3} + R_3 I_{DC3} &= k_4 I_{DC4} + R_4 I_{DC4} \\ \frac{I_{DC3}}{I_{DC4}} &= \frac{k_4 + R_4}{k_3 + R_3} \end{aligned} \tag{2.3}$$

If we assume the voltage increase is small compared to nominal voltage, and the magnitude of k_3, k_4 are much greater than R_3, R_4, then the power sharing between VSC 3 and 4 is

$$\begin{aligned} \frac{P_{DC3}}{P_{DC4}} &= \frac{V_{DC3} I_{DC3}}{V_{DC4} I_{DC4}} \\ &\approx \frac{I_{DC3}}{I_{DC4}} \\ &= \frac{k_4}{k_3} \end{aligned} \tag{2.4}$$

Equation (2.4) illustrates that the slope of the voltage droop characteristic will determine the power sharing between terminals [30, 39]. The droop gain also influences the DC voltage disturbance and grid stability [31, 40, 41]. Different from voltage margin control, in which only one terminal controls the DC voltage at a time, voltage droop control enables any number of terminals to adjust the DC voltage to reach the desired steady state condition.

An appropriate multi-terminal HVDC grid control scheme should be able to maintain at steady state when a DC side fault occurs. The next section gives review of voltage source converters topologies and then types of possible DC side fault are discussed.

2.3 Voltage source converters

2.3.1 Non-Modular Voltage Source Converter (VSC) topologies

This section contains a literature review of VSC topologies proposed for HVDC systems. Discussion is provided on the advantages and disadvantages of each topology for HVDC power transmission and the ability of each converter to withstand DC faults. The discussion is limited to comparison of VSC topologies and not on the comparison with line commutated alternatives.

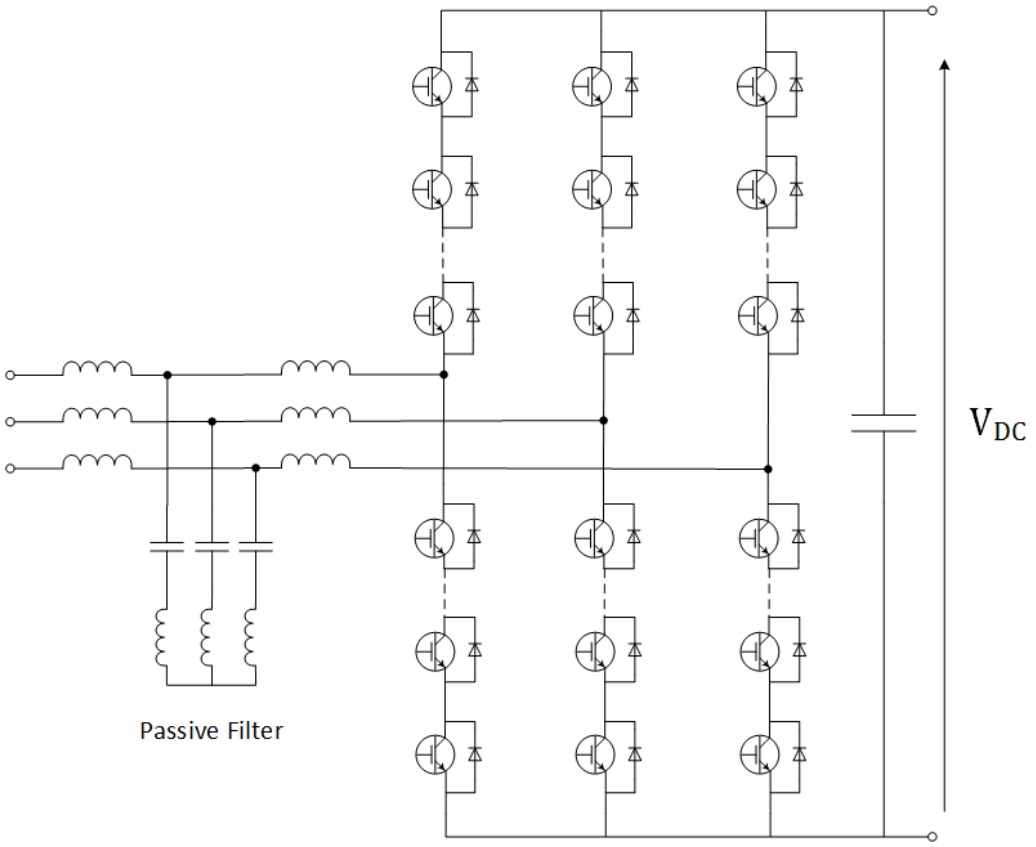
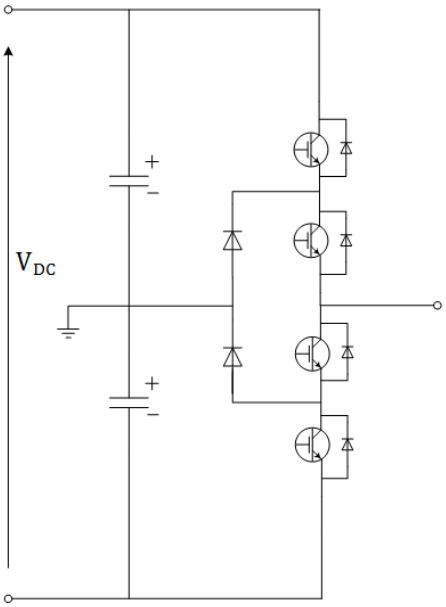


Figure 2.15: Two level Voltage Source Converter

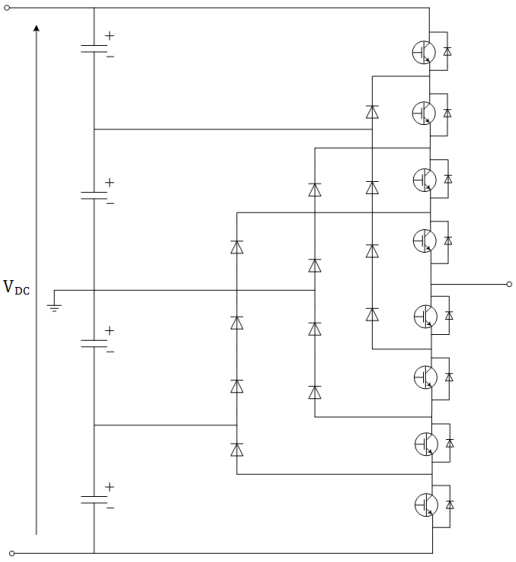
Two level converter topology

In Figure 2.15, a two level converter is shown [42]; for HVDC applications a high number (greater than 100) of series connected IGBTs are required to achieve the necessary voltage rating. The advantage of the two-level VSC for HVDC power transmission is it is a relatively simple circuit to control with techniques well published in the literature [43–50]. The disadvantages of this converter when used for this application arise from the requirement to use PWM to decouple the AC voltage from the DC voltage magnitude [51, 52]. This requires that the series string of IGBTs are hard switched introducing additional switching loss as well as extra complexity required to dynamically share the device voltage during the switching event. The PWM switching pattern will also introduce harmonics into the output voltage; which require bulky passive filters to mitigate them to acceptable levels defined by the grid codes [53, 54].

Further disadvantages include poor DC side fault performance; when the DC voltage is depressed, such that when the AC voltage exceeds that of the over-modulation region permitted by triple harmonic injection, then the AC voltage causes the two-level converter to rectify into DC grid and the AC breaker must be opened. Additionally when the DC grid voltage is fully reversed the IGBT diodes will begin to conduct regardless of the state of the IGBTs and the AC side breaker [55, 56].



(a) 3-level diode clamped topology



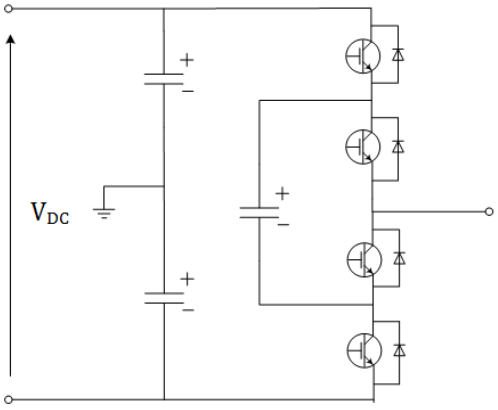
(b) 5-level diode clamped topology

Figure 2.16: Topologies of 3-level converter

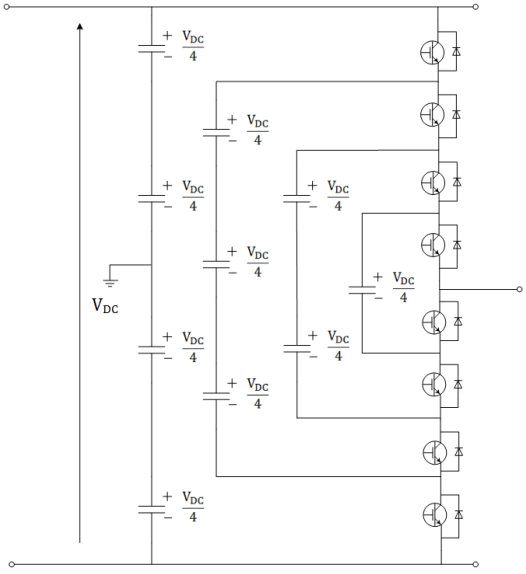
Non-Modular Multilevel topologies

In Figure 2.16a, one phase of a three-level diode-clamped converter is shown [57]. It is a three-level inverter it has available voltage outputs of $+V_{dc}, 0$ and $-V_{dc}$. The advantages are relatively low switching loss and a good basic AC waveform compared to the two level converter [51]. If the converter is extended to further levels additional clamping diode pairs need to be introduced as shown for the five level case in Figure 2.16b. The total number of diode pairs increases rapidly with the number of levels [58]. For one phase of N-level diode clamping inverter requires (N-1) capacitors, 2(N-1) switches and (N-1)(N-2) clamping diode [59]. The non-modular nature of the topology also means that the clamping diodes do not have a common voltage rating; i.e. some clamping diodes need to be rated for the full DC bus and others do not . Assuming series connected devices are used to achieve this voltage rating, it can be observed that for each extra level many more components are required. Additionally the split DC-Link capacitors introduces complexity in voltage balancing [60, 61].

In Figure 2.17a, one phase of three-level floating capacitor topology is shown. It is also called "capacitor clamped" and "flying capacitor" [62–64]. Instead of adding diodes as in Figure 2.16a, floating DC capacitors, C_f, are added. The advantages are low switching loss, good AC waveform compared to the two-level inverter, and the switches (have the same duty) are at the same rating. Similarly to the diode clamped-topology, when the number of levels is increased, the number of added capacitors increases rapidly. For one



(a) 3-level floating capcitor topology



(b) 5-level floating capcitor topology

Figure 2.17: Topologies of 5-level converter

phase of an N-level flying-capacitor converter, (N-1)(N-2)/2 flying capacitors and (N-1) main dc bus capacitors are required [60]. This large number of capacitors also leads to a large footprint [51].
As with the two-level voltage source inverter a reversal of the DC bus causes the diodes in both the diode-camped and floating capacitor topology to conduct, thus it is not suitable for use in multi-terminal HVDC systems relying on the converter to provide the fault blocking capability.

2.3.2 Modular topologies

Modular multilevel converter (MMC) converter

The modular multilevel converter was first proposed in 2003 [65]. The MMC converter shown in Figure 2.18a (half-bridge variant shown) is constructed from a number of series connected sub-modules [42, 66, 67]. The advantages of this topology include scalability, modularity, and low switching losses [68–70].

The modular nature of the converter means that the same building blocks can be used to expand the converter to higher voltages with more levels. This has benefits for commercialization such as reducing development costs and reduction in spares holding requirements [68, 71].

Each sub-module, used as a power electronics building block, includes a self-contained DC-Link which allows at least a two-level output and at the

same time restricts the voltage seen across the semiconductors. The consequence of this is that the required high voltage rating can be achieved, while semiconductor voltage sharing issues are mitigated, switching losses are reduced. Additionally the high number or output levels means the converter is able to produce a cleaner output voltage reducing passive filter requirements [72–75].

The disadvantage, of what is essentially taking the bulk energy storage components and distributing them in a smart way around the converter, is that additional complexity is required in the way that energy is managed [76–83].

The MMC as classically proposed is formed from half-bridge sub-modules as shown in Figure 2.18a. The half-bridge sub-module MMC suffers from poor fault performance for similar reasons to the two-level inverter; the IGBT anti parallel diode starts to conduct if the DC bus voltage is reversed. Additionally as each sub-module cannot produce a negative output, over-modulation is only possible via triple harmonic injection, as a consequence a DC voltage depression limits the output AC voltage such that converter will need to be disconnected via opening of the AC circuit breaker.

Variants of the traditional MMC can be constructed using alternative sub-modules. Figure 2.18b shows proposed sub-module topologies [66]. The full-bridge sub-module is able to an output produce voltage of $+V_c, 0$ and $-V_c$. The ability to be able to produce a negative voltage means that the

converter is able operate even during a full reversal of the DC bus voltage [67]. However, the use of additional semiconductors increases the losses. For the Clamp-Double Sub-Module, it acts as two half-bridge sub-modules in normal condition. When a fault occurs, the IGBT T5 is able to cut off the fault current. Modular High Frequency is used for low power range.

Parallel hybrid Converter

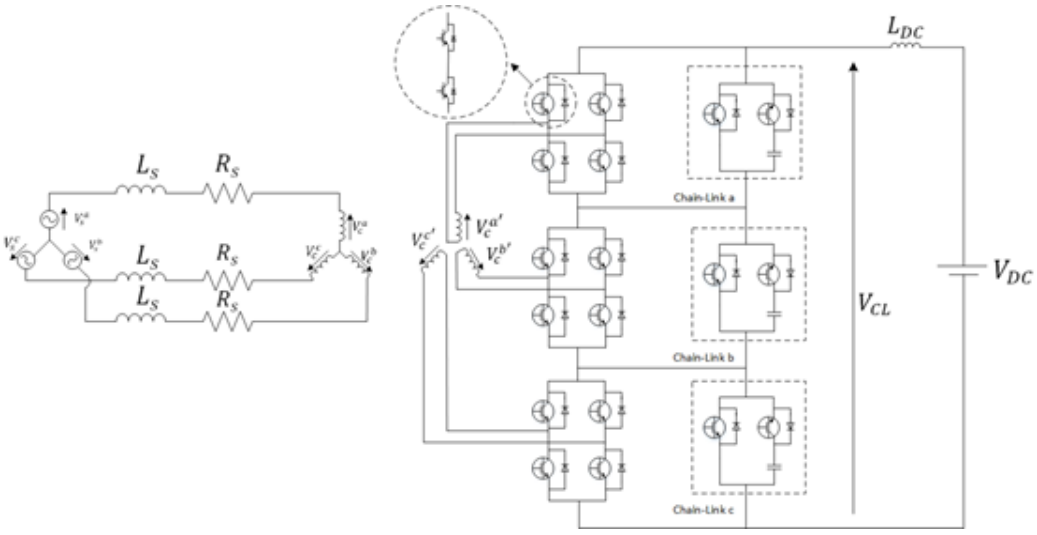
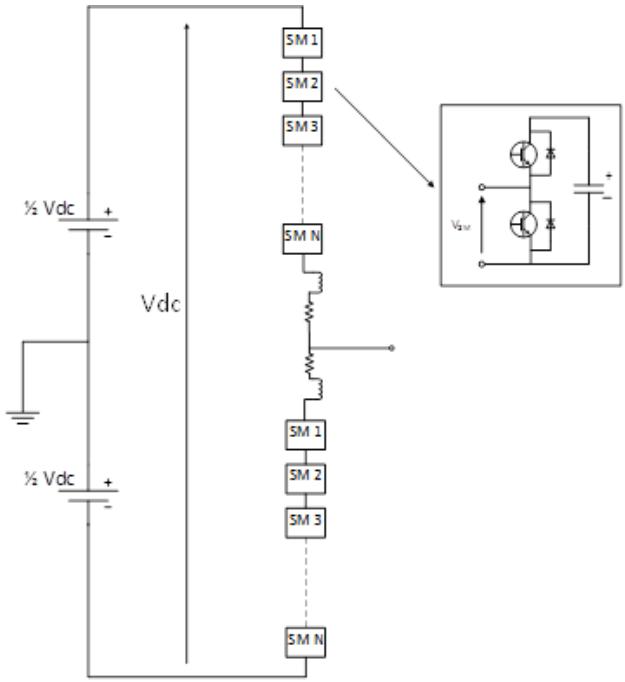
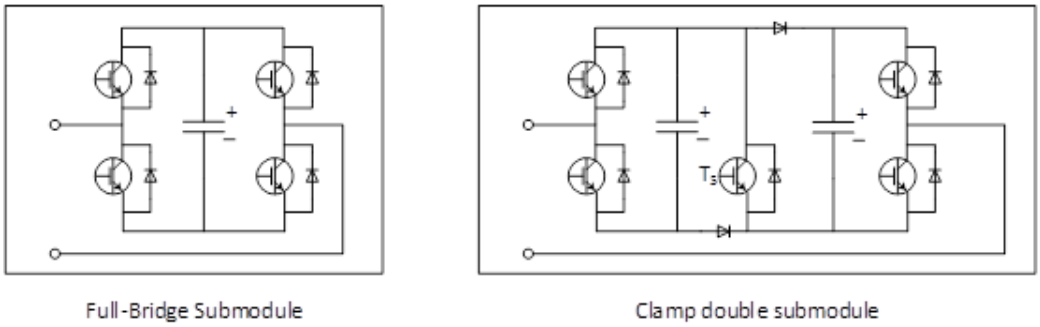


Figure 2.19: Three phase hybrid VSC topology [84]

Figure 2.19 shows the VSC, referred to here as The Parallel Hybrid Converter, first published in [84]. Each phase of the converter is constructed from an H-bridge in parallel with half-bridge sub-modules. The series-string of half-bridges are operated as to produce the rectified target AC voltage, this waveform is then unfolded using the H-Bridge valves which are soft



(a) One phase of MMC with half-bridge sub-module [65]



(b) sub-module of Full-Bridge and Clamp-Double [66, 67]

Figure 2.18: Topologies of MMC converter

switched at fundamental frequency. On the DC side, the three phases are connected in series such that rectified phase voltage sums. The addition of triplen harmonics can be used to decouple the AC and DC side voltage to avoid PWM of the H-Bridge valve which sits in the main power path [84, 85]. The summation of the rectified sinusoids results in 6n harmonics on the DC bus, further injection of triplen harmonics can be used to eliminate these harmonics [86]. This technique has been extended in [87] to produce a smooth DC output voltage.

The advantages of this topology are that the loss is very low, between 0.85 to 1.2% [85, 88], and reduced sub-module size and number.

The IGBT reverse blocking diodes in both the sub-modules and the H-Bridge mean DC-Link voltage reversal will result in the conduction of these devices. Additionally the published triplen harmonic injection technique that allows decoupling of the AC and DC side magnitudes has a maximum range that would be exceeded in DC voltage depressions.

Two level inverter with Multi-Level Series Active Filter

The topology depicted in Figure 2.20 was first proposed for HVDC applications in [89] and further published in [90].

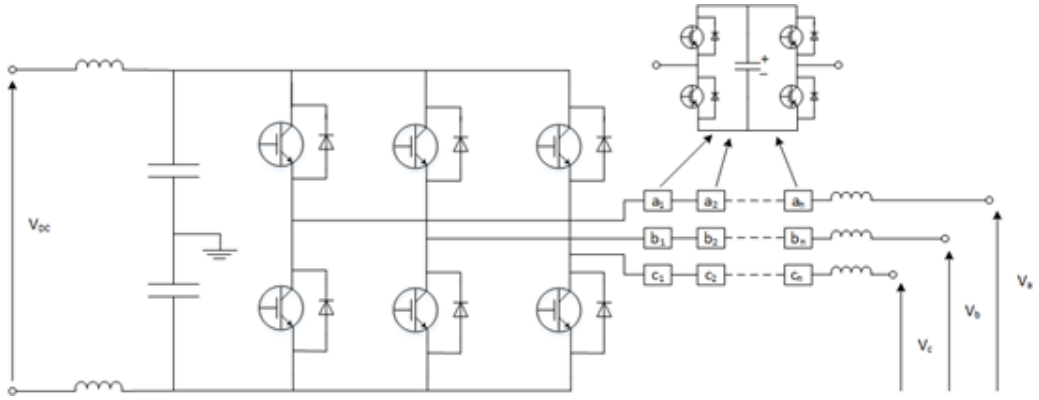


Figure 2.20: Hybrid converter topology [89]

The converter is operated by low frequency hard switching of the inverter IGBTs. The output is then actively filtered using full-bridge sub-modules [90].

Advantages of this topology include, AC fault ride through, both symmetrical and asymmetrical AC faults [90], it has been proposed in literature that a smaller size sub-module capacitance could be used than in the MMC [90].

The inclusion of AC full bridge sub-modules allow DC fault ride through of depressed DC bus voltages without conduction of the two level inverter anti-parallel diodes [90]. In the case of negative DC voltages the inverter diodes still begin to conduct for the duration of the negative fault. However unlike a standard 2-level inverter the full bridge modules allow the AC network to be decoupled from the DC fault.

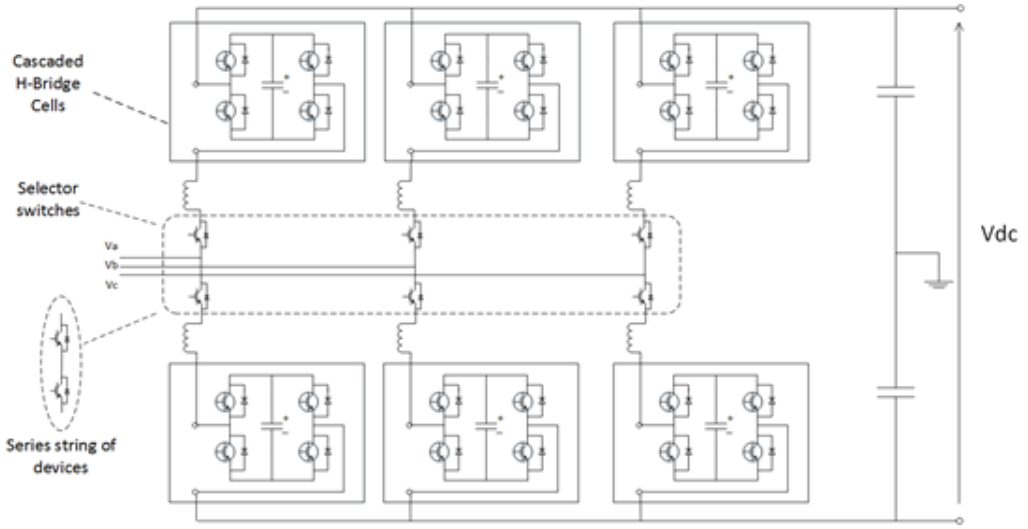


Figure 2.21: Alternate-Arm Multilevel converter topology

Alternate-Arm Multilevel (AAC) converter

The Alternate-Arm Multilevel converter (AAC) was first proposed in [89] and more extensively published in [91–96], is depicted in Figure 2.21. In this hybrid topology, a series string of IGBTs are connected in series with a series string of full-bridge sub-modules to form a converter arm. The addition of the series string of IGBTs, referred to as the director switch, enables the arm to be switched off for approximately half of a fundamental period. Doing so allows the positive and negative half cycles to be generated by the upper and lower arm respectively, such that the available voltage requirement for the arm is approximately halved with respect to the MMC, thus the number of sub-modules required is reduced [93].

The action of switching each arm in and out at fundamental frequency has the effect of rectifying the current into the DC-Link such that a DC filter is

required to prevent un-wanted DC current harmonics [91, 93]. Additionally the circuit must be operated around a sweet spot for optimal performance [93]. This sweet spot voltage requires the converter to over-modulate such that full-bridge sub-modules are required. The use of full-bridge sub-modules gives the circuit inherent DC fault blocking capability and allows it operate during DC faults [91].

2.4 HVDC grids DC side faults

DC side faults management is critical for HVDC grid transmission. DC faults can be classified as temporary and permanent dependent on the fault clearance time. Temporary faults usually happen on overhead lines due to lightning, the converter can recover after the DC fault is cleared. Permanent faults usually happen to cables as them need a long time to repair. Since this thesis focuses on converter operation after a permanent DC side fault occurs, the background of HVDC cables and proposed fault management schemes will be briefly introduced.

2.4.1 Background to HVDC cables

HVDC cable systems include three parts: cable, joint and end terminations. The joint is used to connect cables to reach the desired length. The end termination is used to reduce the electrical stress at the end of the cable to provide adequate electrical and mechanical properties [97]. Presently there are

mainly two types of cable used for HVDC VSC systems: Mass-impregnated HVDC cables and Extruded HVDC Cable such as XLPE (self-contained fluid filled SCFF is also available, but not widely in use) [98, 99].

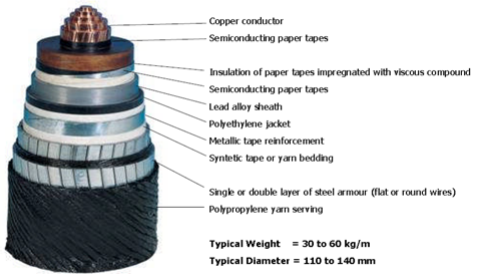


Figure 2.22: The structure of Mass-impregnated (MI) cable [100]

Mass-impregnated (MI) cable is also known as paper lapped cable. Figure 2.22 shows the structure of Mass-Impregnated cable. It uses paper tapes as the insulation [97, 101]. Currently this type of cable is mostly used because they have been in service for 40 years and are highly reliable. At present the rating is up to $\pm 600kV$ and $1800ADC$ [102]. The conductor size is typically up to $2500mm^2$.

Extruded cable is also known as polymeric cable. Figure 2.23 shows the structure of extruded cable. Extruded cables such as Cross-Linked Polyethylene (XLPE) cables are mainly used in Voltage Source Converter applications that allow the power flow to reverse without reversing the polarity [101, 103]. To date, this technology has been applied at voltages up to $\pm 320kV$ (in service with a power capacity of 800 MW) [104], and up to 525 kV, 2.6 GW extruded HVDC cable system has been developed [105].

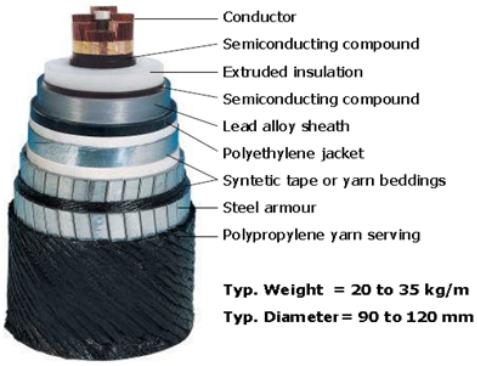


Figure 2.23: Structure of extruded cable [100]

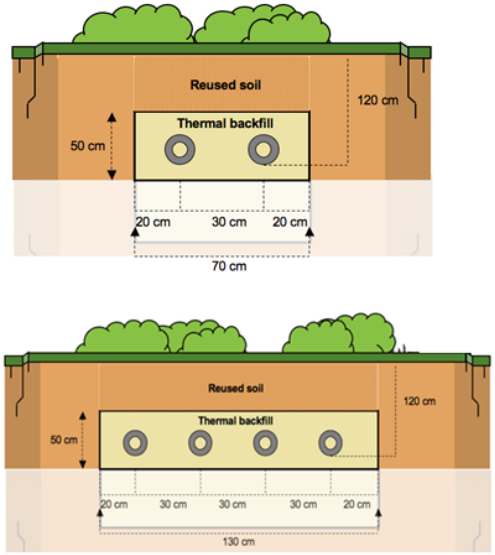


Figure 2.24: Upper: 1 Bipole HVDC system, 320kV, 1 GW lower: 2 Bipole HVDC system, 320kV, 2 GW [98]

Where HVDC cables are buried underground the cables are buried usually 1-1.5 meter deep and 1 meter wide, as shown in Figure 2.24 [98].

In submarine cable installations a distinction is made between shallow

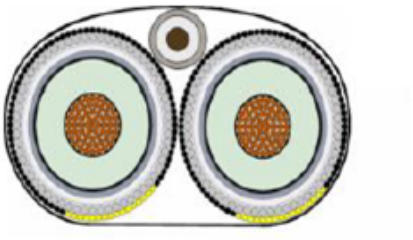


Figure 2.25: Two power and one optical cable in a bundle

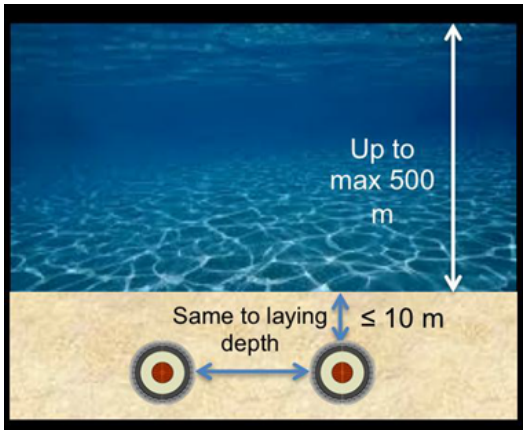


Figure 2.26: Submarine cable laying in shallow water [102]

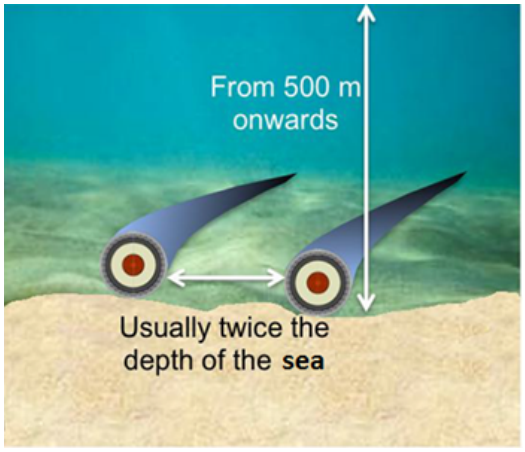


Figure 2.27: Submarine cable laying in deep water [102]

water cable lying (i.e. up to a maximum depth of 500m) and deep water cable lying. For cable systems in shallow waters, burial is mandatory to protect

the cable against the risk of damage from fishing gear and anchors [106–108]. The cable can be buried in bundle configuration (as shown in Figure 2.25) or individually. When buried individually, the distance between the cables will be at least the water depth (Figure 2.26). In deep water, the threat of anchors is no longer exist, so a burial operation can be omitted. The distance between the cables is usually as great as twice the sea depth. As shown in Figure 2.27. The purpose of the large distance is avoiding overlapping when recover the cable from damage [102, 106].

2.4.2 DC circuit breaker

In order to manage DC side faults, various DC circuit breaker topologies have been proposed [109]. The difficulty for DC circuit breakers compared to AC circuit breakers is due to the absence of natural current zero crossings. The HVDC circuit breakers reported in the literature can be classified as resonant breaker, solid-state breaker and hybrid breaker [110, 111].

The resonant breaker has the advantage of low cost and low on state loss, but the drawback is that it is not fast enough [109, 110]. On the other hand, the solid-state breaker is fast enough however the on state loss is significant [110]. The hybrid breaker combines the merits of fast switching speed and comparatively low on state loss and appears to be more attractive than the other two [111].

Figure 2.28 shows the topology of a modular hybrid IGBT DC breaker. It was first proposed in 2011 [112]. In normal operation, all the current flows through a fast disconnector and auxiliary DC breaker. Since there is no current in main DC breaker, there is no power loss from the main breaker. After the DC fault occurs, there are three steps to stop the fault current.

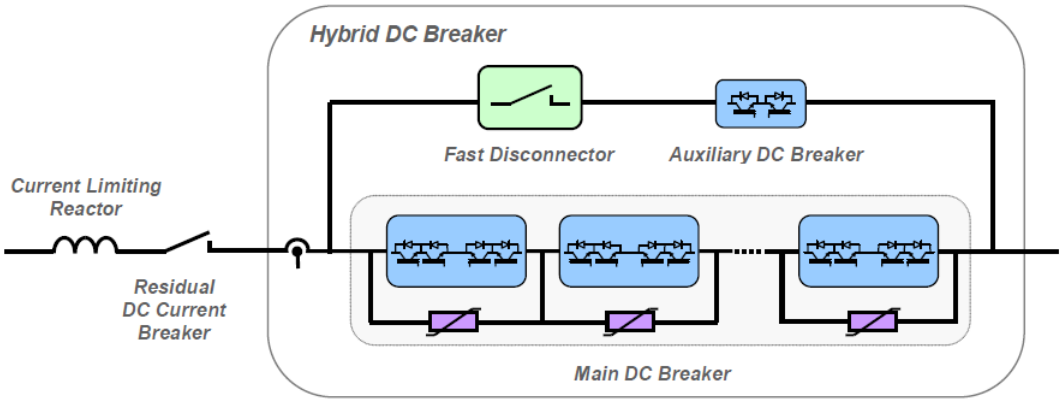


Figure 2.28: Topology of modular hybrid IGBT DC breaker [112]

First After the DC side fault is detected, the auxiliary DC breaker opens to direct the fault current flow through the main DC breaker.

Second The fast disconnector will open after the current flow through it is low enough.

Third the main DC breaker opens to cut-off the fault current

The DC circuit breaker breaks the current by generating a counter voltage larger than the system voltage. In [112], the main DC breaker is designed for larger than $1.5pu$ system DC voltage. As shown in figure 2.28, the main

DC breaker consists a large number of IGBTs due to the voltage rating requirement. This leads to high economic cost.

Besides DC circuit breakers, the converters with fault ride through capability are also able to block a DC side fault.

2.5 DC fault management with fault blocking converters

The DC side fault can be divided as temporary fault and permanent fault. The DC fault type depends on the transmission line. For cable transmission, the fault usually are permanent and require some time to repair. For overhead line transmission, most DC fault due to lightning strike or flash-over is temporary. So it is possible to bring the HVDC system back to operation quickly with reverse blocking converters.

The DC fault that occurs on overhead line is usually caused by lightning strikes. For this type of fault, the full-bridge sub-module can cut off the current by insert reversing voltage [113]. As stated before in section 2.3, some VSC topologies have the DC fault blocking capability. The converter will attempts restart multiple times (typically three times according to SIEMENS) after provide reverse voltage. As a result, the system availability can be increased.

The DC fault right through capability of AAC has been investigated in [93], where the simulation results shows that the AAC behave as a STATCOM during a temporary DC side fault and back to operation after the fault is cleared. In [90] the temporary solid pole-to-pole DC fault right through capability of Two level inverter with multi-level series active filter has been presented. Besides these two converter topologies, there are some new sub-module topologies has been proposed. In [66], a Clamp-Double Sub-module structure is given, as shown in figure 2.29; in [114], a half-bridge with double-thyristor-switch sub-module is presented, as shown in figure 2.30; in [115], a novel three-level cell topology is proposed, as shown in figure 2.31; in [116], a unipolar-voltage full-bridge sub-module and a three-level cross-connected sub-module are proposed, as shown in figure 2.32 and 2.33.

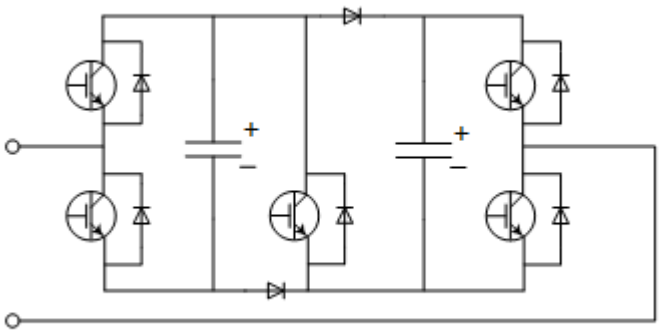


Figure 2.29: Structure of Clamp-Double Sub-module [66]

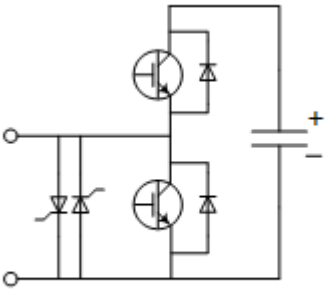


Figure 2.30: Structure of half-bridge with double-thyristor-switch sub-module [114]

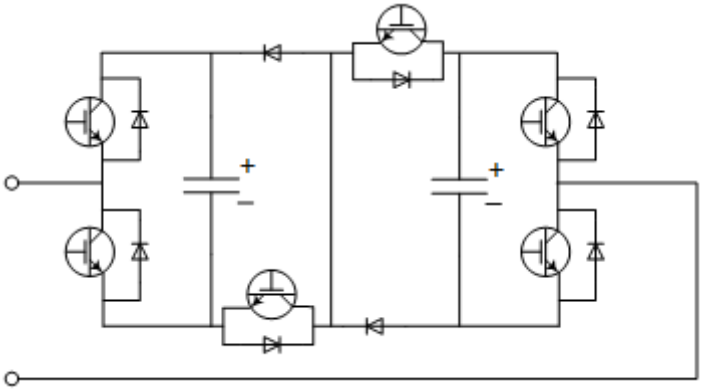


Figure 2.31: Structure of three-level cell [115]

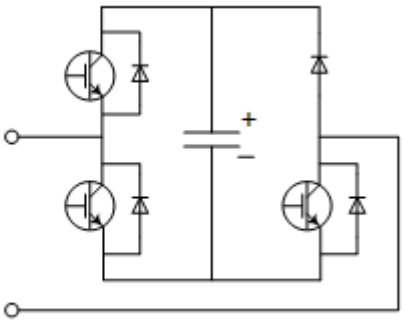


Figure 2.32: Structure of unipolar-voltage full-bridge sub-module [116]

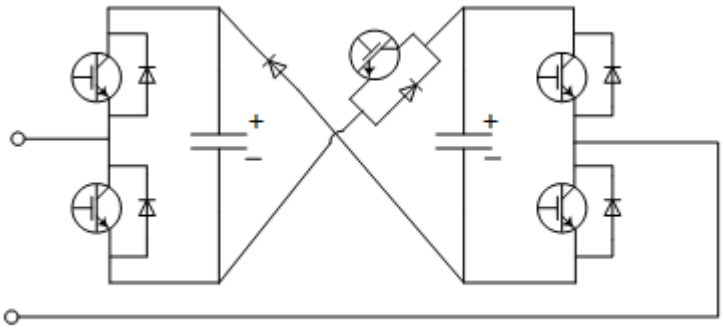


Figure 2.33: Structure of three-level cross-connected sub-module [116]

The above research mainly focus on the DC fault handling capability. The converters with fault blocking capability are able to back to operation after the fault is cleared. However, when the DC fault is permanent which is highly possible for cable transmission, it takes a long time to clear the fault. It would be an advantage if HVDC system can continue to operate under DC fault. [117] proposed a method to ensure the healthy DC network continue to operate by using additional DC passive components and novel converter control combined with mechanical DCCBs. In this thesis, the author proposes another method to keep the point-to-point HVDC system continue to operation under DC fault.

2.6 Summary

HVDC VSC system grid provides a viable solution for future bulk power transmission required due to the development of large renewable energy installation. The configuration of VSC converters can be classified into the fol-

lowing types, asymmetric monopole, symmetric monopole and bipole. The three types of HVDC system configuration can be connected together.

The topology of HVDC grid can be a mix of star, ring and mesh. The optimal topology depends on the terminal locations and power flow scenarios. Power flow of multi-terminal HVDC grid can be controlled by device or power flow control schemes. Published device power flow controller include thyristor power flow controller, DC/DC device and current flow controller. Published power flow control schemes include master-slave control, voltage margin control and voltage droop control.

Voltage Source Converter topologies consist of non-modular topology including two level converter, diode-clamped converter, floating capacitor converter; and modular topology including modular multilevel converter (MMC), parallel hybrid converter, two level inverter with multi-level series active filter and alternate arm multilevel converter (AAC). There are mainly two types of cable used for HVDC VSC systems: Mass-impregnated HVDC cables and Extruded HVDC cables such as XLPE. Hybrid IGBT DC breaker combines the merits of fast switching speed and comparatively low on state loss appears to be more attractive among various proposed HVDC circuit breaker topologies.

For temporary DC fault occurs on point-to-point or radical HVDC system, the converter with fault blocking capability could back to normal operation after the DC side fault is cleared. If the DC fault is permanent,

which is usually happened on cable transmission, one method of continuous operation of HVDC system is proposed in [117] with additional devices. For the point-to-point HVDC system with full-bridge MMC, it is possible to continue to operation under DC fault without additional components. In the following of this thesis, the operation methods of the point-to-point HVDC system continuous operation with the dc side fault is presented.

Chapter 3

DC fault ride through operation of a single full-bridge MMC converter

3.1 Introduction

The Modular Multilevel Converter (MMC) was first proposed by Prof. R. Marquardt in 2001 [118]. Since this time the topology has been adopted for commercial application by Siemens, ABB and Alstom Grid. The MMC has the following advantages over the two level inverter used in previous generation HVDC voltage source converters:

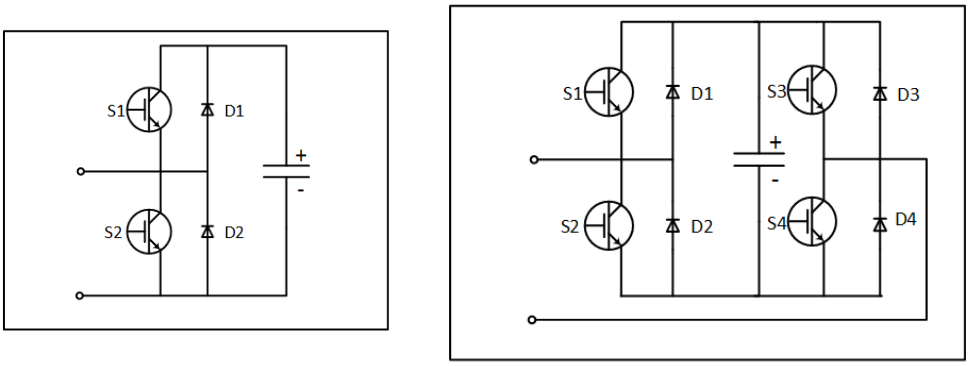
- Scalability, the modular structure of the MMC enables high voltages to be designed for by inserting large number of sub-modules;

- High power quality, the large number of sub-modules leads to a great number of voltage levels, therefore, the output voltage has low harmonic distortion and is able to meet the grid code without large AC harmonic filters;

- Low switching frequency, the modulation strategy for the MMC enables high quality waveforms to be produced while switching each sub-module close to fundamental frequency, reducing switching losses;

- High availability, due to the modular construction, MMC is able to insert redundant sub-modules in the converter arms, providing faulted sub-modules can be bypassed the MMC can continue to operate even if there is a sub-module failure.

There have been several variants of the MMC proposed, utilising alternative sub-modules. One approach is to use the half-bridge sub-module shown in Figure 3.2a. This sub-module voltage V_{sm} is able to produce two levels v_c and 0, where V_c is the sub-module capacitor voltage, thus an arm populated with just half bridge sub-modules is only able to produce a unipolar waveform and cannot respond to DC faults. Another approach uses the full-bridge sub-module shown in Figure 3.2b. This sub-module is able to produce 3 levels V_c,0 and $-V_c$. An MMC converter populated with full-bridge sub-modules is able to continue to produce the rated AC waveform for up to a complete reversal of the DC-Link voltage and as such it has a DC fault blocking response.



(a) Half-bridge sub-module

(b) Full-bridge sub-module

Figure 3.2: The structures of Modular Multilevel Converter sub-module

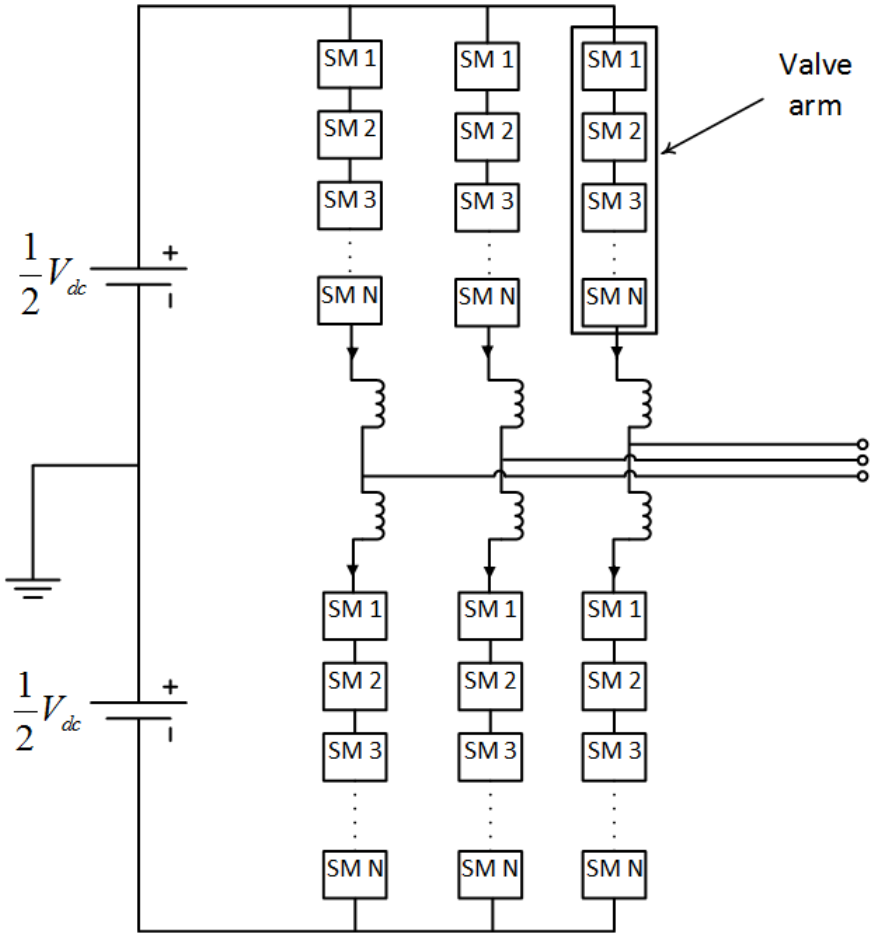


Figure 3.1: Modular Multilevel Converter structure

This chapter presents an analysis of DC fault responses for the MMC converter, initially normal operation is considered showing the approach needed to complete the analysis.

3.2 Normal operation of standard MMC converter

The MMC converter topology is shown in figure 3.1. It uses a modular structure where each arm is populated with sub-modules. In this thesis only the half-bridge and full-bridge sub-modules variants are considered; the structure of these sub-modules are shown in figure 3.2a and 3.2b respectively. Alternative sub-modules have been proposed in [66, 67], but are not considered in this work. The available states of the sub-module are shown in table 3.1 and 3.2; by correct modulation of these sub-module states the converter can be controlled to produce both an AC waveform at the AC terminals of the converter and a DC voltage at the DC bus.

Table 3.1: Control states of half-bridge sub-module

S1	S2	V_{sm}	operating state
ON	OFF	$+V_c$	1
OFF	ON	0	2

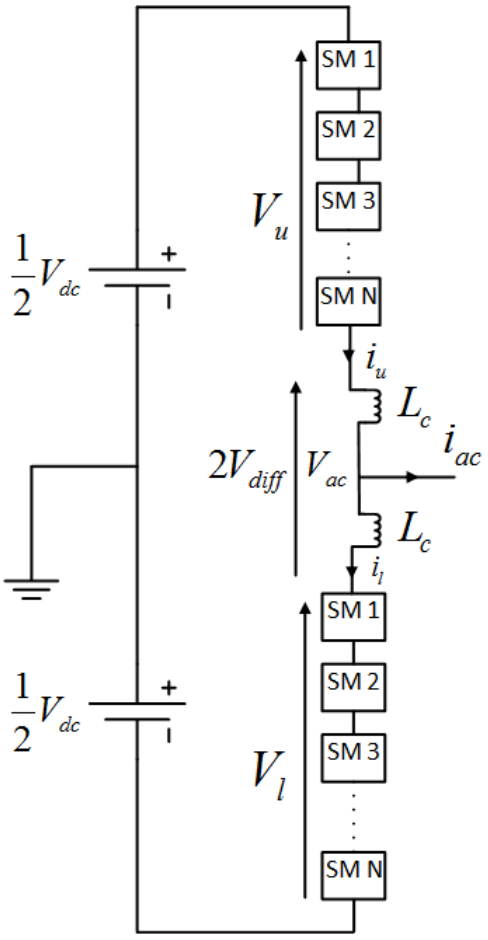


Figure 3.3: One single phase MMC structure

Table 3.2: Control states of full-bridge sub-module

S1	S2	S3	S4	V_{sm}	operating state
ON	OFF	OFF	ON	$+V_c$	1
ON	OFF	ON	OFF	0	2
OFF	ON	OFF	ON	0	3
OFF	ON	ON	OFF	$-V_c$	4

$$V_u = \frac{1}{2}V_{dc} - V_{ac} - L_c\frac{di_u}{dt} \tag{3.1}$$

$$V_l = \frac{1}{2}V_{dc} + V_{ac} - L_c\frac{di_l}{dt} \tag{3.2}$$

$$V_{dc} = V_u + V_l + L_c\frac{di_u}{dt} + L_c\frac{di_l}{dt} \tag{3.3}$$

$$V_{ac} = \frac{1}{2}(V_l - V_u) \tag{3.4}$$

The DC converter voltage is produced by the sum of inserted sub-modules in both the upper and lower arms; conversely the target AC voltage is given by the difference in upper and lower arm voltage. Thus equations (3.1) to (3.4) can be used to derive the required upper and lower arm voltages V_u, V_l

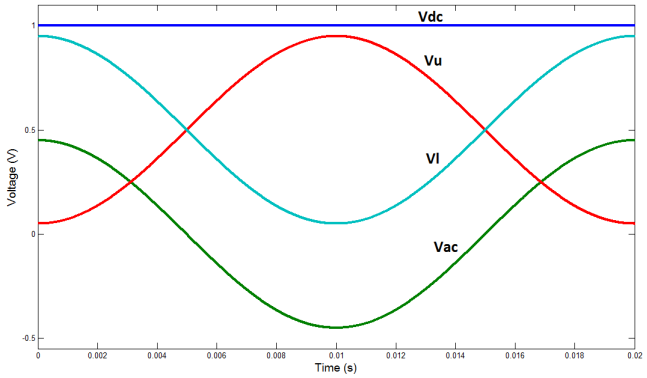


Figure 3.4: The voltage relations of V_{dc}, V_{ac}, V_u and V_l

as shown in figure 3.3. The voltage and current in the equations are instantaneous value. Figure 3.4 illustrates these characteristics. It shows that the maximum arm voltage will be the DC voltage V_{dc}, so that if there are N sub-modules in one arm, the capacitor voltage V_c should be at least be V_{dc}/N. It also shows that the amplitude of AC voltage V_{ac} can not be larger than $\frac{V_{dc}}{2}$.

The target inserted voltage can be achieved using a modulation technique such as in-phase disposition (IPD) level shifted modulation or phase shift modulation [77, 82, 119–121] to control the number of inserted sub-modules. An insertion index of the upper and lower arms, n_u,n_l, between -1 and 1 is defined here, to describe the number of inserted sub-module numbers N_u,N_l as a fraction of the total number available, N; negative numbers are used to represent sub-modules producing negative voltages. Although only a discrete number of levels are available it is assumed here that the number of sub-modules and so available levels of the converter is great enough that this index can be considered continuous.

$$n_u = N_u/N$$

$$n_l = N_l/N$$

Ideally, the sum of inserted upper and lower arm capacitors voltages should be equal to DC voltage, assuming that the ripple of capacitor voltage is small, then

$$\sum V_{cu} \approx \sum V_{cl} \approx V_{dc}$$

Where V_{cu},V_{cl} are the upper and lower arm sub-module capacitor voltage.

The power pulsation in each of the arms, arising from the interaction of the arm voltage and the arm current, results in a deviation in the bulk energy stored in the sub-module capacitors. In order that there is sufficient available voltage to meet the target required voltage demand, the capacitors must be selected appropriately based on the inequality shown in (3.5). As will be discussed in the next section this energy deviation can result in DC harmonic circulation if the insertion index of upper and lower arm n_u, n_l are not compensated for appropriately.

$$
\begin{aligned}
n_u &= \frac{\frac{1}{2}V_{dc} - V_{ac}^{ref} - V_{diff}^{ref}}{\sum V_{cu}} \\
&\approx \frac{\frac{1}{2}V_{dc} - V_{ac}^{ref} - V_{diff}^{ref}}{V_{dc}} \\
n_l &= \frac{\frac{1}{2}V_{dc} + V_{ac}^{ref} - V_{diff}^{ref}}{\sum V_{cl}} \\
&\approx \frac{\frac{1}{2}V_{dc} + V_{ac}^{ref} - V_{diff}^{ref}}{V_{dc}}
\end{aligned}
\tag{3.5}
$$

3.2.1 Steady state analysis of MMC converter

Analysis of the limb current in the MMC converter is not trivial and there are several published methods for doing so [122–124]. Here methods of estimating the arm current are discussed assuming harmonic suppression techniques are not used. These methods can be classified into two types based on the assumptions used. The first approach [122] assumes all the limb current harmonics exist. The second method [123] assumes the second harmonic in the limb current is fixed to a particular value; this can be achieved by appropriate control of the insertion index. It is a reasonable assumption since the second harmonic is the most significant component [78, 122, 125, 126].

The first method [122] assumes that the arm currents I_u,I_l contain one third dc current I_{dc}, half ac current I_{ac} and all orders of harmonics I_n, also the switching function only contains dc and fundamental frequency components, as shown in equation (3.6)(3.7). Under the ideal situation, where all the

sub-modules capacitor voltage in one arm are the same, the upper and lower arm voltage V_u,V_l can be calculated as the multiplication of the switching function, sub-module numbers in one arm and sub-module voltage as shown in equation (3.8).

$$\begin{aligned} I_u &= \frac{1}{3}I_{dc} + \frac{1}{2}I_{ac} + \sum_{n=1}^{\infty} I_n \\ I_l &= \frac{1}{3}I_{dc} - \frac{1}{2}I_{ac} + \sum_{n=1}^{\infty} I_n \end{aligned} \tag{3.6}$$

where $I_n = \hat{i_n}\cos(n\omega t + \phi_n)$, $I_{ac} = \hat{i_{ac}}\cos(\omega t + \phi_{ac})$

$$\begin{aligned} n_u &= \frac{1}{2}(1 - m\cos(\omega t)) \\ n_l &= \frac{1}{2}(1 + m\cos(\omega t)) \end{aligned} \tag{3.7}$$

$$\begin{aligned} V_u &= n_u \times N \times V_{cu} \\ &= N n_u \frac{1}{C}\int i_{cu} dt \\ &= N n_u \frac{1}{C}\int n_u I_u dt \\ V_l &= N n_l \frac{1}{C}\int n_l I_l dt \end{aligned} \tag{3.8}$$

The relationship between the phase-leg voltage V_{ph}= $V_u + V_l$ and the arm current is described by equation (3.9), where C is the sub-module capacitance

and i_{cu} is the current flow through the sub-module capacitor.

$$V_{ph} = V_u + V_l = \frac{N}{C}(n_u \int n_u I_u dt + n_l \int n_l I_l dt) \tag{3.9}$$

Inserting (3.6) and (3.7) into (3.9) gives

$$\begin{aligned}
\frac{2CV_{ph}}{N} =& \frac{2C(V_u + V_l)}{N} \\
=& \int (n_u I_u + n_l I_l)dt - m\cos(\omega t)\int (n_u I_u - n_l I_l)dt \\
=& \int (\frac{1}{3}I_{dc} + \sum_{n=1}^{\infty} I_n - m\frac{1}{2}I_{ac}\cos(\omega t))dt \\
& - m\cos(\omega t)\int (\frac{1}{2}I_{ac} - m\frac{1}{3}I_{dc}\cos(\omega t) - m\cos(\omega t)\sum_{n=1}^{\infty} I_n)dt
\end{aligned} \tag{3.10}$$

In equation (3.10), integral terms on right side should be zero, otherwise the phase-leg voltage will increase or decrease with time. This constraint determines the relation between the DC current I_{dc} and AC current I_{ac} to be:

$$I_{dc} = \frac{3m\hat{i_{ac}}}{2}\cos(\phi_{ac}) \tag{3.11}$$

Using f_n represents the nth harmonic in the right side of equation (3.9). Let f represent fundamental frequency, then $f_n = n * f$. V_n represents the nth harmonic of phase-leg on the left side, then

$$f_n = \frac{2C}{N} V_n \tag{3.12}$$

Equation (3.12) can be described by two Matrix equations. There is a general solution for these matrix equations which is given in detail in [122]. It is worth noting that two conclusions based on the general solution can be drawn. 1) there are no odd harmonics; 2) the second harmonic is directly proportional to the amplitude of the ac current, and for a given AC current magnitude, the second harmonic is reduced when there is only active power.

The second harmonic can be estimated with the assumption that the dc side is a constant voltage source and the 4th harmonic is much smaller than the second one. The estimation equation is given in (3.13).

$$i_2 = \mathrm{Re}\{\frac{-j(\frac{1}{2}\hat{i_{ac}}\frac{3m}{4\omega}e^{j\phi_{ac}} - \frac{m^2 I_{dc}}{2\omega})}{\frac{2C}{N}(j2\omega L_C + R) - j\frac{6+4m^2}{12\omega}} e^{j2\omega t}\} \tag{3.13}$$

As has been demonstrated in the first limb current analysis method, it is reasonable to consider the second harmonic is the dominant harmonic, as also described in [78, 122, 125, 126]. The second method [123] takes advantage of this fact and assumes the arm current only contains the second harmonic, besides the fundamental ac and dc current. The switching function only contains the fundamental frequency as in the first method. These assumptions

are described in (3.14) and (3.7)

$$\begin{aligned} I_u(t) &= \frac{1}{3}I_{dc} + \frac{1}{2}\hat{i_{ac}}\sin(\omega t + \phi_{ac}) + \hat{i_2}\sin(2\omega t + \theta) \\ I_l(t) &= \frac{1}{3}I_{dc} - \frac{1}{2}\hat{i_{ac}}\sin(\omega t + \phi_{ac}) + \hat{i_2}\sin(2\omega t + \theta) \end{aligned} \tag{3.14}$$

The phase-leg voltage $V_{ph} = V_u + V_l$ can be calculated by substituting (3.9). The resultant equation can be considered to have a mean or DC component and a ripple component containing AC harmonics. If it is assumed that the converter is operated such that the average sub-module voltage is given by $\frac{V_{dc}}{N}$, then the DC mean value will be given by V_{dc}. The AC component is represented here by ΔV_{ph}.

$$V_{ph} = V_u + V_l = V_{dc} + \Delta V_{ph} \tag{3.15}$$

Using $\Delta V_{ph}^{(2)}$ to represent the second harmonic voltage in the ΔV_{ph}, it can be derived from (3.9). It should correspond with the second harmonic current in (3.14). Then (3.16) is obtained to derive the second harmonic current. The second harmonic is calculated as equation (3.17), and the voltage ripple can also be calculated once the second harmonic current is known.

$$\hat{i_2}\sin(2\omega t+\theta) = -\frac{\Delta V_{ph}^{(2)}}{j2\omega 2L_C} \tag{3.16}$$

$$\begin{aligned} \hat{i_2} &= \frac{\sqrt{(A\cos\varphi + B)^2 + (A\sin\varphi)^2}}{1 - \dfrac{N}{16\omega^2 CLc} - \dfrac{m^2 N}{24\omega^2 CLc}} \\ \theta &= \arctan(A\cos\varphi + B, -A\sin\varphi) \end{aligned} \tag{3.17}$$

where

$$A = \frac{3}{64}\frac{mN\hat{i_{ac}}}{\omega^2 CLc}, B = -\frac{N}{48}\frac{m^2 i_{dc}}{\omega^2 CLc}$$

Of the arm current analysis methods presented, the first method is more complex providing an estimate of all harmonics in the arm, as the second harmonic has been found to be the dominant harmonic the second method presented provides a sound estimation without the extra complexity.

3.2.2 Energy deviation in limb

The energy deviation W_u,W_l in the limb can be calculated as (3.18), where P_u,P_l are the power flow through the upper and lower arms. These equations are general and do not take into account the method used for limb current calculation; however the accuracy of the result will be determined by the method used.

$$
\begin{aligned}
W_u &= \int P_u = \int V_u I_u \\
W_l &= \int P_l = \int V_l I_l
\end{aligned}
\tag{3.18}
$$

According to fig 3.3, the total energy in the upper and lower arm can be calculated as equation (3.19). The arm current is replaced by an AC current and circulating current I_{diff}; and the arm voltage is replaced by a DC voltage, AC voltage and the voltage across the arm inductor V_{diff}, L_c represents the arm inductor.

$$
\begin{aligned}
\frac{d\sum W_u}{dt} &= V_u I_u = (\frac{1}{2}V_{dc} - V_{ac} - V_{diff})(\frac{1}{2}I_{ac} + I_{diff}) \\
\frac{d\sum W_l}{dt} &= V_l I_l = (\frac{1}{2}V_{dc} + V_{ac} - V_{diff})(-\frac{1}{2}I_{ac} + I_{diff})
\end{aligned}
\tag{3.19}
$$

Where

$$
\begin{aligned}
I_{diff} &= \frac{1}{2}(I_u + I_l) \\
V_{diff} &= L_c \frac{dI_{diff}}{dt}
\end{aligned}
\tag{3.20}
$$

Then the total energy of the upper and lower arm ΣW_C and energy difference between upper and lower arm ΔW_C are:

$$\frac{d\sum W_C}{dt} = (V_{dc} - 2V_{diff})I_{diff} - V_{ac}I_{ac} \tag{3.21}$$

$$\frac{d\Delta W_C}{dt} = -2V_{ac}I_{diff} + (\frac{1}{2}V_{dc} - V_{diff})I_{ac} \tag{3.22}$$

From inspection of equation (4.17), it can be seen that the dc component in the difference current, I_{diff}, causes the total stored energy in the capacitors $\sum W_C$ to increase or decrease depending on the sign. It can be further seen from equation 4.18 that the dc component in i_{diff} has no impact on the difference in the upper and lower stored energy. The fundamental frequency component in i_{diff} can cause a change in ΔW_C due to the $V_{ac}i_{diff}$ part. The $V_{diff}i_{ac}$ part also causes a change since i_{diff} and V_{diff} have the same frequency components. But $V_{diff}i_{ac}$ should be much smaller than $V_{ac}i_{diff}$. Thus dc component in i_{diff} can be used to control the total stored energy in one phase-leg, and an ac component in i_{diff} can regulate the difference between the upper and lower arm [80]. This will be discussed further in chapter 4.

In this thesis the MMC is operated such that the second harmonic current is eliminated using a proportional resonant (PR) controller. As a result, the arm voltage and current will be controlled to be the same as in equation (3.23), and the voltage across the arm inductor is considered to be very small. Assuming the voltage balance is fast enough, the sub-module capacitor voltage could be estimated accurately based on the power flow through the arm. Equations (3.24) to (3.28) demonstrate the steps.

$$
\begin{aligned}
V_u &= \frac{1}{2}V_{dc} - \hat{v_{ac}}cos(wt) \\
I_u &= \frac{1}{3}I_{dc} + \frac{1}{2}\hat{i_{ac}}cos(wt) \\
V_l &= \frac{1}{2}V_{dc} + \hat{v_{ac}}cos(wt) \\
I_l &= \frac{1}{3}I_{dc} - \frac{1}{2}\hat{i_{ac}}cos(wt)
\end{aligned}
\tag{3.23}
$$

Then the power flow through the upper arm will be:

$$
\begin{aligned}
P_u =& V_u \times I_u \\
=& \frac{1}{6}V_{dc}I_{dc} - \frac{1}{3}\hat{v_{ac}}I_{DC}cos(wt) \\
&+ \frac{1}{4}V_{dc}\hat{i_{ac}}cos(wt) - \frac{1}{4}\hat{v_{ac}}\hat{i_{ac}} \\
&- \frac{1}{4}\hat{v_{ac}}\hat{i_{ac}}cos(2wt)
\end{aligned}
\tag{3.24}
$$

The sum of DC components in 3.24 will be zero since the DC side power is equal to the AC side power, otherwise the voltage of sub-module capacitors would be unstable. The upper arm energy variation is the integration of the ac components of 3.24.

$$\begin{aligned}\Delta W_u &= \int P_u \\ &= -\frac{1}{3w}\hat{v_{ac}}I_{dc}sin(wt) \\ &\quad + \frac{1}{4w}V_{dc}\hat{i_{ac}}sin(wt) \\ &\quad - \frac{1}{8w}\hat{v_{ac}}\hat{i_{ac}}sin(2wt)\end{aligned} \tag{3.25}$$

For the lower arm

$$\begin{aligned}\Delta W_l &= \int P_l \\ &= \frac{1}{3w}\hat{v_{ac}}I_{dc}sin(wt) \\ &\quad - \frac{1}{4w}V_{dc}\hat{i_{ac}}sin(wt) \\ &\quad - \frac{1}{8w}\hat{v_{ac}}\hat{i_{ac}}sin(2wt)\end{aligned} \tag{3.26}$$

If it is assumed that the average voltage of the capacitor is v_0, then the total energy of the capacitor is

$$W(t) = \frac{1}{2}NCv_0^2 + \Delta W(t) \tag{3.27}$$

so that the capacitor voltages are equal to

$$v_c(t) = \sqrt{\frac{2(\frac{1}{2}NCv_0^2 + \Delta W(t))}{NC}} = \sqrt{v_0^2 + \frac{2}{NC}\Delta W(t)} \tag{3.28}$$

3.3 Operation with one faulted cable

According to a CIGRE report [106], the average time required to repair a faulted sub-marine cable is two months. In the case of off-shore power transmission the total disconnection of the HVDC link will impact the onshore power system. It would be an advantageous if transmission could continue to at least partially operate during the repair time.

This section describes post fault operation modes that allow power transfer during a pole to ground fault. First the post fault arrangement is considered, then methods of fault ride through are presented that enable continued power transfer. The methods that will be presented can be summarised in table 3.3.

Table 3.3: Different modes of operation

	V_{dc}	Available power	Cable stress	Transformer stress	Available voltage requirement
Norm Op	1pu	1pu	0.5pu	0pu	[0,1]pu
Fault Op1	1pu	1pu	1pu	0.5pu	[0,1]pu
Fault Op2	0.5pu	0.5pu	0.5pu	0.25pu	[-0.25,0.75]pu
Fault Op3	0.5pu	0.5pu	0.5pu	0pu	[-0.5,1]pu
Fault Op4	0.5pu	0.5pu	0.5pu	0.125pu	[-0.375,0.875]pu
Fault Op5	0.5pu	0.5pu	0.5pu	0.375pu	[-0.375,0.875]pu

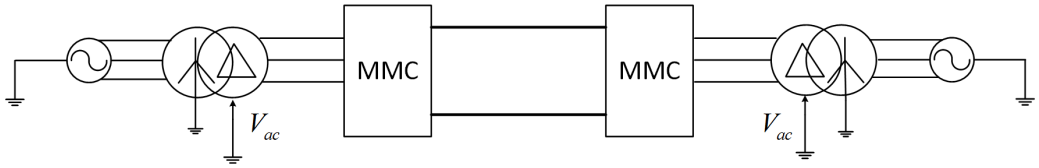
3.3.1 Post fault arrangement

The HVDC arrangement considered in this work is a symmetric monopole [127], ie, the station is formed from one converter with a positive and negative DC pole such that a fixed path is provided for the return current ; additionally the positive and negative DC poles are operated at $\pm\frac{1}{2}V_{dc}$.

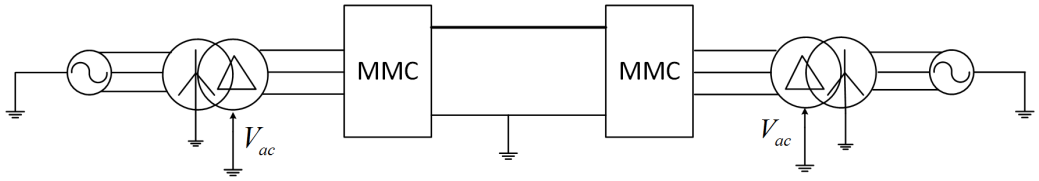
In the event of a fault that does not damage the cable conductor but only causes an insulation breakdown; such that the cable becomes permanently electrically connected ground then it would be possible to continue to operate at rated power. This is under the assumption that HVDC installation could stand the double rated voltage seen at the cable terminals. Additionally in the event of a complete conductor cut, it would be possible to isolate the cable and reconfigure to an asymmetric monopole arrangement provided a non-metallic ground return path could be temporarily provided. To enable this switch gear would have to be provided, however this would not have to break a DC fault, nor switch under load or high voltage. Figure 3.5 shows the pre fault arrangement and the two faulted arrangements.

If the station and line cannot be operated at the full HVDC voltage it is also possible that the same arrangements could be used but with the DC-Link voltage at $\frac{1}{2}V_{dc}$. In this way no extra voltage stress is seen at the cable terminals.

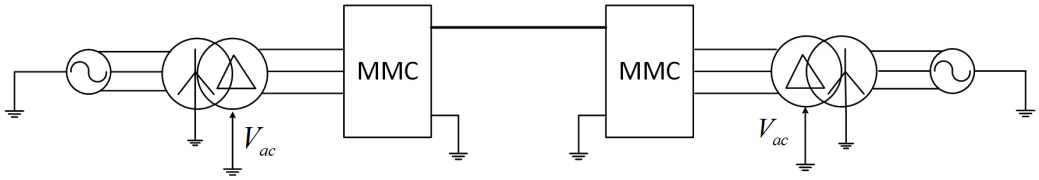
In the following sections pole to ground faults are considered and meth-



(a) The symmetric configuration of two MMC HVDC system



(b) The asymmetric configuration with metallic ground return



(c) The asymmetric configuration without metallic ground return

Figure 3.5: The reconfiguration of symmetric operation to asymmetric operation

ods of continuous faulted operation are presented, as it is arbitrary as to whether the fault occurs on the positive or negative pole; for convenience the DC fault is assumed to occur on the negative pole line.

Figure 3.6 shows the circuit structure of the steady state fault operation of the MMC after a line-to-ground fault on the negative pole. Since the DC side voltage is half rated voltage, and assuming that the cable current can not reach a higher value, the maximum power rating of faulted operation is half rated power.

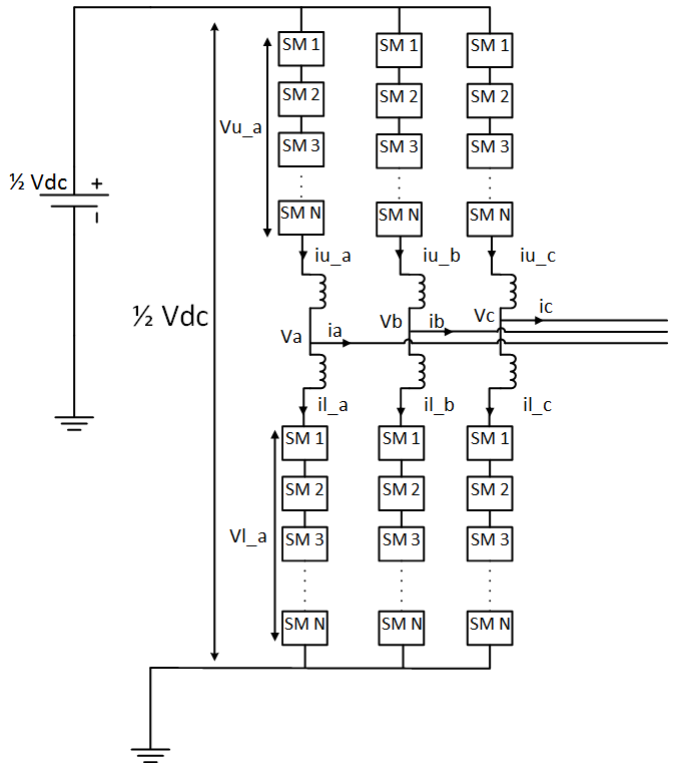


Figure 3.6: MMC fault operation circuit structure

3.3.2 Operation with extra voltage stress on the transformer

If it is assumed that the converter station and cable are able to support the additional DC voltage stress of the fault, then power transmission can continue at its rated value by floating the transmission system with the fault, that is one pole operates around $0PUV_{dc}$ with respect to earth and the other pole operate at $\pm 1PU$, which is referred to as Fault Op1 in table 3.3. If the installed cable is not able to tolerate such voltage, but the transformer is able to operate with $0.25PUV_{dc}$ DC voltage stress then 0.5 PU power transmission can continue.

When operating in this mode the active power could be freely separated between the upper and lower arm. As long as the DC side voltage is equal to $\frac{1}{2}V_{dc}$, the MMC is able to continue operating. Firstly assume there is only active power transmission. Defining the real power proportion on the upper arm as P_e, where $0 \leq P_e \leq 1$, then the lower arm real power proportion is $1 - P_e$.

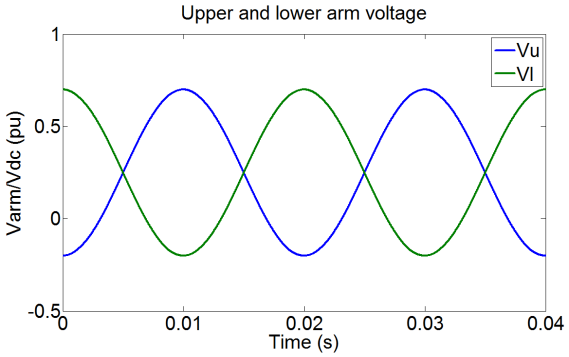
Assume that at this stage, the power factor is 1. The arm voltage and current are calculated as equation (3.29) and (3.30).

$$
\begin{aligned}
V_u &= P_e \times \frac{1}{2} V_{dc} - V_{ac} \\
V_l &= (1 - P_e) \times \frac{1}{2} V_{dc} + V_{ac}
\end{aligned}
\tag{3.29}
$$

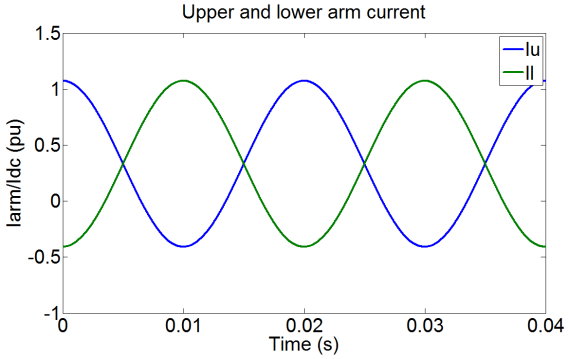
$$
\begin{aligned}
I_u &= \frac{1}{3} I_{dc} + P_e \times I_{ac} \\
I_l &= \frac{1}{3} I_{dc} - (1 - P_e) \times I_{ac}
\end{aligned}
\tag{3.30}
$$

When $P_e = 0.5$, which is referred to as Fault Op2 in table 3.3, the real power splits evenly between the upper and lower arms. Then the voltage and current of the two arms are symmetric, which leads to symmetric sub-module capacitor voltages, as shown in figure 3.7. Fault Op3 mode corresponds to operation when $P_e = 1$, Fault Op4 mode corresponds to operation when $P_e = 0.75$, and Fault Op5 mode to $P_e = 0.25$. As P_e can be freely chosen between $[0, 1]$, these value are selected to provide examples of how the cable stress and transformer stress and available voltage requirement relate to P_e.

Assume the reactive power proportion on upper arm is R_u, which is used to refer the percentage of reactive power proportion on upper arm. The range of R_u is $[0, 1]$. Using I_{real} and $I_{reactive}$ to represent the active and reactive current, then the arm current is equation (3.31). For instance if the reactive power is the same as active power, then the arm voltage and current are shown in figure 3.8.

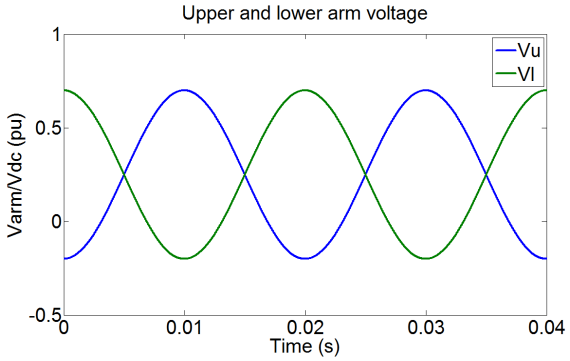


(a) The upper and lower arm voltage when $P_e = 0.5$

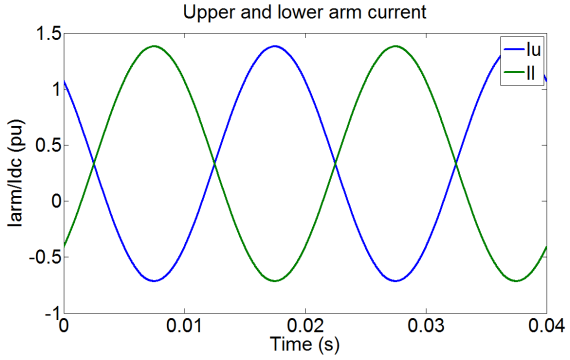


(b) The upper and lower arm current when $P_e = 0.5$

Figure 3.7: Arm voltage and current when $P_e = 0.5$, Fault Op2 mode



(a) The upper and lower arm voltage when $P_e = 0.5$ and $R_u = 0.5$



(b) The upper and lower arm current when $P_e = 0.5$ and $R_u = 0.5$

Figure 3.8: Arm voltage and current when $P_e = 0.5$ and $R_u = 0.5$

$$
\begin{aligned}
I_u &= \frac{1}{3} I_{dc} + P_e \times I_{real} \cos(wt) + R_u \times I_{reactive} \cos(wt + \frac{\pi}{2}) \\
I_l &= \frac{1}{3} I_{dc} - (1 - P_e) \times I_{real} \cos(wt) - (1 - R_u) \times I_{reactive} \cos(wt + \frac{\pi}{2})
\end{aligned}
\tag{3.31}
$$

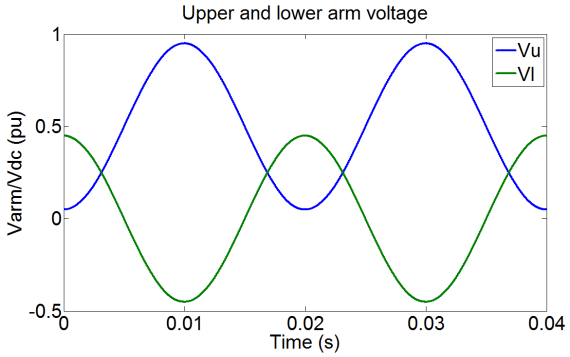
3.3.3 Operation with no additional voltage stress

In Fault Op3 where $P_e = 1$, the upper arm provides the same voltage as in normal operation and the lower arm provides the same as AC voltage. Under this asymmetric fault operation, all the AC current flows through the upper arm. As a result, the upper arm current consist of one third of the DC current and all of the AC current, the lower arm current consist of only one third of the DC current and no AC current. The corresponding arm voltage and current are shown in figure 3.9a.

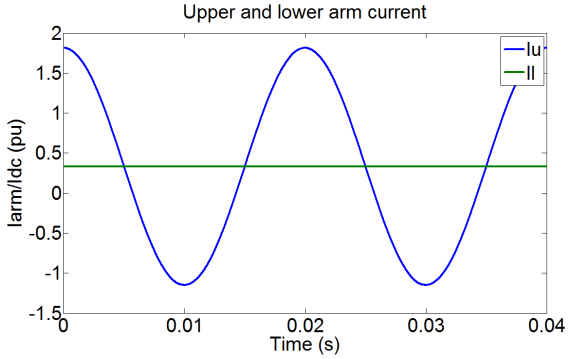
$$\begin{aligned} V_u &= \frac{1}{2}V_{dc} - V_{ac} \\ V_l &= V_{ac} \end{aligned} \tag{3.32}$$

$$\begin{aligned} I_u &= \frac{1}{3}I_{dc} + I_{ac} \\ I_l &= \frac{1}{3}I_{dc} \end{aligned} \tag{3.33}$$

The advantage of this operation mode is that there is no DC voltage stress on the AC side transformer. However, from the power loss aspect, this mode generates the most power loss, the details will be given in section 3.3.5.



(a) The upper and lower arm voltage when $P_e = 1$



(b) The upper and lower arm current when $P_e = 1$

Figure 3.9: Arm voltage and current when $P_e = 1$, Fault Op3 mode

3.3.4 Capacitor voltage estimation

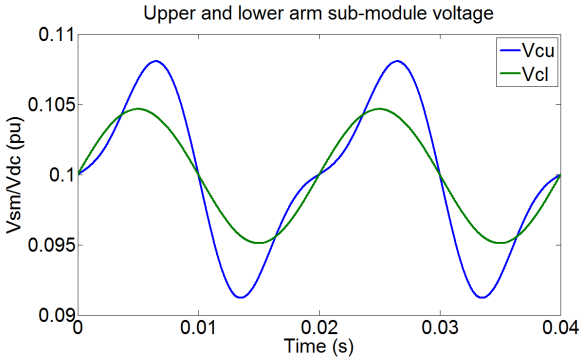
By using the same method that was applied for normal operation, the energy deviation for faulted operation can be calculated. As shown in figure 3.6, the power flow through the arm could be calculated by multiplying arm voltage and arm current. The calculation is given in equation (3.34) and (3.35).

$$\begin{aligned}
V_u =& P_e\frac{1}{2}V_{dc} - \hat{v_{ac}}\cos(wt) \\
I_u =& \frac{1}{3}I_{dc} + P_e\hat{i_{ac}}\cos(wt) \\
P_u =& \frac{1}{6}P_eV_{dc}I_{dc} - \frac{1}{3}\hat{v_{ac}}I_{dc}\cos(wt) \\
&+ \frac{1}{2}{P_e}^2V_{dc}\hat{i_{ac}}\cos(wt) - \frac{1}{2}P_e\hat{v_{ac}}\hat{i_{ac}} \\
&- \frac{1}{2}P_e\hat{v_{ac}}\hat{i_{ac}}\cos(2wt) \qquad (3.34) \\
\Delta W_u =& \int P_u \\
=& -\frac{1}{3w}\hat{v_{ac}}I_{dc}\sin(wt) + \frac{1}{2w}P_e^2V_{dc}\hat{i_{ac}}\sin(wt) \\
&- \frac{1}{4w}P_e\hat{v_{ac}}\hat{i_{ac}}\sin(2wt) \\
V_{cu} =& \sqrt{{V_{cuaverage}}^2 + \frac{2}{NC}\Delta W_u}
\end{aligned}$$

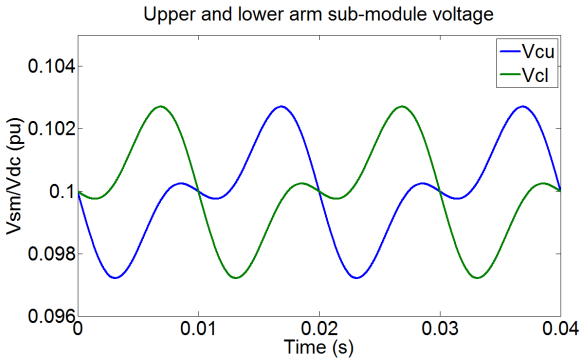
$$
\begin{aligned}
V_l =& (1-P_e)\,\frac{1}{2}V_{dc} + \hat{v_{ac}}\cos(wt) \\
I_l =& \frac{1}{3}I_{dc} - (1-P_e)\hat{i_{ac}}\cos(wt) \\
P_l =& \frac{1}{6}(1-P_e)V_{dc}I_{dc} - \frac{1}{3}\hat{v_{ac}}I_{dc}\cos(wt) \\
&+ \frac{1}{2}(1-P_e)^2 V_{dc}\hat{i_{ac}}\cos(wt) - \frac{1}{2}(1-P_e)\hat{v_{ac}}\hat{i_{ac}} \\
&- \frac{1}{2}(1-P_e)\hat{v_{ac}}\hat{i_{ac}}\cos(2wt) \qquad (3.35) \\
\Delta W_l =& \int P_l \\
=& \frac{1}{3w}\hat{v_{ac}}I_{dc}\sin(wt) - \frac{1}{2w}(1-P_e)^2 V_{dc}\hat{i_{ac}}\sin(wt) \\
&- \frac{1}{4w}(1-P_e)\hat{v_{ac}}\hat{i_{ac}}\sin(2wt) \\
V_{cl} =& \sqrt{{V_{claverage}}^2 + \frac{2}{NC}\Delta W_l}
\end{aligned}
$$

As shown in figure 3.10, the upper and lower capacitor voltages are asymmetric when $P_e = 1$ and $P_e = 0$, and symmetric when $P_e = 0.5$. Since the capacitor voltage is determined by the arm voltage and current, they are symmetric whenever the arm voltage and current are also symmetric. The main advantage of symmetric operation is that it produce the least power loss, which is explained in next subsection.

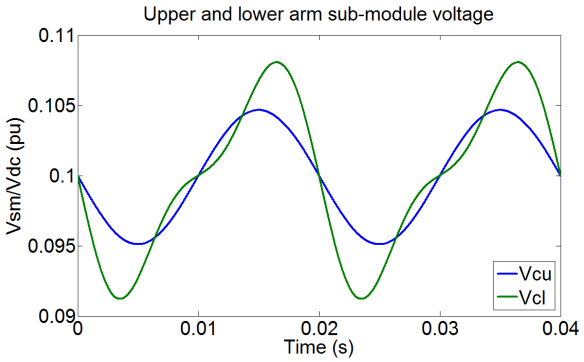
If we take the reactive power distribution into consideration, the complexity is doubled with another variable R_u. Nevertheless, the calculation method is the same. Equations (3.36) and (3.37) illustrate the capacitor voltage calculation with reactive power.



(a) the capacitor voltage when $P_e = 1$



(b) the capacitor voltage when $P_e = 0.5$



(c) the capacitor voltage when $P_e = 0$

Figure 3.10: The capacitor voltage estimation for different P_e value

$$
\begin{aligned}
V_u =& P_e\frac{1}{2}V_{dc} - V_{ac}cos(wt) \\
I_u =& \frac{1}{3}I_{dc} + P_eI_{real}cos(wt) + R_uI_{reactive}cos(wt+\frac{\pi}{2}) \\
P_u =& \frac{1}{6}P_eV_{dc}I_{dc} + \frac{1}{2}P_e^2V_{dc}I_{real}cos(wt) \\
& - \frac{1}{2}P_eR_uV_{dc}I_{reactive}sin(wt) - \frac{1}{3}V_{ac}I_{dc}cos(wt) \\
& - \frac{1}{2}P_eV_{ac}I_{real}cos(2wt) - \frac{1}{2}P_eV_{ac}I_{real} \\
& + \frac{1}{2}R_uV_{ac}I_{reactive}sin(2wt) \\
\Delta W_u =& + \frac{1}{2w}P_e^2V_{dc}I_{real}sin(wt) + \frac{1}{2w}P_eR_uV_{dc}I_{reactive}cos(wt) \\
& - \frac{1}{3w}V_{ac}I_{dc}sin(wt) - \frac{1}{4w}P_eV_{ac}I_{real}sin(2wt) \\
& - \frac{1}{4w}R_uV_{ac}I_{reactive}cos(2wt) \\
V_{cu} =& \sqrt{{V_{cuaverage}}^2 + \frac{2}{NC}\Delta W_u}
\end{aligned}
\tag{3.36}
$$

$$
\begin{aligned}
V_l =& P_e\frac{1}{2}V_{dc} + V_{ac}cos(wt) \\
I_l =& \frac{1}{3}I_{dc} - (1-P_e)I_{real}cos(wt) + (1-R_u)I_{reactive}cos(wt+\frac{\pi}{2}) \\
P_l =& \frac{1}{6}(1-P_e)V_{dc}I_{dc} - \frac{1}{2}(1-P_e)^2V_{dc}I_{real}cos(wt) \\
&+ \frac{1}{2}(1-P_e)(1-R_u)V_{dc}I_{reactive}sin(wt) + \frac{1}{3}V_{ac}I_{dc}cos(wt) \\
&- \frac{1}{2}(1-P_e)V_{ac}I_{real}cos(2wt) - \frac{1}{2}(1-P_e)V_{ac}I_{real} \\
&+ \frac{1}{2}(1-R_u)V_{ac}I_{reactive}sin(2wt) \\
\Delta W_l =& -\frac{1}{2w}(1-P_e)^2V_{dc}I_{real}sin(wt) - \frac{1}{2w}(1-P_e)(1-R_u)V_{dc}I_{reactive}cos(wt) \\
&+ \frac{1}{3w}V_{ac}I_{dc}sin(wt) - \frac{1}{4w}(1-P_e)V_{ac}I_{real}sin(2wt) \\
&- \frac{1}{4w}(1-R_u)V_{ac}I_{reactive}cos(2wt) \\
V_{cl} =& \sqrt{{V_{claverage}}^2 + \frac{2}{NC}\Delta W_l}
\end{aligned}
\tag{3.37}
$$

3.3.5 Best mode for partial power transmission from the power loss point of view

The power loss of an MMC mainly comes from the IGBTs. For the semiconductor devices, the power loss consists of conduction loss and switching loss. In both normal and faulted operation, each sub-module capacitor voltage of the MMC is controlled to stay at a certain mean voltage. Consequently, the power loss depends largely on the current flow through the device. Consider the magnitude of current as a function of the variables P_e and R_u, the minimum of the arm current magnitude can be calculated, and this point also

leads to the minimum power loss.

The power loss calculation detail is given in the Appendix. Based on the analysis, the best mode for partial power transmission is to equally separate the real power and reactive power between the upper and lower arms. The reason is that at this point the conduction loss is lowest and the switching loss for an MMC can be very small compared to the conduction loss due to the low switching frequency. The lowest conduction loss condition leads to the lowest total power loss of the MMC.

Figure 3.11 upper shows the semiconductor on-state characteristics. The on-state voltage is non-linear with current. In order to analysis the power loss, the an approximation is used to linearise the on-state voltage with current, as illustrated in Figure 3.11 lower [128]. The simplified conduction loss equation for calculating IGBT conduction loss P_{CT} and Diode conduction loss P_{CD} are:

$$\begin{aligned} P_{CT} &= V_{CE0} \times I_{Cav} + r_{0T} \times I_{Crms}^2 \\ P_{CD} &= V_{F0} \times I_{Dav} + r_{0D} \times I_{Drms}^2 \end{aligned} \tag{3.38}$$

According to I_u, I_l in equation (3.36) and (3.37),

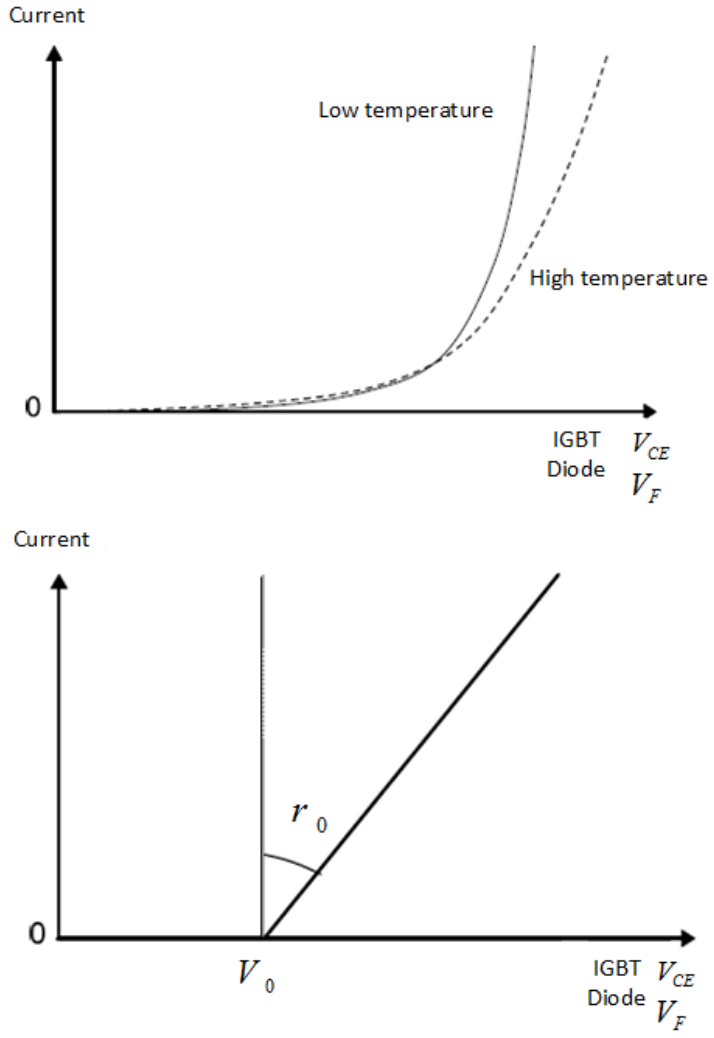


Figure 3.11: Typical IGBT and diode on-state characteristics: real (upper) and piecewise-linear approximation (lower) [128]

$$\begin{aligned} I_{Cav} &= I_{Dav} = \frac{1}{3} I_{DC} \\ I^2_{Crms} &= I^2_{Crms} = I^2_{urms} or I^2_{lrms} \end{aligned} \tag{3.39}$$

Since I_{DC} is a constant value independent of P_e, R_u, the conduction loss

P_{con} for one phase reach a minimum when $I^2_{urms} + I^2_{lrms}$ reaches a minimum. Separating the upper and lower arm into the dc component and ac component, then

$$\begin{aligned} I^2_{urms} &= I^2_{urmsDC} + I^2_{urmsAC} \\ I^2_{lrms} &= I^2_{lrmsDC} + I^2_{lrmsAC} \end{aligned} \tag{3.40}$$

Where,

$$\begin{aligned} I^2_{urmsDC} &= I^2_{lrmsDC} = (\frac{1}{3} I_{DC})^2 \\ I^2_{urmsAC} &= \frac{1}{2}[(P_e \times I_{real})^2 + (R_u \times I_{reactive})^2] \\ I^2_{lrmsAC} &= \frac{1}{2}[((1 - P_e) \times I_{real})^2 + ((1 - R_u) \times I_{reactive})^2] \end{aligned}$$

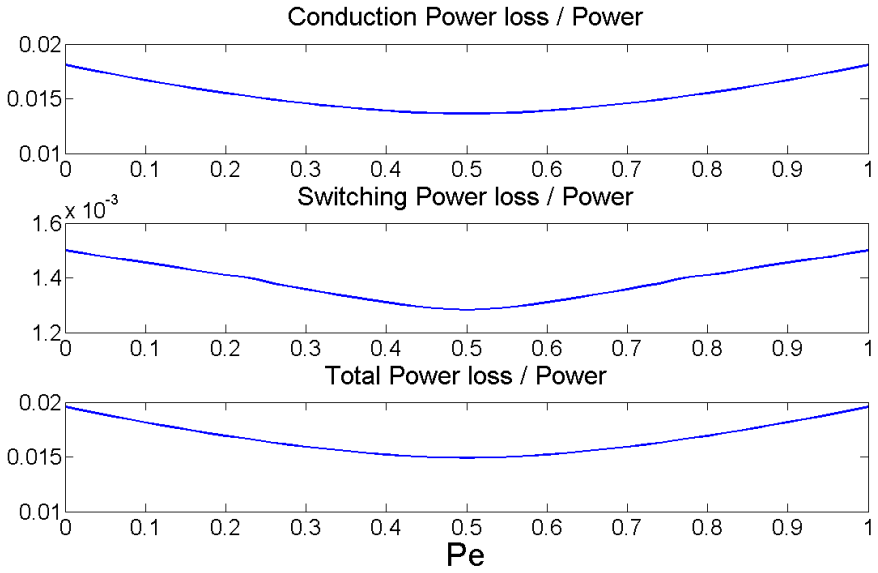
Based on the above equations, the conduction loss P_{con} for each phase reaches a minimum when $I^2_{urmsAC} + I^2_{lrmsAC}$ reaches a minimum. Letting $P_{cmin} = I^2_{urmsAC} + I^2_{lrmsAC}$, the minimum point can be calculated by using differentiation.

$$
\begin{aligned}
P_{cmin} &= I_{urmsAC}^2 + I_{lrmsAC}^2 \\
&= \frac{1}{2}[(P_e \times I_{real})^2 \\
&+ (R_u \times I_{reactive})^2 + ((1 - P_e) \times I_{real})^2 \\
&+ ((1 - R_u) \times I_{reactive})^2] \\
\frac{d}{P_e} P_{cmin} &= 0 \Rightarrow P_e = 0.5 \\
\frac{d}{R_u} P_{cmin} &= 0 \Rightarrow R_u = 0.5
\end{aligned}
\tag{3.41}
$$

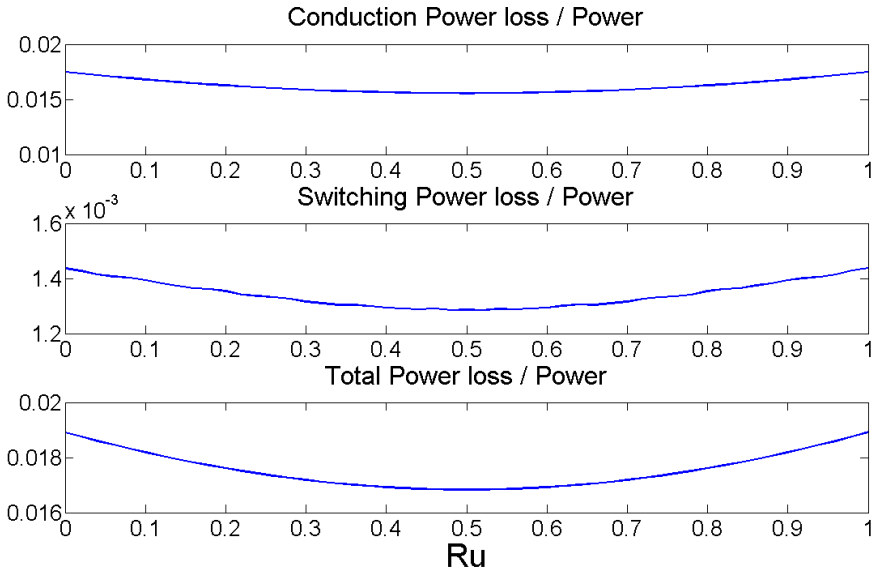
Table 3.4: Data used for power loss calculation

Parameters	Data from [129]
V_{dc}	$\pm 320kV$
V_{AC}	$333kV$
P	$1000MW$
Q	$350Mvar$
N	400

The power loss of a full-bridge MMC is calculated by using the MMC data from [129] as shown in table 3.4, the thermal data sheet from Mitsubishi Electric CM1200HG-66H and setting the carrier frequency to $1800Hz$. Figure 3.12 presents the conduction, switching and total power loss versus P_e and R_u. For P_e in figure 3.12 (a), the active power is $500MW$ and there is no reactive power. For R_u in figure 3.12 (b), the active power is $500MW$ and the reactive power is $Q = 350Mvar$. This figure demonstrates that the conduction loss is a minimum when $P_e = 0.5$ and $R_u = 0.5$, as expected. Unlike conduction loss, the switching loss line is not a continuous function,



(a) Power loss calculation when $P = 500MW, Q = 0, N = 400$



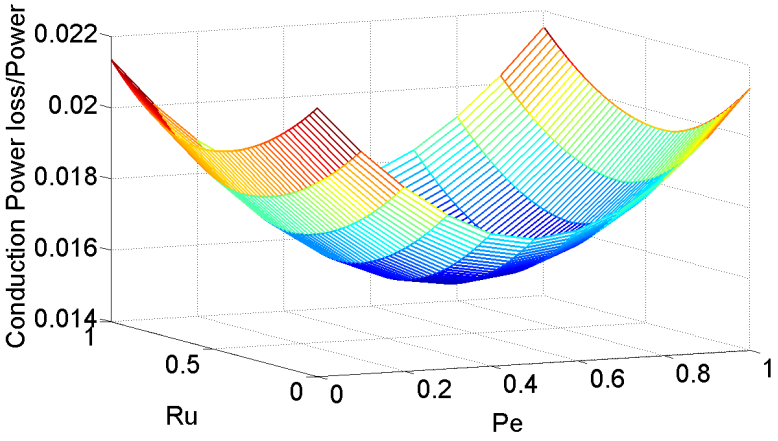
(b) Power loss calculation when $P = 500MW, Q = 350Mvar, N = 400, Pe = 0.5$

Figure 3.12: The power loss calculation

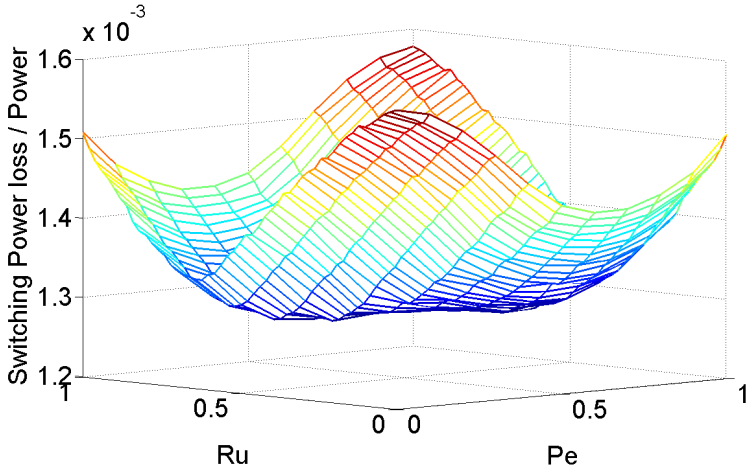
since the switching function is non-linear.

A 3D figure of power loss vs P_e, R_u is shown in Figure 3.13. It illustrates that the conduction loss and total power loss is minimum when $P_e = 0.5, R_u = 0.5$. The switching loss is not clearly shown, but the minimum is clearly near the centre. Based on the above analysis, from the power loss aspect, the best mode for partial power power transmission is when $P_e = 0.5, R_u = 0.5$.

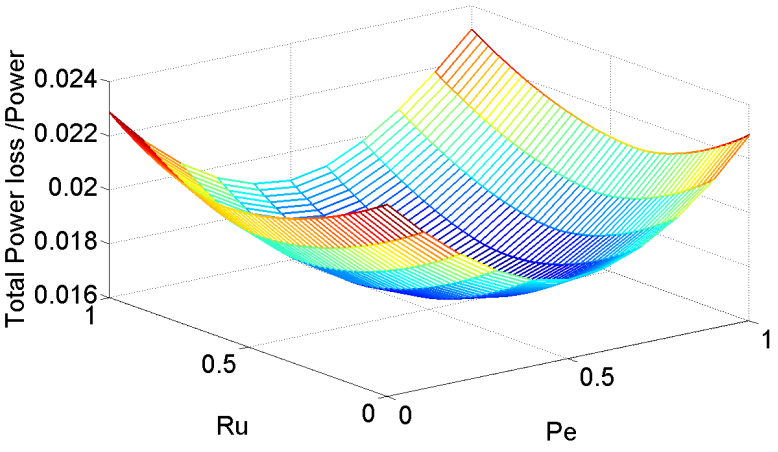
Note that post fault operation does not increase losses in the system, so that there is no requirement of additional device or cooling. Meanwhile, since the arm current is no bigger than in normal operation, the capacitor voltage ripple is no bigger than before. As a result, no extra rating required for sub-module capacitor.



(a) Conduction loss when $P = 500MW, Q = 350Mvar$



(b) Switching loss when $P = 500MW, Q = 350Mvar$



(c) Total Power loss when $P = 500MW, Q = 350Mvar$

Figure 3.13: The 3D power loss illustration

3.4 Operation with pole-to-pole fault

Although a line-to-line fault hardly ever happens, the full-bridge MMC could operate as a STATCOM in this condition. A Full-bridge MMC can continue to provide reactive power to the AC side. In figure 3.14, the circuit of the MMC after a line-to-line fault is presented. The DC side of the MMC is short circuited and directly connect to ground, On the AC side the converter continue is unchanged but the real power demand is set to zero.

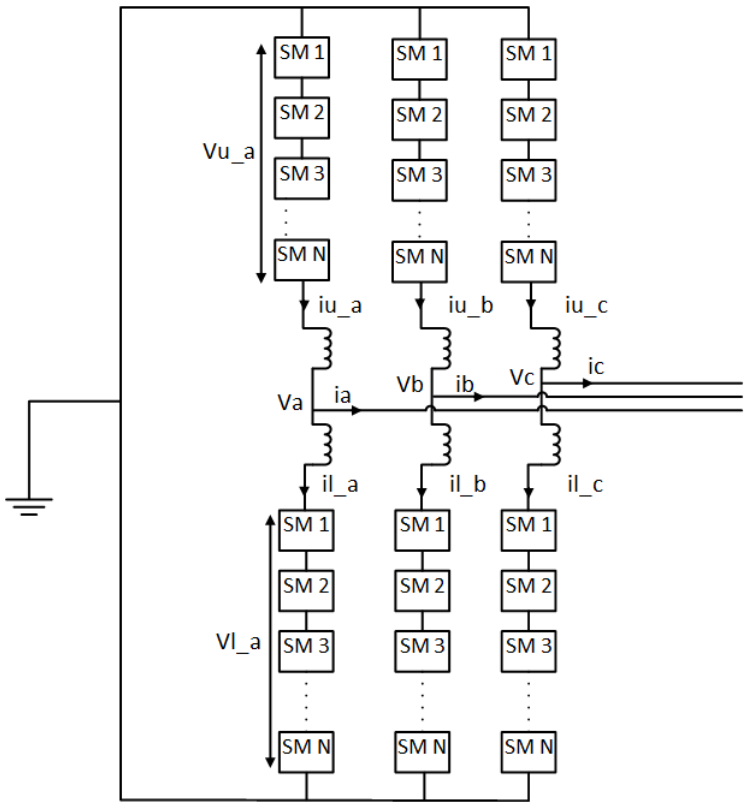


Figure 3.14: The circuit structure of MMC steady state operation with line-to-line DC side fault

During STATCOM operation, the AC side of MMC can remain connected

to the AC grid. The sum of the upper and lower arm voltages and currents are calculated based on equation (3.42).

$$\begin{aligned} V_u &= -V_{ac} \\ V_l &= +V_{ac} \\ I_u &= R_u I_{ac} \\ I_l &= -(1 - R_u) I_{ac} \end{aligned} \tag{3.42}$$

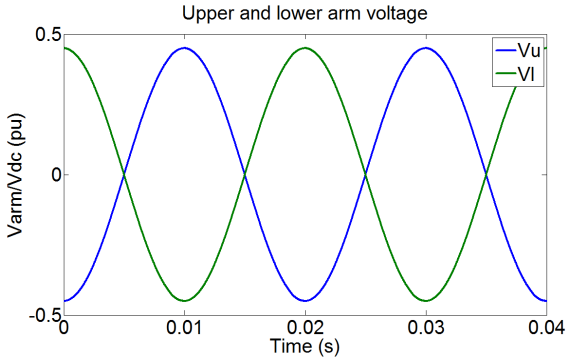
Similar to before, the sub-module capacitor voltage can be estimated by calculating the power flow through the arm. Assume $V_{ac} = \hat{v_{ac}} \cos(wt)$, $I_{ac} = \hat{i_{ac}} \cos(wt + \frac{\pi}{2})$ since only reactive power exists and the harmonics in current are eliminated by the PR controller. Then the voltage on the sub-module capacitor is calculated as equation (3.43) and (3.44).

$$\begin{aligned} P_u =& V_u I_u \\ =& -\hat{v_{ac}} \cos(wt) \times R_u \hat{i_{ac}} \cos(wt + \frac{\pi}{2}) \\ =& -\frac{1}{2} \hat{v_{ac}} R_u \hat{i_{ac}} \cos(2wt + \frac{\pi}{2}) \\ \Delta W_u =& \int P_u \\ =& -\frac{1}{4w} \hat{v_{ac}} R_u \hat{i_{ac}} \sin(2wt + \frac{\pi}{2}) \\ V_{cu} =& \sqrt{V_{caverage}^2 + \frac{2}{NC} \Delta W_u)} \end{aligned} \tag{3.43}$$

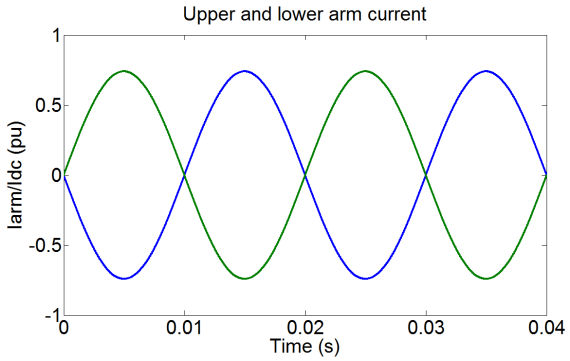
$$
\begin{aligned}
P_l =& V_l I_l \\
=& \hat{v_{ac}} \cos(wt) \times -(1 - R_u) \hat{i_{ac}} \cos(wt + \frac{\pi}{2}) \\
=& -\frac{1}{2} \hat{v_{ac}} (1 - R_u) \hat{i_{ac}} \cos(2wt + \frac{\pi}{2}) \\
\Delta W_l =& \int P_l \\
=& -\frac{1}{4w} \hat{v_{ac}} (1 - R_u) \hat{i_{ac}} \sin(2wt + \frac{\pi}{2}) \\
V_{cl} =& \sqrt{V_{caverage}^2 + \frac{2}{NC} \Delta W_l)}
\end{aligned}
\tag{3.44}
$$

The upper and lower arm voltages are independent of R_u, but the arm current varies with Ru. When $R_u = 0.5$, the arm voltage, current and sub-module voltage are shown in figure 3.15. Note that based on the analysis when $R_u = 0.5$, $\Delta W_u = \Delta W_l \Rightarrow V_{cu} = V_{cl}$.

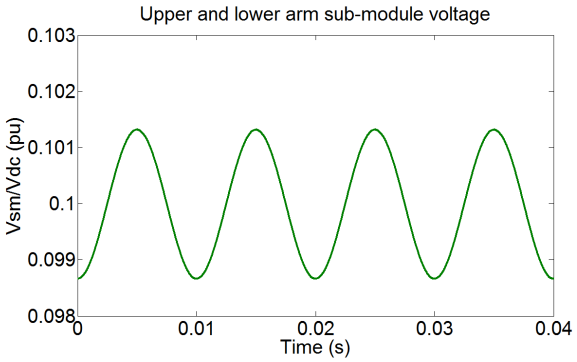
When $R_u = 1$, which means all the reactive power comes from the upper arm, the arm voltage, current and sub-module voltage are shown in figure 3.16. The arm voltage is still the same, but all the current goes through the upper arm. As a result, the sub-module capacitor voltages of upper arm and lower arm are different.



(a) The upper and lower arm voltage

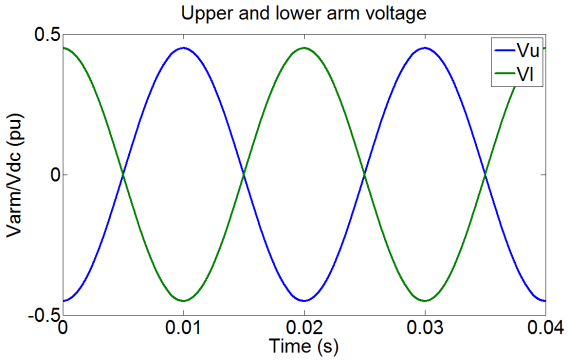


(b) The upper and lower arm current

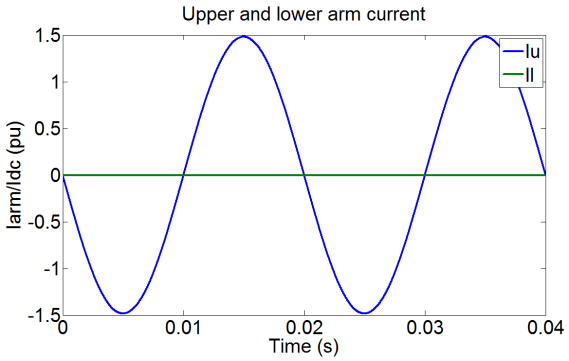


(c) The upper and lower arm sub-module capacitor voltage

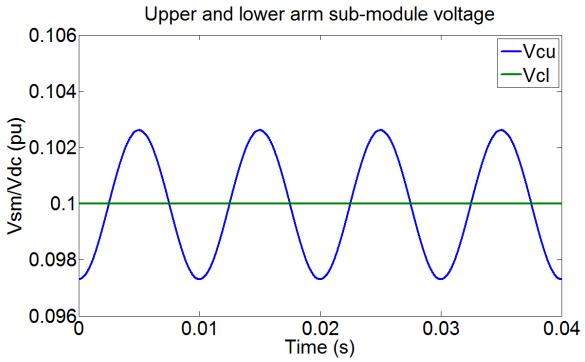
Figure 3.15: Arm voltage, current and sub-module voltage when $R_u = 0.5$



(a) The upper and lower arm voltage



(b) The upper and lower arm current



(c) The upper and lower arm sub-module capacitor voltage

Figure 3.16: Arm voltage, current and sub-module voltage when $R_u = 1$

3.5 Summary

This chapter has presented the normal operation of a standard MMC converter and has analysed post-fault operation of a full-bridge MMC converter.

MMC steady state operation has been investigated. Specifically the harmonic circulating current and the sub-module capacitor voltage characteristics. The second order harmonic is the most significant circulating current harmonic and the sub-module capacitor voltage can be estimated by calculating the power expression for the arm.

Depended on the different active power and reactive power distribution between the upper and lower arms, a full-bridge MMC is able to continue to transfer half rated power after a line-to-ground fault. Variables P_e, R_u are defined to represent the active power and reactive power proportions. When $P_e = 0.5$, the upper and lower arm voltages and sub-module capacitor voltage are all symmetric. The advantage of this operation mode is that the power loss is a minimum compared to other modes. Under this situation, the transformer needs to bear $0.25pu$ dc voltage stress. When $P_e = 1$, there is no dc voltage stress on the transformer but the power loss is a maximum compared to other modes. Trade off can be made between transformer stress and power loss.

The full-bridge MMC is also capable of providing reactive power to the AC side after line-to-line fault. The reactive power can be distributed flexibly

between the upper and lower arms. The same as before, when the reactive power is equally distributed between the upper and lower arms the power loss is the minimum.

Chapter 4

Modular multi-level converter control scheme

4.1 Introduction

This chapter presents an overview of the modulation and control schemes required to implement the proposed methods of operation in chapter 3; these can be broken down into arm modulation technique, sub-module rotation algorithm, AC current control, even harmonic elimination control, stored energy control and finally DC grid voltage control. A brief review of multi-level modulation methods is presented before the chosen in-phase level disposition (IPD) scheme is described in more detail; then the implemented sub-module rotation algorithm used is described and how it fits in with the modulation scheme. A review of AC current techniques is presented before the selected vector control technique is described. In chapter 3 analysis of the operating modes proposed are conducted assuming second harmonic elimination. A

review of the published methods of achieving this is presented as is a novel method based on the PR method found in literature. In order to avoid sub-module voltage shift due to the post-fault operation, energy control is developed. Last, DC voltage control involves the use of a PI controller to regulate the DC side voltage.

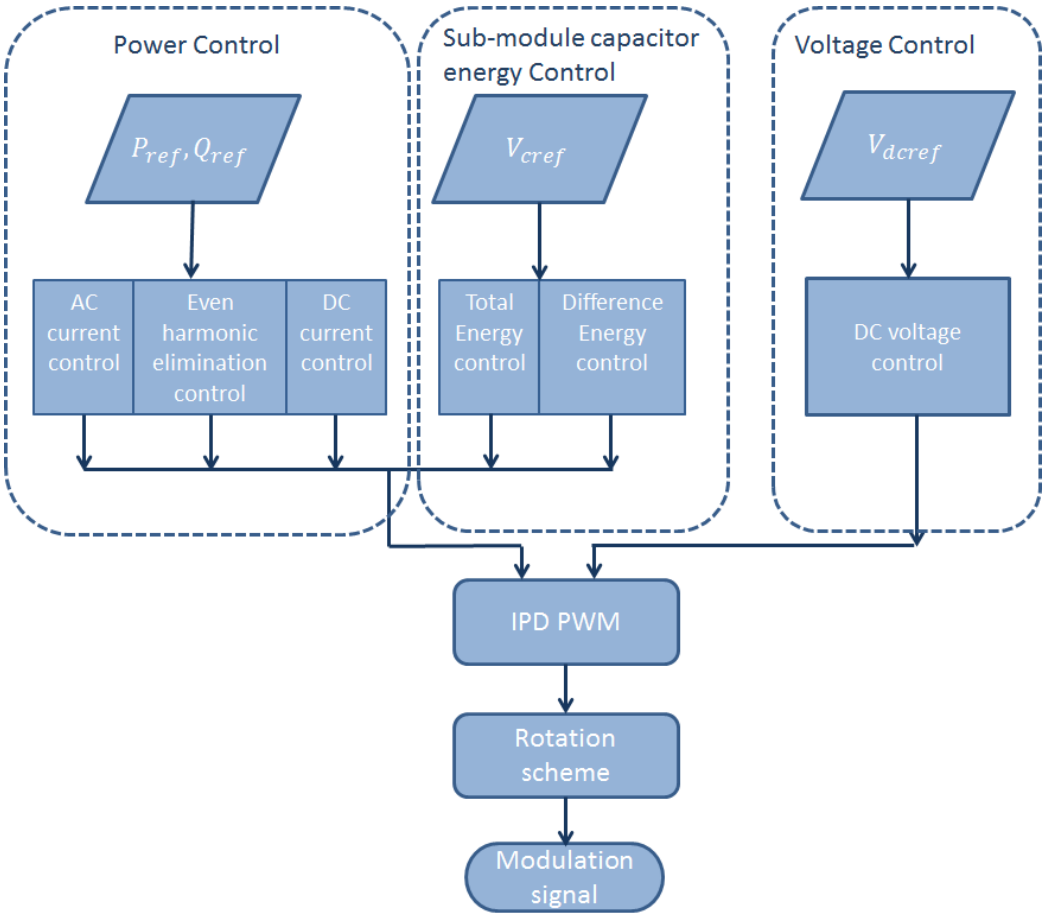


Figure 4.1: Control scheme organisation chart

Figure 4.1 shows the control scheme organisation in this thesis. The control scheme can be divided as current control and voltage control. Power

control includes AC closed loop current control, even harmonic elimination control, used to eliminate the second harmonic circulating current and DC current control. Energy control consists of total energy control which is used to control all the energy stored in the sub-module capacitor of one phase, and difference energy control which is used to equalise the energy of the upper arm and lower arm in one phase. DC voltage control is used to regulate the converter DC voltage to reference value. Then all the control outputs are used to produce the target arm voltage, In-phase level disposition (IPD) modulation is used to control the MMC to provide the target voltage. Afterwards, a rotation algorithm is used to keep the energy evenly distributed in each arm. Finally, a modulation signal is provided to MMC.

4.2 Modulation method level shifted carrier PWM

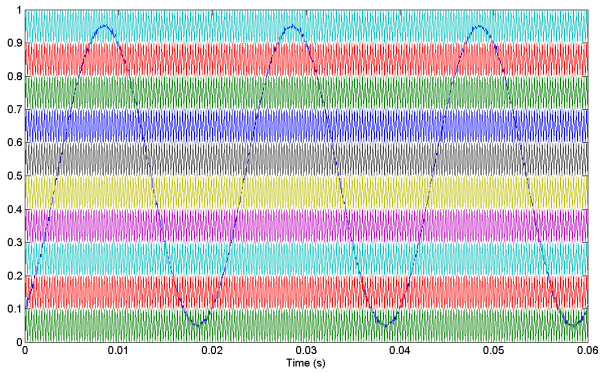
There are several multi-level modulation techniques presented in literature, such as level shifted modulation [77, 82], phase shifted modulation [70, 121] and selective harmonic elimination pulse width modulation [130]. If Level shifted modulation is used, a rotation method is required in order to balance the sub-module voltage [77]. The rotation method is unnecessary for the In phase shifted modulation method. However, it can be used in conjunction with the phase shifted modulation method [70, 121] to increase the performance. The selective harmonic elimination method is able to eliminate

harmonics, but the typical benefits of SHE are also reduced when there are such a high number of sub-modules used as the grid code can be easily met [131, 132].

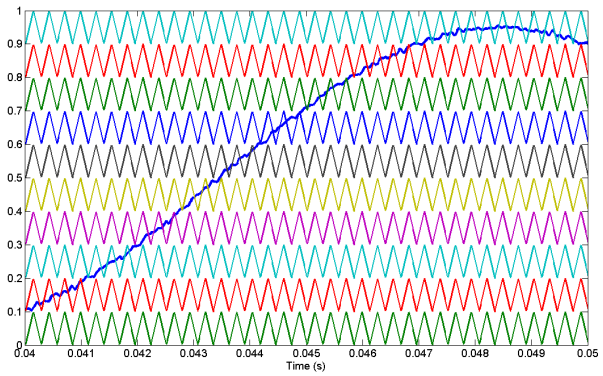
In this thesis, in-phase disposition (IPD) level shifted carrier PWM is used for the modulation, and it is now described in detail. It is not anticipated that this modulation method would be adopted in full-scale systems as the extra switching loss from the final cell PWM is unnecessary. However it is a scheme that is simple to implement and allows demonstration of the focus of this work, which is the DC fault ride through techniques presented in chapter 3.

IPD level shifted modulation is a carrier based modulation techniques that require generation of a modulation wave representing the target inserted voltage. The modulating wave is compared to a high frequency carrier to produce a switching waveform. Carriers are arranged in levels representing the available output levels of the converter as shown in figure 4.2. In the example shown in figure 4.2b, there are 10 levels carrier corresponding to 10 MMC sub-modules. However, each carrier does not necessarily correspond to a specific sub-module. A rotation algorithm, described in section 4.3, is applied to ensure capacitor energy is well distributed in the arm.

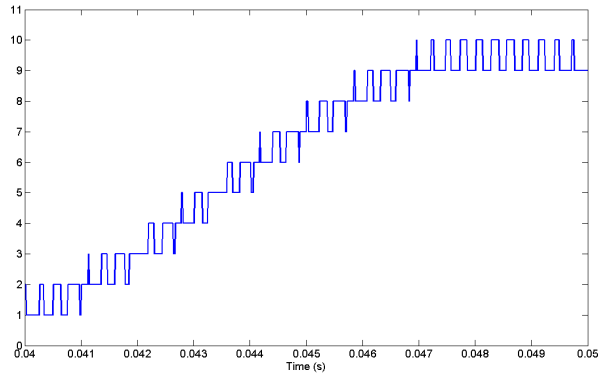
Figure 4.2c shows the switching waveform by comparing modulation waveform with carrier. The waveform contains only an integer number of levels and corresponds to the number of sub-modules that should be gated on. N_s



(a) Level shifted modulation example

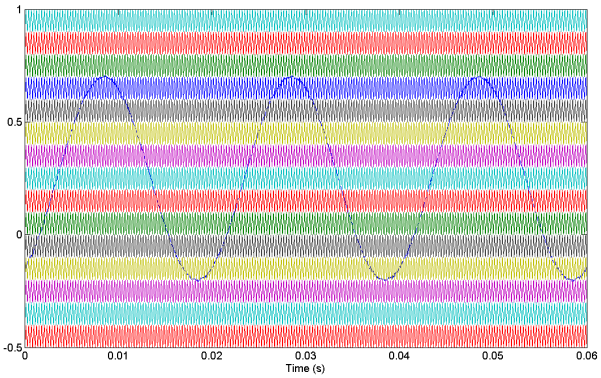


(b) zoom in Level shifted modulation example

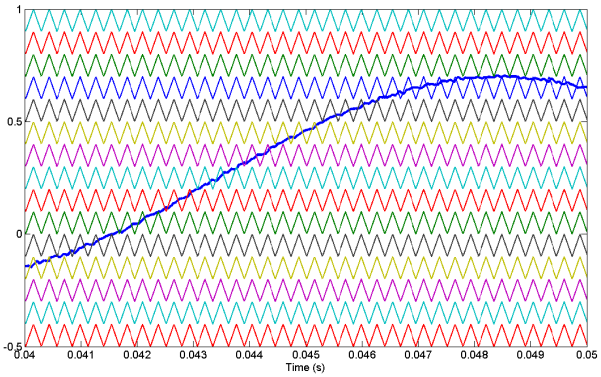


(c) Switching waveform N_s

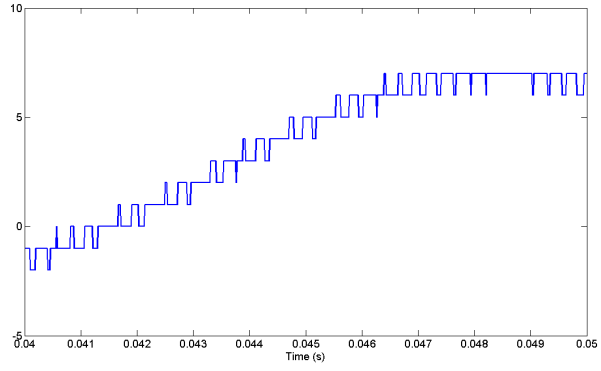
Figure 4.2: Level shifted modulation



(a) Level shifted modulation example for post-fault operation



(b) zoom in Level shifted modulation example for post-fault operation



(c) Switching waveform N_s for post-fault operation

Figure 4.3: Level shifted modulation for post-fault operation

is used to represent the modulation number of the inserted sub-module. The sub-module rotation algorithm is subsequently applied and will select the appropriate sub-modules based on this number.

The modes of operation presented in chapter 3 require that a negative voltage be inserted, an example of which is provided in figure 4.3. In this case additional negative level carriers are provided representing the capability of the full-bridge sub-module cells. During this negative voltage region a negative value of the inserted sub-module number, N_s, is generated. By using this technique the modulation strategy does not need to change between normal and post-fault operation.

4.3 Sub-module rotation algorithm

A rotation algorithm has been implemented to ensure that the sub-modules capacitor voltages within an arm stay balanced and do not diverge. The inserted sub-module is chosen according to arm current I_{valve}. Figure A.3 shows the implemented rotation algorithm for an MMC in the normal operation [73], the case where N_s is positive. There are 3 steps of this rotation algorithm.

1. The inserted sub-module number N_s, which is calculated from level shifted PWM, is compared with the current number of inserted sub-modules N_c.

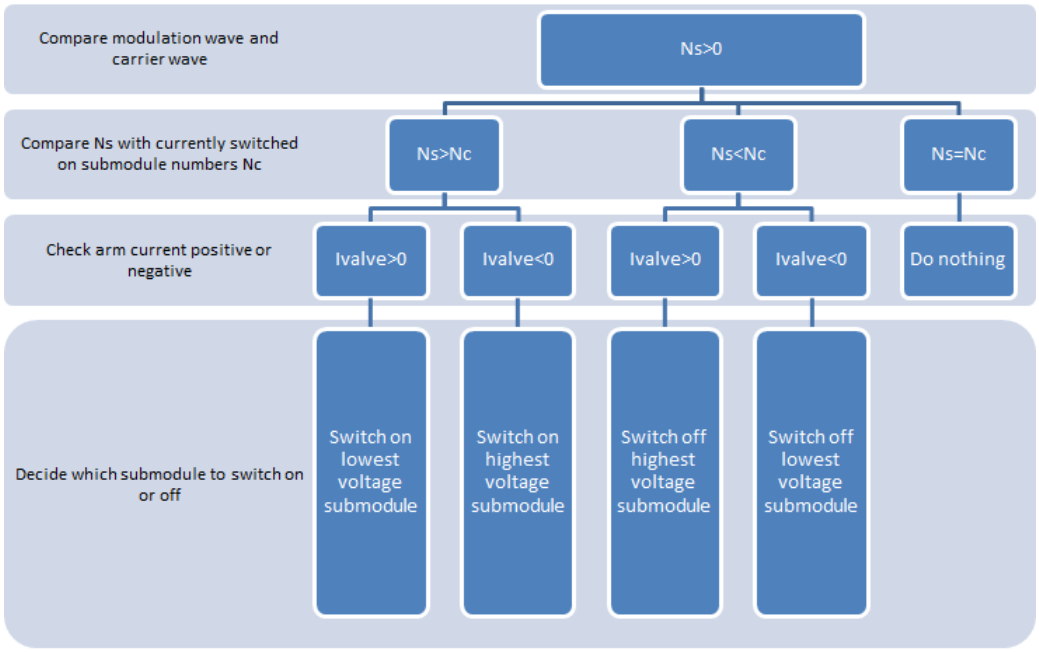


Figure 4.4: The flow chart of normal operation rotation algorithm ($N_s > 0$)

(a) if $N_s > N_c$, which means the reference voltage is larger than the current voltage, one or more sub-modules need to be switched on.

(b) if $N_s < N_c$, which means the reference voltage is smaller than the current voltage, one or more sub-modules need to be switched off.

(c) if $N_s = N_c$, then no sub-module needs to be switched on or off.

2. Depending on the valve current (positive or negative), select the sub-module with the lowest voltage or highest voltage.

(a) if $I_{valve} > 0$, it means that the inserted sub-module will be charged. So switch on the lowest voltage sub-module when $N_s > N_c$ or

switch off the highest voltage sub-module when $N_s < N_c$.

(b) if $I_{valve} < 0$, it means that the inserted sub-module will be discharged. So switch on the highest voltage sub-module when $N_s > N_c$ or switch off the lowest voltage sub-module when $N_s < N_c$.

For post-fault operation, the arm voltage needs to able to provide negative voltage. Consequently N_s will have a negative value during a fundamental period. When the sub-modules are producing a negative output and the valve current is positive, the capacitor will be discharge and vice versa. An updated flow chart showing the post fault rotation scheme is shown in figure 4.5.

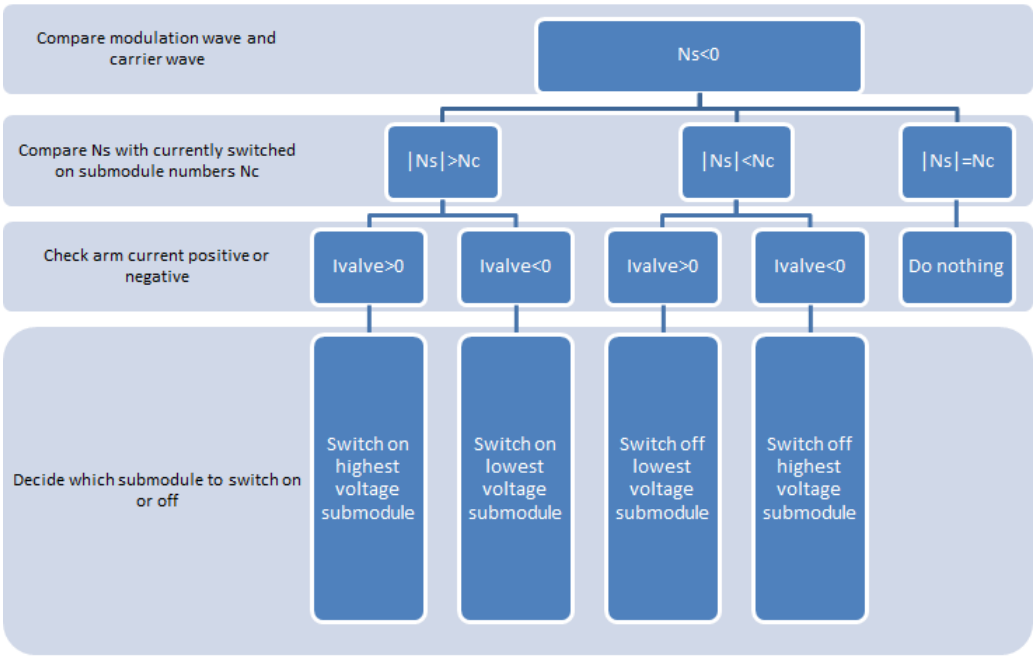


Figure 4.5: The flow chart of normal operation rotation algorithm ($N_s < 0$)

1. When $N_s \leq 0$, the absolute value of inserted sub-module number N_s is compared with current inserted sub-module number N_c.

   (a) if $|N_s| > N_c$, one sub-module to provide $-V_c$ needs to be switched on.

   (b) if $|N_s| < N_c$, one sub-module to provide $-V_c$ needs to be switched off.

   (c) if $|N_s| = N_c$, then the no sub-module needs to be switched on or off.

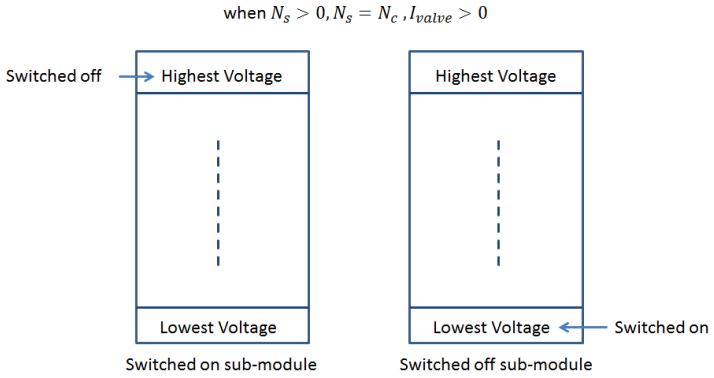
2. If the arm current is positive or negative, select the sub-module with the lowest voltage or highest voltage respectively.

   (a) if $I_{valve} > 0$, it means that the inserted sub-module will be discharged. So switch on the highest voltage sub-module when $|N_s| > N_c$ or switch off the lowest voltage sub-module when $|N_s| < N_c$.

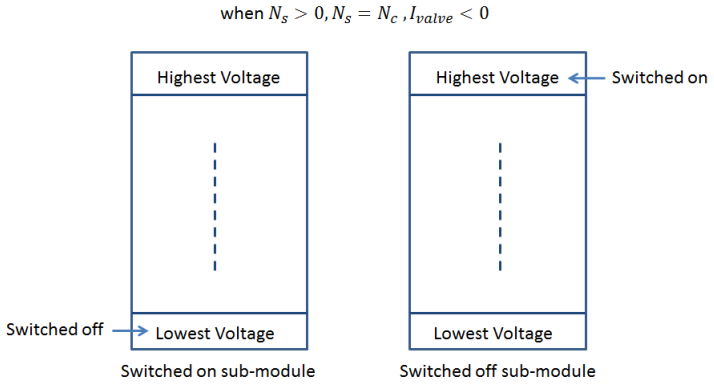
   (b) if $I_{valve} < 0$, it means that the inserted sub-module will be charged. So switch on the lowest voltage sub-module when when $|N_s| > N_c$ or switch off the highest voltage sub-module when $|N_s| < N_c$.

Even though the post-fault operation rotation is more complex than that for normal operation, the post-fault algorithm functions for both operation modes. As such, the rotation scheme is a unified scheme for all normal and faulted operation.

Based on the implemented modulation technique an on-off switching event typically occurs once every carrier period, such that switching loss is a function of carrier frequency. A comparison of switching loss versus carrier frequency is present in detail in Appendix. In the rotation algorithms presented the rotation speed is locked to the carrier frequency. The proposed scheme could be enhanced by allowing rotation events to happen when there is no change in the inserted sub-module index. The algorithm is shown in figure 4.6. It achieves better voltage balancing but at the cost is increased switching loss. Overall the rotation algorithm is a trade-off between switching loss and either capacitor voltage deviation or capacitor size.



(a) Increased rotation example when $N_s = N_c, I_{valve} > 0$



(b) Increased rotation example when $N_s = N_c, I_{valve} < 0$

Figure 4.6: Increased rotation example when $N_s = N_c > 0$

4.4 AC current control

There are several proposed AC current control schemes in literature that can be adopted for use with the MMC converter [74, 133–136]. In [133], a proportional current controller with a feed-forward voltage and a dq coupling elimination term is used to control the current. In [74], predictive control is used. In [74, 135, 136], vector control scheme is utilised to regulate AC current. In this work a vector control scheme has been adopted. The advantage of using vector control is that by projecting the AC abc values onto a rotating axis they appear as DC terms, allowing a discreetly implemented PI control to easily track the active power and reactive power references independently.

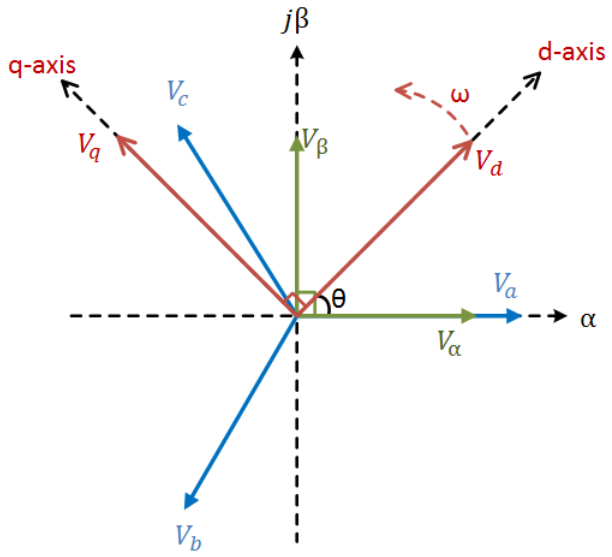


Figure 4.7: Three phase system stationary phase coordinate system to rotating coordinate system

Figure 4.7 shows a stationary phase coordinate system and a rotating coordinate system. The three phase system voltage are named V_{abc}, the sta-

tionary two phase coordinate system voltage is named $V_{\alpha\beta}$ and the rotating two phase coordinate system voltage are named V_{dq}.

$$T_{\alpha\beta 0} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{4.1}$$

$$\begin{aligned} \begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} &= T_{\alpha\beta 0} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \\ &= T_{\alpha\beta 0} \begin{bmatrix} U_m \cos(\omega t) \\ U_m \cos(\omega t - \frac{2\pi}{3}) \\ U_m \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \\ &= \begin{bmatrix} U_m \cos(\omega t) \\ U_m \sin(\omega t) \\ 0 \end{bmatrix} \end{aligned} \tag{4.2}$$

$$T_{dq0} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \tag{4.3}$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = T_{dq0} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} U_m \\ 0 \end{bmatrix} \tag{4.4}$$

Clarke transform

The Clarke transformation (4.1) is used to calculate the projection of V_{abc} on α and β axis. As stated in equation (4.1) and (4.2), assuming V_a is in phase with V_α and all three phases are balanced, the stationary voltage will be given by (4.2).

Park transform

The Park transformation, as stated in equation (4.3) and (4.4), is used to calculate the projection of $V_{\alpha\beta}$ on d and q axis, where d and q axis are rotating with angular velocity ω.

A simple model of the AC side of converter using ideal voltages sources is shown in figure 4.8. Using the Park transform, the relationship of a vector on the dq axis and a vector on the $\alpha\beta$ axis is given by equation (4.5). By using vector represention of the voltage source voltage $\vec{V_s}$, the converter AC side voltage $\vec{V_c}$ and current $\vec{i}$, the KVL equation of the model is (4.6).

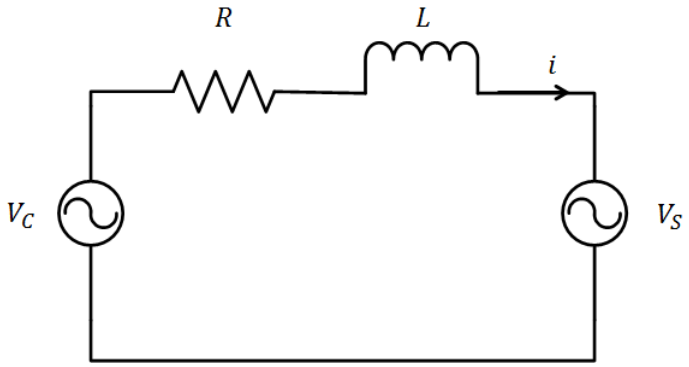


Figure 4.8: Model of AC side of converter

$$f_d + jf_q = (f_\alpha + jf_\beta)e^{-\rho(t)} \Rightarrow \vec{f} = f_\alpha + jf_\beta = (f_d + jf_q)e^{\rho(t)} \tag{4.5}$$

Where $\rho(t)$ is equal to the phase angle in radians given by $\omega_0 t + \theta_0$, typically this would be extracted by a Phase-locked loop (PLL) as in [43]. By analysing Fig 4.8,

$$L\frac{d}{dt}(\vec{i}) = -R\vec{i} + \vec{V_c} - \vec{V_s} \tag{4.6}$$

let $\vec{V_s} = \hat{V_s}e^{j(\omega_0 t+\theta_0)}, \vec{i} = i_{dq}e^{j\rho}, \vec{V_c} = V_{cdq}e^{j\rho}$, Then

$$L\frac{d}{dt}(i_{dq}e^{j\rho}) = -Ri_{dq}e^{j\rho} + V_{cdq}e^{j\rho} - V_{sdq}e^{j\rho}$$

which can be rewritten as

$$L(e^{j\rho}\frac{d}{dt}i_{dq} + ji_{dq}\frac{d\rho}{dt}) = -Ri_{dq}e^{j\rho} + V_{cdq}e^{j\rho} - V_{sdq}e^{j\rho}$$

substituting for $\frac{d\rho}{dt} = \omega_0, i_{dq} = I_d + jI_q, V_{cdq} = V_{cd} + jV_{cq}, V_{sdq} = V_{sd} + jV_{sq}$
The equation (4.6) can be rewritten as:

$$L\frac{dI_d}{dt} = L\omega_0 I_q - RI_d + V_{cd} - V_{sd} \tag{4.7}$$

$$L\frac{dI_q}{dt} = -L\omega_0 I_d - RI_q + V_{cq} - V_{sq} \tag{4.8}$$

In order to decouple the cross coupling terms $L\omega_0 I_q$ and $-L\omega_0 I_d$ two decoupling terms are added the output of PI controller along with feedforward of the supply voltage in the dq axis, as shown in figure 4.9. This enables decoupled closed loop regulation of the line current. The total converter voltage demand (V_{cd}, V_{cq}) is then given by equation (4.9).

$$\begin{aligned} V_{cd} &= V_d - L\omega_0 I_q + V_{sd} \\ V_{cq} &= V_q + -L\omega_0 I_d + V_{sq} \end{aligned} \tag{4.9}$$

The relationship between the converter in the dq axis, V_{dq} , and the line current is then given by equation (4.7).

$$V_d = RI_d + L\frac{dI_d}{dt}$$
$$V_q = RI_q + L\frac{dI_q}{dt} \tag{4.10}$$

$$V_d = RI_d + LsI_d$$
$$V_q = RI_q + LsI_q \tag{4.11}$$

Based on equation (4.10) and the control system described in figure 4.9, the control system can be represented as a block diagram as given in figure 4.10 where the plant for the system is given by (4.11). The gains for the PI controller can the be calculated form the transfer function based on this transfer function.

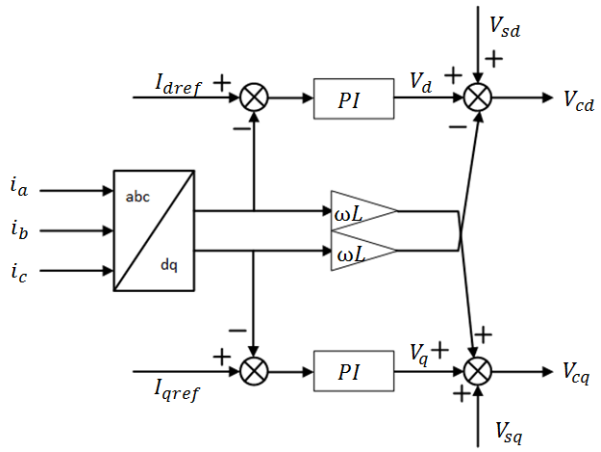


Figure 4.9: Decoupled vector control scheme for the AC side current

The reference values for I_d, I_q are calculated in open-loop based on active and reactive power references as in (4.12). $S(t), P(t), Q(t)$ refer to instanta-

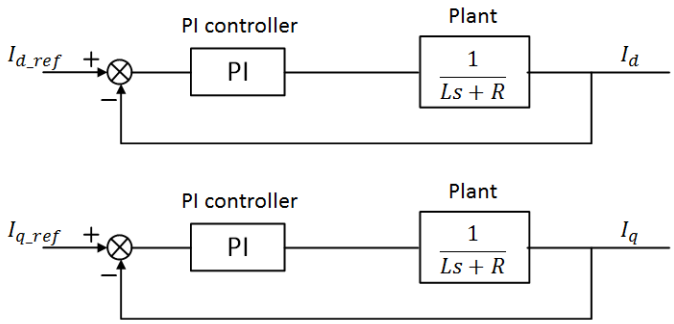


Figure 4.10: Block diagram of closed-loop current controller

neous complex power, instantaneous active power and instantaneous reactive power respectively. In a real system it is likely that a slow closed loop PQ controller would be added to ensure power demands are met; however it is unlikely that the implementation of such a controller would significantly affect the transient DC fault ride through performance of the converter and as such has been neglected.

$$\begin{aligned} S(t) &= P(t) + jQ(t) = \frac{3}{2}\hat{V(t)}\hat{I(t)}^{*} \\ P(t) &= \frac{3}{2}[V_{sd}(t)I_d(t) + V_{sq}(t)I_q(t)] \\ Q(t) &= \frac{3}{2}[-V_{sd}(t)I_q(t) + V_{sq}(t)I_d(t)] \end{aligned} \tag{4.12}$$

In this work the rotating dq axis is aligned with the supply voltage such that in steady state $V_{sq} = 0$. As a consequence I_d and I_q will determine $P(t), Q(t)$ respectively.

$$
\begin{aligned}
I_{dref}(t) &= \frac{2P_{ref}(t)}{3V_{sd}} \\
I_{qref}(t) &= -\frac{2Q_{ref}(t)}{3V_{sd}}
\end{aligned}
\tag{4.13}
$$

4.5 Even harmonic elimination

In chapter 3, analysis showed that the dominant harmonic in the arm current is the second order harmonic. This section presents a proportional resonant control to minimize the second order harmonic current.

Proportional-Resonant Control (PR control) has been proposed as a control method to suppress the second harmonic circulating current in MMC converters [137, 138]. An alternative control method for control of the second harmonic using a rotating reference frame has also been proposed in [70]. In this work PR control is used.

The PR control consists two terms: the proportional term and the resonant term. The proportional term is the same as PI control as it is frequency independent. For the resonant term, a dc quantity is calculated by multiplying the input signal by a sine and cosine waveform, which both have the reference frequency, so that the PR controller can control a DC value instead of an AC value. The detail of the theory is shown in figure 4.11. After multiplying the input signal $e(t)$ by $sin(w_0t)$ and $cos(w_0t)$, it goes through the integral control term and also the double-frequency part is removed, so that only the dc component is left. Then the output is multiplied the sine

and cosine wave again to retrieve to AC waveform. The transfer function for H_{AC} is shown in equation (4.14), with the proportional term:

$$H_{DC}(s) = K_p + \frac{K_i}{s}$$
$$H_{AC}(s) = K_p + \frac{2K_i s}{s^2 + w_0^2} \tag{4.14}$$

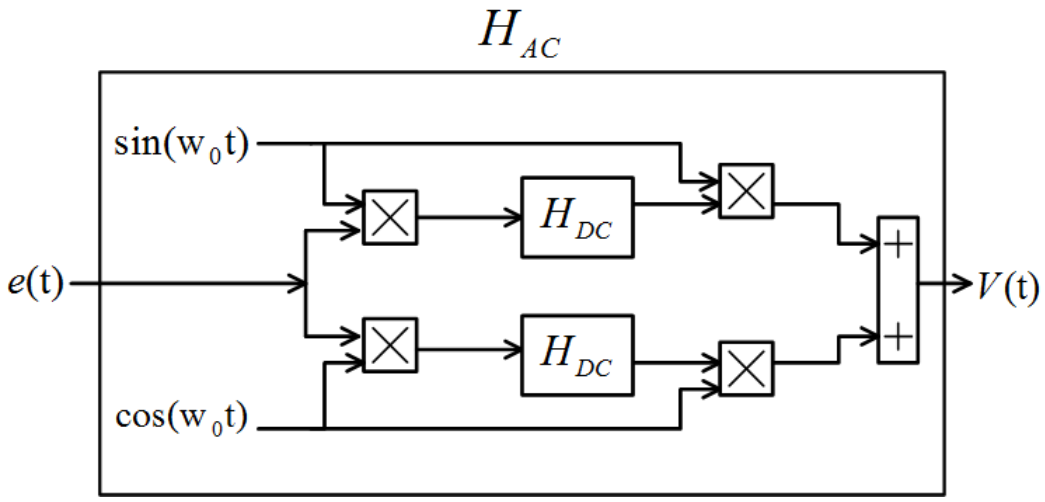


Figure 4.11: PR control block [139]

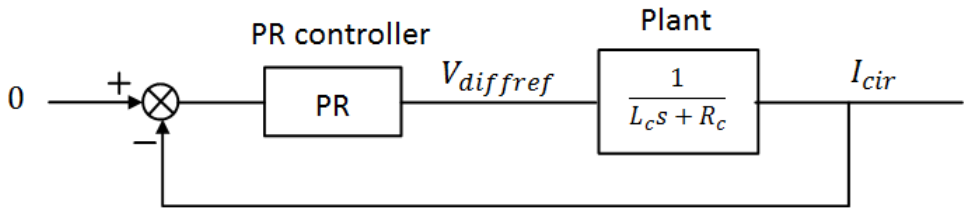


Figure 4.12: Block diagram of standard closed-loop PR controller

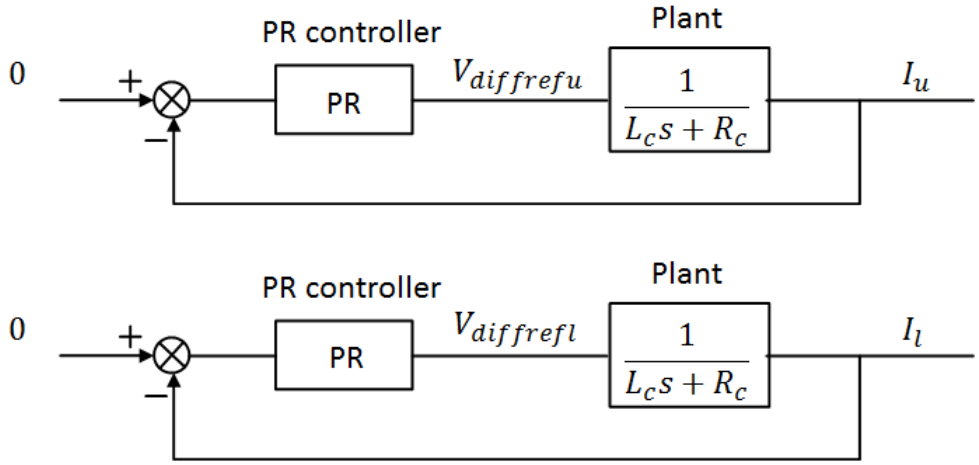


Figure 4.13: Block diagram of closed-loop PR controller

A control block diagram showing the implementation of PR control proposed in literature for second harmonic suppression is shown in figure 4.12. Where $I_{cir} = \frac{I_u + I_l}{2}$ is the circulating current of one phase, L_c,R_c are arm inductance and arm resistance. This approach generates a reference second harmonic voltage component to be inserted in the DC path of the current and it assumed that the distribution of this component should be equally split amongst the upper and lower arms. This works well for the case when the arms are operating symmetrically as the second harmonic component that is naturally generated by the arms is in phase and of equal magnitude. However when the arms operate asymmetrically during post fault operation as proposed in section 3.3. The second harmonic component produced by each arm is no longer of equal phase and magnitude; thus to prevent a second harmonic component being seen by the network a method of removing the second order harmonic voltage from each arm must be used. It is proposed here that independent control is given for the upper and lower arm, as shown

in figure 4.13, this ensures that neither the upper or lower limb currents contain a second order harmonic current. In practice complete elimination of the second order component will not be possible; as such the controller should be tuned to have sufficient attenuation that when any residual current in the arm interacts with the arm impedance the AC voltage produced at the network terminals meets the grid code. The references for the arm current are calculated based on the reference input, as equation (4.15).

$$I_{uref} = \frac{1}{3} I_{dcref} + P_e I_{realref} + R_u I_{reactiveref} \tag{4.15}$$

$$I_{lref} = \frac{1}{3} I_{dcref} - (1 - P_e) I_{realref} - (1 - R_u) I_{reactiveref} \tag{4.16}$$

By using an AC current controller and a PR controller, the AC component of the sub-module capacitor voltage is under control. But the DC component, which is also referred to as the sub-module capacitor average voltage, is not being controlled yet. In post-fault operation, the upper and lower arm DC components of the sub-module voltage are asymmetrical whenever the upper and lower current are not. As a result, sub-module average voltage control is required.

4.6 Control of the MMC sub-module capacitor average voltage

In normal operation, the sub-module capacitor voltage will reach a natural balance in steady state without any control. The sub-module capacitor average voltage of the upper and lower arms are the same since the arm currents are symmetric, while the average voltage magnitude is not being controlled. But in post-fault operation, the sub-module capacitor average voltage of the upper and lower arms are no longer the same since the arm currents are asymmetric. Consequently, a sub-module capacitor average voltage control is necessary. It is possible to regulate the energy stored in each arm using closed-loop control, which is the method preferred in this work. The control loops used can be separated into total phase capacitor energy controller and energy control is separated as total capacitor energy control and upper and lower difference energy control [80].

The equations of the total energy for one phase $\sum W_c$, and the energy difference of upper and lower arm for one phase ΔW_c are discussed in chapter 3 section 3.2.2, and repeated here in equation (4.17) and (4.18).

$$\frac{d\sum W_c}{dt} = (V_{dc} - 2V_{diff})I_{diff} - V_{ac}I_{ac} \tag{4.17}$$

$$\frac{d\Delta W_c}{dt} = -2V_{ac}I_{diff} + (\frac{1}{2}V_{dc} - V_{diff})I_{ac} \tag{4.18}$$

4.6.1 Per-phase total capacitor energy control

In equation (4.17), V_{diff} is the voltage across the arm inductor and I_{diff} is the circulating current of one phase. The DC component of the right side of equation (4.17) will affect the average magnitude of $\sum W_c$. Assuming the DC reference voltage, V_{dc}, is much greater than V_{diff} then the dc component of $(V_{dc} - 2V_{diff})I_{diff}$ is equal to $V_{dc} \times \frac{1}{3} I_{dc}$. The dc component of $V_{ac}I_{ac}$ is equal to $\frac{1}{2}\hat{V_{ac}}\hat{I_{ac}}\cos(\phi) = \frac{1}{3}P_{ref} = \frac{1}{2}V_d I_d$. Then equation (4.17) can be rewritten as in (4.19), where $V_{dc} \times \frac{1}{3} I_{dc}$ is one third of the power from dc side, $\frac{1}{2}V_d I_d$ is one third of the power from ac side. This shows that the total energy of the sub-module capacitor can be controlled by the difference between the power from the dc side and the ac side.

$$\begin{aligned} \frac{d\sum W_c}{dt} &= P_{dc} - P_{ac} \\ &= V_{dc} \times \frac{1}{3} I_{dc} - \frac{1}{2} V_d I_d \end{aligned} \tag{4.19}$$

let $I_{dc} = I_{dcref} + \Delta I_{dc}, I_d = I_{dref} + \Delta I_d$. Ideally, in steady state $\frac{1}{3}V_{dc} \times I_{dcref} = \frac{1}{2}V_d I_d$ so that the average dc voltage is stable. From the view of energy, when the DC side power equals the AC side, there is no change in energy accumulated inside the converter. If an unbalance is created between the DC and AC side power, the energy inside the converter can be controlled to decrease or increase. As a result, by changing ΔI_{dc} or ΔI_d the dc voltage of the sub-module capacitor can be controlled.

Control of total stored sub-module energy using power from the DC side

For one phase of the MMC converter, assuming AC side energy is kept to be equal to the reference and DC side energy is used to control $\sum W_C$, which means $I_{dc} = I_{dcref} + \Delta I_{dc}, I_d = I_{dref}$, then $V_{dc}\frac{1}{3}\Delta I_{dc}$ is the rate of change accumulated of energy in the two arms of a phase. Substituting $\sum W_C = \frac{1}{2}2NCV_{csm}^2 = NC_{sm}V_{csm}^2$ into equation (4.19), gives:

$$NC_{sm}\frac{d}{dt}(V_{csmref}^2 - V_{csm}^2) = V_{dc}\frac{1}{3}\Delta I_{dc} \tag{4.20}$$

Let $V_{csmref}^2 - V_{csm}^2 = \Delta E_T$, and in Laplace form

$$NC_{sm}s\Delta E_T = \frac{1}{3}V_{dc}\Delta I_{dc} \tag{4.21}$$

The total energy closed-loop controller is shown in figure 4.14. ΔI_{dc} is used as the reference of the dc current controller.

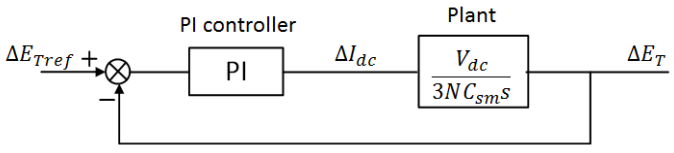


Figure 4.14: The closed-loop controller of total energy from DC side

DC current control

For one phase of the MMC converter, a voltage can be imposed across the arm inductor to control the dc current. Although it is unnecessary in normal operation, it is required when using closed-loop total capacitor energy control applied on the dc side. The relation between dc current I_{dc} and the inductor voltage V_{diff} are:

$$L_c \frac{d}{dt}(\frac{1}{3}I_{dc}) + R_c \frac{1}{3} I_{dc} = V_{diff} \tag{4.22}$$

In Laplace form,

$$I_{dc} = \frac{3}{L_c s + R_c} V_{diff} \tag{4.23}$$

The closed-loop dc current controller is shown in figure 4.15.

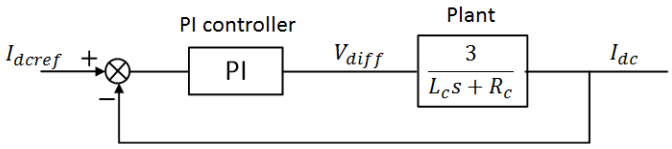


Figure 4.15: The closed-loop controller for the dc current

Figure 4.16 shows the cascaded controller for total energy control from the dc side.

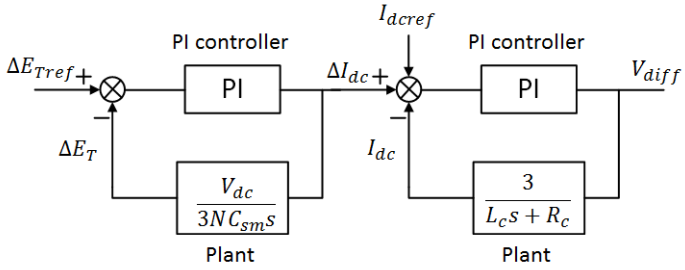


Figure 4.16: The cascaded closed-loop controller of total energy from DC side

Sub-module total stored energy control by using power from AC side

Alternatively, the total energy can be controlled from the AC side by ΔI_d. Assuming $I_{dc} = I_{dcref}, I_d = I_{dref} + \Delta I_d$, the rate of change of energy accumulated inside the phase is $\frac{1}{2}V_d I_d$.

$$NC_{sm}\frac{d}{dt}(V_{csmref}^2 - V_{csm}^2) = \frac{1}{2}V_d \Delta I_d \tag{4.24}$$

Let $V_{csmref}^2 - V_{csm}^2 = \Delta E_T$, and in Laplace form

$$NC_{sm}s\Delta E_T = \frac{1}{2}V_d \Delta I_d \tag{4.25}$$

Then the total energy closed-loop controller according to (4.25) is shown in figure 4.17. ΔI_d is used as the reference of the AC current controller.

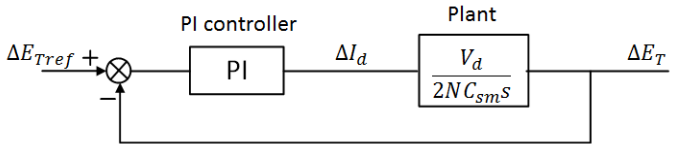


Figure 4.17: The closed-loop controller for the total energy from the AC side

4.6.2 Difference energy of upper and lower arm control

A further energy control is required to balance the dc component of the stored energy in the upper and lower arms of a phase. This can be done by circulating a fundamental frequency component current in the limb.

Referring back to equation (4.18), the fundamental frequency current component of I_{diff} will affect ΔW_C. Assuming there is a fundamental frequency circulating current I_1 exists, and $V_{ac} \gg V_{diff}$, $V_{ac} = \hat{V_{ac}} \cos(\omega t)$ and $I_1 = \hat{I_1} \cos(\omega t + \phi)$. Let $\Delta W_C = \frac{1}{2} N C_{sm} (V_{cu}^2 - V_{cl}^2)$, equation (4.18) can be rewritten as :

$$\frac{1}{2} N C_{sm} \frac{d}{dt} (V_{cu}^2 - V_{cl}^2) = -\hat{V_{ac}} \hat{I_1} \cos\phi \tag{4.26}$$

Let $\Delta E_D = V_{cu}^2 - V_{cl}^2$, in Laplace form, then

$$\frac{1}{2}NC_{sm}s\Delta E_D = -\hat{V_{ac}}\hat{I_1}\cos\phi \tag{4.27}$$

Assuming $\phi = 0$, the upper and lower capacitor voltage difference controller is shown in figure 4.18. Based on equation (4.27), the upper and lower arm voltage difference can be controlled by injecting a fundamental frequency circulating current.

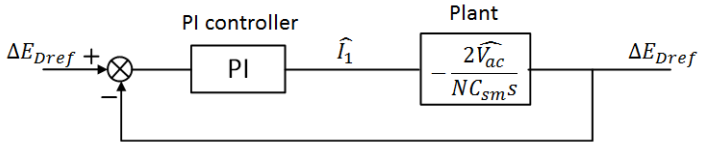


Figure 4.18: The closed-loop controller of arm average voltage difference

4.7 DC grid voltage control

Using the carrier based modulation method discussed in section 4.1 the DC grid voltage, V_{dc}, can be controlled in open-loop by feeding forward a DC reference into the modulating wave. Using this open-loop approach can generate an error in the output voltage, which can be attributed to the interaction between the modulating wave containing AC and DC components and the time varying sub-module voltages. To compensate for this error it is proposed that a PI controller is used in conjunction with the feedforward term as shown in figure 4.19.

$$
\begin{aligned}
V_u &= N n_u V_{cu} \\
&= N \frac{\frac{1}{2}V_{dc} - V_{acref} - V_{diffuref}}{V_{dc}} \times (V_{cudc} + V_{cuac})
\end{aligned}
\tag{4.28}
$$

Take the upper arm as example, as shown in equation (4.28). The capacitor voltage is divided as dc component V_{cudc} and ac component V_{cuac}. V_{cudc} is being controlled to equal V_{dc}/N; V_{cuac} is a function of controlled arm current. For the modulation n_u, V_{acref} and $V_{diffuref}$ are both controlled by the AC current controller and even harmonic controller. As a result, the DC component of V_u will not be equal to half DC voltage. In order to adjust the DC voltage of the arm leg, V_m is added to the modulation signal.

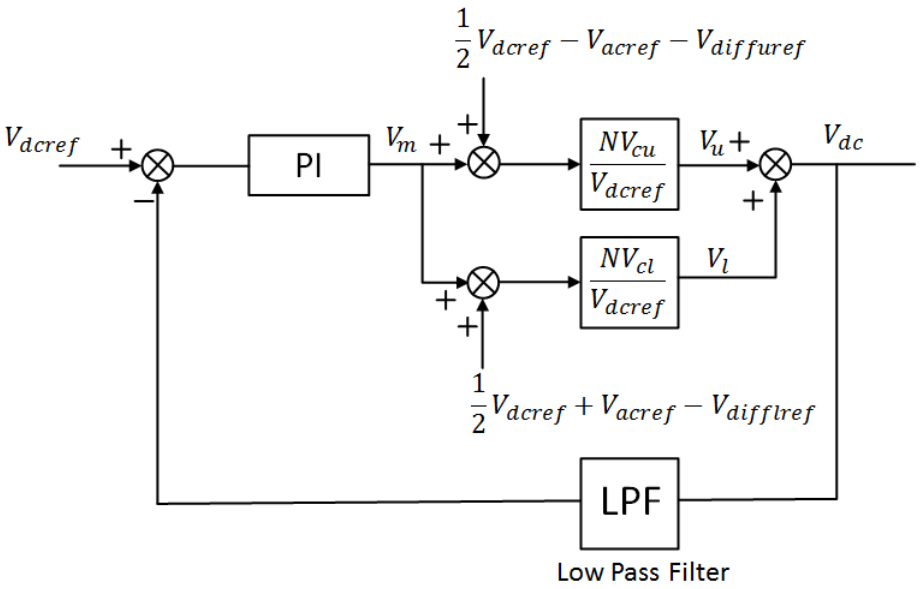


Figure 4.19: The closed-loop controller of DC voltage

Figure 4.19 shows the closed-loop controller for the DC voltage. The compensation value V_m is added to the with modulation wave, and then multiplied with $\frac{NV_{cu}}{V_{dcref}}$ and $\frac{NV_{cl}}{V_{dcref}}$. Over a fundamental period, these two terms are controlled to be one. The low pass filter is designed for a cut frequency of $\frac{1}{10}$ fundamental frequency, which is $5Hz$. As a result, the PI controller is tuned according to the low pass filter.

This DC voltage controller is only used on one side in a point-to-point HVDC transmission. However, in order to control the power flow in Multi-terminal DC grids , DC voltage control can be used on any terminal. At that time, the reference can be provide by the droop or margin controller to regulate the power flow.

4.8 Summary

This chapter has presented the development of modulation, current and energy controllers for the MMC. The dq control method is used to regulate the AC current for its high control performance. Harmonic elimination involves the use of a PR controller since the main harmonic is the 100Hz circulating current. The PR controller are separated as two individual controllers due to the asymmetry of the arm current under post-fault operation.

The sub-module average voltage is adjusted to equal the reference value after the implementation of the energy control. This control is not necessary

for normal operation for in most cases the average sub-module voltage is equal to V_{dc}/N by natural balancing. However, by using energy control, the sub-module average voltage can be assigned other magnitudes. This energy control is more useful and essential for post-fault operation, in order to let the upper and lower arm sub-modules average voltage achieve V_{dc}/N. The DC voltage is controlled by a PI controller. The reference for the DC voltage can be predefined or provided by the DC grid power flow controller. For a point-to-point HVDC system, one terminal will control the power, the whole control loop is shown in figure 4.20; and the other terminal will control the dc voltage, the whole control loop is shown in figure 4.21.

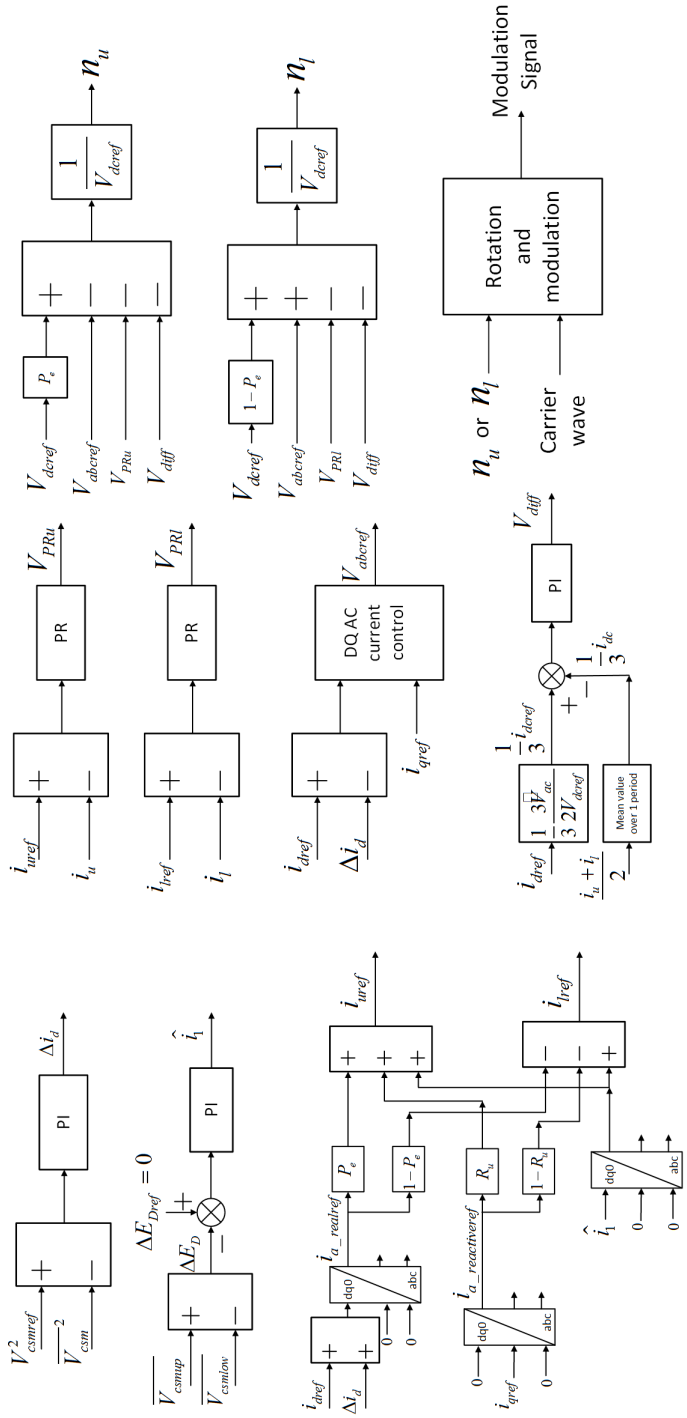


Figure 4.20: The whole control loop of power control terminal

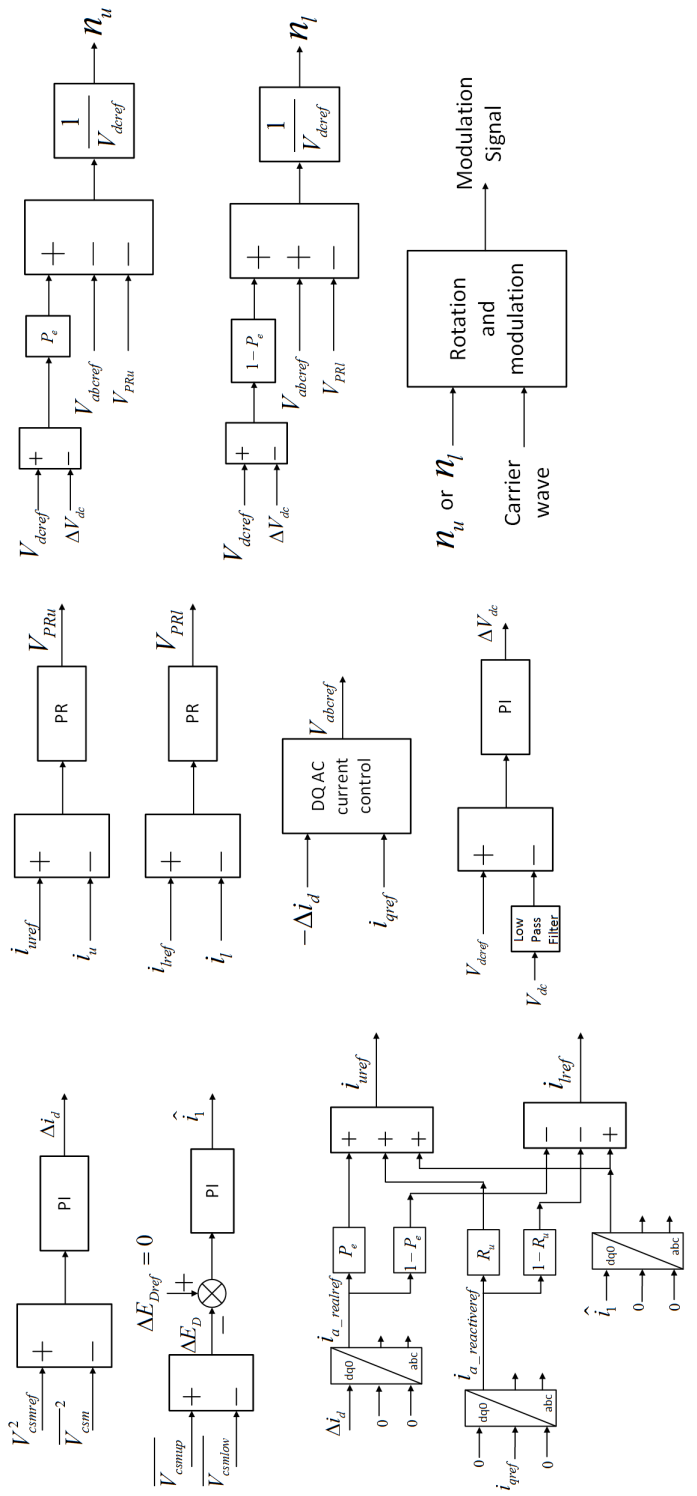


Figure 4.21: The whole control loop of voltage control terminal

Chapter 5

Multi-terminal DC Grid modelling

5.1 Introduction

This chapter explains in detail the modelling of a 4-terminal DC grid. Background information is provided of the CIGRE multi-terminal HVDC grid used as the basis for this model. Derivation of model component values of arm inductance, sub-module capacitance and cable parameters are demonstrated by scaling down the data from CIGRE model using a per unit system. The distributed cable model used to represent the transmission networks in the simulation is introduced. A non-switching model of the MMC converter is developed in order to reduce model computation time and make simulation of the presented grid feasible. Simulations are presented to demonstrate the non-switching model performance.

5.2 CIGRE multi-terminal DC grid test system

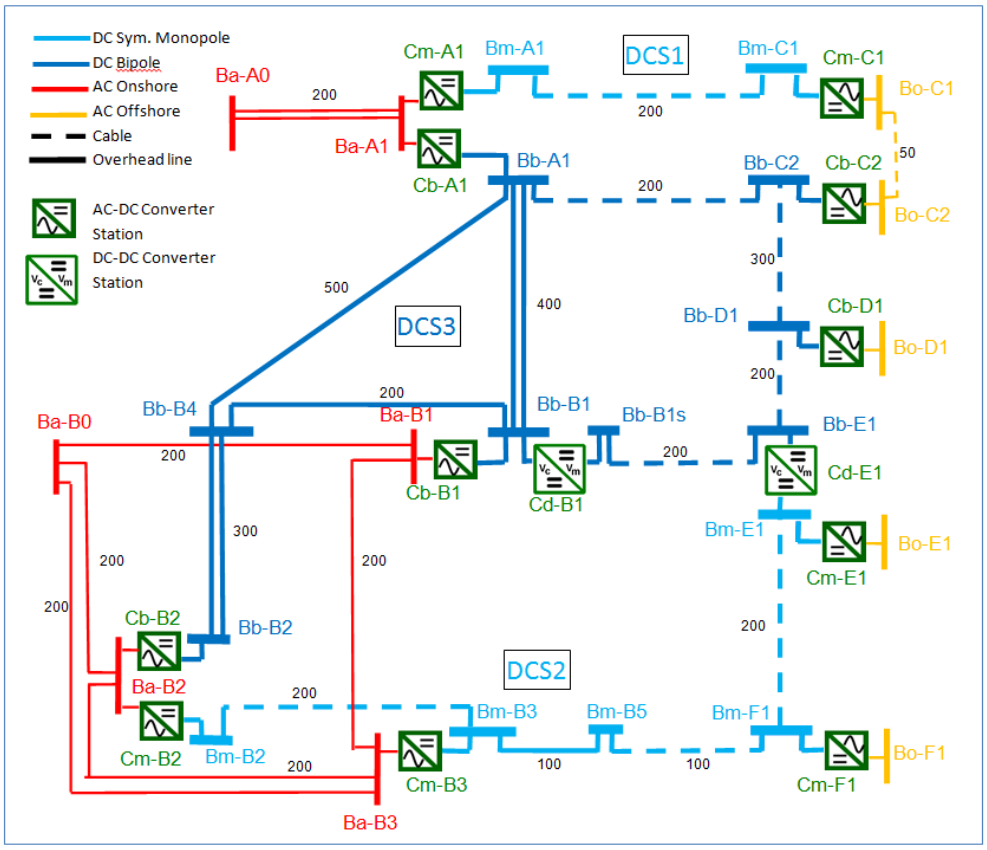


Figure 5.1: The CIGRE B4 DC Grid Test System

A DC grid test system has been proposed by the CIGRE B4 working group [140]. It is an example of a future meshed HVDC grid; the purpose of the test grid is provide a benchmark model, accordingly this thesis uses the parameters based on this model so that the results can be compared with other studies which also use the same model.

As shown in figure 5.1, the whole system contains three VSC DC systems that can be used separately. DC system 1 which on the top of the figure is a 2-terminal symmetric monopole system; DC system 2 which is at the bottom of the figure is a 4-terminal symmetric system, this system can be classified as a star system; DC system 3 which is at the middle of the figure is a 5-terminal bipole HVDC system, it is a meshed HVDC system. DC-DC converter B1 is used to control power flow; when not performing this function, it can be bypassed. The other DC-DC converter E1 connects DC system 2 and 3 because the voltage of the bipole system is twice the voltage of the monopole system in the model. It can be removed to disconnect the two DC systems.

As simulating the proposed grid would be too computationally intensive in this thesis the benchmark grid is reduced to just contain DC system 1. It is a point-to-point symmetric monopole HVDC system.The transmission distance between the two converters is 200km, made using DC cable. The full-bridge MMC topology is chosen as the VSC topology to investigate operation after a DC side fault. In order to simulate the MMC converter in Simulink, the parameters and the number of sub-modules need to be scaled to a lower value too, otherwise, the number of sub-modules of MMC will make the simulation to computationally intensive to simulate in a reasonable time. The next section explains the scaling method and the implications for the accuracy of the model.

5.3 Scaling method

DC system DCS 1 in "The CIGRE B4 DC Grid Test System" document are given in fig 5.1. The pu value of the converter is given in table 5.1, where the inductor L contains converter transformer inductance 18% and half the converter arm inductance (15%/2).

Table 5.1: The PU values of converter from CIGRE DC Grid System

Component	S	L	R	G	C
PU value	1	25.5%	1.00%	0.10%	60ms

The number of sub-modules is chosen to be 10 sub-modules in each arm, this allows a good compromise between producing reasonable waveforms and computation time of the simulation. Based on ten sub-modules per arm operating at a DC bus voltage of $20kV$, the AC RMS line voltage V_{AC} is set to $11kV$. Based on the Cigre P.U. values given in table 5.1 and using the per unit system given by equation (5.1), the absolute values of the modelled system can be given in Table 5.2.

$$
\begin{aligned}
Z_{ACbase} &= V_{AC}^2/S \\
Z_{DCbase} &= V_{DC}^2/S \\
L &= L_{PU} \times Z_{ACbase}/w \\
R &= R_{PU} \times Z_{ACbase}/w \\
G &= G_{PU}/Z_{DCbase} \\
C &= C_{PU}/Z_{DCbase} \\
C_{sm} &= N \times C/6
\end{aligned}
\tag{5.1}
$$

Table 5.2: The parameters for the simulation model

Component	S (MVA)	L (mH)	R (Ω)	G (μS)	C_{cell} (mF)
Values	20	4.9	0.0605	50	5

An alternative method for scaling the sub-module cell capacitance known as energy scaling is also possible. The energy scaling method ensures the ratio between the stored bulk energy inside the converter and the power rating remains the same in the two models. In equation (5.2) the ratio between stored bulk energy and rated power is defined as the time constant τ_W; typical values of this would be $30 - 40kJ/MVA$ [129, 141]. From equation (5.2) , equation (5.3) can be defined which shows the relationship between the sub-module capacitance in the reference system and the scaled system.

$$\tau_W = \frac{W_{ref}}{S_{ref}} = \frac{W_{scaled}}{S_{scaled}} \tag{5.2}$$

$$C_{scaled} = C_{ref} \frac{S_{scaled}}{S_{ref}} \frac{N_{ref}}{N_{scaled}} \frac{V_{Cref}^2}{V_{Cscaled}^2} \tag{5.3}$$

An example system from [129] is taken as a reference for comparison with the Cigre model; this is a 401-level MMC with a τ_W equal to $30kJ/MVA$. Using the energy scaling method previously described the scaled parameters are given in Table 5.3. As shown, the energy scaling capacitance is approximately the same as the value in Table 5.2.

Table 5.3: The energy scaling capacitance

Parameters	S (MVA)	N	V_C (V)	C (mF)	$\tau_W(kJ/MVA)$
Reference	1059	400	1600	10	30
Scaled	20	10	2000	5.1	30

The Cigre model also includes parameters for the transmission line; for the model used in this work this is scaled using the same per unit system as describe in equation (5.1). The new per unit length parameters are shown in Table 5.4.

Table 5.4: The CIGRE DC Grid System parameters of $\pm 200kV, 800MVA$ DC cable and the scaled $\pm 10kV, 20MVA$ parameters

Parameters	R $[\Omega/km]$	L $[mH/km]$	C $[\ \mu F/km]$	Max current $[A]$
$\pm 200kV$ CIGRE reference	0.0095	2.111	0.2104	1962
$\pm 10kV$ scaled	0.00095	0.2111	2.104	

5.4 Cable modelling methods

In the DC system modelled in this work, a 200 km long cable connects the two converters. A comparison of the published methods of cable modelling is provided here. To fully demonstrate DC fault protection strategies the fault transient in the grid must be considered which cannot be properly done without a suitable cable or line model.

There are several overhead lines or cable models found in the literature. They could be divided into categorise such as PI model, Distributed parameter model/Bergeron Model and Frequency dependent model [142–147]. These three models will be briefly introduced in the following sections.

5.4.1 PI section transmission line model

The PI section model represent the transmission line with lumped R, L and C components, as shown in figure 5.2. As the model is composed of electrical components it is easy to implement in simulation software and also physically in hardware. The required number of sections for the distributed parameter

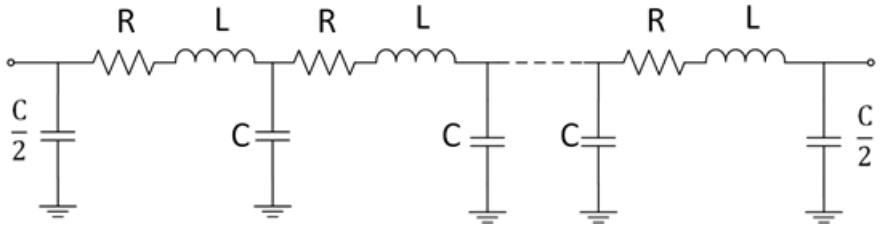


Figure 5.2: The configuration of PI model

model is a function of the frequencies of interest and the cable length. An equation for calculating the required number of sections is given in equation (5.4) [148].

$$f_{max} = \frac{N_{section} \times v}{8 l_{total}} \tag{5.4}$$

Where f_{max} is the approximation of the maximum frequency range represented by PI line model, $N_{section}$ is the number of PI sections, v is the propagation speed, l_{total} is the length of the line.

The result of this relationship means that as the cable length increases, for a given frequency range of interest, the required number of sections makes the model cumbersome. Additionally the insertion of discrete lumped components introduces extra resonant combinations between capacitors and inductors such that false resonances may be observed in the simulation model.

5.4.2 Distributed Parameter Model/Bergeron Model

The Bergeron model represents the line inductance and capacitance as distributed parameters while the cable resistance is represented as a lumped parameter [149]. The configuration of a distributed parameter model is shown in figure 5.3, and is defined in equation (5.5). It is accurate upto a certain frequency since all calculated parameters are calculated at this specific frequency. The Bergeron model is roughly equal to a PI model with infinite sections, thus when the transmission line is long enough (transport delay longer than simulation time step), the Bergeron model is preferable to the PI model [145].

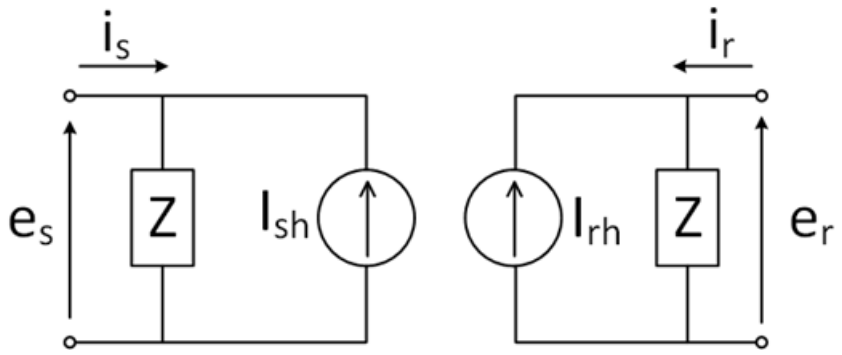


Figure 5.3: The configuration of a Distributed Parameter Model

$$
\begin{aligned}
I_{sh} &= (\frac{1+h}{2})[\frac{1}{Z}e_r(t-\tau) + hi_r(t-\tau)] + (\frac{1-h}{2})[\frac{1}{Z}e_s(t-\tau) + hi_s(t-\tau)] \\
I_{rh} &= (\frac{1+h}{2})[\frac{1}{Z}e_s(t-\tau) + hi_s(t-\tau)] + (\frac{1-h}{2})[\frac{1}{Z}e_r(t-\tau) + hi_r(t-\tau)] \\
Z &= Z_c + R/4 \\
\tau &= l\sqrt{L'C'} \\
h &= \frac{Z_c - R/4}{Z_c + R/4}
\end{aligned}
\tag{5.5}
$$

where e_r, e_s are the two terminal voltages, Z_c is the characteristic impedance, τ is the transport delay, l is the line length [149, 150].

5.4.3 Frequency Dependent Model

A limitation of the Bergeron model is that the line parameters are not frequency dependent; thus, the skin effect cannot be included into the Bergeron model. The frequency dependent model does not have this limitation as it is solved in the frequency domain, this allows the skin effect to be modelled. Frequency solved parameters are convolved into their equivalent time-domain characteristics. It represents R, L and C as distributed parameters. The frequency dependent model circuit and calculation are shown in figure 5.4 and equation (5.6).

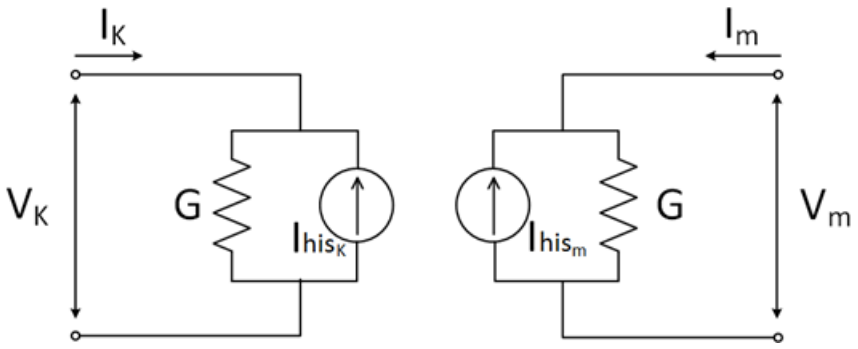


Figure 5.4: Norton equivalent for transmission line model

$$
\begin{aligned}
I_k(n) &= G \cdot V_k(n) - Ihis_k(n) \\
I_{kr}(n) &= I_k(n) - I_{ki}(n) \\
I_{ki}(n+1) &= H \star I_{mr}(n-\tau) \\
Ihis_k(n+1) &= Y_c^{'} \star V_k(n) - 2I_{ki}(n+1)
\end{aligned}
\tag{5.6}
$$

The frequency dependent (phase) model is based on the theory presented in [151]. A propagation function matrix H and the characteristic admittance matrix Y_c are calculated in the frequency domain, and then approximated and replaced by equivalent low order rational functions. The time domain implementation is shown in Figure 5.4. It is known as the most accurate model [152]. However, it was deemed too complicated/unfeasible to implement this model within the scope of this project, using the Simulink software chosen for the power electronics model. As as a consequence this model is not used in this thesis.

Where $\star$ indicates a convolution integral, $H = e^{-\sqrt{ZYl}}$ is the propagation

function matrix and $Y_c = Z^{-1}\sqrt{ZY}$ is the characteristic admittance matrix.

In the simulation work presented in this thesis simulation, the cable model is chosen to be the distributed parameter model. The reason is that the transmission line is 200km, which makes the transport delay $\tau = 4.215ms$. The simulation time step $T_s = 1e-5s$. Since $T_s \ll \tau$, the distributed model is able to model the cable adequately.

5.5 Non-switching model MMC converter

A non-switching model of the MMC converter is developed here to allow the efficient computation of multi-terminal DC grid behaviour. There are a number of simplified models of the MMC converter proposed in literature [78, 129, 153–155]; they can be divided into three groups.

The first one is referred to here as the efficient model, where the submodule circuit is simplified to Thevenin or Norton equivalent circuit [78, 153]. The second one is referred to as the averaged model, where the AC side arm legs are modelled as a controlled voltage source and on the DC side MMC is modelled as a controlled current source with capacitor [129]. The third one is referred to as the mathematical model, where the whole system is written in equations in the time-domain [154] or in the frequency-domain [155]. These methods each have their own advantages from different aspects. To enable the same implementation of the control system to be used for

the switching model and for the non-switching model the efficient modelling method is employed. This allows a fair comparison between the models to be made.

5.5.1 Theory of non-switching efficient model of the MMC

In this section a Thevenin equivalent circuit is presented; initially the model is developed and results presented for the condition where there are always two IGBTs gated on is considered for both normal operation and faulted operation. Following this the condition where the IGBTs are blocked is considered.

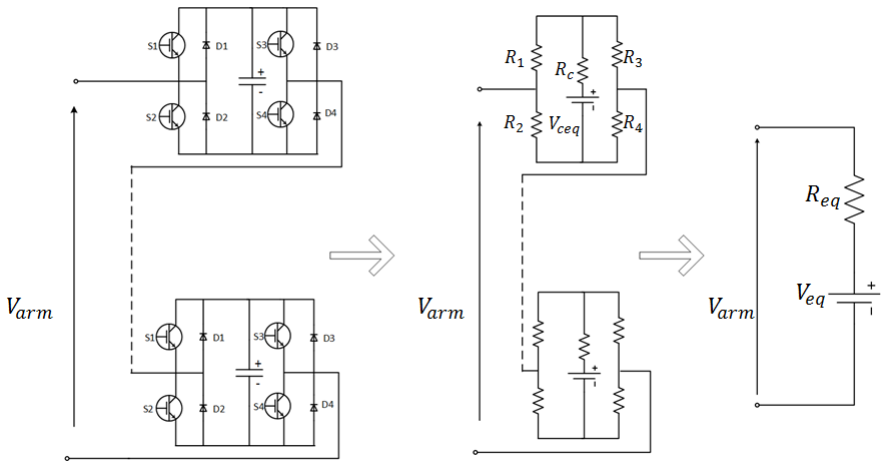


Figure 5.5: Thevenin equivalent circuit for one arm of the MMC

As shown in figure 5.5, the full-bridge sub-module capacitor is replaced by Thevenin equivalent circuit and eventually the arm is modelled as a single

Thevenin equivalent circuit [78]. The sub-module capacitor model values of the resistor and voltage source are calculated based on equations (5.7) and (5.8).

$$\begin{aligned} V_c(t) &= \frac{1}{C}\int I_c(t) \\ &\approx V_c(t-\Delta T) + \frac{1}{C}(\frac{I_c(t-\Delta T)+I_c(t)}{2})\Delta T \\ &= V_c(t-\Delta T) + \frac{\Delta T}{2C}I_c(t-\Delta T) + \frac{\Delta T}{2C}I_c(t) \end{aligned} \tag{5.7}$$

Let $R_c = \frac{\Delta T}{2C}, V_{ceq}(t-\Delta T) = V_c(t-\Delta T) + \frac{\Delta T}{2C}I_c(t-\Delta T)$. Then,

$$V_c(t) = R_c I_c(t) + V_{ceq}(t-\Delta T) \tag{5.8}$$

The sub-module output voltage, figure 5.6 shows the equivalent circuit. Using the simplified model of an IGBT and diode described in chapter 3 section 3.3.5, the on-state resistance of an IGBT with diode is R_{on}, the off-state resistance is R_{off} and $R_{on} \ll R_{off}$. The output voltage of sub-module Vsm, and the equivalent resistance R_{sm} are dependent on state input to the sub-module, s. It has three states for one sub-module: $1, 0, -1$. Where $s = 1$ is used to represents positive sub-module output voltage;$s = 0$ represents Zero state of the sub-module; $s = -1$ represents sub-module negative sub-module output voltage. The sub-module equivalent circuit can be calculated as equation (5.9). According to the state of s, equation (5.9) can be rewritten as (5.10).

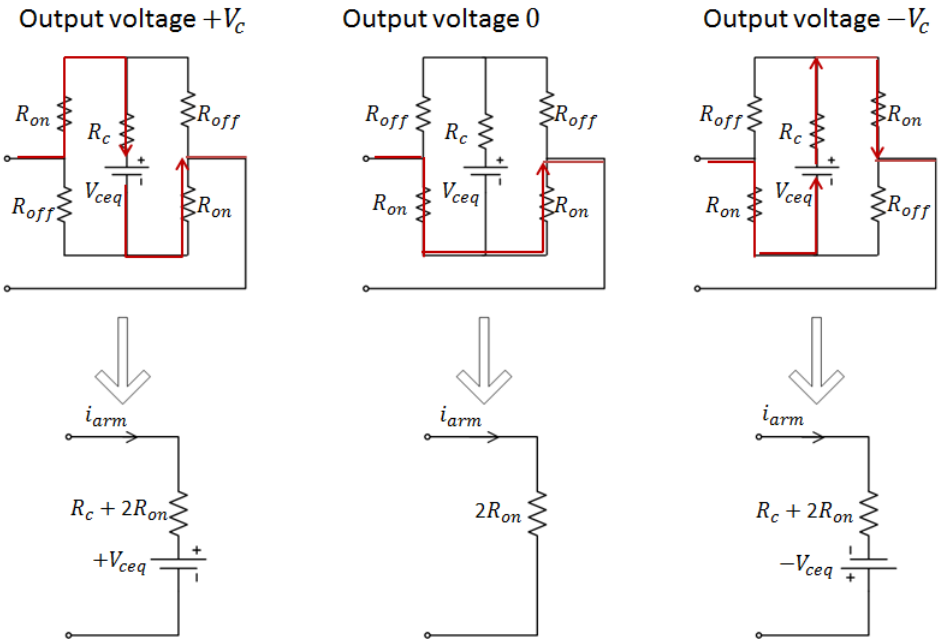


Figure 5.6: Thevenin equivalent circuit for one sub-module of MMC

$$V_{sm}(t) = \begin{cases} (R_c + 2R_{on}) \times I_{arm}(t) + V_{ceq}(t - \Delta T) & \text{if } s = 1 \\ 2R_{on} \times I_{arm}(t) & \text{if } s = 0 \\ (R_c + 2R_{on}) \times I_{arm}(t) - V_{ceq}(t - \Delta T) & \text{if } s = -1 \end{cases} \tag{5.9}$$

$$\begin{aligned} V_{sm}(t) &= [(R_c + 2R_{on}) \times |s| + 2R_{on} \times (1 - |s|)] \times I_{arm}(t) + s \times V_{ceq}(t - \Delta T) \\ &= (R_c \times |s| + 2R_{on}) \times I_{arm}(t) + s \times V_{ceq}(t - \Delta T) \end{aligned} \tag{5.10}$$

Summing the total sub-modules in an arm, N, the total arm voltage equa-

tion is given by (5.10); the arm voltage, including resistive voltage drops, can be represented as in equation (5.11). As shown in figure 5.5, the non-switching model replaces each arm of the MMC converter by a resistor R_{eq} and controlled voltage source V_{eq}.

$$\begin{aligned} V_{arm} &= \sum_{i=1}^{N} V_{sm_i}(t) \\ &= (R_c \times \sum_{i=1}^{N} |s_i| + 2R_{on}) \times I_{arm}(t) + \sum_{i=1}^{N} s_i \times V_{ceq_i}(t - \Delta T) \end{aligned} \tag{5.11}$$

5.5.2 Comparison simulation results of switching model and non-switching model in steady state

In the following simulation results, the arm circuit of an MMC is represented by the model described in the previous section; i.e. a controlled voltage source where the magnitude V_{arm} is calculated according to equation (5.11). The variable resistor is represented by a controlled voltage source, where the current provides the control feedback. The simulation circuit is shown in figure 5.7, R_{eq}, V_{eq} are given in equation (5.12). Although the output electrical voltage is the sum of the sub-modules voltage, each sub-module voltage is calculated separately; thus the individual voltage is available to be used for the sub-module capacitor balancing scheme described in chapter 4 section 3.

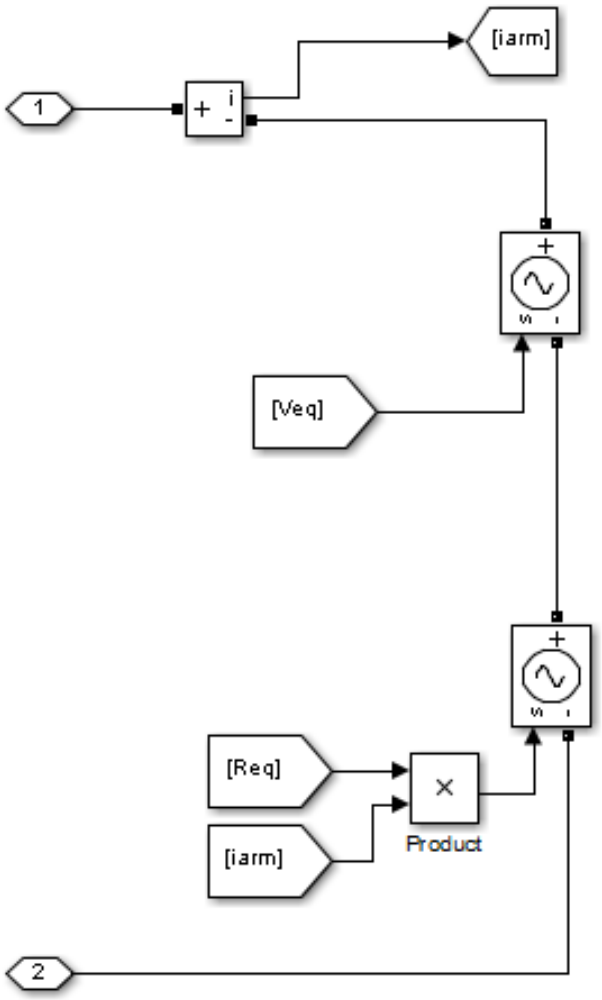


Figure 5.7: Non-switching model of one MMC arm

$$R_{eq} = (R_c \times \sum_{i=1}^{N} |s_i| + 2R_{on})$$
$$V_{eq} = \sum_{i=1}^{N} s_i \times V_{ceq_i}(t - \Delta T) \tag{5.12}$$

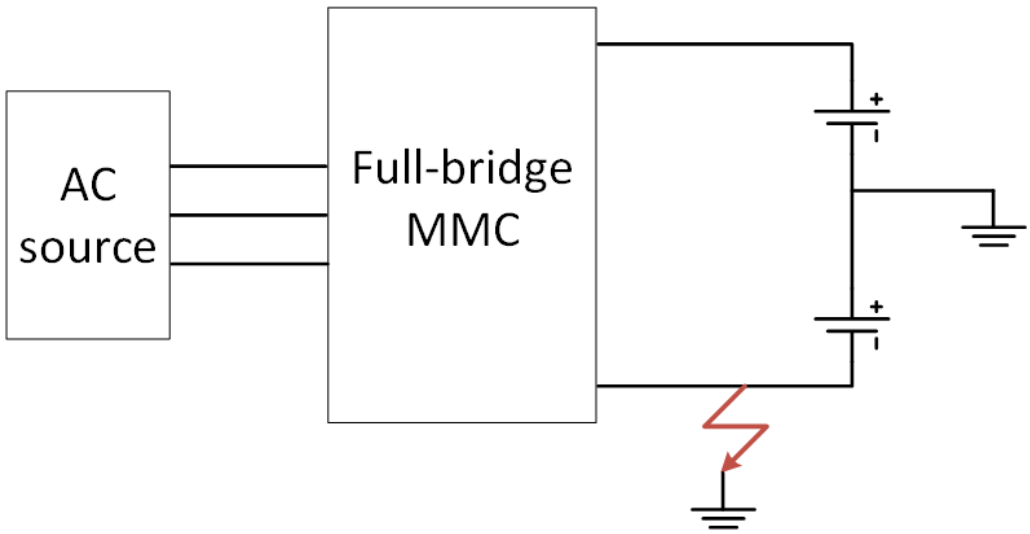


Figure 5.8: MMC simulation circuit of switching and non-switching model comparison

Simulation results are presented here to show a comparison between the switching and non-switching model during normal operation and after a line-to-ground fault; a full set of simulation results are presented in chapter 6. The simulation circuit is shown in figure 5.8. A three phase MMC converter is connected to DC voltage source on the DC side. A line-to-ground fault is set, all reference and control signals remain the same after the fault happens. Both the switching and non-switching MMC models use this configuration in order to compare them. The simulation results one period before and after the fault are illustrated in figure 5.9. In these simulation results the rated

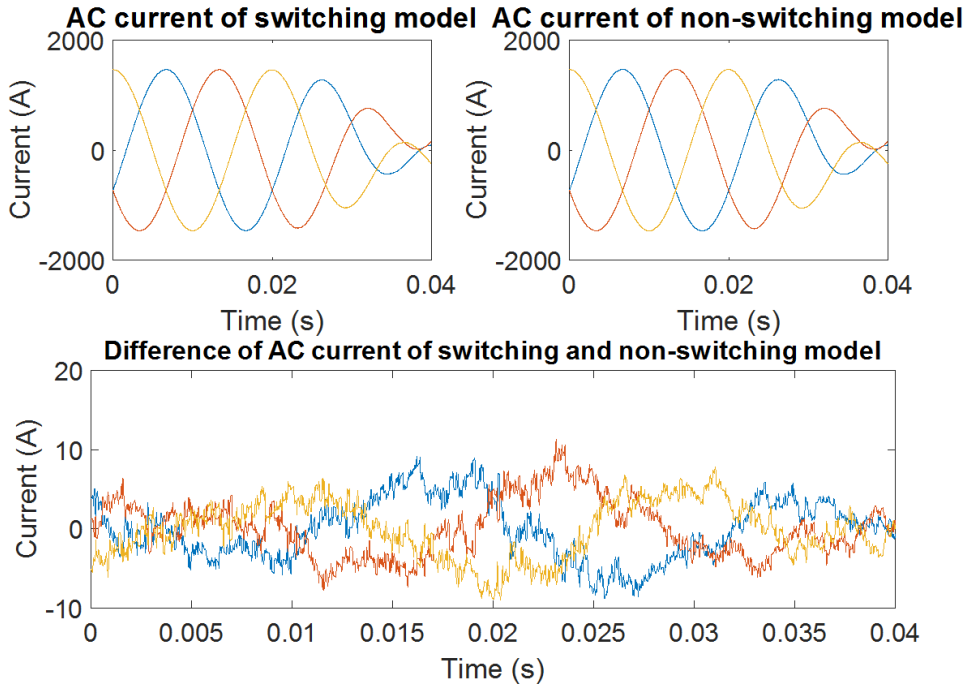
conditions are as table 5.2, i.e. DC side voltage is $V_{dc} = 20kV$, power $P = 20MW$. Discussion of thes results focuses on the comparison of the models. A discussion of the fault response is the focus of the following chapter.

Figure 5.9 presented the AC current, DC current, one phase arm current and one phase sub-module capacitor voltage simulation results and the difference of switching and non-switching model simulation results. For the sub-module capacitor voltage, the difference is calculated based on the average magnitude of one arm sub-modules. As shown, the difference between the two models is small.

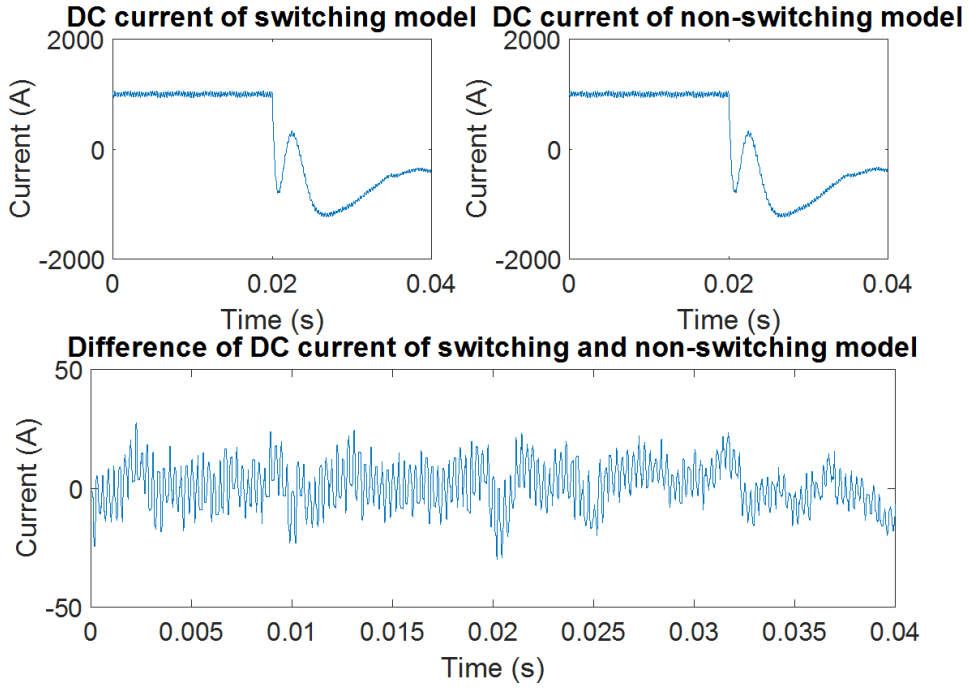
Simulation for post fault operation is also shown for the condition where one pole is grounded as described in chapter 3 section 3.3.2. The simulation circuit is shown in figure 5.10. The simulation results are shown in figure 5.11. Under these condition the DC side voltage is $V_{dc} = 10kV$, power $P = 10MW$ and $P_e = 0.5$. The simulation results for $P_e = 1$ are shown in figure 5.12. As can be seen in these figures, the non-switching model is close to the switching model in steady state operation and transient after line-to-ground fault.

5.5.3 Non-switching model of MMC when all IGBTs blocked

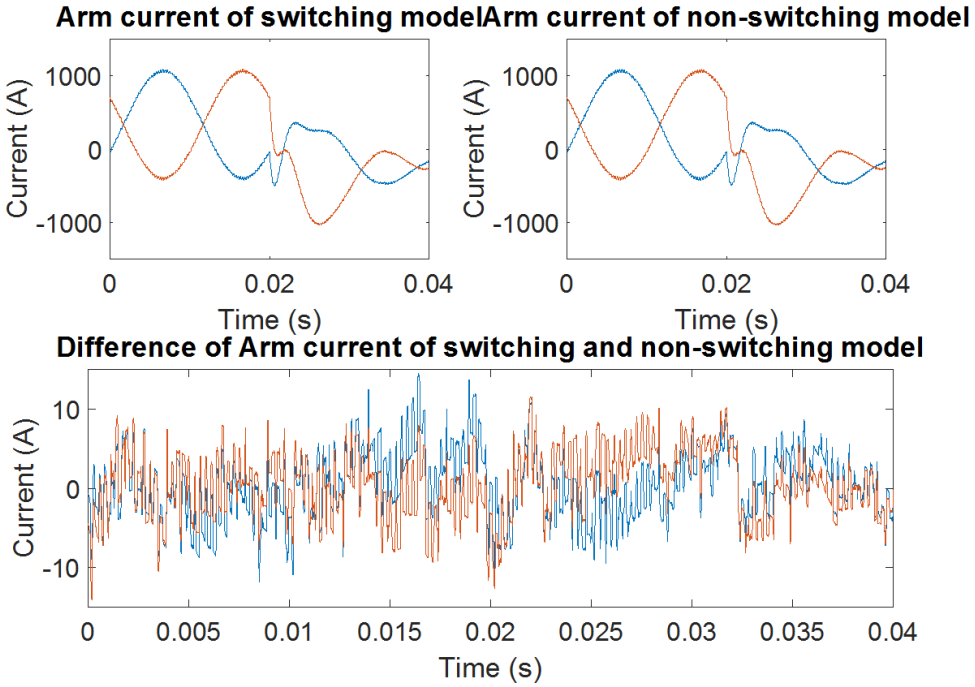
Provided there is sufficient negative available voltage from the full-bridge sub-modules, the MMC is able to cut the fault current by opening all IGBTs. For this condition the equivalent circuit is now extended. The simulation



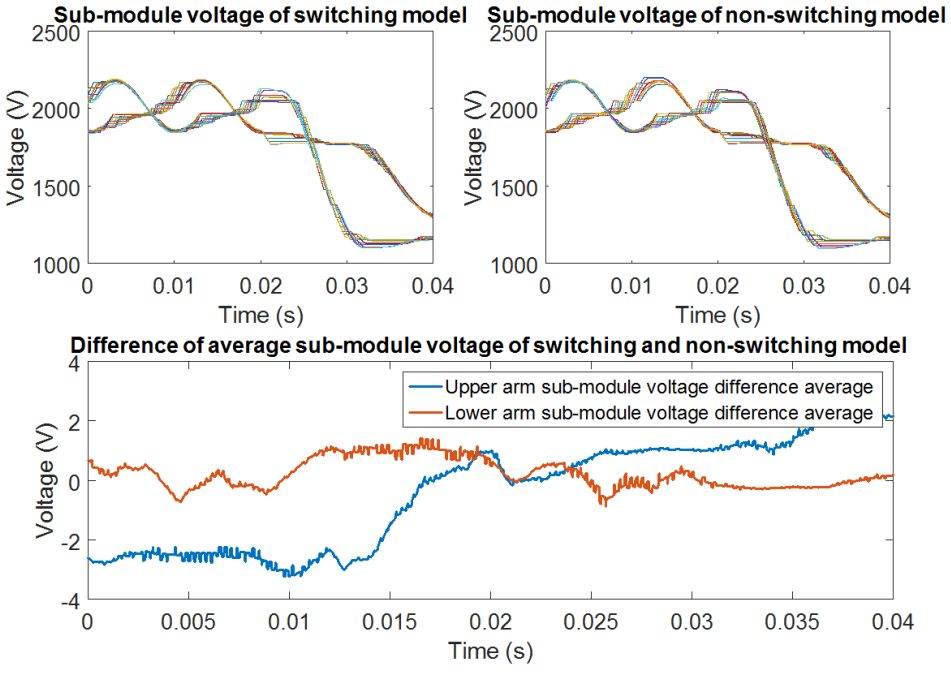
(a) AC current



(b) DC current



(c) Arm current



(d) Sub-module voltage

Figure 5.9: Simulation results comparison between switching model and non-switching model in normal operation and after line-to-ground fault

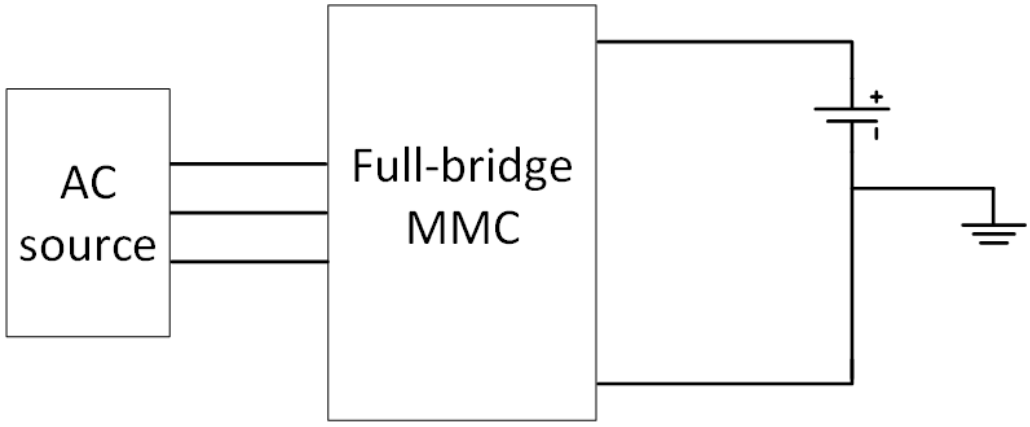
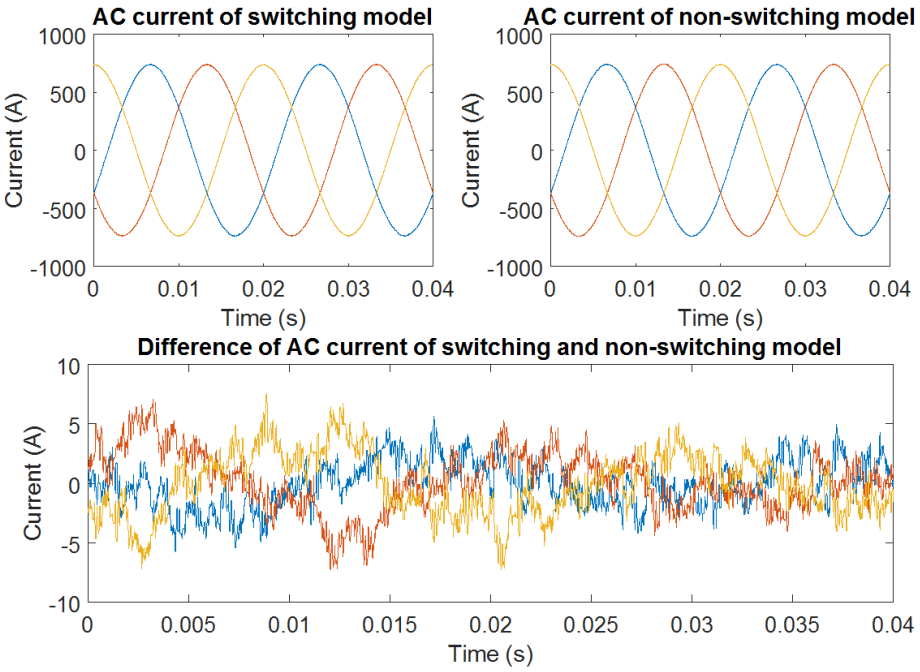


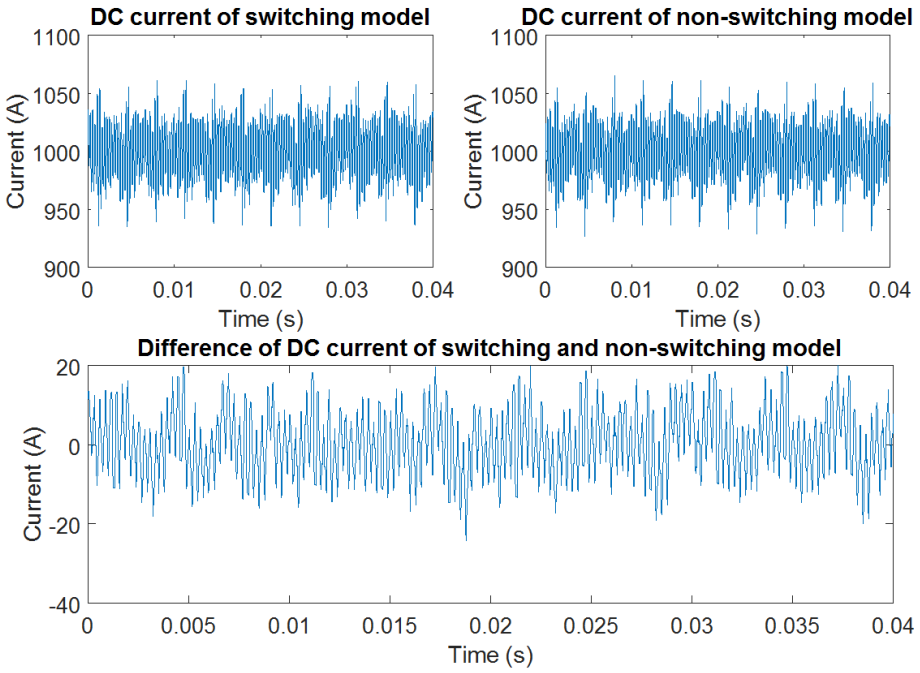
Figure 5.10: MMC simulation circuit of switching and non-switching model comparison for post fault operation

circuit is shown in figure 5.13, the ideal switches are used to switch the circuit according to the IGBT blocked signal, $IGBTB$. In normal operation $IGBTB = 1$, at this time the equivalent circuit is the same as in figure 5.10; when all IGBTs are blocked, $IGBTB = 0$, the equivalent circuit is the same as in figure 5.14. However, this model extension increased the number of switching components. It is only used when investigate the IGTB blocking condition.

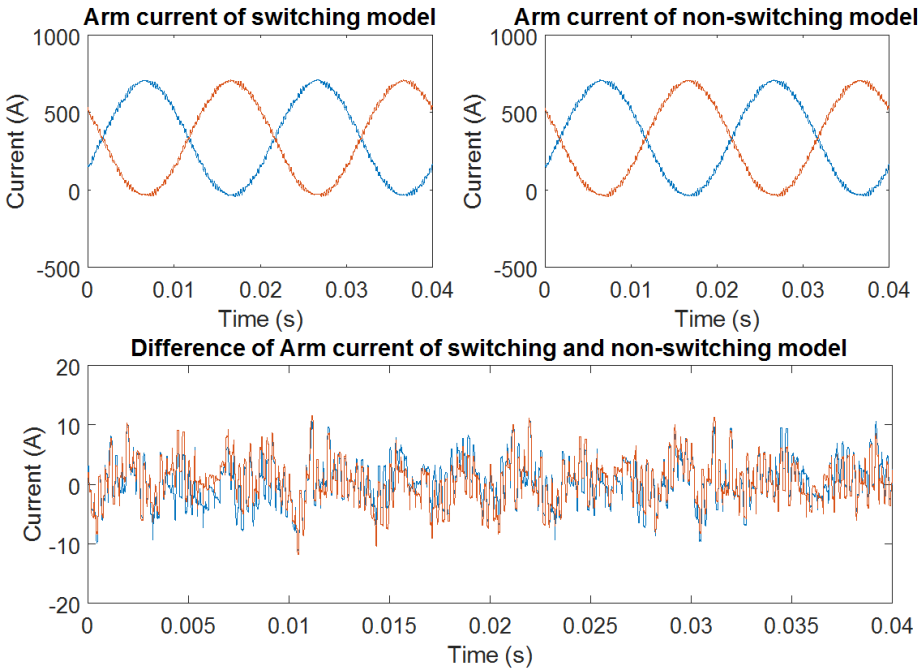
In order to compare the simulation results of non-switching and switching model when all IGBTs are blocked, the normal operation MMC circuit is used as before. The line-to-ground fault occurs at $t = 0.2s$, and at time $t = 0.3s$, all IGBTs are blocked. The simulation results are presented in figure5.15. As shown, before all IGBTs are blocked at $t = 0.3s$, the difference between the two models is small as before. After $t = 0.3s$, there is an overshoot after the line current reaches zero, as shown in figure 5.16. In



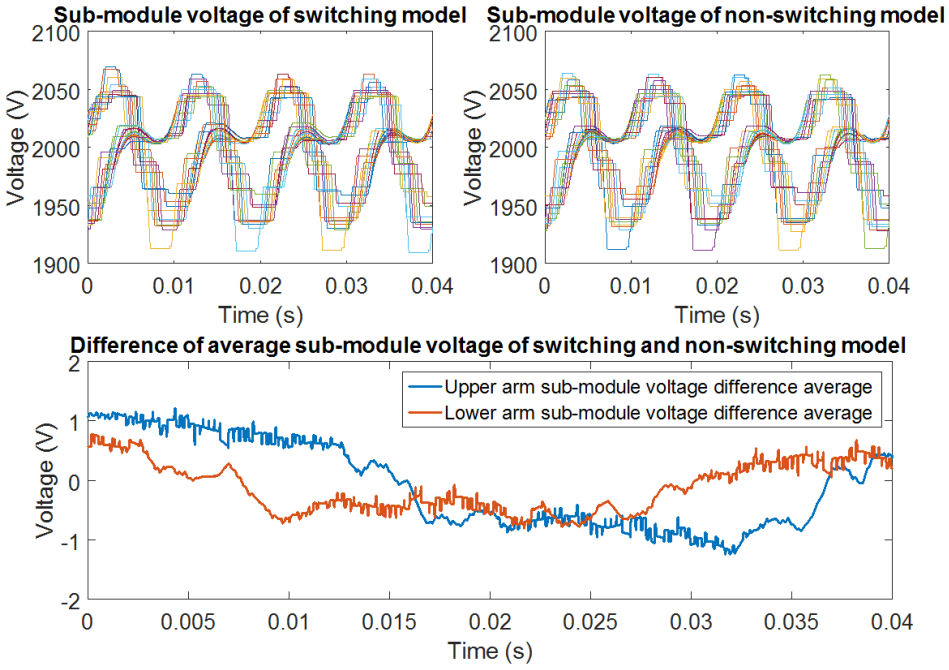
(a) AC current



(b) DC current

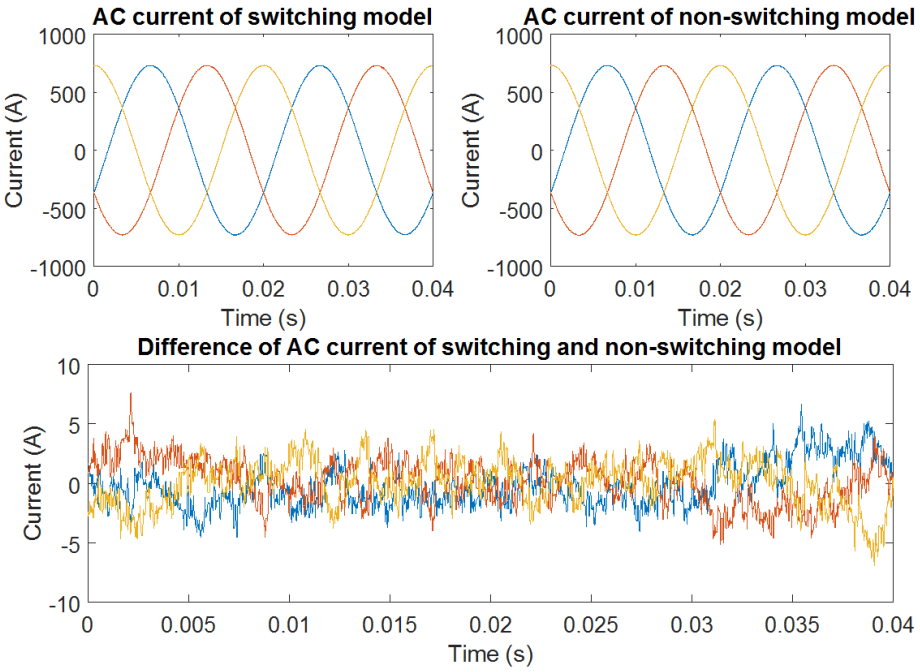


(c) Arm current

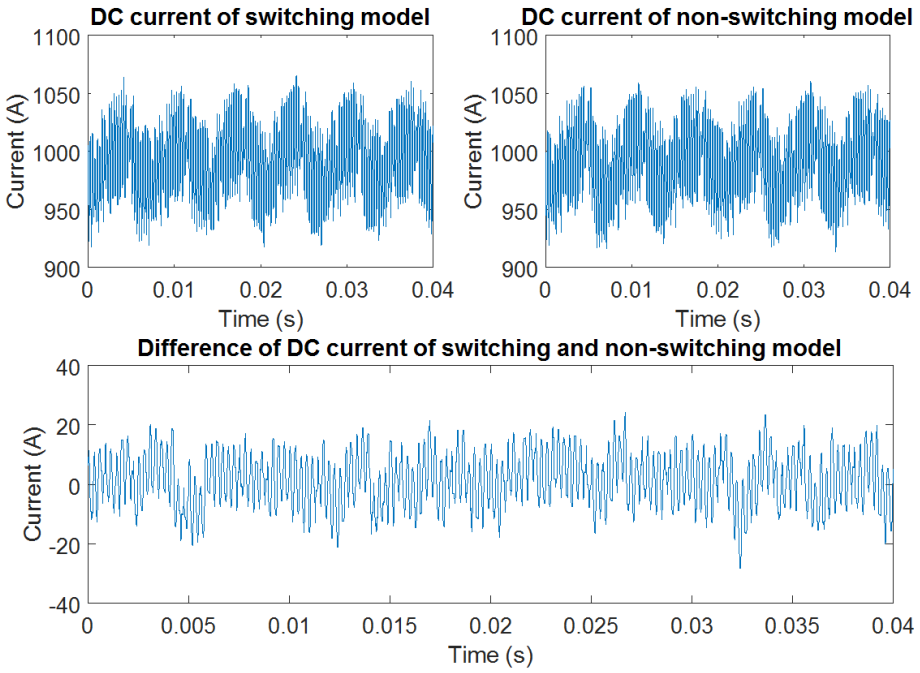


(d) Sub-module voltage

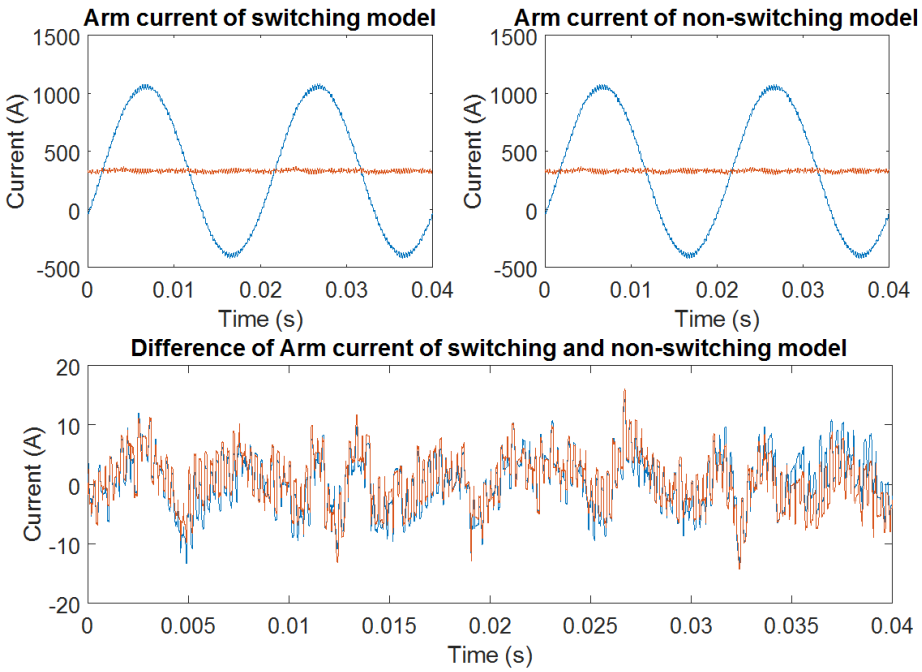
Figure 5.11: Simulation results comparison between switching model and non-switching model in post-fault operation when $P_e = 0.5$



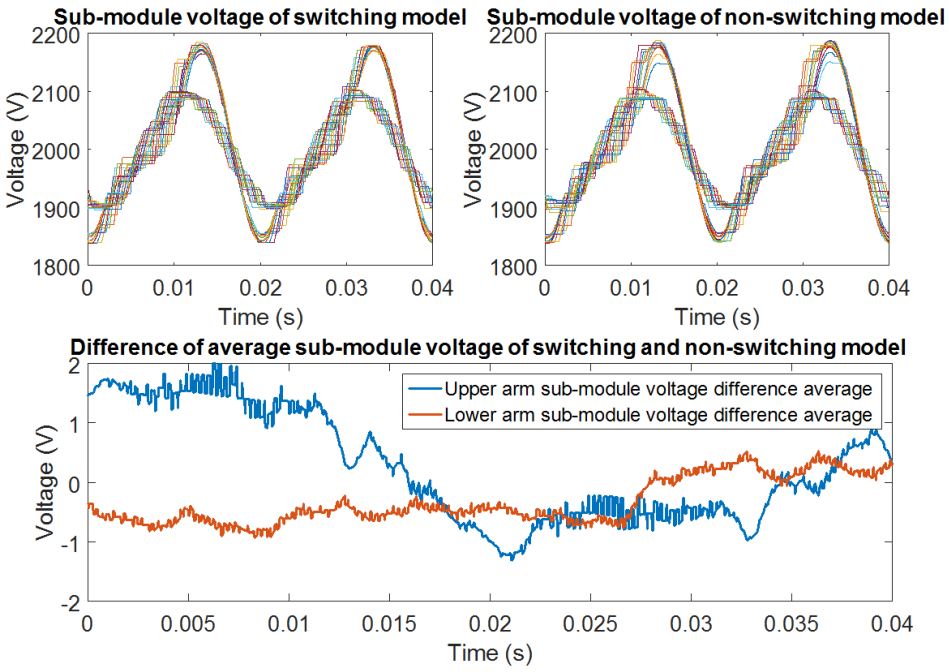
(a) AC current



(b) DC current



(c) Arm current



(d) Sub-module voltage

Figure 5.12: Simulation results comparison between switching model and non-switching model in post-fault operation when $P_e = 1$

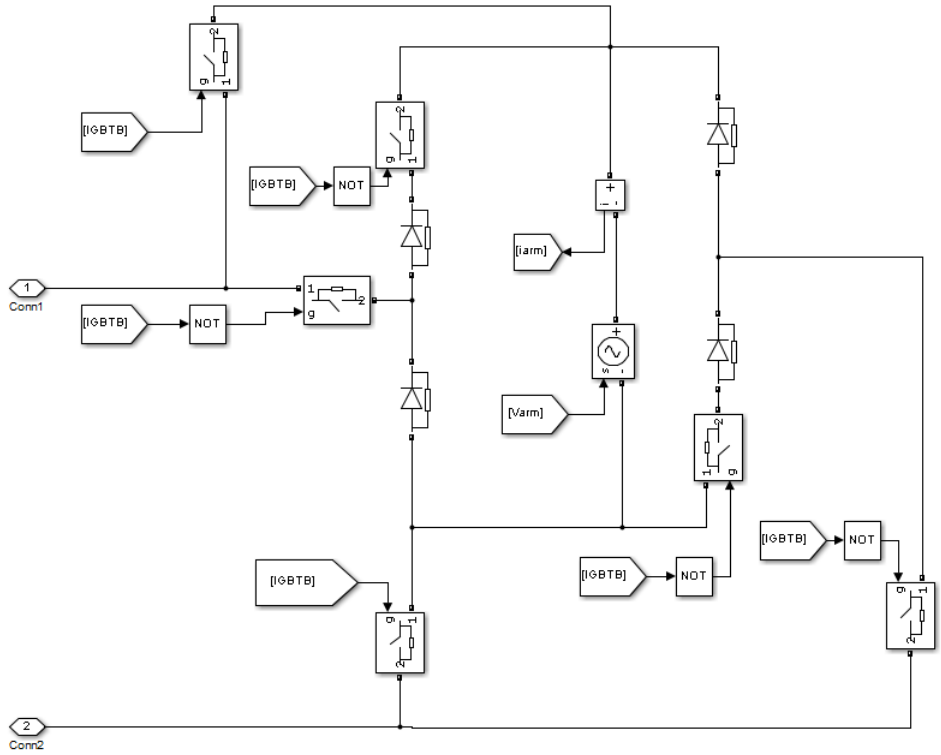


Figure 5.13: MMC arm simulation circuit of non-switching model with IGBTs blocked capability

the simulation circuit, the ideal switch is modelled as a large resistor when opened. As a result, the current is not completely cut off. Nevertheless, as a percentage error the overshoot is small, this non-switching model provides the similar simulation results to the switching model.

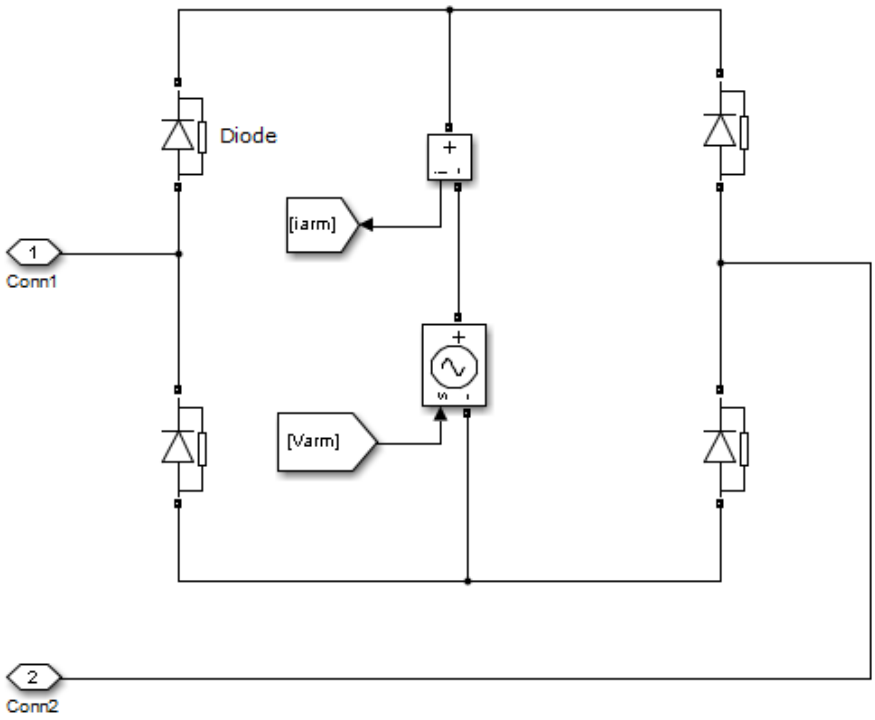
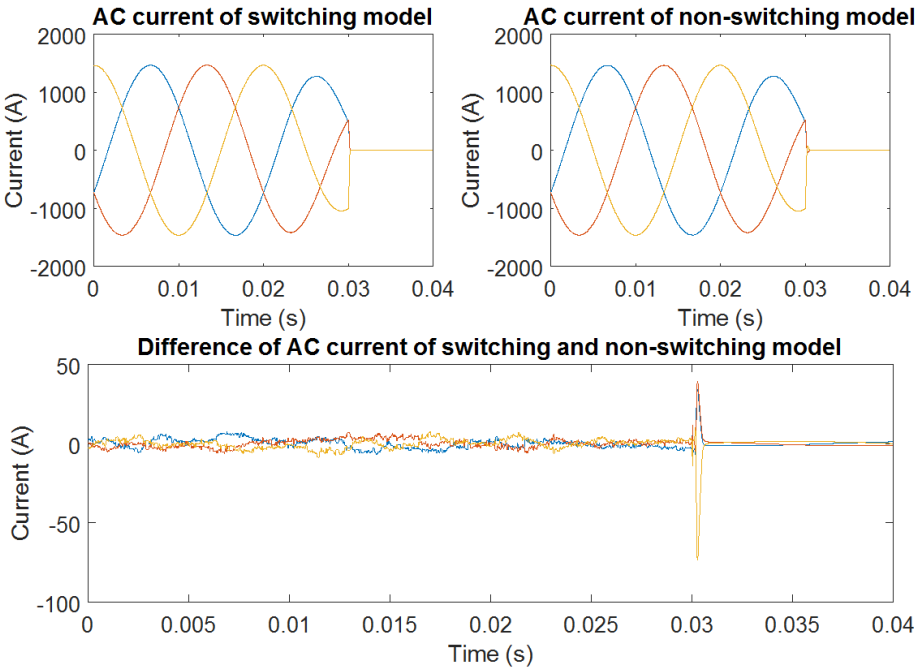
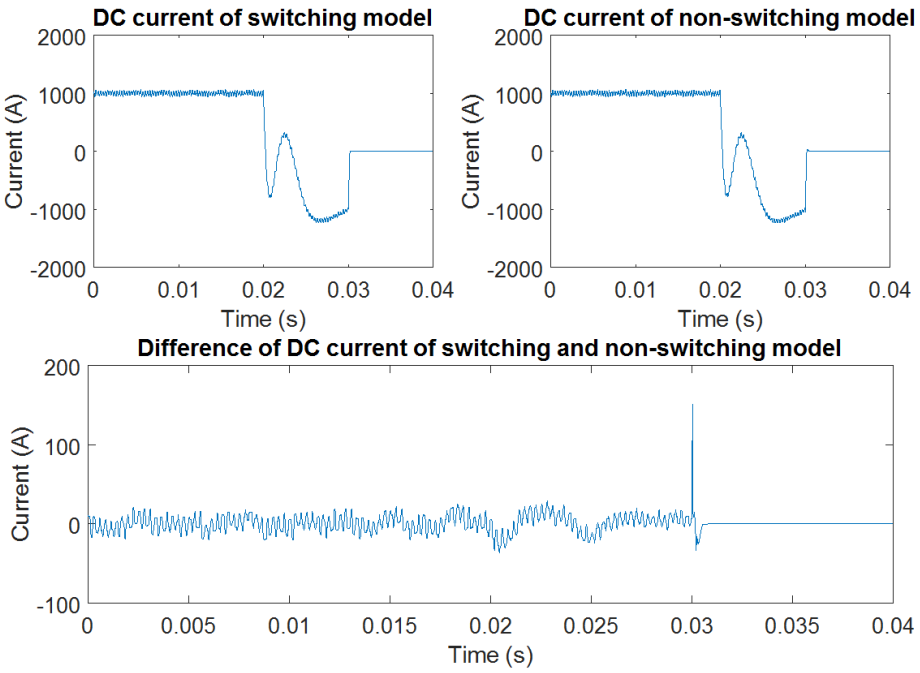


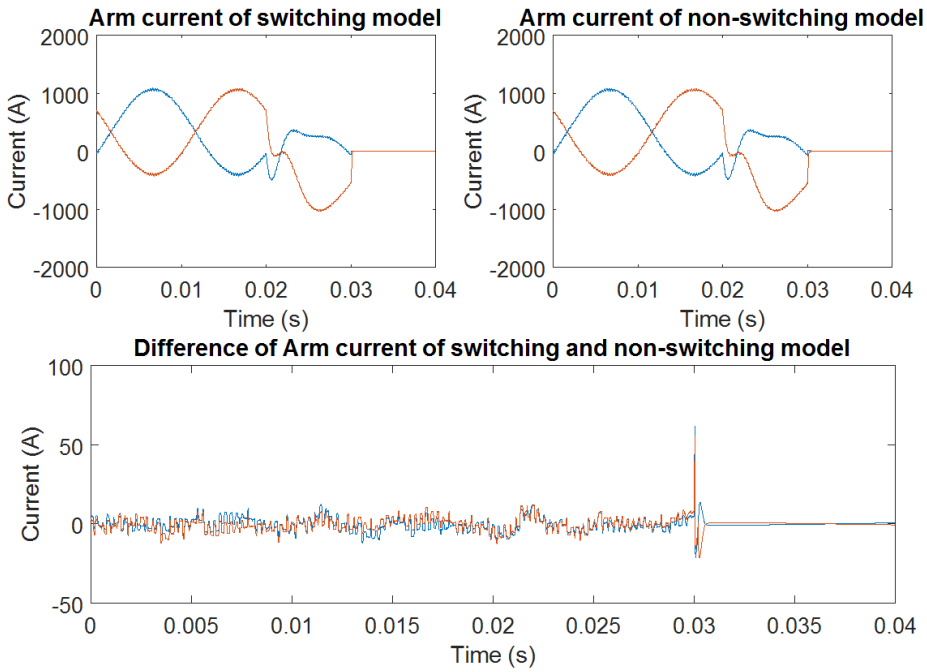
Figure 5.14: MMC arm simulation circuit of non-switching model when all IGBTs opened



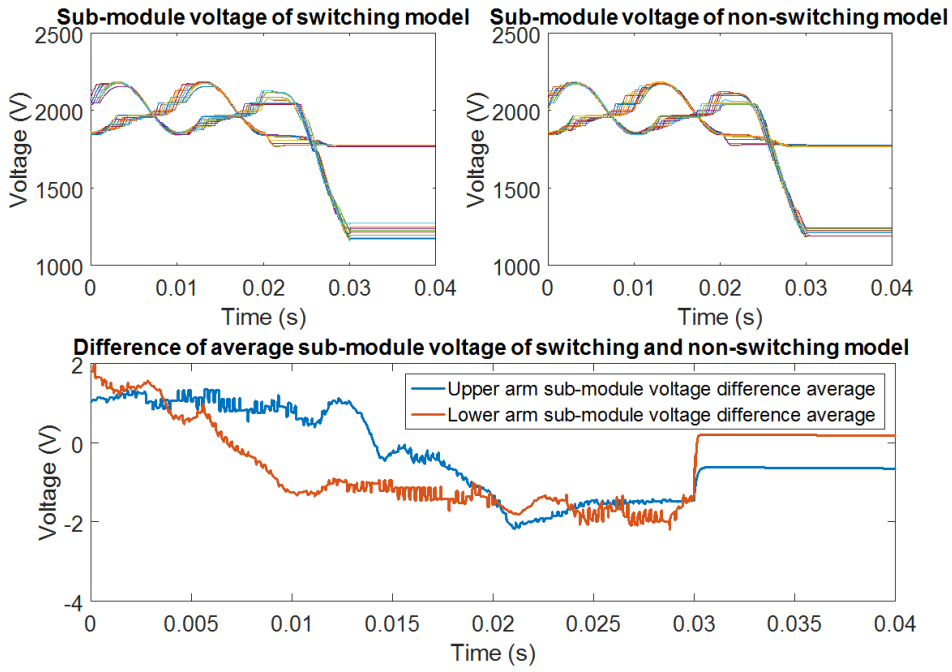
(a) AC current



(b) DC current



(c) Arm current



(d) Sub-module voltage

Figure 5.15: Simulation results comparison between switching model and non-switching model with IGBTs blocked capability

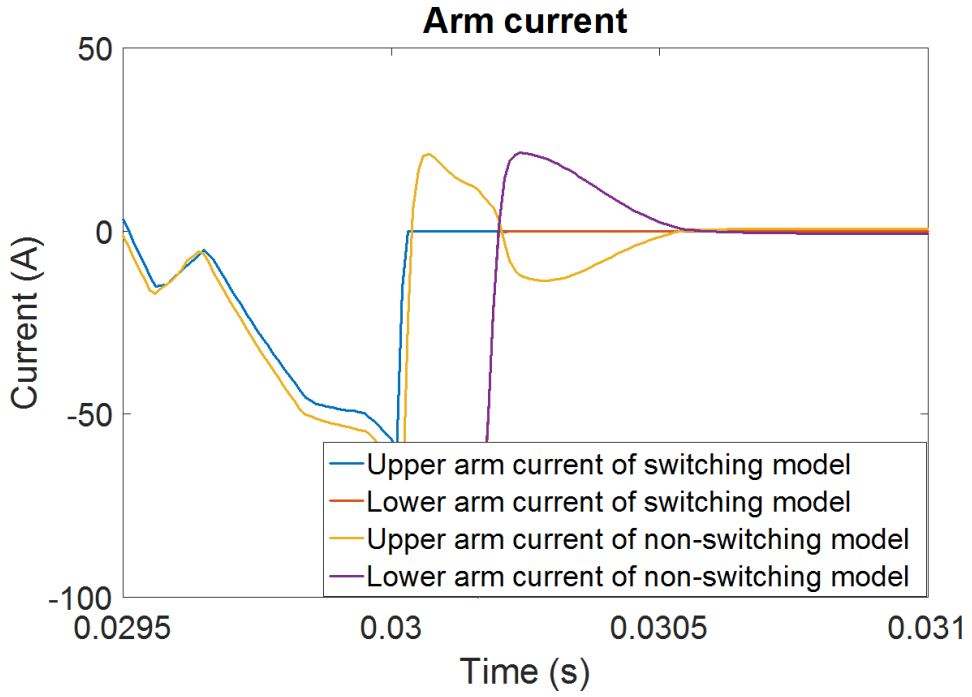


Figure 5.16: MMC arm current of switching and non-switching model zoom in

5.6 Summary

This chapter has described modelling of a 4-terminal DC grid which consists of a 21-level MMC converter. It will be used to verify the DC fault ride through techniques presented in chapter 3. The MMC component and cable parameters are calculated based on the CIGRE model. A distributed parameter transmission line model has been chosen to be used. A non-switching MMC model has also been developed to reduce the computation time in simulating a complex DC grid. In the following chapter, the non-switching model is used for simulation.

Chapter 6

Simulation results

6.1 Introduction

To verify the theoretical work presented in this thesis a 21-level full-bridge MMC converter has been simulated. This chapter presents the simulation results for normal operation and post fault operation of a point-to-point HVDC system with second harmonic elimination and sub-module capacitor voltage energy control.

6.2 Simulation circuit and parameters

A point-to-point HVDC system is implemented using Matlab Simulink so that the post-fault operation method developed in Chapter 3 and the control schemes in Chapter 4 can be applied. The aim is to verify the analysis presented in chapter 3. These simulation studies will be the full switching model for the proposed system.

The simulation circuit for normal operation is shown in figure 6.1 and the simulation circuit for post fault operation is shown in figure 6.2. During faulted operation it is assumed that the line-to-ground fault occurs in the middle of negative pole cable. Both MMC converters are populated with full-bridge sub-modules. The control scheme for the point to point HVDC system is as is presented in [22] and described in chapter 2 section 2.2.2. One MMC converter is operated in power mode; i.e. it injects as much current as is needed into the grid to achieve the power demand, while operating within the limits of the converter. The other converter controls the DC voltage with closed loop voltage control, in a multi-terminal system this would absorb any difference in power from the power nodes and inject this onto its local AC grid. The detail control loop has shown in the end of chapter 4.

Figure 6.3 shows the arrangement for faulted operation of post line-to-line fault operation circuit. Again the fault is assumed happened at the middle of the cable. In the simulation, the middle point of the faulted cable is assumed constantly connected to the ground. In theory, the converter can also reconstruct the grounding point at the faulted pole. However, this may not prove to be practical as it may accelerate corrosion in local pipework.

The simulation parameters are calculated based on the scaling method described in Chapter 5. The MMC converter parameters are presented in table 6.1 and the cable between the converters are presented in table 6.2. As shown, the power demand for normal operation is 20MW and for line-to-

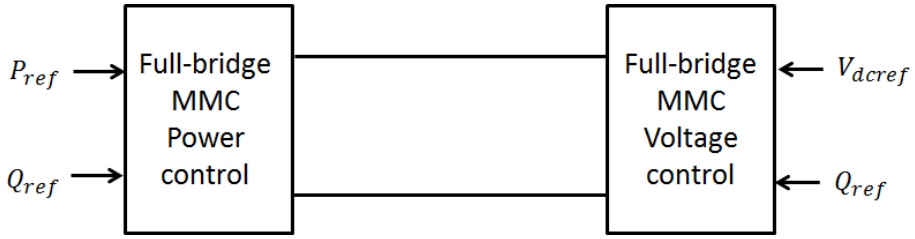


Figure 6.1: Simulation circuit of normal operation

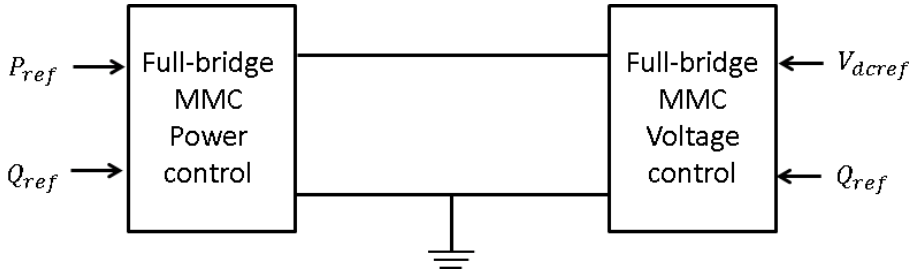


Figure 6.2: Simulation circuit of post line-to-ground fault operation

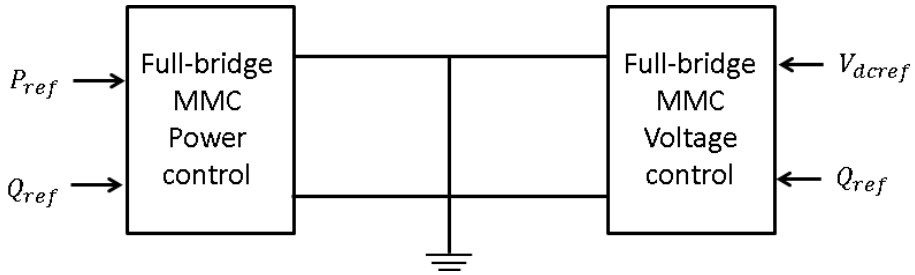


Figure 6.3: Simulation circuit of post line-to-line fault operation

ground post fault operation is 10MW. The operation modes table is repeated here in table 6.3.

Table 6.1: Simulation parameters used for MMC converter in point to point scheme

P	$20MW$ for normal operation $20MW$ for faulted operation mode 1 $10MW$ for faulted operation mode 2-5
Q	$0var$
N	10
V_{dc}	$20kV$
$V_{acLLrms}$	$11kV$
R_s	0.0605Ω
L_s	$3.5mH$
L_c	$2.9mH$
C_{sm}	$5mF$
$V_{sminitial}$	$2kV$
T_s	$1e^{-5}s$

Table 6.2: Simulation parameters used for transmission cable in point to point scheme

R'	L'	C'	$Length$
0.00095Ω	$0.2111mH$	$2.104\mu F$	$200km$

Table 6.3: Different modes of operation

	V_{dc}	Available power	Cable stress	Transformer stress	Available voltage requirement
Norm Op	1pu	1pu	0.5pu	0pu	[0,1]pu
Fault Op1	1pu	1pu	1pu	0.5pu	[0,1]pu
Fault Op2	0.5pu	0.5pu	0.5pu	0.25pu	[-0.25,0.75]pu
Fault Op3	0.5pu	0.5pu	0.5pu	0pu	[-0.5,1]pu
Fault Op4	0.5pu	0.5pu	0.5pu	0.125pu	[-0.375,0.875]pu
Fault Op5	0.5pu	0.5pu	0.5pu	0.375pu	[-0.375,0.875]pu

6.3 Full-bridge MMC steady state normal operation results

Figure 6.4 shows the AC current, arm voltage and sub-module capacitor voltage of one phase, the dc current and the positive pole and negative pole cable voltage to ground. The cable voltage and current simulation results passed a low pass filter in order to show the average magnitude. As should be expected, in steady state normal operation arm voltages are positive all the time and the sub-modules act as half-bridges. The upper and lower arm sub-module capacitor voltages are symmetric; the cable voltages are $\pm\frac{1}{2}V_{dc}$ respectively. The sub-module capacitor voltages remain converged, demonstrating that the rotation scheme is balancing the sub-modules correctly.

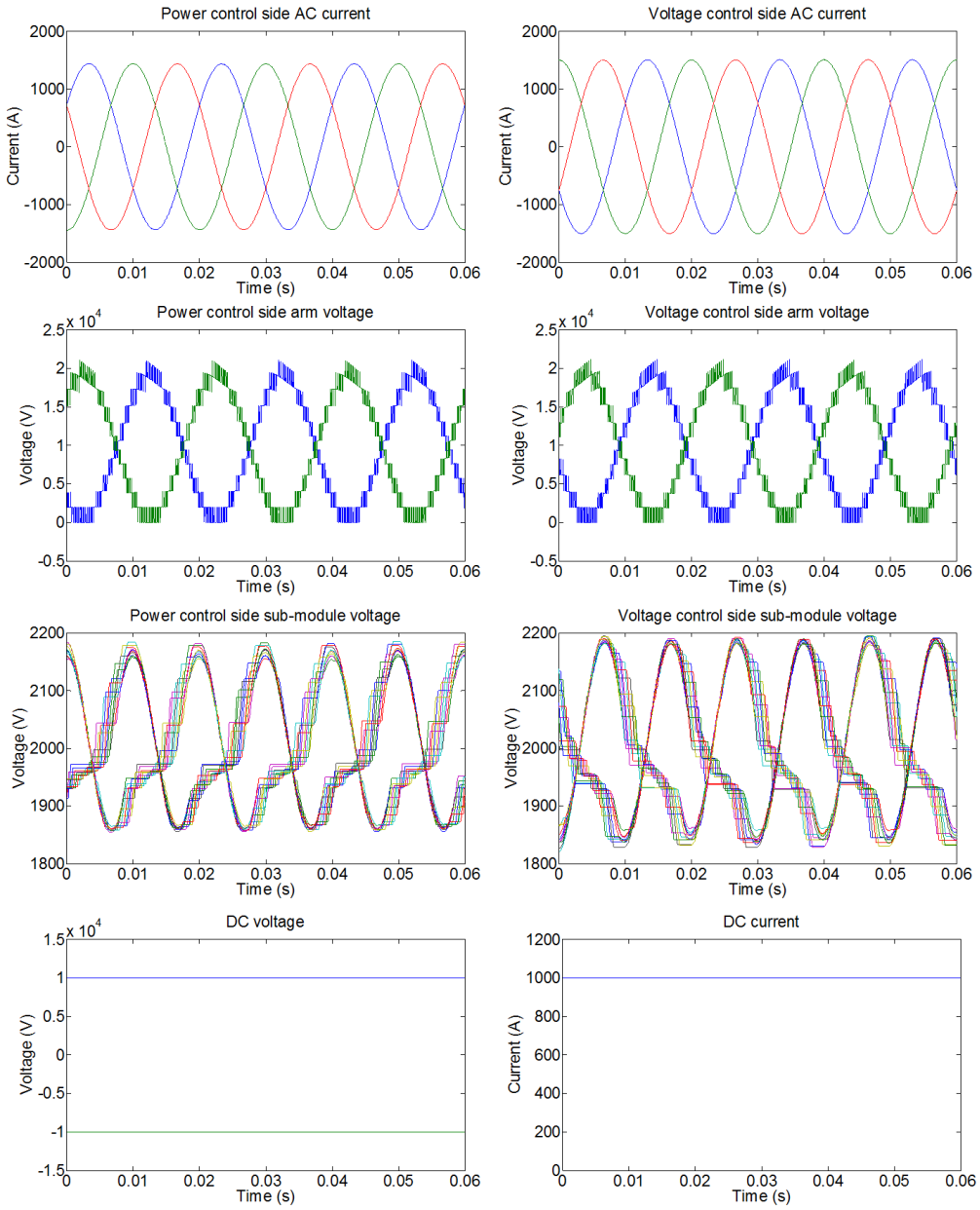


Figure 6.4: Simulation results of normal operation

6.4 Full-bridge MMC steady state operation after line-to-ground fault

Figure 6.5 shows the simulation results of post fault operation mode 1 where the power demand and dc voltage reference are the same as normal opera-

tion. Assuming a line-to-ground fault occurs at the middle of the negative pole cable, the faulted cable is connected to ground as shown in figure 6.2. The AC current, arm voltage and sub-module capacitor voltage are the same as in figure 6.4; this is to be expected as the only difference is the shifting of the ground reference, which can be seen in positive and negative pole cable voltages. To operate in this mode the cable rating and converter plant needs to have twice the DC voltage rating it would need for normal operation. The dc voltage stress applied in common mode to the transformer is $\frac{1}{2}V_{dc}$, thus the transformer insulation would also have be designed to withstand this stress. However, if the cable voltage can not exceed the rated value, the post fault operation modes 2 to 5 can be used.

Simulation results of post fault operation mode 2 where $P_e = 0.5$ are shown in figure 6.6. Under this operation mode, both the power demand and DC voltage are set to be the half of the rated magnitude, as they are for post fault operation modes 3 to 5. As the power has been reduced by half, the AC current has also been reduced to half the magnitude of that in figure 6.4 and 6.5. The positive pole voltage to ground is $+V_{dc}$. The arm voltage range is approximately $[-\frac{1}{4}V_{dc}, \frac{3}{4}V_{dc}]$, but the exact range depends on the AC voltage magnitude. This means the dc voltage stress on the ac side of the transformer is $\frac{1}{4}V_{dc}$. The transformer DC voltage stress is equal to the DC component of lower arm voltage as analysed. In figure 6.6, the DC voltage of lower arm is $\frac{1}{4}V_{dc}$. The arm voltage of the power control side and voltage control side is slightly different due to the DC voltage drop in the transmission cable. On the voltage control side, there are two sub-

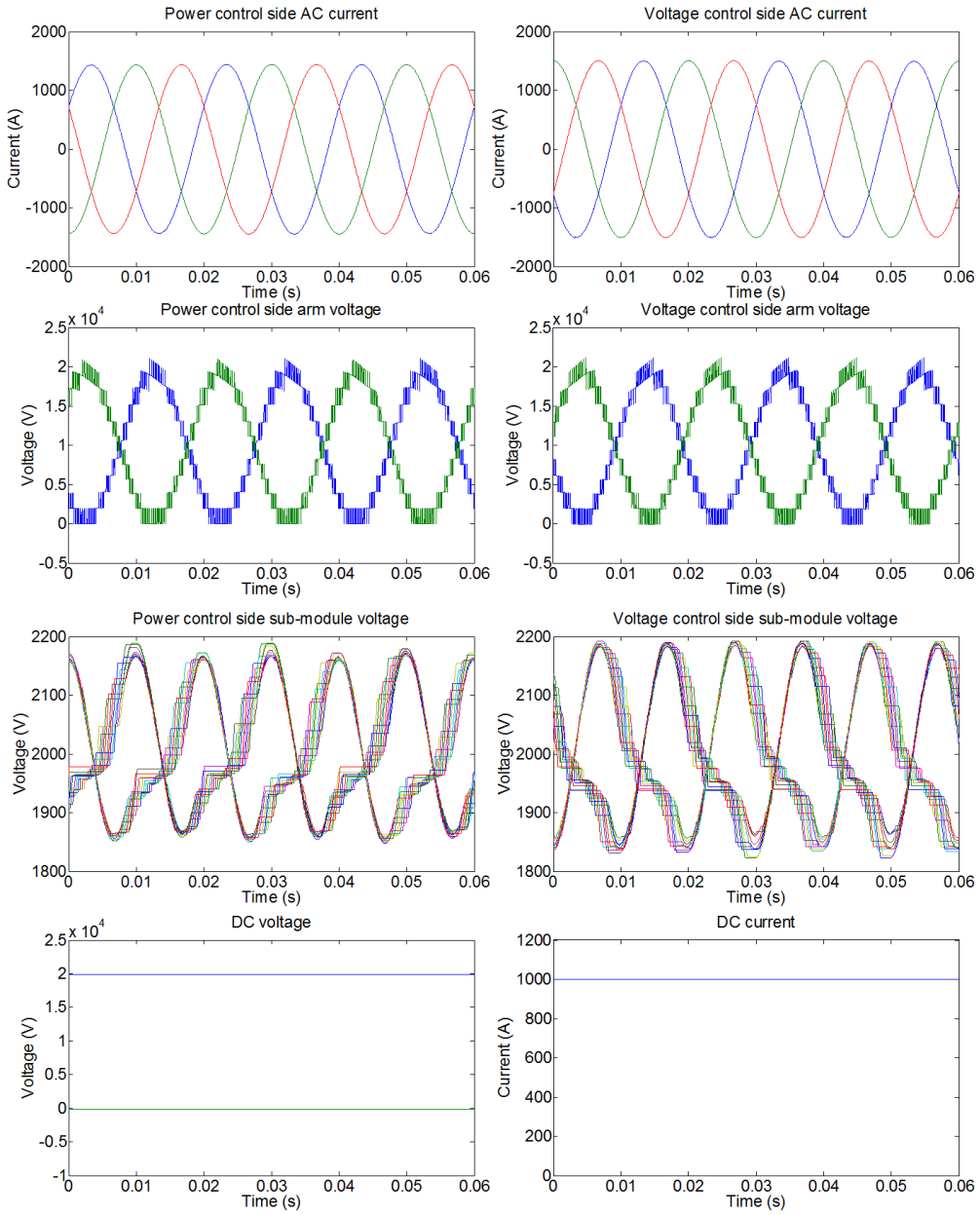


Figure 6.5: Simulation results of post fault operation mode 1

module capacitor voltage ripple are slightly larger than the rest sub-modules. The reason is that in the simulation, the rotation method decided that the sub-modules only switch when there the total inserted sub-module numbers

changed in order to reduce the switching loss. As can be seen in the voltage control side arm voltage plot in this figure, there is a time range where the arm voltage is the same. As a result, no sub-module need to be switched so that there are two inserted sub-modules continue to be charged.

The advantage of operation mode 2 over operation 1 is the reduction in plant rating however this is at the expense of allowable power transmission. Operation modes 3-5 allow a further reduction in the insulation voltage rating of the transformer, but at the penalty of higher transmission losses during DC fault ride through.

Figure 6.7 shows the simulation results of post fault operation mode 3 where $P_e = 1$. As was the case with operating mode 2, the ac current and dc voltage are half rated value. In this mode of operation the upper and lower arm voltage are no longer symmetric. The voltage range for the upper arm is approximately $[0, V_{dc}]$; and the lower arm is $[-\frac{1}{2}V_{dc}, \frac{1}{2}V_{dc}]$. As the power pulsation in the arms is no longer symmetric (180 phase shifted), the sub-module capacitor voltage in the upper and lower arm is also no longer symmetric.

The main advantage of post fault operation mode 3 is that the ac side transformer dc voltage stress is 0, however at the expense of increased semiconductor loss compared to operating mode 2, as shown in chapter 3 section 3.3.5.

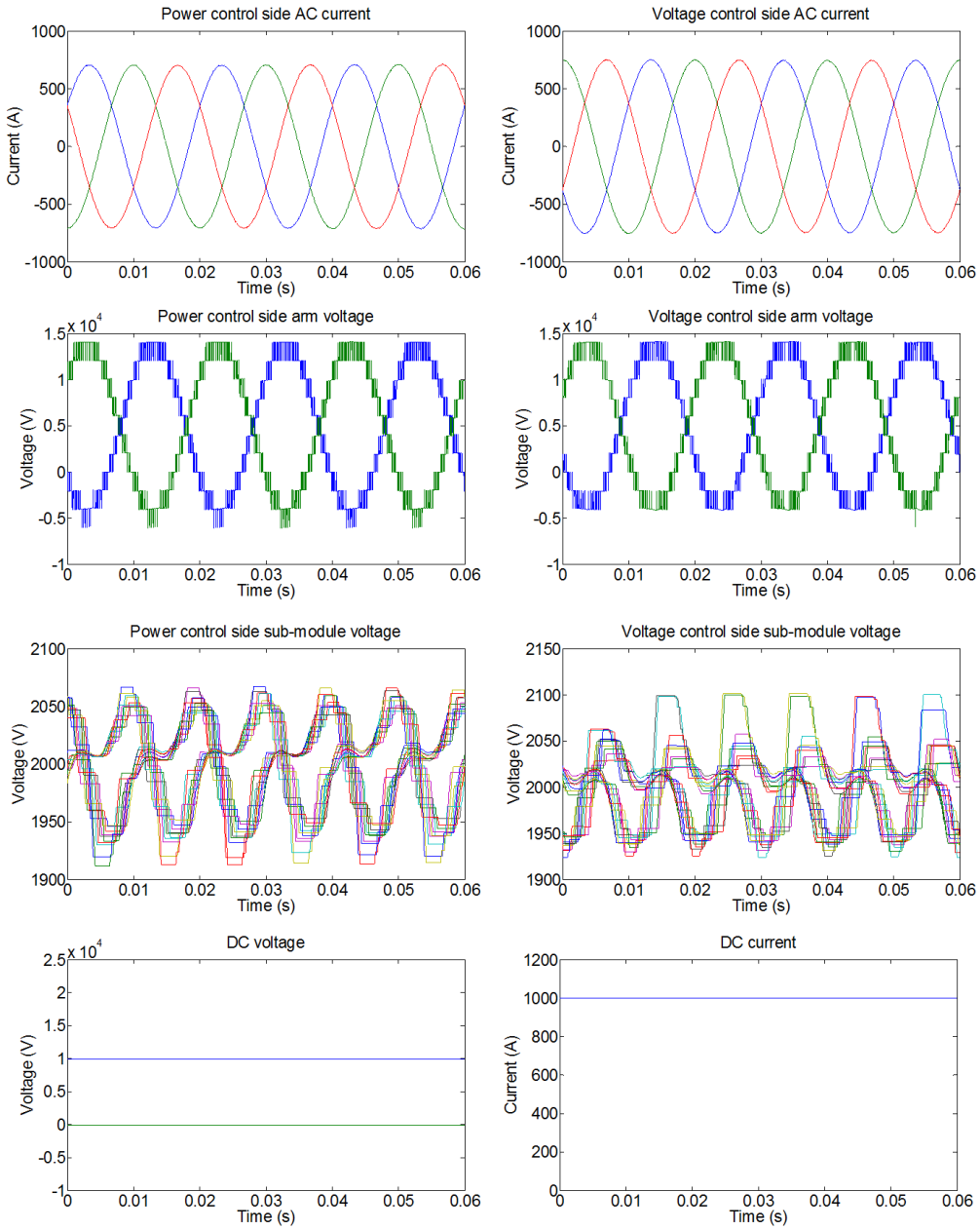


Figure 6.6: Simulation results of post fault operation mode 2

The simulation results of post fault operation mode 4 and 5 are shown in figure 6.8 and figure 6.9, $P_e = 0.75$ and $P_e = 0.25$ respectively. When $P_e = 0.75$, the upper arm voltage range is approximately $[-\frac{1}{8}V_{dc}, \frac{7}{8}V_{dc}]$; the

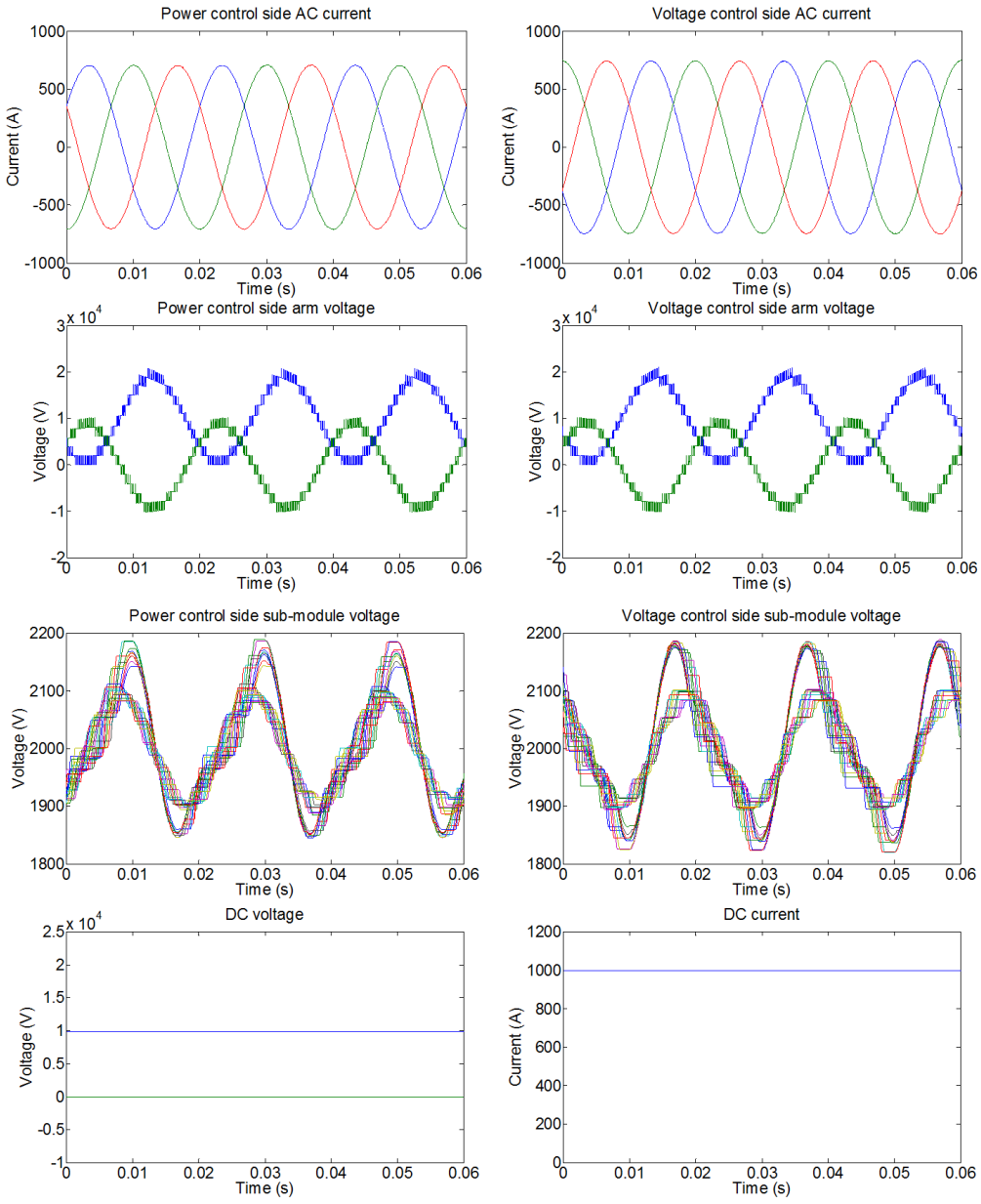


Figure 6.7: Simulation results of post fault operation mode 3

lower arm voltage range is approximately $[-\frac{3}{8}V_{dc}, \frac{5}{8}V_{dc}]$. The ac transformer dc voltage stress is $\frac{1}{8}V_{dc}$. The sub-module capacitor voltage from upper and lower arm are not symmetric, but have the same DC component.

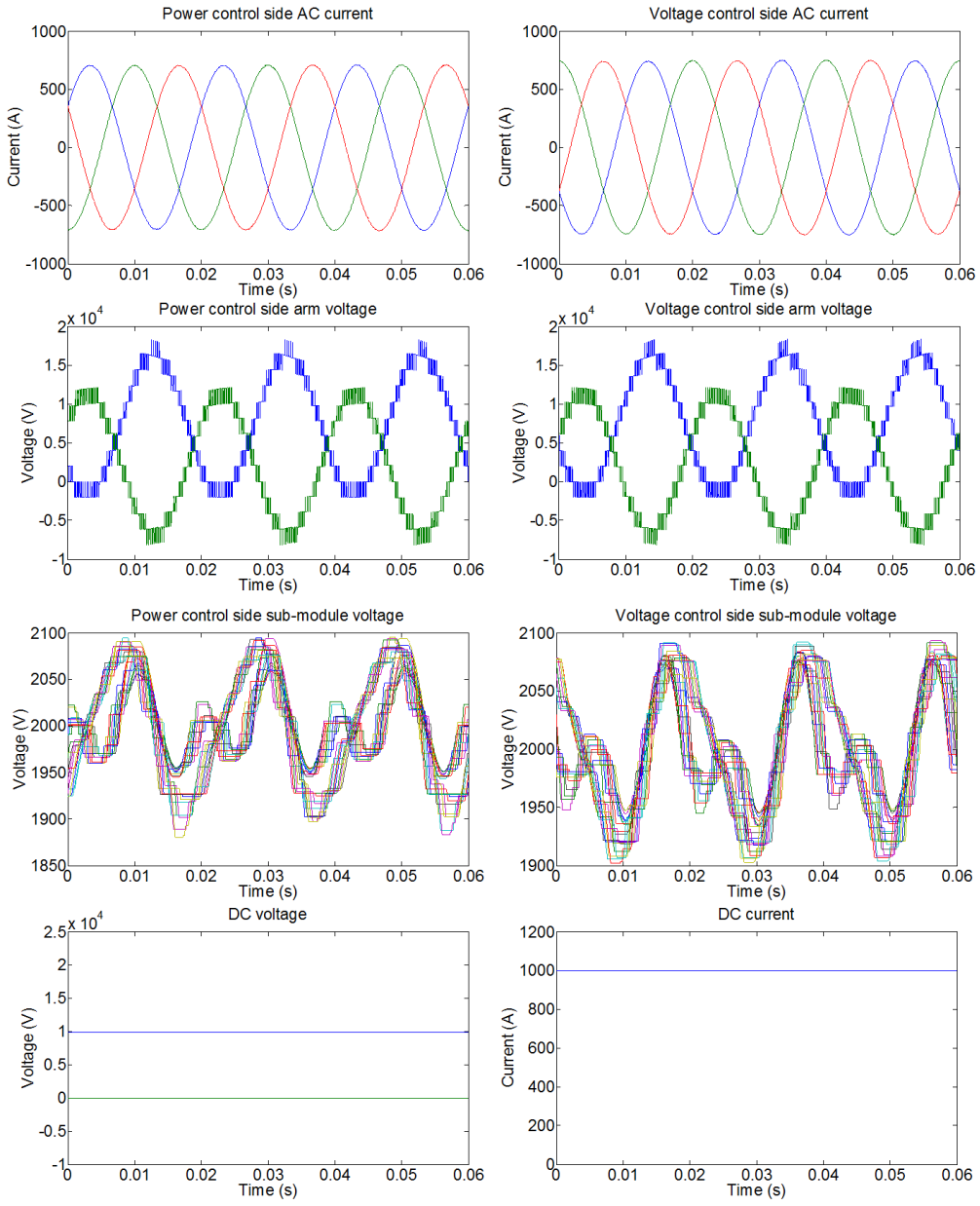


Figure 6.8: Simulation results of post fault operation mode 4

The arm voltage ranges when $P_e = 0.25$ are $[-\frac{3}{8}V_{dc}, \frac{5}{8}V_{dc}]$ for upper arm and $[-\frac{1}{8}V_{dc}, \frac{7}{8}V_{dc}]$ for lower arm. The ac transformer dc voltage stress is

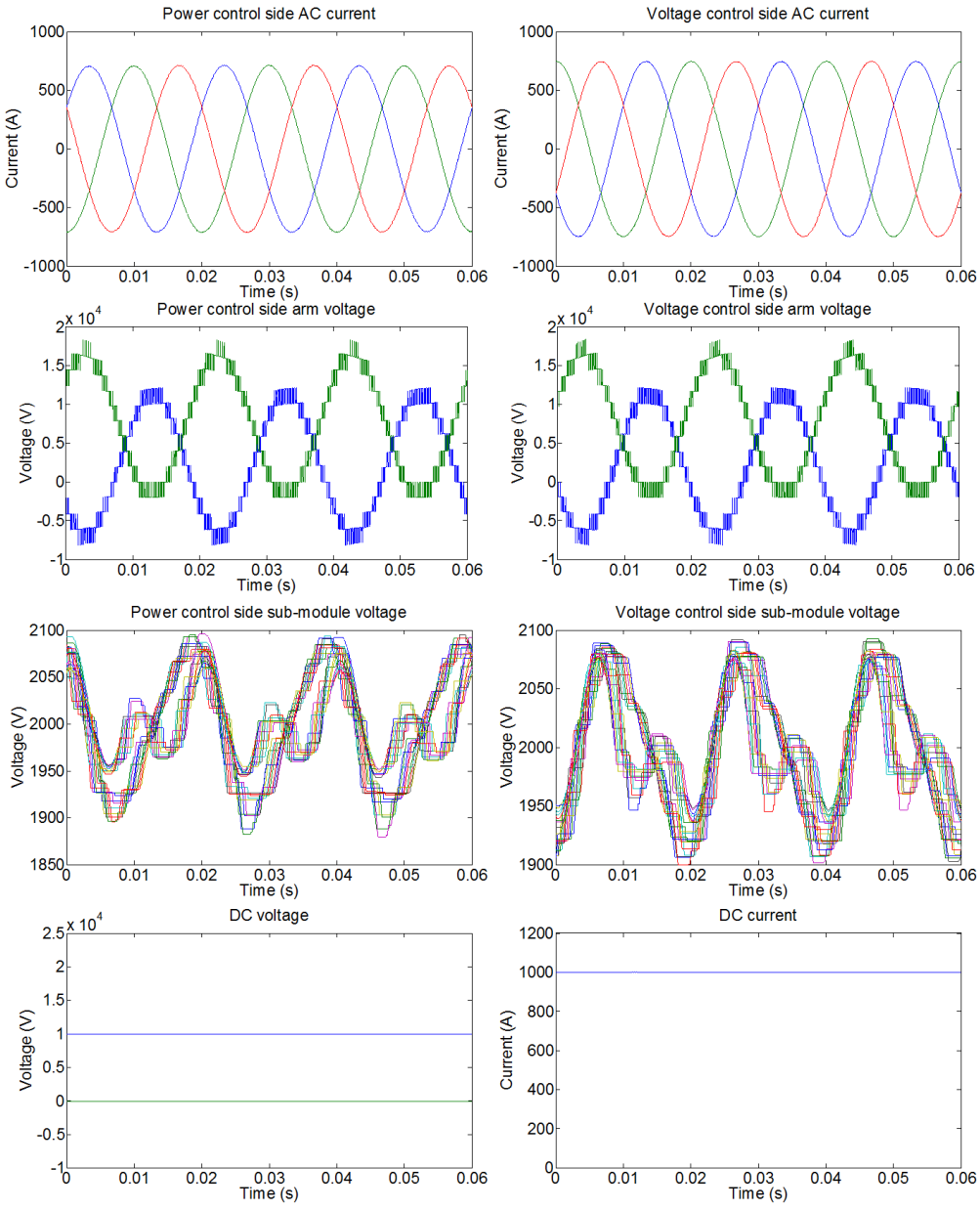


Figure 6.9: Simulation results of post fault operation mode 5

$\frac{3}{8}V_{dc}$. Figure 6.8 and figure 6.9 illustrate that the control scheme is working for any $P_e \in [0, 1]$. Larger magnitude leads to smaller dc voltage stress on ac transformer.

6.5 Full-bridge MMC steady state operation for line-to-line fault

Figure 6.10 shows simulation results for point-to-point HVDC system operating with a line to line fault. In this scenario, the active power demand is set to zero and the reactive power demand for both sides are set to $Q = 10MVAr$, also assuming $R_u = 0.5$.

As can be seen, with the sub-module capacitor voltages controlled to their nominal values, reactive power is exchanged with the AC grid. There is no dc voltage stress on ac side transformer. The voltage range of the upper and lower arms are both $[-V_{dc}, V_{dc}]$.

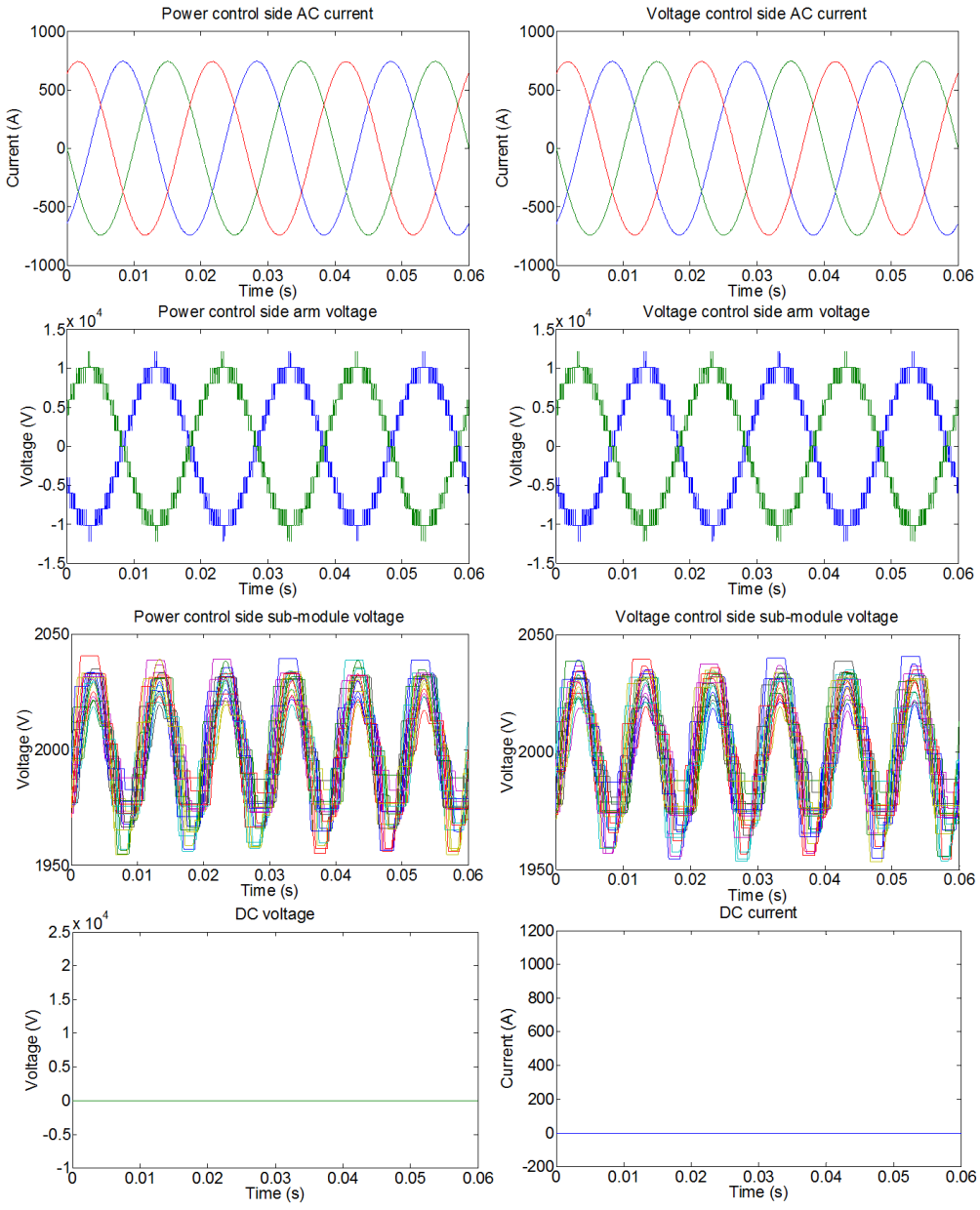


Figure 6.10: Simulation results of line-to-line post fault operation

6.6 Comparison between analysis sub-module capacitor results and simulation results

In chapter 3, the sub-module capacitor voltage has been estimated. The analysed results is compared with the simulation results in figure 6.11 and

figure 6.12.

Figure 6.11 shows the sub-module capacitor voltage when $P_e = 0.5$, the upper plot is the analysis result, the middle plot and lower plot are the simulation result of power control terminal and voltage control terminal. As can be seen, the lowest voltage ripple value and largest value in analysis result versus the capacitor average voltage are approximate $\frac{0.097}{0.1}$ and $\frac{0.103}{0.1}$. Also, the upper and lower arm sub-module capacitor voltage are symmetric so that the largest and lowest value are the same. When the average capacitor voltage is $2000V$, the voltage ripple is between $1940V$ to 2060. These magnitudes match the simulation results.

In the upper plot of figure 6.11, the sub-module capacitor voltage waveforms are continuous and smooth. The reason is that in the analysis the rotation speed is assumed to be infinite, which means all the sub-module capacitor voltage in one arm are the same. But in simulation, the rotation algorithm is different to the analysis. There is only one sub-module is switched whenever the required inserted sub-module numbers changed. As a result, each sub-module capacitor voltage depends on the modulation signal and arm current and will be different from each other. As shown in the middle and lower plot, the simulation results of sub-module capacitor voltage have flat tops and not continuous.

Similarly, figure 6.12 shows the sub-module capacitor voltage when $P_e = 1$. For upper arm, the lowest voltage ripple value and largest value in analysis

result versus the capacitor average voltage are approximate $\frac{0.092}{0.1}$ and $\frac{0.108}{0.1}$. When the average capacitor voltage is $2000V$, the voltage ripple is between $1840V$ to 2160. For lower arm, the lowest voltage ripple value and largest value in analysis result versus the capacitor average voltage are approximate $\frac{0.095}{0.1}$ and $\frac{0.105}{0.1}$. When the average capacitor voltage is $2000V$, the voltage ripple is between $1900V$ to 2100. These magnitudes also match the simulation results.

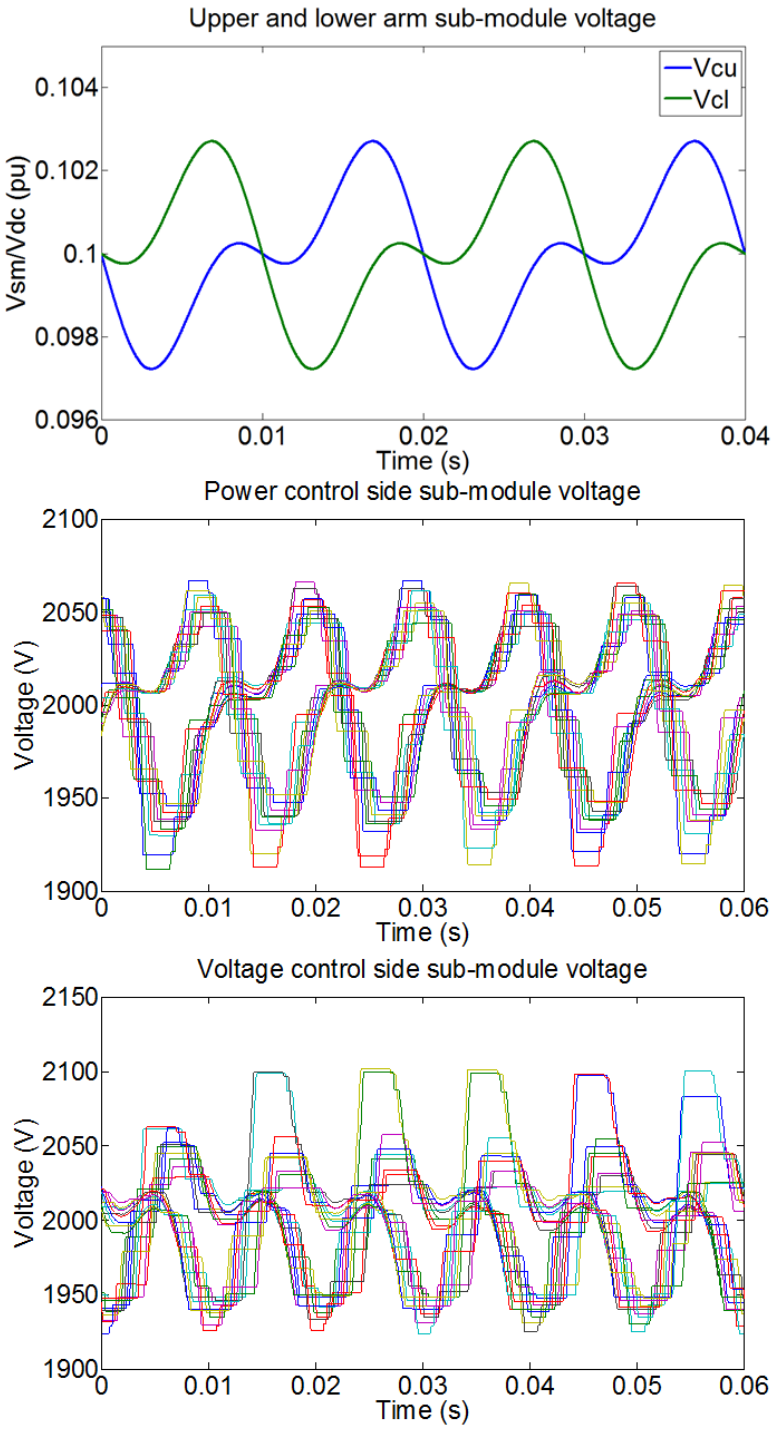


Figure 6.11: Comparison of sub-module capacitor voltage when $P_e = 0.5$

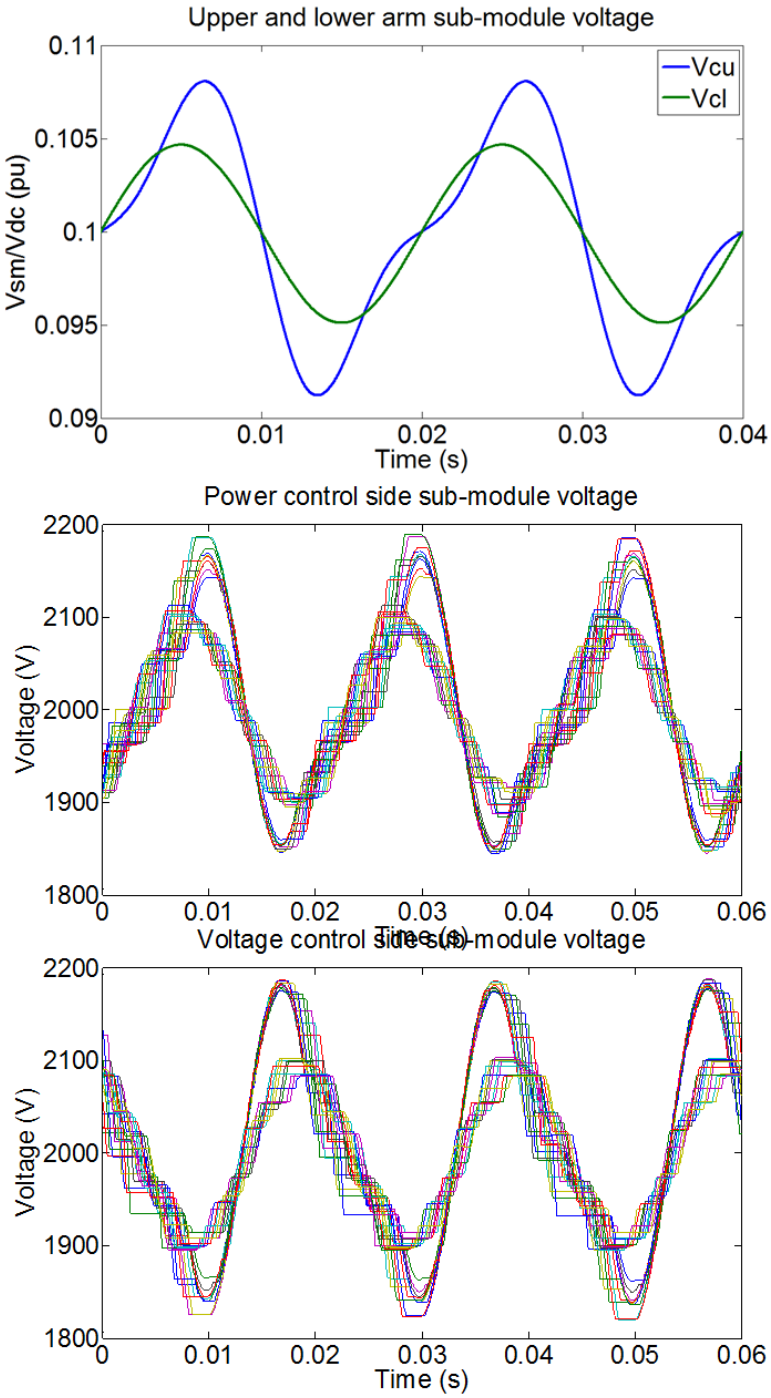


Figure 6.12: Comparison of sub-module capacitor voltage when $P_e = 1$

6.7 Summary

This chapter has presented simulation results for normal and faulted operation of point-to-point HVDC scheme defined in the Cigre bench mark model [140] and the simulation results for a four-terminal DC grids.

The simulation results of the point-to-point full-bridge MMC system proved voltage balancing control, current control and dc voltage control operate satisfactorily. The post line-to-ground fault operation modes listed in chapter 3 are applied to the point-to-point system. The factor P_e, defined in chapter 3, can be chosen flexibly between $[0, 1]$, when $P_e = 0.5$ the conduction loss is minimum and when $P_e = 1$ there is no dc voltage stress on transformer. Under all these post-fault operation mode, the system is able to transfer half of the rated power.

Applying the post line-to-line fault operation to a point-to-point full-bridge MMC system, it is shown that the system can provide reactive power to both AC networks and keep the converter station operational by ensuring the sub-module capacitor voltages remain at their nominal level.

Chapter 7

Conclusion and Further Work

Modular multilevel converters (MMC) provide the ability to create high voltage waveforms by increasing the number of sub-modules. The large number of sub-modules leads to a high quality waveform despite the low switching frequency. Each arm of a full-bridge modular multilevel converter consists of many full-bridge sub-module which are made up of a full-bridge with a capacitor. In a point-to-point HVDC system or a DC grid, a DC side fault can result in a whole system outage. Since a DC side fault is usually permanent and the full-bridge MMC has the DC fault ride through capability, it is able to continue transmitting power with one cable connected to ground.

This thesis has presented several post fault operation methods using a full-bridge MMC to keep the DC system operational after a DC side fault. In the case of a pole-to-ground fault when the cable can afford two times rated voltage and the AC side transformer can with stand half V_{dc}, the MMC can operate as in normal conditions and continues to transfer rated power; this is

achieved by allowing the system to float up with the grounding of the system. However, in the case that the cable cannot support this additional voltage, the full-bridge MMC can maintain the DC voltage at half the normal operating voltage and continue to transfer half rated power. The proposed post fault operating modes require different allowable voltage stress and voltage range requirements. For a line-to-line fault, the full-bridge MMC is able to continue connected to the AC grid and provide reactive power, while the arm voltage range requirement is $[-\frac{1}{2}V_{dc}, \frac{1}{2}V_{dc}]$.

To minimise the transformer DC voltage stress and reduce the insulation requirement operating mode 3 is best. In this mode only one arm produces a DC voltage and as a consequence non of the real components of the AC current flows in that arm. From the power loss point of view, when the current in the upper arm and lower arm are symmetric which is referred to as post fault operation mode 2, the conduction power loss is minimum. This is because the semiconductor conduction loss associated with the resistive component is minimised by sharing the load equally between the two limbs. Another advantage of this operation mode is that the negative arm voltage range requirement is also lowest. The arm voltage needs to be able to provide $-\frac{1}{4}V_{dc}$ in mode 2 while in mode 1 needs to be able to provide $-\frac{1}{2}V_{dc}$. This would be of particular importance for future work investigating the reduction of semi-conductor loss using partial population of full bridge and half bridge sub-modules, which has not been analysed in this thesis.

In order to ensure that sub-module capacitor voltages remain converged

within an arm while still producing the target voltage, a rotation scheme with level shifted PWM is used. The modulation wave is compared with carrier waves so that the number of sub-modules to be switched in can be determined. The sub-module rotation scheme discharges the capacitor with highest voltage and charges the capacitor with lowest voltage, ensuring that the capacitor voltages remain converged.

The target modulation wave is determined by the control system. The full-bridge MMC control system in this work contains AC current control, arm current control, sub-module capacitor voltage control. In the case of arm current control, proportional resonant control is used to eliminate second order harmonic circulating current. Second order harmonic circulating current is caused by the twice fundamental period power pulsation which unless properly compensated for in the modulating wave causes the insertion of a second order arm voltage into the limbs. It exist in both normal operation and post fault operation condition. The upper and lower arm PR controllers are separated in some modes of operation, as the power pulsation in each arm is not symmetrical and without appropriate control an even harmonic could be applied to the network. The energy control is used to maintain the sub-module capacitor voltage. In normal operation, the upper and lower arm the sub-module capacitor average voltage is naturally balanced as Vdc/N. However, in some post fault operation modes, the sub-module capacitor average voltage of upper and lower arms are not the same as in normal operation and have been controlled using a closed loop energy control. The energy control consists of total energy control and difference energy control.Total energy

control ensures the energy summation of upper and lower arm are the same as the reference value. Difference energy control ensure the energy difference between upper and lower arm is zero. As a result, the sub-module capacitor average voltage of both upper and lower arm are controlled.

The post fault operation is investigated by simulating a point-to-point DC system. Under all post fault operation modes. It has been verified that the full-bridge MMC simulation results are as predicated through the analysis of chapter 3. The implemented control systems have also been verified with the second harmonic circulating current eliminated and the sub-module capacitor arm voltage maintained to $\frac{V_{dc}}{N}$.

7.1 Summary of achievements

The following points summarise the achievements presented in this thesis.

- A literature review of HVDC grids topologies, the DC grid power flow control methods and modular multilevel converter has been conducted.
- A review of modular multilevel converter normal operation analysis has also been made in detail.
- A novel post fault operation method which applied to the full-bridge modular multilevel converter has been presented and analysed. The advantages and disadvantages of different post fault operation modes has been presented.

- The new management algorithm for the full-bridge MMC such that it can continue to transmission power with one cable grounded after a dc side line-to-ground fault. The operation can be extended to minimize voltage stress on the ac side transformer. The MMC has to operate asymmetrically to remove voltage stress on transformer, thus the second harmonic circulating current and the sub-module capacitor voltage need to be controlled.

- The new management scheme can eliminate second harmonic arm current for post fault operation.

- The new management scheme can control the total energy of one phase and can control the energy difference in the upper and lower arms, to balance sub-modules energy of the upper and lower arms for asymmetric post fault operation.

- A power loss calculation method for full-bridge modular multilevel converter in the post fault operation has been presented.

- A control scheme for eliminating second order harmonic circulating current and controlling sub-module capacitor voltage has been developed and applied for full-bridge modular multilevel converter. The method presented is particularly important for preventing even harmonic voltage injection onto the AC grid when using some of the faulted modes operation presented.

- A point-to-point DC system was simulated in Matlab/Simulink to investigate the presented post fault operation scheme.

7.2 Future work

This work has identified the negative available voltage requirement for the modes of operation presented; future work could use the voltage requirement to define the minimum number of full-bridge sub-modules need so that the converter could be populated with half-bridge and full-bridges sub-modules. Future work would analyse, the benefit in terms of reduction of conduction losses, while also analysing the balancing method needed. It is anticipated that mixed sub-module types will present problems in capacitor balancing which will need to be addressed; these include ensuring that when AC/DC power transfer is non zero over the period of negative/positive voltage insertion a method of transferring sufficient energy from the half-bridge to the full-bridge is provided. Additionally to prevent excess voltage ripple on the sub-modules the capacitance of the full-bridge sub-module could be made larger to the half-bridge sub-module.

The transient response of pole-to-ground and pole-to-pole fault could be explored. As could the effect of fault location and fault detection time on the transient response could be made.

The construction of a full-bridge modular multilevel converter to allow validation of the post fault operation modes in practical a rig should also be undertaken.

In a multi-terminal DC system, the transient response and the interaction

between the converters will be complicated. If a meshed grid is used a line-to-ground fault would connect all the cables to the grounded point. In this case, reducing the DC side voltage by a half to continue to transfer power may be inappropriate. Alternative grounding methods under this situation should be investigated.

Appendix A

Appendix

A.1 Power Loss Calculation

A.1.1 Conduction loss In Normal Operation for All Full-Bridge Sub-module

In normal operation, the conducted components in sub-module is depended on output voltage and the valve current. The figure A.1 shows the conduction path of Full-Bridge sub-module in normal operation.The table A.1 shows the conducted components in the sub-module.

Output Voltage	$+V_C$	0
Sub-module Utilization factor	$P_C(t)$	$1 - P_C(t)$
$I_{valve} > 0$	$D1, D4$	$T3, D4$
$I_{valve} > 0$	$T1, T4$	$D3, T4$

Table A.1: Conducted components of Full-Bridge sub-module in Normal Operation

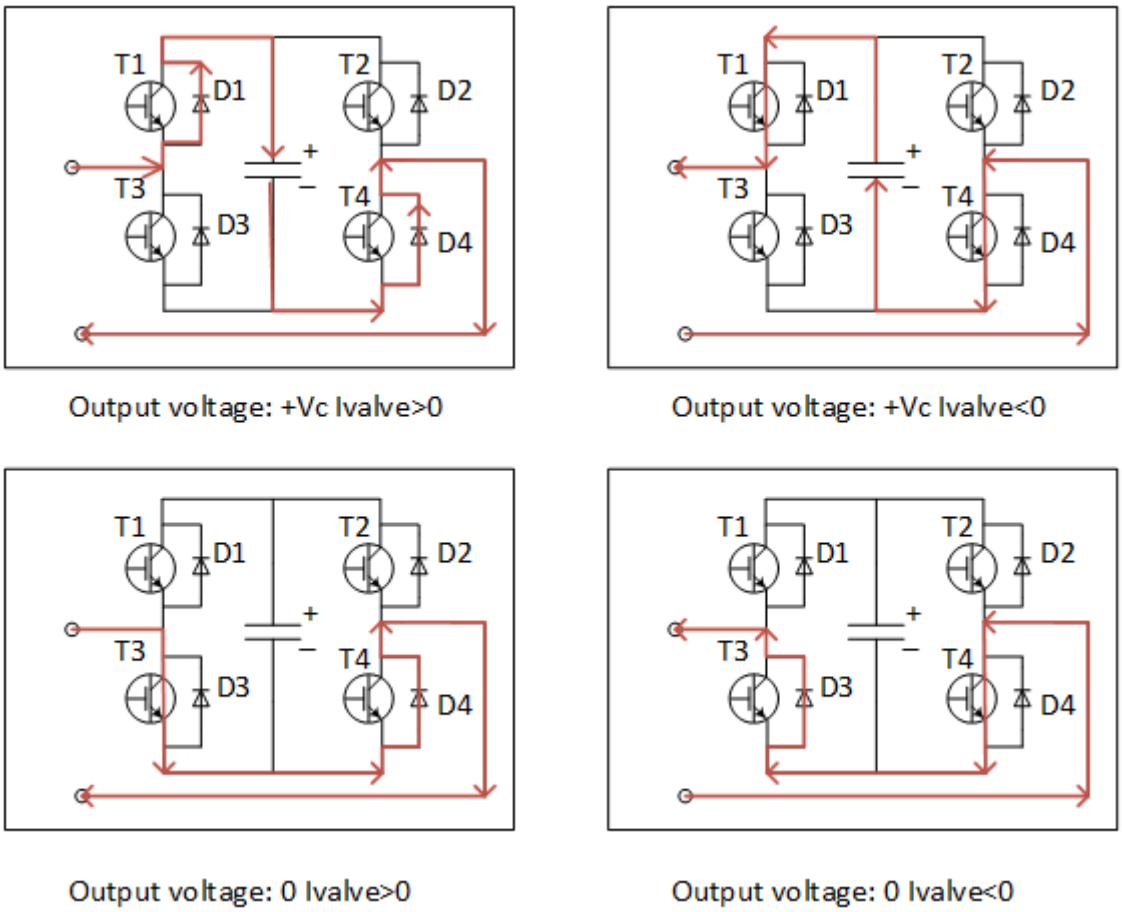


Figure A.1: Conduction Path of Full-Bridge sub-module in Normal Operation

$$P_C(t) = \frac{V_{arm}(t)}{V_C(t)} \tag{A.1}$$

where $V_{arm}(t)$ is the output voltage of the valve, and $V_C(t)$ is the average voltage of sub-module capacitors in the valve.

Assume that $I_p = I_{valve}$ when $I_{valve} > 0$, and $I_n = I_{valve}$ when $I_{valve} < 0$. Based on the table A.1, the conduction loss of each component is able to be

calculated.

$$
\begin{aligned}
P_{conT1} &= I_n \times P_C(t) \times V_{CE} \\
P_{conD1} &= I_p \times P_C(t) \times V_F \\
P_{conT2} &= 0 \\
P_{conD2} &= 0 \\
P_{conT3} &= I_p \times (1 - P_C(t)) \times V_{CE} \\
P_{conD3} &= I_n \times (1 - P_C(t)) \times V_F \\
P_{conT4} &= I_n \times V_{CE} \\
P_{conD4} &= I_p \times V_F
\end{aligned}
\tag{A.2}
$$

A.1.2 Switching loss In Normal Operation for All Full-Bridge Sub-module

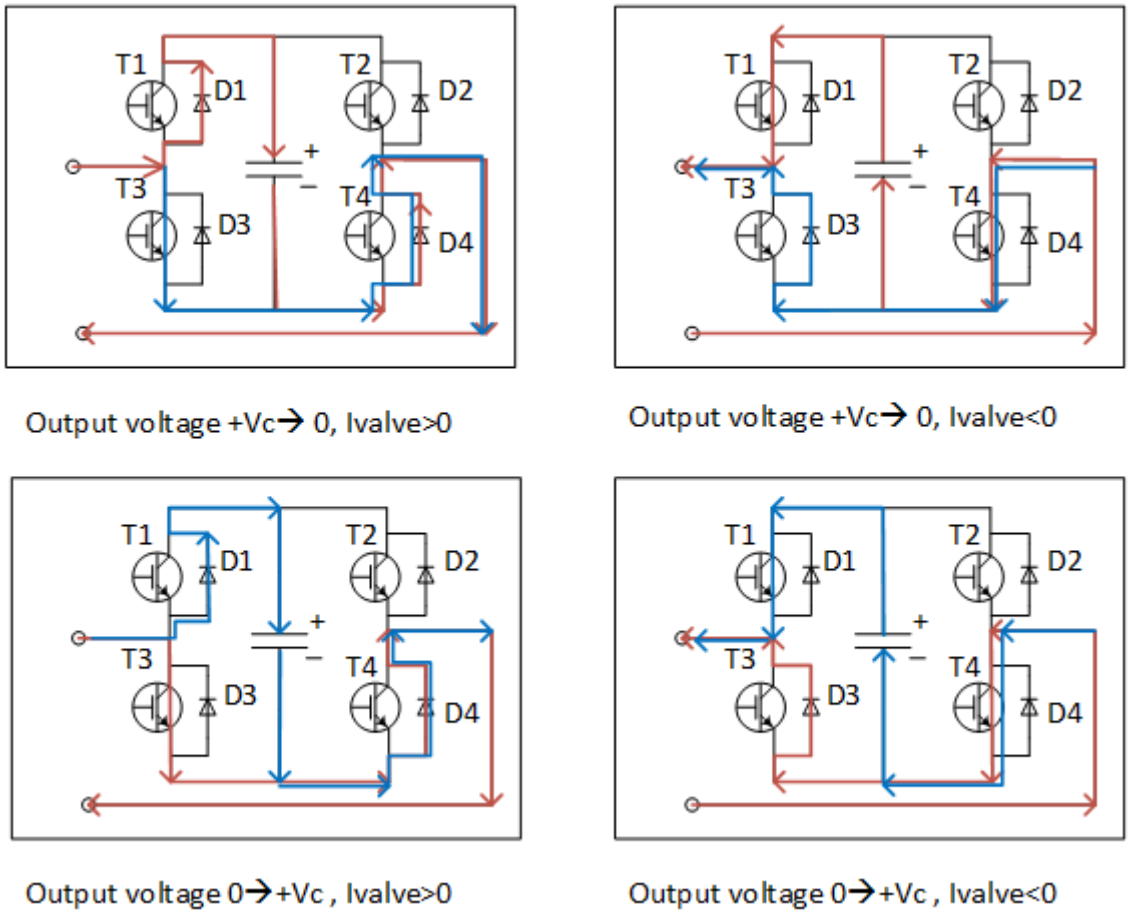


Figure A.2: Switching Path of Full-Bridge sub-module in Normal Operation (red to blue)

$[T1 \quad T2]$	$[1 \quad 0] \rightarrow [0 \quad 0]$	$[0 \quad 0] \rightarrow [1 \quad 0]$
$I_{valve} > 0$	$1\ E_{on}(T3), \quad 1\ E_{rec}(D1)$	$1\ E_{off}(T3)$
$I_{valve} > 0$	$1\ E_{off}(T1)$	$1\ E_{on}(T1), \quad 1\ E_{rec}(D3)$

Table A.2: Switching components of Full-Bridge sub-module in Normal Operation

For the script calculation, the rotation method is that compare the modulation wave and the carrier wave, when the modulation wave cross the carrier wave, there is one submodule need to switch on or off. When modulation wave is increasing, switch one on, otherwise, switch one off. Then based on Ivalve sign, choose the sub-module with highest voltage or the lowest.

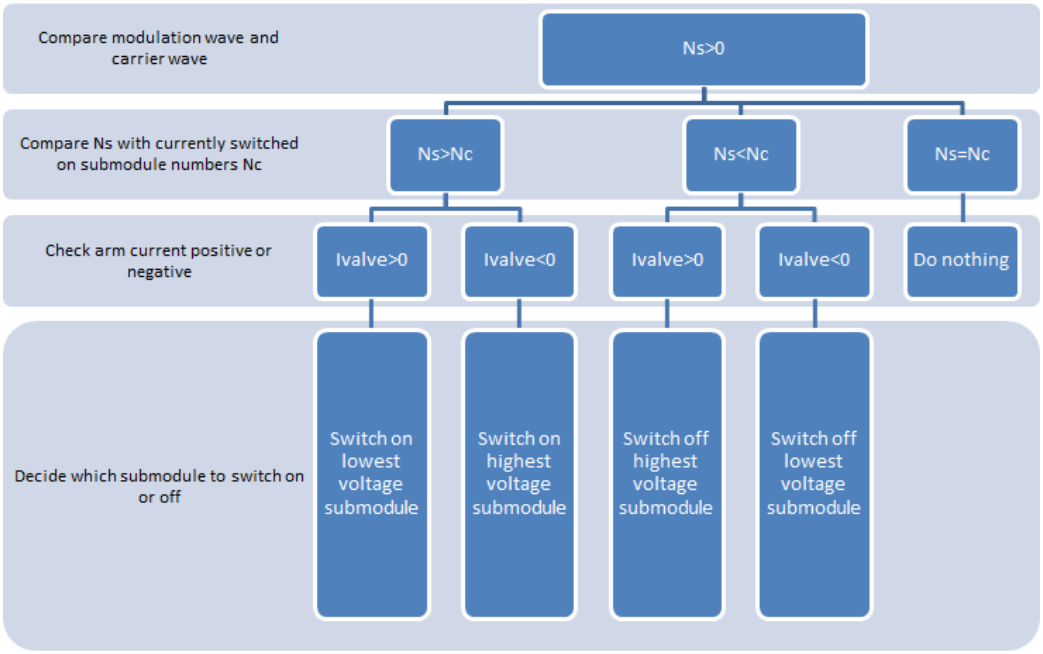


Figure A.3: The flow chart of rotation method

Based on the rotation method, the switching loss calculation is assumed all the submodules have the same voltage. The calculation algorithm is:

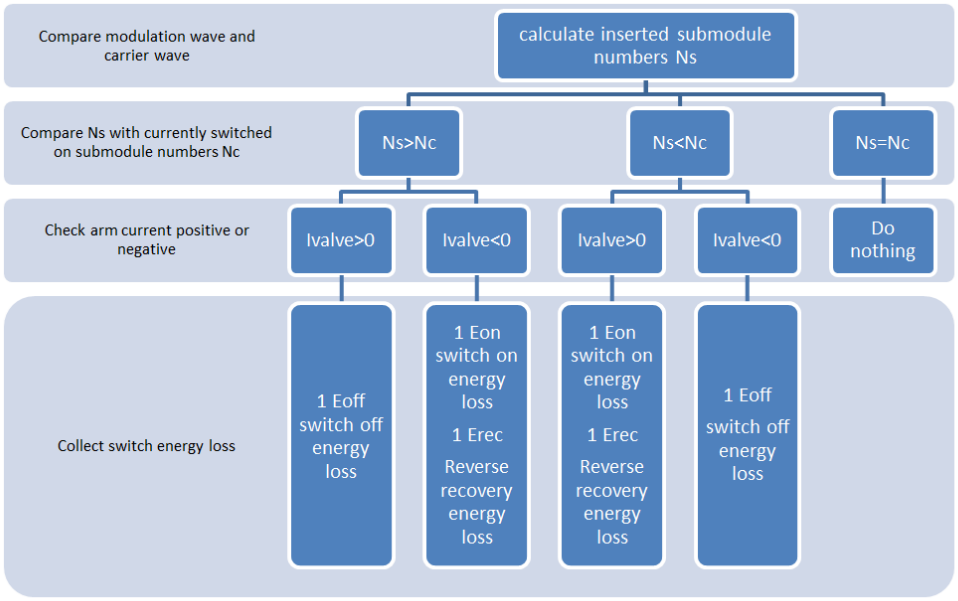


Figure A.4: The flow chart of switching loss calculation

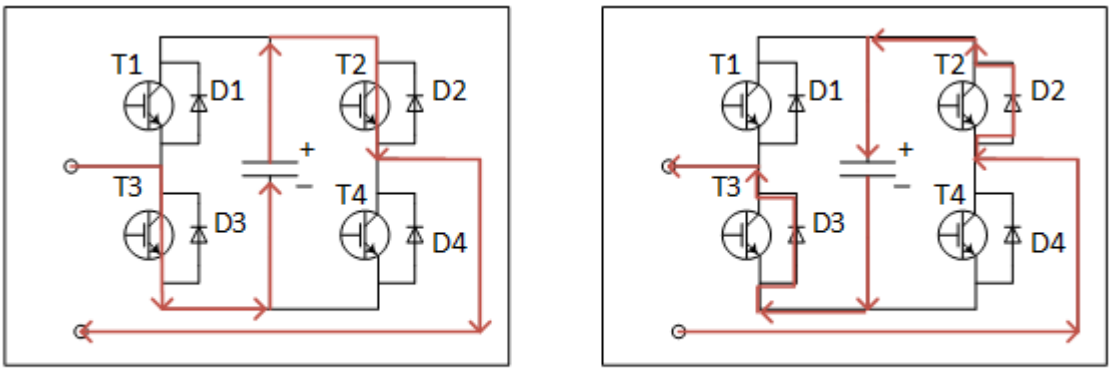


Figure A.5: Conduction Path for -Vc output voltage of Full-Bridge Sub-module in Fault Operation

Conduction Loss

Output Voltage	$+Vc$	0	$-Vc$
Sub-module Utilization Factor	$P_{cposi}(t)$	$P_{czero}(t)$	$P_{cnega}(t)$
$I_{valve} > 0$	$D1, D4$	$T3, D4$	$T3, T2$
$I_{valve} > 0$	$T1, T4$	$D3, T4$	$D2, D3$

Table A.3: Conducted components of Full-Bridge sub-module in Fault Operation

$$P_{cposi}(t) = \begin{cases} \frac{V_{arm}(t)}{V_c(t)} \ (when \ \frac{V_{arm}(t)}{V_c(t)} > 0) \\ 0 \qquad\qquad (when \ \frac{V_{arm}(t)}{V_c(t)} \leq 0) \end{cases}$$

$$P_{cnega}(t) = \begin{cases} 0 \qquad\qquad (when \ \frac{V_{arm}(t)}{V_c(t)} \geq 0) \\ \frac{V_{arm}(t)}{V_c(t)} \qquad (when \ \frac{V_{arm}(t)}{V_c(t)} < 0) \end{cases}$$

$$P_{czero}(t) = 1 - P_{cposi}(t) - P_{cnega}(t)$$

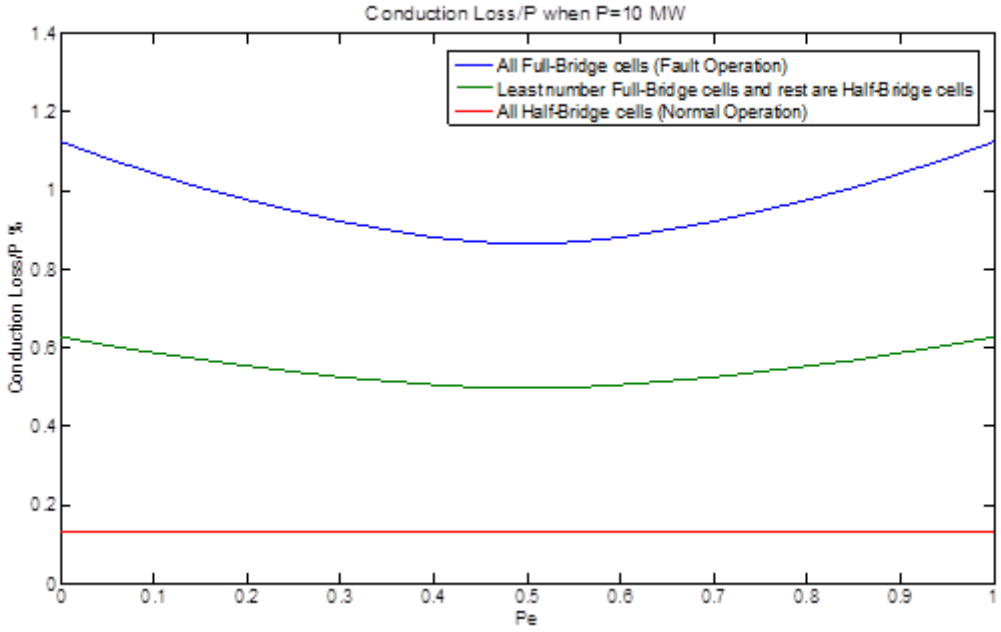


Figure A.6: Conduction Loss VS Pe when P=10MW,Q=0

$$
\begin{aligned}
P_{conT1} &= I_n \times P_{cposi}(t) \times V_{CE} \\
P_{conD1} &= I_p \times P_{cposi}(t) \times V_F \\
P_{conT2} &= I_p \times P_{cnega}(t) \times V_{CE} \\
P_{conD2} &= I_n \times P_{cnega}(t) \times V_F \\
P_{conT3} &= I_p \times P_{czero}(t) \times V_{CE} + I_p \times P_{cnega}(t) \times V_{CE} \\
P_{conD3} &= I_n \times P_{czero}(t) \times V_F + I_n \times P_{cnega}(t) \times V_F \\
P_{conT4} &= I_n \times P_{czero}(t) \times V_{CE} + I_n \times P_{cposi}(t) \times V_{CE} \\
P_{conD4} &= I_p \times P_{czero}(t) \times V_F + I_p \times P_{cposi}(t) \times V_F
\end{aligned}
\tag{A.3}
$$

A.1.3 Conduction Loss for different Pe (P=10MW)

The figure A.6 show that the conduction loss with different P_e values. The blue line is the conduction $loss/P$ when all the cells are Full-Bridge. The red line is when all the cells are Half-bridge, but this result is not depend on P_e, the line is there to show the conduction loss in normal operation . The green line is when there are least number Full-Bridge cells.

The least Full-Bridge number N_{FB} is depend on P_e.

$$N_{FB} = \begin{cases} 0.5 * Pe & Pe \geq 0.5 \\ 0.5 * (1 - Pe) & Pe < 0.5 \end{cases}$$

For example, when Pe=0.5, assume that $V_{ac} \cong \frac{1}{2}V_{dc}$. Then the upper arm voltage $V_u \in [-\frac{1}{4}V_{dc}, \frac{3}{4}V_{dc}]$, the lower arm voltage $V_l \in [-\frac{1}{4}V_{dc}, \frac{3}{4}V_{dc}]$.

So that of both upper arm and lower arm need to be Full-Bridge. When $P_e = 1$, The upper arm voltage $V_u \in [0, V_{dc}]$, The lower arm voltage $V_l \in [-\frac{1}{2}V_{dc}, \frac{1}{2}V_{dc}]$. Then half of the lower arm cells need to be full-Bridge, but since the faulted line could be the positive or negative, half of the upper arm cells need also be full-bridge to operate in this mode.

A.1.4 Switching Loss calculation for different Pe (P=10MW)

The switching path of full-bridge sub-module and the corresponding components are shown in figure A.7 and table A.4.

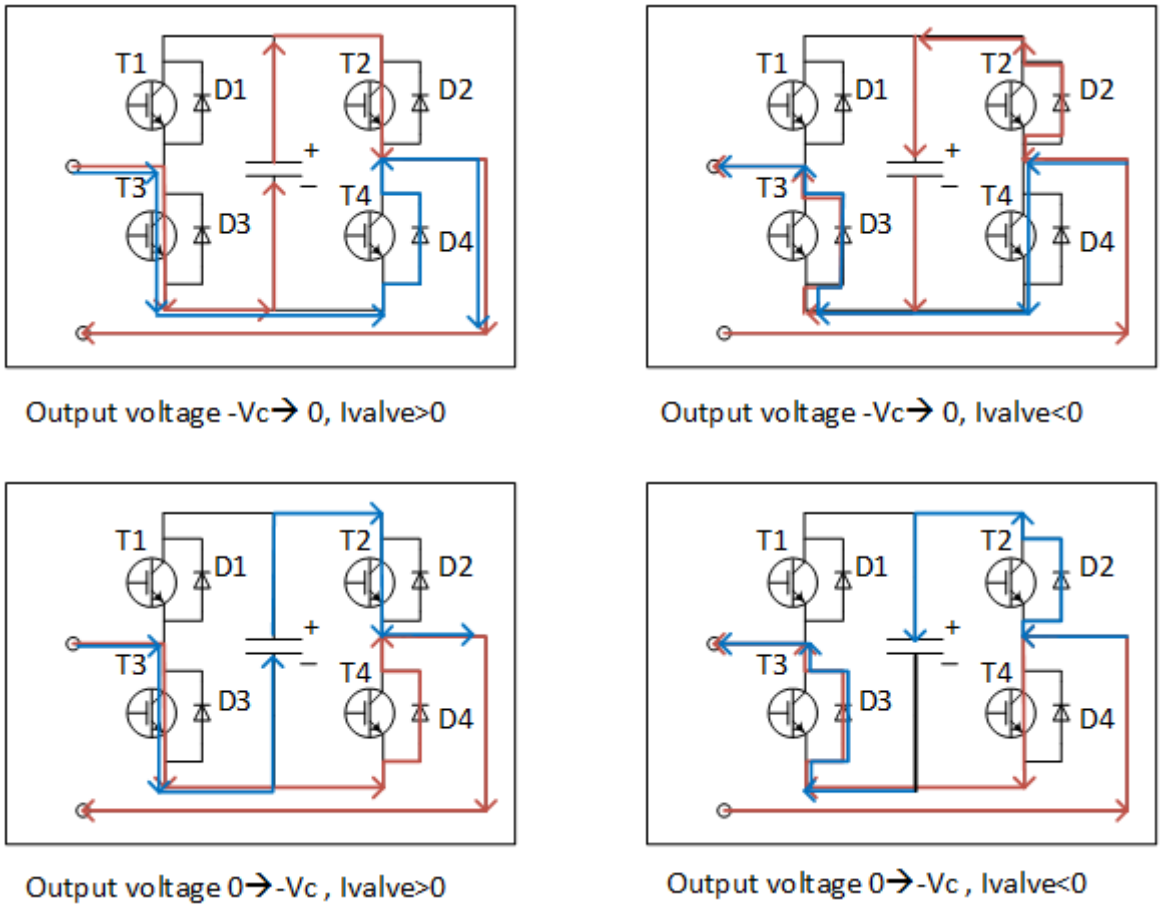


Figure A.7: Switching path of Full-Bridge sub-module in Fault Operation

In theory, the sub-module could change state direct between $+Vc$ to Vc. But in operation, there is no need to since it cause more switching components. So the state change between $+Vc$ and Vc is not included in the table A.4.

Output Voltage	$+Vc \rightarrow 0$	$0 \rightarrow +Vc$	$0 \rightarrow -Vc$	$-Vc \rightarrow 0$
$I_{valve} > 0$	1 $E_{on}(T3)$, 1 $E_{rec}(D1)$	1 $E_{off}(T3)$	1 $E_{on}(T2)$, 1 $E_{rec}(D4)$	1 $E_{off}(T2)$
$I_{valve} > 0$	1 $E_{off}(T1)$	1 $E_{on}(T1)$, 1 $E_{rec}(D3)$	1 $E_{off}(T4)$	1 $E_{on}(T4)$, 1 $E_{rec}(D2)$

Table A.4: Switching components of Full-Bridge sub-module

A.1.5 Conduction Loss for different Carrier frequency

The figure A.8 shows that when P=10MW, Q=0, despite the oscillation spikes, switching loss is lowest when Pe=0.5 as conduction loss.

Figure A.9 shows that switching loss increase with the carrier frequency, approximately linear.

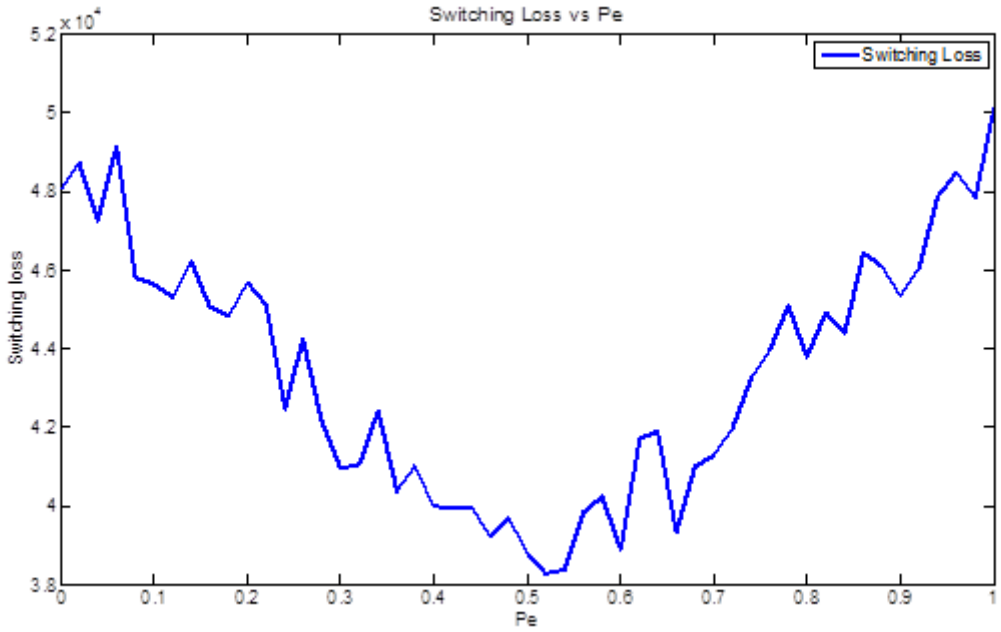


Figure A.8: Switching Loss VS Pe when P=10MW,Q=0

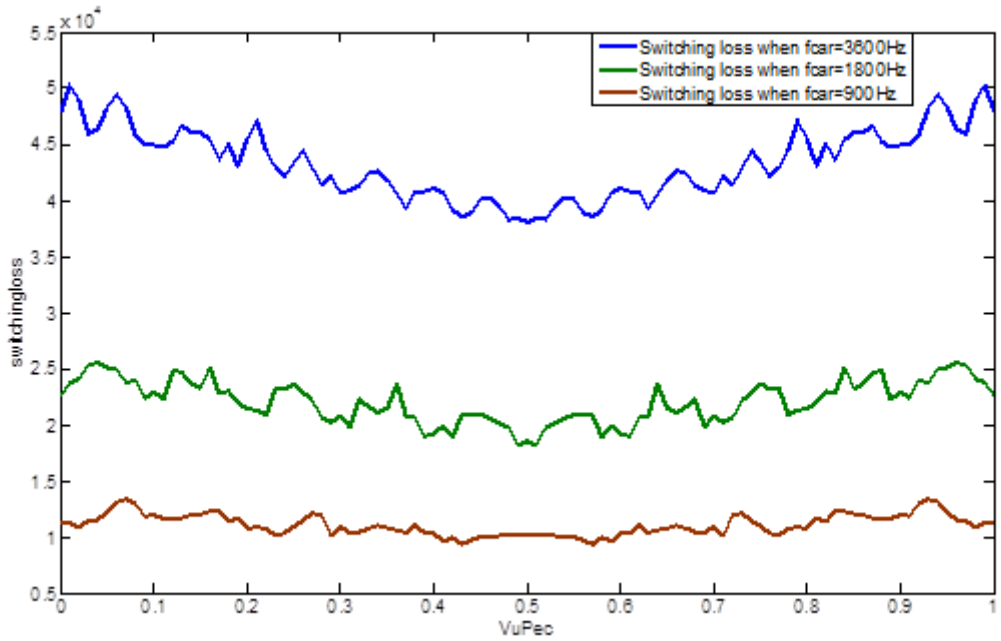


Figure A.9: Switching loss comparison when P=10MW, carrier frequency is 3600Hz, 1800Hz,900Hz

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