# Matrix Converter Based on Trapezoidal Current Injection

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Abstract- The Matrix Converter (MC) is a direct AC-AC power converter featuring high power density and high efficiency. However, the conventional MC (CMC) topologies require high control complexity and high transistor capacity, hindering the wide applications. An emerging MC topology (3CI-MC) based on the third-harmonic current injection (3CI) reduces the control complexity, but require more transistors and complex clamping circuit. This paper proposes the trapezoidal current injection (TCI) technique to form a novel MC topology (TCI-MC), which consists of a line-commutated converter (LCC), a TCI circuit and a voltage source converter (VSC). Compared with the 3CI-MC, the proposed TCI-MC not only maintains the advantages of simple modulation and independent voltage control, but also achieves lower current stress on the LCC part of the circuit. The total transistor capacity of the proposed TCI-MC is the lowest among all the considered MC topologies. The clamping circuit is also simplified and the bidirectional switches are eliminated, reducing the implementation cost. Simulation and experimental results have verified the validity of the proposed topology.

## I. INTRODUCTION

A C-AC converters are widely used in industry applications, such as adjustable speed drives and renewable energy integration [1]-[2]. The typical AC-AC converter topology with bidirectional power flow capability is the back-to-back (B2B) converter, as shown in Fig. 1(a), which is composed of two voltage source converters (VSCs). The B2B converter features a simple structure and control. The cost is also relatively low. Yet, it requires bulky filter inductors and large DC-link capacitors [3]. Besides, the switching losses are relatively high, since all the devices work in PWM mode [4].

The matrix converter (MC), which achieves direct power conversion without intermediate energy storage elements, is considered a promising alternative to the B2B converter [5]-[6]. The conventional MC (CMC) topologies include the direct (DMC) and indirect (IMC) type [3], as shown in Fig. 1(b) and Fig. 1(c) respectively. Each bidirectional switch required by CMCs is usually constructed with two transistors. It has been demonstrated that CMCs can achieve much higher power density and efficiency than B2B converters [7]-[9]. Therefore, CMCs have received extensive and continuous attention for decades [10]-[12]. Nevertheless, the input and output control of CMCs are tightly coupled in the modulation, resulting in the complex switching sequences for normal operation. This is the side-effect of eliminating intermediate energy storage elements [13]. Besides, CMCs require 18 transistors handling the full power, resulting in much higher transistor VA capacity than the B2B converter [3]. Consequently, CMCs are often criticized for the higher complexity and cost compared to the B2B converter. These drawbacks have hindered the wide applications of CMCs.



Fig. 1 (a) the typical back-to-back (B2B) converter; (b) the direct matrix converter (DMC); (c) the indirect matrix converter (IMC).

To improve the performance of CMCs, various advanced variants of MC topologies have been proposed in literature, mainly motivated by the physical two-stage feature of the IMC. In [14], the sparse MCs are proposed by modifying the rectifier stage of IMC, which reduces the transistor count but at the cost of higher conduction losses or losing bidirectional power flow capability. Incorporating the Z-source networks at the input or the DC-link of CMCs produces the topologies of Z-source MCs [15]-[16]. The Z-source MCs are able to boost the voltage utilization ratio [17], but the power density is reduced since some large passive components are used. Many other improved MC topologies can also be found in literature [18]-[21]. Though these topologies are advantageous in some specific applications, but the CMCs still dominate studies in the general cases.

In [22], a novel MC topology (3CI-MC) based on active third-harmonic current injection (3CI) is proposed, as shown in Fig. 2(a). The 3CI-MC can be derived by replacing the rectifier stage of IMC with a line-commutated converter (LCC) and a 3CI circuit in parallel. The LCC handles the main power flow while the 3CI compensates the harmonics generated by the LCC. The 3CI technique had been adopted in rectifier applications to promote the converter efficiency [23]. According to [22], the 3CI-MC not only maintains the major



Fig. 2 Topologies of matrix converter based on (a) active third-harmonic current injection (3CI); (b) trapezoidal current injection (TCI).

features of CMCs, but also achieves much lower control complexity since the input and output control can be easily decoupled in the modulation. No complex switching sequence is required by 3CI-MC. Also, the current stress of the 3CI circuit is only half of the input current amplitude. In recent years, progress was made with the 3CI-MC, further improving its performance. In [24] and [25], the 3CI-MC with multiple output-stage VSCs and the three-level T-type 3CI-MC are proposed. In [26], the input current distortion at the sector boundary is suppressed by adding a LC filter in the DC-link. In [27] and [28], improved 3CI-MC topologies with auxiliary switches are proposed to extend the control range of input reactive power.

The advantages of 3CI-MC prove that it is a promising MC topology. Motivated by the concept of 3CI technique, this paper proposes a trapezoidal current injection (TCI) technique and applies it to replace the 3CI technique, forming a novel MC topology (TCI-MC), as shown in Fig. 2(b). Compared with the emerging 3CI-MC, the proposed TCI-MC not only maintains its superior control performance, but also offers more advantages:

- Transistor count is reduced from 20 to 18.
- Clamping circuit is simplified with two fewer diodes.
- The LCC part has lower current stress.
- The total transistor capacity is reduced.
- Bidirectional switches are eliminated.

The rest of this paper is organized as follows: Section II introduces the operation and control of the proposed TCI-MC; Section III presents power loss analysis; Section IV shows the comparison with other AC-AC topologies; Section V provides the simulation and experimental results. Section VI draws the conclusion.

# II. OPERATION AND CONTROL OF TCI-MC

#### A. Topology Description

As shown in Fig. 2(b), the proposed topology is composed of three three-phase bridges which act as the LCC, TCI, and VSC. These three parts share the common DC-link without energy storage elements. An LC filter is placed at the input side of LCC, and hence the input of LCC should be considered as a three-phase voltage source imposed by the filter capacitors. Together with the three-phase input filter inductors  $L_h$ , the TCI is placed in parallel with the LCC. It should be noted that although the LCC and TCI have the same transistor configuration as the VSC, both of them are not fully controllable VSCs, because the electrical characteristics of the input and the DC-link of them are quite different to the typical VSC. If bidirectional power flow capability is not required, the LCC could be replaced with a simple three-phase diode rectifier to reduce cost. The detailed operation principle of the topology will be presented in this section.

By comparing Fig. 2(a) and (b), it is clear that the TCI-MC and 3CI-MC have the same LCC and VSC parts, and the difference lies in the additional current injection circuit. The TCI-MC only requires 18 transistors, the same with CMCs but two less than the 3CI-MC. Besides, since the bridges always provide a path for the inductor current, the clamping circuit of the TCI-MC consists of only a diode and a capacitor, two diodes less than the 3CI-MC. The advantage of the proposed TCI-MC is the lower current stress in the LCC circuit. Together with the low current stress on the TCI circuit, the proposed topology requires the lowest transistor capacity among all the considered MC topologies.

# B. Operation Principle of 3CI-MC

To better show how the proposed TCI-MC obtains sinusoidal input and output currents, the operation principle of 3CI-MC is firstly presented, its key waveforms are shown in Fig. 3. A comprehensive study of the 3CI technique can be referred to [22] and [23].

Table 1. Switching States of LCC and SCI in the SCI-MC											
$S_{hn}$	Shp	Sh56	Sh34	S <sub>h12</sub>	S <sub>16</sub>	S <sub>15</sub>	<b>S</b> <sub>14</sub>	S <sub>13</sub>	S <sub>12</sub>	S <sub>11</sub>	Sector
VM	PV	0	1	0	1	0	0	0	0	1	Ι
VM	PV	0	0	1	1	0	0	1	0	0	II
VM	PV	1	0	0	0	0	0	1	1	0	III
VM	PV	0	1	0	0	1	0	0	1	0	IV
VM	PV	0	0	1	0	1	1	0	0	0	V
VM	PV	1	0	0	0	0	1	0	0	1	VI

Table I. Switching States of LCC and 3CI in the 3CI-MC

Since the input of the LCC is a three-phase voltage source, the LCC cannot work in PWM mode. Switching states of the LCC in 3CI-MC are listed in Table I. In each input voltage sector, only the transistor in the upper arm corresponding to the maximum input voltage and the transistor in the lower arm corresponding to the minimum input voltage are turned on, while the rest transistors in the LCC maintain off. Therefore,



Fig. 3 Key waveforms (in p.u.) of the 3CI-MC and TCI-MC. All the terms represent only the low-frequency components. The input voltages, input currents, the DC-link voltage and current are the same for both converters.

the maximum input line-to-line voltage is always imposed on the DC-link of 3CI-MC. With the feedforward compensation of DC-link voltage fluctuation, the VSC part can generate balanced and sinusoidal output currents. In turn, the transferred active power  $p_{pn}$  on the DC-link is constant, the DC-link current  $i_{pn}$  fluctuates accordingly.

It is known that the LCC functions like a bidirectional diode rectifier. As a result, the LCC generates rich low-frequency harmonics in input currents if the 3CI circuit is disabled. Therefore, the objective of 3CI is to compensate for these low-



Fig. 4 Current flow paths of 3CI-MC and TCI-MC in sector II.

frequency harmonics. According to [22]-[23], the reference current  $i_h^*$  of 3CI is always equal to the reference input phase current corresponding to the middle input voltage.

$$i_{h}^{*} = \begin{cases} i_{iA}^{*}, |u_{iB}| \ge |u_{iA}| \ge |u_{iC}| \text{ or } |u_{iC}| \ge |u_{iA}| \ge |u_{iB}| \\ i_{iB}^{*}, |u_{iA}| \ge |u_{iB}| \ge |u_{iC}| \text{ or } |u_{iC}| \ge |u_{iB}| \ge |u_{iA}|. \end{cases}$$
(1)

The half bridge is composed of  $S_{hp}$  and  $S_{hn}$ , which are fully controllable and work in a PWM mode. With closed-loop control, the actual  $i_h$  of 3CI tracks  $i_h^*$ .

It can be inferred from (1) that, when the three-phase reference input currents are sinusoidal, the waveform of  $i_h$  is close to a triangular wave, as shown in Fig. 3 (a). Each of the three bidirectional switches (i.e.  $S_{h12}$ ,  $S_{h34}$ , and  $S_{h56}$ ) in the 3CI circuit is switched on when the corresponding input voltage is the middle, as listed in Table I. Therefore, each phase current (e.g.  $i_{hA}$  in sector II) of 3CI only takes a part of  $i_h$ . The injected harmonic current  $i_h$  affects the LCC currents in a manner such that all the three-phase input currents  $i_{iA}$ ,  $i_{iB}$ ,  $i_{iC}$  realize sinusoidal [22]-[23].

### C. Operation Principle of TCI-MC

In the proposed TCI-MC, the TCI circuit is composed of a three-phase bridge with a filter inductor for each input phase, which is similar to a VSC. However, each bridge in the TCI circuit is not always fully controllable, because the DC-link voltage of TCI-MC is not high enough. Each bridge therefore works in PWM mode only when the corresponding input voltage allows, while the switching state is fixed in the rest of the sectors. Switching states of LCC and TCI in TCI-MC are listed in Table II. The LCCs in TCI-MC and 3CI-MC have the same switching states.

Table II. Switching States of LCC and TCI in the TCI-MC

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Sector	S <sub>11</sub>	<b>S</b> <sub>12</sub>	S <sub>13</sub>	S <sub>14</sub>	S <sub>15</sub>	S <sub>16</sub>	S <sub>h1</sub>	S <sub>h2</sub>	S <sub>h3</sub>	S <sub>h4</sub>	S <sub>h5</sub>	S <sub>h6</sub>
Ι	1	0	0	0	0	1	1	0	PV	VМ	0	1
II	0	0	1	0	0	1	PV	ŴМ	1	0	0	1
III	0	1	1	0	0	0	0	1	1	0	PV	VМ
IV	0	1	0	0	1	0	0	1	PV	ŴМ	1	0
V	0	0	0	1	1	0	PV	ŴМ	0	1	1	0
VI	1	0	0	1	0	0	1	0	0	1	PV	VM

Taking sector II as an example to illustrate the operation principle of TCI-MC. In this sector, input voltages satisfy  $u_{iB} \ge u_{iA} \ge u_{iC}$ . Therefore, in the TCI circuit, transistors  $S_{h3}$  and  $S_{h6}$  are in the on-state while  $S_{h4}$  and  $S_{h5}$  are in the off-state

throughout sector II. The phase A bridge of the TCI is fully controllable, and thus  $S_{h1}$  and  $S_{h2}$  work in PWM mode. The current flow paths of 3CI-MC and TCI-MC in sector II are shown in Fig. 4.

The VSC part can be modelled as a current source  $i_{pn}$  at the DC-link. It is clear that, for input phase A, the current flow paths of 3CI-MC and TCI-MC are exactly the same if the voltage drops across the transistors are ignorable. Therefore, if PWM signals of  $S_{hp}$  and  $S_{hn}$  in the 3CI are applied to  $S_{h1}$  and  $S_{h2}$  in the TCI, the TCI-MC can obtain  $i_{iA}$  in the same way as 3CI-MC. Similarly,  $i_{iB}$  and  $i_{iC}$  in the TCI-MC are also the same as those in the 3CI-MC. Therefore, the proposed TCI-MC is able to achieve sinusoidal input currents, in the same manner as the 3CI-MC.

The key difference between the 3CI-MC and the TCI-MC is the input current distribution. When input voltages enter sector III from sector II,  $i_{hA}$  generated by the 3CI circuit drops to zero immediately since the bidirectional switch  $S_{h12}$  in 3CI-MC is turned off. However, for the TCI-MC,  $i_{hA}$  maintains constant in sector III, which can be inferred from the values of  $i_{hB}$  and  $i_{hC}$  in sector II. As shown in Fig. 4(b), voltage drops across the filter inductors of phase B and C are zero, assuming voltage drops across the transistors are negligible. As a result,  $i_{hB}$  and  $i_{hC}$  remain at their last values when the corresponding bridge works in PWM mode. Similarly,  $i_{hA}$  in sector III remains its last value in sector II. Therefore,  $i_{hA}$  presents the trapezoidal waveform throughout the six sectors, as shown in Fig. 3(b), which is the basis of the proposed technique.

From the above analysis it can be seen that  $i_{iA}$  is sinusoidal through the control of the TCI and  $i_{hA}$  is actively determined by the switching states of the TCI. Consequently,  $i_{IA}$  is passively determined by  $i_{iA}$  and  $i_{hA}$ , namely

$$i_{\rm lA} = i_{\rm iA} - i_{\rm hA}, \qquad (2)$$

where the capacitor current is ignored. As it can be seen from Fig. 3(b) and Fig. 4(b), the LCC and TCI in the TCI-MC share the input current stress. Therefore, compared with the 3CI-MC, the TCI-MC has more balanced current stress between LCC and TCI. This helps to improve the transistor utilization and reduce the total transistor capacity. The current stress will be further discussed in the Section IV.

# D. Modulation and Control Strategy

The modulation algorithm and control strategy for the proposed TCI-MC can be translated from the 3CI-MC with minor modifications, as shown in Fig. 5. The switching states of the LCC and TCI (except the bridge working in PWM mode) can be directly determined based on Table II. Since the DC-link voltage of TCI-MC is not constant, feedforward compensation is used in the modulation of the VSC part. Namely, the instantaneous DC-link voltage  $u_{pn}$  is calculated based on the measured input voltages and then used for normalizing the modulation (SVPWM) is adopted for generating the gate signals of the VSC. Closed-loop control can be applied to the output currents if necessary.

Because only one bridge of the TCI works in PWM mode in each sector, the three-phase TCI currents can share one



Fig. 5 Control strategy of the proposed TCI-MC

controller  $G_h(s)$ . The reference current  $i_h^*$  is calculated from the supply voltages and reference output active power  $P_o^*$ , which is exactly the same with that in the 3CI-MC [22]. The feedback signal  $i_h$  is selected from the three-phase TCI currents, depending on which phase bridge in the TCI works in PWM mode:

$$i_{\rm h} = \begin{cases} i_{\rm hA}, |u_{\rm iB}| \ge |u_{\rm iA}| \ge |u_{\rm iC}| \ or \ |u_{\rm iC}| \ge |u_{\rm iA}| \ge |u_{\rm iB}| \\ i_{\rm hB}, |u_{\rm iA}| \ge |u_{\rm iB}| \ge |u_{\rm iC}| \ or \ |u_{\rm iC}| \ge |u_{\rm iB}| \ge |u_{\rm iA}|. \end{cases} (3)$$
$$i_{\rm hC}, |u_{\rm iA}| \ge |u_{\rm iC}| \ge |u_{\rm iB}| \ or \ |u_{\rm iB}| \ge |u_{\rm iC}| \ge |u_{\rm iA}|.$$

As presented above, both  $i_h^*$  and  $i_h$  are triangular waves, which is the same as that in the 3CI-MC. The frequency of  $i_h^*$ is  $3\omega$ , and the main component of  $i_h^*$  is the 3<sup>th</sup> harmonic, where  $\omega_i$  is the input angular frequency. Resonant controller is then adopted. Namely, the controller  $G_h(s)$  is expressed as

$$G_{\rm h}(s) = \frac{(k_{\rm r1}s + k_{\rm r2})(L_{\rm h}s + R_{\rm h})}{s^2 + (3\omega_{\rm i})^2},$$
(4)

where  $L_h$  and  $R_h$  are the inductance and parasitic resistance of the filter inductor for the TCI circuit;  $k_{r1}$  and  $k_{r2}$  are two parameters for adjusting the bandwidth.

# **III. POWER LOSS ANALYSIS**

This section presents the power loss analysis for both the 3CI-MC and TCI-MC. For simplicity, only the typical mode with forward power flow is considered, while the reverse power flow can be analyzed similarly. IGBTs are used for analysis. The MOSFETs may generate different results but the analysis method can be easily transplanted.

#### A. Semiconductor Losses

The average and RMS values of currents flowing through the semiconductor devices in the two converters are comparatively listed in Table III, where the current values of the 3CI-MC are provided by [22]. As for the TCI-MC, the current values of VSC are the same as those of the 3CI-MC. The difference lies in the current values of LCC and TCI, which can be calculated based on the waveforms shown in Fig. 3, where  $I_{DLCC}$  and  $I_{DTCI}$  represent the current flowing through the diodes in the LCC and TCI respectively;  $I_{STCI}$  represents the current flowing through the transistors in the TCI.

The conduction and switching loss of the semiconductor devices can be estimated by the current values and other parameters [22]:

$$P_{\rm C,S} = I_{\rm S,AVG} U_{\rm CE0} + I_{\rm S,RMS}^2 R_{\rm s}, \qquad (5)$$

Semiconductor de	Semiconductor devices		$I_{\rm RMS}(A)$
	<i>S</i> <sub>li</sub> (i=1~6)	0	0
LCC of 3CI-MC	D <sub>li</sub> (i=1~6)	$\frac{\sqrt{3}I_{\rm im}}{2\pi}$	$I_{\rm im}\sqrt{rac{1}{6}+rac{\sqrt{3}}{8\pi}}$
	$S_{\rm h12}, S_{\rm h34}, S_{\rm h56}$	$\frac{I_{\rm im}\left(2-\sqrt{3}\right)}{2\pi}$	$I_{\rm im}\sqrt{rac{1}{12}-rac{\sqrt{3}}{8\pi}}$
3CI	$S_{ m hp},S_{ m hn}$	$\frac{3I_{\rm im}}{4\pi} \Big(2 - \sqrt{3}\ln 3\Big)$	$I_{\rm im}\sqrt{\frac{1}{8}+\frac{3\sqrt{3}}{4\pi}\ln\!\left(\frac{3}{4}\right)}$
	$D_{ m hp}, D_{ m hn}$	$\frac{3I_{\rm im}}{4\pi} \Big(2 - 2\sqrt{3} + \sqrt{3}\ln 3\Big)$	$I_{\rm im}\sqrt{\frac{1}{8}+\frac{3\sqrt{3}}{4\pi}\left(\ln\left(\frac{4}{3}\right)-\frac{1}{2}\right)}$
	$S_{\rm li}$ (i=1~6)	0	0
LCC of TCI-MC	<i>D</i> <sub>li</sub> (i=1~6)	$\left(\frac{\sqrt{3}}{2\pi} - \frac{1}{6}\right) I_{\rm im}$	$I_{ m im}\sqrt{rac{1}{4}-rac{3\sqrt{3}}{8\pi}}$
TCI	<i>S</i> <sub>hi</sub> (i=1~6)	$\frac{I_{\rm im}}{2\pi} \left(1 - \frac{\sqrt{3}\ln 3}{2}\right)$	$I_{\rm im}\sqrt{\frac{1}{24} + \frac{\sqrt{3}}{4\pi}\ln\left(\frac{3}{4}\right)}$
	D <sub>hi</sub> (i=1~6)	$\frac{I_{\rm im}}{2\pi} \left(\frac{\pi}{3} + 1 - \sqrt{3} + \frac{\sqrt{3}\ln 3}{2}\right)$	$I_{\rm im}\sqrt{\frac{1}{8}+\frac{\sqrt{3}}{4\pi}\left(\ln\left(\frac{4}{3}\right)-\frac{1}{2}\right)}$
VSC of 3CLMC and TCLMC	$S_{\rm ip}, S_{\rm in}$ (i=u, v, w)	$\frac{I_{\rm om}}{2\pi} \left( 1 + \frac{\sqrt{3}q\cos\varphi_{\rm o}}{2} \ln\left(2 + \sqrt{3}\right) \right)$	$I_{\rm om} \sqrt{\frac{1}{8} - \frac{q\cos\varphi_{\rm o}}{8\pi} \left(\frac{9}{8}\ln 2 - \frac{27}{16}\ln 3 - \frac{5\sqrt{3}\pi}{16}\right)}$
	$D_{\mathrm{ip}}, D_{\mathrm{in}}(\mathrm{i=u, v, w})$	$\frac{I_{\rm om}}{2\pi} \left( 1 - \frac{\sqrt{3}q\cos\varphi_{\rm o}}{2} \ln\left(2 + \sqrt{3}\right) \right)$	$I_{\rm om} \sqrt{\frac{1}{8} + \frac{q \cos \varphi_{\rm o}}{8\pi} \left(\frac{9}{8} \ln 2 - \frac{27}{16} \ln 3 - \frac{5\sqrt{3}\pi}{16}\right)}$

Table III Average and RMS values of the currents flowing through devices in the 3CI-MC and TCI-MC

Note:  $I_{om}$  is the amplitude of output current; q is the voltage transfer radio;  $\varphi_0$  is the load power factor angle.

$$\begin{split} P_{\mathrm{S},\mathrm{S}} &= k_s U_{\mathrm{S,max}} I_{\mathrm{S,AVG}} f_{\mathrm{s}}, \end{split} \tag{6} \\ P_{\mathrm{C,D}} &= I_{\mathrm{D,AVG}} U_{\mathrm{D0}} + I_{\mathrm{D,RMS}}^2 R_{\mathrm{D}}, \end{split} \tag{7}$$

where 
$$P_{C,S}$$
,  $P_{S,S}$  and  $P_{C,D}$  are the conduction loss of IGBTs, the  
switching loss of IGBTs and the loss of diodes, respectively;  
 $U_{CE0}$  and  $U_{D0}$  are the forward voltage of IGBTs and diodes at  
zero current;  $R_s$  and  $R_D$  are the dynamic on-resistance of  
IGBTs and diodes;  $I_{S,AVG}$ ,  $I_{S,RMS}$ ,  $I_{D,AVG}$  and  $I_{D,RMS}$  are the  
average and RMS currents of IGBTs and diodes;  $U_{S,max}$  is the  
voltage stress of IGBTs;  $k_s$  is the switching loss coefficient;  $f_s$   
is the switching frequency. These parameters can be obtained  
from datasheets of the selected IGBT (Part No.

#### B. Inductor Losses

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The inductor loss consists of two parts: the core loss and the parasitic resistor loss. With properly selected magnetic core, the core loss is neglected and only parasitic resistor loss is considered.

1) Loss of  $L_{\rm f}$ : The current of  $L_{\rm f}$  is the input current, so the parasitic resistor loss of Lf can be calculated as

$$P_{\rm Lf} = \left(\frac{I_{\rm im}}{\sqrt{2}}\right)^2 R_{\rm f} = \frac{1}{2} I_{\rm im}^2 R_{\rm f} \,. \tag{8}$$

Eq. (8) is suitable for both 3CI-MC and TCI-MC.

2) Loss of  $L_h$ : The RMS value of  $i_h$  in 3CI-MC can be expressed as

$$I_{\rm h\_RMS} = \sqrt{\frac{3}{\pi}} \left( \int_{\frac{\pi}{3}}^{\frac{\pi}{2}} I_{\rm im}^2 \cos^2 \theta d\theta \right) = I_{\rm im} \sqrt{\frac{1}{4} - \frac{3\sqrt{3}}{8\pi}}$$
(9)

Ignoring the inductor current change in the freewheeling mode, the RMS value of  $i_{hA}$  can be calculated as

$$I_{hA\_RMS} = \sqrt{\frac{1}{\pi}} \left[ 2 \int_{0}^{\frac{\pi}{3}} \left( \frac{I_{im}}{2} \right)^{2} d\theta + \int_{\frac{\pi}{3}}^{\frac{\pi}{2}} I_{im}^{2} \cos^{2} \theta d\theta \right]$$
(10)  
=  $I_{im} \sqrt{\frac{1}{4} - \frac{\sqrt{3}}{8\pi}}$ 

The parasitic resistor losses in 3CI-MC and TCI-MC are obtained as

$$P_{\text{Lh}_{3\text{CI-MC}}} = I_{\text{h}_{\text{RMS}}}^2 R_{\text{h}} \approx 0.04 I_{\text{im}}^2 R_{\text{h}}$$
(11)

$$P_{\rm Lh\_TCI-MC} = I_{\rm hA\_RMS}^2 R_{\rm h} \approx 0.18 I_{\rm im}^2 R_{\rm h}$$
(12)

### C. Quantitative Results

Considering the same working conditions, the power losses of 3CI-MC and TCI-MC are listed in Table IV. The parameters used in analysis are the same with those provided in experiments.

It can be seen from Table IV that the proposed TCI-MC can achieve slightly lower power loss than 3CI-MC. This is mainly because the current stress on the LCC part is smaller. However, it should be noted that the quantitative results listed in Table IV are not of high precision. This is because the parameters for loss analysis are obtained from the figures of the device datasheet, which is not accurate enough. Besides, at

	TCI-MC	3CI-MC	DMC	IMC	B2B
Transistor Count	18	20	18	18	12
Bidirectional Switch Count	0	3	9	6	0
Transistor Voltage Stress	18: U <sub>ilm</sub>	20: U <sub>ilm</sub>	18: $U_{\rm ilm}$	18: $U_{\rm ilm}$	12: U <sub>pn</sub>
Transistor Current Stress	12: <i>I</i> <sub>om</sub> ; 6: 0.5 <i>I</i> <sub>im</sub>	6: $I_{om}$ ; 6: $I_{om}$ +0.5 $I_{im}$ ; 8: 0.5 $I_{im}$	18: <i>I</i> <sub>om</sub>	18: <i>I</i> <sub>om</sub>	6: <i>I</i> <sub>om</sub> , 6: <i>I</i> <sub>im</sub>
Total Transistor Capacity	$12U_{\rm ilm}I_{\rm om}+3U_{\rm ilm}I_{\rm im}$	$12U_{\rm ilm}I_{\rm om}+6U_{\rm ilm}I_{\rm im}$	$18U_{\rm ilm}I_{\rm om}$	$18U_{\rm ilm}I_{\rm om}$	$6U_{\rm pn}I_{\rm om}+6U_{\rm pn}I_{\rm im}$
Conduction Losses	Low	Low	Low	High	Low
Switching Losses	Low	Low	Low	Low	Very High
Additional Clamping Circuit	1 Diode 1 Capacitor	3 Diodes 1 Capacitor	6 Diodes 1 Capacitor	1 Diode 1 Capacitor	/
Modulation Complexity	Low	Low	High	Medium	Low
Max. Voltage Transfer Ratio	$\sqrt{3}/2$	$\sqrt{3}$ / 2	$\sqrt{3}\cos\varphi_{\rm i}/2$	$\sqrt{3}\cos\varphi_{\rm i}/2$	≥1
DC-link Capacitors	No	No	No	No	Large
Input Filter Components	$3L_{\rm f}+3C_{\rm f}+3L_{\rm h}$	$3L_{\rm f}+3C_{\rm f}+1L_{\rm h}$	$3L_{\rm f}+3C_{\rm f}$	$3L_{\rm f}+3C_{\rm f}$	3L <sub>f</sub>

Table V Comparison between the proposed TCI-MC and other AC-AC converters

Note: Comparison among DMC, IMC and B2B can be referred to [7]. The comparison in this table is made incrementally.  $\varphi_i$  is the input power factor angle.

every point of the MC systems, the voltage or current is not constant DC-signal. This means the power loss is always timevariable. Moreover, the power loss of a practical converter depends on many other factors, such as temperature, PCB wiring, gate drivers, parameter mismatch, and etc. To the best knowledge of authors, the mismatch between theoretical loss analysis and experiments is very common in publications of MCs. Yet, the presented analysis process still has reference value to show the differences between 3CI-MC and TCI-MC, if more accurate parameters of the semiconductor devices are available.

			3CI-MC	TCI-MC
		$P_{\rm C,S}$	0 W	0 W
	LCC	$P_{S,S}$	0 W	0 W
	LCC	$P_{\rm C,D}$	24.47 W	8.64 W
		Total	24.47 W	8.64 W
	3CI or TCI	$P_{\rm C,S}$	16.66 W	8.52 W
Comison duston		$P_{\rm S,S}$	12.43 W	12.68 W
losses		$P_{\rm C,D}$	10.85 W	26.91 W
108868		Total	39.94 W	48.11 W
	VSC	$P_{\rm C,S}$	8.92 W	8.92 W
		$P_{\mathrm{S},\mathrm{S}}$	65.14 W	65.14 W
		$P_{\rm C,D}$	3.77 W	3.77 W
		Total	77.83 W	77.83 W
	Total		142.24 W	134.58 W
Indu	ctor Losses	9.65 W	12.76 W	
Tot	al Losses	151.89 W	147.34 W	
Rat	ted power	5.76 kW	5.76 kW	
Calcula	ted Efficiency	97.36%	97.44%	

Table IV. Power Losses of the 3CI-MC and TCI-MC

# IV. COMPARISON WITH OTHER AC-AC CONVERTERS

To highlight the advantages and disadvantages, this section further makes the comparison between the proposed TCI-MC with other AC-AC converters. The selected MC include the 3CI-MC, DMC and IMC as they have similar features with the proposed TCI-MC. The closest rival is the 3CI-MC. The comparison is considered for general applications. Other MC topologies which have different features are not considered. In addition, the widely used B2B converter is included in the comparison. Since the comprehensive comparison between DMC, IMC and B2B has been made in [7], the comparison in this section is made incrementally. The results are listed in Table V. The next sections will show the detailed comparison for some key aspects.

# A. Transistor Count

It can be seen from Fig. 1 and Fig. 2(b) that the TCI-MC and CMCs require 18 transistors, the 3CI-MC requires 20 transistors, while the B2B requires only 12 transistors. Usually, a transistor should be used in the clamping circuit for discharging the clamping capacitors. However, it has small capacity and thus is omitted.

Note that the bidirectional switch is indispensable in CMCs and 3CI-MC. Theoretically, this is not an issue for the operating performance. Yet, the bidirectional switch module is far less common than the half-bridge module in commercial market. From this point of view, compared with other MC topologies, the proposed TCI-MC is able to reduce the implementation cost since it can be constructed with nine half-bridge modules.

#### B. Voltage Stress

Like CMCs, all the transistors in the TCI-MC need to withstand the maximum input line-to-line (L-L) voltage. Therefore, the voltage stresses of CMCs and TCI-MC are all  $U_{\rm ilm}$  which denotes the amplitude of input L-L voltage.

For 3CI-MC, the LCC part, the VSC part and the halfbridge in the 3CI circuit also need to withstand the maximum input L-L voltage. With proper modulation, bidirectional switches in the 3CI circuit only need to withstand the minimum input (L-L) voltage. This means that the voltage stress on the 3CI circuit is only  $0.866U_{ilm}$ . Yet, selection of these transistors must consider the worst and unpredictable cases. As a result, it is reasonable to assume that the voltage stress of all the transistors in 3CI-MC is also  $U_{ilm}$ .

All the considered MC topologies have lower voltage stress than the B2B converter, since the latter has to withstand the maximum DC-link voltage  $U_{pn}$ . For linear modulation, the  $u_{pn}$ 

of B2B should be higher than  $U_{ilm}$  in practice, e.g.  $U_{pn} = 1.1U_{ilm}$ .

### C. Current Stress

In this paper, the current stress on a transistor is defined as the maximum current flowing through it. For CMCs, the current stress is determined by the output current amplitude  $I_{om}$ . For the 3CI-MC and TCI-MC, the current stresses on the 3CI and TCI are the amplitude of the injected harmonic current, which is only  $0.5I_{im}$  where  $I_{im}$  is the input current amplitude.

The difference between 3CI-MC and TCI-MC lies in the current stress on the LCC parts. As shown in Fig. 2, the output current  $i_{LCC}$  of LCC in 3CI-MC can be expressed as

$$i_{\rm LCC} = i_{\rm pn} - i_{\rm hp},\tag{13}$$

where  $i_{pn}$  is the DC-link current flowing into the VSC;  $i_{hp}$  is the current flowing though the transistor  $S_{hp}$ . Due to the lack of DC-link filter components,  $i_{pn}$  has the pulsed waveform of which the maximum is the output current amplitude  $I_{om}$  and the minimum is zero. Certainly, this is only true for the unity output power factor. Under a non-unity output power factor, the maximum and minimum of  $i_{pn}$  could be different, but the analysis can be handily extended. Like  $i_{pn}$ ,  $i_{hp}$  is pulsed between  $i_h$  and 0. Since  $i_h$  is a triangular waveform with an amplitude of  $0.5I_{im}$ , the maximum of  $i_{hp}$  is  $0.5I_{im}$  while the minimum is  $-0.5I_{im}$ . Therefore, the current stress on the LCC in the 3CI-MC can be obtained

$$I_{\rm LCC,peak} = \max(i_{\rm pn}) - \min(i_{\rm hp}) = I_{\rm om} + 0.5I_{\rm im}.$$
 (14)

As shown in Fig. 2(b),  $i_{LCC}$  in the TCI-MC is expressed as

$$i_{\rm LCC} = i_{\rm pn} - (i_{\rm hAp} + i_{\rm hBp} + i_{\rm hCp}) = i_{\rm pn} - i_{\rm hTp},$$
 (15)

where  $i_{hAp}$ ,  $i_{hBp}$  and  $i_{hCp}$  are currents flowing through  $S_{h1}$ ,  $S_{h3}$ and  $S_{h5}$  respectively;  $i_{hTp}$  is the sum of  $i_{hAp}$ ,  $i_{hBp}$  and  $i_{hCp}$ . According to the operation principle of TCI-MC, in each sector, there will be always one current of  $i_{hAp}$ ,  $i_{hBp}$  and  $i_{hCp}$ that maintains  $0.5I_{im}$ , one current is the pulsed triangular waveform of which the amplitude is  $0.5I_{im}$ , and the rest one is zero. This means that the maximum of  $i_{hTp}$  is  $I_{im}$  and the minimum is zero. Therefore, the current stress on the LCC part of the TCI-MC can be obtained as

$$I_{\text{LCC,peak}} = \max\left(i_{\text{pn}}\right) - \min\left(i_{\text{hTp}}\right) = I_{\text{om}}.$$
 (16)

(14) and (16) indicate that, compared with the 3CI-MC, the proposed TCI-MC has lower current stress on the LCC part, while the current stresses on the rest circuits are not changed.

Note that, the above analysis ignores the parasitic resistance of the filter inductors. In practice, the TCI current would drop slowly in the desired flat area, subject to the time constant of the filter inductor. This will influence the current distribution and the current stress. However, the total input currents ( $i_{iA}$ ,  $i_{iB}$ and  $i_{iC}$ ) are not influenced and can still achieve sinusoidal, since they are determined by the control of the TCI circuit. Besides, the proposed topology is still able to reduce the current stress on the LCC circuit, since the TCI always shares the current stress between the devices.

# D. Total Transistor Capacity (TTC)

The total transistor capacity (TTC) of a converter is an important factor influencing the cost. The TTC is related with the transistor count N, the voltage rating and current rating. For simplicity, the TTC index is defined as

$$TTC = \sum_{i=1}^{N} U_{Ri} I_{Ri}, \qquad (17)$$

where  $U_{Ri}$  and  $I_{Ri}$  are the voltage rating and current rating of the *i*th transistor respectively.

Usually,  $U_{Ri}$  and  $I_{Ri}$  are proportional to the voltage stress and current stress respectively. The proportional gain reflects the capacity margin for safe operation. Herein, the gain is considered as unity for simplicity. The TTC can be then calculated for each converter according to the discussion presented in part B and part C of this section. The results are listed in the 6<sup>th</sup> row of Table V. Note that, for MCs,  $I_{im}$  should be less than 0.866 $I_{om}$  in the linear modulation region [7]. It is clear that the TTC of TCI-MC is the lowest among all the MC topologies, which is the benefit of the lower current stress on LCC. Besides, the TTC of TCI-MC approaches that of B2B, indicating that the proposed topology has narrowed the gap between MCs and B2B in terms of transistor cost.

# E. Power Loss

The analysis in Section III shows that the TCI-MC generates slightly lower power loss than the 3CI-MC. This part will further compare them with the CMCs and B2B. Note that more rigorous analysis about CMCs and B2B has been provided in [7]. Due to the limited space, the quantitative analysis about CMCs and B2B are not presented in this paper. Yet, the qualitative discussion is sufficient to get the valuable conclusion.

1) Conduction loss: For a converter, the conduction loss is mainly determined by the count of transistors on the current flow path. Clearly, both the DMC and B2B have very low conduction losses, since only four transistors are located on the current flow path from input side to output side. The conduction loss of IMC is much higher because six transistors are on the path. For 3CI-MC, the 3CI and VSC handle the major power and four transistors are on the path. Though there are more transistors on the current low path of 3CI, the injected current is very small. From this point of view, the conduction loss of 3CI-MC is slightly higher than the DMC, but the difference is ignorable in the total power loss. For the proposed TCI-MC, fewer transistors are in the flow path of the injected harmonic current, as shown in Fig. 4(b). Therefore, the conduction loss of TCI-MC is lower than 3CI-MC. From the input to output, it can be approximately considered that only four transistors are located on the current flow path, despite that some currents have different low path. Therefore, the TCI-MC also has low conduction loss, just like the DMC and B2B.

2) Switching loss: According to the operation principle of 3CI-MC and TCI-MC, they have quite close switching loss which is mainly contributed by the VSC part. Note that, the VSC part is similar to the inverter stage of IMC. Therefore, it can be inferred that the switching loss of 3CI-MC and TCI-MC are slightly higher than IMC, as the input stage of IMC

can achieve zero-current switching [7]. Yet, the injected harmonic current is very small and thus the switching loss of 3CI and TCI circuits only account for a small portion in the total power loss. Therefore, the switching loss of 3CI-MC and TCI-MC is close to the CMCs. They can all achieve much higher efficiency than B2B as both stages of B2B work in hard-switching mode with high chopping current.

3) Inductor loss: Since the 3CI-MC and TCI-MC requires more filter inductors for the harmonic injection circuit, they generate more inductor losses than the CMCs. However, since the inductors in B2B are much larger than that required by MCs, the differences among 3CI-MC, TCI-MC and CMCs are ignorable.

Based on the above analysis, it can be known that the DMC is the most efficient topology. The 3CI-MC and TCI-MC are less efficient than DMC, but is more efficient than IMC. Yet, all the MC topologies can be considered high-efficiency AC-AC converters compared with the B2B, which is consistent with the study in [7].

#### F. Passive Components

It was shown in [7] that the passive components of CMCs could be significantly smaller than the B2B, contributing to the higher power density of CMCs. Compared with CMCs, a 3CI-MC requires one additional filter inductor while the TCI-MC requires three. The design of these inductors is presented in [22]. This is the major drawback of the proposed TCI-MC compared with CMCs and 3CI-MC. In practice, a small filter inductor  $L_h$  is used since the amplitude of the injected harmonic current is only half of the input current amplitude. Moreover, reducing  $L_h$  would not deteriorate the input power quality since the input LC filter is sufficient to attenuate the high-frequency harmonics. Therefore, considering the advantages of the TCI-MC, the cost of the small additional filter inductors is worthy.

#### G. Summary

From the analysis in section II and the comparison in this section, it can be seen that the proposed TCI-MC inherits the advantages of the 3CI-MC, including lower modulation complexity and independent output voltage control. Besides, it has reduced the current stress of the LCC part and further the total transistor capacity, simplified the clamping circuit and eliminated the bidirectional switches. Other merits of TCI-MC and 3CI-MC are similar to the CMCs. Therefore, it can be concluded that the proposed TCI-MC is a promising MC topology with superior comprehensive performance.

#### V. SIMULATION AND EXPERIMENTAL RESULTS

#### A. Simulation and Experimental Parameters

To verify the effectiveness of the proposed TCI technique, a TCI-MC prototype has been constructed, as shown in Fig. 6. Parameters of the prototype are provided in Table VI. For comparison, the 3CI-MC was constructed by replacing the TCI part with a 3CI circuit, the experimental parameters are the same with TCI-MC. The rated output current amplitude is 16 A, and the corresponding rated power is 5.76 kW. A PI-



Fig. 6 Experimental prototype of TCI-MC.

based closed-loop control is applied to the output currents in the synchronous reference frame. A Chroma 61845 programmable AC source acts as the power supply.

Since the input currents of the LCC after the filter capacitors are unavailable in practice. Simulation verification is also implemented to show the current stress comparison. The simulation parameters are the same as the experimental parameters, except that ideal transistors and filter components were used in the simulation.

	TABLE VI Experimental Faramete	15
Variables	Description	Values
$U_{\rm s}$	Nominal Input Voltage (Phase RMS)	220 V
$f_{\mathrm{i}}$	Nominal Input Frequency	50 Hz
$I_{\rm om}$	Nominal Amplitude of Output Current	16 A
$f_{\rm o}$	Nominal Output Frequency	50 Hz
$L_{ m f}$	Input Filter Inductor	1 mH
$R_{ m f}$	Resistance of $L_{\rm f}$	0.04 Ω
$C_{ m f}$	Input Filter Capacitor	15 μF
$R_{ m d}$	Damping Resistor of the Input Filter	15 Ω
$L_{ m h}$	Filter Inductor for the Injection Circuit	1 mH
$R_{ m h}$	Resistance of $L_{\rm h}$	0.04 Ω
$L_{ m o}$	Output Inductor	2 mH
$R_{ m o}$	Output Resistor	15 Ω
IGBT	Power Switches	IKY40N120CS6
DSP	Digital Signal Processor	TMS320F28379D
$f_{\rm sw}$	Switching Frequency	16 kHz
$f_{ m sa}$	Sampling Frequency	32 kHz
$K_{r1}$	First parameter of $G_h(s)$	$1.26 \times 10^{4}$
$K_{r2}$	Second parameter of $G_{\rm h}(s)$	3.86×10 <sup>7</sup>

#### B. Simulation Results

The simulation results are shown in Fig. 7. It can be seen that, the TCI-MC obtains exactly the same input and output currents as the 3CI-MC. Both topologies achieve sinusoidal currents at the input and output sides. The key differences between the two topologies lie in the currents of the LCC and the harmonic current injection circuit. In the 3CI-MC, the 3CI current  $i_{hA}$  drops to zero immediately when the corresponding phase voltage  $u_{sA}$  becomes maximum or minimum. The amplitude of the LCC current  $i_{lA}$  after the filter capacitor is up to 22 A, which is consistent with the theoretical analysis presented in (14). The  $i_{lA}$  before the filter capacitor represents its low-frequency component plus the high-frequency component in  $i_{hA}$ . It can be shown that the amplitude of the low-frequency component of  $i_{lA}$  is about 12.5A, the same with the amplitude of the input current  $i_{lA}$ .

In the TCI-MC, the TCI current  $i_{hA}$  maintains its last value when the corresponding phase voltage  $u_{sA}$  becomes maximum



Fig. 7 Simulation results of (a) 3CI-MC and (b) TCI-MC. Ideal transistors and filter components are adopted in simulation.

or minimum.  $i_{hA}$  presents the trapezoidal waveform, except some high-frequency components are observed when the corresponding voltage is the middle. It can be seen that the amplitude of  $i_{IA}$  after the capacitor is 16A, the same as the output current amplitude. Besides, the amplitude of  $i_{IA}$  before the capacitor is only 6.25A, half of the amplitude of the input current  $i_{IA}$ .

The simulation results have verified that the proposed TCI-MC can achieve the same input and output control performance as the emerging 3CI-MC, but the current stress between the LCC and TCI is more balanced. The current stress on the LCC part is lower than that in the 3CI-MC.

# C. Experimental Results

Experimental results of the 3CI-MC and TCI-MC are shown in Fig. 8 (a) and (b). The filter capacitors are placed as close as to the input of LCC, only the current  $i_{IA}$  before the filter capacitor  $C_f$  is presented. It can be seen that the input and output currents of both the 3CI-MC and TCI-MC are highly sinusoidal. For 3CI-MC, the THDs of  $i_{iA}$  and  $i_{oU}$  are 3.48% and 3.71% respectively. For TCI-MC, the THDs become

3.35% and 3.77%. Therefore, the two topologies can achieve commensurate steady-state control performance.

The key differences between the two topologies lie in the waveforms of  $i_{1A}$  and  $i_{hA}$ . For 3CI-MC, because  $i_{hA}$  drops to zero when  $u_{sA}$  is maximum or minimum among all the threephase voltages, the amplitude of  $i_{1A}$  is the same with  $i_{iA}$ . On the contrary, the  $i_{hA}$  of the TCI-MC in this period is not zero, and thus  $i_{1A}$  is much lower than  $i_{iA}$ . This means the current stress on the LCC part stress is reduced. Note  $i_{hA}$  decreases gradually in this period, resulting from the non-zero resistance of the filter inductors. This will also affect the waveform of  $i_{1A}$ . Even so, the amplitude of  $i_{1A}$  in the TCI-MC is still much lower than for the 3CI-MC.

By changing the reference amplitude of output current, the efficiency curves of 3CI-MC and TCI-MC can be obtained as shown in Fig. 9. It can be seen that the efficiencies are quite close to each other. The efficiency under nominal load is 96.98% for 3CI-MC and 97.04% for TCI-MC. The measured efficiency is slightly lower than calculated. This is because the prototype efficiency is affected by many other factors, such as temperature, PCB wiring, gate drivers, parameter mismatch,



Fig. 8 Experimental results of (a) 3CI-MC and (b) TCI-MC at the steady-state.



Fig. 9 Efficiency of 3CI-MC and TCI-MC under different output currents.

and etc. Considering the measurement error, such difference is ignorable. This is mainly because the conduction loss difference between the input stages of 3CI-MC and TCI-MC is limited and thus is concealed in the total converter loss. Anyhow, Fig. 9 proves that both TCI-MC and 3CI-MC can achieve relatively high efficiency.

Fig. 10 shows the experimental results when the input voltages are disturbed by 5% fundamental negative sequence component, 5% 5th harmonic and 5% 7th harmonic. The considered disturbances cover the most common disturbances in practice. It can be seen that, both the 3CI-MC and TCI-MC could achieve highly sinusoidal output currents even under the severe input disturbances, proving the performance of the two topologies with the associated control strategy. The input currents are distorted, resulting from the lack of energy



storage elements. This is a common issue for the MC topologies. Anyhow, Fig. 10 has verified the effectiveness of the proposed topology under input voltage disturbances.

Experimental results when the output current amplitude steps from 8 A to 16 A are presented in Fig. 11. It can be seen that the two topologies have quite close dynamic control performance at both the input and output side. Therefore, the proposed topology will not affect the dynamic performance. Note the  $i_{hA}$  will drop to zero if the output current is small. This is because of the power dissipation caused by the parasitic resistance of the filter inductor. Yet,  $i_{hA}$  maintains large value when the output current is still reduced, despite of the degradation of  $i_{hA}$  in the desired flat area.

### VI. CONCLUSIONS

With the proposed trapezoidal current injection technique, a novel TCI-MC topology is proposed. As demonstrated by simulation and experimental results, the proposed TCI-MC can reduce the transistor count, hardware complexity, current stress and the total transistor VA capacity. Therefore, it is a stronger competitor than the emerging 3CI-MC and the CMCs to the common B2B converter. For the proposed TCI-MC, optimizing the input filter parameters would be a meaningful work to decrease the adverse effect of the additional inductors.



Fig. 10 Experimental results of (a) 3CI-MC and (b) TCI-MC when the input voltages are disturbed by 5% fundamental negative sequence component, 5% 5th harmonic and 5% 7th harmonic

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Fig. 11 Experimental results of (a) 3CI-MC and (b) TCI-MC when the output current amplitude steps from 8 A to 16 A.

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