

# ANALOG CIRCUITS PLACEMENT: A CONSTRAINT DRIVEN METHODOLOGY

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## ABSTRACT

*This paper presents a new deterministic, relaxation based, placement methodology for analog circuits which takes into account electrical and topological constraints. The methodology is based on a three-steps process: initial constraints driven placement through convex optimisation, mechanical-like relaxation and compression. Experimental results are reported.*

## 1. INTRODUCTION

Since the layout process of analog integrated circuits has to consider the different physical aspects of analog modules, the tight constraints on the parasitics introduced by the physical network (electrical performances constraint) and the topological constraints, it is a difficult and a time consuming task. The heuristic methods proposed to solve this NP-complete, circuits placement problem can be classified into three main categories: *Artificial Intelligence based* ([Ben95] [Pat92]), *Deterministic* (e.g. [Ske72] [Han76] [Hil80] [Ake81] [Iso83] [Bla85]) and *Stochastic* methods ([Kra86]). All the proposed approaches, though achieving specific goals, are characterised by two major drawbacks: the algorithm's computational complexity and the quality of the placement obtained. Approaches aimed at identifying a high quality placement do not take into account the computational complexity of the algorithms and "vice versa". Moreover, many methods either are strongly dependent on the initial placement (connectionist and constructive) or can only produce partial solutions which need post-processing (global placement). Other techniques use simplified models to reduce the inherent number of degrees of freedom of the actual problem (i.e. force and pairwise interchange). Stochastic techniques, on the other hand, are much more independent of the initial solution, but are extremely time consuming.

The deterministic approach presented in this paper combines existing techniques opportunely modified to overcome the above mentioned drawbacks. It is composed by five independent phases: Preplacement, Relaxation, Adjustment, Compression and Folding.

The Preplacement phase is performed by using the Hall method [Hal70] (a quadratic convex optimization) generalized to the two-dimensional case and modified in order to introduce additional electrical and topological design constraints. The next step (Relaxation and Adjustment) consists of a mechanical-like relaxation process, in which continuous translation and rotation are allowed, made highly sensitive to the imposed constraints; moreover device mirroring is introduced to solve some simple cases of link-crossing. Since the minimization of the chosen objective function produces an optimal solution in term of critical connection lengths while area and aspect ratio are ignored, further operations (Compression and Folding) directed to the optimization of chip area have to be performed (force-directed compacting and folding).

The rest of this extended summary is organized as follows. Section II details the preplacement technique. The relaxation and the adjustment heuristics is then introduced in section III, while section IV introduces the post-processing phases in which compression and folding are performed in order to optimize the global area occupied. Section V briefly discusses some

implementation issues, showing the basic heuristics adopted. Finally, section VI provides the experimental results together with an overall evaluation of the algorithm.

## 2. PREPLACEMENT

In the preplacement phase, the  $N$  devices composing the network are simply represented in terms of dimensionless entities. The problem can be thus formalized as follows:

*Given  $N$  points in the two-dimensional space and a description of the connections existing among them, find their non-trivial disposition (the disposition is trivial when all points collapse in the origin of the space) which minimizes the overall interconnections weighted length.*

This quadratic, constrained, minimization problem is efficiently solved by the Hall method [Hal70] which has been extended to the two-dimensional case.

Let  $(x_i, y_i)$  be the coordinates of the  $i$ -th cell, and  $C_{ij}$  a normalized coefficient related to the criticality of the connection between the  $i$ -th and the  $j$ -th cell which is zero if the two cells are not directly linked. The problem consists of finding the set of coordinates non-trivial  $(x_i, y_i)$  which minimizes the objective function:

$$w = \frac{1}{2} \sum_{ij} [(x_i - x_j)^2 + (y_i - y_j)^2] \cdot C_{ij} \quad (1)$$

By denoting with  $X$  and  $Y$  the column vectors of the coordinates of the points to be placed, the cost function  $w$  can be rewritten as:

$$w = X'BX + Y'BY \quad (2)$$

where the modified connectivity matrix  $B$  is defined as:

$$B = D - C \text{ where } D_{ij} = \sum_k C_{kj}; D_{ij} = 0, i \neq j \quad (3)$$

In matrix form, the placement problem is that of determining two vectors  $X$  and  $Y$  such that the quadratic forms  $X'BX$  and  $Y'BY$ , with the constraints  $X'X=I$ ,  $Y'Y=I$  and  $X \neq Y$ , are minimized (constraints are introduced to avoid the trivial solution, in which all points are placed in the origin). This constrained minimization problem may be reformulated in terms of two independent eigensystems (Lagrange method), namely:

$$X(B - \lambda I) = 0; Y(B - \mu I) = 0 \quad (4)$$

The quadratic form  $w$  can thus be rewritten as:

$$w = X'BX + Y'BY = \lambda X'X + \mu Y'Y = \lambda + \mu \quad (5)$$

thereafter, the minimum of  $w$  equals the sum of the two smallest non-zero eigenvalues of  $B$ .

The proposed method, when applied to  $N$  points in a two-dimensional space, produces partial layouts that, as experimentations have shown, fully exploit the topological characteristics of the network unravelling interconnections by

minimizing the number of crossings (Fig 1a). Furthermore, the method tends to maintain axial and central symmetries (Fig 1b).

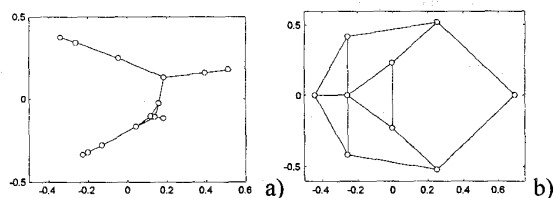


Figure 1. two examples of the application of the proposed method.

### 3 RELAXATION AND ADJUSTMENT

The second phase of the placement process consists of a mechanical-like relaxation where a realistic model is associated with each device. The method is based on the analogy between a system of cells and a physical system of masses and springs (Cell  $\equiv$  Rigid body; Link  $\equiv$  Spring; Criticality  $\equiv$  Elastic constant; Cell area  $\equiv$  Mass). Moreover, each rectangular cell is substituted by a circle, centered in the center of the cell and with a radius equal to one half of the diagonal (figure 2). According to the model and given an initial state, any system will relax (unconstrained) tending to a steady state condition.

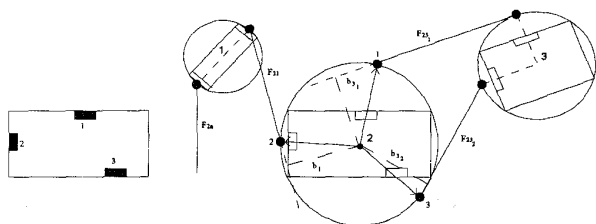


Figure 2: an example of cell, its model used for the relaxation step and the interaction between three devices.

A global evolution of the whole system corresponds to translations in direction of  $F_s$  and rotations in direction of  $M_s$  (the density  $\rho$  has been set to 1 without any loss of generality), therefore the evolution on the energy surface is pulled toward the opposite direction of the gradient so that the global energy  $E_{tot}$  decreases tending to reach a minimum of this function. The convergence of such a relaxation process is assured since it relies on the gradient-descent method.

When the relaxation step is accomplished, the system is constituted by cells whose orientation is not *manhattan*. In order to arrange all cells, which are preventively substituted by their rectangular description, with a side parallel to the chip border, a rearrangement has to be performed on the angular orientations of the cells. As intuition suggests, and experimentations confirm, the cells tend to be oriented toward a preferential direction, with a relatively small dispersion. Each cell is rotated according to the following algorithm

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if ( $|\Delta\theta|$  to make the cell parallel to the preferential direction  $\leq$ 
threshold)
{the cell is rotated immediately in that direction}
else
{the length of its links is evaluated for the two possible orientations
and the position minimizing this length is chosen}.

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This usually results in a good rearrangement of the layout though only a sub-optimal solution is guaranteed.

### 4. COMPRESSION AND FOLDING

Since the area occupied by physical cells is smaller than the outscribed circles, the layout, after adjustment, looks rather sparse. The compression takes place in two separate phases: first a *rough force-directed compaction* and then a *geometrical refinement*. The former is the same employed in the relaxation step.

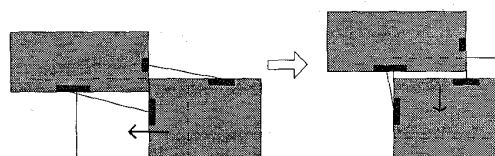


Figure 3: links exert a force directed upward on the empty rectangle; the cell position reached performing such a movement, though it could increase the link lengths, corresponds to a much more compact placement.

The latter consists of the following three steps (figure 3):

1. Reduction of the cell height (width) of a fixed amount.
2. Application of an horizontal (vertical) force to the new system.
3. If overlappings have occurred, the layout along the vertical (horizontal) axis is stretched.

This process is performed in both horizontal and vertical directions. The result of this operation improves the uniformity of the cell density on the chip, but inevitably modifies the aspect ratio of the layout: one dimension is increased while the other tends to decrease. So, a further refinement process, folding, is required.

The procedure, shown in figure 4, is computationally inexpensive and it has proven to be effective.

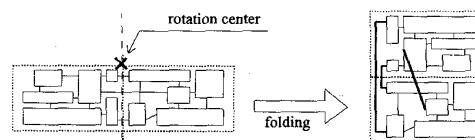


Figure 4.

The figure also shows that some of the links will be stretched, thus increasing the overall connection length. Particular attention has to be used for critical connections which, in such a phase, are constrained to be less than a given value (function of criticality).

## 5. IMPLEMENTATION

The methodology described has been implemented in C language on a *Sun Sparc station 2*. It has required some slight modification to the theoretical methodology, mainly due to its parallel nature. The global structure of CDPAC is outlined in the following figure:

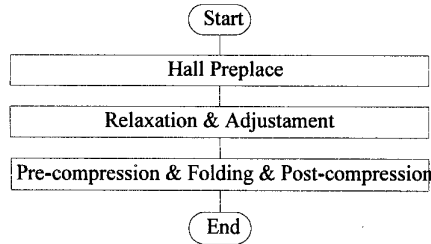


Figure 5.

The relaxation method described before shows two major drawbacks related to the differential and parallel nature of the problem, therefore some heuristics must be introduced.

Since the cells always tend toward the barycenter of the system and only one cell can be moved at a time, the adopted sorting criterion is to move first the cells closer to the barycenter of the system, avoiding the generation of spurious reactions.

The differential nature of the problem and the need to avoid both instability and slow convergence, require a careful choice of  $\Delta t$ , namely:

$$\begin{cases} \Delta t_0 = \Delta t_{MAX} \\ \Delta t_{n+1} = f(\Delta t_n) \end{cases} \quad (6)$$

The value of  $\Delta t_{MAX}$  is determined by imposing that the starting time must be small enough to produce a displacement not exceeding the actual layout dimension. Let  $N$  be the cell number and  $L_i$  the number of links of the  $i$ -th cell. The average force acting on a cell may be overestimated as:

$$F_{MAX} = \frac{|C|_{MAX} \cdot 2R \cdot \sum_j L_j}{N} = |C|_{MAX} \cdot 2R \cdot L_{AVE} \quad (7)$$

where  $|C|_{MAX}$  is the greatest elastic constant involved and  $L_{AVE}$  is the average number of links per cell. This force must produce a displacement smaller than a fixed fraction of the layout dimension  $R$ , when acting for a time  $\Delta t_{MAX}$ :

$$\Delta t_{MAX} < \sqrt{\frac{\alpha}{|C|_{MAX} \cdot L_{AVE}}} \quad \text{where } \alpha < 1 \quad (8)$$

The function (7) should shorten the time step  $\Delta t_n$  to achieve finer adjustments of the placement as the relaxation proceeds. An exponential variation of  $\Delta t_n$ , being  $\delta \approx 1$  the constant, has shown good convergence speed.

Experimentation has shown that during relaxation some configurations can occur that cannot be properly treated according to the model. The forces acting on every single cell,

equivalent to a resultant and a couple, produce both translations and rotations, but they will never be able to flip a cell around any axis (figure 6).

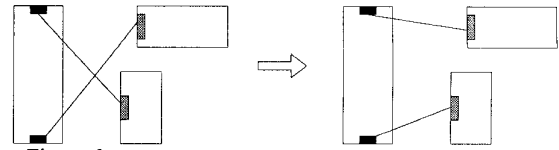


Figure 6.

Since these conditions are some what frequent, a routine has been added to find out these configurations and to solve them -if possible- performing a cell mirroring about a suitable axis.

The relaxation procedure is terminated when, for a given number of consecutive iterations, the movement of the system does not significantly improve the quality of the solution, namely when the total cells displacement is much smaller than the layout dimensions:

$$\sum_j \Delta s_j \leq \mu R \quad (9)$$

being  $\Delta s_j$  the displacement of the  $i$ -th cell, and  $\mu$  a constant (in the range of 0.001 - 0.01).

## 6. EXPERIMENTAL RESULTS

The program CDPAC has been applied on some analog integrated circuits, each characterized by a different number of components. Computational times required for the placement and the number of cells of each circuit are reported in table 1.

Circuit	Cells	Preplace	Relax.	Compress	Total
PUPPY	8	0.017	0.31	0.25	0.58
ATT	12	0.017	0.4	0.25	0.67
TRAMP	14	0.016	0.72	0.35	1.09
TWOTRA	24	0.033	1.48	0.56	2.07
AMP	25	0.033	2.51	0.46	3.00
AMP3STA	46	0.230	6.05	1.88	8.16
$\mu A791$ no pad	51	0.560	24.73	5.98	22.84
$\mu A791$	87	1.230	154.11	12.85	168.19

Table 1

The computational complexity of the algorithms implementing the proposed methodology has been theoretically analyzed and the results are reported in table 2 in which  $N$  indicates the number of the cells and  $M$  the number of iterations required for convergence; circuits with up to 90 cells have been placed and  $M$  has turned out to be less than  $45N$ .

Preplacement	$O(N^3)$
Relaxation	$O(M \cdot N^2)$
Adjustment	$O(N)$
Compression	$O(M \cdot N^2)$
Folding	$O(N)$
<b>Overall complexity</b>	<b><math>O(N^3)</math></b>

Table 2

Figure 7, which reports the approximation function (obtained with *Least Square Error*  $\{f(N, N^2, N^3)\}$ ) related to the computational times in table 2, confirms the theoretical analysis previously presented.

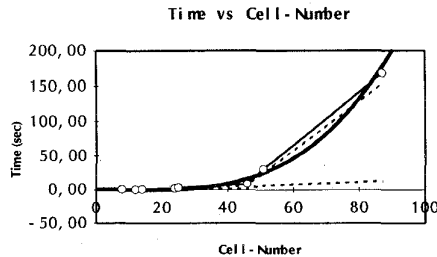


Figure 7.

To test the dependency of the algorithm upon user-definable parameters, further experiments have been carried out on 4 circuits. Since the central force has turned out to be the parameter mostly affecting the behaviour of the algorithm, each circuit has been placed by varying its value between 0 and 10 with a 0.5 step. The following table shows best- and worst-case experimental data.

Circuit	Job time	Covering ratio (%)	Aspect ratio	Connections length
PUPPY	1.0-2.6	33.2-53.8	1.0-1.8	724-998
AMP	4.3-7.3	46.4-75.3	1.2-1.9	3369-5493
AMP3STA	17.1-32.7	34.9-56.7	1.1-1.9	6443- 11925
$\mu$ A791	42.2-169.9	51.2-71.3	1.0-1.7	16177-23230

Table 3

Table 4 reports the Pearson correlation coefficients between different circuits characteristic. As the correlations show, the algorithm behaviour is satisfactory since the optimization of a generic parameter produces, statistically, the optimization of the others.

Variables	Correlation Coefficient	Error
Central Force - Aspect Ratio	-0.26	1.20%
Covering Ratio - Area	-0.81	0.01%
Aspect Ratio - Area	0.30	0.30%
Aspect Ratio - Connections length	-0.42	0.01%

Table 4

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