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Characterization of Seamless CdTe Photon Counting X-ray Detector

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***Abstract*—Spectrally selective X-ray imaging provides improved material and tissue discrimination in comparison to state-of-art dual energy technologies that are commonly used in medical, industrial, and security applications. Cadmium Telluride (CdTe) and Cadmium Zinc Telluride (CdZnTe) based line scanners and small size two-dimensional X-ray sensors are emerging to the market, but the need for large scale panels is axiomatic. In this study, a seamless CdTe tile was developed that enables the implementation of large-sized, energy selective X-ray detector panels. The developed tile consists of a 64 × 64 pixel array (with 150 µm pitch) with a necessary substrate, ASIC, and CdTe crystal. The performance of the constructed seamless tile was characterized by focusing on spectral resolution and stability. In addition, a simple pixel trimming method that automates the equalization of each energy selective pixel was developed and analyzed.**

The obtained results suggest that the proposed concept of seamless (tileable) detector structures is a feasible approach to scale up panel sizes. The seamless tile shows comparable spectral resolution and stability performance with commercial CdTe sensors. The effect of tile to tile variation, the realization of a large-scale panel, as well as the charge sharing performance, were left out of the scope and are to be studied in the next phase.

***Index Terms*—Photon counting detector, CdTe, ASIC, material discrimination, direct conversion, multi-energy, X-ray imaging.**

I. Introduction

CADMIUM Telluride and Cadmium Zinc Telluride (Cd(Zn)Te) are two of the most promising materials for the energy selective direct conversion X-ray imaging sensors [1]. Energy selective (spectroscopic) imaging devices are needed for material and tissue discrimination in industrial, security, and medical applications [2]. Both line scanners and two-dimensional direct conversion imaging devices (panels) show benefits such as high spatial resolution and signal to noise ratio over the conventional (single and dual-energy) X-ray imaging systems [3] [4]. The X-ray detector technology has undergone many improvements over the years and the direct conversion technology is now considered mature enough to be exploited for commercial applications [5].

A typical CdTe sensor consists of a CdTe-crystal or crystals, an ASIC and a data acquisition board. Shortly, an X-ray photon that is absorbed by the detector element, generates a charge cloud that is proportional to the photon energy. This charge cloud travels to the respective electrodes (bias and pixel electrode), if an electrical field is applied through bias voltage. The charge cloud is collected by the ASIC through the pixels. The ASIC has front-end electronics for each pixel that consists of digital and analog parts. The front-end electronics counts the absorbed photons (also called hits) within the pixel if the energy is higher than the defined threshold value. Since the generated current is proportional to the hit energy, the photon energy can be determined. A data acquisition board is used for the backend electronics, to read the data from the ASIC and to control the ASIC.

Many of direct conversion imaging devices are 3-side buttable [6] [7]. Hence, one edge of the ASIC has a dedicated area for wire-bond I/O pads, causing significant dead space to that side of the device. This limits the possibilities for scaling up the imaging device to 2 rows. To build large detector panels with wire-bonding technology requires to use large size CdTe crystals and use different sized pixels at the wire-bond edge. This leads to inhomogeneous images and causes complications during image processing, which are particularly undesired in medical applications. Furthermore, the growth of large-sized single CdTe or CdZnTe crystals is a demanding and time-consuming process, which increases the manufacturing costs significantly. Wafer sizes with 100 mm in diameter are commonly available, but crystals larger than 20 mm × 20 mm in size are still expensive [8], causing the crystal-ASIC package (also called hybrids) to be one of the most expensive parts of such an imaging device. Seamless hybrid detector technologies have been developed for larger crystals sizes [9] [10] and are typically done by using Through Silicon Via (TSV) technology

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to replace the wire bond I/Os of 3-side buttable devices. Fig. 1 shows schematic cross-sectional drawings of three different approaches. A wire bonded ASIC (A) is typically used by MediPix products and a typical structure of a CdTe sensor with TSV technology (B), as for example introduced by M. Tamaki *et al.* [11]. It is also worth mentioning that both the wire bonded and the TSV approach fix the ASIC-CdTe package firmly to the data acquisition board and preventing therefore replacement of malfunctioning packages.

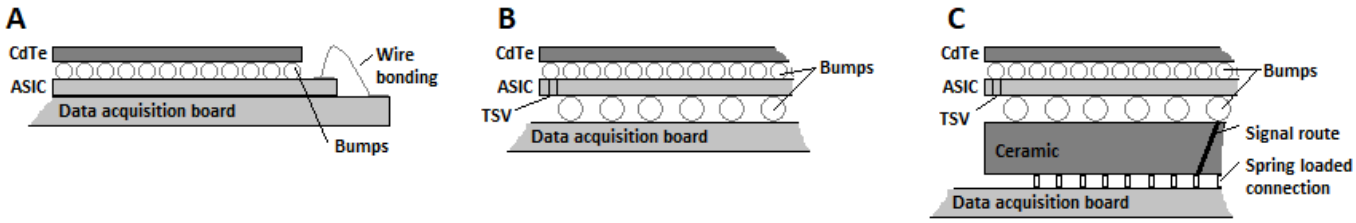

Figure 1: A Wire bonded three edge tileable structure, B. A TSV-based, four edge tileable structure, C. In house made tile sensor with ceramic and spring-loaded connection to the data acquisition board. Please note that A and B are firmly fixed to data acquisition board and are not replaceable.

In this study a scalable structure of a tiled hybrid sensor was developed. Each (sensor) tile is built on a ceramic substrate and can be fixed to the data acquisition board with spring-loaded connectors. This enables the replacement of individual sensor tiles (see Fig. 1, C). By adding multiple tiles to the same detector panel, a large and seamless panel with lesser mechanical limitations can be implemented and at reduced costs because malfunctioning tiles can be replaced. This work focuses on the investigation of ASIC trimming, dead time, energy-linearity, -resolution, and -stability of a single tile, but without the charge sharing corrections. This is referred to as single pixel mode in this study. The results from this study are to be used as a baseline for further publications.

II. In house made hybrid tile

In this study, seamless CdTe hybrid tiles consisting of 64 × 64 pixels were produced. Each tile has its own CdTe crystal, ASIC and ceramic substrate as shown in Fig. 1. C. Fig 2 shows the top and bottom view of an assembled tile. The chosen approach does not limit the size of the detector panel, as no side requires wire-bonds. However, the active area is restricted by the data acquisition board, which is designed for a certain amount of tiles.

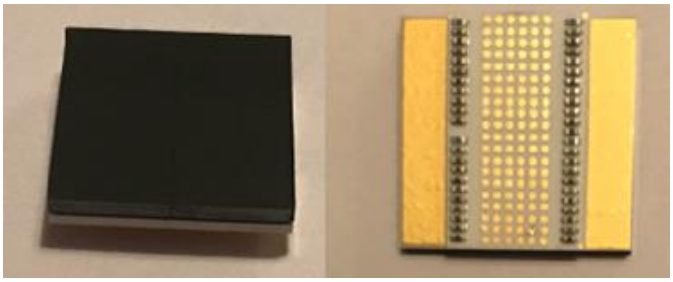

Figure 2: In house made hybrid tile. Left: tile from bias side, the CdTe crystal is visible. Right: tile from the readout side of the ceramic.

A. CdTe crystal

The used CdTe crystals are provided by Acrorad with 64 × 64 Schottky-type electrodes. Pixels have a squared metallization at half of the pixel pitch (150 µm), with round contact openings. External dimensions of the crystal are $9.675 \times 9.675\ mm^2 \pm 0.02$ mm. The crystal thickness is 1.000 mm +/- 0.02 mm. A Schottky type Aluminum contact is used on the pixel side of the crystal and a Platinum contact on the bias side.

B. ASIC

The ASIC called XPC4k (X-ray Photon Counting 4k) is designed in AGH University of Science and Technology, Cracow, Poland. The core of the integrated circuit fabricated in CMOS 180 nm technology is a matrix of 64 × 64 pixels with a pitch of 150 µm. Each readout pixel operates in the single photon counting mode and allows the processing of electron signals generated in a CdTe detector. Fig. 3a shows the simplified scheme of a single pixel. The pixel contains Charge Sensitive Amplifier (CSA), shaper, four independent operating discriminators, and four 12-bits counters. The CSA integrates the current signal from a detector on the feedback capacitance C_{fcsa}, while the active resistive feedback R_{fcsa} provides the discharge of feedback capacitance and compensation of the detector leakage current. The shaper stage filters the CSA output signal to improve the signal to noise ratio and adds more gain in the signal processing chain. The shaper gain is determined by the ratio of the effective capacitance C_s at the shaper input to the shaper feedback capacitance C_{sf}. The possibility of control capacitance C_s allows trimming shaper gain. Further signal processing at the shaper output is performed by four discriminators operating with four independent threshold levels VT0 – VT3. The properly set discriminator threshold cuts the noise and counts only the X-ray hits with an amplitude higher than a given threshold. The discriminator thresholds are set globally for all the pixels in the matrix and the thresholds can be adjusted depending on the applied X-ray energy and the application requirements. The known problem of a single photon counting detector is the offset spread (called also threshold dispersion) from pixel to pixel [12]. To minimize offset spread at the discriminator inputs, there are local offset correction blocks (DACtrim) controlled by 6-bits and working for each discriminator in each pixel independently. The control and readout of the 64 × 64 pixel matrix require the periphery circuits like bias DACs, pixel matrix control block, global shift register, I/O control logic, LVDS drivers, and receivers. All these peripheries blocks are distributed partially in the pixels

and partially in the area between the pixels (see Fig. 3b). The through silicon via (TSV) technology allows to bias and control the ASIC from the bottom side pads and keep total ASIC area of 9.6 × 9.6 mm². The ASIC is designed to operate in the temperature range from -10 degrees of Celsius to +50 degrees of Celsius with the power consumption at room temperature of 470 mW. Signals from the ASIC to the data acquisition board are routed through the ceramic substrate. Importantly, the ceramic surface also conducts the heat away from the ASIC.

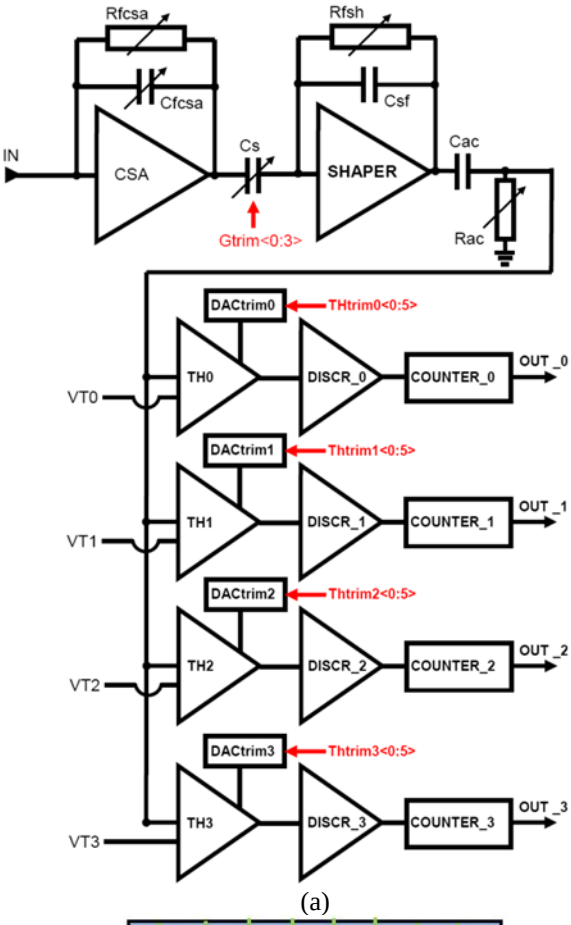

Fig. 3. XPC4k ASIC: a) block diagram of a single pixel, b) simplified view of chip layout with periphery placement(green).

C. Tile test bench and experimental setup

The in house-made detector and test system consist of a tile test socket (A), data acquisition board (B), and a temperature control unit (C) as shown in Fig. 4.

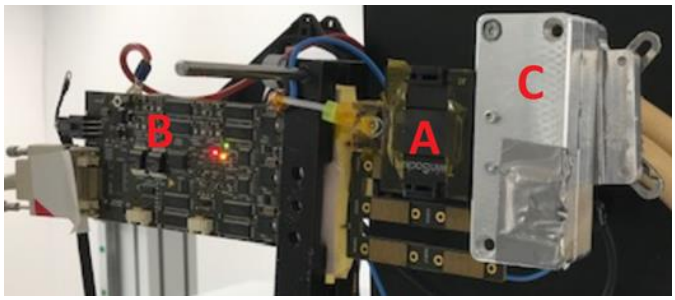

Figure 4: Tile test interface, A) Tile test socket, B) Data acquisition board, C) Temperature control unit.

The tile test socket is used to ensure mechanical and electrical connection to the single tile. It further contributes to the biasing and temperature controlling functions. The lid of the tile test socket presses down and locks tile to the data acquisition board, by the use of spring loaded connections. The bias voltage to the CdTe is conducted via the lid of the socket.

The data acquisition board controls the ASIC, performs the data collection from the ASIC, and further sends the data via camera link [13] to the control PC. In addition, the data acquisition board contains the necessary voltage regulators to provide electrical power to the ASIC.

The temperature control unit is a Julabo F25-MA Refrigerated/ Heating Circulator that is connected to the socket, to keep ASIC temperature stable at a set value. The temperature sensor is located at the bottom surface of the ceramic substrate and measured to be 30.5 degrees of Celsius. The utilized data acquisition board supports up to 8 × 8 tiles, which will be evaluated in a subsequent study. The needed control, calibration, and interface systems were developed and implemented into an in-house software with a user interface (UI).

A Keithley 2410C source meter was used to provide the bias voltage for the detector tile. All the measurements were performed in a dedicated X-ray test room with an MXRP-160C X-ray tube source. Technical details for the X-ray tube are listed in Table I. The spectral measurements were performed with X-ray fluorescence targets and an Am-241 radioactive source of 3.7 GBq activity. The principle of the dead time and X-ray fluorescence setups are presented in Fig. 5.

TABLE I
CHARACTERISTICS OF X-RAY SYSTEM

Parameter	Details
Target material	W
Focal spot acc. EN 12543	l=0.4mm, w=4.0mm
Inherent filtration	0.5 mm Ti + 2.0 mm, H2O + 2.0 mm Al
External filtration	Not applicable
Radiation coverage	360 degrees x 40 degrees
Nominal tube voltage	160 kVp
Max. tube current at 160 kVp	6.2 mA

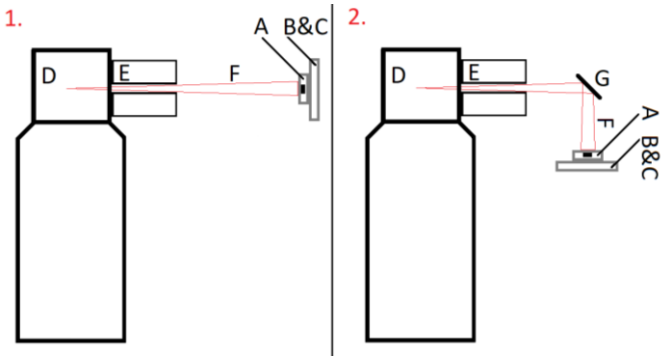

Figure 5: 1. Dead time test setup. 2. XRF test setup. A) tile and test socket, B & C) test interface and cooling block. D) X-ray tube, E) Collimator F) red line indicates the X-ray beam and G) XRF target.

The ASIC trimming and image processes algorithms were developed using MATLAB (R2016B with image processing toolbox) [14] as well as Minitab for the statistical analyses [15].

III. Methods

An ASIC trimming method is needed to unify the response of all pixels and minimize the pixel to pixel variations, which are caused by ASIC nonidealities. After trimming, the evaluation of flux dependency (dead time), energy resolution, energy linearity, and energy stability were investigated.

All spectra that were collected for this study, were calculated from the integral data set (also called integral spectra) of each measurement. An example is presented in Chapter IV. D. Energy resolution, Fig. 17. The integral dataset is obtained by scanning the thresholds of each pixel, in which a discriminator is counting all the pulses that are above a defined threshold value. If the threshold value is then iteratively incremented and plotted versus the threshold value, then an integral pulse height spectrum can be collected. Finally, the differential spectrum is obtained by subtracting the counts of two adjacent thresholds from the integral spectrum and plotting the results versus the threshold value [7] [12].

The detector bias was set to -500 V_{dc} and 1000 ms integration time, for most of the experiments. The tile temperature was kept at 30.5 degrees of Celsius. This temperature was optimized for stable tile temperature while avoiding condensation from ambient air at the socket surface. All the deviations from these conditions are described separately in the corresponding test descriptions.

A. ASIC trimming

An important calibration step for such devices is called ASIC (or pixel) trimming, which ensures that all pixels behave in the same way, despite their individual nonidealities. The influence of local material nonidealities is increasing with decreasing pixel sizes, causing crosstalk and noise floor fluctuation. ASIC trimming is used to unify these variations in the pixel response. The in-house designed ASICs have global and local trimming parameters for each pixel's analog front-end. The global trimming parameters are the same for all pixels on the same ASIC and local trimming parameters can be defined separately for each pixel. In this study, the focus is on a single tile and therefore local trimming parameters, threshold trimming (THtrim, 6-bit) and gain trimming (Gtrim, 4-bit), are the most critical parameters to be equalized.

The pixel offset noise is approximated to follow a normal distribution, as shown in Fig. 6. The pixel threshold values for the noise peak are trimmed so that variation of peak locations is minimized. Offset trimming can be done by digital to analog converter (DACtrim) local trimming variable, which is a 6-bit parameter. The trimming procedure takes a relatively long time, especially since it needs to be performed for all pixels separately. Therefore, algorithms have been developed to accelerate the trimming procedure [16] [17].

Several methods can be used to perform the gain trimming [18] [19]. In this work X-ray fluorescence (XRF) method is used because it is cost-effective, the fluorescence peaks can easily be defined, and it works for a wide range of calibration peaks. The trimming itself is based on optimizing the threshold value for a known X-ray fluorescence peak [20] [21].

To avoid disadvantageous polarization effects caused by the prolonged biasing time [22], test times were kept below 600 seconds. Polarization was briefly tested after ASIC trimming with two scans. The first ranging from 0 - 300 seconds and the second ranging from 300 – 600 seconds, each using a Tungsten target. The integration time was reduced to 500 ms to keep the scanning time short enough. All other parameters remain the same.

The XRF experiments used a setup as depicted in Fig. 5.2., with a distance from the focal spot to the target of 120 mm and from the target to CdTe of 50 mm. A tungsten target with Kα at 59.3 keV was selected in this work, which is close to Am-241 photon peak energy of 59.5 keV.

B. Dead time

For medical applications detector operating under high flux conditions are very important. Thus, the detector's dead time is a critical performance factor. Dead time is caused by the nonideal signal processing time of a real detector. The hit of charges generates the pulses, for which processing takes a finite amount of time. If another hit occurs within the same conversion time, it will increase the amplitude of the first counted pulse, causing the so-called pileup effect [23]. This effect distorts the detected energy response. In addition, a flux dependent count loss occurs, if several photons hit within the same process period. The higher the X-ray flux is, the higher the count loss will be [24]. The XPC4k ASIC was designed based on the paralyzable detector model [25] and the output count rate, R_o follows equation (1) as a function of the X-ray tube current I

$$R_o = I \cdot a \cdot e^{-Ib}, \quad (1)$$

where a and b are constants. In ideal case b is equal to 0 and equation (1) can be written as

$$R_i = R_o = I \cdot a, \quad (2)$$

where R_i is the input count rate. Thus, the input count rate can be defined as a function of the output count rate

$$R_o = R_i e^{-R_i \tau}, \quad (3)$$

where dead time (τ) is equal to b/a. The dead time and maximum count rate at 10% dead time loss can be calculated from linear fitting

$$-\ln\left(\frac{R_o}{a \cdot I}\right) = a \cdot I \cdot \tau. \quad (4)$$

The detector count rate performance can be characterized by a 10% dead time loss ratio (DLR) [25].

Deadtime measurements were performed using a 70 kVp X-ray tube setting and 100 mm distance from the X-ray focal spot to the surface of the crystal (see Fig. 4.1.). The tube current was variated from 1 mA to 20 mA in steps of 1 mA. The detector's integration time was set to 1000 ms and the bias voltage was set to -500 V_{dc}.

C. Energy linearity

The energy nonlinearity of a detector tile is mainly caused by the ASIC's analog front-end electronics, limited power supply voltage and a trade-off between gain, noise, and power consumption in a single readout pixel [26]. The energy non-linearity can be measured using the same methods as during the gain trimming phase. In this study, the XRF method was used for trimming. In Table II the used fluorescence targets and corresponding K_α-peaks are presented. The used targets were selected to be within the detector's energy range. The threshold value for K_α- and K_β-peaks are defined and linear fitting is performed to derive the energy-threshold curve.

The XRF experiments were performed with 160 kVp and 6.25 mA X-ray tube settings for all targets. Other settings were as for case 2 in Fig. 5.2.

TABLE II
K_α ENERGIES FOR XRF TARGETS

Element	K_α (keV)	K_β (keV)
Molybdenum	17.48	19.61
Silver	22.16	24.94
Gadolinium	42.98	48.72
Tungsten	59.31	67.23
Lead	74.96	84.92

D. Energy resolution

The energy resolution of the detector is affected by the charge sharing effect between pixels. Charge sharing increases when the pixel size decreases. However, the influence of charge sharing and the correction thereof is left for further studies. Furthermore, there are different methods for charge sharing corrections [27-29]. The energy resolution can be tested utilizing synchrotron, X-ray fluorescence, or monochromatic radioactive sources. In this study, an Am-241 was used. Since the activity of the available source was low that the integration time had to be increased. Furthermore, filtering and averaging over groups of pixels was required. In this study Savitzky–Golay filter was used to reduce the noise from the recorded spectrum [30]. In each spectrum, peak location, peak to valley ratio, full width at half maximum (FWHM), and energy resolution are determined. The distance from the source to the detector crystal was about 20 mm.

E. Energy stability

Detectors stability plays an important role in commercial applications. End users should not see a drifting of the photon peak if the detector is properly calibrated. Preferably, the energy peak should stay at the same position within the defined environmental operating conditions.

Typically, the stability issues are caused by temperature and biasing voltage variations. With Schottky type detectors, the energy resolution increases when the temperature decreases. Most of the ASICs are optimized so that temperature effects are taken into account in the design phase and being thus negligible in comparison with the temperature effects coming from the Cd(Zn)Te crystal. The instability on the crystal level is caused by the temperature dependency of charge transport [31]. Preferably, the crystal temperature should be as low as possible to ensure high stability [32]. However, a compromise between crystal and ASIC operation temperature has to be found. The energy stability of the detector was studied by varying the bias voltage and temperature. Both tests were performed using the Tungsten XRF target. The used bias voltages were set to -450, -490, -500, -510 and, -550 V_{dc} and were chosen based on the operational voltage, for which the detector was designed. Increasing the bias voltage and decreasing the temperature improves the spectral resolution of the detector (peak to valley ratio and full width from maximum) [33]. Temperature dependencies were studied under the same conditions as the bias voltage. A constant bias voltage (-500 V_{dc}) and the system temperatures were varied between 31.5, 32.5, and 35.5 degrees Celsius. A CdTe detector under operation is subject to the polarization effect. This effect depends on the amplitude of bias voltage, but also the temperature and total time that bias applied [34]-[36]. A brief study of the polarization effect is presented in section IV. A.

IV. RESULTS

A. ASIC trimming

In this study the following offset trimming algorithm was developed:

1.) Perform threshold scan from 0 LSB to 511 LSB for each THtrim value from 0 LSB to 63 LSB.
2.) Find the threshold value where the peak is located for each pixel and for each THtrim value.
3.) Calculate the THtrim versus peak location curve for each pixel.
4.) Define the target threshold and define the closest THtrim value from the curve.
5.) Save the THtrim value of each pixel to a configuration file.

Taking into account the width of the offset peak (Fig. 6.) and the variation of peak positions after offset scanning, it is possible to define the lowest useful threshold value. For the detector developed for this work, the offset peak's FWHM is 2-3 last significant bits (LSB).

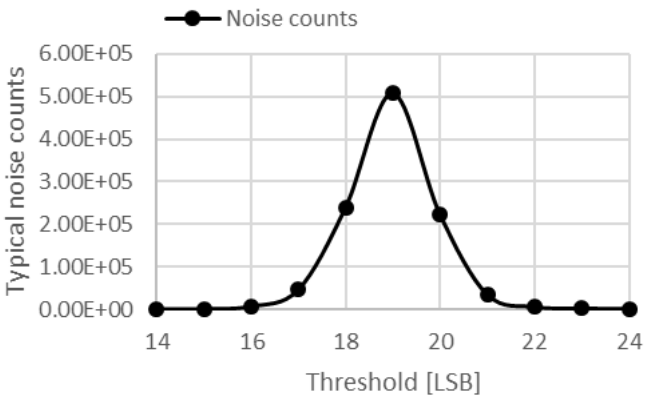

Figure 6: Typical offset noise counts.

A third-degree polynomial curve fit for the THtrim-threshold curve measured with 100 ms integration time was used in this study to fit the measured thresholds. The target threshold was set to be 19 a.u. Fig. 7. shows the variation of offset peak location before and after the trimming. The ASIC trimming method allowed to reduce the standard deviation of peak positions from 4.7 to 0.43 LSB.

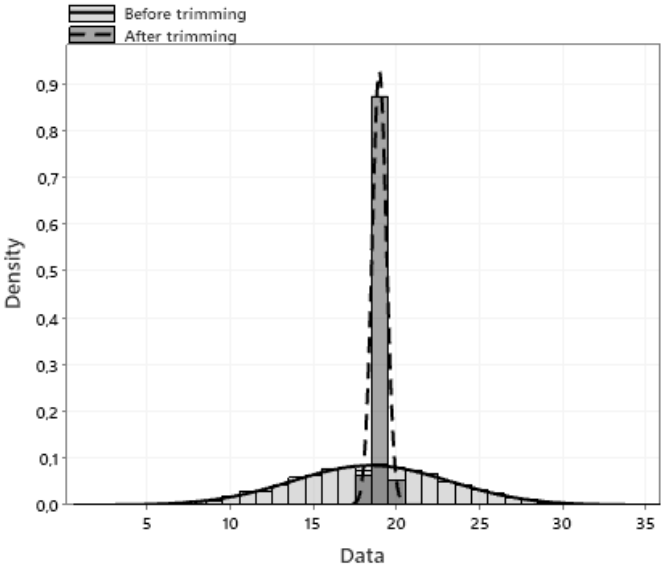

Figure 7: Pixel offset noise peak position (Threshold LSB) before and after trimming, of one ASIC with 64 × 64 pixels.

Gain trimming was performed in a similar way to the offset trimming algorithm, where the Gtrim instead of THtrim value was optimized. An example XRF signal that was measured is depicted in Fig. 8. All counts are normalized to the peak heights.

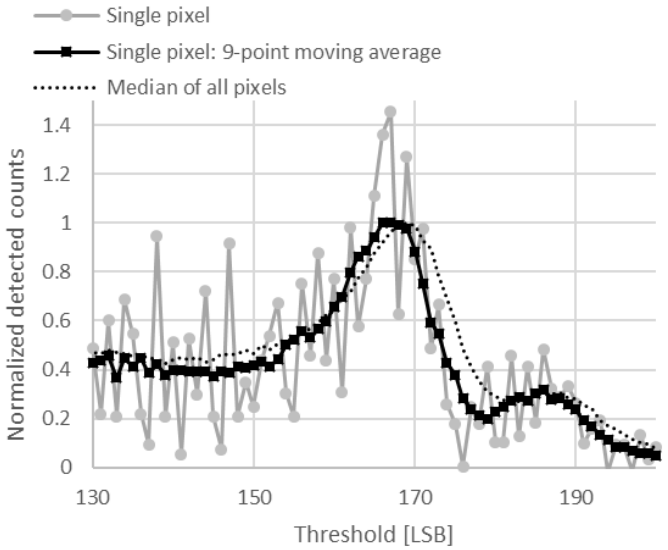

Figure 8: Tungsten Kα peak for single pixel and median of all pixels.

The median of the peak location for each Gtrim value is plotted in Fig. 9. The repetitive pattern in Fig. 9 is caused by the additional parasitics capacitance of the switches at the shaper input (see Fig. 3a).

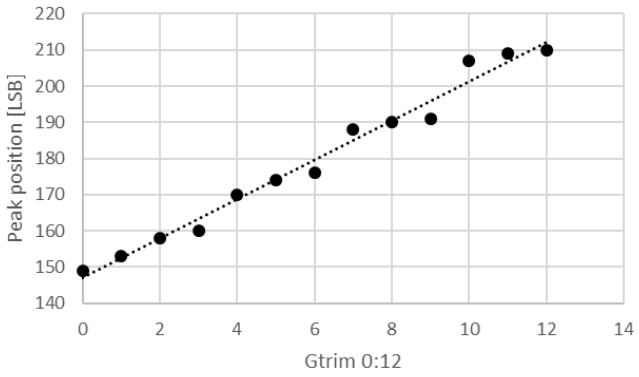

Figure 9: Gtrim versus peak position [LSB].

The linear fit of the peak position graph (Fig. 9) shows that the minimum resolution for trimming is approximately 4 LSB. This means that increasing the Gtrim value by 1 changes the peak location by +4 LSB. The fitted line follows the equation

$$\text{Peak} = 5.434 * \text{Gtrim} + 147.010, \quad (5)$$

where Peak is peak position [LSB] with given gain trimming value (Gtrim). The correlation to the fitted line is $R^2 = 0.9809$. A nominal target value was selected so that most of the pixels are trimmable to the target threshold value. These optimizations result in a threshold value of 175 (Fig. 10) and a median value for Gtrim of 5.

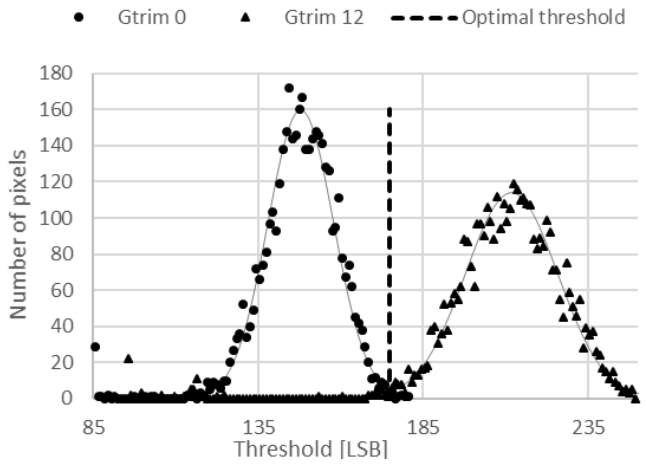

Figure 10: Gain trimming: Threshold value optimization.

To illustrate the effect of trimming, the peak position variation before trimming and after trimming is presented in Fig. 11. The standard deviation before and after trimming are 11.25 and 2.34 LSB, respectively.

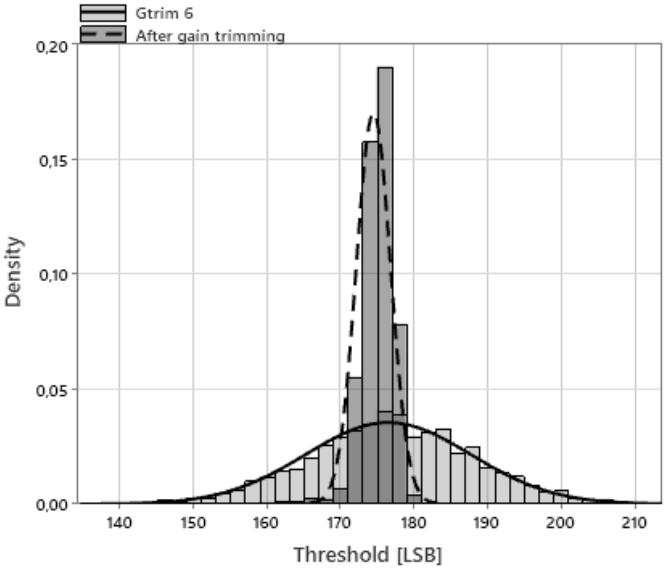

Figure 11: Pixel XRF peak position (Threshold LSB) before and after trimming of the Gtrim parameter, one ASIC.

Figure 12 shows the spectra of 2 different bias voltages, with -200 V_{dc} and -500 V_{dc}, respectively. A threshold scan was acquired from 150 LSB to 210 LSB during a period of 0 - 300 seconds and 300 - 600 seconds. Bias voltage and X-ray radiation were continuously operational during the full 10 minutes operation. In the period of 300 – 600 seconds and -200 V_{dc}, the Tungsten peak has clearly drifted to lower thresholds and its intensity has decreased. At -500 V_{dc} location of the Tungsten peak did not change in the period of 300 – 600 seconds but lost approximately 5% of its intensity.

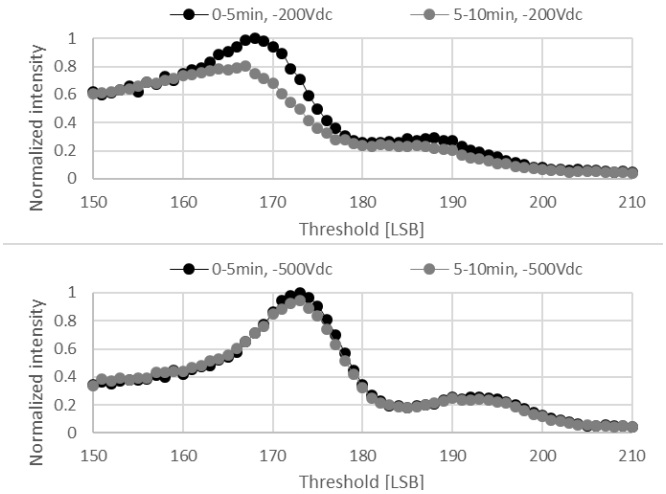

Figure 12. Comparison of energy spectra with -200 V_{dc} and -500 V_{dc} bias measured between 0 - 300 seconds and 300 - 600 seconds, after the bias was turned on.

B. Dead time

Fig. 13 shows measured input count rate vs. output count rate. In the single pixel mode, the dead time was measured to be 188 ns and the count rate at 10% DLR was calculated to be 560 kcnt/ s/ pixel, based on Eq. (4). The correlation to the exponential fitted line was $R^2 = 0.9999$.

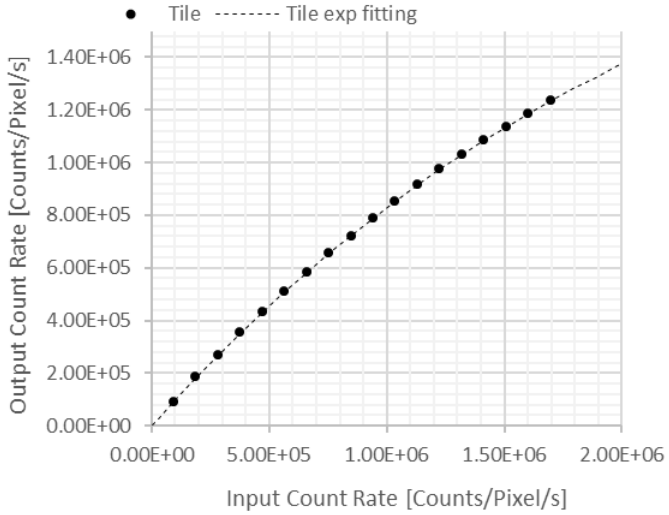

Figure 13: Measured dead time and fit at 70 kVp and 1000ms integration time.

C. Energy linearity

The energy linearity was made after ASIC trimming using the XRF method and selected XRF targets with conditions described in section III. To reduce noise, a region of interest (ROI) of 10 × 10 pixels at nine different locations of the ASIC was used, see Fig. 14.

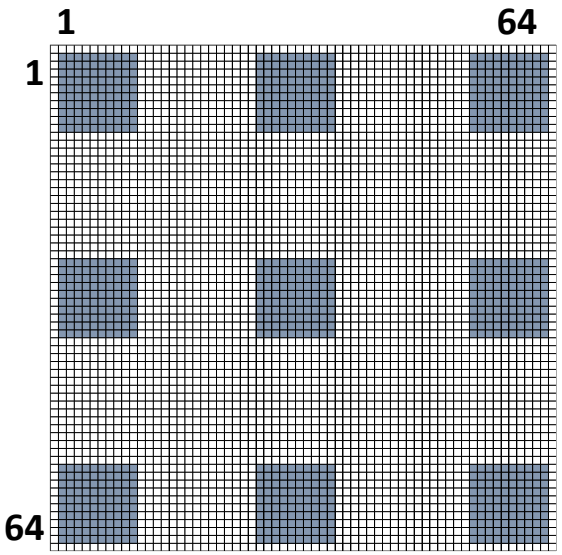

Figure 14: Locations of 10x10 ROI's within the 64 × 64 array.

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Within each ROI, the median peak value of all 10 × 10 pixels (in LSB) was used for linear fitting.

The K_α -peak can be detected clearly from all targets, the K_β can also be detected from Pb, W, and Gd. However, the K_β -peak from Mo and Ag are only visible as a shoulder, because these peaks are superimposed with the K_α peaks of the respective targets. The Mo and Ag K_β -peaks are therefore not considered further in this work. In addition, the $K\alpha$ and $K\beta$ -peaks from the Cd fluorescence (23.2keV, 5% intensity; 26.1keV, 1.5% intensity) also and $K\alpha$ and $K\beta$ -peaks from the Te fluorescence (27.5keV, 1.5% intensity; 31.0keV, 0.4% intensity) are part of the spectra. These peaks however are consolidated with the Ag $K\alpha$ and $K\beta$ -peaks, due to their similar energies and small intensities [37] as illustrated in Fig. 15. This figure also shows the normalized peaks for used XRF targets, the peak location vs. peak energy A linear fit (Equation 6) of the data of Fig. 15 can be found in Fig. 16.

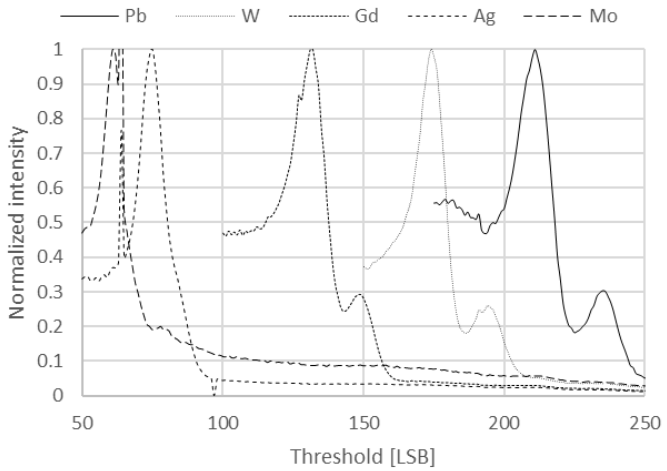

Figure 15: Normalized K_α-peaks for Pb, W, Gd, Ag, and Mo. All XRF peaks of Pb, W, and Gd can clearly be separated.

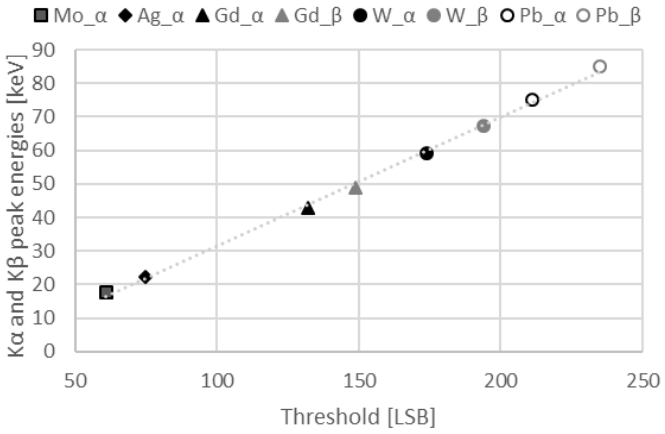

Figure 16: K_α- and K_β -peaks for Mo, Ag, Gd, W, and Pb targets.

The fitted line follows the equation

$$E = 0.386 * thd - 7.236, \quad (6)$$

where E is energy [keV], thd is threshold variable. The offset gain from the fitted line is 0.386. The maximum deviation from the fitted line is 1.49 keV at the energy of the Gd_β peak. Peak correlation to the fitted line was $R^2 = 0.9981$.

D. Energy resolution

Energy resolution determination was made using Am-241 source with the conditions described in section III. The number of counts at a single pixel level was too low and thus the corresponding ROIs of the energy linearity measurements (see Figure 14) were used. The results were furthermore averaged over 10 repetitions of the measurements.

Fig. 17 shows the integral spectrum with error bars and differential spectrum with Gaussian fit for Am-241 photo peak in the same plot. The FWHM was estimated from the Gaussian fit to be 9.02 LSB, which is equivalent to 3.48keV and was obtained through equation (6). Thus, the corresponding energy resolution at the Am-241 photopeak is 5.84%. The peak to valley ratio was approximately 4 +/- 0.43.

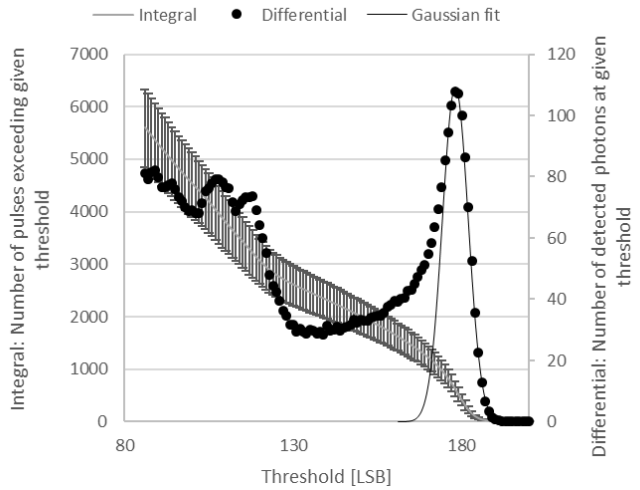

Figure 17: Am-241 sweep: Peak spectrum differential curve and integral curve with error margins.

E. Energy stability

Energy stability was studied by varying the bias voltage and temperature. The region of interest remained the same as is described in Fig. 14. Both tests were made using the Tungsten XRF target. Fig. 18, shows the XRF peaks as a function of the threshold with different bias voltages. The measured peak positions and peak to valley ratios for different biasing voltages are summarized in Table III.

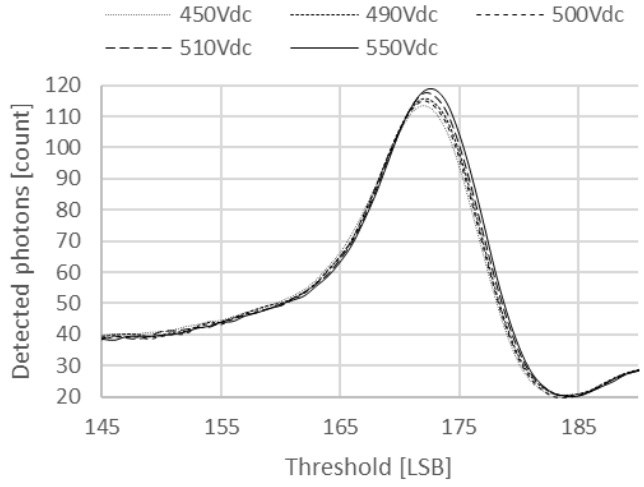

Figure 18: Tungsten K_α-peak versus bias dependency. A comparably little variation can be observed with moderate temperature changes.

TABLE III
BIAS VS. TUNGSTEN K_α -PEAK

Bias voltage [V_{dc}]	Peak position [LSB]	Peak to valley
-450	172 ± 0.5	2.83 ± 0.25
-490	172 ± 0.5	2.89 ± 0.25
-500	172 ± 0.5	2.88 ± 0.40
-510	172 ± 0.5	2.94 ± 0.40
-550	173 ± 0.5	2.96 ± 0.35

XRF peaks for different temperatures can be seen in Fig. 19 and the corresponding peak position and peak to valley ratios are summarized in Table IV. Peak locations were observed to remain at the same location, indicating that there is no significant energy drift caused by temperature fluctuation.

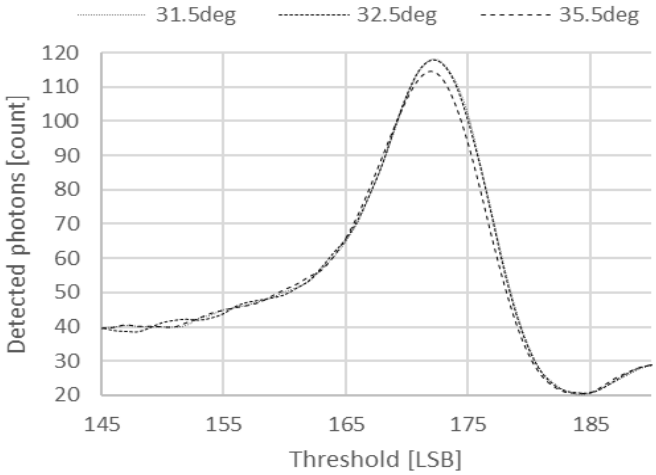

Figure 19: Tungsten K_α-peak versus temperature dependency. A comparably little variation can be observed with moderate temperature changes.

TABLE IV
TEMPERATURE VS. TUNGSTEN K_α -PEAK

Temperature [ºC]	Peak position [LSB]	Peak to valley
31.5	172 ± 0.5	2.95 ± 0.25
32.5	172 ± 0.5	2.95 ± 0.25
35.5	172 ± 0.5	2.87 ± 0.30

V. DISCUSSION

Results are very consistent compared to reference designs such as Pixirad Pixie III [38] and Medipix [24]. The offset trimming method is close to the ideal case where the variation is ±0.5 LSB. In reality, this will be increased because of the non-ideal pixel response and additional pixels that show decreased response for some reason (e.g. larger deviation of the bias voltage and temperature from measured values). The limiting factor for the accuracy of the gain trimming is to get enough counts to every pixel so that the XRF-peak is clearly visible in the spectra. This can be achieved with longer integration times. However, it has to be optimized in order to avoid disturbing polarization and temperature effects. Also, an iterative trimming algorithm might help for future studies. However, the developed trimming algorithms provided adequate results for this study.

The measured dead time was 188ns. As a reference, the equivalent value for Medipix is between 400 - 690 ns and Pixirad Pixie III 300 ns in single pixel mode.

No nonlinear behavior could be observed within the range of XRF target energies. The peak positions follow well the fitted line curve (Fig. 16), which indicates a predictable linear response of the final detector. For a comparison IBEX chip at DECTRIS with Acrorad Co. Ltd CdTe crystal shows a differential nonlinearity of 3.41 keV, but with a wider range of test points that ranged from 10 keV up to 150 keV [19]. Measured correlation, $R^2 = 0.9981$, is close to the Medipix3RX, which was measured to be $R^2 = 0.9972$ with a range of 17.48 keV up to 74.96 keV [39].

The energy resolution of the tested detector tile was determined to be < 3.5keV FWHM with a peak to valley ratio of 4 ± 0.43. Using a pulsed bias operation mode would allow slight improvement of the energy resolution and peak to valley ratio, compared to the measured values. For comparison, IBEX ASIC Monte-Carlo simulations and measurements predicted a peak to valley ratio of approximately 5 and 2.25 +/- 0.25 keV FWHM for 150 µm pixel size and at 60 keV and 500 V_{dc} bias [40]. Deviations from IBEX ASIC simulations might originate from the design differences of the gain, biasing, or trimming algorithms. Furthermore, synchrotron radiation was used for the IBEX ASIC measurements and not the full spectrum of a Tungsten X-Ray tube. The energy resolution of the MediPix3 ASIC was measured to be approximately 2 keV [41].

Changes of the bias voltage (500 +/- 50 V_{dc}) did not cause any significant peak drift that might cause unwanted distortions for spectrally resolved images. The polarization effect was found to be small at -500 V_{dc} and within the scanning time of 10 minutes (Fig. 12), while the intended operation time of the applications is less than 1 minute. Higher bias voltages were not studied to avoid damages to the sensor element. Nonetheless, pulsed bias voltage operation or higher bias voltages can be

used to reduce the polarization effect, if the back-end electronics is capable to provide these, or the leakage current remains low enough to clearly distinguish signals from the noise [35]. This test was left out from this study, because the influence of polarization was found to be comparably small for the intended application. Higher bias voltage allows to reduce the polarization effect, but also increases the leakage current, which in this study is ultimately limited by maximum compliance of the employed source meter. In addition, temperature dependency studies were conducted over expected the range of sensor temperature variation. The determined temperature stability of the detector was better than expected. Nonetheless, controlling the heat that is generated by ASICs is critical when building up a multi-tile panel. Keeping all tiles of a full panel detector at the same temperature ensures also a more uniform response after calibration of the panel and if the test environment changes slightly.

Future studies will focus on the evaluation of charge sharing, pixel binning on an individual detector tile basis. As well as on charge sharing, pixel binning, and pixel trimming on a detector panel basis that consists of several individual detector tiles.

VI. CONCLUSION

The obtained results show that it is possible to develop a cost-effective and scalable solution for photon counting detector applications. The tested functional parameters of the tile were found to be comparable with the conventional wire bonded 3-side tile configurations. In addition, the detector tile's energy stability was found to be at the appropriate level for direct, energy selective X-ray detection. The proposed concept is a viable basis for the scaling studies, starting at the tile hybrid level to the multi-tile panel level.

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