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Switching waveform design with gate charge control for power MOSFETs

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ABSTRACT

The switching waveform design, especially controlling and optimizing the slew rate, is an efficient technique to mitigate the trade-off between decreasing the loss and increasing the noise of the switching power device. The digital active gate driver which generates the gate waveform to achieve the designed switching waveform requires a significant computational burden because the optimum driving point is searched automatically and comprehensively. This paper proposes a novel and simple method to calculate gate waveforms to achieve the designed switching waveforms. This method calculates how much gate charge is additionally required to match the designed waveform by exploiting the voltage and current response of the power device to the small gate charge pulse. The validation of this method is demonstrated by simulation in the case of both the drain-source voltage design and the drain current design. The deviation from the designed waveform is quantified in this paper.

1. Introduction

Suppressing the loss by use of high-frequency switching devices is one of the approaches to improve the efficiency of and reduce the weight of power electronic converters. High slew rate in voltage or current caused by driving the power device exerts a negative influence on the stable operation of the converters due to an increased EMI noise, a false turn-on, and a large voltage overshoot (Black, 2007; Oswald, Anthony, McNeill, & Stark, 2014).

To mitigate the trade-off between the improvement of efficiency and the stable operation of the power electric converters, the control and the optimization of slew rate are of importance. Various methods including Active Gate Driving (AGD) technique have been presented not only for silicon insulated gate bipolar transistors (IGBTs) but also for wide-bandgap power metal-oxide-semiconductor field-effect transistors (MOSFETs) to address this issue (Camacho, Sala, Ghorbani, & Martinez, 2017; Dymond et al., 2016; Eberle, Zhang, Liu, & Sen, 2008; Egashira, Oomori, & Omura, 2022; Fujita, 2013; Idir, Bausière, & Franchaud, 2006; John, Suh, & Lipo, 1999; Lobsiger & Kolar, 2015; Musumeci, Raciti, Testa, Galluzzo, & Melito, 1997; Takamiya et al., 2017; Vamshi Krishna & Hatua, 2018; Yang, Yuan, Zhang, & Palmer, 2015). The most commonly used gate drivers are voltage-source drivers without gate current control, and some of them with more complex structures or control algorithms have been reported (Fujita, 2013; Idir et al., 2006; Yang et al., 2015). The current-source drivers can be implemented using multiple switches or by current sources instead of switches (Eberle et al., 2008; Takamiya et al., 2017; Vamshi Krishna & Hatua, 2018). Some active gate drivers change the gate resistance dynamically (Camacho, Sala, Ghorbani, & Martinez, 2017; Dymond et al., 2016). The digital active gate driver, which controls and drives a power device using digital technology, has been actively investigated in recent years with improving the performance of digital hardware such as FPGAs or DSPs (Blank, Glück, Kugi, & Kreuter, 2015; Cheng et al., 2019; Dang, Kuhn, & Mertens, 2013; Dymond et al., 2016, 2018; Jones & Rogers, 2017; Liu et al., 2021; Miyazaki et al., 2017; Morikawa, Sai, Hata, & Takamiya, 2020; Schindler, Koeppl, Wicht, & Groeger, 2017; Takamiya et al., 2017).

In particular, the programmable digital active gate driver presented in Liu et al. (2021); Morikawa et al. (2020) generates an arbitrary gate drive waveform and finds the optimum gate driving point in terms of efficiency and stable operation. One of the practical ways to find the optimal driving point is the machine-based optimization using the simulated annealing algorithm (Miyazaki, Takamiya, & Sakurai, 2016). In this method, the optimized output waveform from the gate driver is obtained by automatically searching the minimum value of the objective function with parameters such as switching loss, voltage overshoot, and spectrum (Cheng et al., 2019; Miyazaki et al., 2017; Morikawa et al., 2020). Since the automatically searching requires a large number of iterative simulations, it takes time to find the optimum. This paper proposes a novel and simple method to obtain a gate drive waveform

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from a switching waveform, which can help exploring the optimal gate driving points.

Sections 2 and 3 describe the concept and the formulation of the proposed method. Section 4 demonstrates to validate the method by estimating the gate drive waveform from the target drain-source voltage waveform. The accuracy of the proposed method and applying this method to the drain current design are discussed in Section 5. Section 6 concludes together with the findings of the paper.

2. Conception of switching waveform design with gate charge control

Fig. 1 shows the ideal switching waveforms of MOSFET driven by a current-source gate driver.

As shown in the figure, it is found that the drain-source voltage V_{DS} and the drain current I_{DS} can be expressed by the function of the gate charge of MOSFET Q_g because Q_g is monotonically changed during the transition of V_{DS} or I_{DS}. Hence, there exists a close relationship between the slew rate dV_{DS}/dt or dI_{DS}/dt and dQ_g/dt. This means that it is possible to design the switching waveform by controlling the gate charge.

Fig. 2 shows a conceptual diagram of the proposed switching waveform design method. Fig. 3 depicts a schematic diagram of the digital active gate driving circuit based on the proposed method. The target waveform is defined as the switching waveform to be designed. The base waveform is the switching waveform observed by the waveform data acquisition system. The Gate Charge Controller (GCC) is comprised of a microcontroller, a memory, D/A converters (DACs), and voltage-controlled current sources (VCCSs). The GCC has three functions: waveform analysis, gate charge pulse calculation, and gate current pulse generation. The microcontroller takes the difference between the target waveform and the base waveform with the waveform analysis function, then calculates the gate charge pulse using the relationship between V_{DS} or I_{DS} and Q_g stored in the memory so that the target waveform is obtained. The gate current pulse is generated by the circuitry consisting of the microcontroller, the DACs, and the VCCSs by time differentiating of the gate charge pulse. A PWM signal monitored by the microcontroller triggers this circuitry, and the microcontroller

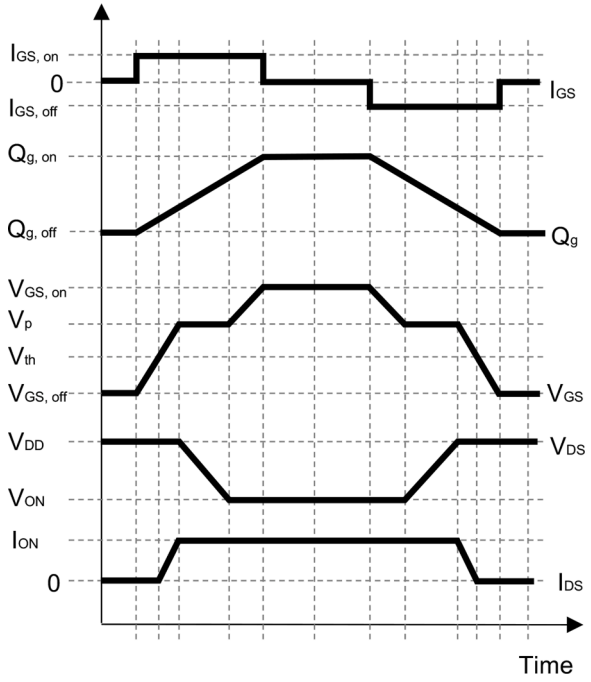

Fig. 1. Schematic diagram of switching waveforms when a MOSFET is driven by a current-source gate driver. V_p and V_{th} are the plateau voltage and the threshold voltage, respectively.

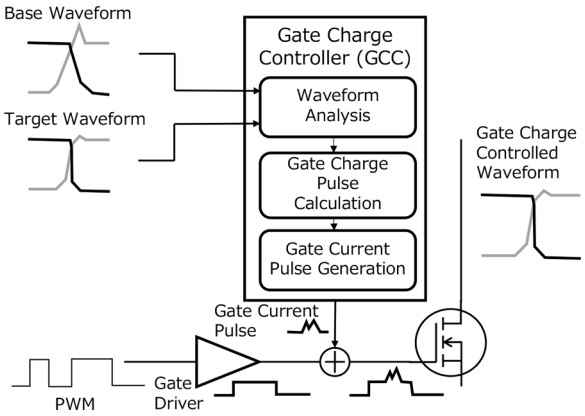

Fig. 2. Concept of the proposed method.

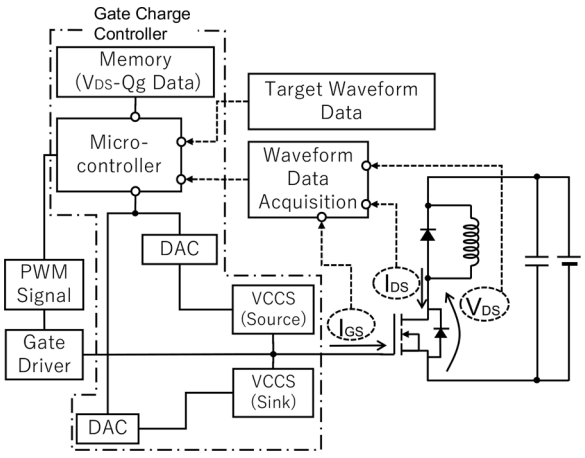

Fig. 3. Circuit diagram of the system based on the proposed method.

outputs the digital signal required to make the gate current pulse to the DACs at a timing that takes into account the delay time to be occurred by the DACs and the VCCSs. The gate current pulse generated by the DACs and the VCCSs is superimposed on the conventional gate driver output. An example of the gate current pulse generation using VCCS was demonstrated in Egashira et al. (2022). As shown in Fig. 3, two sets of DAC and VCCS are prepared as a source and a sink to charge or discharge the gate of the MOSFET.

3. Formulation of the proposed method

Fig. 4 depicts the notional plots between drain-source voltage and gate charge with time t as a parameter. In the region $[Q_g(a), Q_g(b)]$ where V_{DS} monotonically decreases against Q_g, $V_{DS}(t)$ can be expressed as

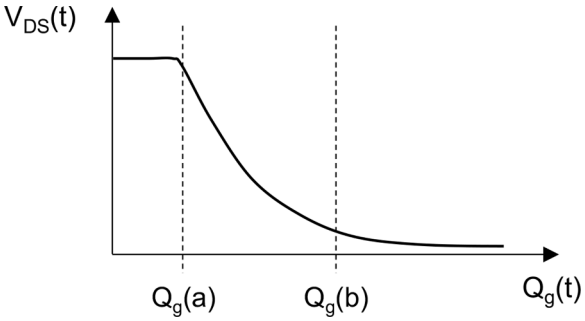

Fig. 4. Relationship between gate charge and drain-source voltage.

below.

$$V_{DS}(t) = f_{QV}\left(Q_g(t)\right) \tag{1}$$

where, $a \le t \le b$

The relationship between the deviation of V_{DS} and that of Q_g can be derived from Eq. (1) with the following definitions and assumptions.

$Q_{g0}(t)$ and $V_{DS0}(t)$ are defined as the gate charge and the drain-source voltage, respectively, when the MOSFET is driven by the gate current $I_{GS0}(t)$. The deviation from $Q_{g0}(t)$, $\Delta Q_g(t)$ is assumed to be zero at both ends of the region $[Q_g(a), Q_g(b)]$, namely, $\Delta Q_g(a) = \Delta Q_g(b) = 0$. Hence, the deviation from $V_{DS0}(t)$, $\Delta V_{DS}(t)$ becomes zero at both ends, $\Delta V_{DS}(a) = \Delta V_{DS}(b) = 0$. With a further assumption that $\Delta Q_g(t)$ is much smaller than $Q_{g0}(t)$, Eq. (1) can be linearized as follows:

$$V_{DS0}(t) + \Delta V_{DS}(t) = f_{QV}\left(Q_{g0}(t)\right) + \left(\frac{\partial f_{QV}}{\partial Q_g}\right)\Delta Q_g(t) \tag{2}$$

The correlation between $\Delta Q_g(t)$ and $\Delta V_{DS}(t)$ is quantified from Eq. (2) by exploiting the monotonicity of f_{QV}.

$$\Delta Q_g(t) = \left(\frac{\partial f_{QV}}{\partial Q_g}\right)^{-1} \Delta V_{DS}(t) \tag{3}$$

The gate current pulse output from the GCC, $\Delta I_{GS}(t)$ is derived from time differentiating both sides of Eq. (3).

$$\Delta I_{GS}(t) = \left(\frac{\partial f_{QV}}{\partial Q_g}\right)^{-1} \frac{\partial}{\partial t}\Delta V_{DS}(t) \tag{4}$$

The discretized forms of time-dependent gate charge and drain-source voltage are defined with a time interval τ and integer n as follows.

$$Q_g[n] := Q_g(n\tau) \tag{5}$$

$$V_{DS}[n] := V_{DS}(n\tau) \tag{6}$$

In the region $[Q_g(\alpha\tau), Q_g(\beta\tau)]$ where V_{DS} monotonically decreases against Q_g, $V_{DS}[n]$ can be expressed as a monotone function of $Q_g[n]$. The discretized form of the gate current pulse output from the GCC, $\Delta I_{GS}[n]$ is derived in a similar manner as previously presented.

$$\Delta I_{GS}[n] = \left(\frac{\partial f_{QV}}{\partial Q_g}[n]\right)^{-1} \frac{\Delta V_{DS}[n] - \Delta V_{DS}[n-1]}{\tau} \tag{7}$$

where $\Delta V_{DS}[\alpha - 1] = \Delta V_{DS}[\alpha] = \Delta V_{DS}[\beta] = 0$, and $\Delta Q_g[\alpha] = \Delta Q_g[\beta] = 0$.

It is noted that the expression of function f_{QV} must be explicitly defined in advance to determine ΔI_{GS} by the continuous gate charge control method in Eq. (4) or the discrete gate charge control method in Eq. (7). It is important to develop a method to calculate ΔI_{GS} without obtaining the detail of function f_{QV} from the practical viewpoint because the expression of function f_{QV} is not easy to estimate in many cases.

For the discrete gate charge control method, $\frac{\partial f_{QV}}{\partial Q_g}[n]$ can be calculated by using the drain-source voltage response to the small gate charge pulse rather than by using the explicit description of function f_{QV}. The detail of this method is described in the next section with simulation results.

4. Results

The model of RCJ700N20, Si-MOSFET was used for all SPICE simulations in this work. To verify the model, the relationship between Q_g and V_{DS} was measured. The device was driven under the resistive load with the supply voltage V_{DD} of 15 V and the drain current I_{ON} of 3 A. Fig. 5 compares the measured $Q_g - V_{DS}$ curve with the simulated result. Both of the curves are well-matched.

Fig. 6 illustrates the circuit diagram utilized in the simulation to verify the proposed method. The stray capacitance of the diode and the stray inductance in the circuit are assumed to be negligible. The

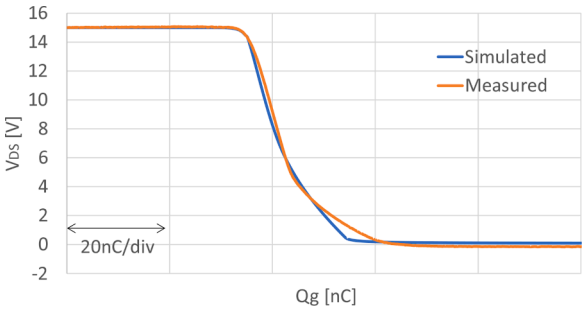

Fig. 5. Measured relationship between the gate charge and the drain-source voltage of RCJ700N20.

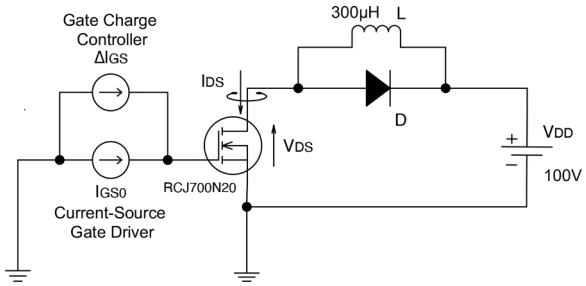

Fig. 6. Circuit diagram to verify the proposed method.

MOSFET is driven by a current-source gate driver. V_{DD} of 100 V and I_{ON} of 50 A are set for this numerical study. I_{GS0} is set to 20 mA at turn-on, and − 20 mA at turn-off.

Fig. 7 shows the switching waveforms without any current pulse from the GCC. $V_{GS0}(t)$ and $I_{DS0}(t)$ are defined as the gate-source voltage and drain current, respectively, when the MOSFET is driven by the gate

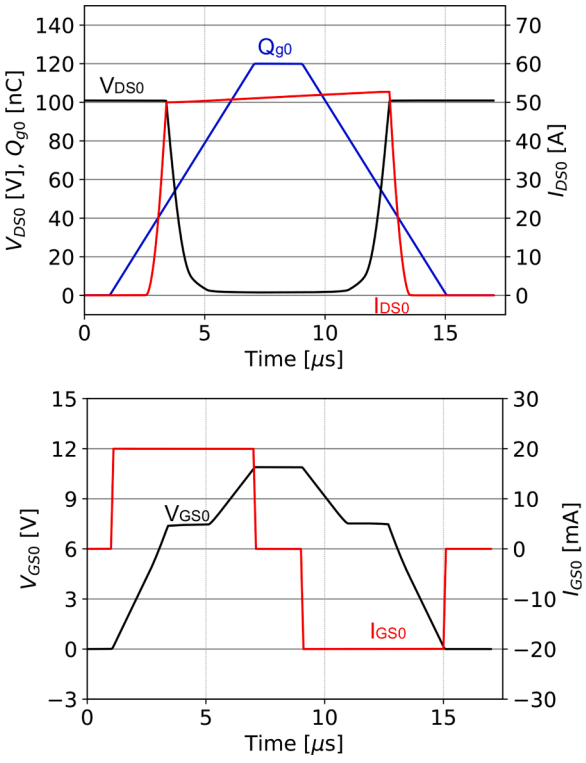

Fig. 7. Voltage and current switching waveforms during turn-on and off with the current-source gate driver.

current $I_{GS0}(t)$.

In this section, the verification is performed with the trajectory of drain-source voltage at the turn-off phase. The target waveform of drain-source voltage is designed by adding the deviation $\Delta V_{DS}(t)$ from the base waveform $V_{DS0}(t)$. As an example of the waveform design to reduce the switching loss, $\Delta V_{DS}(t)$ is defined by Eq. (8) taking into account that the Gaussian function has smoothness. Fig. 8 shows the base and target waveform of the drain-source voltage.

$$\Delta V_{DS} = -30.0 \exp\left(-\frac{(t-4.4)^2}{0.02}\right) \tag{8}$$

4.1. Waveform design by continuous gate charge control method

When $\Delta I_{GS}(t)$ is calculated from Eq. (4), the explicit description of function f_{QV} and its derivative with respect to Q_g are necessary. The function f_{QV} is approximated by a quadratic function in the region where the drain-source voltage decreases monotonically against the gate charge. V_{DS} - Q_g curve derived from Fig. 7 and the domain of the function f_{QV} are shown in Fig. 9. By fitting the curve in the domain, $\left(\frac{\partial f_{QV}}{\partial Q_g}\right)^{-1}$ is expressed as follows.

$$\left(\frac{\partial f_{QV}}{\partial Q_g}\right)^{-1} = \frac{1}{0.3152 Q_g - 22.5} \tag{9}$$

The gate current pulse output from the GCC is obtained from Eqs. (4), (8), and (9). Fig. 10 shows the pulse of the gate charge and the gate current required to be added in order to achieve the target drain-source voltage waveform in the case that the deviation from the base waveform is given by Eq. (8).

With the calculated gate current pulse output from the GCC, the drain-source voltage waveform was simulated. Fig. 11 compares the simulated waveform with the target waveform to evaluate the validity of the proposed method when the expression of the relationship between the drain-source voltage and the gate charge is explicitly known. Since the simulated waveform shows good agreement with the target waveform, it is considered to be able to design the drain-source voltage waveform from the existing base waveform by the continuous gate charge control method.

4.2. Waveform design by discrete gate charge control method

The proposed method requires deriving an explicit description of function f_{QV}, even approximately, as demonstrated in the previous subsection. This procedure is indispensable for the continuous gate charge control method but not for the discrete gate charge control method. It is because $\partial f_{QV}/\partial Q_g$ for each time interval τ in Eq. (7) is attained by exploring drain-source voltage response to small gate charge pulse.

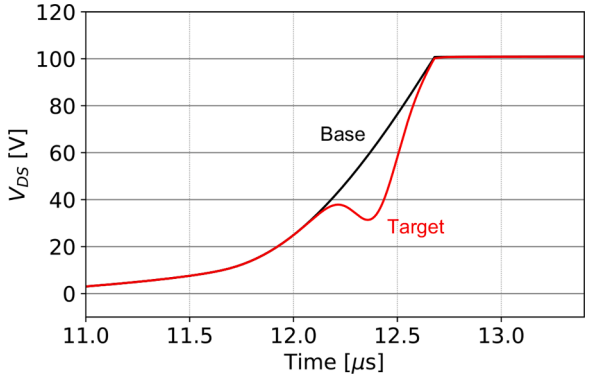

Fig. 8. Target and base drain-source voltage waveform during turn-off.

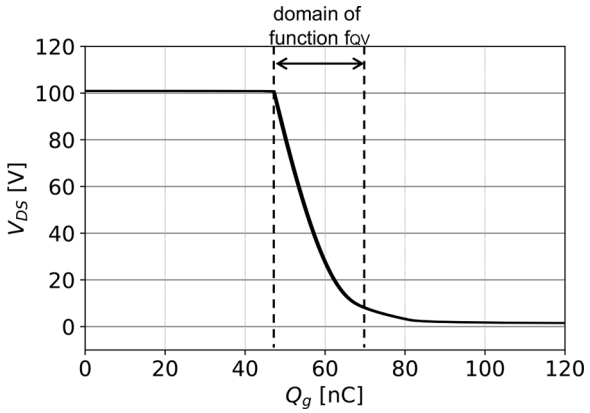

Fig. 9. Dependence of the drain-source voltage on the gate charge during the miller plateau.

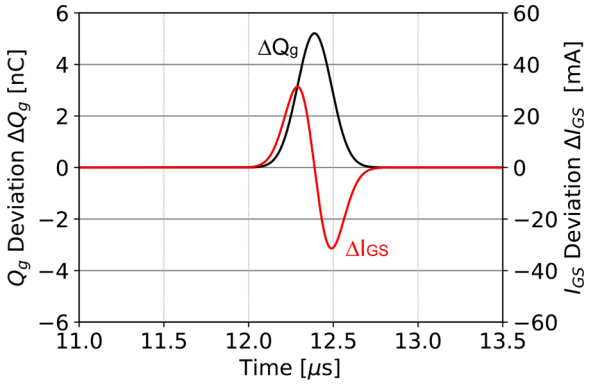

Fig. 10. Calculated gate charge and gate current pulse to obtain the target waveform based on the continuous gate charge control method.

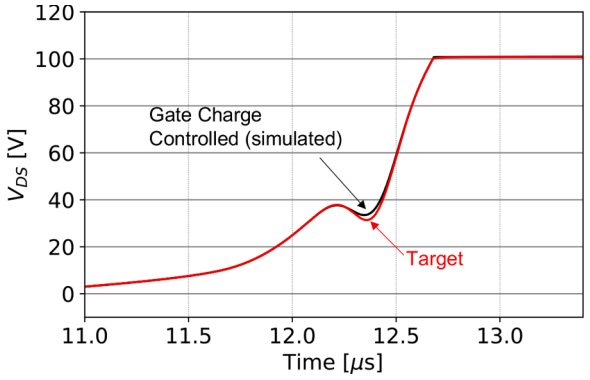

Fig. 11. Simulated drain-source voltage waveform during turn-off, based on the continuous gate charge control method.

The small gate charge pulse denoted by $\widetilde{Q_g}(t,m)$ is defined as in Eq. (10). In Eq. (10), m is an integer in $\alpha \le m \le \beta$.

$$\widetilde{Q_g}(t,m) = q_m \, \varphi\left(\frac{t}{\tau} - m\right) \tag{10}$$

Here, $\varphi(x)$ is described as

$$\varphi(x) = \begin{cases} 1-|x| & |x| \le 1 \\ 0 & |x| > 1 \end{cases} \tag{11}$$

Hence, the small gate current pulse to generate $\widetilde{Q_g}(t,m)$ is obtained by

differentiating both sides of Eq. (10) with respect to time.

$$\widetilde{I_{GS}}(t,m) = q_m \frac{d}{dt}\,\varphi\left(\frac{t}{\tau} - m\right) \tag{12}$$

As an example, a small triangular gate charge pulse and the gate current waveform to generate it are plotted in Figs. 12 and 13respectively. τ was set as 0.1 μs.

The drain-source voltage response to $\widetilde{Q_g}(t,m)$, which is denoted by $\widetilde{V_{DS}}(t,m)$ can be expressed as follows for $\alpha \le m \le \beta$.

$$\widetilde{V_{DS}}(t,m) = v_m\,\varphi\left(\frac{t}{\tau} - m\right) \tag{13}$$

Since the time delay of the response of drain-source voltage to gate charge is negligible, Eq. (14) is derived from Eqs. (10) and (13).

$$\frac{\partial V_{DS}}{\partial Q_g}[m] = \frac{v_m}{q_m} \tag{14}$$

$\widetilde{V_{DS}}(t,m)$ is calculated by taking the difference between $V_{DS}(t,m)$ obtained by adding the small gate current pulse $\widetilde{I_{GS}}(t,m)$ to $I_{GS0}(t)$ and $V_{DS0}(t)$. Figs. 14 and 15 exemplify plots of $\widetilde{Q_g}(t,m)$ and $\widetilde{V_{DS}}(t,m)$ for each m in $\alpha \le m \le \beta$, respectively.

Since $\Delta V_{DS}(t)$ can be expressed as in Eq. (15) with the coefficient λ_m which is the ratio between $\Delta V_{DS}[m]$ and v_m, $\Delta I_{GS}(t)$ is derived as in Eq. (16) using Eqs. (4), (12), and (14).

$$\Delta V_{DS}(t) = \sum_m \lambda_m v_m\,\varphi\left(\frac{t}{\tau} - m\right) \tag{15}$$

$$\Delta I_{GS}(t) = \sum_m \lambda_m \widetilde{I_{GS}}(t,m) \tag{16}$$

Therefore, given that the drain-source voltage response to the small gate charge pulse is known, the gate current pulse output from the GCC to obtain the target waveform is able to be calculated by Eq. (16) without having the exact form of the function f_{QV}.

Fig. 16 shows the pulse of the gate charge and the gate current pulse output from the GCC using the method explained above. The current pulse is required to be added to the gate driver output in order to achieve the target drain-source voltage waveform in the case that its deviation from the base waveform is given by Eq. (8).

Fig. 17 compares the simulated waveform to the target waveform to evaluate the validity of the proposed discrete gate charge control method. In comparison with Fig. 11, the difference between the target and the simulated waveform is a little bit large. This is attributable to 0.1μs of the time interval τ. It is expected that a much smaller deviation will be observed by reducing the time interval.

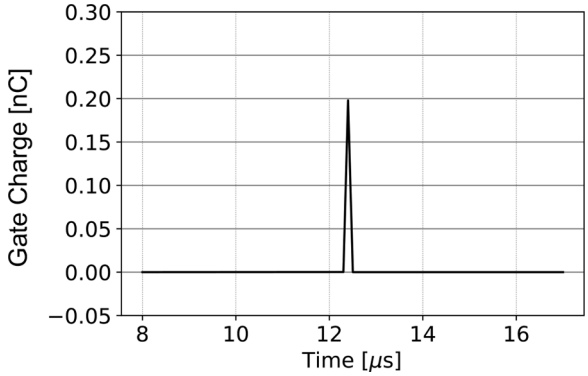

Fig. 12. Small triangular gate charge pulse.

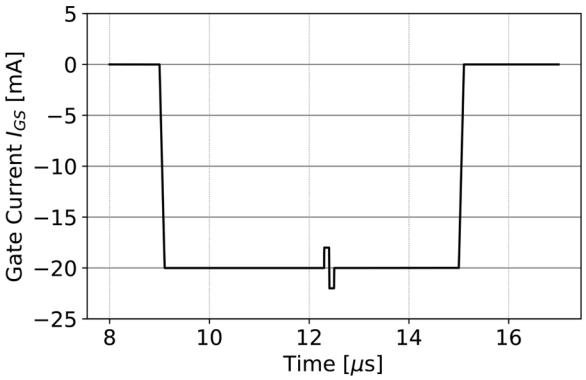

Fig. 13. Gate current waveform with the small pulse to generate the triangular gate charge pulse during turn-off.

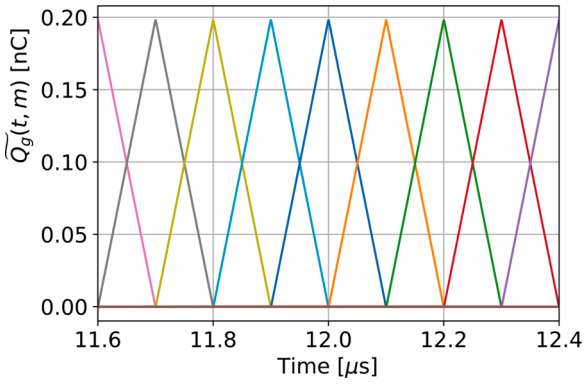

Fig. 14. Small gate charge pulse train.

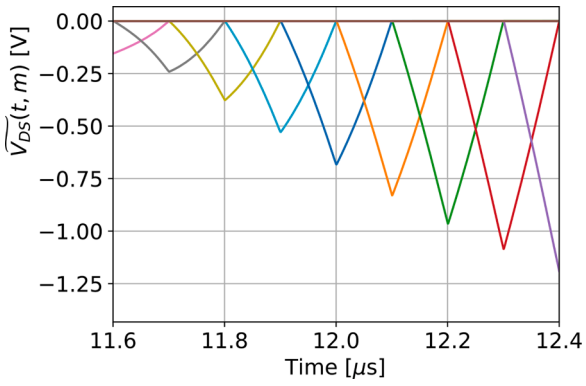

Fig. 15. Drain-source voltage response to the small gate charge pulse train.

5. Discussions

5.1. Waveform matching error of discrete gate charge control method

The estimation of the gate current pulse output from the GCC based on the proposed method assumed sufficiently small $\Delta Q_g(t)$ with respect to $Q_{g0}(t)$ and a linear relation between drain-source voltage and gate charge. Therefore, it is predicted that the simulated waveform will deviate significantly from the target waveform as the maximum value of the Q_g deviation ratio, which is defined by $\Delta Q_g(t)/Q_{g0}(t)$, increases. To examine this prediction, the waveform matching error between the target and the simulated waveform, represented by M, is formulated by the following equation.

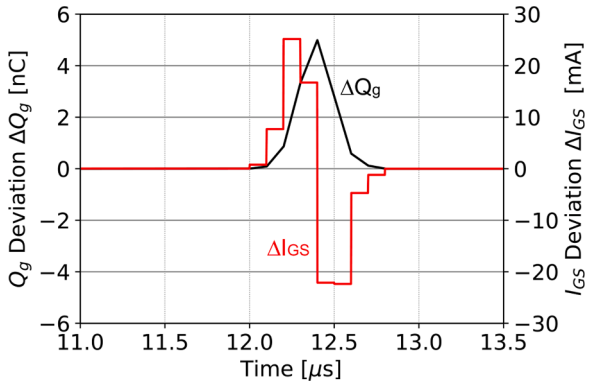

Fig. 16. Calculated gate charge and gate current pulse to obtain the target waveform based on the discrete gate control method.

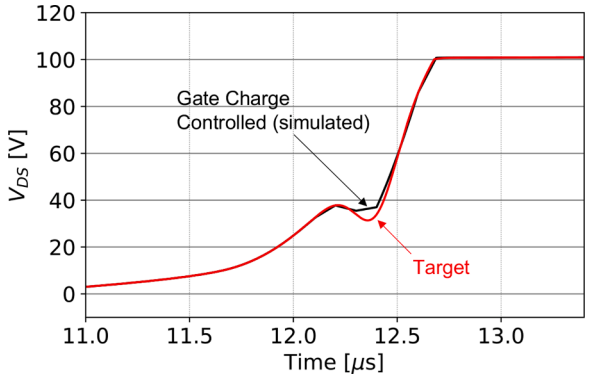

Fig. 17. Simulated drain-source voltage waveform during turn-off, based on the discrete gate charge control method.

$$M = \frac{\left| \int V_{DSo}(t) I_{DSo}(t) dt - \int V_{DSs}(t) I_{DSs}(t) dt \right|}{\int V_{DSo}(t) I_{DSo}(t) dt} \tag{17}$$

Subscript o refers to the target waveform and subscript s refers to the simulated waveform. The integral time starts from the time when V_{DS} is over 10% of V_{DD} and ends at the time when I_{DS} reaches 10% of I_{ON}.

Fig. 18 plots the waveform matching error computed by Eq. (17) as a function of the maximum value of Q_g deviation ratio. $\Delta Q_g(t)/Q_{g0}(t)$ was calculated based on the method described in Section 4.2 with the deviation of the target waveform from the base waveform given by Eq. (18). σ was set to be fixed as 0.1 μs but V_{peak} and μ were adjusted so that the maximum Q_g deviation ratio is varied from 0 to 16%.

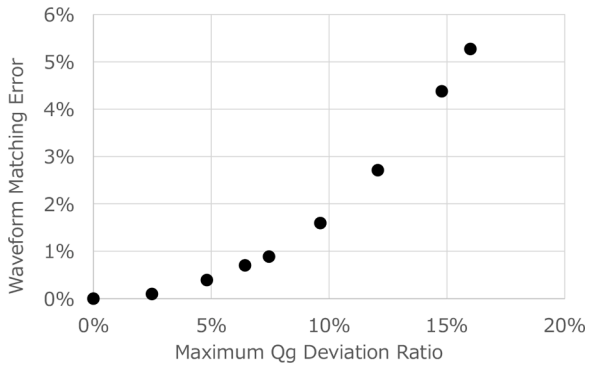

Fig. 18. Dependence of waveform matching error on maximum Qg deviation ratio.

$$\Delta V_{DS} = V_{peak} \exp\left(-\frac{(t-\mu)}{2\sigma^2} \right) \tag{18}$$

According to Fig. 18, the waveform matching error increases with the square of the maximum Q_g deviation ratio. This is attributed to the premise of the proposed method in which the relationship between the drain-source voltage and the gate charge is regarded as linear as shown in Eq. (2). From this figure, the waveform matching error is suppressed by less than 5% when the maximum Q_g deviation ratio is within 15%. Therefore, the waveform matching error from the target waveform can be well suppressed by using the proposed method several times, even though the deviation of the target waveform from the base waveform is large.

5.2. Expansion to drain current waveform design

The gate current pulse output from the GCC can be calculated from the target waveform of the drain current $I_{DS}(t)$ in a similar manner to the method described in the previous sections. In the region $[Q_g(c), Q_g(d)]$ where $I_{DS}(t)$ increases monotonically with respect to $Q_g(t)$, $I_{DS}(t)$ can be expressed as a function of $Q_g(t)$ as below under the assumption that the stray inductance in the power loop is negligible.

$$I_{DS}(t) = f_{QI}\left(Q_g(t)\right) \tag{19}$$

where, $c \le t \le d$

Assuming that the deviation from $Q_{g0}(t)$ at both ends of the region $[Q_g(c), Q_g(d)]$ is zero, the gate current pulse output from the GCC, which is required to add $\Delta I_{DS}(t)$ to $I_{DS0}(t)$, is expressed as in Eq. (20). Here, $Q_{g0}(t)$ and $I_{DS0}(t)$ are defined as the gate charge and the drain current respectively when the MOSFET is driven by the gate current $I_{GS0}(t)$.

$$\Delta I_{GS}(t) = \left(\frac{\partial f_{QI}}{\partial Q_g} \right)^{-1} \frac{\partial}{\partial t} \Delta I_{DS}(t) \tag{20}$$

$\Delta I_{DS}(t)$ is described below similar to Eq. (15) using the drain current response to the small gate charge pulse $\widetilde{Q_g}(t,m)$, which is denoted by $\widetilde{I_{DS}}(t,m)$.

$$\Delta I_{DS}(t) = \sum_m \beta_m \widetilde{I_{DS}}(t,m) \tag{21}$$

Hence, the gate current pulse output from the GCC is represented in the discretized form without the exact expression of function f_{QI} as shown in Eq. (22) similar to Eq. (16).

$$\Delta I_{GS}(t) = \sum_m \beta_m \widetilde{I_{GS}}(t,m) \tag{22}$$

In the same manner as the previous section, the verification was performed with the trajectory of the drain current at the turn-off phase. The target waveform of the drain current is obtained by adding the deviation $\Delta I_{DS}(t)$ to the base waveform $I_{DS0}(t)$. As an example of the waveform design to reduce the switching loss, $\Delta I_{DS}(t)$ is defined by Eq. (23) taking into account that the Gaussian function has smoothness. Fig. 19 shows the base and target waveform of the drain current.

$$\Delta I_{DS} = -15.0 \exp\left(-\frac{(t-4.9)^2}{0.01} \right) \tag{23}$$

The drain current waveform was simulated with the gate current pulse output from the GCC calculated from Eqs. (21) to (23). In comparison of the target and the simulated waveform in Fig. 20, it is found that the proposed method is applicable to design the drain current waveform with the premise that the drain current response to the small gate charge pulse is known and that the stray inductance in the power loop is negligible.

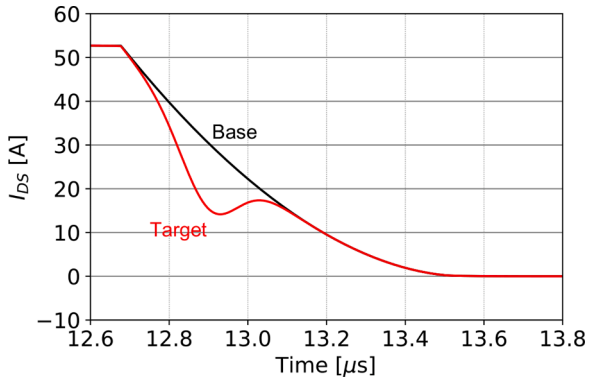

Fig. 19. Target and base drain current waveform during turn-off.

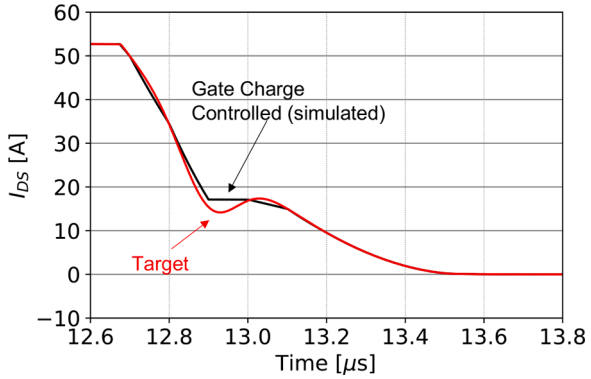

Fig. 20. Simulated drain current waveform during turn-off, based on the discrete gate charge control method.

5.3. Waveform design with stray inductance

The proposed method for obtaining the gate current pulse output from the GCC to match the designed switching waveform has been verified with the assumption of negligible stray inductance in the power loop. In this section, the impact of the stray inductance on the proposed method is discussed.

The simulation was performed using the circuit diagram as shown in Fig. 6 with 70 nH of stray inductance inserted between the drain terminal of the MOSFET and the inductor. The same ΔV_{DS} and ΔI_{DS} described in Eqs. (8) and (23) respectively were used for the simulation. The drain-source voltage and the drain current response, $\widetilde{V_{DS}}(t,m)$ and $\widetilde{I_{DS}}(t,m)$, to the small gate charge pulse $\widetilde{Q_g}(t,m)$ were re-calculated taking the stray inductance into account.

Fig. 21 depicts the comparison of the target and the simulated waveform for the drain-source voltage and the drain current when the stray inductance in the power loop is not negligible. As shown in Fig. 21 (a), the difference between the simulated and the target becomes large after the voltage transition completes although both are very close during the transition. It is found that the proposed method is effective as a voltage slew rate control method regardless of the stray inductance in the power loop.

From Fig. 21(b), the deviation from the target waveform is observed during the transition of the drain current. Since the slopes of both waveforms are close, the timing difference in which I_{DS} starts to drop is considered to be the main reason for this deviation. The timing difference is attributable that the drain-source voltage in the domain of the function f_{QI} is given by not the constant voltage V_{DD} assumed in the proposed method but the time-varying voltage $V_{DS}(t) = V_{DD} + L_s \cdot dI_{DS}/dt$, taking the stray inductance L_s into consideration.

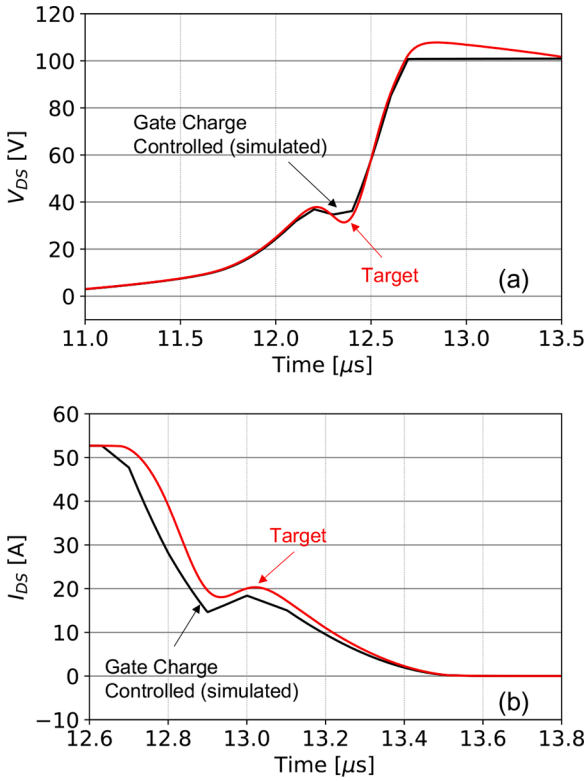

Fig. 21. Simulated drain-source voltage (a) and drain current (b) waveform during turn-off, based on the discrete gate charge control method in the case that stray inductance is not negligible.

5.4. Comparison of the proposed methods with published works

Table 1 shows the comparison of the proposed method with the published works. The published methods control one or a couple of parameters related to the switching process, such as slew rate, loss, and overshoot, or an objective function defined by a combination of two parameters, whereas this method controls the switching waveform itself. The proposed method makes it possible to directly adjust a part of the waveform as well as to improve the overall switching performance.

Since the method reported here makes use of the drain-source voltage or the drain current response to the small gate charge pulse to obtain the gate current waveform, the time interval of the gate current waveform is determined by the width of the small gate charge pulse. This method can generate the gate current waveform with a finer time interval than the method in which the turn-on and the turn-off switching process are each subdivided into four stages and the feedback control is performed at each stage (Dang et al., 2013). It is the same as other methods to set time intervals that are sufficiently smaller than the time required for turn-on and turn-off transitions, taking into account the device type to be driven.

Furthermore, the time required to reach the target value can be suppressed in this method because it does not involve finding the target value by manual trial-and-error or by metaheuristic algorithm as reported in Cheng et al. (2019); Dymond et al. (2018); Liu et al. (2021); Miyazaki et al. (2016); Morikawa et al. (2020).

6. Conclusion

This article proposed a novel method to obtain the gate waveform from the switching waveform based on the drain-source voltage or the drain current response to the small gate charge pulse. It has been

Table 1
Comparison with previous works.

	Dang et al. (2013)	Dymond et al. (2018); Liu et al. (2021)	Miyazaki et al. (2016); Morikawa et al. (2020)	Cheng et al. (2019)	This work
Device type, Rating	Si-IGBT 3300 V	GaN-FET 40 V GaN-HEMT 650 V	Si-IGBT 600 V Si-IGBT 1200 V	Si-IGBT 1700 V	Si-MOSFET 200 V
Control Target	dV/dt, dI/dt, reverserecovery current	Loss, V_{DS} over-shoot, V_{DS} spectrum	Euclidean norm of loss and V_{CE}, I_{CE} overshoot or EMI spectrum area (Object function)	Sum of loss and surge voltage (Object function)	Switching waveform (V_{DS}, I_{DS})
Target value setting	Required	Required	Not necessary	Not necessary	Required
How to reach the target value	LUT of gate current for each stage is updated by feedback control.	Gate resistance profile is provided by trial-and-error and open-loop control.	The gate current waveform is obtained by finding the minimum of object function using simulated annealing (SA).	Same as Miyazaki et al. (2016); Morikawa et al. (2020) but using particle swarm optimization (PSO).	The gate current waveform is obtained using V_{DS} or I_{DS} response to the small Qg pulse.
Waveform replicability	Yes	Yes	No(Due to SA)	No(Due to PSO)	Yes
Time interval	4 stages in each turn-on and turn-off process	150 ps Dymond et al. (2018) 100 ps Liu et al. (2021)	200 ns Morikawa et al. (2020) 80 ns Miyazaki et al. (2016)	20 ns	100 ns
Time cost to reach the target value	Small	Middle	Large	Middle	Small

validated with the simulation that when the deviation of gate charge for designing the drain-source voltage waveform is less than 15%, the proposed method provides the waveform matched to the design well. Slew rate control is one of the methods with the aim of improving the trade-off between EMI noise suppression and switching loss reduction. The proposed method for designing the switching waveform changes the voltage or the current slope locally during its transition so that the waveform matches the target and the switching loss is reduced. Hence, adding the proposed GCC to the conventional gate driving circuit with low current output for switching the MOSFET slowly in terms of EMI noise suppression is able to provide an efficient solution to mitigate the trade-off. Furthermore, since the proposed method offers a way to find the gate driving point to attain the desired switching waveform, it is considered that this method can contribute to reducing the computational burden to search for the optimum in the digital active gate driver.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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