Parasitic oscillation analysis of trench IGBT during short-circuit type II using TCAD-based signal flow graph model

doi: https://doi.org/10.1109/TED.2022.3202883

Parasitic oscillation analysis of trench IGBT during short-circuit type II using TCAD-based signal flow graph model

Hiroshi Kono and Ichiro Omura, *Member, IEEE*

***Abstract*—The oscillation phenomenon of trench-type insulated gate bipolar transistors during short-circuit type II was investigated experimentally and theoretically. The gate resistance required to suppress oscillations decreased with an increasing collector voltage. The oscillation conditions were calculated from the signal flow graph model using the S-parameter based on a technology computer-aided design simulation. The calculation results reproduced the locus of the collector voltage dependence of the experimentally measured gate resistance. The oscillation mechanism was investigated using the device simulation. The response of carrier density modulation at the base-drift layer boundary was found to transmit to the collector side through the electron-hole plasma region during the oscillation, indicating that the transfer characteristics of the carrier density modulation in the drift region at the specific collector voltage influence the collector voltage dependence of the short-circuit oscillation. The influence of circuit parameters on the oscillation was also investigated. An increase in the emitter inductance suppressed the oscillations, whereas an increase in gate inductance increases oscillations.**

***Index Terms*—IGBT, Oscillation, S-parameter, Signal flow graph, short-circuit, TCAD.**

I. Introduction

To achieve smaller volume and lower power consumption in power conversion systems, power devices with higher current densities and speeds have been developed. As the characteristics of these devices improve, the suppression of parasitic turn-on and parasitic oscillation during the switching operation and electromagnetic compatibility (EMC) to ensure reliability have become important issues. In addition to the nominal operation, stable operation during avalanche and short-circuit (SC) protections should be ensured for reliability and EMC of power devices and power conversion units. The stability of silicon-insulated gate bipolar transistors (Si-IGBTs) and silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) under SC type I, II, and III conditions has been studied [1-6].

In discussing the oscillation phenomena during SC operation, technology computer-aided design (TCAD) mixed-mode simulation is an effective tool to simultaneously calculate the internal state of the device and the state of the circuit [2, 4-6]. However, TCAD mixed-mode simulations require considerable computational time. Hence, this method is not suitable for designing a stable power conversion circuit system because the investigation of the oscillation condition cannot be completed within a reasonable time.

The authors proposed a simple but powerful method to calculate the oscillation conditions of power devices coupled with TCAD-simulated S-parameters and a novel signal-flow graph model. Recently, the S-parameter has been used in RF and microwave circuit designs, and for circuit parameter measurement and EMC analysis of power devices [7-9]. The proposed method can be applied to analyze the oscillation conditions based on semiconductor physics within a short computational time, according to which stable and unstable conditions were directly calculated using the Nyquist stability criterion. This also led to a quantitative design margin for stable designs [10]. The authors' previous paper focused on the theoretical proposal, and the application to the experimentally observed phenomena was not sufficiently discussed.

In this study, we applied the proposed method to the oscillation phenomenon of IGBTs during SC type II. The peak value of the current in SC type II is greater than that in SC type I because di/dt is determined using the parasitic inductance of the SC loop and the DC link voltage [3]. The oscillation

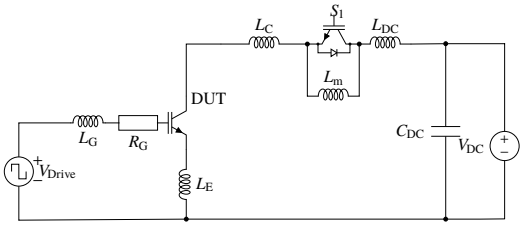


Fig. 1 Experimental circuit to investigate the oscillation phenomenon of IGBT. The circuit comprises a low-side IGBT as a DUT and a high-side IGBT module as a switch S_1. To reproduce SC type II, S_1 was switched on while the low-side gate was on.

Hiroshi Kono, was with Kyushu Institute of Technology, 1-1 Sensui-cho, Tobata-ku, Kitakyushu-city, Fukuoka 804-8550, Japan. He is now with Toshiba Electronic devices and storage corporation (hiroshi.kono@toshiba.co.jp).

Ichiro Omura is with Kyushu Institute of Technology, 2-4, Hibikino, Wakamatsu-ku, Kitakyushu 808-0196, Japan.

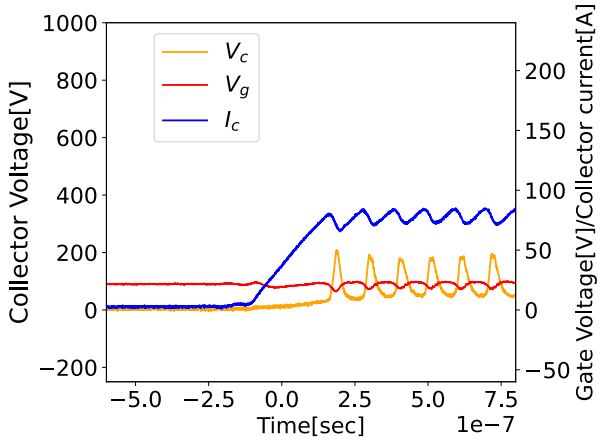
conditions are investigated experimentally, analyzed using the proposed method, and the results are compared.

The electron-hole plasma inside the device can also be the origin of oscillation phenomena in IGBTs, unlike SiC-MOSFETs treated in the previous study. We investigated the relationship between the internal carrier response of the IGBT and oscillation phenomena. We also investigated the impact of circuit parameters on oscillations.

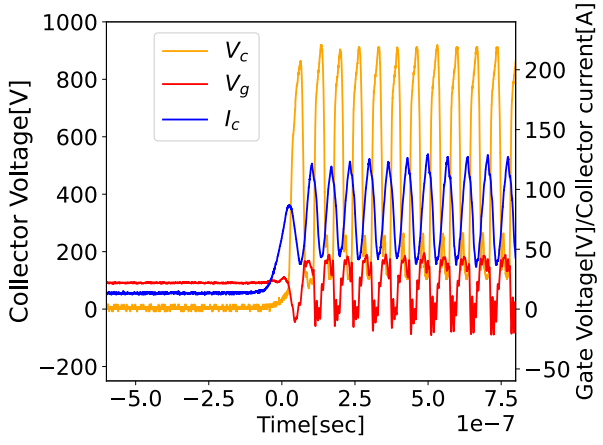
This paper further elaborates on the report presented at CIPS2022 [11] with adding new investigation results on the effect of parasitic inductance on the oscillation phenomena.

II. Experiment

Fig. 1 shows the circuit used in the experiments to investigate the oscillation phenomena in SC type II. Commercial Si-IGBTs (Infineon IGW08T120FKSA1 1200 V, 16 A) were used as the device under tests (DUTs). L_G, L_E, L_C, and L_{dL} are stray inductances, and L_m is the load inductance. These values were evaluated through measurements using an impedance analyzer and switching waveform comparison. An Si-IGBT module with a sufficiently high rated current was used as the high-side switch S_1.



(a) V_c = 100 V



(b) V_c = 600 V

Fig. 2 Switching waveforms of the IGBT during the SC type II. The high-side switch is switched ON while the low-side IGBT's gate was ON. The short-circuit current induces a parasitic oscillation of the low-side IGBT.

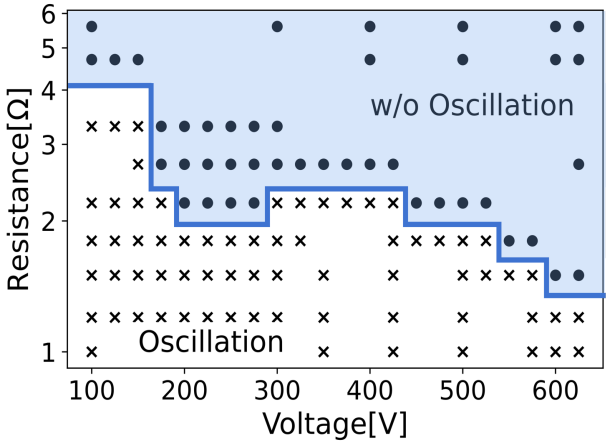


Fig. 3 Presence of the oscillation on the gate resistance and collector voltage. The circles indicate the points where no oscillation is observed, and the crosses indicate the points where oscillation is observed.

The experiments were conducted at room temperature. The driving gate voltage was 20/−5 V. The gate resistance R_G and collector voltage V_{DC} varied. Table I lists the evaluated parameters. To reproduce SC type II, S_1 was switched ON while the low-side gate was ON.

TABLE I
Circuit parameters shown in Fig. 1

L_G	L_E	L_{DC}	L_C	L_m
200 nH	5 nH	20 nH	20 nH	100 µH
R_G	V_{Drive} *on*	V_{Drive} *off*	V_{DC}	C_{DC}
Variable	20 V	-5 V	Variable	100 µF

Fig. 2 shows the switching waveforms of the IGBT in SC type II when V_{DC} = 100 V, R_G = 3.3 Ω and when V_{DC} = 600 V and R_G = 1.2 Ω. The short-circuit event induces gate and collector voltages, and collector current oscillations.

Under each condition, the gate and collector voltages oscillation occurred in SC type II when V_{DC} = 100 V and 600 V, respectively. The oscillation frequencies were 9.2 and 15.1 MHz when V_{DC} = 100 V and 600 V, respectively.

These oscillations can be suppressed by increasing the gate resistance. Fig. 3 shows the presence of oscillations depending on the gate resistance and collector voltage. The circles indicate the points of no oscillations and the crosses indicate the points at which oscillation was observed. The gate resistance required to suppress the oscillation increased with decreasing collector voltage. Based on the result, oscillation is more likely to occur as the collector voltage decreases.

III. TCAD Simulation Model for IGBT

To investigate the oscillation phenomena of the Si-IGBT during SC Type II, the signal flow method and S-parameter were computed using the TCAD device simulation proposed in the author's previous paper [10].

A TCAD simulation model was introduced to calculate the oscillation conditions. An IGBT with a trench field-stop

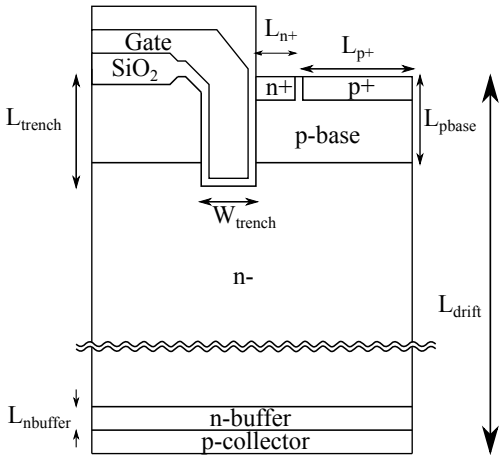


Fig. 4 Simulation structure of the trench IGBT.

structure was used as the IGW08T120 [12], [13]. The detailed design parameters of the IGBT were unclear because it was a commercial product. Thus, the structure shown in Fig. 4 was assumed.

The device parameters were determined by referring to previous studies on the simulation model analysis for trench field-stop IGBTs [14] and by comparing the calculation results with the characteristics provided in the datasheet [15]. These calculated values are equivalent to the on-voltage and output capacitances provided in the datasheet. The current saturation characteristic at high voltages is approximately 100 A, which is similar to the saturation current in the SC test. Table II lists the device parameters of the TCAD device model.

Table II
Device parameters of the TCAD device model

L_{drift}	130 µm	L_{trench}	4 µm
L_{n+}	1.3 µm	L_{p+}	5 µm
W_{trench}	2 µm	$L_{p\text{-}base}$	3.5 µm
$n_{p\text{-}base}$	$5 \times 10^{16}\text{cm}^{-3}$	n_{drift}	$1 \times 10^{14}\text{cm}^{-3}$
$n_{n\text{-}buffer}$	$2 \times 10^{17}\text{cm}^{-3}$	$L_{n\text{-}buffer}$	2 µm

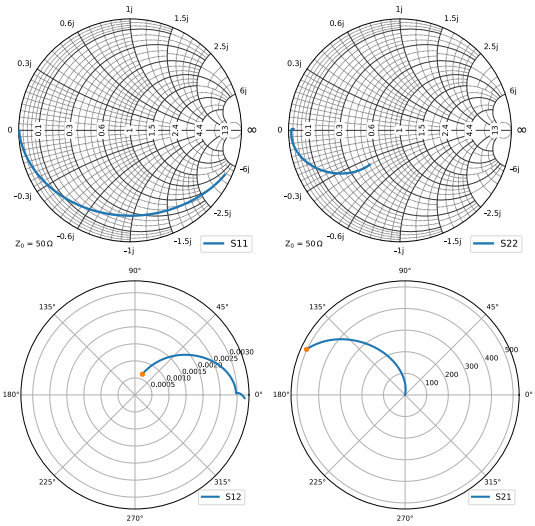
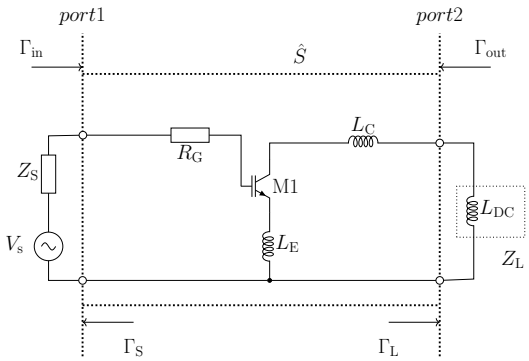


Fig. 5 Smith charts of the calculated S-parameters when V_C = 100 V.

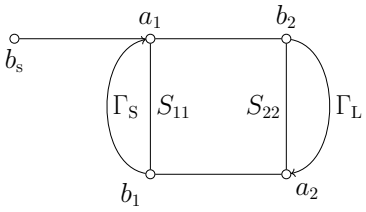
The S-parameters of the assumed simulation model structure can be calculated using the small-signal AC analysis function of a TCAD simulator. Fig. 5 shows the S-parameters plotted on the Smith charts, which are a representation in the reflection coefficient plane. In the graphs of S_{11} and S_{22}, the abscissa is the magnitude of the real part of the reflection coefficient. The upper half has a positive complex component and the lower half has a negative complex component. It is normalized by the characteristic impedance. The reflection coefficient is 0 at the center, 1 at the right end, and -1 at the left end, respectively. In the graphs of S_{12} and S_{21}, the isomorphic direction indicates the magnitude of the reflection coefficient, and the angular direction indicates the phase. Here, the S-parameters were computed from 100 kHz to 1 GHz.

IV. Signal Flow Model for IGBT

A small-signal equivalent circuit was introduced to analyze the oscillation conditions. High-side diodes D_1 and L_m can be considered to be shorted during SC type II. The gate voltage source V_{Drive} can be replaced by its source impedance Z_s and small-signal source V_s. Based on assumptions, C_{DC} can ignore its impedance in the frequency range where oscillation phenomena occur. The chopper circuit shown in Fig. 1 can be transformed into an equivalent small-signal circuit, as shown in Fig. 6(a). $\hat{S}$ is defined as the S-parameter in the area enclosed by the dotted black line in Fig. 6(a). The overall S-parameter is calculated based on the S-parameter of the IGBT and parasitic elements of the circuit. The details of this method are described in [10].



(a) Equivalent small-signal circuit



(b) Equivalent signal flow graph

Fig. 6 Simplified equivalent circuit and equivalent signal flow graph.

Fig. 6(b) shows the signal flow graph in Fig. 6(a). b_s is the input signal. a_1, b_1, a_2, and b_2 are the power waves defined as follows:

$$a_n = \frac{1}{2\sqrt{Z_0}}(V_n + Z_0 I_n), \quad (1)$$

$$b_n = \frac{1}{2\sqrt{Z_0}}(V_n - Z_0 I_n), \quad (2)$$

where index n refers to either port number 1 or 2. Z_0 is the characteristic impedance. Here, Z_0 was set to 50 Ω. The oscillation conditions were not influenced by this assumption. The S-parameter is defined as follows:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix},$$

$$S_{ii} = \frac{b_i}{a_i}\Big|_{a_k=0, k=1,2, k\neq i},$$

$$S_{ij} = \frac{b_j}{a_i}\Big|_{a_k=0, k=1,2, k\neq i}.$$

Here, Γ_L and Γ_S are the input and load reflection coefficients, respectively.

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0},$$

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0},$$

where Z_L and Z_S are the impedances of the signal source and the load, respectively. Their impedances are expressed as $Z_S = i\omega L_G$ and $Z_L = i\omega L_{DC}$, respectively.

Using the signal flow graph analysis technique [10], Γ_{in} can be written as

$$\Gamma_L = \frac{a_1}{b_1} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}.$$

The transfer function b_1/b_s is expressed as follows [10]:

$$\frac{b_1}{b_s} = \frac{\Gamma_{in}}{1 - \Gamma_S \Gamma_{in}}.$$

The oscillation condition can be evaluated using the loop gain [9]. This is expressed as follows:

$$1 - \left(S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right)\Gamma_S = 0$$

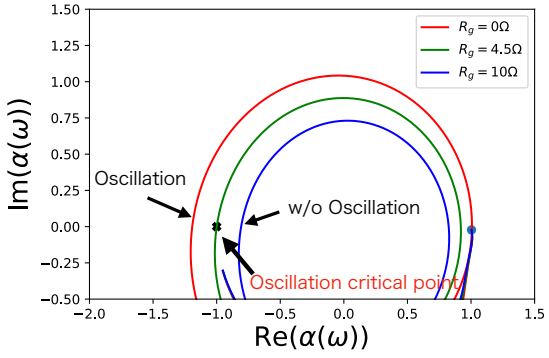


Fig. 7 Gate resistance dependence of the Nyquist plot of α(ω) when V_c = 100 V and V_g = 20 V.

The Nyquist stability condition was used to compute oscillation conditions. The oscillation condition factor is introduced as

$$\alpha(\omega) = -\left(S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right)\Gamma_S.$$

V. OSCILLATION CONDITION ANALYSIS

The dependence of the critical gate resistance on the collector voltage to suppress the oscillation was calculated using the Nyquist stability criterion with the oscillation condition factor α(ω) and compared with the experimental results.

Fig. 7 shows the gate-resistance dependence of the Nyquist plot of α(ω). The S-parameter of the IGBT was calculated at V_c = 100 V and V_g = 15 V using the TCAD simulation. Since this system is a second-order or higher system, it can have an oscillating solution depending on the circuit parameters. With an increase in resistance from 0.0 Ω to 10 Ω, the intersection of

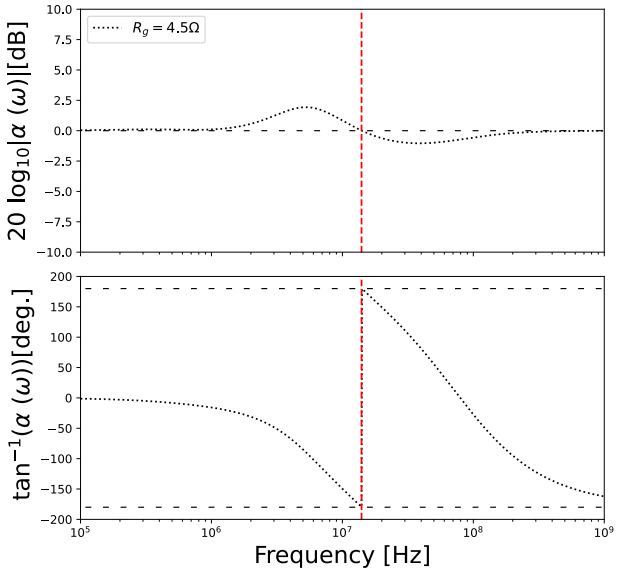


Fig. 8 Bode diagram of the oscillation factor α(ω). The phase and gain of the loop gain are -180° and 0 db respectively when R_g = 4.5 Ω.

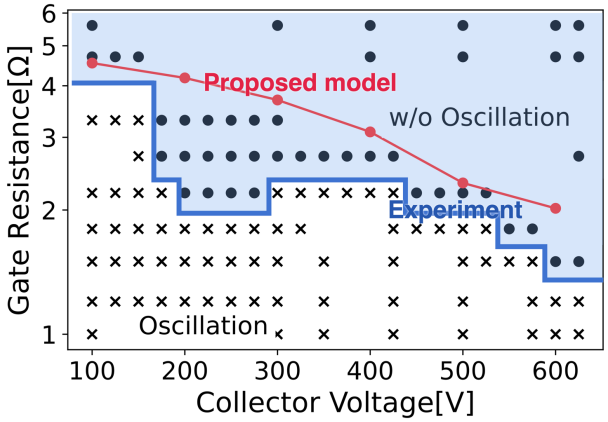


Fig. 9 Calculated drain voltage dependence of the critical gate resistance for oscillation suppression.

the plotted line and the imaginary axis moves from the left to the right of (−1, 0j). The intersection represents the loop gain intensity. Fig. 8 shows the Bode diagram of the oscillation factor α(ω). The upper and bottom figures show the loop gain and phase when R_g = 4.5 Ω. The loop gain becomes 1 at the frequency in which the phase shift becomes -180°. Thus, oscillation is suppressed when the intersection is to the right of (−1, 0j).

Fig. 9 shows the calculated collector-voltage dependence of the gate resistance to suppress oscillations. The gate resistance decreases as the collector voltage increases. These results are consistent with the experimental results.

VI. ANALYSIS OF OSCILLATION MECHANISM

The origin of oscillation suppression during SC type II at higher collector voltages is discussed in this section.

Figs. 10 and 11 show the electric field and carrier distribution during SC type II calculated using the TCAD simulation when V_c = 100 V and 600 V, respectively. In Fig. 10, the dotted and solid lines indicate the electric fields when V_c = 100 V and 600 V, respectively. In Fig. 11, the solid and dotted lines indicate the electron and hole distributions, respectively. The cut-out position was at the right end of the cross-sectional view of the device, as shown in Fig. 4. Conductivity modulation is induced by hole injection from the collector side.

When V_c is 100 V, a region exists where the carrier density decreases up to approximately 30 μm from the junction surface.

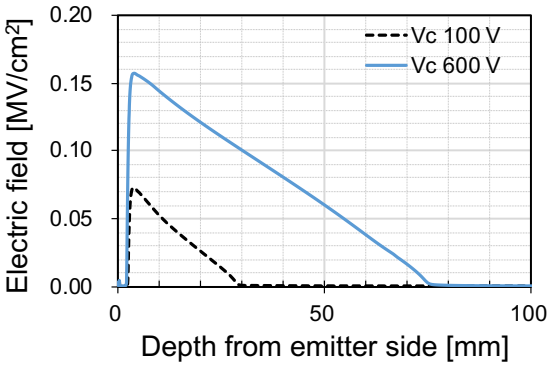


Fig. 10 Electric field distribution during SC type II when V_c = 100 V and 600 V.

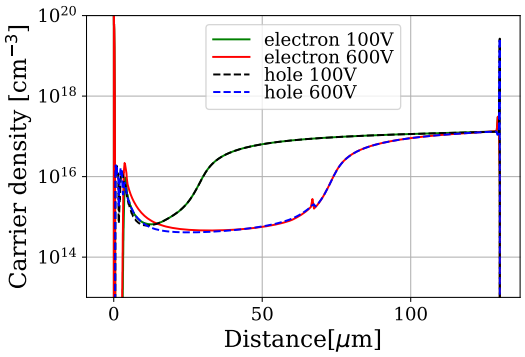
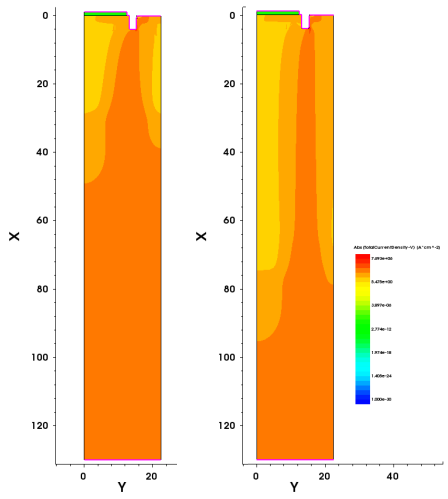


Fig. 11 Carrier density distribution during SC type II when V_c = 100 V and 600 V.



V_c = 100 V V_c = 600 V

Fig. 12 Current density distribution when V_c = 100 V and 600 V.

This carrier distribution indicates that the electron-hole plasma from the device surface to 30 μm was swept out when V_c = 100 V. As observed in the electric field distribution in Fig. 10, the electric field increases and exhibits a triangular shape in this region.

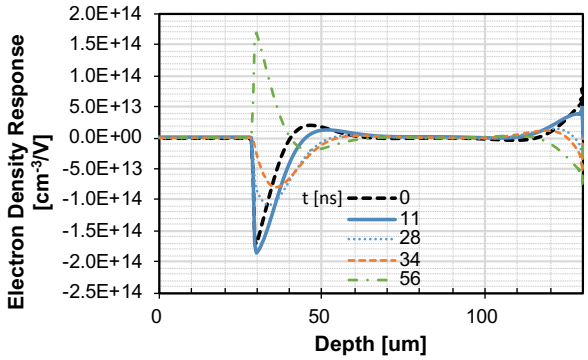
This region with a high electric field intensity increases to 70 μm by increasing the collector voltage to 600 V, as shown in Fig. 10. The maximum electric field was not higher than the critical electric field of silicon. Therefore, this oscillation is not caused by the carrier generation mechanism of impact ionization, as in the IMPATT oscillation.

Fig. 12 shows the current density distribution during SC type II using the TCAD simulation when V_c = 100 V and 600 V. The current flows from the collector side through the floating p-region and trench channel to the emitter. A narrowing of the current occurs in the high electric field region, and its width becomes narrower as the collector voltage increases.

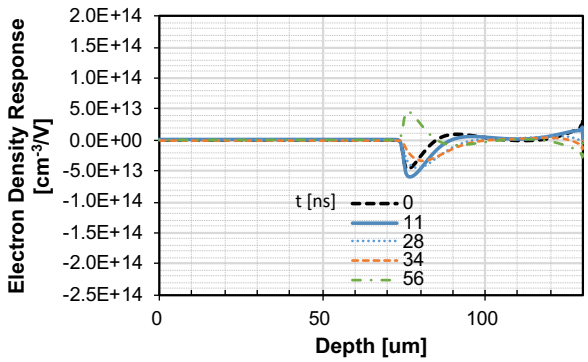
In the TCAD simulator, ξ_{total} is expressed using DC and AC components [16]. The AC response ξ to the external field is defined as follows:

$$\xi_{total} = \xi_{DC} + \xi_{AC} = \xi_{DC} + \xi e^{i\omega t}.$$

Fig. 13 shows the time dependence of electron density response calculated from $\xi e^{i\omega t}$ of the electron density response at 8.9 MHz when V_c =100 V and 600 V. It shows the time response for half of the oscillation period. The cut-out position is the right end of the device shown in Fig. 4. The carrier density response at the boundary of the plasma region is high under each voltage condition. The carrier density responses were high on the collector side, and were greater at 100 V than at 600 V. Therefore, in the oscillatory state, an increase or decrease in the thickness of the high-electric-field region is propagated as a modulation of the carrier concentration at the edge of the electron-hole plasma region.



(a) V_c = 100 V



(b) V_c = 600 V

Fig. 13 Calculated time dependence of electron density responses when V_c =100 V and V_c =600 V.

Fig. 14 shows the derivative of the electric potential response. This can be considered as the response of the electric field. The time dependence of the electric field calculated from the real and imaginary parts of the electric-field response shown in Fig. 14 is shown in Figs. 15 and 16. When the collector voltage was 100 V, the response of the electric field was quadrangular, rather than triangular. The width of the high-electric-field region decreased more when the collector voltage was 100 V than when it was 600 V. When the collector voltage was 600 V, the electric field response remained small because

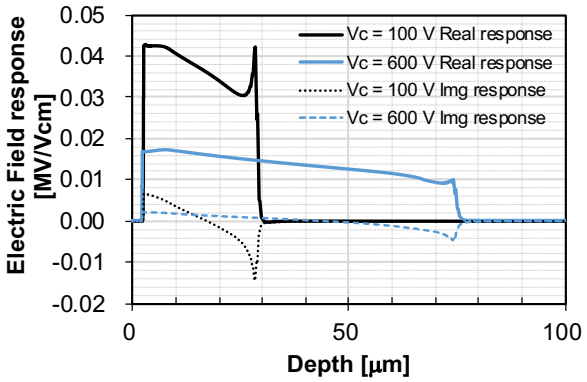


Fig. 14 Electric field responses for collector voltages calculated by the derivation of the potential response when V_c = 100 V and 600 V.

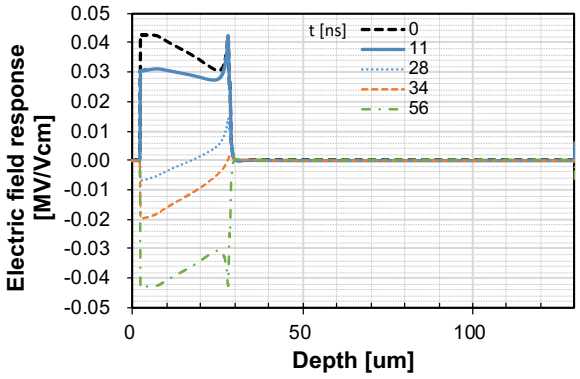


Fig. 15 Electric field time dependences for collector voltages when V_c

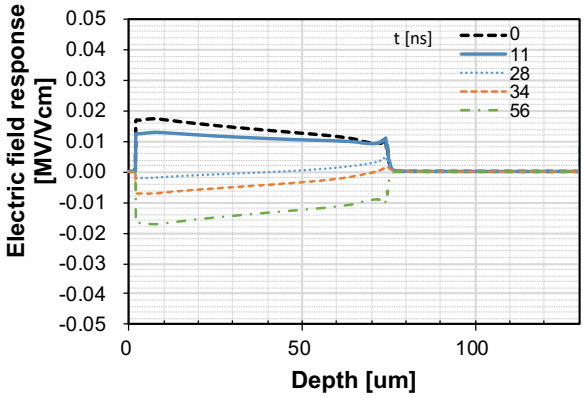


Fig. 16 Electric field time dependences for collector voltages when V_c

of the width of the high-electric-field region. These periodic modulations of electron-hole plasma density and electric field intensity have been reported in previous studies using TCAD mixed-mode simulations [5,6]. Our proposed method can take into account the internal device behavior without using mixed-mode simulation.

As earlier mentioned, the electron-hole plasma contributes to the oscillation in response to the external field; the carrier density and electric field distribution response to the external

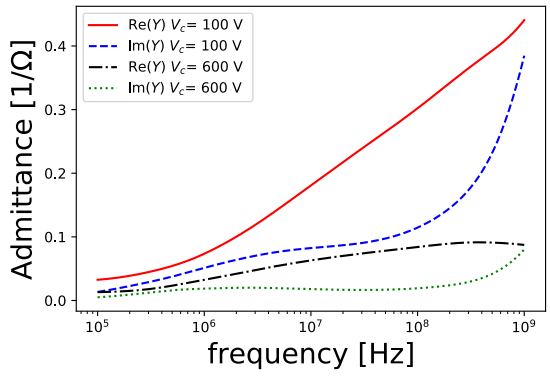


Fig. 17 Admittance matrix dependences for collector voltages when V_c = 100 V and 600 V. Red and blue lines indicate real and imaginal parts of admittance when V_c =100 V, respectively. Black and green lines indicate real and imaginal parts of admittance when V_c = 600 V, respectively.

field reduces when a higher voltage is applied. In the oscillation state, the current response to the external field depends on the carrier density, electric field, and carrier mobility, which in turn depend on the electric field distribution. TCAD simulation can simultaneously calculate these effects as a Y-parameter. Fig. 17 shows the frequency dependence of the Y-parameter from collector to collector for V_c = 100 V and V_c = 600 V. The frequency response at lower voltages is greater than that at higher voltages.

The effect of the combination of the internal state of the device and circuit parameters on the oscillation will be discussed. Thus, the effects of L_E, L_C, and L_G on oscillation conditions were calculated. Fig. 18 shows the L_E and L_C dependences of the critical gate resistance calculated using α(ω). Here, the values listed in Table I are used for the other parameters. Based on the calculation results, there is an area with a high critical gate resistance in the region where L_E is less than 1 nH and the critical gate resistance in this region decreases as L_C increases. Fig. 19 shows an enlarged view of this region with a small L_E, according to which the circuit becomes unstable around L_c = 20 nH and gradually stabilizes at larger values of L_c when L_E =0 nH.

Some studies show that smaller emitter inductance tends

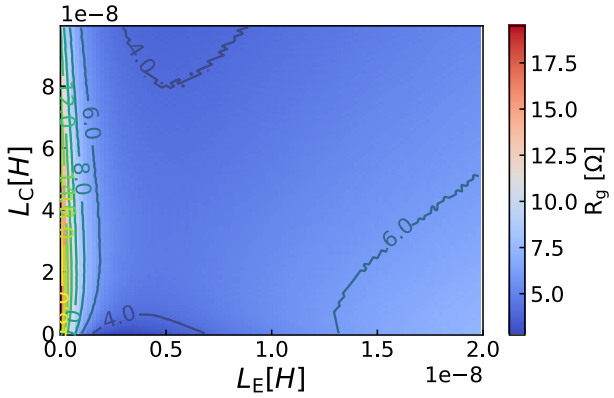


Fig. 18 L_E and L_C dependence of the critical gate resistance calculated using α(w). The values listed in Table I are used for the other parameters.

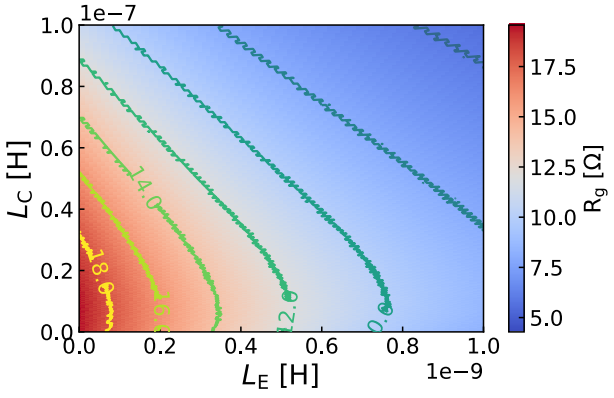


Fig. 19 Magnified view of the region with small L_E and L_C in Fig. 17. The values listed in Table I are used for the other parameters.

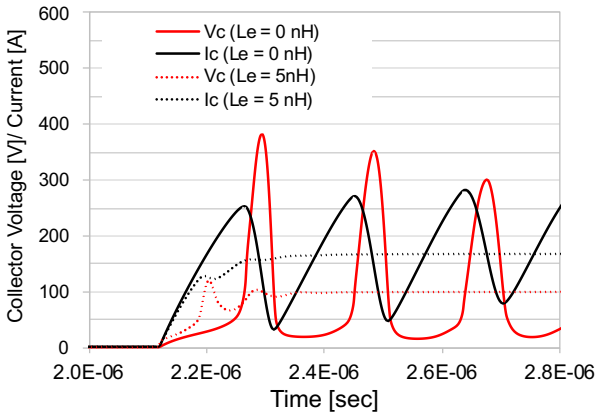


Fig. 20 TCAD simulated switching waveforms of the IGBT during the SC type II. The short-circuit event starts at 2.1 μsec. The red and black line indicate the collector voltage and current. The solid and dotted line means L_E = 0 nH and 5 nH, respectively. The gate resistance was set as 10 Ω. The values listed in Table I are used for the other parameters.

to suppress oscillation during switching operation [10, 17], however, this result suggests that there is a parameter region where oscillation is suppressed when emitter inductance is increased. This was validated by using TCAD mixed-mode simulation. Fig. 20 shows TCAD simulated switching waveforms of the IGBT during the SC type II. The short-circuit event starts at 2.1 μsec. The red and black line indicate the collector voltage and current. The solid and dotted line means L_E = 0 nH and 5 nH, respectively. The gate resistance was set as 10 Ω. The values listed in Table I are used for the other parameters. When L_E = 5 nH, no oscillation phenomenon occurs during SC type II. On the other hand, when L_E = 0 nH, oscillation occurs due to SC type II. As expected by the proposed method, it is confirmed that oscillation can be suppressed by increasing L_E in a certain parameter region. In general, L_E can work as a high-frequency filter and provide feedback to the gate loop with respect to the current in the main circuit. It is considered that larger L_E suppresses the gain of the oscillation mode.

Fig. 21 shows L_E and L_G dependence of the critical gate

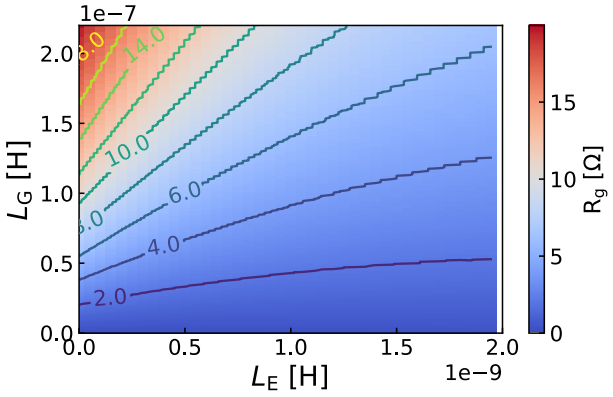


Fig. 21 L_E and L_G dependence of the critical gate resistance calculated using α(w). The values listed in Table I are used for the other parameters.

resistance calculated using $\alpha(\omega)$. When L_E is zero, the critical gate resistance increases as L_G increases. When L_G was held constant, the critical gate resistance decreased as L_E increased, and the circuit stabilized as L_E increased.

The relationship between L_E, L_G, L_C, and the critical gate resistance indicates that a small emitter inductance destabilized the circuit; therefore, setting the emitter inductance value to an appropriate value is important for circuit stabilization. For circuit stabilization, increasing L_E rather than L_C can suppress the oscillation while minimizing the increase in the main circuit inductance. However, as the gate inductance L_G is increased, the critical gate resistance increases and oscillation is more likely to occur. Therefore, the gate inductance should be maintained as small as possible.

VII. SUMMARY

The oscillation phenomenon of trench-type IGBTs during short-circuit type II was investigated experimentally. The oscillation during the short-circuit operation can be suppressed by increasing the gate resistance. The resistance required for oscillation suppression decreases with an increase in the collector voltage.

The oscillation conditions were calculated from the signal flow graph using the S-parameter of the trench-type IGBT based on TCAD simulation. The calculation results reproduced the locus of the collector voltage dependence of the gate resistance required to suppress oscillations. The proposed method can be used to evaluate the oscillation condition depending on the collector voltage and gate resistance through a simple calculation using a signal flow method and the S-parameters computed using TCAD device simulation.

The internal state of the device during oscillation was investigated using a TCAD simulation. It was found that a high-electric-field region is formed at the base-drift layer boundary, and the effect of the modulation of the electron and hole-density-discharged carriers is transmitted to the collector side through the electron-hole plasma region during the oscillation. Moreover, the carrier response was higher at low collector voltages, where the depth of this region was smaller than that at high collector voltages with large depth. These results suggest that the transfer characteristics of the carrier distribution through the carrier discharge region and the electron-hole plasma cause the drain voltage dependence of the short-circuit oscillation conditions.

The impact of the stray inductance on the critical gate resistance to suppress oscillation was also evaluated. As L_E decreased, the critical gate resistance decreased. Thus, and an appropriate L_E is important to stabilize the circuit.

As discussed here, the oscillation phenomenon of SC type II is caused by the distribution of electron and hole plasma inside the device. The response of the electric field inside the device to the external voltage, and circuit parasitic parameters are critical in the oscillation conditions. Therefore, a method to simultaneously handle the internal device conditions and circuit stability is necessary to understand such oscillation phenomena and design a stable circuit. Our proposed method addresses these requirements and is considered useful for the design of power electronics systems.

REFERENCES

[1] P. Diaz Reigosa, R. Wu, F. Iannuzzo and F. Blaabjerg, "Evidence of Gate Voltage Oscillations during Short Circuit of Commercial 1.7 kV / 1 kA IGBT Power Modules," in *Proc. PCIM Europe 2015*, 2015, pp. 1-8.

[2] U. Grossner, B. Kakarla, T. Ziemann, J. Muting, R. Stark, and Kovacevic-Badstuebner, I. "Requirements for highly accurate multiphysics modeling of SiC power MOSFETs and power modules," *ECS Transactions*, 80(7) 89-100, 2017.

[3] J. Lutz, R. Dobler, J. Mari and M. Menzel, "Short circuit III in high power IGBTs," in *Proc. 13th European Conference on Power Electronics and Applications*, 2009, pp. 1-8.

[4] E. Velander et al., "Analysis of short circuit type II and III of high voltage SiC MOSFETs with fast current source gate drive principle," in Proc. *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 3392-3397.

[5] P. D. Reigosa, F. Iannuzzo, M. Rahimo, C. Corvasce and F. Blaabjerg, "Improving the Short-Circuit Reliability in IGBTs: How to Mitigate Oscillations," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5603-5612, July, 2018.

[6] V. van Treek, H. Schulze, F. Niedernostheide, C. Sandow, R. Baburske and F. Pfirsch, "Influence of doping profiles and chip temperature on short-circuit oscillations of IGBTs," *in Proc. 30th International Symposium on Power Semiconductor Devices and ICs*, 2018, pp. 108-111.

[7] M. Tsukuda, K. Kawakami and I. Omura, "Scattering parameter approach to power MOSFET design for EMI," in *Proc. 24th International Symposium on Power Semiconductor Devices and ICs*, 2012, pp. 181-184.

[8] T. Liu, T. T. Y. Wong and Z. J. Shen, "A New Characterization Technique for Extracting Parasitic Inductances of SiC Power MOSFETs in Discrete and Module Packages Based on Two-Port S-Parameters Measurement," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9819-9833, Nov. 2018.

[9] C. Abbate, G. Busatto, F. Iannuzzo, C. Ronsisvalle, A. Sanseverino, and F. Velardi, "Scattering parameter approach applied to the stability analysis of power IGBTs in short circuit," Microelectronics Reliability, 53(9-11), 1707-1712, 2013.

[10] H. Kono and I. Omura, "Study of parasitic oscillation of a multi-chip SiC MOSFET circuit based on a signal flow graph model by TCAD simulation," *Solid-State Electronics*, vol. 177, p. 107884, 2021.

[11] H. Kono and I. Omura, "A Study of a parasitic oscillation of trench IGBT in short-circuit mode based on signal flow graph model," in *Proc. 12th International Conference on Integrated Power Electronics Systems (CIPS 2022)*, Berlin/Germany, March 15 – 17 2022, pp. 487-492.

[12] T. Laska, M. Munzer, F. Pfirsch, C. Schaeffer and T. Schmidt, "The Field Stop IGBT (FS IGBT). A new power device concept with a great improvement potential," in *Proc. 12th International Symposium on Power Semiconductor Devices & ICs. Proceedings*, 2000, pp. 355-358.

[13] T. Laska, G. Miller, M. Pfaffenlehner, P. Turkes, D. Berger, B. Gutsmann, P. Kanschat, and M. Munzer, "Short circuit properties of Trench-/Field-Stop-IGBTs-design aspects for a superior robustness," in *Proc. IEEE 15th International Symposium on Power Semiconductor Devices and ICs*, 2003, pp. 152-155.

[14] Y. Chen, H. Luo, W. Li, X. He, F. Iannuzzo and F. Blaabjerg, "Analytical and Experimental Investigation on A Dynamic Thermo-Sensitive Electrical Parameter With Maximum dI_C/dt During Turn-off for High Power Trench Gate/Field-Stop IGBT Modules," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6394-6404, Aug. 2017.

[15] IGW08T120 datasheet rev.2.6, Infineon Technology, 2009.

[16] Sentaurus Device User Guide, Version L-2016.03, Synopsys, Mountain View, CA, USA, March. 2016.

[17] K. Saito, T. Miyoshi, D. Kawase, S. Hayakawa, T. Masuda and Y. Sasajima, "Simplified Model Analysis of Self-Excited Oscillation and Its Suppression in a High-Voltage Common Package for Si-IGBT and SiC-MOS," IEEE Transactions on Electron Devices, vol. 65, no. 3, pp. 1063-1071, 2018.