Speed-Up Gate Pulse Method to Suppress Switching Loss and Surge Voltage for MOS Gate Power Devices

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***Abstract*—There is a trade-off between surge voltage and switching loss in power semiconductors, and it has been difficult to reduce both. In order to solve this problem, the digital gate drive method has been studied. However, the digital gate drive method has the problem that the gate drive circuit is complicated and it takes time to search for the optimal drive waveform. In this study, we have proposed a new method that does not require optimization search, but only adds a simple circuit, which is expected to have the same effect as the digital gate drive method.**

Keywords—Trade-off, surge voltage, switching loss

I. INTRODUCTION

A power semiconductor device operates at high frequency, switching loss need to be reduced and thus surge voltage increased. If the surge voltage is suppressed, on the other hand, the switching loss increases since the switching loss and surge voltage are under the trade-off relation. To improve the trade-off, many research results have been reported, specially, those on digitally controlled gate drive technology. Although the digitally controlled gate drives show significant improvement of the tradeoff, they need to repeat substantially large number of experiments and/or simulations to find the optimum gate waveform [1-8]. Therefore, simple and low-cost method to improve the trade-off between switching loss and drain surge voltage has been required. In the present research the authors demonstrated a simple yet efficient gate drive method to improve the trade-off by reducing both turn-off loss and surge voltage, without optimization process.

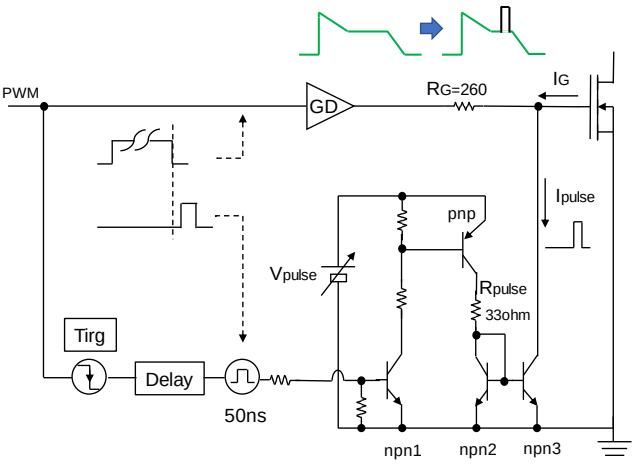
II. SPPED-UP GATE PULSE METHOD

A. *Advantage of the proposed method*

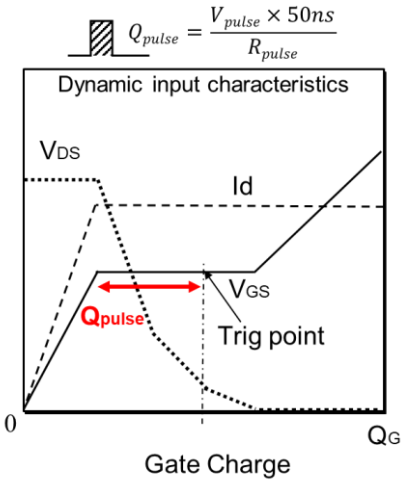
A new gate drive method was proposed. In the method, predetermined short pulse current discharges the gate capacitance and enhance the switching speed during Miller period without affecting surge voltage. The method is simple yet efficient to improve the trade-off between switching loss and surge voltage. Furthermore, the pulse condition is determined from the datasheet or a simple one-time switching test.

B. *Speed-Up Gate Pulse circuit for demonstration*

We have fabricated a speed-up pulse circuit that can be used for various MOS gated power semiconductors including IGBT and SiC-MOSFET with different ratings. The schematics of the proposed method is shown Fig. 1 (a). The amount of charge to be discharged was determined by the pulse circuit voltage V_{pulse} and pulse width (50ns for this demonstration). The speed-up pulse circuit uses a current mirror circuit and consists of two npn transistors and one pnp transistor. The circuit is very simple and can be connected to the device terminals without any change of the original gate drive circuit. The speed-up pulse circuit is used to discharge the gate charge instantaneously during the turn-off of the power semiconductor. The amount of discharge was ~20% of total charge which corresponds to the gate charge during the drain voltage rise time (Q_{pulse}) as shown in Fig. 1 (b). Since the speed-up factor is based on the gate Miller charge, the speed-up pulse trigger timing and the charge is determined from the dynamic input characteristics curve shown on the data sheet of the power MOSFET / IGBT and the method does not require any optimization process such as the simulated annealing or the particle swarm optimization methods with long experiment and computing time to search an optimum gate pulse patterns as often required in digitally controlled gate drivers.



(a) Speed-up gate pulse circuit and SiC-MOSFET (SCT3030AL) .



(b) Dynamic input characteristics

Fig.1 Speed-up circuit and dynamic input characteristics

The speed-up gate pulse circuit works as follows. The square wave triggered by turn-on pulse or gate waveform turns on Tr. npn1 and turns on Tr. pnp. At the same time, Tr. npn2 and Tr. npn3 are turned on and the gate charge is discharged from the gate. Tr. npn2 and Tr. npn3 have the same amount of current flowing through them and the amount of discharged gate charge is simply determined by R_{pulse}, V_{pulse} and the pulse width. The circuit is built on a universal board with bipolar transistors of low cost general purpose products. The speed-up pulse timing can be changed by the delay.

III. EXPERIMENTAL RESULTS

A. *Trade-off for comparison*

The trade-off curve comparison with / without a speed-up gate pulse circuit is analyzed. The amount of discharged gate charge is setted to be 21nC, the pulse width is fixed at 50ns, and the switching waveform is obtained by changing the pulse timing by the delay. As the pulse timing delay became longer, the switching loss was reduced by 57% (3.015mJ to 1.295mJ) while suppressing the surge voltage. Figure 2 shows the actual waveforms compared with the trade-off curves. If the speed-up pulse waveform discharges the gate charge at the timing of the fall of the drain current, the surge voltage increases (corresponding points (E) and (D), see also Fig. 4). From this analysis, it is possible to reduce the switching loss to the maximum extent by discharging the gate charge at the timing before the drain current falls. Therefore, the optimum delay and pulse charge can be determined from "dynamic input characteristic curves provided from the suppliers or obtained by a simple switching test.

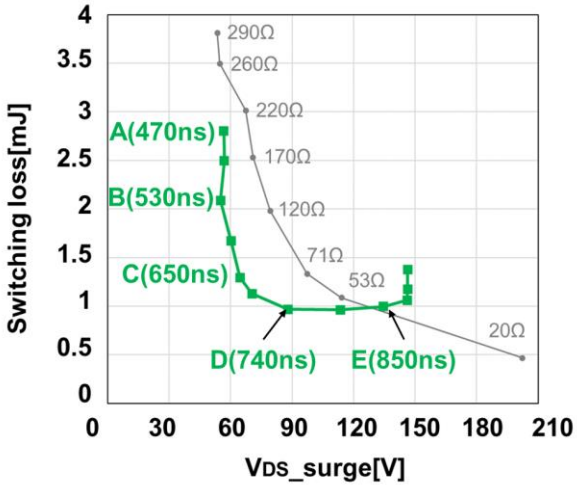


Fig. 2 Trade-off curve analysis results

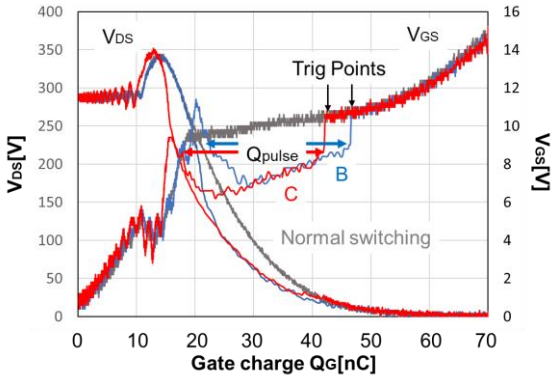


Fig. 3 Dynamic Input Characteristics obtained by a simple switching test.

Loci of V_{GS}-Q_G and V_{DS}-Q_G for turn-off without pulse (normal switching), timing (B) and (C) are shown in Fig. 3. Triggering points are shown as well. Precise pulse timing and the charge can be determined by experimentally obtained Loci instead of "Dynamic input characteristic" in the datasheet or a simple switching test. Fig. 4 shows waveforms for different pulse timings corresponding to the points (A)~(E) in Fig. 2.

B. *Trade-off curves for different pulse charges*

Figure 5 summarized the trade-off curves for different amounts of pulse charge obtained by changing pulse delay time. In case of small pulse charge, the effect to the loss

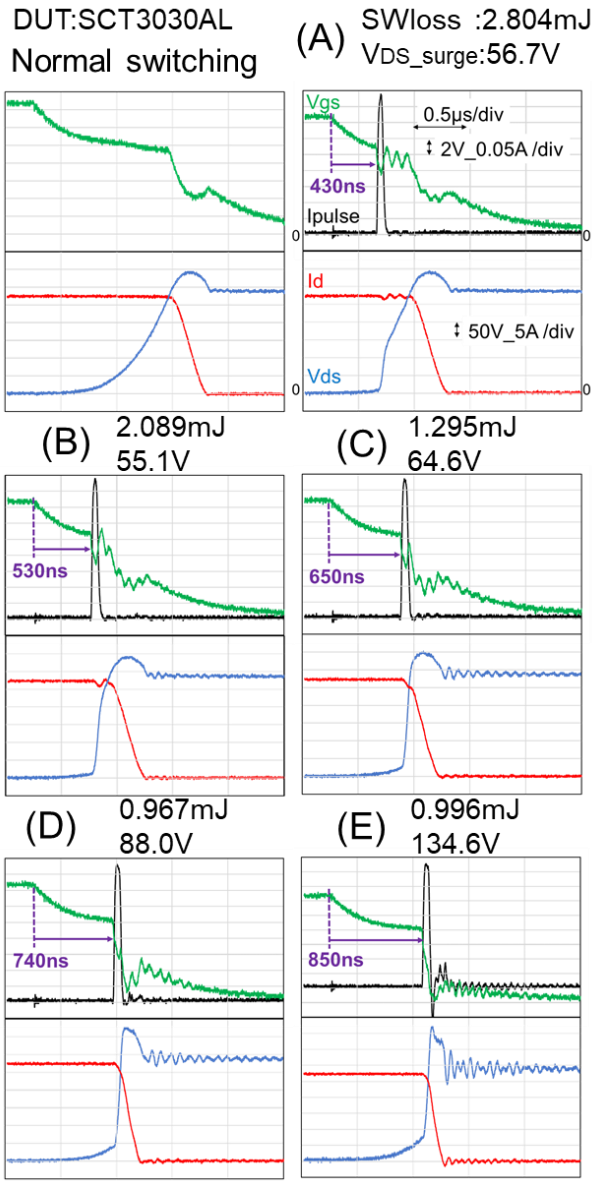


Fig. 4 Switching waveforms for different pulse timings.

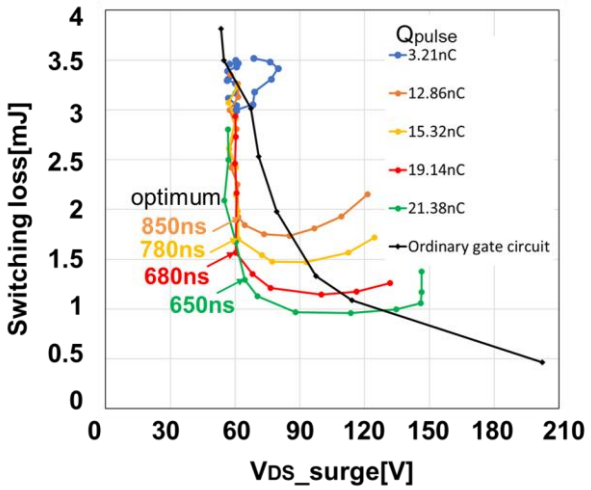


Fig. 5 Trade-off curve analysis when varying the discharge charge.

reduction was limited since the amount of charge was not sufficient to reduce the V_{DS} raise time. The total amount of gate charge Q_G was 70-80 nC (Fig. 4), and if more than 25% of the total charge is discharged by the proposed speed-up pulse metho, the improvement rate of switching loss will achieve more than 50%. Thus, the pulse input timing can be calculated from the dynamic input characteristics based on the amount of discharge charge.

IV. TRADE-OFF BY CHANGING Q_{PULSE}

A trade-off analysis was performed by fixing the pulse timing input (delay=0s) and varying only the discharge charge amount. The pulse timing is set at the start of turn-off. At this time, the pulse width was set to 100ns and changed the pulse current. By discharging the gate charge until the drain current falls, it was demonstrated that the switching loss is reduced by 56.2% while suppressing the surge voltage. The test results are shown in Fig. 6.

At a discharge charge of 21nC, we were able to achieve the loss reduction equivalent to the trade-off curve by

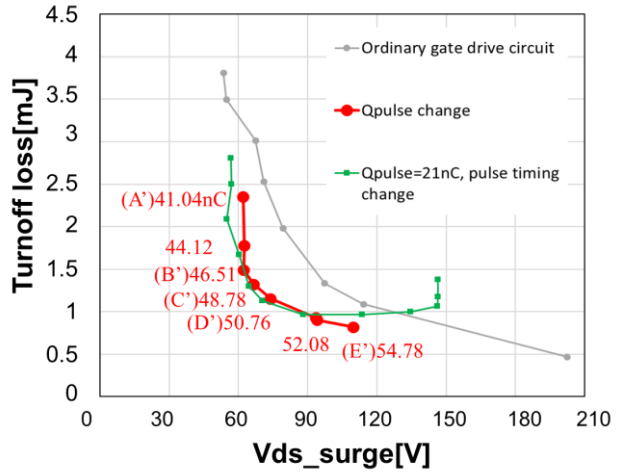


Fig. 6 Tray-off curve analysis when pulse timing is fixed.

varying the pulse timing shown in Fig. 2. In addition, since it does not require pulse timing delay adjustment, we believe that it can be easily applied practical cases.

As the amount of discharged charge is increased, the surge voltage increases because it affects the fall speed of the drain current (see point (E')). The actual switching waveform is shown in Fig. 7 at point (C'), where the switching loss is reduced while suppressing the surge voltage. At point (E'), the amount of discharge charge is too large, which affects the fall of the drain current and increases the surge voltage, so it is necessary to calculate the optimal amount of discharge charge. The optimal amount of discharge charge can be simply determined by using the dynamic input characteristics. By calculating the gate charge until the drain current falls from the dynamic input characteristics, and then discharging that gate charge with the speed-up gate pulse circuit, it is possible to suppress the increase in surge voltage and reduce switching loss without affecting the fall of the drain current (see Figure 8).

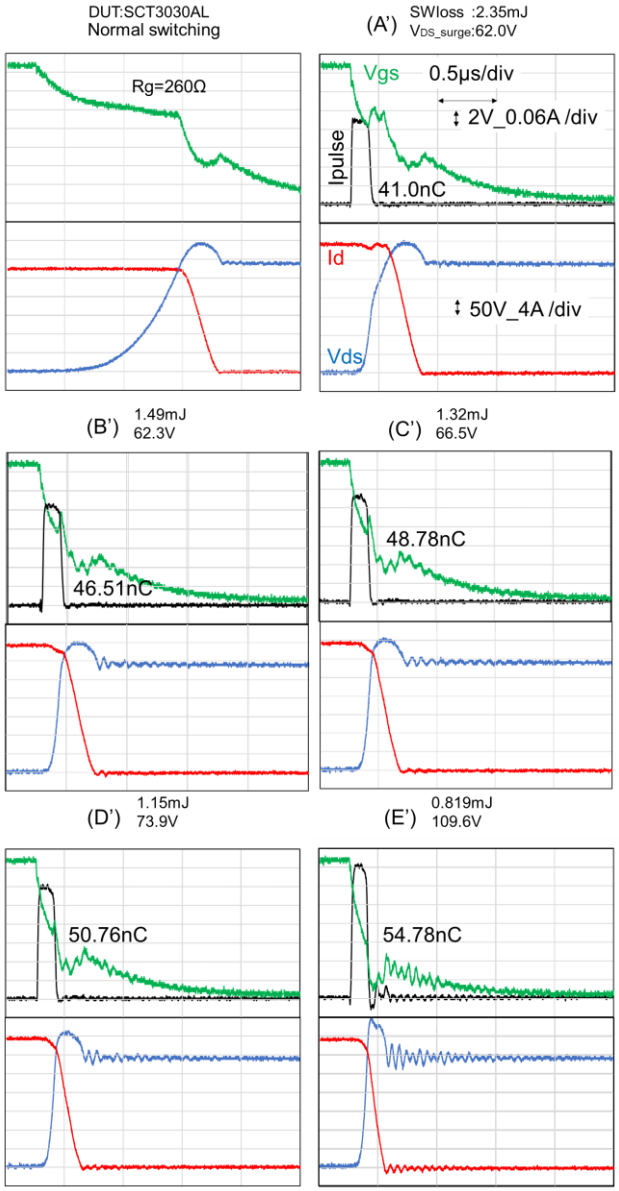


Fig. 7 Each switching waveform when pulse width is fixed

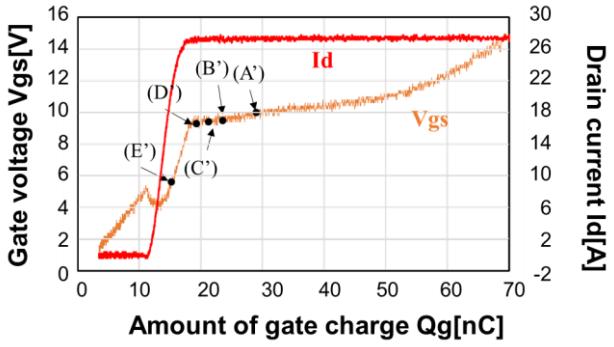


Fig. 8 Dynamic input characteristics (relationship between Vgs, Id, and Qg)

V. Q_{PULSE} SETTING FOR DIFFERENT DRAIN CURRENT CONDITION

In previous sections, the drains switching current has been fixed. Here we consider the different switching current cases since the switching current changes according to output current waveform of inverters. Basically, the simplest method is that the amount of discharege charge should be set under maximum switching current since the major swithching loss is generated at the high current switching condition. As shown in Fig. 9, for lower drain current condition, the optimal amount of discharge charge becomes larger, which means the pre-determined Qpulse will not induce high surge voltages.

VI. CONCLUSION

As described above, we were able to reduce power dissipation by simply connecting the speed-up gate pulse circuit to the general gate drive circuit. When the pulse timing and the amount of discharge charge of the gate charge were optimized, a 57% reduction in power dissipation was achieved. When the pulse timing was fixed and only the amount of gate charge discharge was optimized, the loss was reduced by 56.2%. The optimal amount of discharge charge can be calculated from the dynamic input characteristics provided by the supplier. This technique contributes to the reduction of power semiconductor losses.

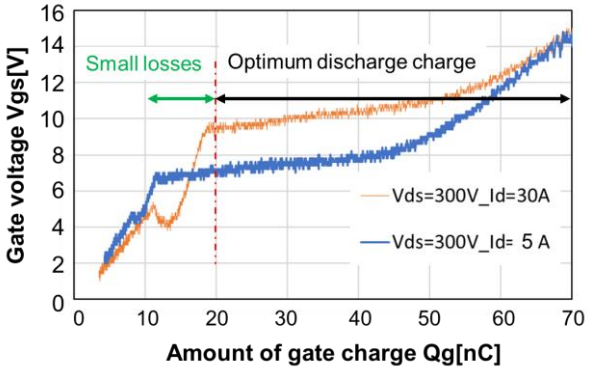


Figure 9 Dynamic input characteristics when the drain current changes

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