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Etching Process Module Development for SiC CMOS

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Materials Science

by

Weston Reed Renfrow
Missouri State University
Bachelor of Science in Physics/Engineering & Applied Physics, 2019

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University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

____
H. Alan Mantooth, Ph.D.
Dissertation Director

____
Zhong Chen, Ph.D.
Committee Member

____
Greg Salamo, Ph.D.
Committee Member

____
Matthew Leftwich, Ph.D.
Ex-Officio Member

The following signatories attest that all software used in this thesis was legally licensed for use by Weston Renfrow for research purposes and publication.

___________________________________ ___________________________________

Mr. Weston Renfrow, Student

Dr. H. Alan Mantooth, Thesis Director

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___________________________________ ___________________________________

Dr. Matthew Leftwich, Program Director

Dr. H. Alan Mantooth, Thesis Director

List of Published and Planned Papers Used in this Dissertation

Part of Chapter 1, Chapter 3, and Chapter 4 is planned to be published in:

> "ICP Etching of Intrinsic and Doped SiC With Chlorine-Based Gas Compositions"
> Renfrow R., Di Mauro A., Rice T., Chen K, Mantooth H. A., Chen Z., (2022)

Abstract

Silicon Carbide (SiC) is an exciting material that is growing in popularity for having qualities that make it a helpful semiconductor in extreme environments where silicon devices fail. The development of a SiC CMOS is in its infancy. There are many improvements that need to be made to develop this technology further. Photolithography is the most significant bottleneck in the etching process; it was studied and improved upon. Etching SiC can be a challenge with its reinforced crystal structure. Chlorine-based inductively coupled plasma (ICP) etching of intrinsic SiC and doped SiC, SiO_2, and Silicon has been studied. A baseline chlorine gas recipe containing Cl_2 and BCl_3 was studied and characterized. The average SiC etch rate of this recipe was found to be 1330 Å/min. The Cl_2 concentration was then varied to over five total experimental recipes. The results show that Cl-based gas produces little change in etch rates between intrinsic SiC and doped SiC except for the recipe containing 66% Cl_2. This recipe provided etch rates that were proportional to doping concentration but independent of the dopant species. These results also showed a high critical dimension bias due to sidewall passivation. Buffered oxide etching (BOE) was conducted on SiO_2 for the purposed of etching field oxide, gate oxide, and hardmasks. The studies of BOE were inconsistent with the results found in the literature. Instead, an ICP method and a liftoff method was used on SiO_2 as an alternative. Results from this study found that the desired SiO_2 etching can be achieved without the use of BOE, which can be hazardous. The ICP etch rate of SiO_2 was 1006 Å/min. Both ICP and liftoff had higher quality pattern transfer than BOE. The future works of these results have also been described.

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I would like to thank the members of my research group, Kevin, Tanner, Anthony, and Hayden. They were always there to help me and answer questions when I needed them. I asked too much of them sometimes, yet they were always there to assist me with long days in the lab. Photolithography would have been a nightmare without these men.

Lastly, I would like to thank John Ransom. His fabrication expertise was particularly helpful near the end of my research. He was under no obligation to answer my questions, yet our discussions were enlightening and enjoyable.

Dedication

This thesis is dedicated to my parents, Bill and Carol Renfrow. These last two and a half years have been difficult. There have been the highest highs and lowest lows. Their unconditional love and support were the only things I could count on during this time. I owe everything to them.

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Chapter 1. Introduction

In 1906, J. C. Bose patented his design for the first form of radio wave communication. Cat's-whisker crystal radio detectors were the first commercial use of silicon as a semiconductor (Emerson, 1998). The first transistor was invented in 1947 by J. Bardeen, W. Brattain, and W. Shockley at Bell Labs. It was about the size of a thumbnail. Only 50 years later, over 9 million could be made on a single silicon wafer (Cressler, Siliocn Earth, 2009). Silicon is the most common element in the galaxy and the second most common on earth. It makes up over 27% of the earth's crust and is found in rocks and soils. It can also be found naturally in plants and animals (Silicon, n.d.). Silicon has become one of the most important electronic materials on earth for several different reasons: It is cheap, nontoxic, mechanically stable, has good thermal properties, and insulating SiO_2 can easily be grown on silicon substrates. For these reasons, the number of silicon transistors has grown to over ten quintillions in only 70 years since the invention of the first transistor (Cressler, Siliocn Earth, 2009). Silicon may be a miracle material for everyday use on earth, but silicon has limitations when brought to extreme conditions.

There are few conditions that are too harsh for silicon-based electronics. Developing electronics that can function in these harsh environments is essential. Consider satellites that are operating in earth's orbit where there is a high level of radiation, or a spacecraft designed to travel to the surface of Venus where temperatures reach 460°C and pressures of 9.4MPa (Neudeck, et al., 2016). These extreme environments are rare, but electronic devices that can withstand extreme environments are necessary for scientific research and development.

There are many extreme conditions that should be considered when designing electronics. The material used should be able to maintain functionality met with these conditions: high radiation or magnetic fields, high temperatures, low temperatures, and corrosive chemicals.

Radiation can ionize the material or displace the atomic lattice, changing its structure. These environments are common in both earth's orbit and deep space. Communication satellites and spaceships are commonly met with radiation-rich environments.

Commercial operating temperatures for electronics are between 0°C to 85°C. Some commercial applications call for -55°C to 125°C. The material should be able to function well outside those ranges. The surface of Mars can get as low as -143° C and deep space can reach -146°C. The automotive and aerospace industry requires operation at high temperatures up to 300°C on earth, while the surface of Venus can reach up to 600°C (Cressler & Mantooth, Extreme Environment Electronics, 2013). All electronic materials and packaging used in the device should handle these temperatures together without expanding or contracting to the point of destruction.

Consider a chemical sensor that is designed to be ingested by a human. The chemicals in the body are corrosive and can dissolve electronics. The packaging of the device cannot protect it because the sensor must be in contact with the chemical. In this situation, the material in the device must be able to withstand the corrosive material while also being non-toxic (Cressler & Mantooth, Extreme Environment Electronics, 2013). Many of these conditions exist simultaneously in a single environment. The electronic device must be durable to withstand many of these conditions at once. A different material must be used in situations where silicon will not function properly. One material that is gaining interest is Silicon Carbide.

Silicon carbide (SiC) has grown in popularity for being a promising material in high-temperature and extreme environment devices. SiC is a wide bandgap group IV semiconductor material with a low intrinsic carrier concentration compared to silicon. SiC has high thermal conductivity, allowing for quicker heat removal. Having a high drift saturation velocity allows SiC devices to have higher switching speeds with less loss of power. SiC has a higher critical electric field than silicon; therefore, a much higher doping concentration can be achieved. High doping concentrations cause the on-resistance to improve in SiC devices, which means a SiC power device has lower conduction losses and higher efficiency. These properties allow SiC devices to be used in extreme conditions where silicon devices would lose functionality. For relatively short time durations, many SiC devices have been shown to function at temperatures as high as 600°C. Theoretically, SiC devices could function as hot as 800°C (Cressler & Mantooth, Extreme Environment Electronics, 2013). These devices have applications in a wide range of industries, such as aerospace, power generation, and transportation. Although SiC has many unique benefits that make it a suitable material for extreme environment electronics, there are many drawbacks to using SiC.

SiC can be expensive. A single 6-inch wafer of high-quality SiC can cost as much as $1,500 (Kulu, 2020). This can make prototyping SiC power devices a costly endeavor. They are expensive compared to the low price of $2 per square inch of Silicon wafers (Mulay, 2022). SiC can also be a difficult material to work with. SiC is the third hardest composite material in the world. This means SiC requires more energy and higher temperatures during the manufacturing process (Lovati, 2021). This makes it one of the most fragile as well. Silicon carbide wafers shatter easily if not taken care of. SiC is more difficult to etch than other semiconductor materials. Its etch rates are slower, making it too slow for deep etching (Tadjer, et al., 2017).

Most published studies on plasma etching SiC deal with fluorinated gas mixtures such as SF_6, NF_3, CHF3, and CF_4 (Yih & Steckl, 1995; Kim, et al., 2004; Osipov, et al., 2020; Camara & Zekentes, 1959-1963; Tadjer, et al., 2017; Khan & Adesida, 1999; Ozgur & Huff, 2017; Wang, et al., 1998; Ruixue, Yintang, & Ru, 2009; Pan & Steckl, 1990). SiC etching studies using chlorine-based gases, especially Cl_2/BCl_3 mixtures, have been less studied (Ekinci, et al., 2014). This thesis aims to understand the etching mechanisms of SiC with Cl_2/BCl_3 plasmas. This thesis aims to improve the etching process modules involved with SiC CMOS fabrication. These topics include photolithography development, inductively coupled plasma etch characterization, buffered oxide etching, and other methods to etch silicon dioxide.

Chapter 2. Background and Literature Review

Intrinsic semiconductors cannot conduct electricity by themselves. In order for semiconductor devices to function properly, the device must contain a combination of doped semiconductor materials, which are crystals that intentionally have added impurities. N-type semiconductors contain impurities that displace the crystal atoms for new atoms that give the crystal extra electrons. In the case of SiC, nitrogen is used. P-type semiconductors are given impurities that contain holes, which are atoms that can easily take on an additional electron. SiC is given Al. Both electrons and holes are considered charge carriers, meaning both can flow throw the crystal to carry chare, creating an electrical current. Holes are thought of as a moving species, but electrons are the only species that flow. When a P/N junction is formed, the interface between the two materials becomes a depletion region which is a region that lacks charge carriers. Under the right conditions, a doped semiconductor can invert to become the opposite type. A P-type can act like an N-type, for example. This is known as an inversion region (Shroder, 2006).

To understand a SiC CMOS, first, a MOSFET must be understood. A MOSFET, metal-oxide-semiconductor field-effect transistor, can be an N-channel MOSFET (NMOS) or a P-Channel MOSFET (PMOS). An NMOS in enhancement mode is designed with a P-type substrate and two heavily doped N+ regions making up the source and drain terminals. The P/N junction naturally forms the depletion region. Between the two terminals, a layer of oxide and a layer of metal is deposited to form the gate terminal. When a positive voltage greater than the threshold voltage is applied to the gate terminal, a capacitance effect takes place that pushes the holes in the substrate away from the surface. A depletion region is formed that spans both N+ regions. When the source voltage is great enough, an inversion region then spans through the depletion region. Now, electrons can flow through the source terminal to the drain terminal (Bishop, 2020). Figure 2.1 illustrates this.

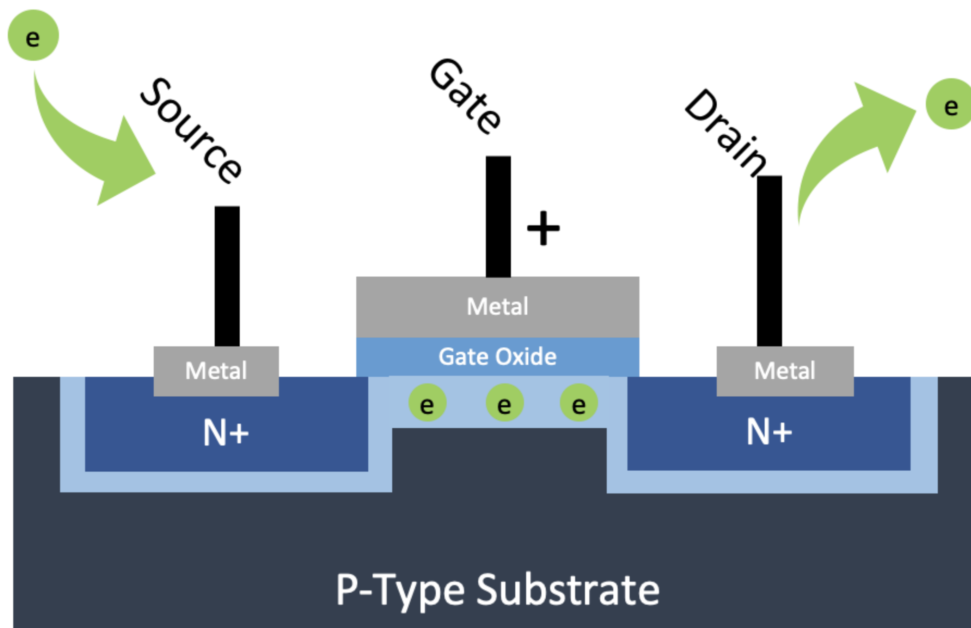


Figure 2.1 NMOS Enhancement Mode

When a positive voltage greater than the threshold voltage is applied to the gate terminal, the current can flow. When there is not a high enough voltage current cannot. This transistor is essentially a switch with no moving parts. Enough transistors organized in specific patterns can be used for digital computations. A PMOS transistor is designed to be the opposite. The gate terminal requires a negative voltage for current to flow, but the charge carriers are holes, not electrons. A CMOS (Complementary MOSFET) is an NMOS and PMOS fabricated together on the same substrate. A CMOS adds body terminals to allow for the capacitance effect in the gate terminals, as well as field oxide to insulate the entire circuit. Figure 2.2 shows the layout of the SiC CMOS.

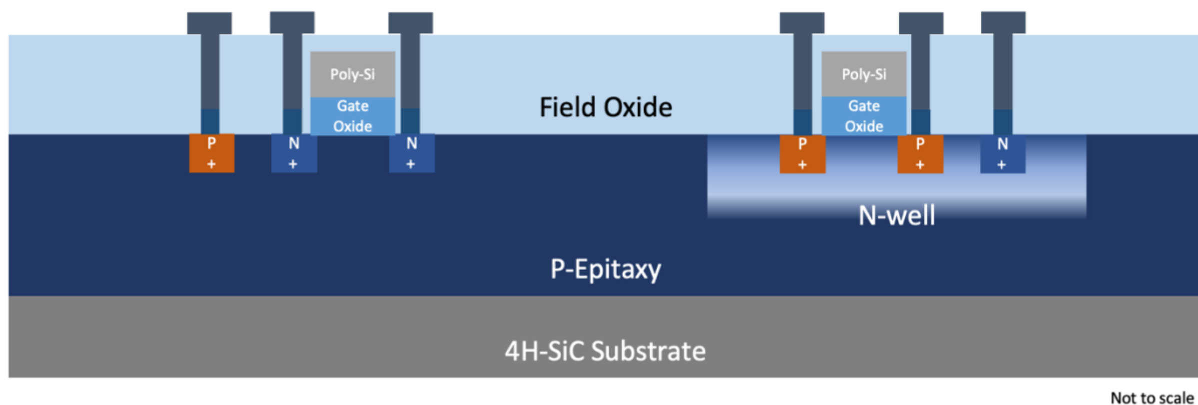


Figure 2.2 SiC CMOS

The fabrication of the SiC CMOS requires various materials to be etched. One example is etching through the field oxide to the surface of the substrate. In an ideal situation, the etch would be perfectly anisotropic and stop at the surface. However, with plasma etching, there is a probability of over-etching to the SiC surface. So, the etch profile of SiC must also be studied. The etching process modules that this thesis will help develop are the photolithography process, the chlorine-based ICP etch recipe characterization, and oxide etching for the purpose of field oxide, gate oxide, and hardmask deposition.

Photolithography is an essential step in semiconductor fabrication. It is repeated between 10 and 40 times in the process of fabricating a single circuit. For large fabs owned by major semiconductor companies, photolithography makes up approximately 30% of the manufacturing cost (Mack, 2007). Photolithography is used for ion implantation, film deposition, and etching. Having an accurate and reliable photolithography process is critical in IC fabrication. Improving this was the first step in developing the etching process modules. The features and resolution of a mask is determined by the photolithography process. A higher resolution allows for smaller feature sizes which can reduce the size of the device. Moore's law predicts that devices reduce in size by half every year. As Moore's law progresses, there is a demand for a more refined photolithography process. The resolution and accuracy of the photolithography process must continue to improve.

The photolithography process varies by types of photoresists, exposure method, and process module requirements, but the general process follows these main steps. Clean substrate, spin coat, post-apply bake (PAB), exposure, post-exposure bake (PEB), then development. Once the photoresist is successfully applied and developed, the substrate undergoes the next fabrication step, etching, implantation, etc., then the photoresist is removed, and, if needed, the entire process is repeated.

Photolithography uses a light-sensitive polymer called photoresist to develop a three-dimensional mask that is then used to protect areas on the substrate from being etched. The photoresist reacts to intense UV light and becomes soluble in a developer solution. There are three main ways that this is done: contact lithography, proximity lithography, and projection lithography.

Contact lithography is the most rudimentary method of lithography and is the method that will be described further in the experimental portion of this thesis. It involves pressing a photomask tightly to the substrate to ensure there are no gaps. It is then shining an intense light through the photomask and developing the image that is printed on the photomask. Other methods include proximity lithography, which has a gap between the substrate and photomask. And projection lithography, which is far more popular (Mack, 2007). It uses a lens between the photomask and the substrate that can focus the light to form a sharper image.

Contact aligners use a photomask which is a transparent screen that is printed with a pattern. The wafer is placed on the loading tray and can be finely adjusted to ensure precise alignment. Once the wafer is placed, contact is initiated. The photomask comes in direct contact with the wafer, and pressure is applied to ensure there is no space between the photomask and the wafer. Then an intense light is shined for a desired amount of time. Contact alignment produces a high resolution depending on the wavelength of the light (Mack, 2007).

Projection alignment uses a lens between the photomask and the wafer that focuses the light to a much higher resolution. There are two types of projection alignment: scanners and steppers. Scanners use a photomask that contains the entire pattern to be used over the whole wafer but scans through portions of the wafer at a single time. It can expose small areas of the wafer at once. Stepping uses a similar process, but the photomask only contains a small fraction of the entire mask. It then steps through each section of the wafer, repeating the same pattern until the entire mask is exposed. A hybrid, step-and-scan method has become the choice method for lithography today. This method uses a stepper mask and scans the mask in one direction before moving to a new location on the wafer and repeating the scan (Mack, 2007).

The photolithography process uses a photoresist, a light-sensitive polymer, to coat the surface of a semiconductor wafer. The wafer is uniformly coated using a spin coat method, where the rotational speed of the wafer determines the thickness of the photoresist. As the wafer spins, the photoresist is added. The centrifugal force pushes the liquid photoresist to the edges of the wafer. Excess photoresist flies from the substrate. The centrifugal forces, relative to the speed of rotation and mass of the photoresist, are met with frictional forces relative to the surface of the substrate and viscosity of the liquid. Once the forces reach an equilibrium, the photoresist ceases to spread, and a uniform layer of photoresist is applied. The thickness of the photoresist can be controlled by changing the rotational speed of the wafer. (1) shows the relationship of thickness to viscosity (v) and spin speed (ω) (Mack, 2007).

$$thickness \propto \frac{v^{0.4}}{\omega^{0.5}} \qquad \text{(Equation 1)}$$

Photoresist comes in two varieties, positive and negative. For a positive photoresist, the light exposure reacts with the photoresist, causing it to be soluble in a developer solution. The product is washed away in the developer solution leaving behind the three-dimensional pattern. A negative photoresist reacts with the light exposure to become insoluble in a developer solution. The photoresist is washed away by the developer, while the product remains to leave behind the three-dimensional pattern.

Determining the proper exposure time is essential for accurate pattern transfer with a high resolution. Exposure time that is too short will not fully develop the features. Not enough carboxylic acid will be produced, and the photoresist will not be soluble in the developer solution. Exposure time that is too long will over-develop the mask. Features will not be

accurately transferred. Edges will be rounded, and images will be distorted. To determine the proper exposure time, we must consider the optical absorption properties of the material.

As light passes through a material, the intensity of the light (or photon flux) decreases. This is described in Lambert's law shown in equation two, where α is the absorption coefficient for the material, *x* is the direction light is traveling, and *I* am the intensity or photon flux of light (Mack, 2007; Kasap, 2018).

$$\frac{dI}{dx} = -\alpha I \qquad \text{(Equation 2)}$$

A positive photoresist is made up of three different parts: novolac resin (R), a sensitizer (*M*), and a liquid solvent (*S*). The novolac resin is used to increase the structural properties and etch resistance of the mask. The solvent is a photoactive compound (PAC), typically diazonaphthoquinone (DNQ). It reacts with the UV light, g-line (436nm) or i-line (365nm), to create a carboxylic acid (P) which is soluble in the developer solution. As the concentration of DNQ is converted to a carboxylic acid, concentration P grows while concentration M reduces. Equation 3 shows the total concentration remains constant. The liquid solvent is in place to assist with spin coat application. A liquid is much easier to apply in a uniform thickness. Most of the solvent is baked out during the post-apply bake. The result is a hardened mask that is resistant to etching. Each of these parts determines how light is absorbed into the material.

$$P = M_0 - M \qquad \text{(Equation 3)}$$

The Beer law for the absorption coefficient of absorbing material in a nonadsorbing solvent is shown to be proportional to the sum of each of the concentrations of the absorbing materials times the material's absorption coefficient (Mack, 2007). Beer's law for N number of

solvents is shown in equation 4, where a_i is material i's absorption coefficient, and C_i is material i's concentration. It can be applied to the three parts in a photoresist shown in equation 5, which can be written as equation 6.

$$\alpha_{solution} = \sum_{i=1}^{N} a_i \, C_i \qquad \text{(Equation 4)}$$

$$\alpha_{solution} = a_M M + a_P P + a_R R + a_S S \qquad \text{(Equation 5)}$$

$$\alpha_{solution} = Am + B \qquad \text{(Equation 6)}$$

Where,

$$A = (a_M - a_P) M_0 \qquad \text{(Equation 7)}$$

$$B = (a_P M_0) + a_R R + a_s S \qquad \text{(Equation 8)}$$

$$m = \frac{M}{M_0} \qquad \text{(Equation 9)}$$

A and B are two very important parameters for determining the absorption of light for photoresists. They are known as the bleachable (A) and nonbleachable (B) absorption coefficients. The bleachable absorption coefficient tells how the color of the photoresist changes with exposure. If A is positive, the photoresist will get lighter. If A is negative, the photoresist will get darker. This seemingly insignificant detail has a large impact on determining the exposure rate of the photoresist. Because the photoresist changes color as it is being exposed, it also changes its exposure absorption coefficients. These parameters must be known to determine the exposure rate of the material.

These two parameters are not all that are needed to understand the absorption of the photoresist. To further understand the full picture, we must shift from the macroscopic scale to the microscopic scale. We see that while DNQ is being converted to a carboxylic acid, there is a short-lived intermediate chemical that is formed. The concentration of which is denoted as M^*.

The new chemical reaction is shown in equation 10. Where k_1, k_2, and k_3 are rate constants for each reaction.

$$M \underset{k_1}{\overset{k_2}{\longleftrightarrow}} M^* \overset{k_3}{\rightarrow} P \qquad \text{(Equation 10)}$$

Now, a set of differential equations can be written to describe how the concentrations change with time in equation 11. Some initial conditions can be written in equation 14, and one assumption can be made dealing with the concentration of the intermediate chemical in equation 16. Because the intermediate chemical is short-lived (only 10^{-8}s or less (Mack, 2007)), each molecule exists for only a short time before being converted to a carboxylic acid. Therefore, the concentration remains mostly constant throughout the entire reaction. Solving these equations gives equation 17.

$$\frac{dM}{dt} = k_2 M^* - k_1 M \qquad \text{(Equation 11)}$$

$$\frac{dM^*}{dt} = k_1 M - (k_2 + k_3) M^* \qquad \text{(Equation 12)}$$

$$\frac{dP}{dt} = k_2 M^* \qquad \text{(Equation 13)}$$

$$M(t = 0) = M_0 \qquad \text{(Equation 14)}$$

$$M^*(t = 0) = P(t = 0) = 0 \qquad \text{(Equation 15)}$$

$$\frac{dM^*}{dt} = 0 \qquad \text{(Equation 16)}$$

$$\frac{dM}{dt} = -\frac{k_1 k_3}{k_2 + k_3} M = -KM \qquad \text{(Equation 17)}$$

The variable *K* is the overall rate constant. *K* is proportional to the intensity of radiation. By the Grotthus-Draper law, only the light that is absorbed into the material can create a chemical change in the material (Rennie & Law, 2016). The amount of that that is absorbed is

proportional to the energy flux or intensity of light and the surface area that is absorbing light. Intensity can be written in terms of photon flux and energy per photon (hc/λ), shown in equation 18. Where φ_M is the density of photons being absorbed by material M, and v is the velocity the photons are traveling (the speed of light). The amount of light that is absorbed by material M is also dependent on the molecular absorption cross-section of material M, σ_M. So, equation 17 can now be re-written as dm/dt in terms of Intensity, the absorption cross-section, and photon flux, Φ, equation 19. Solving equation 20 for *m* leads to equation 21, which reveals an exponential relationship between *m* and *t*. equation 19 can be simplified to equation 20 with the addition of the constant C. By relating the absorption cross-section to molar absorptivity, C can be made more useful in terms of the absorption coefficient, a_M, and Avogadro's number, N_A.

$$I = v\varphi_M\left(\frac{hc}{\lambda}\right) \quad \text{(Equation 18)}$$

$$\frac{dm}{dt} = -\Phi\sigma_M\left(\frac{\lambda}{hc}\right)Im = -\frac{\Phi a_M}{N_A}\left(\frac{\lambda}{hc}\right)Im \quad \text{(Equation 19)}$$

$$\frac{dm}{dt} = -CIm \quad \text{(Equation 20)}$$

$$m = e^{-CIt} \quad \text{(Equation 21)}$$

$$C = \Phi\sigma_M\left(\frac{\lambda}{hc}\right) = \frac{\Phi a_M}{N_A}\left(\frac{\lambda}{hc}\right) \quad \text{(Equation 22)}$$

The constant C in equation 20 is known as the exposure rate constant. It tells how the photoresist changes with time. It is the third and final parameter for photoabsorption in a photoresist. These are known as the Dill parameters or ABC parameters. These three parameters are needed to fully understand how light is absorbed into the photoresist.

The amount of exposure needed to complete the reaction is determined by the exposure dose and the thickness of the photoresist. Exposure dose can be found by integrating equation 21

to give equation 23. The exposure dose is equivalent to the intensity of the light times time. For a given light intensity, the exposure dose can be easily calibrated by adjusting the time the photoresist is exposed to the intense light. Since the photoresist changes color in relationship to the bleachable absorption coefficient, the light passing through the photoresist changes intensity as the material changes. The concentration in the sensitizer changes at different rates throughout the material. Thus the difference in intensity at the top layer of photoresist I(0), and the bottom layer of photoresist I(x) must be determined. To do this, we apply Beer's law equation 6 to Lambert's law equation 2 to give equation 24 and solve it analytically. The result shown in equation 25 shows the relationship between the intensity at the top layer of the photoresist and the bottom layer of the photoresist. As can be expected, the difference in intensity is dependent on photoresist thickness and the bleachable coefficient.

$$Dose = \int_0^t I dt = It \qquad \text{(Equation 23)}$$

$$\frac{dI}{dx} = -(Am + B)I \qquad \text{(Equation 24)}$$

$$\frac{I(z)}{I(0)} = \left(\frac{m(z)}{m(0)}\right) e^{-Az} \qquad \text{(Equation 25)}$$

With these equations derived from Lambert's law of absorption and Beer's law, the rate at which the DNQ-based photoresist changes with exposure can be calculated. Parameter A tells the bleachable coefficient and how the photoresist lightens or darkens during exposure. B tells nonbleachable coefficient, how solvents react to exposure. C tells exposure rate and how the fraction of reactant and product change with time. With a given light intensity and photoresist thickness, the exposure time can be calculated.

For negative photoresists, the areas that are in contact with the light are the areas that remain after the development process. The areas that were not in contact with the light are the

areas that are washed away. This is because a carboxylic acid is formed during the post-exposure bake. It cross-links with the resin. Therefore, it is soluble in the developer solution and can be washed away (Mack, 2007). The proper exposure time can be determined for a specific photoresist and used to create a high-resolution mask for etching.

When etching semiconductor devices, the device's functionality will depend on the quality of the etch. Anisotropic etch means that the etch rate is constant in all directions. The result is a rounded profile. An anisotropic etch means the etch rate is higher in one direction and, ideally, zero in all other directions. These two etch profiles are represented in

Etching can be done in two ways, wet etching or dry etching. Wet etching uses liquid chemicals such as hydrazine (N_2H_4), potassium hydroxide (KOH), or Tetramethylammonium hydroxide ($N(CH_3)_4OH$, TMAH). to etch SiO_2, BOE, buffered oxide etching, uses ammonium fluoride (NH_4F) mixed with hydrofluoric acid (HF) to etch isotropic profile (Ekström, 2019). Wet etching is used to remove trace layers of oxide from the surface of the substrate. BOE can be used to etch the insulating SiO_2 layer. Currently, there is no conventional way of using room temperature wet chemicals for etching patterns into SiC. Dry etching can be done using reactive ion etching (RIE). Variations of RIE exist as inductively coupled plasma (ICP) or magnetically

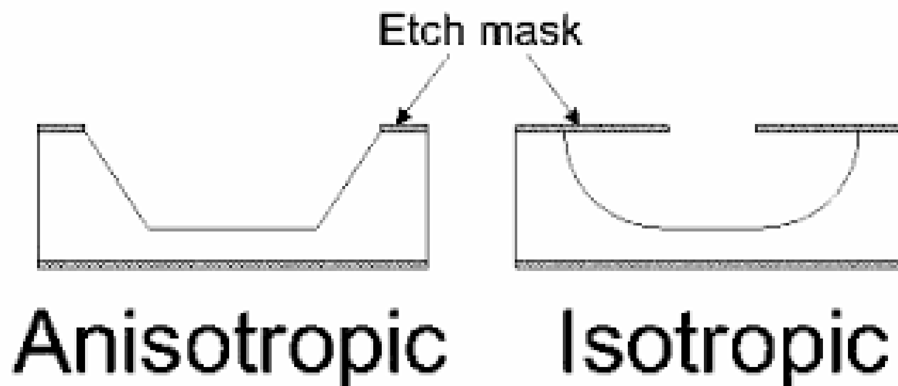


Figure 2.3 Anisotropic etch profile vs. Isotropic etch profile

enhanced reactive ion etching (MERIE). These use plasma to pattern the material and allow for etching high aspect ratios and deep vias. Plasma etching works by three main mechanisms: first, electrons are dissociated from the gas mixture into a plasma. Second, a high etch rate is achieved by ion bombardment, which breaks bonds at the top monolayers of the substrate. Third and most advantageous, an anisotropic etch is achieved by the electric field of the ion sheath in the chamber (d'Agostino, et al., 2008).

RIE etching is a more common method for etching SiC that uses both physical and chemical components. It uses RF current to induce a magnetic field which creates a plasma. The magnetic field forces the plasma in a singular direction toward the substrate, where the ions react with the surface of the material and create an anisotropic etch profile. RIE uses a combination of F-, Cl-, or Br- based chemicals for both Si and SiC. F- based plasmas give a higher etch rate and more isotropic profile, while Cl- based plasmas give a more anisotropic profile. (Ekström, 2019)

Parallel plate RIE is designed with a top electrode that is grounded and an opposing bottom electrode, where the wafer sits. RF current is applied to the bottom electrode through a

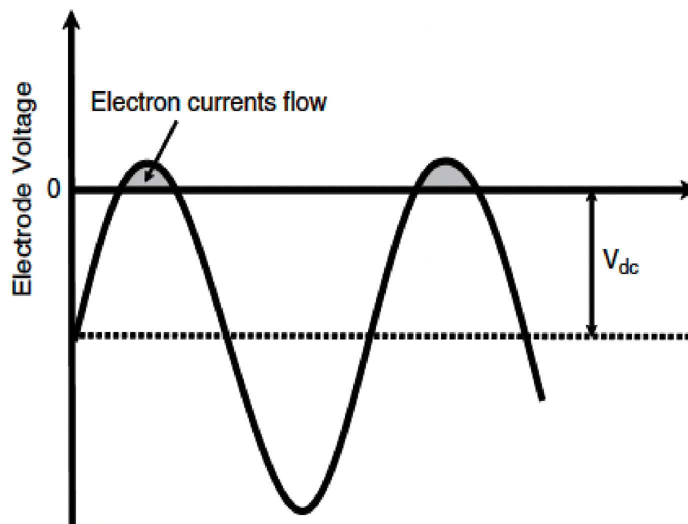


Figure 2.4 RF Waveform at bottom electrode (Nojiri, 2012)

blocking capacitor at a frequency of 13.56MHz. The capacitor causes the electrode to gradually shift towards a negative potential. This is known as a direct current bias (V_{dc}). The resulting RF current at the bottom electrode is shifted in the negative direction. The potential is only positive for a short time each cycle while mostly staying negative. Figure 2.4 shows the voltage at the lower electrode given by the RF power through the blocking capacitor. The top portion of the etching chamber is fitted with a showerhead that releases the etching gases. The RF power causes an acceleration in the electrons that ionizes the gas. A plasma is created containing cations, electrons, neutral atoms, and sometimes radicals if the energy is high enough. Electrons, being 100,000 times smaller than ions, can change directions quickly and follow the RF oscillation provided by the electric field. They can flow in both directions towards both electrodes. Ions have much more mass than electrons. They do not have enough time to oscillate directions and are therefore continuously moving in a single direction towards the bottom electrode. Electrons are pushed away from the bottom electrode when the electrode has a negative potential. Because of V_{dc}, very few electrons are in the region near the electrode at any given time. This region is known as the ion sheath because there are few ion-electron collisions in this region; thus, no light is emitted (Nojiri, 2012). The plasma is at equipotential, meaning ions flow randomly throughout. At the ion sheath region, the reactive ions move in a single direction without interference from elections, allowing the wafer to be etched anisotropically.

Inductively coupled plasma (ICP) etching is a type of RIE where the plasma is generated independently from the RF power of the bottom electrode. An induction coil is added around the etch chamber to induce a magnetic field vertically through the chamber. This magnetic field is what induces an electric field inside the chamber, which produces the plasma. The RF power from the electrode is what directs the motion of the ions. This added induction allows for

independent control of the plasma creation. A higher density plasma can be created using ICP (Nojiri, 2012). ICP allows for the operator to control many different parameters for the etch. Various types of materials or etch demands may require changes in the etch recipe. The etch can be adjusted to fit specific needs by changing various parameters of the etch recipes, such as chemical composition, chamber pressure, and RF power.

Chemical composition in the chamber can affect the etch profile. As the name implies, reactive ion etching is made up of ions traveling in a single direction and hitting the surface of the material, which causes a reaction, and the wafer material is removed. Ion-assisted etching makes up a large percentage of the total etching mechanism. Etching also occurs by radical atoms and physical sputtering by ions, but these mechanisms contribute little to the overall etch rate. Ion-assisted etching is what gives the etch an anisotropic etch profile. This mechanism depends on the target material and the gasses used. The ion-assisted reaction can change etch characterization based on the configuration of gasses used in the chamber (Zhou, Cao, & Liu, 2010; Ekinci, et al., 2014; Y. H. Lee, Yeom, Lee, Yoo, & Kim, 1998; Wang, et al., 1998; J. K. Sheu, 1999; Lin Sha, 2003). For silicon wafers, Cl^+ ions and Br^+ have a higher ion-assisted etch percentage than F^+ ions (Nojiri, 2012). This means that using the gasses chlorine and bromine-based gases such as Cl_2 and HBr can give a more anisotropic etch than fluorine-based gases for silicon wafers.

Chamber pressure is another important etching parameter to consider because it can also influence the etch profile. As mentioned before, the ion sheath is a region in the chamber where the ions can flow in a single direction without interference from electrons. With lower pressure, there will be fewer particles colliding with the ion flow. The lack of interference allows the ions to flow without scattering. The term for this is the mean free path. The mean free path is the

average distance the ion can travel without colliding with another particle, and it is inversely proportional to the chamber pressure. If the mean free path is adequately larger than the ion sheath, the ions will be able to travel in a straight line directly to the wafer. If the mean free path is smaller than the ion sheath, the ions will be more likely to scatter and travel at random angles. This will cause the sidewalls of the etch profile to be contacted by ions. The etch profile is more isotropic. In the case of an ICP etcher, the plasma density is much higher, while the ion sheath is much shorter. Thus, the mean free path can be longer than the ion sheath, so ion scattering is rate. ICP creates a more anisotropic etch than RIE.

The average amplitude of the RF voltage ($\overline{V_{rf}}$) determines the thickness and potential of the ion sheath. This comes from the V_{dc}, which is dependent on the difference in electrode voltage and surface area of the electrodes$\left(\frac{V_1}{V_2} = \left(\frac{S_2}{S_1}\right)^4\right)$ (Nojiri, 2012; Bogdanova, Lopaev, & Zyryanov, 2016). Using a modified version of the Child-Lagmuir in equation 26, the thickness of the ion sheath (s) can be calculated, where ε_0 is the dielectric constant, $\overline{J_\iota}$ is the mean current Ion density, and M is ion mass. This shows how V_{rf} is related to the ion sheath thickness. Thus RF power can determine the etching profile (Nojiri, 2012) (Bogdanova, Lopaev, & Zyryanov, 2016).

$$s = \left(\frac{0.82\varepsilon_0}{\overline{J_\iota}}\right)^{\frac{1}{2}} \left(\frac{2e}{M}\right)^{\frac{1}{4}} \left(\frac{1}{2}\left(\overline{V_{rf}} - V_{dc}\right)\right)^{\frac{3}{4}} \quad \text{(Equation 26)}$$

According to (Nojiri, 2012), there are five parameters used to evaluate the quality of an etching procedure. The parameters help compare etches and look for improvements among different recipes. The first is etch rate (ER). This is the rate at which the material is removed while being etched. Consider a substrate of a certain material with a thin film of another material deposited with a known thickness on top. Then a photoresist mask is deposited with a known

thickness on the top layer. The goal of the etch is to etch through the thin film entirely without etching away the underlying substrate. The ER for the photoresist, target film, and underlying substrate must all be known when performing an etch. This is to determine the proper etch time and ensure that the etch reaches a targeted depth without going too far into the underlying substrate. Next is selectivity. This is the ratio of etch rates between two different materials. The ER of photoresist/target film (ER_1/ER_2) must be known, and the ER of target film/Underlying substrate (ER_2/ER_3) must also be known. This means the photoresist has a lower etch rate than the target film. Therefore the film can be etched quickly while the photoresist remains to act as a mask. The selectivity of ER_2/ER_3 must be higher. This ensures that the etch time is calibrated in such a way that it will stop the etch at the exact moment when the film is etched entirely through, and the etch on the underlying substrate is minimized.

The third parameter to measure is the critical dimension (CD) after etching. This is the small change in feature size after the etch is complete. This small difference must be accounted for with each process step in fabrication. The light shines through a mask that is printed with features. It is impossible for the features on the photoresist to be the exact same size as the mask. There is going to be a small change in size. This small change is known as the critical dimension (Mack, 2007; Nojiri, 2012). When the substrate is then brought to be etched, the final etch is going to have a small change in size from the photoresist mask. The compounding change in size is known as the CD shift and is the fourth parameter to measure $\Delta CD = CD_{mask} - CD$. The CD has a direct influence on the transistor performance. It can determine the threshold voltage. If the CD is nonuniform across the wafer, the threshold voltage will also be nonuniform.

The last parameter to measure is the etch profile. The etch profile is the cross-section of the etch, generally viewed with an electron microscope. This can be used to measure the isotropy

of the etch. The etch profile can be measured by measuring the interior angle of the standing structure. This can tell how tapered the etch profile is. The ideal etch profile will have a 90,° angle, while greater than 90° is a reverse taper and must be avoided. A reverse taper can cast a shadow during ion implantation where areas will not be implanted. Figure 2.5 illustrates the five parameters that must be measured.

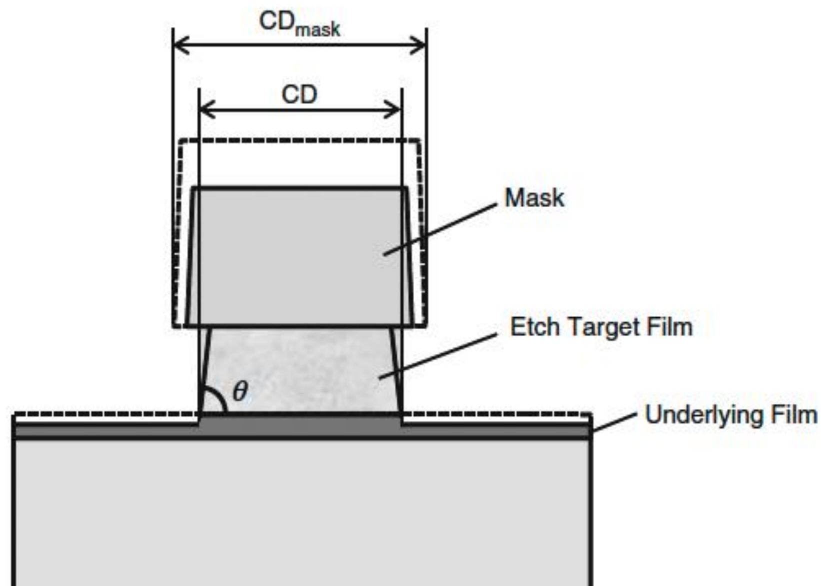


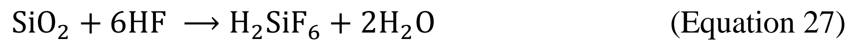
Figure 2.5 Illustration of the 5 parameters to measure for evaluating an etch (Nojiri, 2012).

Certain materials require a more durable mask, such as oxide (Nakamura, Iizuka, & Yano, 1989). A more durable mask can increase the selectivity between the target material and the masking material, although it can cause sidewall passivation, which can decrease the profile angle (Tseng & Tsui, 2016; Tseng & Tsui, 2016). When etching polysilicon, a photoresist does not provide a high enough selectivity. Therefore a hardmask such as SiO_2 can be used (Ekström, 2019). Creating a hardmask is a more complicated process than a photoresist mask. The mask must be deposited or grown and then patterned with a liftoff process or etching process. The result is a layer of material that is patterned, similar to a photoresist mask. After the plasma

etching is finished, the mask must then be removed in order to reveal the etched substrate. This is often done using a wet etching method.

At various stages during the IC fabrication process, it is not necessary to use plasma etching. Wet etching is often a better method. When cleaning the wafer from an oxidized surface or patterning an insulating SiO_2 layer, BOE can be used.

In a CMOS device, insulating SiO_2 is used to isolate the IC from the bulk substrate. There are three reasons why this is required. This reduces leakage current, which improves operation temperature. It reduces capacitance, so the speed is increased, and power requirements are reduced. Noise is reduced for sensitive systems (Honeywell International Inc., 2022). An aqueous solution with hydrofluoric acid is commonly used to pattern SiO_2. The chemical reaction is shown in (Equation 27). The reaction is made up of several steps. Because the reaction rate is independent of agitation, the reaction rate of the slowest reaction will determine the overall reaction rate (Spierings, 1993).



$$SiO_2 + 6HF \longrightarrow H_2SiF_6 + 2H_2O \qquad \text{(Equation 27)}$$

The HF solution is made up of the following species, H^+, F^-, HF_2^-, HF, and H_2O. Oxide reactions in NaF and NH_4F do not etch SiO_2 (Judge, 1971; Tso & Pask, 1982), so it can be concluded that F^- ions do not contribute to the reaction rate. The reaction rate is described by the concentration of HF_2^-, and HF in the solution, though it is disputed which one has a larger impact. The H^+ ions act as a catalyst for the reaction that is described in (Spierings, 1993). The etch rate of the solution is determined by the reactivity of HF, HF_2^-, and H^+. The solution can be adjusted by adding strong acids or fluorides to the mixture. Higher HF concentrations give higher etch rates. Strong acids that can be added to the HF solution are HCl, HNO_3, and H_2SO_4.

For a buffered oxide etch (also known as buffered HF), NH_4F is added to HF. This is exclusively used for etching SiO_2 in the IC fabrication process. BOE solutions are typically a mixture of 40 wt % NH_4F solution with 49 wt % HF solution in various ratios with water added. NH_4F is added to dilute the solution and reduce the etch rate and attack the photoresist. At high NH_4F concentrations, the HF_2^- become inactive due to complications with NH_4^+ ions (Spierings, 1993).

BOE can be applied in several ways: stirring, bubbling, and ultrasonic agitation can be used to increase the effectiveness of the etch. The solution can be sprayed on a flat wafer as it rotates to increase uniformity. An aerosol BOE solution can be used to increase the anisotropy of the etch. Wax can be applied manually to the surface to protect regions from the etchant. For smaller dimensions that are commonly found in IC design, the photoresist is used. Pure HF can remove the adhesion of the photoresist from the surface. This can be a problem with high HF concentrations or long etch times. NH_4F has been shown to reduce the attack on photoresists (Spierings, 1993). Increased temperatures can also be used to increase etch rate, therefore, reducing etch time and the attack on a photoresist (Burham, Sugandi, Nor, & Majlis, 2016). In some cases where a deep etch is required, an HF-resistant film is required, such as chromium that is patterned with a photolithographic process.

Aqueous HF solutions provide isotropic etch profiles. When a masking material such as photoresist or chromium is used, the mask has strong adhesion to the surface of the substrate. This creates rounded sidewalls. Delamination of the mask can cause the material to have a tapered sidewall. The tapered sidewall can also be done intentionally by using a second film below the mask that has a higher etch rate than the oxide. The selectivity between these two materials determines the slope of the etch profile (Spierings, 1993).

The photolithography and etching mechanisms described above will need to be studied. To understand how these methods can be used in SiC CMOS fabrication, these methods must be recreated in our lab. The following chapter will discuss the methods used to recreate state-of-the-art using the facilities available at the University of Arkansas. The results of these initial studies will be described in the following section as well. Then, in chapter 4, the experiments will be conducted to improve these results so that they may be utilized in CMOS fabrication.

Chapter 3. Etching Process Methods

This chapter will discuss the initial experiments that were conducted to recreate state-of-the-art. Methods for photolithography, ICP, and BOE will be attempted. The methods and results will be described in detail. In chapter 4, changes to the original methods will be made. The same equipment and facilities will be used throughout the following chapters.

3.1 Photolithography

With any etching process in IC fabrication, the resolution can only be as precise as the preceding photoresist resolution. A photolithography mask recipe capable of depositing a high-resolution mask must be developed before any etching studies can commence.

First, a photomask was designed for the purposes of calibration. The goal of this mask was to determine the minimum feature size that the photolithography process could create accurately. To test the accuracy of pattern transfer, different shapes with various angles were used. The shapes that were used were: squares, circles, donuts (varying thicknesses), and 5-point stars. Each shape was repeated and re-sized to fit inside a square with the following side lengths: 1-10μm, 15μm, 20μm, 25μm, 30μm, 40μm, 50μm, and 115μm. Rectangles of various sizes were

used to fill up empty space on the mask. Cross-shaped alignment marks were added in the corner of each 1cm x 1cm pattern to help with alignment. The 1cm x 1cm pattern was repeated on a 10x10 array to complete the mask. An AutoCAD blueprint image of the 1cm x 1cm pattern is shown in Figure 3.1.

Once the photomask was designed and manufactured, photolithography procedures could commence. The standard photolithography procedure for the University of Arkansas facilities was performed. The general process goes as follows: clean wafer, spin coat photoresist, post-

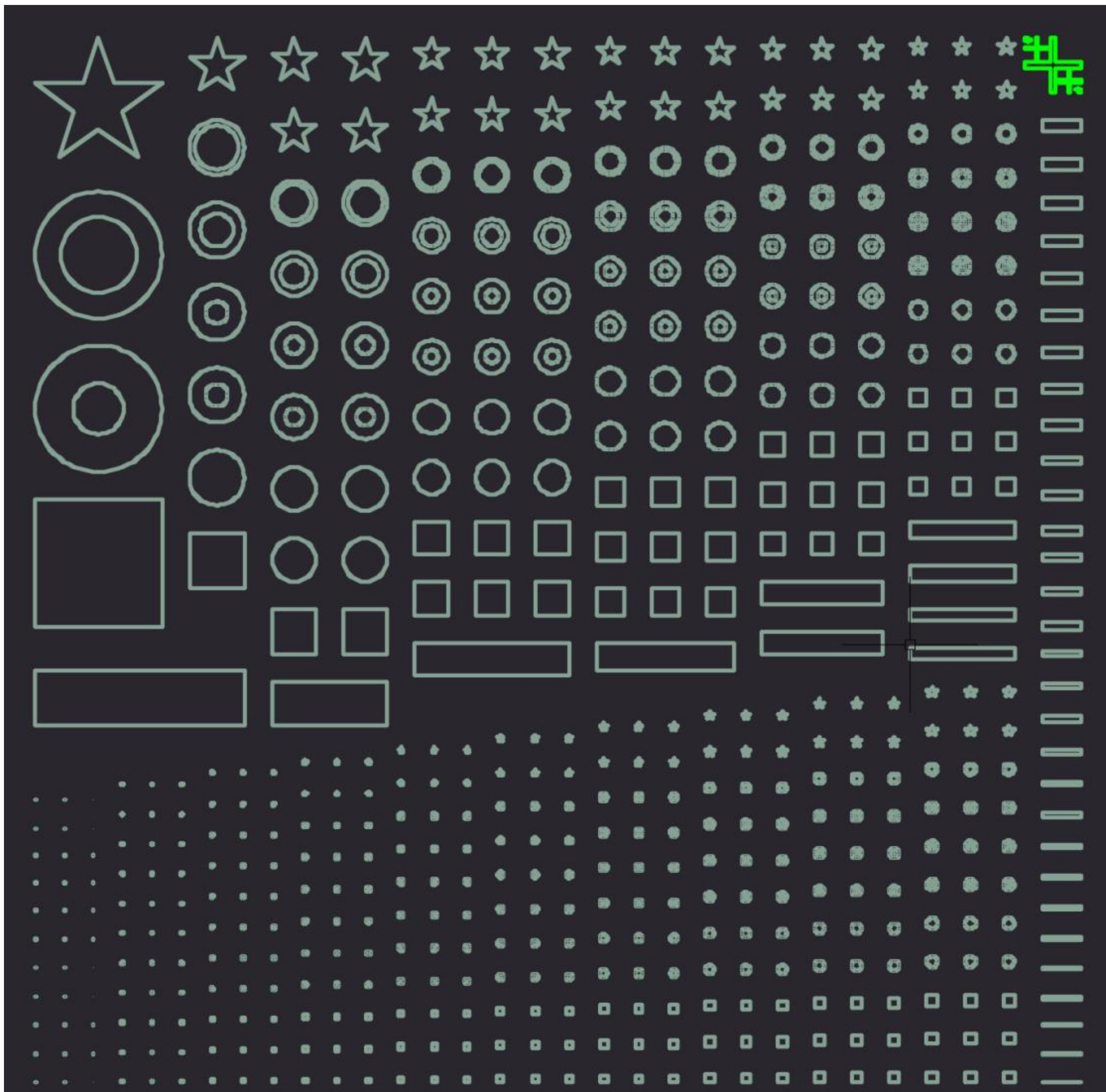


Figure 3.1 AutoCAD generated image of photomask design that will be used.

Apply bake (PAB), alignment and exposure, post-exposure bake, flood exposure, and development. The exact specifications of the procedure for this control experiment are described in the original traveler shown in Appendix A. The traveler recommends each sample undergoes a 9-step sample cleaning process that involves 3-5 minutes of sonication steps in acetone, methanol, and IPA. In this experiment, we shortened this cleaning process to a 5-minutes acetone sonication, IPA rinse, DI water bath, N_2 blow-dry, and 2-minute dry bake at 100°C. This was to save time when processing many samples, and given the condition of the cleanroom, small particles interfering with our results were inevitable.

A spin coater was used to spread the photoresist across the sample. First, HMDS was coated on the sample to promote adhesion. This was applied with a small amount of chemicals and a rotation speed of 4000 rpm. The excess HMDS was removed during the rotation, and an even layer of HMDS was left across the entire sample. HMDS is indented to be entirely evaporated before moving on to the next step. The next step was adding a photoresist in a similar fashion. The photoresist used was AZ nLOF 2035, a negative resist. The rotation speed used was 3000rpm, which, according to the datasheet (Merk KGaA, 2021)leaves a layer of photoresist with a thickness of 3.5µm. The physics behind the spin coat process is described in (Mack, 2007). During the spin coat process, the centrifugal force pushes the photoresist away from the center of rotation. The opposing frictional force pushes the photoresist towards the center of rotation. Initially, the centrifugal force, proportional to the mass of the liquid, is greater than the frictional force. Therefore, some amount of photoresist is flung off the sample. This continues until the centrifugal and frictional forces are balanced, then no more photoresist is removed. The result is an even layer of photoresist across the sample. After the photoresist is applied, a soft bake is required to adhere the photoresist to the sample. The photoresist is now ready for

exposure. However,, this is one negative result of this spin coat process. Due to the shape of the sample, there is a higher amount of surface tension along the edge during the rotation time. This results in a thicker amount of liquid building along the edges of the sample. This is referred to as the edge bead. If the edge bead is left on the sample, the contact aligner will not be able to make an even contact, and exposure will not be accurate. To remove the edge bead, the datasheet (Merk KGaA, 2021) and (Mack, 2007) recommend using edge bead remover, which thins the photoresist without removing the photoresist entirely. However, for experimental purposes, acetone, which removes the photoresist entirely and leaves a rough edge, is acceptable. The sample is now ready to be loaded unto the contact aligner.

The aligner that was used is a Karl Suss MJB-3 contact aligner. The first step is loading the photomask. The photomask is designed so that the pattern is printed on one side of a transparent pane of plastic. The other side of the mask does not have an image printed on it. The sample is intended to be in as close contact with the pattern as possible. Therefore, the side that has the image printed on it is the side that must be in contact with the sample. This is to reduce any refraction that may occur as the light passes through the mask. Visual observation of the mask will show that one side of the mask is mirrored while the other has a chrome look. The chrome side is the side required to be in contact with the sample. When placing the photomask in the vacuum holder, the mask must cover all vacuum holes so that a proper vacuum hold can be established. Chrome, or contact, the side must be facing up. The aligner that was used has a problem that results in only one quadrant of the loading area receiving proper exposure. This requires that the photomask must be designed in four quadrants, with each quadrant being a different pattern. The photomask must be orientated so that the intended pattern is in the right quadrant. Figure 3.2 shows the proper mask setup. Once the vacuum hold is initiated, the entire

apparatus is then flipped at a 180° turn so that the side that was once facing up is now facing down. The apparatus is then inserted into the contact aligner, and the sample is ready to be loaded for exposure.

The sample can now be placed on the wafer chuck. This is done by sliding the chuck out to its loading position, placing the sample in the lower right-hand quadrant, then closing the tray. To ensure proper alignment, the adjustment knobs are used to change the X, Y, and rotational axis. Once alignment is exactly as indented, it is time to initiate contact. Once there has been contact between the mask and the sample, no more alignment adjustments can be made, and contact cannot be broken. Although the sample and mask are in contact, there is still space between the sample and mask. The Z-axis dial must be turned until it cannot rotate anymore. This raises the wafer chuck so that the sample is pressed against the mask with a higher pressure than before. Full contact is now being made with the sample. It is time to expose the sample.

Assuming an exposure time of 17.7 seconds, adjust the time dial to approximately 18 seconds and expose the sample. A post-exposure bake (PEB) is required at 110°C for 60 seconds. Although not specified in the traveler, our early trials used a flood exposure step of 60 seconds without the photomask in place. For the flood exposure, there is no need to initiate contact, simply place the sample on the chuck and expose it for 60 seconds. The final step in the photolithography process is to develop the photoresist.

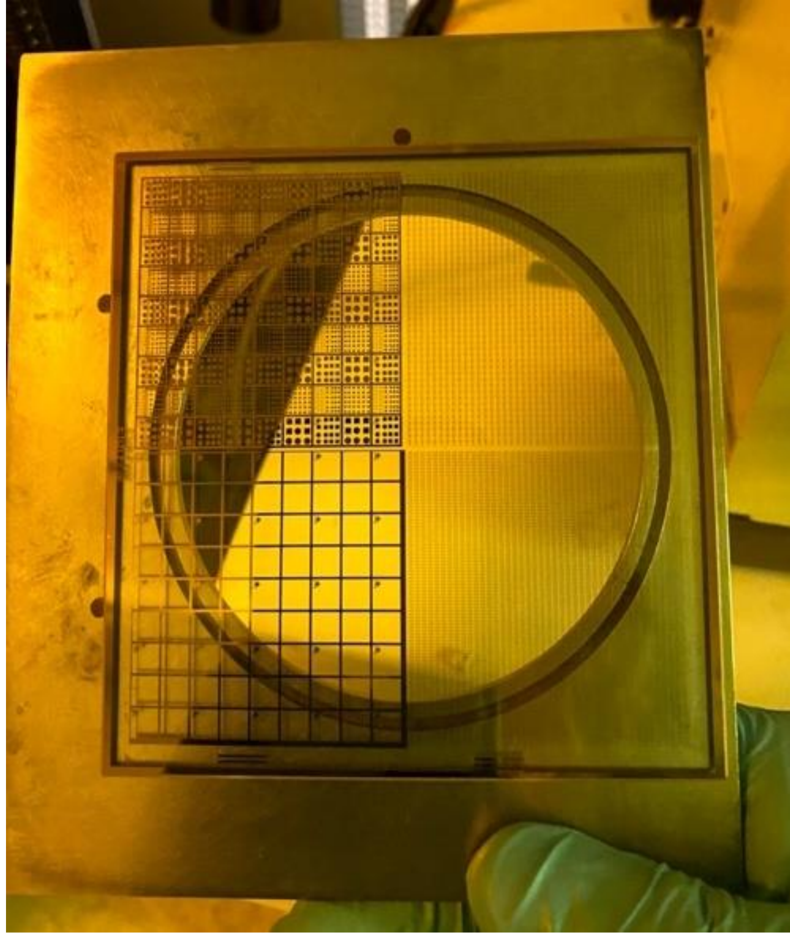


Figure 3.2 Photomask being loaded into aligner

To do this, the sample is held in a beaker with developer liquid for a specified amount of time, then immediately removed and placed in a water bath to stop development. The sample is then dried with N_2 blow-drier. The developer used in early trials was AZ 726 MIF for 35 seconds. The Keysight microscope was used to view the results shown in Figure 3.3 and Figure 3.4. The results show that this photolithography procedure was unable to accurately transfer the features of the photomask to the photoresist. The smallest features were not transferred at all, while the larger features were not accurately represented. It should also be noted that circular features were transferred with high accuracy. This is because circular objects do not require a high resolution to be transferred with photolithography. 3.2 shows the same sample at a higher magnification. It shows a feature that is intended to be a perfect square with right angles. This

shows that the angles are not, in fact, rounded but have a jagged or wavey edge. This wave resembles that of a light wave. This implies that the high-intensity light from the exposure lamp may be refracting at the corners. A higher resolution is needed to obtain sharper corners and smaller feature sizes.

3.2 Inductively Coupled Plasma

When etching a CMOS device, it is critical that the etch is calibrated so that it etches the desired depth without over-etching. When layers of varying materials are deposited on a substrate, the different materials could have different etch rates. These values must be known for calibration. As described in the previous section, etch rate and selectivity are measurements that must be taken to help calibrate the etching procedure. At the time of this study, the ICP etcher has only access to Cl_2, BCl_3, NF_3, and N_2. A reliable value for the etch rate of SiC must be determined at an ICP recipe that is known to work.

To do this, gas chemistry in this baseline recipe that has been known to work with GaN (Lee, et al., 1998; Kim, Yeom, Lee, & Kim, 1999) was used for SiC. The photoresist was applied using the photolithography process described previously. The same calibration mask was used for all etching experiments to directly compare critical dimensions between photolithography and etching. The detailed procedure for ICP etching in the Nanofab lab is shown in Appendix I.

Exchanger 2 Temp: 35°C	Cl_2: 13 sccm	Time: XX:XX
Sample-ICP Temp: 40°C	BCl_3: 25 sccm	RF1 Power: 300W

Chamber Pressure: 10mT	N_2: 00 sccm	RF2 Power: 1000W

Table 3.1 shows the temperatures, chamber pressure, flow rates, etch time, and RF power that was used for the baseline recipe. RF1 is the power at the bottom electrode where the wafer sits, and RF2 is the power at the induction coil that generates the plasma. The total flow rate for the gases was 38 sccm, where Cl_2 made up approximately 34%.

Using a Dektek 3030 profilometer, the etch depth was measured. The photoresist was removed with acetone before etching depths were measured. Figure 3.5 shows the path of the stylist on the etched SiC sample after the photoresist was removed. The red line shows the path and direction the stylist traveled on the sample. This path was chosen because the larger features made for easier measurements and more repeatable results. The etch depth was measured at various points across the substrate and then averaged together to get a reliable estimate for the depth of the etch. This measurement is then divided by the etch time to give the average etch rate across the sample. The first two samples that were etched using the baseline ICP recipe shown in Table 3.1 for one minute had an average depth of 137.1 nm. The same recipe was then used to etch SiC samples for 1-5 mins. The data shown in Figure 3.6 shows a linear relationship with a slope of 1330 Å/min. Data was collected for a three min etch, but the gas lines in the ICP needed to be cleaned. The collected data was unreliable and thrown out

There is little known about the etching performance of SiC with Chlorine based gases. To design the plasma etching process modules for the SiC CMOS, more needs to be understood. The five parameters need to be measured. Etch rate, selectivity, CD, CD shift, and etch profile need to be measured for SiC, doped SiC, polysilicon, SiO_2, and photoresist. New gas ratios must also be experimented with to determine how the selectivity changes with the gas recipe. The next section will discuss the procedure used to study the plasma etching performance of SiC.

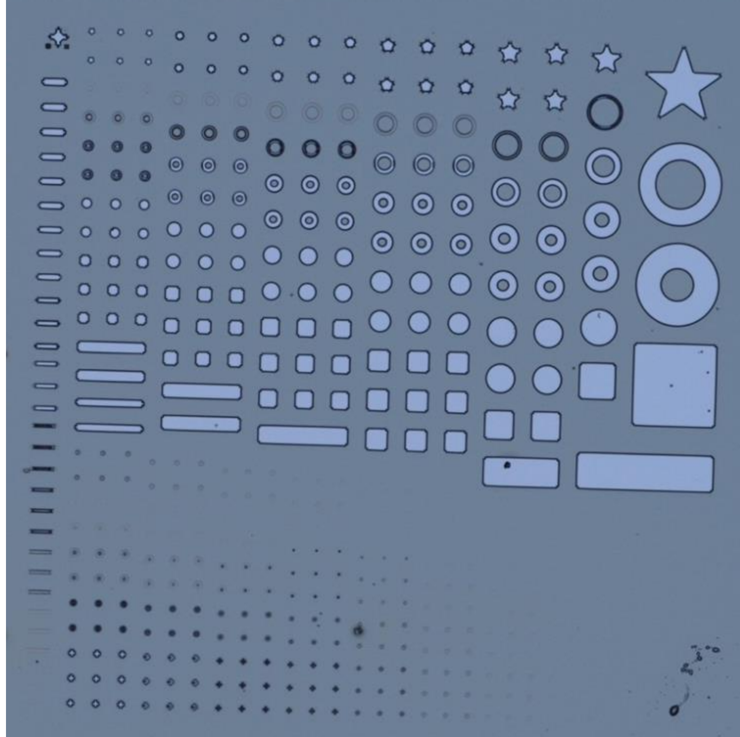


Figure 3.3 Photoresist on Si wafer using original photolithography process.

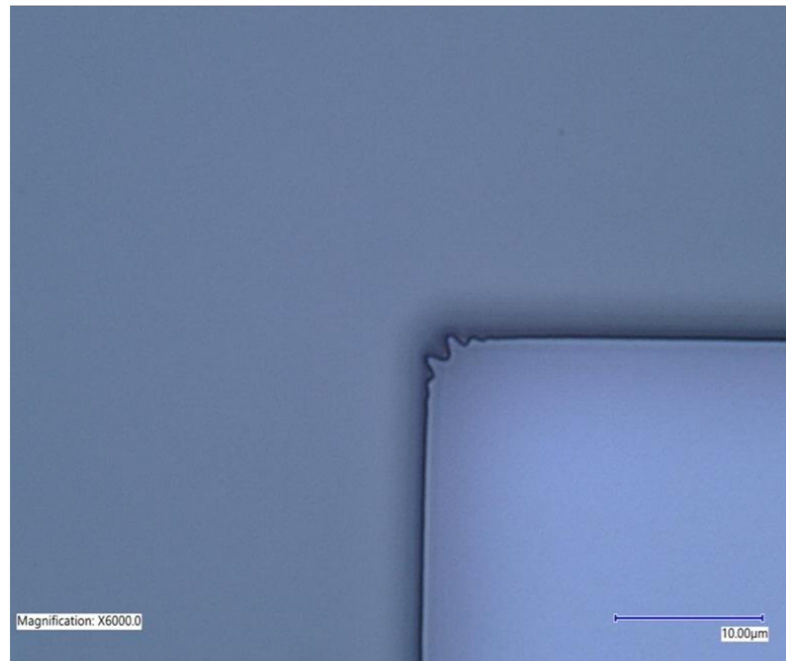


Figure 3.4 High magnification image of photoresist on Si wafer

Table 3.1 Baseline ICP Recipe

Exchanger 2 Temp: 35°C	Cl_2: 13 sccm	Time: XX:XX
Sample-ICP Temp: 40°C	BCl_3: 25 sccm	RF1 Power: 300W
Chamber Pressure: 10mT	N_2: 00 sccm	RF2 Power: 1000W

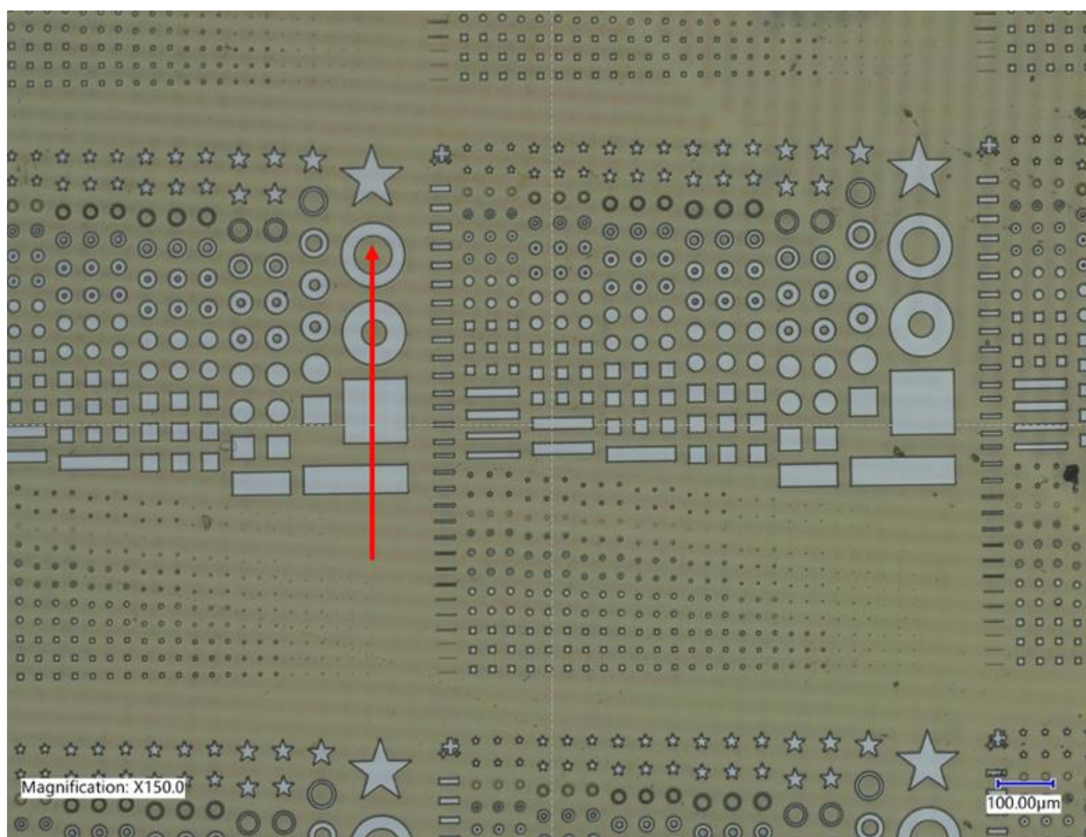


Figure 3.5 SiC etch using the baseline ICP recipe with red line indicating the path of profilometer measurements.

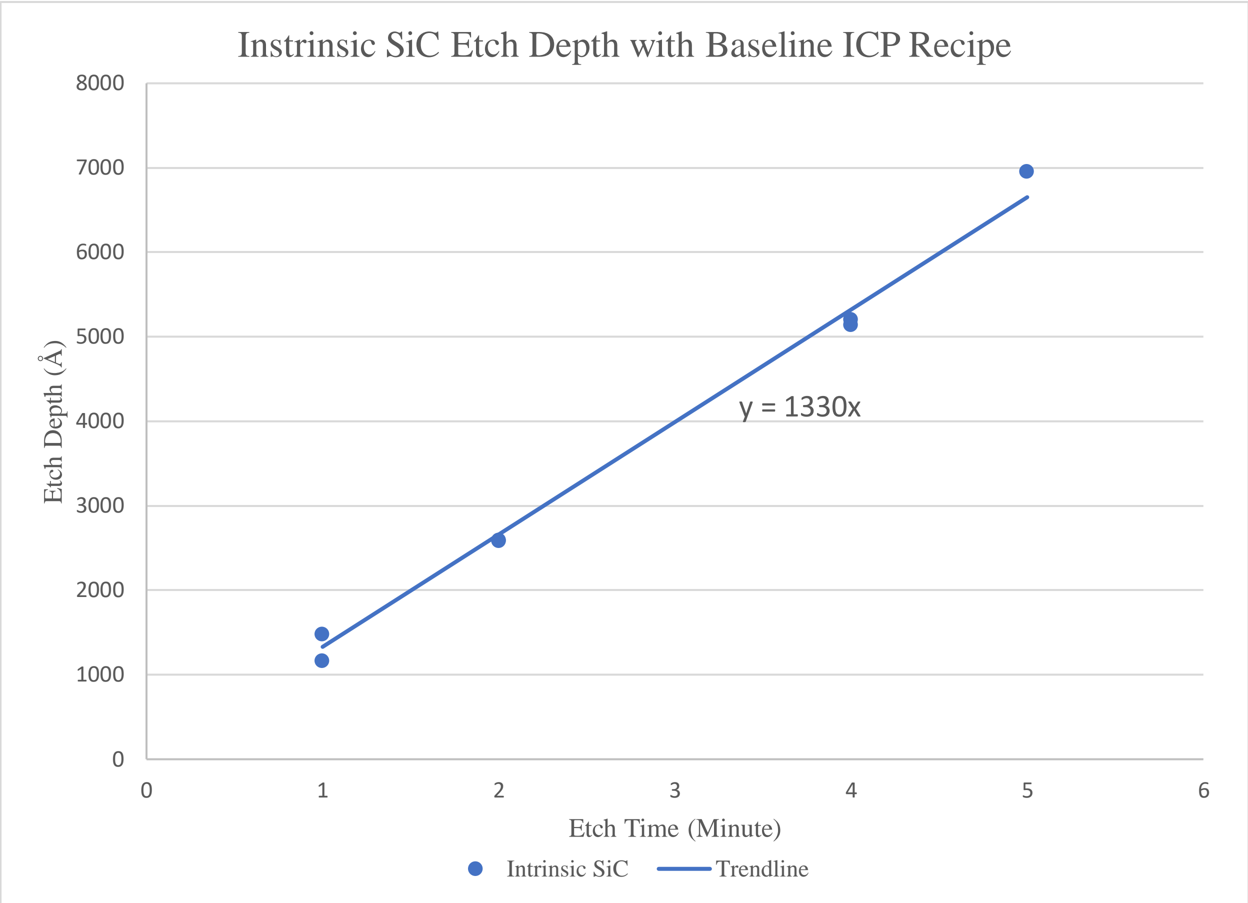


Figure 3.6 Etch depth for intrinsic SiC etching with the baseline recipe

3.3 Buffered Oxide Etching

As described in previous sections, buffered oxide etching is a wet etching method for etching silicon dioxide from the surface of a silicon wafer. This method can be used to remove the oxidation layer from the surface of a substrate. It can be used to pattern oxide for the use of an insulating field oxide or gate oxide in a CMOS device or a hardmask layer that can be used for high selectivity plasma etching.

Like the method for calibrating a plasma etch, a baseline etch recipe is used before improvements to the recipe can be made. The baseline recipe used a BOE solution that was pre-

mixed 5:1 ratio. This is one part by weight hydrofluoric acid (HF) and five parts by weight ammonium fluoride (NH_4F). This was mixed with water in a 20% by vol BOE solution in a 100 mL total volume. A single silicon sample was deposited with a layer SiO_2 by sputtering. Using ellipsometry, the approximate thickness of the oxide layer was 136nm for this first sample. The sample was then deposited with a photoresist mask identical to the mask used for photolithography calibration. Then it was cleaved into three separate samples. Each sample was submerged in the solution 60s, 40s, and 20s, respectively. The solution was not agitated during the etching time. The only agitation comes from submerging the sample and removing it from the solution Figure 3.7 shows the three samples that were etching using this BOE solution. It can be seen from Figure 3.7 that the longer the sample was submerged in the solution, the more oxide was etched. The oxide will continue to be etched until the underlying Si substrate is revealed. The etching does not appear to be consistent throughout the entire sample.

It appears the larger features are etched more quickly than the smaller features. This is likely due to the larger surface area that is in contact with the etching solution. Figure 3.8 shows a close-up view of the sample that was etched for the 60s. The sharp points on the star have become more rounded, and the inner circles of the donut shapes have disappeared. This is likely due to the isotropic etch profile that etches in all directions.

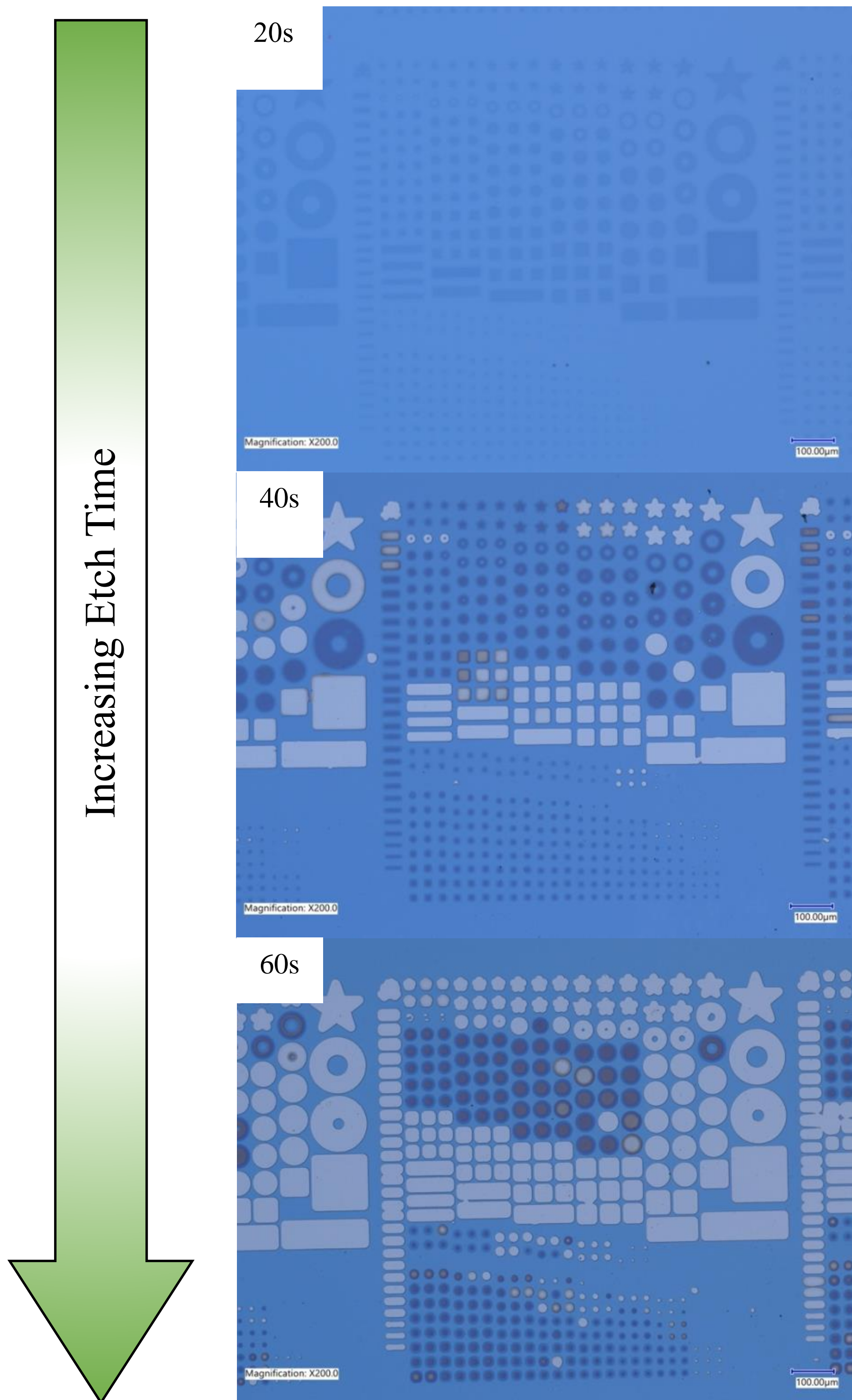


Figure 3.7 Si Substrate with SiO_2 etched with BOE for 20 s, 40 s, and 60 s.

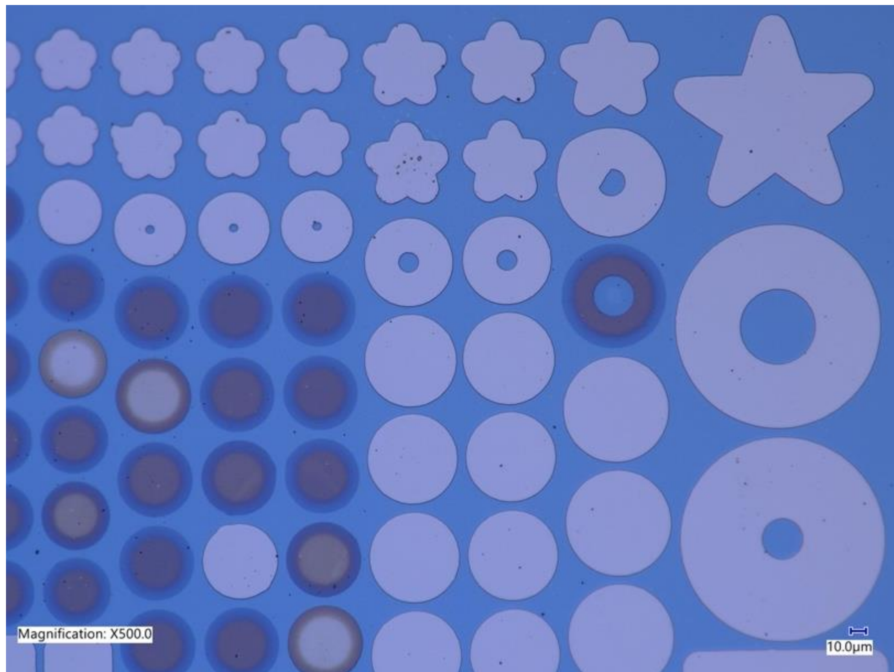


Figure 3.8 Detail image of the Si substrate with an SiO2 layer that had been etched for 60 s.

In some cases, silicon dioxide can be used as a hardmask for plasma etching. When etching polysilicon with plasma, high selectivity is required to reduce over-etching and micro-trenching. Photoresist tends to add carbon to the gas inside the plasma chamber and then redeposit that carbon onto the substrate, causing micromasking. This will reduce the etch rate. Silicon dioxide has a high selectivity to polysilicon without the micromasking effect of photoresist. For this reason, silicon dioxide is preferred for etching polysilicon (Ekström, 2019; Bell, Joubert, & Vallier, 1996). For an oxide hardmask to be effective, it must have a high resolution and be etched entirely through to the target material. This can be a difficult task considering the nature of wet etching and the isotropic etch profile it gives. A possible solution to this problem is using a lift-off method to pattern the silicon dioxide. This will be described in later sections.

A method for depositing a silicon dioxide hardmask from sputter deposition that can be used for polysilicon plasma etching must be developed. The resolution of the mask will need to

be improved, and the etch must be more consistent. The wet etches rate will need to be determined to create a method for depositing a hardmask. The plasma etches rates for silicon dioxide and polysilicon will be measured to verify if silicon dioxide will make a suitable hardmask.

There are many improvements that need to be made to the etching process modules of the SiC CMOS. The photolithography recipe must be improved to increase resolution and pattern transfer accuracy. This will be done by analyzing the photolithography process to determine areas for improvement. The critical dimension of the photoresist will be determined by measuring the resolution of images of the photoresist and comparing them to the photomask. The plasma etching recipe will need to be calibrated for the various materials that will be etched. This will be done by varying the gas mixtures that are used to etch the material. To determine the quality of the etch, the five parameters mentioned before will be measured for these materials and gas combinations. Lastly, the hardmask deposition process will be determined by using various BOE recipes and attempting an oxide liftoff attempt. Then that hardmask will be tested with polysilicon in an ICP etcher. These methods for improving the process modules will be described in greater detail in the following chapters.

Chapter 4. Etching Process Module Development and Results

This chapter will discuss the experiment design and results that have been conducted to improve the methods that have been described in the previous chapter. These experiments aim to improve the accuracy of pattern transfer from the mask. The selectivity of different etch chemistries have also been studied to characterize chlorine-based ICP etches with SiC. SiO_2 etching with ICP and BOE has been studied along with an alternative to etching, liftoff.

4.1 Photolithography

The initial resolution for the mask was not sufficient to perform etching experiments. It would be too difficult to make observations on the quality of the etch if the mask was poor quality. To improve the quality of the photoresist mask, the photolithography procedure had to be changed.

The first change that was made to the procedure was the exposure time. The original instruction was to expose the photoresist for 17.7 seconds. There was no explanation of where that exposure time came from. A more accurate exposure time can be calculated from equation 23. The exposure time is equal to the exposure dose of a given photoresist at a certain thickness divided by the intensity of the lamp in the aligner, which can change as the bulb ages. For our given photoresist, AZ nLOF 2035, at a thickness of 3.5µm, is 80 mJ/cm^2. To calculate the exposure dose for a different thickness becomes a difficult math problem involving analytical calculus (Mack, 2007). So it is better to keep the thickness at 3.5 µm and use the given exposure dose. Now the proper exposure time can be calculated for the measured lamp intensity.

A higher resolution was achieved by changing the photolithography procedure. The datasheet (Merk KGaA, 2021) recommended AZ 726 MIF developer for a development time of 35 s or AZ 300 MIF for a development time of 120 s. To test if this new developer was an improvement, two identical Si samples were processed in photolithography simultaneously. Photolithography processes were identical (described in Appendix A). The only change in the two procedures is the developer and development time. Sample one used the AZ 726 MIF for 35 s. Sample two used AZ 300 MIF for 120s. The higher quality procedure would be used for the etching studies. The results are shown below in Figure 4.2and Figure 4.1.

The figures above show a subtle difference in photoresist quality. It is most noticeable when looking at the small features and at the sharp edges of the features. There appear to be more small features being developed with the AZ 300 MIF developer. The quality of the image transfer is also higher. By looking closely at the sharp edges of the square features, the corners appear more rounded, and less of the wave pattern appears. There also appears to be a thicker parameter around the features that were developed with AZ 300 MIF. This indicates that there may be more of a tapered sidewall in the photoresist.

It should also be noted that while the photolithography process has been changed to increase the high-quality pattern transfer, there is still variation between samples. This is most likely due to the contact aligner. For the contact alignment to be done properly, it requires contact at high pressure with no space between the sample and the photo mask. The contact aligner at the photolithography facility is not always consistent with the amount of pressure that is applied; therefore, variations appear. However, by doing these tests simultaneously, with the only difference being the developer used, it is reasonable to assume the difference in photoresist quality is from the developer.

This is because the two developers used have different properties that affect the development. The developer AZ 726 MIF is a surfactant developer. Meaning it has a surface-acting agent additive that causes faster etching at the surface of the photoresist. This allows for faster development and sidewalls that are steeper. AZ 300 MIF does not have a surface-acting additive, so the development rate is slower and requires more development time. This also explains why the sidewalls may be more tapered. Developers that are less surfactant can produce shaper profiles (Mack, 2007). This is why we see sharper corners with the features developed with AZ 300 MIF.

There are still improvements that can be made with the photolithography process. This new developer solution gave higher resolution, which was an improvement. With the contact aligner giving variations in contact pressure, it was believed that the highest quality photoresist could be achieved in this facility, was achieved. Now that a somewhat reliable photolithography procedure was developed, etching studies could commence.

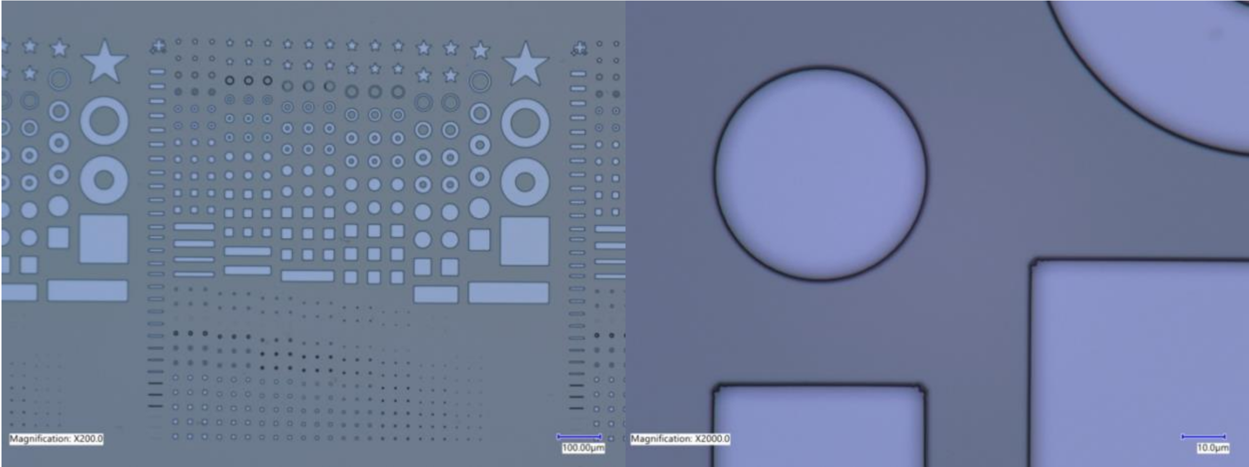


Figure 4.2 Photoresist that was developed with AZ 726 MIF for 35 s.

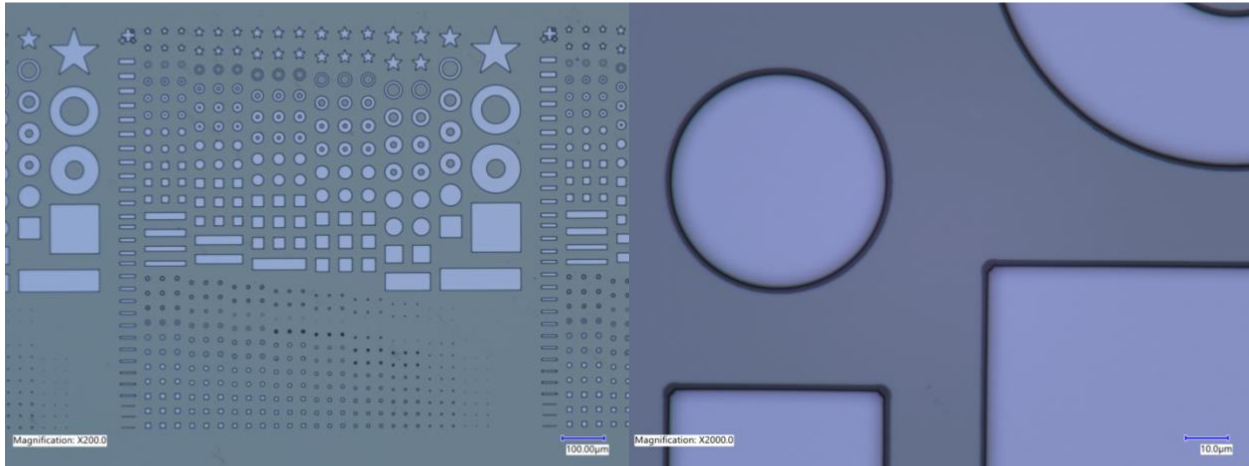


Figure 4.1 Photoresist that was developed with AZ 300 MIF for 120 s

4.2 Inductively Coupled Plasma

This chapter will discuss two studies that have been conducted, as well as initial trials to ensure the results were reliable for the baseline recipe. These two studies include a characterization study and a gas composition study. The former consists of etching various materials that are of interest in SiC CMOS fabrication in order to characterize the baseline ICP recipe. The latter consists of etching intrinsic SiC with doped SiC using five different etching recipes that consist of different gas compositions.

4.2.1 ICP Characterization Study

This characterization study aims to measure each of the five characterization parameters described preciously for the baseline recipe. The etch rates and selectivity of SiC (intrinsic and doped), Si, and SiO_2 have been determined. The CD, CD shift, and profile angle of SiC was measured. Each etches that was conducted used the photolithography process described previously. Because the ICP is a long process, most experiments took place over two days, where photolithography was conducted on the samples on the first day while the etch was conducted the next day. The samples were stored in a dark cabinet in the cleanroom but were not contained in an N_2 dry box.

The etch rate values were calculated by measuring the depth of the etch using the profilometer. A minimum of 3 sample points were taken across the surface of each sample. Then the recorded values were averaged and divided by the total etch time to give the average etch rate for that sample. There was a minimum of 2 samples of each material. The etch rates of each sample were then averaged together to give the etch rate for that material. A thin layer of oxide was deposited on a Si substrate. The initial etch time of 2 minutes was too long for the deposited oxide. It had

been etched entirely through, and the surface of the underlying Si substrate had been etched. The etch rate became impossible to measure accurately. Another etch batch was conducted for 30 seconds containing only the SiO_2 samples. This etch resulted in a shallow etch, but it was deep enough for the etch depth to be measured and the etch rate to be calculated. The results are shown in Figure 4.3

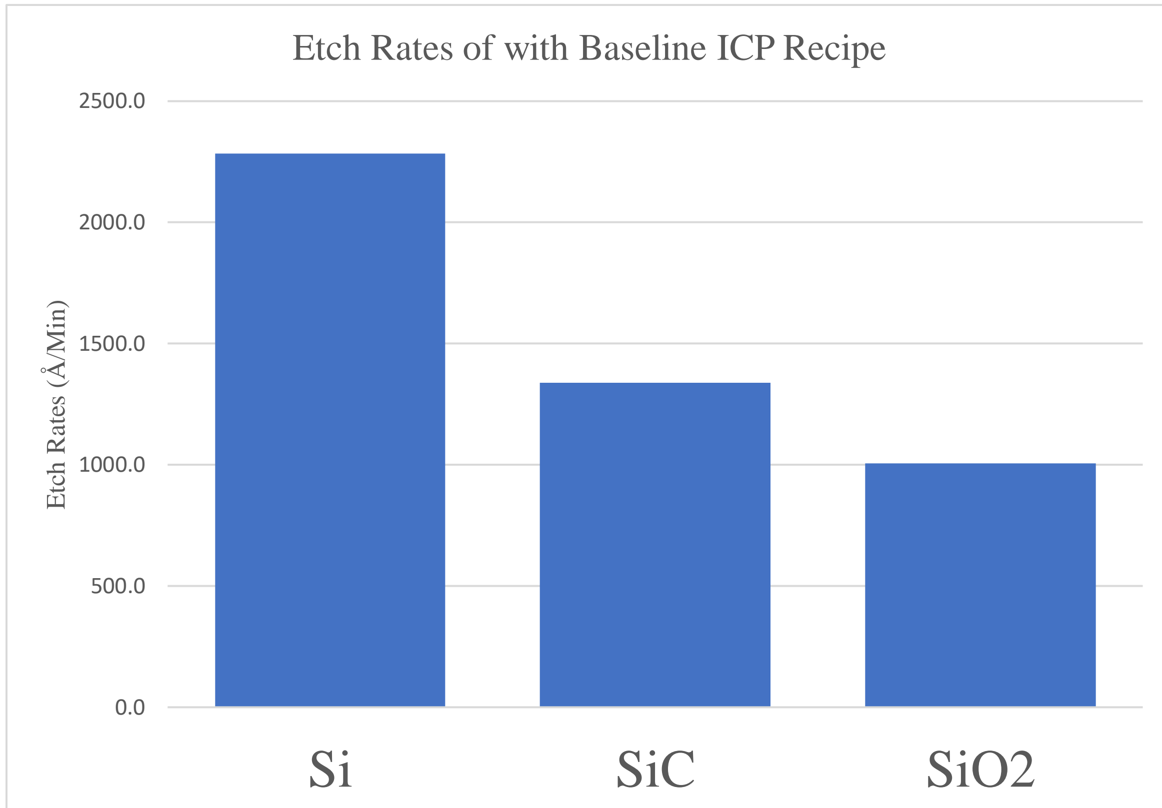


Figure 4.3 Average etch rates of the baseline ICP recipe

These results show what was expected. Si has the highest etch rate, while SiO_2 has the lowest. SiC is in between. These results were then used to plot the selectivity between each material. These results are shown in Figure 4.4.

The selectivity of a given material pair tells how the materials are etched when stacked on one another. This value is useful for determining the likely hood of over-etching through the target material to the underlying substrate. A highly selective material pair indicates that the

likelihood of over-etching is low. The underlying substrate has a lower etch rate than the target material. Therefore the target can be etched entirely through without fear of etching a large amount of the substrate material. A selectivity value close to 1 indicates that both materials have similar etch rates. So, an over-etch is likely. A selectivity value that is much lower than 1 indicates that the underlying substrate has a much higher etch rate than the target material. Therefore the likelihood of etching deep into the substrate is high. This should be avoided during IC fabrication. The selectivity value is useful for determining the effectiveness of a hardmask. For a hardmask to be useful, it must have a lower etch rate than the target material. This is to allow for deeper etches into the target material before the mask is etched away entirely. Of course, the thickness of the mask must be sufficient for the planned etch recipe. The selectivity is calculated by finding the ratio of $ER_{target}/ER_{substrate}$.

There is a high selectivity between Si and SiO_2, greater than two. This indicates that SiO_2 would make a suitable hardmask for Si if photoresist was not an option. It is possible that depositing SiO_2 using a CVD method would increase selectivity (Wellmann, Ohtani, & Rupp, 2022). For deep Si etching, a thick SiO_2 mask would be required because SiO_2 etches differently than photoresists. SiO_2 etches at a constant rate while photoresist does not. A photoresist is made up of various components that etch at different rates, so the photoresist does not etch at a constant rate. These results also show that etching the field oxide down to the SiC surface has a high probability of over-etching. This is because the selectivity of SiO_2 to SiC is less than one. This is a low selectivity which can make it difficult to stop the etch at the intended depth. The N+ or P+ regions are likely to be etched, so the etch profile of these regions must also be studied.

Figure 4.5a) shows an intrinsic SiC sample with a layer of photoresist applied. This sample was then etched using the baseline ICP recipe, and the photoresist was removed. The

results of the ICP etch are shown in Figure 4.5 b) These images side-by-side show how small features that appear in the photoresist are shrunken by the end of etch. Sufficiently small features do not appear in the etch at all. This is due to the critical dimension bias of the etch. This CD value will need to be measured in order to calibrate the mask design to mitigate and account for this phenomenon.

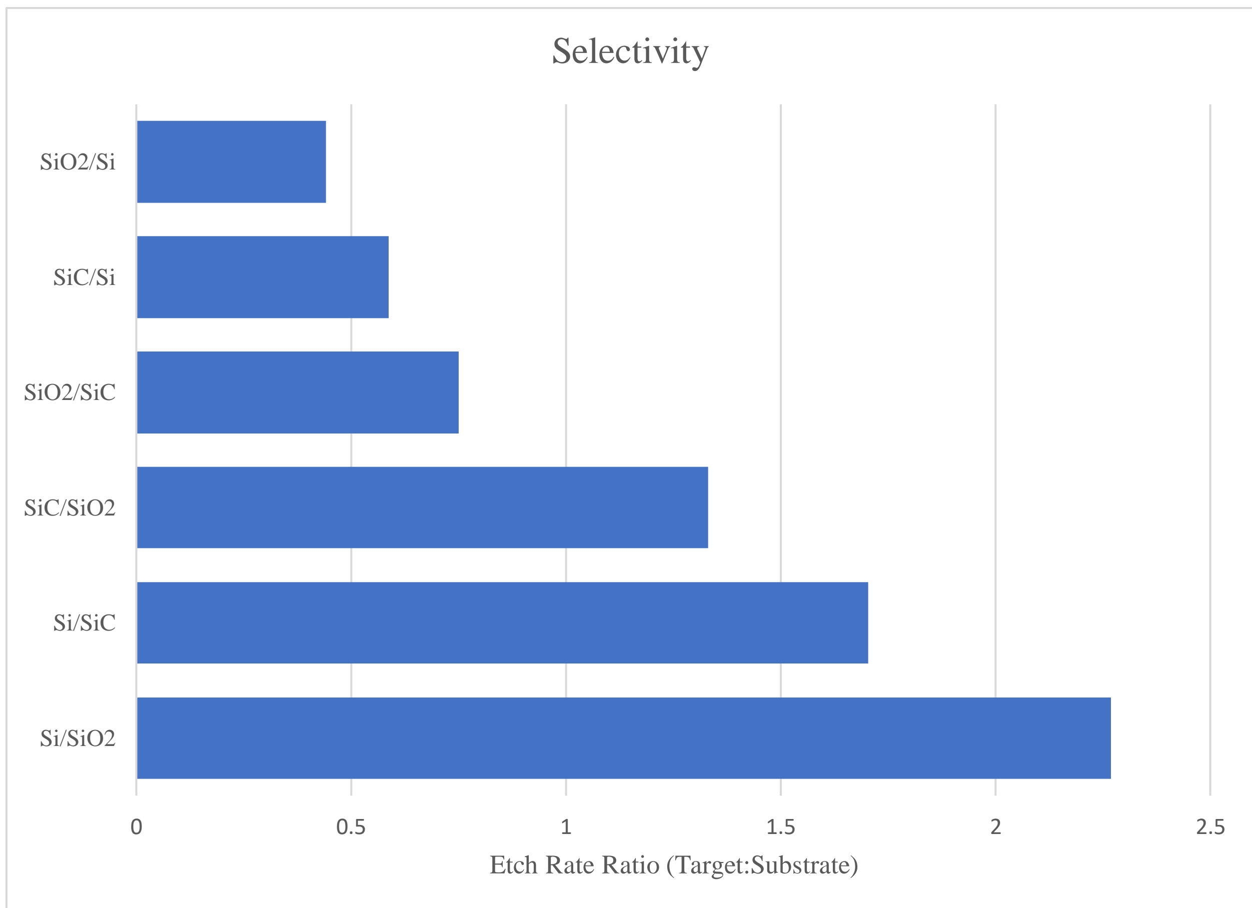


Figure 4.4 Selectivity between SiC, Si, and SiO_2

When describing the critical dimension is important to understand that CD cannot be universally determined for all etch scenarios. There are countless variables that can change the CD, and it can be different across a single wafer. The CD is affected by things like the etch

depth, the profile angle, the feature shape, the surface area of the feature, etc. When these CD bias measurements were conducted, they were all done on the same feature on substrates that were all etched under similar conditions.

Critical dimension bias is typically measured with a CD-SEM , which uses software to automatically measure the dimensions of a feature. CD-SEM is not accessible at this time, so a simpler method was utilized. This was measured using the image processing software Fiji ImageJ. This software counts the pixels of a given length or area and then applies the scale of the image to determine the value of a certain length in microns. The dimensions of a rectangular feature were measured by measuring the innermost line of the feature. This gives an estimated value for the length and width of the rectangular feature that was designed to be 10 µm by 30 µm. The length and width were taken at three points on a single sample, then averaged together. A total of four samples were used to collect data, two intrinsic SiC, one N+, and one P+. Comparing the change in distance from the photoresist and the size of the etch will give the CD bias. The CD bias from the photoresist dimensions to the etch dimensions was found to be approximately 2.2 µm.

The AutoCAD design for this particular feature was 30 µm by 10 µm. The average dimensions of the final etched feature were 25.4 µm by 5.4 µm. Both the height and the width decreased in size by 4.6 µm. That is the total CD shift. When analyzing small features of only a few microns, this is a sizable shift. To some degree, this value can be decreased. Using high-quality masks for alignment can help. Improving the photolithography procedure can also help. The largest factor contributing to the CD shift is the CD bias between the photoresist and the final etch. The reason the CD bias is so large is due to the profile angle. Figure 4.6 shows an SEM image of an N+ SiC sample etched with the baseline recipe at a 52° angle

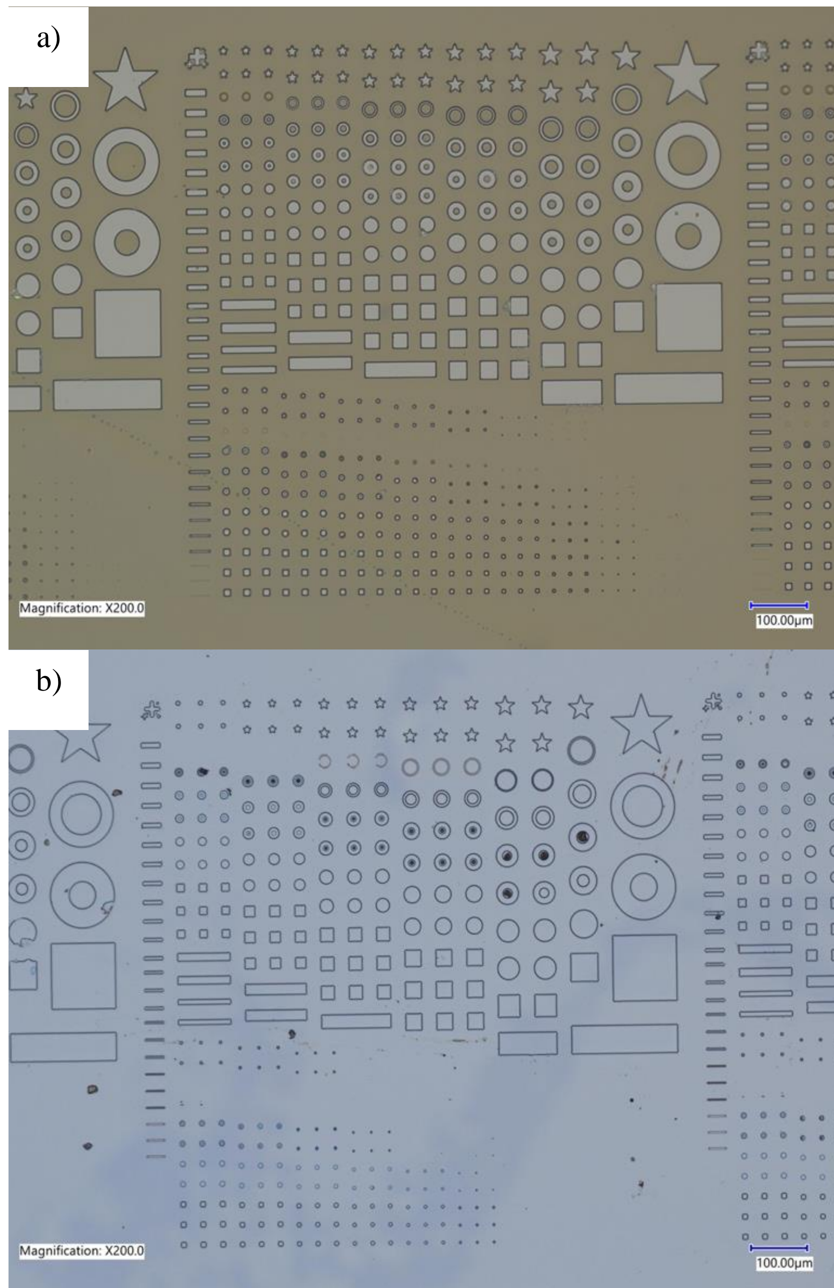


Figure 4.5a) SiC with photoresist applied before an ICP etch. b) the same SiC sample after the ICP etch with the photoresist removed

The SEM image shows a rough sidewall that is highly tapered. This angle is the cause of the high CD bias. The possible reasons for this tapering, along with possible solutions, will be described in later sections. The profile angle was attempted to be measured but unsuccessfully.

In most literature, the etch profile can be captured with SEM using FIB. A portion of the etch feature can be etched away. Then the viewing angle can be changed to 90°, and the profile can be clearly seen. Then the angle can be visualized as well as measured. This viewing angle was not achieved in this study. The maximum viewing angle that was achieved was 52°. At that angle, the FIB etching did not enhance the viewing perspective. Therefore, the angle had to be measured in a different, less reliable fashion. The depth of the etch was measured using the profilometer, then the horizontal distance of the tapering was measured by counting pixels from the SEM images taken at 0° degrees. The acute profile angle can be calculated using trigonometry. Two samples were measured. The average vertical distance was 1400 Å, and the average horizontal distance was 8500 Å, lending a profile angle of 9°. This angle is far smaller than expected and much less than found in the literature (Tseng & Tsui, 2016). The SEM images do not appear to have an angle that small. This unexpected value is suspected to be incorrect. Two separate methods were used for measuring distance, these two methods were not extremely accurate, and they were not calibrated together. This value cannot be trusted, and a more reliable method such as SEM images with FIB must be used in the future.

Now that five parameters for etching characterizations of the baseline recipe are determined, the baseline ICP recipe has been characterized to the best of our ability. New ICP etching experiments can be explored with a baseline study to compare them. The cause of the tapered profile can also be studied

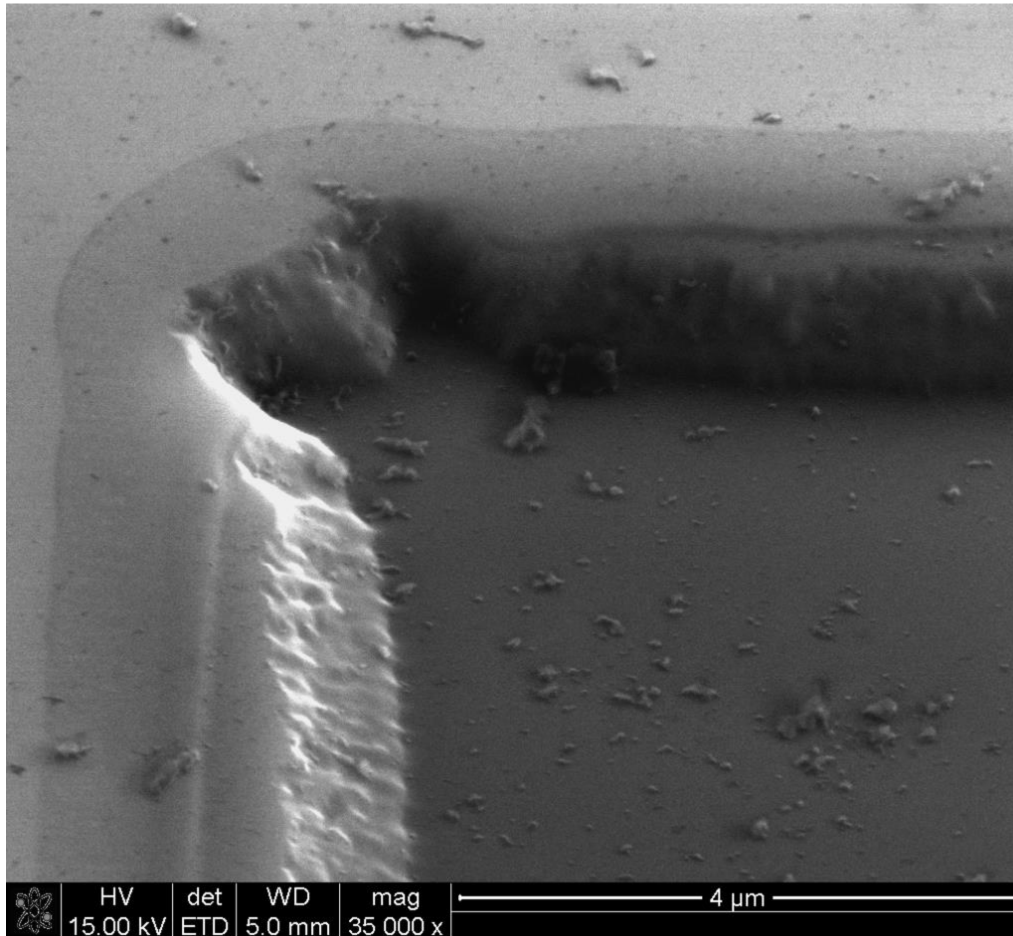


Figure 4.6 SEM image N+ SiC etched with the baseline ICP recipe shown a 52° angle

4.2.2 ICP Gas Flow Composition

The etch rates and selectivity of various materials used in SiC CMOS fabrication have been measured and calculated for the baseline recipe. The baseline recipe has a constant flow rate of 38 sccm that is made up of 13sccm Cl_2 and 25sccm BCl_3. The gas combination can have a large effect on the etch characterization (Zhou, Cao, & Liu, 2010; Ekinci, et al., 2014; Y. H. Lee, Yeom, Lee, Yoo, & Kim, 1998; Wang, et al., 1998; J. K. Sheu, 1999; Lin Sha, 2003). Up until now, no etch experiment has been conducted in our lab using different combinations of chlorine-based gases, and few studies have been conducted by etching SiC with Cl_2/BCl_3. This next study

is going to attempt to look at how chlorine concentration affects the etch characterization and determine the optimal gas flow configuration that creates the highest selectivity among different doping concentrations of SiC.

The baseline study is approximately 34% Cl_2 by volume. Five new etch recipes will be attempted with identical parameters except for the gas flow configuration. The total gas flow rate will remain at a constant 38 sccm, but the configuration will vary. The ratios that will be explored are 0%, 34%, 50%, 66% and 100% Cl_2. Recipe #2 is the baseline recipe used in the previous etching experiment.

This gas flow rate study is going to focus on the etch rates and selectivity between the variations of intrinsic and doped SiC. The materials that will be used will be samples of intrinsic SiC, N-well, N+, P-Well, and P+. A minimum of two samples of each material will be used for each etching recipe except for N-well. Due to material availability at the time of this study, we were short one N-well sample. The majority of the data for this study was conducted over two days, with a three-month gap between (due to material and equipment availability). Each recipe was done with large batches containing all samples at once, except for Recipe #4, which was conducted in two separate batches. Multiple batches were conducted in series to save time on machine boot-up procedures. Each batch was etched for five minutes except for Recipe #2. Being that Recipe #2 is the baseline study, the data from previous studies was used for this comparison. No redundant data was taken with the baseline recipe. The gases were set to a constant flow rate as the etch was running. However, the recipes at the upper and lower extremes (Recipe #1 and #5) had difficulty reaching or maintaining the set flow rate. Recipe #1 couldn't reach the set flow rate of 38 sccm BCl_3, and Recipe #5 reached the set flow rate of 38 sccm Cl_2 but couldn't maintain a constant flow rate and began to slow down as the etch neared the end.

The photolithography procedure preceded the etch experiment by less than 24 hours, where all samples scheduled to be etched were processed simultaneously. Then the samples were stored in a dark, clean room environment where they were etched the next day. Never leaving the cleanroom or encountering outside light. No sample that had undergone photolithography was left in the cleanroom for longer than a 24-hour period. Due to this precaution, it was impossible to collect data on the CD bias and resolution of the photoresist that had been deposited because this would require removing the samples from the clean room environment and exposing the photoresist to the intense light of the optical microscope. Therefore, CD bias data cannot be collected from the photoresist to the etch.

The etch rates can be displayed as a function of the gas composition. Average SiC etch rates are shown as a function of the % Cl_2 by vol. in the total gas mixture. We can see how etch rates increase with higher concentrations of Cl_2 in the gas mixture. Etch rates increase linearly until the mixture reaches approximately 50% Cl_2 to 50% BCl_3, where it begins to plateau. These results show that Cl-based gas chemistries are very robust when etching SiC. The Cl_2 percentage does not play a large role in the etching performance after a concentration of 50% Cl_2. As mentioned previously, the extreme ends, 0%, and 100%, of this study were difficult to maintain. The ICP machine was unable to maintain a constant flow rate at the desired 38 sccm. This also indicates that this is robust gas chemistry. The etch rates follow the same trend. If the ICP happens to malfunction and the flow rate is unstable, this gas recipe can still be relied upon. The average SiC etch rate of all samples is shown in Figure 4.7.

If the etch rates are grouped by dopant, something interesting and unexpected emerges. This is shown in Figure 4.8 Each material follows the same trend, again indicating this is a robust recipe until the Cl_2 percentage reaches approximately 66%. Here the etch rates begin to

diverge before converging again at 100% Cl_2 concentration. This divergence occurs at Recipe #4.

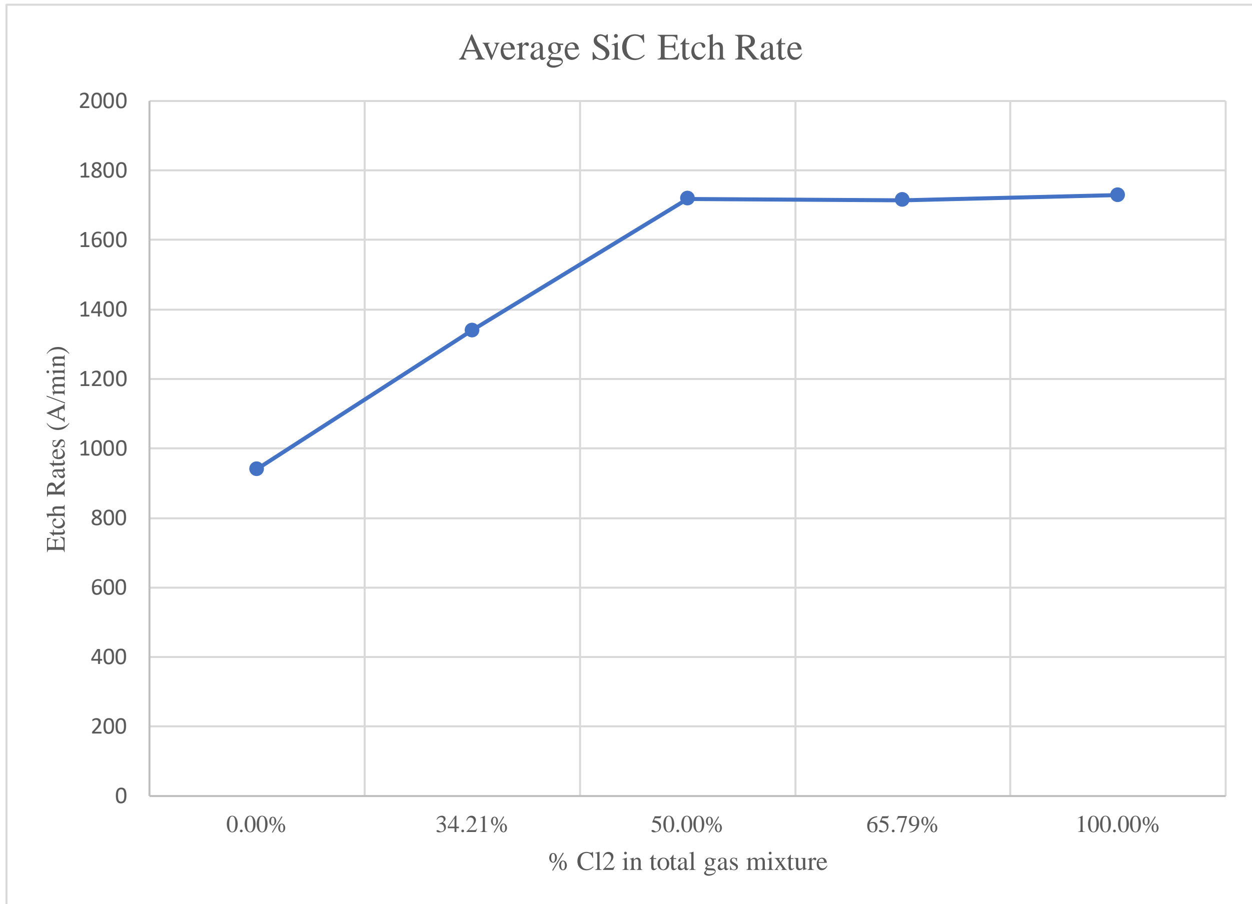


Figure 4.7 Average SiC etch rate by chlorine percentage

Figure 4.9 shows the etch rates of each material plotted on a linear scale with the doping concentrations plotted on a logarithmic scale. From this graph, a relationship can be seen. The etch rates are related to the doping concentration, regardless of the dopant species. We see that intrinsic SiC has the highest etch rate because there are no dopants. P+ SiC has the lowest etch rate because it has a doping concentration of 5E19 cm^{-3}. This data shows that the doping species is irrelevant. P-type samples are doped with nitrogen, while N-type samples are doped with

aluminum. Recipe #4 etches only the SiC crystal and is slowed down by impurities regardless of the material.

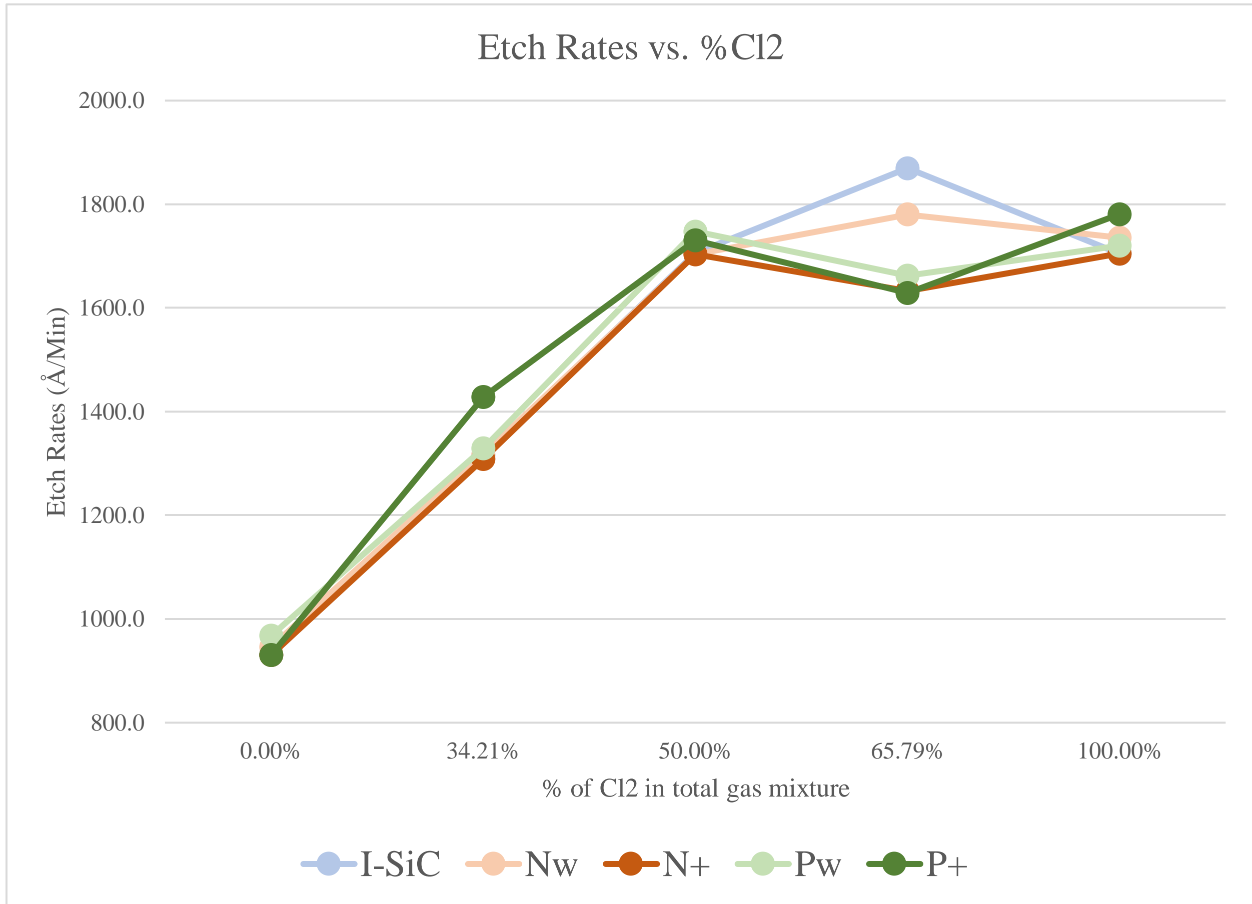


Figure 4.8 Etch rates of doped SiC

SEM images of the P+ SiC samples were taken to analyze the etch profile of recipes #2, #3, and #4. The images are shown in Figure 4.10. Many things can be learned from these images, as well as questions that have yet to be fully answered.

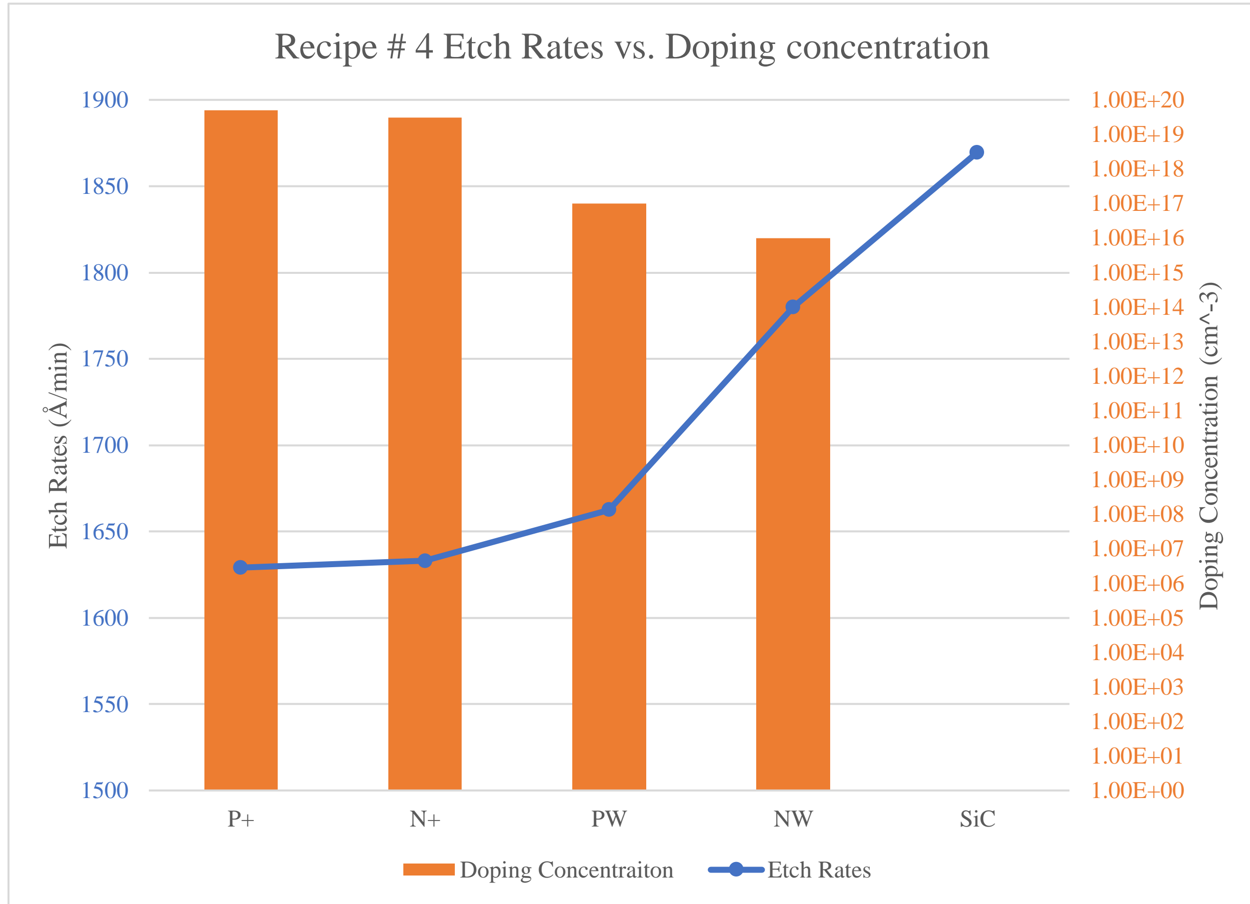


Figure 4.9 Etch rates of samples etched with Recipe #4 vs. doping concentrations

Firstly, there appears to be a grain pattern on the surface of the substrate. This is a phenomenon that occurs during the epitaxy growth of P-type silicon carbide, known as step-bunching. It has been reported on and determined to have a negligible effect on electrical performance (Chao, et al., 2015). Each of these samples happened to be diced from the same wafer, so it makes sense that each would have the same step bunching. Next, the floor of etch is very smooth. This is due to the Cl_2/BCl_3 gas chemistry, which has been shown to produce smooth surfaces (Ekinci, et al., 2014). There are a few spots on the floor of the etch profile that are not smooth. It is likely this is contamination from debris that was collected during

transportation. The debris appears to be proportional outside the etch as well as inside the etch. The sidewalls, however, are much rougher than the floor of the etch, and the corners of the rectangle are also rounded in a fashion that looks similar to the leaves of a clover. This roughness appears to be contributing to the tapered sidewalls and the high CD bias. Lastly, in recipes #2 and #4, it appears there is a step from the edge of the etch profile to the top of the tapered sidewall. Between these two points, there is a flat region that looks similar to the etch floor.

The step could possibly be caused by a deteriorating photoresist. As the etch process takes place, the photoresist is also being etched. Because we are using a developer with a slower development rate, the sidewalls of the photoresist are tapered. This could mean that the thinner areas of the photoresist are being etched away entirely after some time, and a larger area is exposed to the ions later in the etch. This could be why the step occurs. A similar etch profile has been documented in (Pearton, Shul, & Ren, 2000)

The rounded corners and the rough sidewalls are believed to be from the same cause. Sidewall passivation. During the etch process, sometimes a radical etch by-product is ejected from the surface of the substrate and flung in a random direction. Occasionally, the by-product re-deposits on the surface of the sidewall, creating a micromask that hinders the etch process. This creates a tapered sidewall and a rough surface. This is the likely cause of the rough sidewalls shown. It is unsure at this time what by-products that are causing this sidewall passivation, but there are a few possibilities.

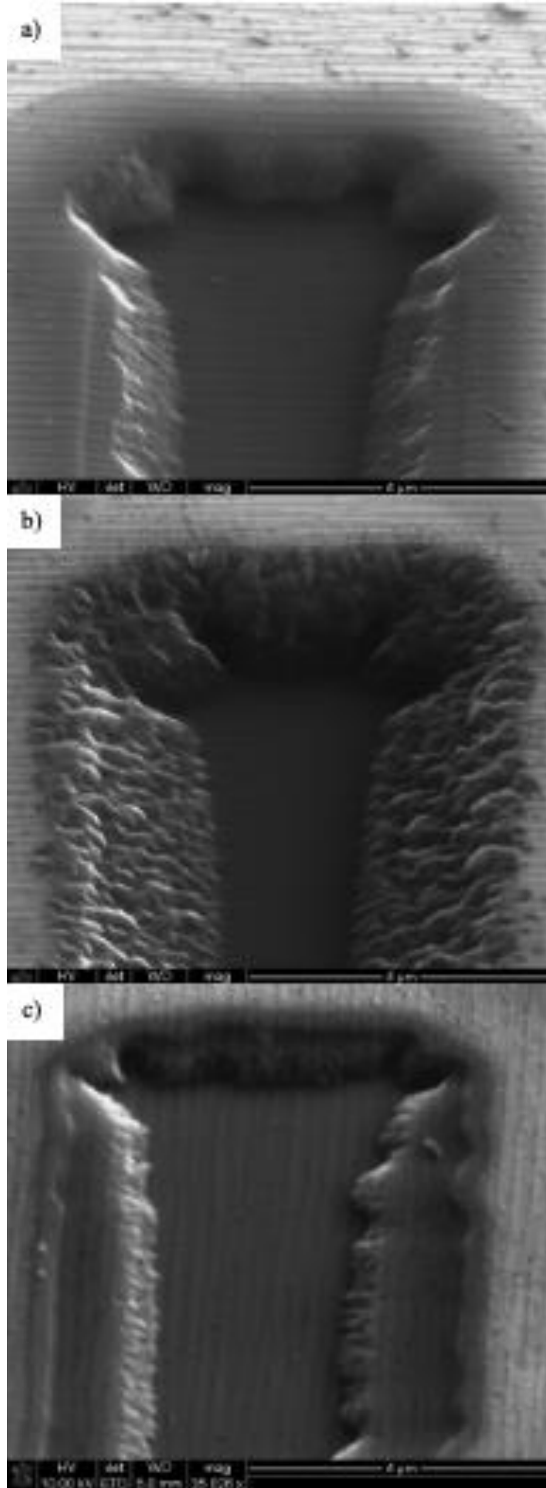


Figure 4.10 SEM images of the etch profile of P+ SiC samples etched with a) Recipe #2 b) Recipe #3 and c) Recipe #4

Sidewall passivation from Cl-based chemistry has been discussed in the literature (Tseng & Tsui, 2016). One likely possibility is sidewall passivation from a photoresist. Photoresist has been known to redeposit onto the surface, creating a micromask effect. It is possible the micromasking is occurring on the sidewall. Another possible explanation for the sidewall passivation is Chlorine radicals. Chlorine ions can react with the surface of the SiC and create $SiCl_x$, CCl_x ($x \leq 3$), or other molecules. These radicals can also deposit themselves on the surface of the sidewall, which can slow the etching process down. The last possible explanation for the sidewall passivation is the least likely, but still possible. Oxygen can bond with silicon to form silicon oxide or bond with chlorine to form oxychloride. This is common when SiO_2 is the masking material. These can also deposit on the sidewall. This possibility is the least likely because there should be no oxygen in this chamber. There is no oxygen in the etching recipes, so how could the oxygen be entering the vacuum chamber? The oxygen source could be coming from the surface of the photoresist or the surface of the SiC substrate. These surfaces can oxidate from oxygen exposure. These samples were never stored in an N_2 dry box, so oxidation is likely, but the oxygen concentration should be low. Another source of oxygen could be from the photoresist. As discussed previously, the photoresist converts to a carboxylic acid during exposure, meaning it absorbs the humidity from the air (Mack, 2007). Some of these carboxyl groups could be left behind, which can contribute to the oxygen concentration in the chamber.

It is unsure which of these possibilities is the cause of the sidewall passivation. It could be any combination of these. There are some ways to test these theories. EDX can be used to determine the materials on the substrate. If Cl or O is found on the substrate after the etch, these could be large indicators of the cause. If there is an unexpectedly high amount of C, this could be a sign that the photoresist is the cause of the passivation. If oxygen is the cause, removing the

oxidation prior to the etch could reduce the passivation. BOE or piranha etch can be used. If Chlorine is the cause, experimenting if F-based gas chemistries could solve this problem.

These ICP studies characterized a Cl_2/BCl_3 ICP recipe as well as experimented with new gas compositions. The gas composition study determined that Cl_2/BCl_3 ICP recipes are highly robust. Any small change in composition, doping concentration or flow rate will not have a large impact on the etching results for SiC. These recipes result in smooth surfaces, but sidewall passivation was found to be a problem. The next section is going to explore SiO_2 etching with BOE, as well as BOE alternatives.

4.3 Oxide Etching Development

SiO_2 will be studied in this section for the purposes of etching insulating oxide layers of SiC CMOS devices such as gate oxide or field oxide. It will also be used for etching hardmasks for ICP etching with high selectivity.

4.3.1 Buffered Oxide Etching

As mentioned previously, SiO_2 is a commonly used hardmask for polysilicon (Ekström, 2019; Tseng & Tsui, 2016). This was verified by etching both Si and SiO_2 with ICP to show the high selectivity between Si:SiO_2. However, creating a SiO_2 hard mask with an accurate pattern transfer for small features can be a difficult task. This next study will be to attempt a Si etch using an oxide hardmask. Then to explore various ways that the oxide hardmask can be developed. Methods that will be used include buffered oxide etching, ICP, and Liftoff.

An ICP etch using Recipe #2 (baseline recipe) was attempted on a silicon substrate with an oxide hardmask to explore if a hardmask etch could be recreated in our lab with our deposited

SiO_2 sputter deposition. The Si samples that were used in this experiment had already been prepared because they were the same samples that were used in the early BOE experiments that have already been described and shown in Figure 3.7. The samples chosen were the samples etched for 40s and 60s because these samples had large areas where the oxide had been etched all the way through, and the Si substrate was exposed. This would allow for the Si to be etched while the oxide acts as a mask. Unfortunately, the isotropic nature of BOE etching caused the oxide layer to have poor pattern transfer. However, observations can still be made from the accuracy to which the hardmask was able to transfer the patterns to the Si substrate. To ensure that the thickness of the oxide mask (about 105 nm) was sufficient for an ICP etch, the etch time was kept short. A 30s etch with Recipe #2 was chosen. After the ICP etch, the oxide layer was removed entirely by soaking the sample in a 10% BOE solution for 40s. The ICP etch rates and selectivity of this etch have already been described in the previous sections. In Figure 4.11, we see the results before the ICP etch and after ICP etch. Figure 4.11 a) shows the oxide layer that had been etched with 20% BOE for 40. Figure 4.11 b) shows the same sample after the ICP etch with the hardmask removed. c) shows the Si substrate with a layer of SiO_2 that was etched with the 20% BOE solution for 60 s. d) shows the same sample after the etch with the SiO_2 layer was removed by dipping the sample into a BOE solution with no mask until the layer was removed. Here we see that SiO_2 can act as a hardmask for Si. The areas of the mask that left the Si substrate exposed to the plasma were able to be etched, and the pattern in the mask was transferred. Some problems arise with this hardmask. Many of the areas were not uniformly etched. Some of the small areas in the mask were not etched entirely through. A thin layer of oxide remained in the area that should have exposed Si. In these areas, the Si was not etched, and the pattern was not transferred. The other problem is the isotropic nature of wet etching. The

liquid solution etches uniformly in all directions as opposed to plasma etching, where all etching occurs in a single direction. This causes the patterns in the mask to not be transferred correctly. The shapes gain rounded edges or begin to bleed out and touch the neighboring feature. For an oxide hardmask to be a viable tool for SiC CMOS fabrication, the hardmask deposition needs to be improved so that the pattern can be more accurately transferred to the Si substrate.

The first attempt to improve the oxide hardmask deposition is to characterize the BOE etching procedure. This meant determining the etch recipe for giving the highest pattern transfer resolution and uniformity. Etch rate values are not useful when the etch is not uniform across the sample. According to (General Chemical Electronic Chemicals Group), the etch rate for a pure BOE 5:1 solution is 102-112 nm/min at room temperature. Our ellipsometry measurements show the estimated thickness of the oxide layer was 132nm. This was verified with a profilometer after the etch to show an average thickness of 130.8nm. In our experiment, we diluted the solution from 20% BOE (5:1) to 80% H_2O by volume. This should drastically reduce the etch rate of the solution to approximately 22nm/min. Even when considering reasonable error or variations in room conditions, the 40s etch, and the 60s etch should not be etched entirely through to the substrate, yet that is what we see in Figure 3.7. This is likely due to the non-uniformity of the etch. The larger features have more surface area in contact with the etching solution, which results in a faster etch rate. Therefore, BOE characterization experiments will focus on uniformity and pattern resolution. Most observations will be qualitative. To create a more uniform etch, the 20% BOE solution was reduced to a 10% BOE by volume solution. The

intention behind this was to slow the etching down to give the smaller features more time to be in contact with the etching solution.

The first etch experiment using a 10% BOE solution was conducted using one Si substrate that was deposited with a thicker SiO_2 layer, about 350-400nm. The thicker oxide results in green color. The Si substrate was cleaved into four quadrants. Three of the quadrants were used for this study, and the fourth was held back for a future study. Each of the three samples were submerged in a 10% solution for the same amount of time as the first BOE

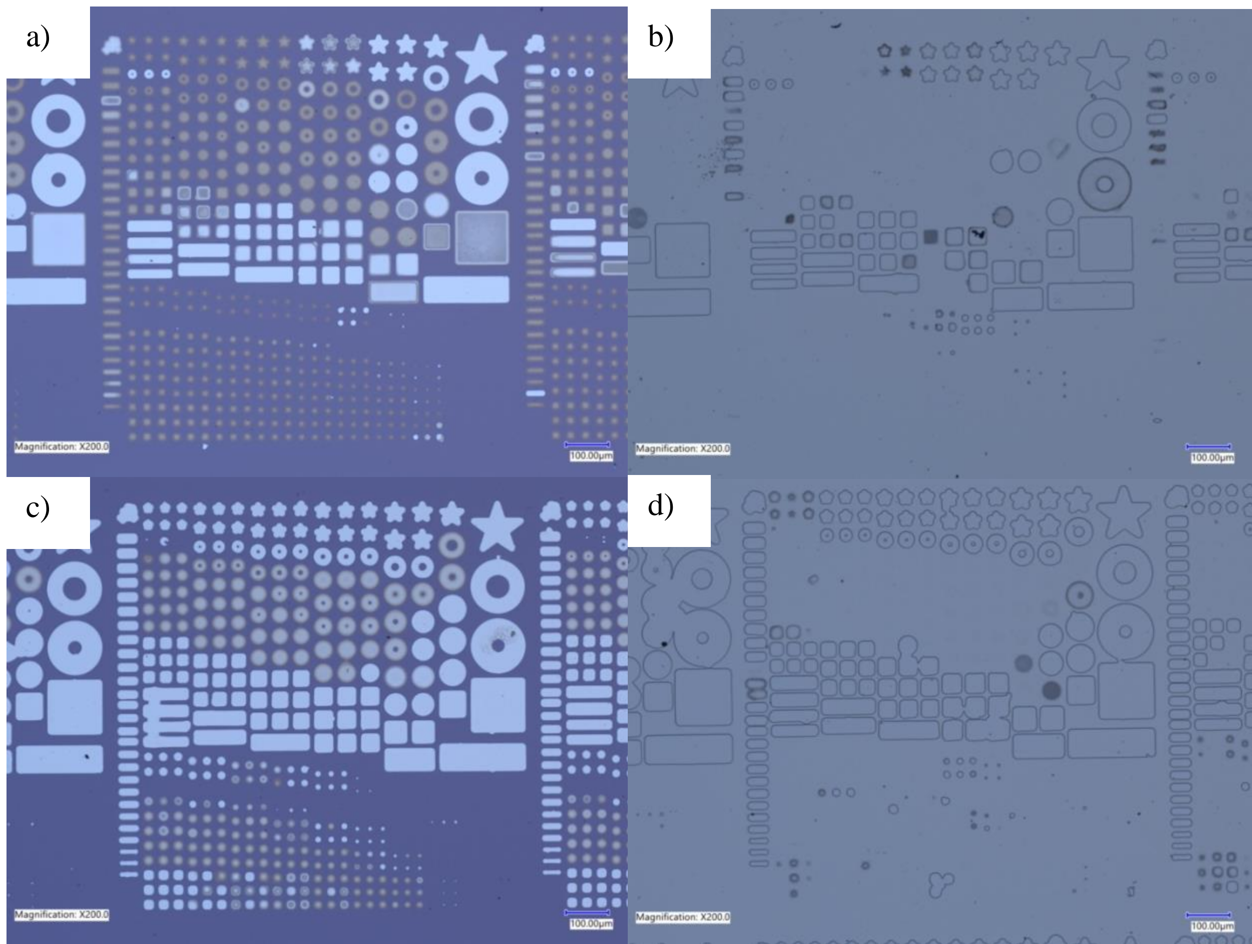


Figure 4.11 a) Si substrate with an SiO2 layer that had been etched with BOE for 40 s. b) the same sample that had been etched with ICP for 30 s then the SiO2 hardmask was removed. c) a Si substrate with an SiO_2 layer that had been etched with BOE for 60s. d) the same sample after a 30 s ICP etch and the hardmask was removed.

experiment: 20s, 40s, and 60s. The expected etch rate from the literature was 110 Å/min

(Spierings, 1993). The surface was too shallow and too rough for the profilometer to accurately measure the etch depth, so AFM was used. The results showed that the etch rate was approximately 40Å/min with the 10% solution and 34 Å/min with the 5% solution. As hypothesized, the etch rate was reduced but by a greater amount than expected. The oxide was not etched entirely through. As a continuation of this study, three more samples were etched for increasing amounts of time: 80s, 100s, and 120s. The fourth sample that was held back was added to this new study and was etched for 120s. Two more samples from a different substate were also added to this study and etched for 80s and 100s. This is the explanation for the variations in oxide color. The purple oxide color is likely a thicker layer of oxide, it does not indicate a different quality of oxide Figure 4.13 Oxide samples that were etched in 10% BOE solution for 40s, 80s, and 120s show three of the six total BOE etches that conducted. The entire samples are shown to emphasize the lack of uniformity across the samples.

We can see from Figure 4.13 that there is a slower progression in etch depth, indicating a slower etch rate, as hypothesized. Nowhere on the sample was the oxide etched entirely through to the substrate. There still lies the problem of etch uniformity, both across the entire sample and uniformity between feature sizes. We can also see increased etch depth along the edges of the samples. In a further attempt to increase uniformity by slowing the etch rate down, a 10% BOE solution was used with three more SiO_2 samples. The etch times were: 80s, 100s, and 120s. These times proved to be too short. Etches were too shallow to make any qualitative observations with an optical microscope.

At this point, we have attempted a 20% BOE solution etch for 20s-60s. This was deemed to be too high of an etch rate, thus etching the material too quickly. We have attempted etching with a 10% BOE solution for 20s-120s. This was deemed to have a lower etch rate but not low

enough to solve the problems of uniformity that we have seen. We have attempted etching with a 5% BOE solution for 80s-120s. This was deemed to have too low of an etch rate to make meaningful observations. The logical next step is to increase the etch time of the 10% and 5% solutions to maximize solution exposure time for the small features that are etched slower.

The etch times were determined by assuming an etch rate of 110nm/min for pure BOE 5:1 taken from (General Chemical Electronic Chemicals Group). Diluting to a 10% solution should give an approximate etch rate of 11nm/min. A 5% solution would give an approximate etch rate of 6nm/min. Using these estimated etch rate values, a target of 60nm and 120nm were chosen. The etch times are shown in Figure 4.12. Using Si substrates with a layer of SiO_2 between 350nm to 400nm thick, there should be no risk of etching down to the Si substrate. The hope of this study is to finally see uniform etching across the sample surface as well as between the varying feature sizes. If the oxide etch rate is faster than assumed, and the underlying Si substrate is exposed, as long as the etch is uniform across the sample, the recipe would be considered usable for developing a hardmask.

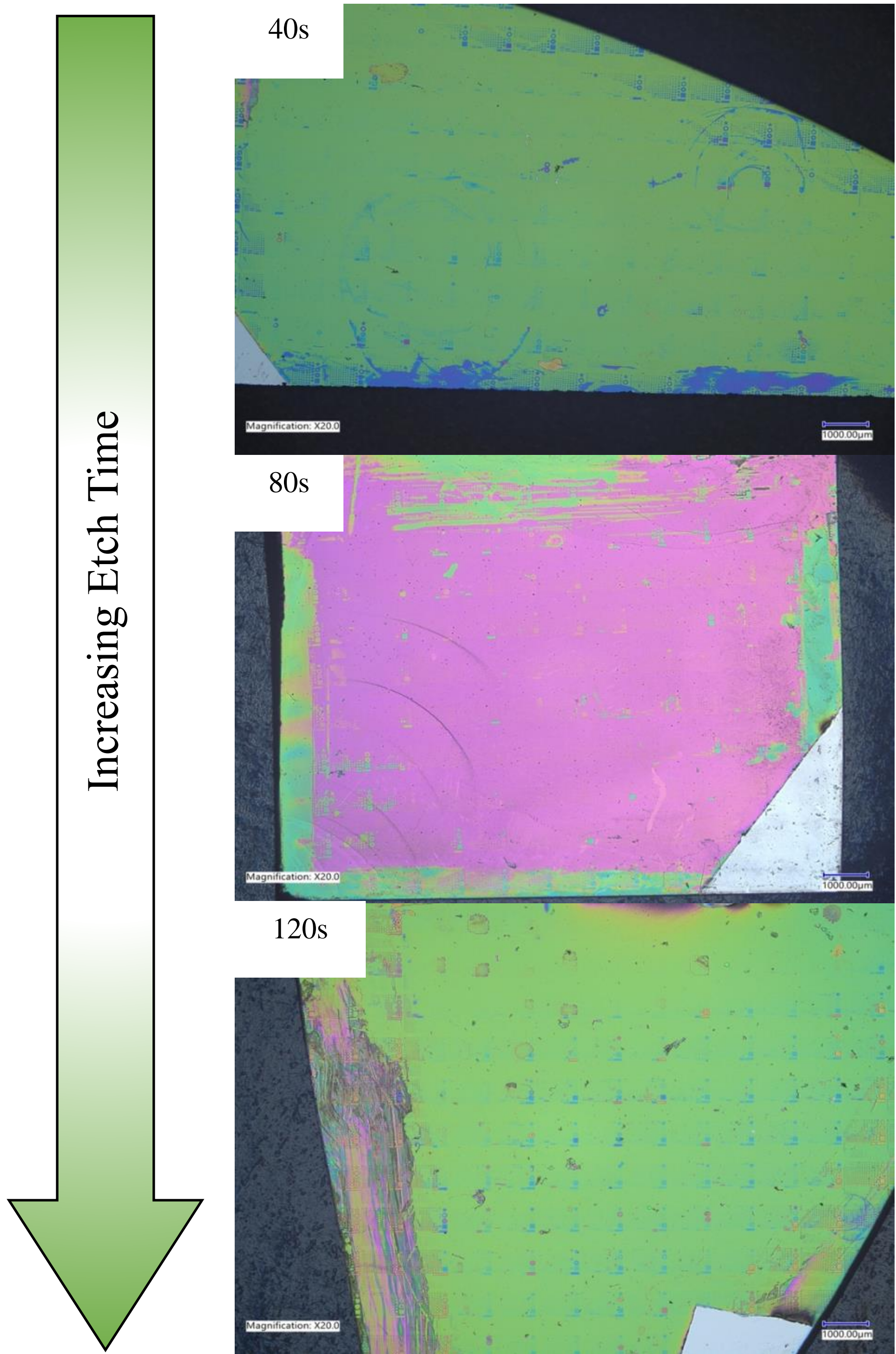


Figure 4.12 Oxide samples that were etched in 10% BOE solution for 40s, 80s, and 120s

Table 4.1 The etch times and expected etch depths of the two BOE solutions

Expected Etch Depth	10% BOE Solution	5% BOE Solution
60nm	5min	10min
120nm	10min	20min

In Figure 4.14, we see the results for the 5min, and 10min etches with 10% BOE solution. We can see that the solution etched entirely through the oxide layer down to the Si substrate. By profilometer, the oxide thickness was verified. The thickness was 360nm and 390nm for the two samples. Making the etch rate far greater than the expected etch rate but impossible to calculate exactly. The 5min etch was not uniform across the sample. Some regions show much etch depth, while others show little etch at all. For both etch trials, the etches were not uniform for varying etch sizes either. Many of the smaller features had a layer of oxide left behind.

In Figure 4.15 and Figure 4.16, we see the results from the 10min and 20min etches. We see both etches etched down to the Si substrate. The thickness of the oxide layer was verified at 390nm for both samples. This again indicates the etch rates were much faster than hypothesized. The most encouraging takeaway from this study is the similarity between the two BOE solutions. This experiment was designed to achieve similar results using two different etching solutions. Although the hypothesized etch rates were not replicated, the etch rates between the two solutions are similar. We can also achieve deeper etches with longer etch times. The pattern transfer is still undesirable for both solutions. The sample that was etched with the 5% BOE solution for 5mins produced the most consistent and uniform etch compared to all other samples. This sample would make a more suitable hardmask because more features would be transferred

to the underlying substrate. We can see in **Error! Reference source not found.** a close-up of the sample that was etched with the 5% solution for 20min. We can see a rainbow diffraction pattern surrounding the features. We can also see fringing happening at the borders of the features. This effect has been reported by Burham et. Al. (Burham, Sugandi, Nor, & Majlis, 2016). This effect is due to the photoresist weakening from being submerged in the etchant for long amounts of time. The solution described in that study is to increase the temperature of the etchant solution. This will reduce the time the sample is submerged, thus reducing the effect of the etchant on the photoresist.

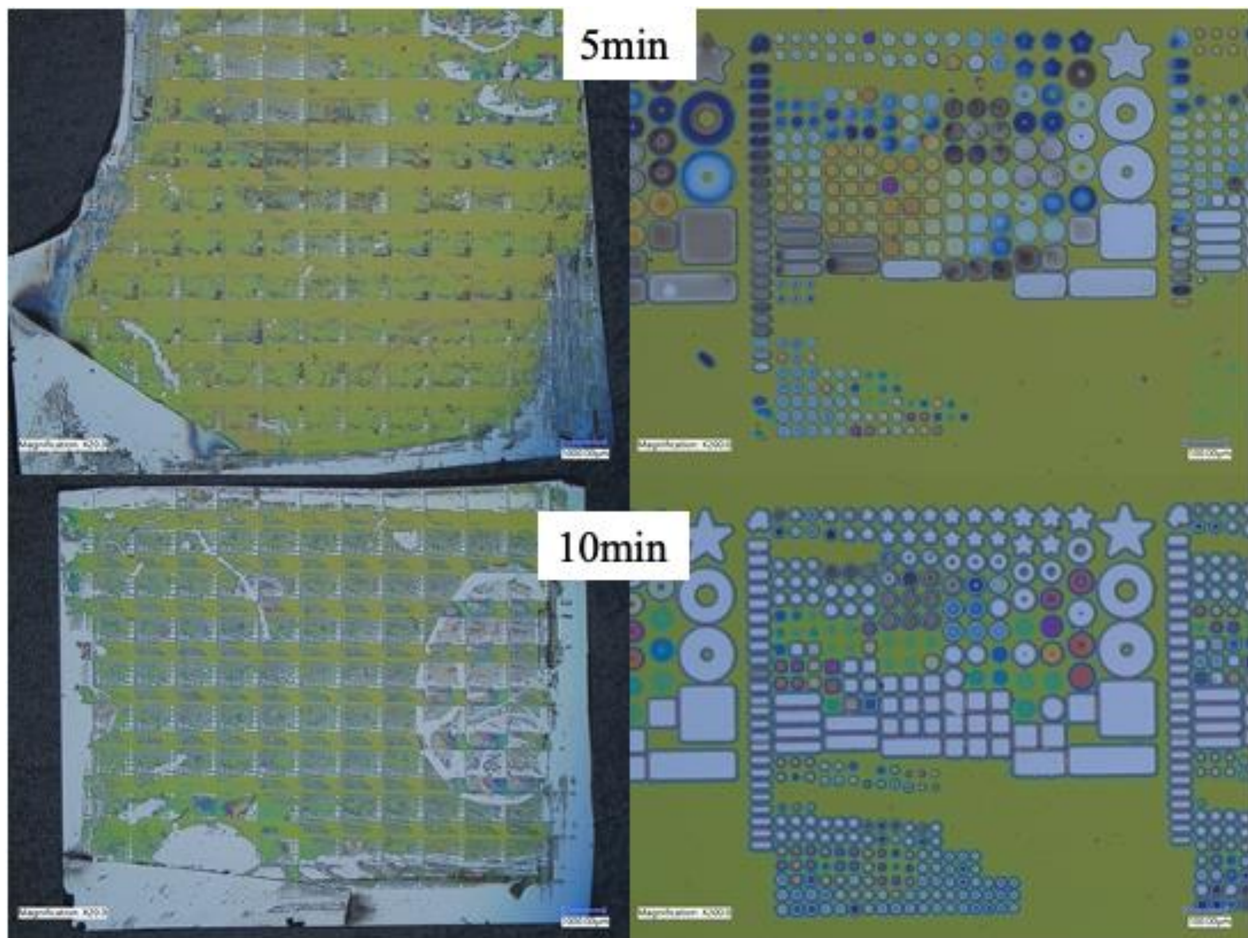


Figure 4.14 The two samples that were etched with the 10% solution for 5 min and 10 min

This method was not attempted in at the university facility. Given the health risks associated with hydrofluoric acid and the current conditions of the acid wet bench, it was deemed unsafe to attempt BOE at high temperatures. Instead, oxide etching was explored through the now familiar method of ICP etching, as well as a liftoff method.

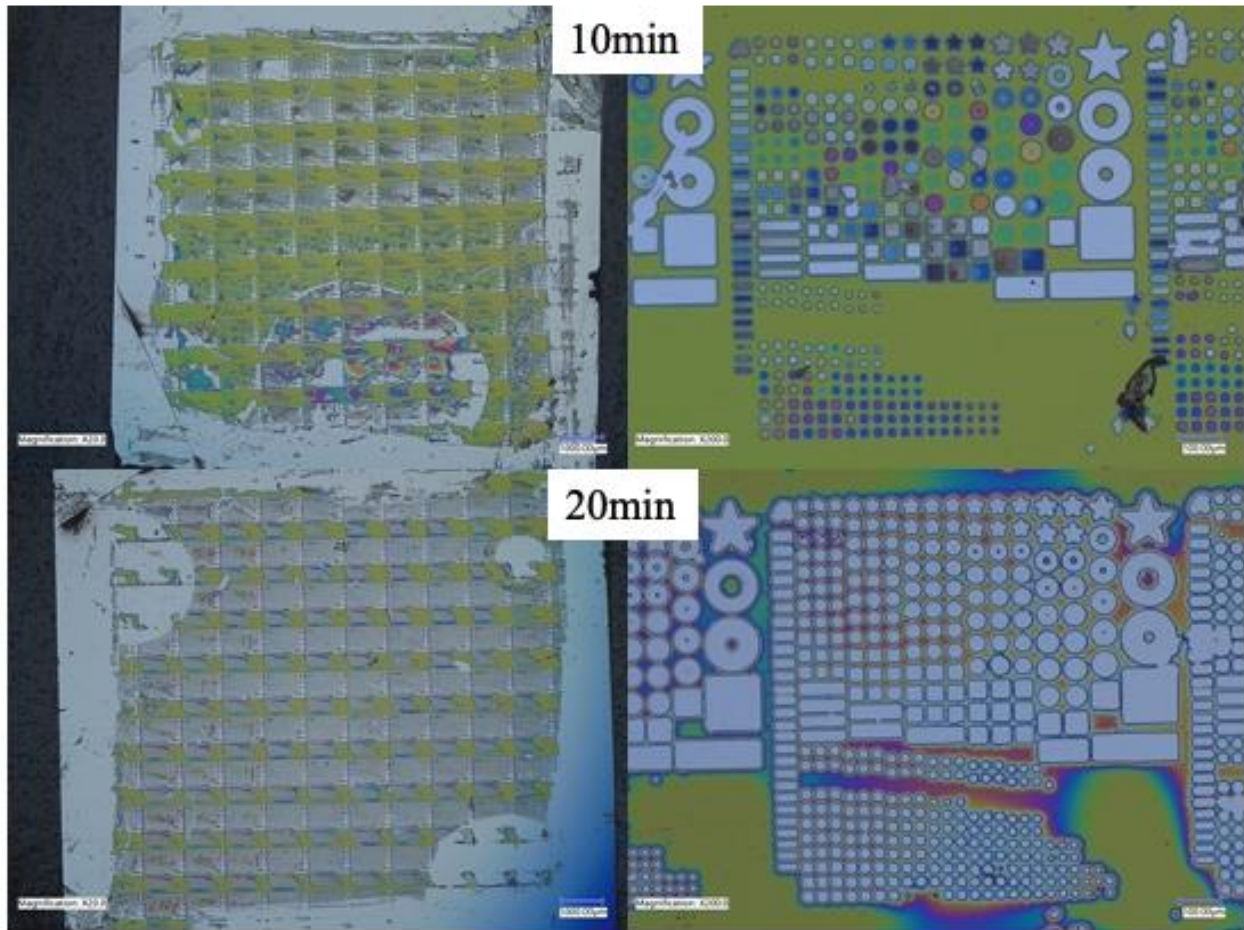


Figure 4.15 The two samples that were etched with the 5% BOE solution for 10 min and 20 min

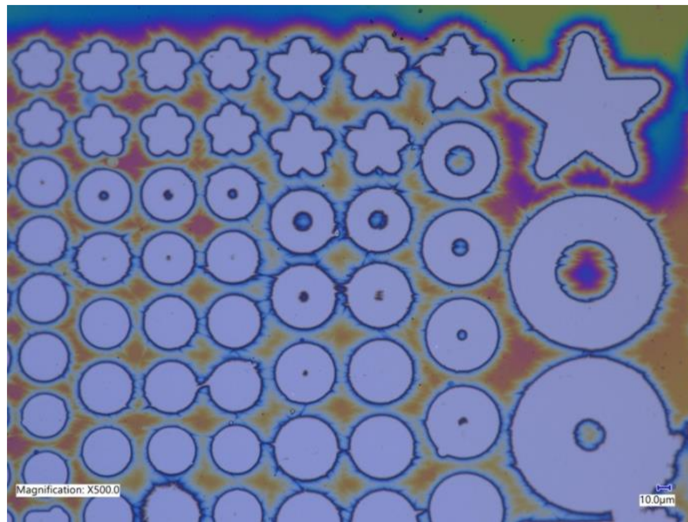


Figure 4.16 Detail image of the pattern transfer from the 20 min etch with 5% BOE solution

4.3.2 Oxide Etching with ICP

SiO_2 has already been etched with ICP. The etch rate data and selectivity has been described in chapter 4.2.1. This section is going to focus on the qualitative data collected from the SiO_2 etching experiments in comparison to the BOE etching experiments. Two ICP etching experiments were performed on Si substrates with a layer of deposited SiO_2 with a thickness of approximately 300 nm to 500 nm. The experiments were intended to replicate an etch procedure for creating field oxide, a thin layer of oxide. The other experiment was designed to create an oxide hardmask that could be used for etching polysilicon. Both experiments were etched with the baseline recipe on two samples with approximately the same thickness of the oxide.

The first experiment was to replicate an etch that might be used to replicate a field oxide etch. The etch experiment is designed to produce a thin layer of oxide without over-etching to the Si substrate. The estimated etch rate that was used for calculations was 104 nm/min. This was based on the first ICP oxide etch experiment. Without knowing the exact thickness of the oxide layer, a relatively conservative etch time was used, 150 seconds. This was estimated to give an

approximate etch depth of 260 nm. The expected oxide thickness after the etch was estimated to be between 40 nm to 240nm. One etched sample is shown in Figure 4.17.

The results shown in Figure 4.17 have a far higher pattern accuracy and uniformity than all previous BOE experiments. From the image, the pattern appears not to have been etched entirely through to the substrate. To confirm this, the oxide was removed after depth measurements were taken to determine if the underlying substrate had been etched. From optical microscope images, there did not appear to be any damage to the substrate, thus confirming the substrate had not been etched. The average etch depth for these two samples were 242 nm. Assuming a SiO_2 thickness of 296 nm (measured from a sample in the following experiment), the remaining SiO_2 thickness in the etched regions is 54 nm. A uniform, accurate, and precise thin layer of oxide was successfully produced using ICP.

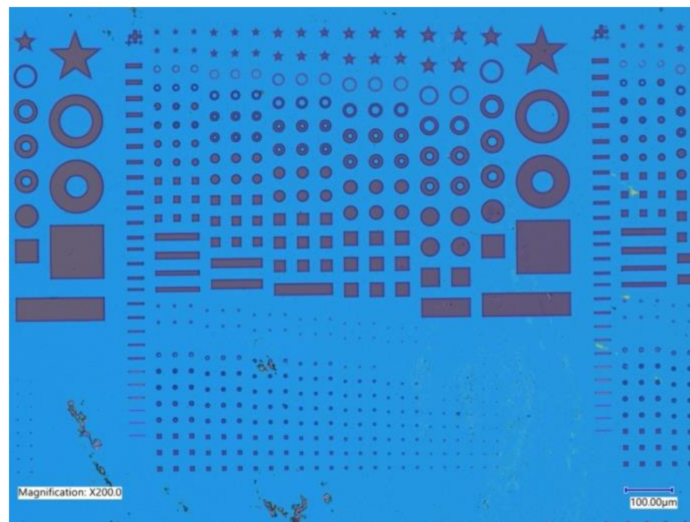


Figure 4.17 Oxide etched with ICP baseline recipe

The next experiment replicates an over-etch scenario. An etch that was intentionally designed to etch through the SiO_2 layer into the underlying Si substrate was performed. The purpose of this etch was to attempt a Si etch with an oxide hardmask but to do it in one etching step. This etch will test the selectivity of the two materials if it is accurate or not while also

showing if the pattern transfer can be improved upon from the past hardmask experiment described in chapter 3. This etch used two samples that were similar to samples used previously. The etch time was doubled to 5 minutes. Using the estimated etch rates of 104 nm/minutes for SiO_2, 234 nm/min, and the estimated SiO_2 thickness between 300nm to 500nm, the estimated total etch profile for the Si substrate will be between 45 nm and 500 nm, depending on how thick the oxide layer is. The results after the etch and photoresist removal are shown in Figure 4.18 a) where the oxide layer remains fully intact. Some residual photoresist remains because photoresist can be difficult to remove after long etches. Figure 4.18b) shows the same Si substrate after the oxide layer has been removed by soaking the substrate in a BOE solution with no mask.

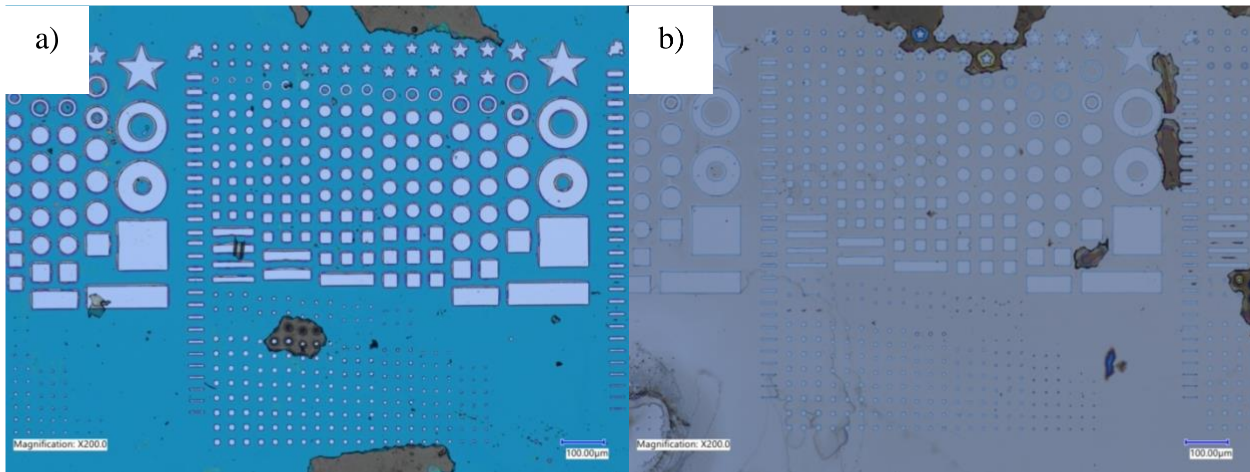


Figure 4.18 a) Si substrate with layer of SiO2 etched with ICP after the etch with photoresist removed. b) The same Si substrate after the SiO2 layer was removed

After measuring the etch profile, the results show the oxide thickness was 296 nm. The total etch profile was 575 nm. Thus the Si etch depth was 271 nm. With these two etch depths being nearly equal, the selectivity of Si:SiO_2 is close to 1:1. This is less than the originally hypothesized selectivity of greater than two. The figure shows a pattern transfer that is more

accurate and uniform than the BOE hard mask. There are no features that appeared in the hardmask that did not appear in the substrate. There is, however, a noticeable CD shift. Some of the smaller features in the substrate. This is due to the profile angle of the etch. As the etch goes deeper, the effects of the angle become more apparent. The profile in the mask becomes sloped enough that the plasma is not able to penetrate the surface of the substrate. Thus, a CD shift occurs, and small features are not transferred.

These two experiments show that ICP etching can be an improvement to BOE for SiO_2 etching. It can have a more accurate pattern transfer and a more predictable etch rate that is constant throughout the substrate. There are some drawbacks to using ICP to etch SiO_2 when deposited on a Si substrate. The Si substrate has a higher etch rate than SiO_2, so the risk of over-etching is likely. For robustness, a study was conducted to explore the possibility of creating an oxide hard mask without the use of wet or dry etching. A SiO_2 oxide liftoff was conducted.

4.3.3 Oxide Liftoff

The liftoff method is commonly used in IC fabrication for removing regions of deposited metals. It requires using a photoresist mask to block the metal from being deposited in specified regions. When the metal is deposited, it coats the entire surface of the substrate except for the regions where the photoresist has been deposited. Then by using acetone, or a stronger solution, the photoresist is removed, leaving behind only the deposited metal in the desired regions of the substrate.

Photolithography was performed on the substrate using the same photoresist and photomask as all previous experiments prior to this. Then the substrate was sent to be deposited with SiO_2. The same thickness of SiO_2 was deposited, approximately 300 nm to 500 nm. Then

the sample was submerged in TechniStrip® MLO 07. This solution is an advanced photoresist remover that is designed to remove the photoresist quickly while etching metal and oxides at a slow rate. The solution datasheet recommends a temperature of 65°C. However, better results were achieved by heating to a minimum temperature of 75°C. The samples were submerged for 3 minutes or as long as it took to remove the SiO_2. Agitating the solution helped increase the removal process. The results of this liftoff study are shown in Figure 4.19. Figure 4.19a) shows the Si substrate with the photoresist and SiO_2 deposited. Figure 4.19b) shows the same substrate after the liftoff process.

The images show the before and after the Techinistrip® MLO 07. Although Figure 4.19 b) looks like past etching experiments. It is inverted. The features are not etched into the surfaces. They are protruding out. This was verified using the profilometer to measure an average thickness of 422 nm. This is the thickness of the deposited oxide layer. The images show high pattern transfer accuracy with very little CD shift. Almost all features in the photoresist were transferred to the substrate.

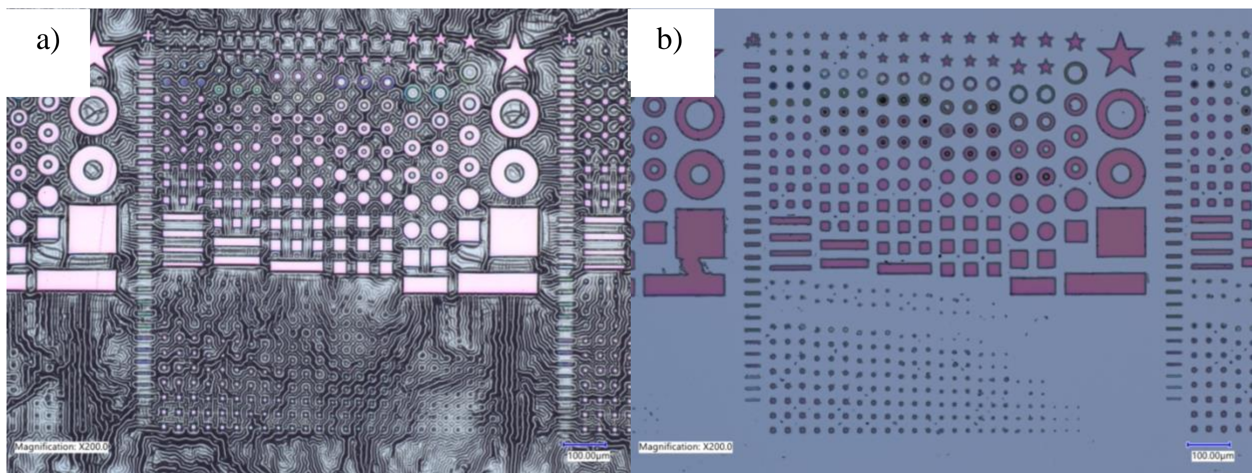


Figure 4.19 a) Si substrate with photoresist and SiO2 deposited. b) the same substrate after liftoff.

This chapter has described the steps taken to characterize and improve on the initial results of the photolithography, ICP etching, and SiO_2 etching. The resolution in photolithography has been improved by changing the photolithography recipe to be in line with the recipe recommended by the datasheet, and by studying the exposure times, a method for calculating the exposure time has been used to create repeatable results. The ICP etching baseline recipe has been studied with varying materials so that etch rates and selectivity of the materials have been measured. New ICP recipes have been attempted with intrinsic SiC and doped SiC to find how selectivity changes. Varying methods for etching SiO_2 have been explored for field oxide etching as well as oxide hard masks. These include methods include ICP, BOE, and a liftoff method. The results from these studies can be used to make assumptions about these methods, understand the trends associated with materials, and help develop the etching process modules used in SiC CMOS fabrication. The following chapter will further discuss the relevance of the results achieved.

Chapter 5. Conclusion

5.1 Summery

From these studies and results, much can be learned that can aid the development of the SiC CMOS. This thesis has covered the topics of photolithography, plasma etching, wet etching, and liftoff with materials such as intrinsic SiC, doped SiC, Si, and SiO_2.

With each experiment that was conducted, photolithography was performed to create the photoresist mask. Each sample was individually processed. It often required the help of other students. Photolithography was the single most time-consuming process of this study. It was also the most delicate. Any form of pollution s, such as dust particles or excess light, can affect the

outcome of the mask. Any variation in exposure intensity or contact pressure can harm the pattern transfer. Photolithography was also the most important. It was the largest factor in determining the resolution of the etch. If the mask had poor resolution, the etch was going to have a worse resolution. When dealing with minuscule feature sizes, the quality of the mask matters.

This study was able to improve the quality of the photolithography process. The exposure time was studied, and a method for calculating the photoresist based on the light intensity and thickness of the photoresist was calculated to determine how long the photoresist needs to be exposed. A new development procedure using a different development solution was used. These two methods used together were able to improve the photolithography process to create higher resolution masks. This was essential to studying the etch methods.

Although the photolithography resolution had been improved, there were still problems with the consistency between photo lithography samples. When processing many samples at a time, it is likely that not all samples can be produced with the same level of quality. The contact aligner that was used was inconsistent with the level of pressure that was applied. This caused poor contact that hurt the resolution of the masks. The lab facility was open to sunlight. This was clearly a problem when working with a photoresist that is sensitive to light. There were also many issues with working in confined places. The facility was not set up to process large numbers of small samples at a time. Instead, it was designed to process only a few larger samples at once. With the new photolithography procedure under construction and the addition of a stepper aligner, the photolithography process will surely improve. The new facility should be designed with these types of experiments in mind. It should be capable of processing many samples at once, in one singular batch. This would be a great improvement on the current

photolithography procedure, which would improve all other etching processes modules for SiC CMOS fabrication.

The ICP etching process module experiments were met with success. The selectivity between various materials has been demonstrated. Si has been shown to have a higher etch rate than all other materials. This indicates that when etching polysilicon on the surface of a SiC substrate, no matter the epitaxial doping, or if the polysilicon has been deposited on a SiO_2 layer, the polysilicon will have a high selectivity. The inverse is true for SiO_2. The SiO_2 has a low etch rate, making etching for field or gate oxide difficult. However, SiO_2 makes an ideal hardmask for etching Si. The selectivity is greater than two, making deep trench etching possible into Si substrates.

Chlorine-based ICP etching recipes were conducted with Cl_2 and BCl_3. The concentration of Cl_2 was varied to determine how the Cl_2 affects the etch rate and selectivity of doped SiC. The results from this study point to the robustness of the chlorine-based recipes. When etching with chlorine-based plasmas, the selectivity of doped SiC has a very small change. This change is significant because the selectivity can be tuned for the specific application. For example, the selectivity between p+ SiC, and n-well SiC, is less than one using the baseline recipe, but by changing to recipe 4, the selectivity is increased to greater than one. This can be useful when etching for ohmic contacts. It can reduce the likely hood of over-etching. However, the change in selectivity between the baseline and recipe #4 is small. This indicates that if the gas flow rate inside the etching chamber is changed, the selectivity will not change a large amount. Based on these results, the etch rates remain relatively constant when the chlorine concentration reaches 50% or greater.

The success of plasma etching was met with less successful buffered oxide etching. BOE has been shown to be difficult to etch when dealing with small feature sizes. Different concentrations of BOE to water solutions were attempted for a range of etch times. A uniform etch with accurate pattern transfer was not achieved for small feature sizes. Instead, the results show that large features etch faster than small features. The patterns that were transferred were not accurate. The isotropic nature of wet etching causes features to become distorted. Diluting the BOE solution further and increasing the time left no improvement to the etch uniformity. Instead, it caused more damage to the photoresist, which distorted the features even further. For these reasons, BOE has shown to have two uses in SiC CMOS fabrication: removing residual oxide that has accumulated on the surface of the material and for pattern transfer into large materials where pattern accuracy is easier to achieve. The former is true because BOE acts quickly on oxides. When no mask is in place, the oxide can be removed almost instantaneously. The latter has been shown because the large features in this mask were etched quickly. The only distortion found in the feature is from the sharp corners and the inner circle of the donut shapes. For a significantly large feature, these distortions will become less significant. Therefore, BOE etching would be suitable for oxide stripping and large pattern transfer, but not small pattern transfer.

For small pattern transfer, ICP and liftoff are recommended. ICP can transfer patterns with high accuracy and have a constant etch rate, making it more predictable. Constant and predictable etch rates allow the ability to create thin layers of SiO_2 without etching down to the substrate. This is useful for etching field oxide, which is a thin layer of oxide. Using ICP, the oxide can be made even thinner. The downside with ICP etching SiO_2 is the low etch rate of SiO_2 gives a low selectivity. Therefore, over-etching is a concern when etching a layer on top of

a substrate. Using ICP to create a hardmask is not recommended because the substrate could be etched. When factoring in the CD of the oxide, it will have a larger CD shift. For using SiO_2 as a hardmask for polysilicon, liftoff is recommended. A high pattern transfer can be achieved with uniformity across the sample. The SiO_2 can be removed down to the surface of the substrate without the possibility of etching into the substrate. This is an improvement to the hardmask etching procedure. However, liftoff has some drawbacks. When performing liftoff, the design of the mask becomes inverted. Regions that would normally be etched on now have an added layer up. Solutions to this would be to design the mask with this in mind. If this is not possible, using a positive photoresist would work, but that would require a new photolithography procedure with a new photoresist.

The results and data collected in this study that has been described here can lead to many improvements in the fabrication of a SiC CMOS device. This work is meant to be the groundwork for future students to build upon. There are still many directions this research could go. As new facilities are built, and opportunities grow, much more stands to be studied about these etching methods.

5.2 Conclusion and Future Outlook

This thesis has covered a range of different etching methods. The topics described and studied in this thesis include the mechanisms behind how light reacts to photoresists and how masks are developed. Data has been collected, and the process has been improved by changing the photolithography procedure. The design of inductively coupled plasma reactive ion etchers has been described, along with the physics behind how an anisotropic etch is produced using plasma. The selectivity of various materials that are used in SiC CMOShase was shown and

described, then the etching recipe was changed, and the chlorine concentration was varied for doped SiC. BOE was attempted with SiO_2. After undesirable results were found, different procedures were attempted to try and improve the process. While the intended results were not found using ICP, it was determined that other methods would be more reliable for etching SiO_2. SiO_2 field oxide can be more easily etched using ICP. This method gives more compatibility with different feature sizes. For SiO_2 hardmask development, lift-off can produce more reliable results. This thesis studied and improved the etching process modules for developing SiC CMOS devices, but there are still many questions left to be answered.

Future works for these studies are superfluous. Photolithography can be greatly improved by using a more advanced aligner. This can increase the resolution and be more consistent. New photoresists can be attempted, each with its own lithography recipe. This would require developing a new photolithography recipe specific to the new facility and materials.

ICP etching has an infinite number of parameters that could be tested. Each test could make an interesting study. Some possible studies would be to add new materials to the baseline etch study. Aluminum, platinum, or other metals in IC fabrication would make interesting additions. These could be compared to the selectivity data that has been described to find new selectivity values that should be used when designing an IC process flow. All of these materials could be used with different chlorine-based ICP recipes. Other recipes could also be developed. The ICP facility has gas lines for NF_3 as well. A similar study to this could be conducted using Florine-based gas. This would give interesting results with the etch rates and selectivity, but also data on the etch profile should be collected. Chlorine and fluorine are known to have differing chemistries in plasma etches (Ekström, 2019). Deep trench etches must also be studied. The etch profiles created in this study have all been shallow. Data on aspect ratios have been ignored for

this study because shallow etches do not have large variations in aspect ratios. Developing an etch recipe that is used for deep etches with high aspect ratios could be an interesting and meaningful study. ICP etchers have more parameters than just gas configuration. There are many other parameters that this study failed to explore. Parameters such as chamber pressure, electrode RF power, inductor RF power, temperature, total gas flow rate, and DC voltage all have a large effect on the characteristic of the etch profile. This study was unable to explore these topics, but future studies most definitely should.

BOE process modules are far from complete. Future studies should be conducted to determine how higher accuracy of pattern transfer can be achieved, especially with smaller features. ICP and Liftoff methods that have been described are not always applicable to the CMOS process. BOE will need to be utilized. Experiments for BOE should be conducted at high temperatures. This has been suggested in the literature by (Burham, Sugandi, Nor, & Majlis, 2016). This study suggests a solution to the problem described in chapter 4.3. The BOE solution that was used was a 5:1 (ammonium fluoride to hydrofluoric acid) mixture. Using stronger or weaker concentrations would yield different results. This is an interesting study that should take place in the future.

These studies were conducted in the early stages of SiC CMOS development at the University of Arkansas. In the upcoming years, great improvements will be made both in facilities and process development. This thesis hopes to be useful resource in future development. The groundwork that this thesis provides intends to help future researchers achieve their academic goals for years to come.

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Appendix A Description of Research for Popular Publication

No publications resulted from this work.

Appendix B Executive Summary of Newly Created Intellectual Property

No intellectual property resulted from this research.

Appendix C Potential Patent and Commercialization Aspects of Listed Intellectual Property Items

No Patents resulted from this research.

Appendix D Broader Impact of Research

D.1 Applicability of Research Methods to Other Problems

The characterization methods described in this thesis can be applied to any etching method. The five characterization parameters are useful for understanding the quality of the etch. They can be applied to other ICP gas chemistries, as well as wet etching methods. It can be useful for IC fabrication or MEMS fabrication. The method used to measure the etch rate and selectivity was a profilometer. This was a useful method for measuring etch depth that was faster than using AFM. This method can be trusted so long as the profilometer is properly calibrated. The method for using CD was pixel counting from high resolution images. This was somewhat useful. Using a CD-SEM would be more accurate; however it would also take more time. The method for measuring the profile angle was not trustworthy. The ideal method for measuring this angle is to use FIB and take SEM images at a 90° angle to then measure the profile angle.

D.2 Impact of Research Results on U.S. and Global Society

This research was conducted in order to further develop a SiC CMOS device. These devices are used in extreme environments where other, more commonly used, semiconductors fail. SiC CMOS devices can be used in rocket ships and satellites to be sent to deep space. They can also be used on earth when a high voltage requirement needed, or extreme temperatures are reached.

D.3 Impact of Research Results on the Environment

SiC CMOS devices can be used in outer space to further study our solar system. They can also be used in eco-friendly power plants to help produce sustainable energy that can be beneficial to the environment. There are, however, negative impacts on the environment when fabricating these devices. The gas used in ICP etching is toxic and harmful to the environment. After the chamber is evacuated from the gas, it is then pumped into a scrubber, then the atmosphere. The scrubber is used to clean the gas of harmful pollutants but does not eliminate all pollutants. There are also harmful chemicals used when wet etching. All proper disposal procedures were followed during the etching process.

Appendix E Microsoft Project for MS Material Science Degree Plan

Class (37 hrs)	**Mon 1/13/20**	**Thu 5/5/22**	**96%**
Spring 2020 (7 hrs)	**Mon 1/13/20**	**Thu 5/7/20**	**100%**
MEPH 5383 (3) Commercialization of Research	Mon 1/13/20	Thu 5/7/20	100%
CHEM 5243 (3) Electrochemical Methods	Mon 1/13/20	Thu 5/7/20	100%
MEPH 5911 (1) Personnel Management	Mon 1/13/20	Thu 5/7/20	100%
Summer 2020 (3 hrs)	**Mon 5/25/20**	**Thu 7/30/20**	**100%**
ELEG 600V (2) Master' Thesis	Mon 5/25/20	Thu 7/30/20	100%
MSEN 5821 (1) Engineering and Science Ethics	Mon 5/25/20	Thu 7/30/20	100%
Fall 2020 (7 hrs)	**Mon 8/24/20**	**Thu 12/17/20**	**100%**
MSEN 5313 (3) Fundamentals of Materials Science	Mon 8/24/20	Thu 12/17/20	100%
ELEG 5303 (3) Semiconductor Device	Mon 8/24/20	Thu 12/17/20	100%
MSEN 6811 (1) Management and Leadership	Mon 8/24/20	Thu 12/17/20	100%
Spring 2021 (7 hrs)	**Mon 1/11/21**	**Thu 5/6/21**	**100%**
MEEG 5343 (3) Computational Materials Science	Mon 1/11/21	Thu 5/6/21	100%
MSEN 5733L (3) Fabrication at the Nanoscale	Mon 1/11/21	Thu 5/6/21	100%
MSEN 6911 (1) Adv. Management and Leadership	Mon 1/11/21	Thu 5/6/21	100%
Summer 2021 (0 hrs)	**Mon 5/24/21**	**Thu 7/29/21**	**100%**
Internship	Mon 5/24/21	Thu 7/29/21	100%
Fall 2021 (6 hrs)	**Mon 8/23/21**	**Thu 12/16/21**	**100%**
ELEG 5393 (3) Electronic Materials	Mon 8/23/21	Thu 12/16/21	100%
MEEG 5353 (3) Li-Ion Batteries	Mon 8/23/21	Thu 12/16/21	100%
Spring 2022 (7 hrs)	**Mon 1/10/22**	**Thu 5/5/22**	**80%**
MSEN 5322 (2) Materials Characterization	**Mon 1/10/22**	**Thu 5/5/22**	80%
MSEN 5713 (3) ADV Nanomaterials Chem	**Mon 1/10/22**	**Thu 5/5/22**	80%
MSEN 600V (2) Master's Thesis	**Mon 1/10/22**	**Thu 5/5/22**	80%

Task	Start	Finish	% Complete
Background Information	**Mon 5/25/20**	**Thu 12/31/20**	**100%**
Read KTH dissertaion	Mon 5/25/20	Thu 7/30/20	100%
Read papers on plasma etching	Mon 5/25/20	Thu 12/31/20	100%
Begin experiments	**Mon 8/24/20**	**Fri 1/1/21**	**100%**
Photolithography Training	Mon 8/24/20	Sat 10/31/20	100%
Photolirhography Development	Mon 8/24/20	Sat 10/31/20	100%
BOE Training	Mon 8/24/20	Sat 10/31/20	100%
ICP Training	Mon 11/2/20	Fri 1/1/21	100%
Process modules Development	**Mon 1/11/21**	**Fri 5/6/22**	**98%**
ICP Characterization Study	Mon 1/11/21	Mon 1/10/22	100%
BOE Study	Mon 1/11/21	Thu 5/6/21	100%
Thesis writing	Tue 8/24/21	Mon 2/28/22	100%
ICP Gas Composition Study	Mon 11/1/21	Mon 1/31/22	100%
End Game	**Mon 11/1/21**	**Fri 5/6/22**	**96%**
Final Draft	**Mon 11/1/21**	**Fri 4/1/22**	**100%**
Finish writing	Mon 11/1/21	Thu 3/31/22	100%
Approval by professor	Wed 3/2/22	Wed 3/30/22	100%
Approval by MSEN Director	Wed 3/2/22	Wed 3/30/22	100%
Send to committee	Wed 3/2/22	Wed 3/30/22	100%
Final draft finished	Fri 4/1/22	Fri 4/1/22	100%
Submit abstract	Mon 1/10/22	Thu 3/31/22	100%
Announce presentation and defense	Mon 1/10/22	Thu 3/31/22	100%
Apply for graduation	Mon 1/10/22	Tue 3/1/22	100%
Public Presentation	Mon 4/4/22	Mon 4/4/22	100%
Defense	Mon 4/18/22	Mon 4/18/22	0%
Deliver to grad school	Mon 4/18/22	Fri 5/6/22	0%
Dead Day	Fri 5/6/22	Fri 5/6/22	0%

Appendix F Identification of All Software used In Research and Thesis Generation

Software #1
Name: AutoCAD 2020
Purchased by: University of Arkansas

Software #2
Name: Adobe Acrobat Reader DC

Software #3
Name: Microsoft Office
Purchased by: University of Arkansas

Software #4
Name: Fiji ImageJ

Appendix G All Publications Published, Submitted, and Planned

A significant portion of chapter 1, chapter 3, and chapter 4 will be used in a future publication titled "ICP Etching of Intrinsic and Doped SiC With Chlorine-Based Gas Composition.".

Appendix H Photolithography Traveler

Fab Lot #

Print Name:

Start Date:

Due Date:

Mask Set:

Purpose:

Lot#: Photolithography

Device #	Lot #	Description

Sample Pre-clean (Start)				
Date/ Time	1.1	Solvent Clean ☐ Sonicator	☐ Acetone sonication for 5 minutes ☐ Rinse with clean Acetone ☐ Methanol sonication for 5 minutes ☐ Rinse with clean Methanol ☐ IPA sonication for 5 minutes ☐ Rinse with clean IPA ☐ N2 Dry /Dehydration bake, 100 °C for 2 minutes ☐ Rinse with Di water ☐ Remover PG @ 80C for 5min if necessary	

Lithography (Start)				
Date/ Time	4.1	Solvent clean (if not continuous process)	☐ DI water ☐ 5 min dehydration on hotplate at 110° C	
	4.2	Photolithograph y Negative PR ☐ HMDS ☐ Spinner check ☐ Spinner	Recipe 4; 4000 rpm ☐ Apply HMDS ☐ Blue tape Recipe 3, 3000 rpm for 50 seconds ☐ AZ® nLoF 2035 (target ~ 3.5 um) ☐ 2.5-inch chuck w/ skirt ☐ Blue tape 110°C / 60 sec ☐ Check accuracy with thermocouple	

		☐ Hot plate (Soft bake)	☐ Beads removal at the edges (PUT DESIRED MASH HERE)	
		☐ MJB-3	☐ Mask orientation ☐ Use same corner as previous one for consistency ☐ Determine exposure time ☐ Mask cleaning PRS1000 / Acetone & IPA	
		☐ Device #	PR Thickness: ___________um (Profilometer) Energy: ____80_______mJ/cm2 (Tk*27) Intensity: ___________mW/cm2 (From log) Exposure Time: ___17.7_______s (Energy/Intensity)	
		☐ Device #	PR Thickness: ___________um (Profilometer) Energy: _____80______mJ/cm2 (Tk*27) Intensity: ___________mW/cm2 (From log) Exposure Time: ___17.7_______s (Energy/Intensity)	
		☐ Device #	PR Thickness: ___________um (Profilometer) Energy: _____80______mJ/cm2 (Tk*27) Intensity: ___________mW/cm2 (From log) Exposure Time: ____17.7______s (Energy/Intensity)	
			110 °C / 60 sec *Check accuracy with thermocouple*	

		☐ Hot plate (PEB) ☐ Base hood ☐ Inspection Microscope	☐ Develop AZ726 MIF (around 30 seconds) ☐ Rinse in DI water ☐ N2 Blow dry Develop time / Comments Device #: __35 sec_____ Device #: ____________ Device #: ____________ ☐ Smallest Feature O.K.?	

Completed by:
Finish date:
Finish Time:

Appendix I ICP Procedure

ICP Etch - Standard Operating Procedure

Standby setup

Scrubber and all pumps are off

PECVD - ICP chambers are under soft vacuum from previous usage

All gas lines are off at cylinders

CFT-150 (ICP and ebm) chiller is on with set temperature at 20°C and recirculating pressure in range of (65-80) psi. 80 psi is max.

System turn on

Open GN2 dewar valve and valve on the wall

Check and if not, open supply and return valve on the CFT-150 chiller to ICP

Rotate the scrubber panel knob CW to turn on. Press F1 button so water starts filling the reservoir. Once the water is above the mark, press F2 to turn on the sprinklers (Valve V2 should be close and valve V1 should be open 3 turns)

Check and if not, turn on the main power breaker for ICP on the wall behind heat exchangers

Open (two) GN2 and C&D air valves over the ICP (total three valves)

In plasmatherm power module, turn on (green - on, red - off, and note that lights don't work)

Machine power, wait 1 min

Primary mech pump, wait 1 min

Lock pump, wait 1 min

Docking mech pump (PECVD)

Open Cl_2 and BCl_3 gas cylinders. Flow regulators should not need adjustment

ICP and PECVD heat exchangers will be powered ON, press start button, and set them to remote.

Enable on docking blower in power module, and turn on the heater module located below turbo panel

Open the program on computer (login credentials are 4444 and 4444). *Note: 'gas suspected in chamber' warning is normal while pump down. Press hold to reset*

Note: 'No gas flow for 10 mins, N2 gas flow starts' notification can be ignored

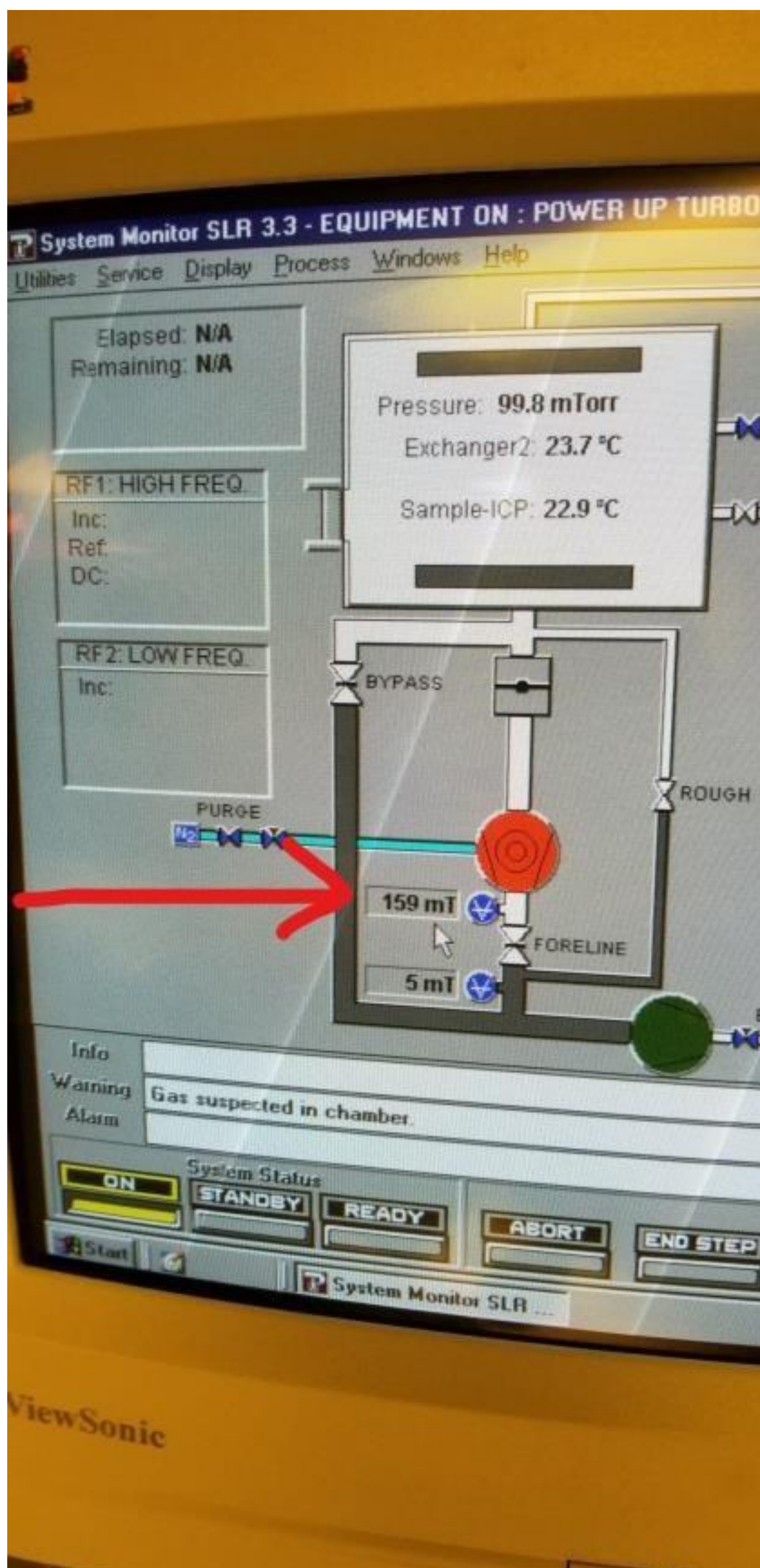
1 - Image illustrates the Cl2 and BCl3 gas lines near cylinders. CW turns to close the cylinder.

First pump down

Press ON, and wait till 'equipment ON parameters applied' info comment to disappear

Turn on turbo pump by ***Utilities>>turbo pump on****. (There is a communication problem with software and sensors, this step doesn't remotely turn on turbo)*

Wait for 500 mT pressure at turbo foreline in chamber diagram. *(Might get an info notification but still wait for it to reach 500 mT)*


System Monitor SLR 3.3 - EQUIPMENT ON : POWER UP TURBO
Utilities Service Display Process Windows Help
Elapsed: N/A
Remaining: N/A
Pressure: 99.8 mTorr
Exchanger2: 23.7 °C
Sample-ICP: 22.9 °C
RF1: HIGH FREQ.
Inc:
Ref:
DC:
RF2: LOW FREQ.
Inc:
BYPASS
ROUGH
PURGE
159 mT
FORELINE
5 mT
Info
Warning
Alarm
Gas suspected in chamber.
System Status
ON
STANDBY
READY
ABORT
END STEP
Start
System Monitor SLR ...
ViewSonic

Press start to turn on the turbo manually. To override software, hit ***display>>SDU>>click the turbo on check button>>hit the red button next to it>>exit***

Wait for turbo speed light to ramp up, and then power setting to ramp down. *(Single LED signifies turbo speed status, while all LEDs signifies the power status. When turbo is started, it increases the speed to maximum, and then decreases the power usage attaining optimal high speed - low power setting)*

When turbo is ready to use, hit ***display>>SDU>>check the turbo ready>> hit the red button next to it>>exit***

Press ***standby.*** Wait till standby parameters applied notification to disappear

Service>>maintenance> pump>>system turbo. If the pressure is around 1 mT, turn on ion gauge by ***utilities>>ion gauge on.*** Wait approx. 5-6 mins to reach 1e-6 Torr, and close the ion gauge by ***utilities>>ion gauge off***

Utilities>>select active chamber>>left chamber to switch active chamber to left PECVD chamber

Service>>maintenance> pump>>chamber (Lo Vac). PECVD chamber has normal manometer (overview diagram might be red and say vacuum), so wait for 3mins after pressure settles at 4 mT. Wait for the complete notification

validate gas and plasma

• Make sure software operates in right chamber, and hit ***Service>>manual>>*** Select the following settings to test N2 plasma

Exchanger2	35°C	Cl2	0	Time	1:00
Sample ICP	40°C	BCl3	0		

Chamber (mT) 10 N2 10 RF1 power 50

NF3 0 RF2 power 400

Press **Gas ON** (*this opens mass flow controllers to set flow*)(check N2 level (actual) should be closer to the set value). Wait till values settle at setpoints

Press **pressure ON** (*this regulates throttle valve to maintain chamber pressure at setpoint*). Wait till values settle at setpoints

Press **RF**, and notice the purple-ish nitrogen plasma glow thru windows in right chamber. While plasma is ON, check the water line in water flowmeter at the back, It should read 0.5 gpm

When plasma is finished, press **ALL OFF** and **EXIT**

First vent

Press stop manually to turn off the turbo. Turbo spins freely under no power throughout following procedure

Utilities>>close gate>> system. Wait for 'system gates closed' notification

Confirm the software is operating in the right chamber, then hit ***service>>maintenance>> vent>>system.*** Hit ***windows>>overview diagram***, loadlock and right chamber turns red and notifies atmosphere pressure level

Use both switches simultaneously to lift the chamber lid to its highest position. Place the samples on insulating sapphire carrier wafer. Use new gloves to place the carrier wafer at the center of chamber carefully. Lower the lid with both switches again simultaneously until no more squeaky sound

Second pump down (from atmosphere)

Service>>maintenance>>pump>>system (big vibrations and sounds are nominal) Note: Hold the loadlock lid down manually by hand. Wait for the notification 'system pumpdown complete'

Press **start** on turbo pump (wait for the LEDs to rise and fall) (Software assumes turbo is on during the whole vent event)

After turbo reaches full speed - low power setting, click ***utilities>>Ion gauge on***. Wait 10 mins after reaching the pressure 5x10^-7 torr. Turn ***off*** the ion gauge to go next step

Clean the chamber with 4 cycles of manual N2 purge without plasma by clicking ***service>>manual mode>>purge*** (1 min N2 flow, and 1 min pump down. Repeat four times). Then hit ***ALL OFF>>exit***

Process

Service>>manual>> set the recipe for etch

Exchanger2 temp 35°C Cl2 13 Time mm:ss

Sample-ICP temp 40°C BCl3 25

Chamber pressure 10 mT N2 00 RF1 power 300 W

NF3 00 RF2 power 1000 W

Press **gas ON** (this opens the mass flow controllers to set flow). Wait till the set points are reached

Press **pressure ON** (this maintains the chamber pressure setpoint by regulating throttle valve)

Note: reading in yellow background implies reading is beyond the tolerance to setpoint

press **RF ON** and notice the plasma glow through window. Log the DCV value in log book

When plasma is finished, press **ALL OFF and purge** the chamber for 3 mins to flush out harmful gases out of chamber. Press **ALL OFF>> exit**

Second Vent

Repeat first vent procedure

Third pump down

Repeat second pump down procedure

Shut down

Press **ON**. Wait for the system ON parameters applied notification to disappear

Utilities>>turbo pump off. Turn off manually by pressing stop button and uncheck turbo is on and turbo ready by entering ***SDU>>turbo ready uncheck***

Turn off docking blower

Turn off plasmatherm controls in the reverse order of start up with 1 min interval

Turn off software and shutdown windows

Docking mech pump, wait for 1 min

Lock pump, wait for 1 min

Primary mech pump, wait for 1 min

Machine power

Turn off six zone heater module below turbo panel

Turn off scrubber by pressing F2>>F1, and red knob to OFF

Close the two N2 valves, air valve, and other gases

Don't forget to turn off N2 dewar