

ELECTRO-THERMAL MODEL FOR LOCK-IN INFRARED IMAGING OF DEFECTS IN PEROVSKITE SOLAR CELLS

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ABSTRACT: The production of uniform layers without defects is crucial for the efficient upscaling of perovskite solar cells. To understand the origin of defects and their impact on efficiency, we compare steady-state (DC) and alternating current (AC) measurements with simulation results obtained by an electro-thermal 2D+1D finite element method (FEM) implemented in the software Laoss. The software supports the upscaling process from small- to large-area devices by solving for the potential and temperature distribution in 2D top and bottom electrode domains, which are coupled by a vertical 1D coupling law. Recently, we extended this FEM model to the frequency domain in order to study both DC and AC characteristics of solar cells. Here, we report on the extension of this frequency-dependent FEM model to the thermal domain, allowing us to calculate amplitude and phase images of solar cells that are voltage-modulated in the dark. We measured and modelled a screen-printed carbon-based hole-transporter-free perovskite solar cell with a defect, appearing as a hotspot in temperature measurements. In contrast to the traditional DLIT method using a large voltage modulation, we introduce a small-signal DLIT (SS-DLIT) imaging method which our model is capable to reproduce. Fitting thermal AC simulations to measured data, allowed to quantify the defect and examine its behaviour and origin.

Keywords: Perovskite, Simulation, Modelling, Experimental Methods, Defects

1 INTRODUCTION

Thin film solar cells such as single-junction perovskite and monolithic perovskite/silicon tandem photovoltaic cells have attracted researchers' attention across the globe in recent years due to rapidly increasing efficiencies. On laboratory scale, single-junction perovskite solar cells (PSCs) currently achieve a power conversion efficiency (PCE) of 25.7 %, while perovskite/silicon tandem cells reached a certified PCE of 31.3 % [1]. Most PSCs use an organic hole transport layer (often spiro-OMeTAD) to facilitate the transport of holes from the perovskite layer to the counter electrode [2]. However, organic hole transport materials (HTM) have been reported to inhibit long-term stability [3]–[5]. In 2012, Etgar et al. [6] presented the first hole transporter-free perovskite solar cell using the methylammonium lead iodide (MAPbI₃) perovskite layer as a photon absorber and hole transporter simultaneously. This type of perovskite solar cell is associated with high stability as recently reported by Mei et al. [7].

When upscaling PSCs, a loss in efficiency is to be expected, since with larger areas, the series resistance increases due to the sheet resistance of the electrodes and the need for current collecting metal grids leads to shadow losses. Furthermore, the probability of defect-occurrence due to the inhomogeneity of the films [8]–[10] increases as well. Jaysankar et al. [11] shows in a recent study that the inhomogeneity of the deposited layers is a key loss factor when scaling up perovskite solar cells.

In this study, we use a commercial software tool called Laoss [12]–[17] developed in-house to better understand and quantify the effects of inhomogeneities and non-ideal electrodes in semiconductor devices through simulations and direct comparison with measurements. Laoss contains a FEM solver that solves Ohm's law for charge transport and Fourier's law for heat transport on 2D top and bottom electrodes. The 2D electrodes are connected by a 1D coupling law for vertical current and heat transport,

neglecting oblique flows of current due to the large aspect ratio of the cell cross-section. This 1D coupling law represents a quasi-ideal device that is not influenced by lateral effects like the sheet resistance and leads to a 2D+1D approach which saves computation time compared to a full 3D simulation.

The software tool has recently been extended by an electrical [15] and thermal small-signal mode to study the influence of defects and non-ideal electrodes in the frequency domain. It calculates and displays potential, source current, and temperature distributions, which for instance help to analyse defect types, predict the performance of an upscaled device or optimise metal grids of semiconductor surfaces, as recently shown by Burwell et al. on an organic solar cell [16].

Since the simulation tool includes heat generation and transport in a semiconductor device caused by a small-signal voltage variation around a certain bias/DC voltage, we have therefore developed a dark lock-in thermography (DLIT) measurement setup with an infrared (IR) camera. In our presented case, a DC voltage is applied to the device and a small rectangular voltage signal with a chosen lock-in frequency is superimposed. A similar method called MPP-SLIT was presented by Sieglöcher et al. in 2014 [18], where a small-signal voltage modulation was applied around the bias of an illuminated cell's MPP. In the following, we refer to this simulation and measurement method as small-signal dark lock-in thermography (SS-DLIT) as this approach differs from the widely used and established DLIT method in which a voltage variation oscillating with a larger amplitude at the lock-in frequency is applied at zero offset voltage [19], [20].

Here, we present Laoss' thermal AC mode and compare SS-DLIT measurements of a screen-printed carbon-based hole transporter-free PSC at different bias voltages with the corresponding electro-thermal SS-DLIT simulations.

The device has revealed a hotspot which we model and quantify with our software by manually fitting the

simulation to SS-DLIT data. In addition, we analyse an electro-luminescence (EL) image of the screen-printed cell qualitatively to draw further conclusions about the analysed defect and other fabrication related artefacts.

2 METHODS

2.1 Device Fabrication

The HTM-free perovskite solar cell was deposited in an n-i-p configuration onto a 400 nm fluorine-doped tin oxide (FTO) coated 2 mm thin glass substrate. A compact 50 nm titanium dioxide layer (cTiO₂) was applied by spray pyrolysis to the FTO-coated glass plate. Mesoporous titanium dioxide (mTiO₂, 500 nm), mesoporous zirconium dioxide (mZrO₂, 1000 nm) and the 10-12 μm carbon layer were screen-printed and the MAPbI₃ precursor was inkjet infiltrated through the carbon top layer and then crystallized at ambient temperature. It is assumed that most of the porous layer stack is filled with perovskite crystals.

In this cell structure, the cTiO₂ functions as a hole blocking and electron transport layer (ETL) and the mTiO₂ and mZrO₂ layers act as a scaffold for the perovskite. The mZrO₂ also serves as a spacer layer between the TiO₂ anode and the carbon cathode (hole collector and electrode at the same time).

The cell was produced by the Swiss Federal Laboratories for Materials Science and Technology (Empa) and the Swiss company Solaronix SA. For this study, we selected a particular cell that appeared to have a hotspot in IR measurements. A schematic cross-section including the defect and an image of the device with an active area of 1.44 cm² is shown in Figure 1.

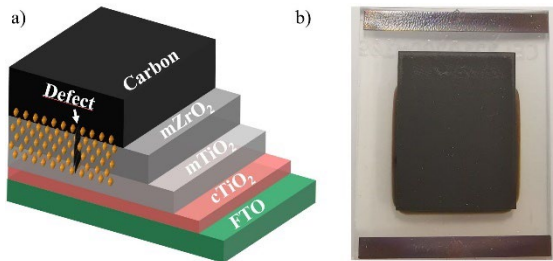


Figure 1: Cross-section of the HTM-free perovskite solar cell with an included pinhole defect (a) and an image of the device facing the carbon top electrode (b).

2.2 Experimental Characterization

For the current-voltage characteristic, the all-in-one measurement platform Paios 4.3.1 [21] from Fluxim AG was used. The cells were measured with 320 sequential steps with 0.2 s measuring time and 1.2 s settling time at each step to reduce hysteresis [22]. The device was measured in the dark with a voltage range from -0.2 to 1.5V in forward direction, resulting in a slow scanning rate of 3.8 mV/s.

The electro-luminescence image presented here, was taken in a dark-chamber, equipped with a Nikon D800 digital camera with a removed infrared radiation filter and an installed longpass filter, blocking visible light. The image was taken after a DC potential of 1.2V was applied to the PSC for approximately 150 s, within which a steady-state current has been reached.

In a DLIT measurement of solar cells, a periodically

pulsed voltage signal, with a specific frequency $f_{lock-in}$ is applied to a device to generate a periodic temperature signal induced by Joule heating [19]. With the LIT method, local heat sources can be better investigated compared to steady-state IR images, due to an increased spatial resolution by several orders of magnitude.

The time-dependent thermal images acquired by the IR camera are demodulated according to the synchronous two-channel correlation with two sets of weighting factors, which approximate a sine and a cosine function. This algorithm allows to compute the amplitude A and the phase Φ of the temperature signal from the "in-phase" S^{0° and the "in quadrature" S^{-90° components. For this study, we have solely examined the temperature amplitude image, which shows the dissipated power and is calculated as

$$A = \sqrt{(S^{0^\circ})^2 + (S^{-90^\circ})^2}. \quad (1)$$

In this study, we investigate thin-film solar cells with a small-signal dark lock-in thermography measurement. The most pronounced difference between DLIT and our SS-DLIT method is the applied voltage oscillation. To compare our thermal AC simulations with measurements, we had to apply a small harmonic voltage signal around a DC bias of a device (s. Figure 2). Using the lock-in algorithm with IR images, it is possible to analyse the temperature increase caused by the small-signal.

To acquire the IR images, we used a PI450i camera (Optris GmbH, Germany) with an image resolution of 382 x 288 pixels and a frame rate of 80 Hz. We use a lock-in frequency $f_{lock-in}$ of 1 Hz resulting in a thermal diffusion length of approximately 1 mm for the carbon electrode. IR images could not be taken through the glass substrate, so they were acquired with the camera facing the carbon electrode. We assume that this will not distort the measured temperature, since the cells are extremely thin compared to their lateral dimension. During the SS-DLIT measurement a DC voltage signal of 0.9, 1.1, 1.3 and 1.6 V and a modulation amplitude of 0.1 V was applied.

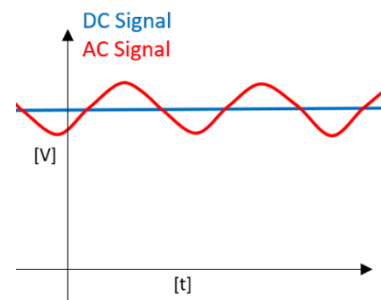


Figure 2: Schematic representation of the superimposed sinusoidal voltage signal applied to the device for the SS-DLIT measurements.

2.3 Modelling

In a large-area semiconductor device, charge carriers travel laterally across the top and bottom electrodes to the charge collecting contacts. The potential distribution on the electrodes can be influenced by various types of defects and ohmic losses due to the sheet resistance R_{sh} , which is a significant part of the resulting series resistance R_s in current-voltage characteristics [23]. The software Laoss accounts for these losses by solving Ohm's law on

the 2D electrodes with the finite element method. In the steady-state (DC, direct current) case, the electrodes are coupled by a 1D current-voltage law (e.g. diode model) [13] and in the time-dependent small-signal (AC) case, the coupling requires an additional frequency and bias voltage φ_{DC} dependent admittance $Y(\omega, \varphi_{DC})$ with the angular frequency $\omega = 2\pi f$. The coupling law represents a quasi-ideal device, which is not influenced by surface effects or defects (e.g. shunts). This 2D+1D concept is illustrated in Figure 3 with the 1D coupling laws symbolized by diodes for the DC case and additional RC elements for the AC case.

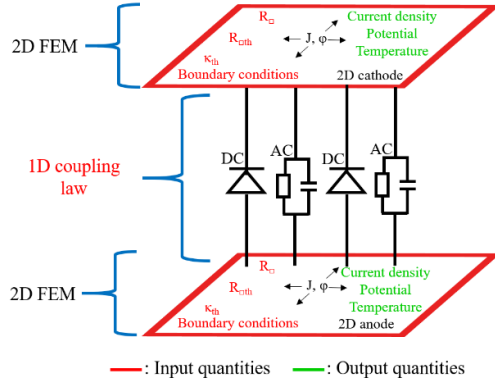


Figure 3: Structure of the electro-thermal model of the Laoss software with the coupled 2D domains and 1D coupling laws (DC and AC).

In this study, we intend to simulate the temperature distribution on a solar cell, caused by a sinusoidal small-signal. We restrict ourselves to the unidirectional electro-thermal coupling thereby assuming that the simulated temperature solely depends on electrical device characteristics and not vice versa.

To solve the thermal AC equations, Laoss requires steady-state temperature and voltage distribution results for the small-signal linearisation. The fundamental heat conservation law for the calculation of the temperature distribution on the top and bottom electrodes in steady-state is described as

$$-\nabla \cdot \left(\frac{1}{R_{th}} \nabla T \right) = P_{joule}^{electrode} + P_{joule}^{stack} - P_{ex}^{envir} \quad (2)$$

and is further explained in [14]. Equation (2) is solved for the temperature distribution T on the electrodes which depends on current-induced Joule heating in the electrodes $P_{joule}^{electrode}$, Joule heating in the stack P_{joule}^{stack} caused by vertically flowing currents, which includes also heat conduction between the electrodes, and convective, conductive and radiative heat exchange with the environment P_{ex}^{envir} . The simulated temperature is also influenced by the thermal sheet resistance R_{th} describing the heat conductivity of the top and bottom electrode materials.

The electro-thermal AC model is based on the three-dimensional diffusion equation for transient heat conduction in solids with the source term q_{source} including Joule heating, the specific heat capacity c_p , the density of the electrode ρ and the thermal conductivity λ and can be written as

$$\rho c_p \frac{\partial T}{\partial t} + \nabla \cdot (-\lambda \nabla T) = q_{source}. \quad (3)$$

A Fourier transform has been applied to obtain the model in frequency domain. Subsequently, a linearisation of the non-linear Joule heating terms around the DC potential and a reduction of the equations from 3D to 2D electrodes was carried out. The resulting equations for the 2D top and bottom electrodes can then be solved for the desired local AC temperature.

The Laoss simulations are based on a 2D top and bottom geometry which also considers the silver, FTO and carbon layers (transition layers) as subdomains, connecting the active area (s. Figure 1b). An active area of 1.44 cm^2 was assumed and a $4e-4 \text{ cm}^2$ rectangular subdomain was added to quantify the defect. Electrical steady-state simulations require sheet resistance values assigned to the individual materials in addition to the 1D coupling law. A vertical 1D coupling law represents an ideal cell and is in the best case a small-area device without any edge effects and low series resistance. In our case, we did not have a small-area device available, so we had to acquire the coupling law from the device itself. To obtain the DC coupling law for the active area, we therefore measured its current-voltage characteristic in the dark and subsequently fitted it with single-diode model parameters. However, this fitted curve was afflicted with a series resistance caused by the transition layers and the top and bottom electrodes of the large-area device. This series resistance has been removed for the 1D coupling law by setting the single-diode model parameter R_s to zero. Laoss later compensates for the series resistance with the electrode's sheet resistances.

To model the defect, we initially decided to use an ohmic coupling law, which is a typical approach when modelling defects [24]. In our case, however, the measured dark current-voltage characteristic of the PSC did not show an increased current at low potentials and therefore had a sufficiently high parallel resistance. Consequently, we modelled the defect with a diode-like behaviour, which is an often used modelling approach for pinhole defects in thin film solar cells [25], [26].

For the AC coupling law $Y(\omega, \varphi_{DC})$ we used the admittance of a parallel RC circuit consisting of a frequency independent conductance $G(\varphi_{DC})$ and a bias voltage independent susceptance $B(\omega)$. The conductance per area is calculated from the provided DC coupling law $f(\varphi_{DC})$, which is a voltage dependent current density:

$$G(\varphi_{DC}) = \frac{\partial f(\varphi_{DC})}{\partial \varphi_{DC}}. \quad (4)$$

The susceptance per area depends on the relative stack permittivity ϵ_r , the frequency and the stack thickness d and is calculated as

$$B(\omega) = \frac{\omega \cdot \epsilon_r \cdot \epsilon_0}{d} \quad (5)$$

This results in the following expression describing the stack admittance:

$$Y(\omega, \varphi_{DC}) = G(\varphi_{DC}) + iB(\omega). \quad (6)$$

For thermal steady-state simulations, the thermal sheet resistance R_{th} for the top and bottom electrodes must be calculated from the thermal conductivity of the electrode materials. Additionally, the thermal conductivity of the stack and the heat transfer coefficient of the individual subdomains have to be provided. Thermal AC simulations

require an additional heat capacity per unit area K_{th} , which can be calculated from the electrode materials as well. The lock-in frequency of the applied voltage signal is 1 Hz for the SS-DLIT simulations, which is consistent with the applied frequency during the measurements.

3 RESULTS

To reproduce the behaviour of the cell with electrical steady-state and thermal AC simulations, we first assigned a resistive behaviour to the defect. However, this led to substantial deviations to the measurements in both the steady-state and the thermal AC simulations. Using a diode model as the coupling law of the defect, we were able to fit the steady-state and thermal AC measurements well.

It is likely that the solar cell has a defect with a semiconductor junction as the analysed sample has been manufactured in ambient air. Consequently, dust particles could cause a clog in the screen-printing mesh, which could lead to pinholes in the layer stack. Pinholes can result in a connection between HTL and ETL and enhance local recombination currents [25]. In our case, a gap in the $mZrO_2$ layer would lead to a connection between the carbon and the $mTiO_2$ layer. Since the finished mesoporous stack is then filled with perovskite precursor, a semiconductor junction with increased recombination currents can form in the pinhole region.

Non-ohmic shunt currents are known to reduce the efficiency of solar cells by increasing the charge carrier recombination and thus increasing the dark saturation current J_0 , leading to a shift of the current-voltage characteristic towards lower voltages and consequently also to a lower open-circuit voltage (V_{oc}) in the illuminated case [24], [27]. To reproduce the SS-DLIT and current-voltage measurements and fit the defect coupling law with Laoss, we took the same single-diode model parameters that we used for the active area coupling law but increased J_0 as a fitting parameter.

Solving the small-signal equations requires steady-state results for the linearisation around the bias potential. Since the current induced Joule heating is crucial for the simulated and measured heating in the cell, we fit the electrical current-voltage simulations to the measurement first. Steady-state simulations also provide the local potential distribution, which is exponentially related [28] to electro-luminescence (EL) images owing to the diode nature of the solar cell. This allows for an additional comparison of the measured EL-image with the simulations and also provides information about the accuracy of the device model. The comparison between the measured EL image and the simulations is further explained in the end of this section.

The measured current-voltage characteristic of the investigated device was manually fitted by adjusting the sheet resistance values of the individual electrode materials. The fitted R_{sh} values, which lead to the current-voltage characteristic shown in Figure 4, are in good agreement with the device manufacturer's reference values. Interestingly, varying J_0 on the coupling law of the defect subdomain had a minimal influence on the resulting current-voltage characteristic regarding the entire voltage range. This is mainly due to its small area and the lack of an ohmic component. Therefore, it would be very difficult to quantify this defect with steady-state data alone. Consequently, the fitting of simulations to additional SS-DLIT measurements becomes advantageous.

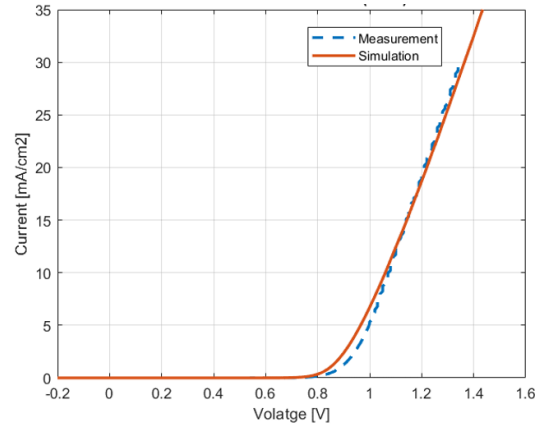


Figure 4: Measured (blue) and simulated (orange) current-voltage characteristic of the perovskite solar cell.

Figure 5 shows the image comparison between the temperature amplitude of the SS-DLIT simulation and the measurement at 0.9 and 1.6 V bias. The comparison at 0.9 V only shows a hotspot (s. Figures 5a and 5b), while at 1.6 V bias, the active area in the upper end of the cell heats up as well (s. Figures 5c and 5d).

As explained, we increased the dark saturation current on the coupling law of the defect subdomain, until we obtained the simulations with the best fitted AC temperature amplitude (s. Figure 6a). For this purpose, we compared the simulated peak AC temperatures of the active area and the defect with those of the measurements at different bias voltages. The comparison between measured and simulated AC temperature amplitude for the two subdomains is shown in Figure 6b. The measured curves show that the maximum temperature on the active area increases continuously, while the maximum temperature at the defect shows a peak and a subsequent decrease at high voltages.

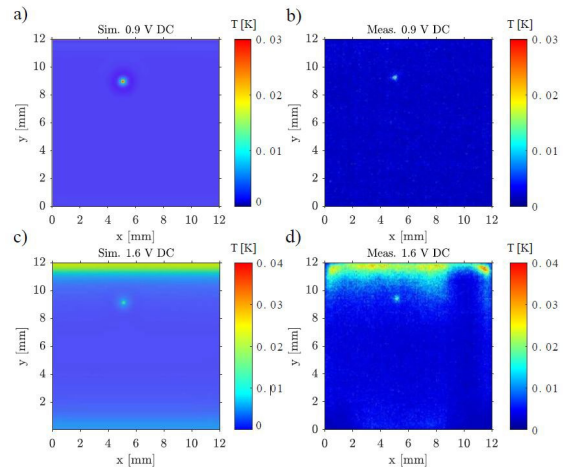


Figure 5: Amplitude image comparison between SS-DLIT simulations at 0.9 V (a) and 1.6 V (c) and measurements at 0.9 V (b) and 1.6 V (d) bias.

The reason for a temperature rise and subsequent drop in the defect subdomain is related to a complex interplay between the two coupling laws and the sheet resistance, which is responsible for a potential drop along the carbon top electrode. At lower voltages, for example at 0.9 V bias, the main current flow and subsequent heating takes place at the defect. At higher voltages, when more current flow is allowed on the active area, more Joule heating occurs in

the upper part of the device. The current takes the path of least resistance, which in this case is the better conducting FTO-bottom electrode. The thermal energy is therefore generated to a greater extent on the upper part active area and less on the defect, which is located further in the center of the device. This can be seen very clearly in the SS-DLIT measurement and simulation at 1.6 V bias.

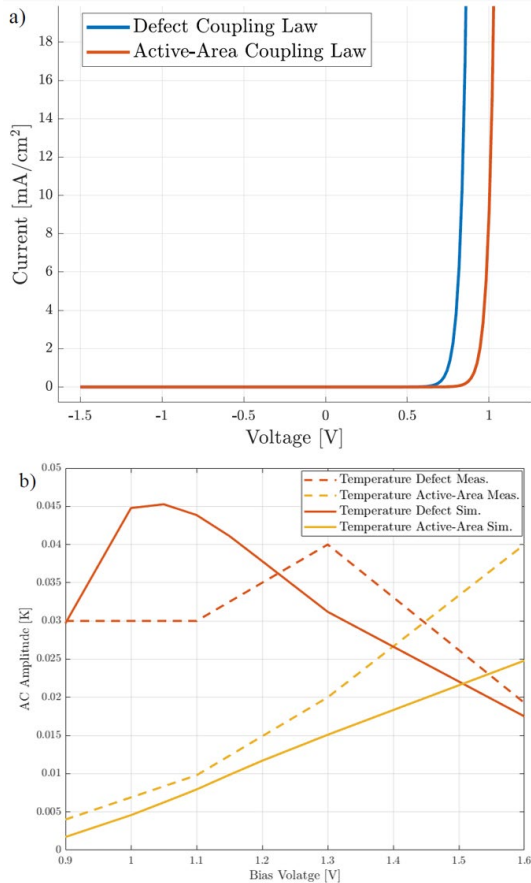


Figure 6: Resulting DC coupling laws of the active-area (orange) and the defect subdomain (blue) in (a) and (b) shows the quantitative comparison between the simulated and measured SS-DLIT temperature amplitude maxima of the defect (orange) and the active area (yellow).

Figure 7 shows the measured and simulated EL image at 1.2 V bias. Defects, such as pinholes, usually show a less radiative dark spot [29], which is clearly visible in the measurement and also in the simulation, where the potential drops in the region of the defect. The EL-measurement shows further interesting artefacts. For example, dark grid lines are visible on the entire right side. After a comparison with the printing mesh sizes used by the manufacturer, it became clear that these originate from applying too much pressure during the screen printing of the carbon layer. Dark spots are also visible on the lower corners. These originate most likely from poor perovskite filling of the porous layers. The qualitative comparison of the EL image with the simulation shows that the luminescence drop caused by the sheet resistance is well reproduced, but the cell has some artefacts such as the poor perovskite filling and the visible screen printing mesh pattern, which have not been modelled for the sake of simplicity.

The grid pattern originating from the screen-printing mesh and dark areas at the lower corners can also be seen

in the SS-DLIT measurement at 1.6 V bias, as these regions heat up less due to the lower injection of charge carriers. Therefore, not only hot spots but also cold spots are important to consider when analysing such thermal measurements.

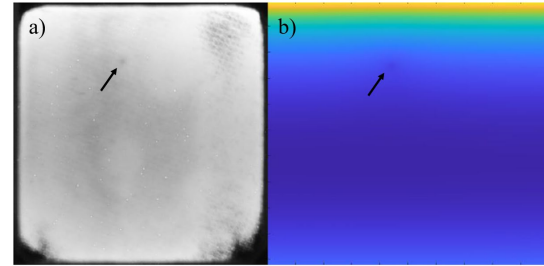


Figure 7: Qualitative comparison between measured EL-image (a) and simulated electro-luminescence based on the potential difference between top and bottom electrode (b), both at 1.2 V bias. The poor perovskite filling and the visible screen-printing mesh pattern have not been modelled for the sake of simplicity.

4 CONCLUSIONS

The prevention of defects during production of large-area perovskite solar cells is a crucial step for their commercialization. For this reason, we modelled a large-area hole-transporter-free carbon-based PSC with a pinhole defect in our FEM simulation tool and fitted the electrical steady-state and thermal AC simulation results to actual measurements (SS-DLIT) in order to characterize the defect and gather insight into its electro-thermal behaviour.

The comparison between SS-DLIT simulations and measurements allowed the characterization of the pinhole defect as we fitted the temperature amplitude of the hotspot and the active area. The SS-DLIT measurement method is worthwhile to compare measurements with simulations in order to better understand the nature of the defects and to quantify them.

This study has shown the potential in detecting nonuniformities in perovskite solar cells from a combination of current-voltage, EL and LIT measurements. These methods, together with semiconductor simulations, complement each other in many ways and can contribute significantly to improve the fabrication process and prevent degradation of solar cells and modules.

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