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Adaptive direct power control based on ANN-GWO for grid interactive renewable energy systems with an improved synchronization technique

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Summary

This paper investigates the improvement of synchronization technique for single-phase inverter. Specifically, the paper proposes a modified structure of second-order generalized integrator with frequency-locked loop (SOGI-FLL) with FLL gain normalization. The proposed structure enhances the frequency detection, which makes it a powerful technique under distorted grid voltage. The validation of the proposed synchronization method includes simulations and experimental tests using Xilinx field programmable gate array (FPGA) as the target device. Moreover, time domain simulations using the direct power control (DPC) with the proposed structure are performed. The decoupled active and reactive powers are controlled using the artificial neural networks (ANNs) trained by the mean of a metaheuristic algorithm. In this paper, the grey wolf optimizer (GWO) is proposed to train the multilayer perceptron (MLP). The proposed approach shows better generation of synchronization signals and smooth power quality, making it suitable for grid-tied and microgrids (MGs) power systems control.

KEYWORDS

adaptive control, direct power control for single-phase inverter, field programmable gate array, frequency-locked loop, neural networks, second-order generalized integrator

List of symbols and abbreviations

Symbols: C_{dc}, DC bus capacitor; C_f, grid filter capacitor; f_n, nominal frequency; f_{sw}, switch frequency; h, main clock of FPGA; K, K', constants of regulation; L, grid filter inductance; L_g, grid line emulator inductance; P^*, Q^*, set real and reactive power, respectively; P_c, capacitor power; P_{dc}, DC power; P_i, ith inputs; qu', in-quadrature voltage generated; R, grid filter resistance; R_g, grid line emulator resistance; T_I, integration step time; T_s, sampling period of analog signals; $t_{s\text{-}FLL}$, FLL settling time; $t_{s\text{-}sogi}$, SOGI settling time; u', in-phase voltage generated; U_{dc}, DC bus voltage; U_g, grid voltage RMS; W_j, ω_{ij}, weights connect the hidden layer to the output and the input layer, respectively; Γ, FLL's constant; ε_v, voltage error; ω'', ω', estimated grid frequency; ω_0, nominal grid pulsation.

Abbreviations: ACO, ant colony optimization; ANN, artificial neural network; DG, distributed generation; DKF, discrete Kalman filter; DPC, direct power control; ES, evolution strategy; FLL, frequency-locked loop; FPGA, field programmable gate array; GA, genetic algorithm; GWO, grey wolf optimizer; ITAE, integral time absolute error; MG, microgrid; MLP, multilayer perceptron; PLL, phase-locked loop; PSO, particle swarm optimization; PWM, pulse width modulation; QSG, quadrature signals generation; RDFT, recursive discrete Fourier transform; RES, renewable energy sources; SOGI, second-order generalized integrator; THD, total harmonics distortion; VSI, voltage source inverter

1 | INTRODUCTION

The global warming owing to the industry development is founded mainly on the increase in fuel consumption for electricity generation and goods transportation.[1] This phenomenon causes serious environmental problems.[1,2] Nowadays, the renewable energy sources (RES) are more and more integrated to the utility generation systems with the aim to produce green energy.[2-4] Hence, power systems will have massive grid-tied renewables and clean sources integrated as distributed generations (DGs). These generations normally use voltage source inverters (VSIs) permitting the control of the generated power.

DGs help to improve global performances of the grid by reducing the line power losses.[1] In contrast, the increased presence of grid-tied renewables via power electronics converters such as the VSI in low voltage (LV) or microgrids (MGs) increased the challenges for ensuring a correct power control, where harmonics, non-linear loads, and disturbances are more present. Therefore, an appropriate synchronization system is mandatory for ensuring accurate and stable synchronization signals free of undesirable oscillations and harmonics, which are essential for a correct power control, hence permitting to improve the power quality of the inverter and to generate better current/voltage waveforms.[5]

Grid synchronization methods include frequency-domain and time-domain methods.[6] The first group mainly uses some Fourier analysis discrete implementation techniques, and the second one tracks the fundamental component of grid voltage using some adaptive loops.[6] Time-domain methods perform better in real-time control.[7] They include conventional phase-locked loop (PLL),[6,8] PLLs based on in-quadrature signals generation (QSG),[6,9,10] PLLs based on adaptive filtering,[6,11-14] second-order generalized integrator (SOGI)–frequency-locked loop (FLL),[6,15] SOGI-FLL with FLL gain normalization,[6,16] and multiple SOGI-FLL. Most of the time-domain methods offer lower complexity compared with recursive discrete Fourier transform (RDFT) and discrete Kalman filter (DKF). However, their implementation complexity increases with the number of estimated harmonics.[17-19] As reported in literature, SOGI-FLL is more and more employed as a synchronization technique because of its simplicity (free of trigonometric functions), which makes it easy to be implemented. However, under highly distorted voltage conditions, this approach presents drift on the estimated frequency, and in some cases, DC offset or unbalance appears on the generated orthogonal signals.

This paper focuses on the improvement of the SOGI-FLL with FLL gain normalization proposed in Xin et al,[16] to generate appropriated synchronization signals along with a lower complexity. More specifically, we introduce a novel structure that permits to overcome the drawback of the previous technique in terms of frequency tracking and stability by keeping a good generation of orthogonal synchronization signals needed for control purposes.

The proposed structure guarantees a threefold goal: (1) to reduce the drift of the estimated frequency presented in the classical implementation of QSG based on SOGI-FLL, (2) to keep a good generation of orthogonal signals without DC offset or unbalance, and (3) to maintain a fast transient response under highly distorted grid voltage conditions.

This paper proposes also a powerful direct power control (DPC) technique for single-phase inverter for grid-tied LV and MG permitting to generate a smooth power quality even under highly distorted grid voltage. The proposed control based on the evolution of instantaneous power theory employs the developed structure of the SOGI-FLL to ensure accurate generation of synchronization signals. Moreover, owing to the intermittency in the DGs, the decoupled active and reactive powers are controlled using the multilayer perceptron (MLP)–artificial neural network (ANN) controllers, which are trained using evolutionary algorithm. The grey wolf optimizer (GWO) is employed to train and ensure the robustness along with a good dynamic response. This algorithm has given higher efficiency avoiding a local minimum due to high exploitation of GWO-MLP compared with the well-known algorithms such as the particle swarm optimization (PSO), genetic algorithm (GA), ant colony optimization (ACO), and evolution strategy (ES).[20]

The rest of this paper comprises the following sections. Section 2 introduces the proposed structure for frequency tracking and synchronization signals generation. Section 3 presents time-domain numerical analysis of the proposed structure and a comparison with traditional solutions. Section 4 provides experimental results of validation under sinusoidal and highly distorted voltage conditions. In Section 5, some discussions of the obtained results are given. Section 6 introduces the proposed DPC technique. Finally, Section 7 gives some concluding remarks and perspectives.

2 | FROM THE QSG TO THE PROPOSED SYNCHRONIZATION STRUCTURE

This work proposes a novel synchronization structure based on the principle of orthogonal or in-QSG from the measured voltage and the SOGI.

2.1 | Previous work

Figure 1A illustrates a block diagram of the QSG based on SOGI. This structure permits the generation of the orthogonal signals from the measured voltage. Moreover, it is easy to be implemented, it has good dynamic performances, and it has the capability to perform a delay-free filter with the desired bandwidth.[6] However, the quality of the generated orthogonal signals is affected if a mismatch of frequency or high content of harmonics appears. Hence, the SOGI-FLL with FLL gain normalization offers a frequency tracking capability, which improves the QSG.[6] Figure 1B illustrates this improved structure,where

$$\varepsilon_{\mathrm{v}} = u_{\mathrm{g}} - u', \tag{1}$$

$$K = \frac{9.2}{t_{\mathrm{s-sogi}}\omega_0}. \tag{2}$$

Equation 2 is determined as follows[6]:
Assuming $\omega = \omega' = \omega_0$, the time response of the SOGI can be evaluated using Equations 3 and 4.

$$u' = \frac{V}{\sqrt{1-(K/2)^2}}\sin\left(\omega\sqrt{1-(K/2)^2}\ t\right)e^{-\frac{K\omega}{2}t} + V\sin(\omega t), \tag{3}$$

$$qu' = \frac{V}{\sqrt{1-(K/2)^2}}\cos\left(\omega\sqrt{1-(K/2)^2}\ t\right)e^{-\frac{K\omega}{2}t} + V\cos(\omega t), \tag{4}$$

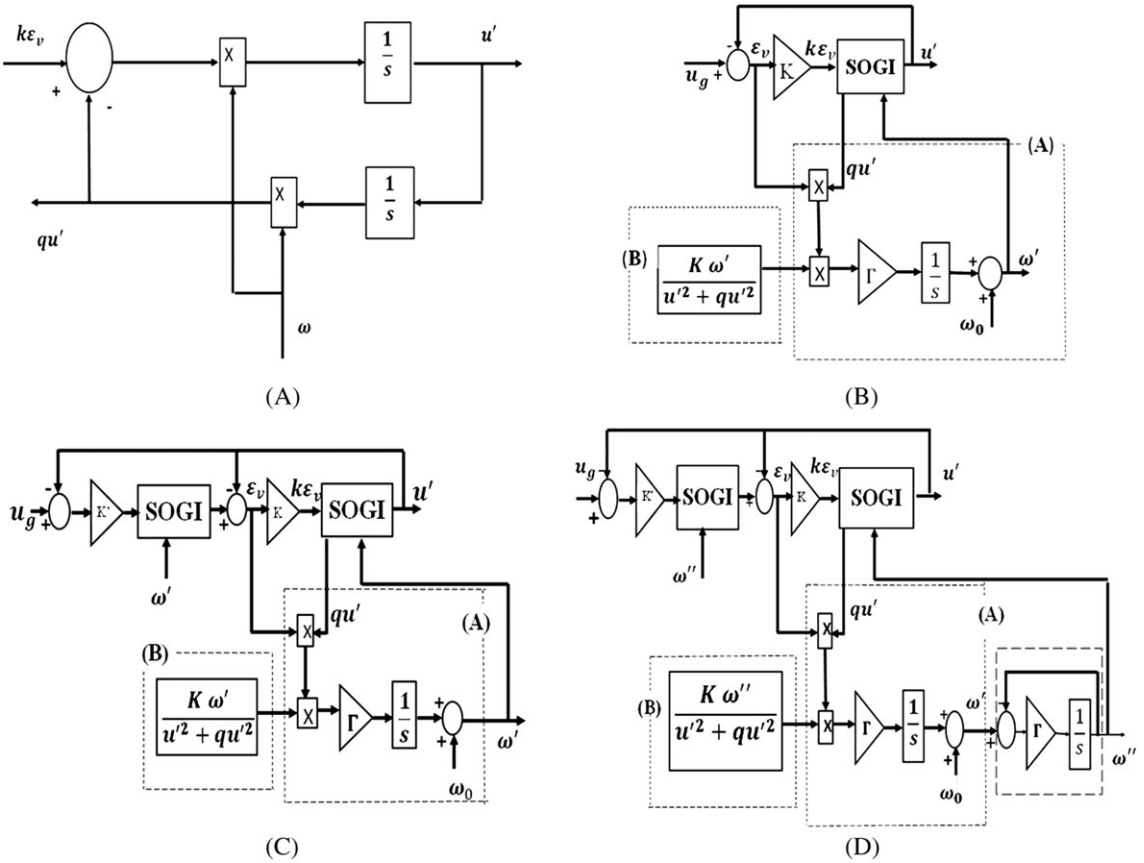

FIGURE 1 Block diagrams of, A, QSG based on SOGI, B, SOGI-FLL, C, dual SOGI-FLL, and, D, the proposed structure

since $\tau = 2/K\omega$ (Equations 3 and 4), subjected to $t_{s\_sogi} = 4.6\ \tau$. Hence, the SOGI's gain can be calculated using Equation 2.

As illustrated, the FLL gain of the SOGI-FLL is online tuned by the mean of feeding back the estimated grid conditions of operation.[6] In Figure 1B, the block marked A corresponds to the FLL and B to the FLL gain normalization. The basic parameter of this technique is the FLL constant Γ defined by (5).[6,21]

$$\Gamma = \frac{4.6}{t_{s-FLL}}, \tag{5}$$

subjected to

$$t_{s-FLL} \geq 2\, t_{s-sogi}. \tag{6}$$

The frequency detection using FLL is a practical method because it does not need the implementation of any trigonometrical function; also, it is effective during grid disturbances and power balancing.[6] Hence, the SOGI-FLL presents a good option for grid-tied synchronization.

Even the good performances for frequency tracking and QSG, the SOGI-FLL is affected by the presence of harmonics in the measured voltage. Thus, the literature reveals two main problems: a DC offset of the generated orthogonal signals and drift (oscillations) of the estimated frequency. Figure 1C presents the dual SOGI with FLL gain normalization proposed in Xin et al,[16] which allows to alleviate the first problem.

2.2 | Proposed structure for QSG using dual SOGI-FLL

In order to overcome the problems of previous work, we propose the use of a second integrator in the FLL, which permits to reduce the drift on the estimated frequency while maintaining a sound generation of orthogonal signals. Figure 1D illustrates the proposed structure for QSG and frequency tracking. The ability of the proposed structure to generate synchronization signals is related to their transfer functions (7) and (8). The bandwidth depicted in Figure 2 A used for QSG depends only on K' and K gains making it a suitable approach in variable frequency studies.

$$D_1(s) = \frac{u'(s)}{u_g(s)} = \frac{K'K\omega''^2 s^2}{s^4 + K\omega'' s^3 + \left(2 + K'K\right)\omega''^2 s^2 + K\omega''^3 s + \omega''^4}, \tag{7}$$

$$Q_1(s) = \frac{qu'(s)}{u_g(s)} = \frac{K'K\omega''^3 s}{s^4 + K\,\omega'' s^3 + \left(2 + K'K\right)\omega''^2 s^2 + K\omega''^3 s + \omega''^4}. \tag{8}$$

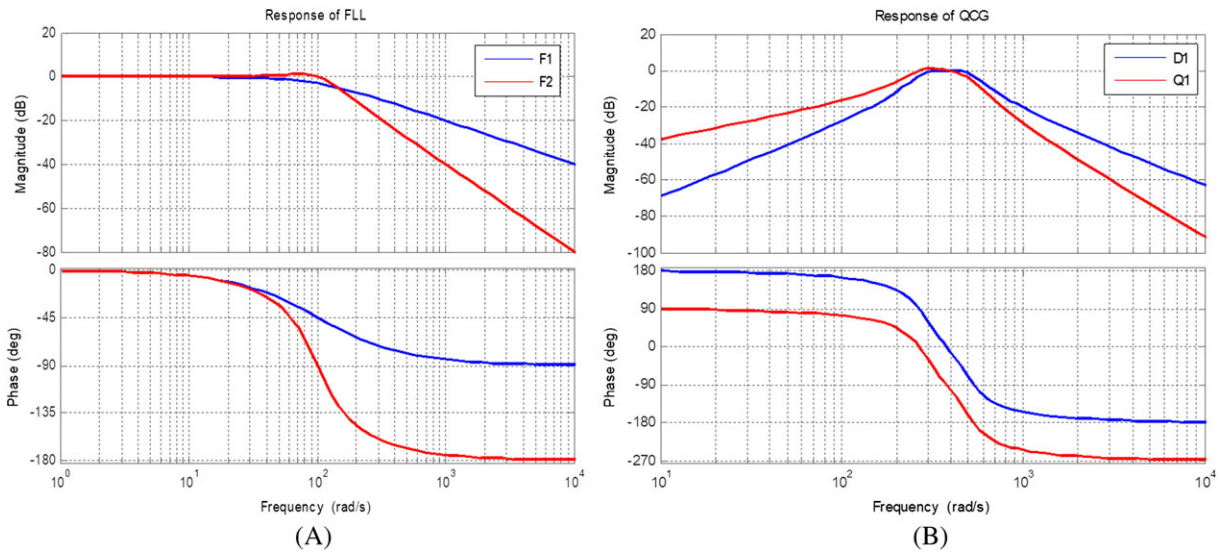

FIGURE 2 Bode plots of, A, the proposed QSG (in-phase and in-quadrature signals) and, B, classical and proposed FLLs

Notice that in previous work,[16] the frequency is tracked using first-order FLL (9):

$$F_1(s) = \frac{\omega'}{\omega} = \frac{\Gamma}{s+\Gamma}, \tag{9}$$

$$F_2(s) = \frac{\omega''}{\omega} = \frac{\Gamma^2}{s^2+\Gamma s} + \Gamma^2. \tag{10}$$

This work suggests a second pure integrator to increase the system order (10), hence improving the low-pass filtering without scarifying transient response as depicted in Figure 2B.

3 | NUMERICAL ANALYSIS OF QSG WITH SOGI UNDER DISTORTED VOLTAGE CONDITIONS

In order to illustrate the advantages of the proposed structure for frequency tracking and QSG, we conduct several numerical simulations that permit to compare it with previously proposed versions of SOGI-FLL.[6,16] In fact, time domain simulations performed with MATLAB software allowed to investigate the behaviour of synchronization techniques under distorted grid voltage. Table 1 shows the details of the harmonics content of the simulated grid voltage.

The simulation results show that classical structure of SOGI-FLL has a poor generation of synchronization signals under distorted grid voltage. More precisely, a DC offset and substantial amplitude differences appear in the generated orthogonal signals. In contrast, the dual SOGI-FLL offers a better generation of orthogonal signals considering its enhanced filtering capability. Figure 3A provides a plot of some electric cycles of these results.

Even if good results are obtained for QSG and better frequency tracking compared with the classical SOGI-FLL, the dual SOGI-FLL presents a drift on the estimated frequency of about 0.3 Hz as illustrated in Figure 3B. Notice that the oscillations observed in the estimated frequency using the classical SOGI-FLL are beyond the recommended limits of grid-connected inverters operation, which are defined within 59.3 to 60.5 Hz. This drift can affect the inverter control; hence, more improvements are required for the estimated frequency.

TABLE 1 Harmonics orders in the grid voltage

Harmonics order	3rd	5th	7th
Magnitudes, %	20	12	10
Phase shifts, rad/s	-0.7π	$0.23\ \pi$	$0.15\ \pi$

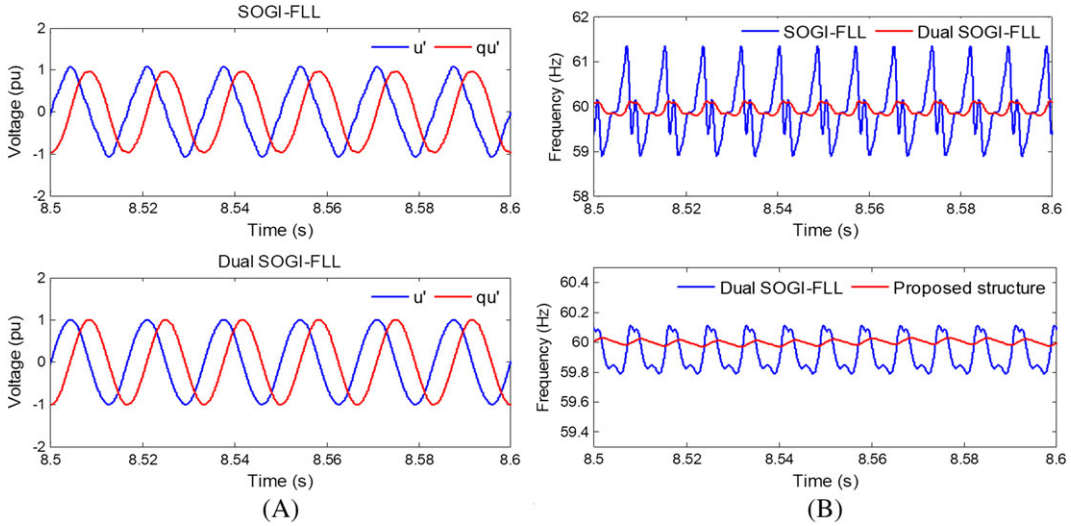

FIGURE 3 Time domain simulation of, A, orthogonal synchronization signals generated and, B, frequency tracking

The proposed technique highly improves the tracking by reducing the frequency drift (Figure 3B) compared with the previous techniques. Obviously, the oscillations on the estimated frequency depend partially on the FLL gain, which determines the settling time. We conducted an impact analysis of such parameters on the performances of the evaluated techniques. Figure 4 shows these results; here, it is clear that the proposed structure permits to obtain better steady-state response with low oscillations (drift) on the estimated frequency without scarifying the transient response.

These simulation results encouraged us to implement and to validate experimentally the proposed QSG technique. The following section will present the experimental validation study.

4 | EXPERIMENTAL VALIDATION

In order to assess and compare the performances of the dual SOGI-FLL and the proposed QSG structure, hardware implementation is performed using a Virtex-5 Xilinx FPGA (XC5VLX110T) as the target device. Thus, the two QSG methods operate in parallel, analysing simultaneously the measured voltage signal with the same conditions of noise and harmonics.

Figure 5 presents a simplified sketch and test bench used for the validation. This configuration offers two possible sources of voltage: (1) a programmable AC voltage source (Elgar SW5250) and (2) grid voltage (120 V/60 Hz) connection. A line emulator permits the interface between the source and the point of measurement.

The AC programmable source offers the possibility of emulating several voltage conditions. The following cases are considered to assess the QSG's performances.

1. Perfect sinusoidal voltage (perfect source).
2. Flat-Top 5: voltage signal with 5% of harmonic distortion.
3. Four 9: voltage signal with Fourier square wave with first, third, fifth, seventh, and ninth harmonics.
4. Noisz100: voltage signal with 100% noise at zero crossings.

Added to the previously described waveforms, we employed frequency jumps to assess the transient and frequency tracking performances.

To assess the performances of the proposed synchronization structure under several critical conditions, a direct hardware implementation is performed using Xilinx system generator as software for the FPGA target device. During the implementation part, the most challenging fact was descripting the overall structure's parts using fixed-point basic blocks along with acceptable resolution to not scarifying the overall FPGA's resources, where the basic blocks include only the arithmetic (+, −, and *). Hence, a mathematical formulation as presented in ((11)) allows the hardware description of all parts of the synchronization structure. Newton-Raphson method[22,23] is used to implement the division

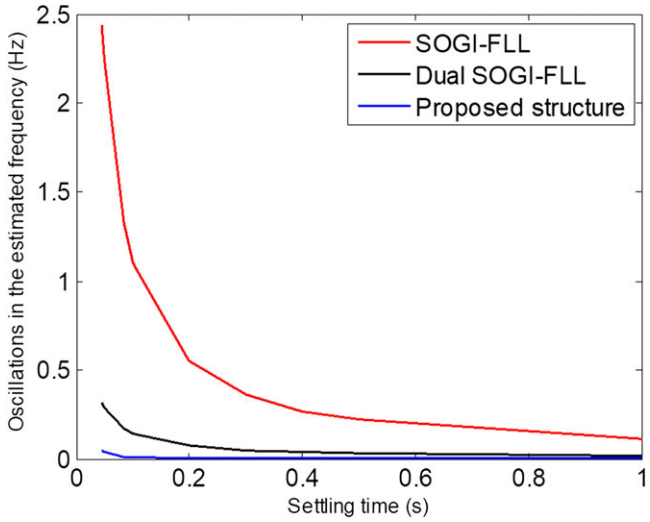

FIGURE 4 Oscillations in the estimated frequency as function of FLL's settling time for classical SOGI-FLL, the dual SOGI-FLL, and the proposed structure

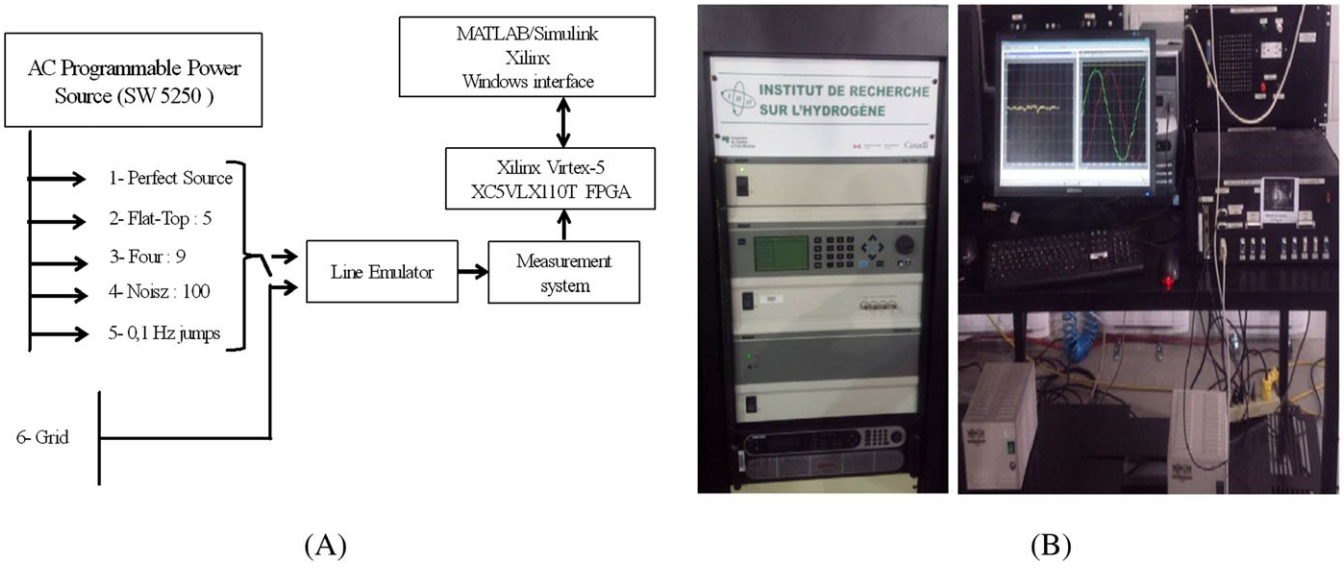

FIGURE 5 Experimental validation: A, block diagram of the test bench and, B, test bench

blocks necessary for the FLL gain normalization. Thus, Equations 12 to 14 detail the implemented procedure for computation of the normalized FLL gain (γ).

$$\begin{cases} k\varepsilon_v' = (U_g - u')K' \\ u_1' = \int (k\varepsilon_v' - qu_1')\omega'' T_I \\ qu_1' = \omega'' \int u_1' T_I \\ k\varepsilon_v = (u_1' - u')K \\ u' = \int (k\varepsilon_v - qu')\omega'' T_I \\ qu' = \omega'' \int u' T_I \\ \gamma = \dfrac{K\omega''}{u'^2 + uq'^2} \\ \omega' = \omega_0 + \int \Gamma qu' (u_1' - u')\gamma T_I \\ \omega'' = \int \Gamma(\omega' - \omega'') T_I \end{cases} \tag{11}$$

$$U'^2 = u'^2 + qu'^2, \tag{12}$$

$$x_{n+1} = x_n(2 - U'^2 x_n), \tag{13}$$

$$\gamma = x_{n+1} K\omega. \tag{14}$$

Euler method (Equation 15) is used to implement numerically the integration blocks necessary for the SOGI and the FLL.[24]

$$y_{n+1} = y_n + \frac{dy}{dt} T_I. \tag{15}$$

4.1 | Case 1: tests using perfect sinusoidal voltage

Accuracy and quality of generated orthogonal signals via a fixed-point implementation of QSG depends partially on the number of bits of arithmetic operations. Figure 6A (case 1) shows the experimental results of QSG using the fixed-point implementation with 16 and 24 bits when a perfect sinusoidal voltage is supplied by the programmable AC source. As illustrated, when 16 bits implementation is employed, a DC offset of about 5.4 V appears on the in-quadrature signal (Figure 6A, 16 bits [case 1]).

In the same way as expected, the estimated frequency is affected by undesirable and unexpected oscillations appearing as illustrated in Figure 6B, 16 bits (case 1). In contrast, the 24-bit implementation of the proposed structure permits a good generation of orthogonal signals and a better frequency tracking free of undesirable oscillations (Figure 6 A,B, 24 bits [case 2]). Obviously, the cost of a direct hardware implementation of the proposed QSG structure increases with the number of bits used for arithmetic resolution; in both cases, the percentage of the DSP blocks used in XC5VLX110T FPGA rises from 31% to 50% (20 to 32 DSP blocks) ranging from 16 to 24 bits. Notice that the proposed structure uses two more multipliers than the conventional structure of the dual SOGI-FLL, which employs 18 DSP blocks. An optimized implementation could permit in both cases to reduce the number of resources necessary to achieve the QSG.

4.2 | Case 2: tests using voltage signal distorted (Flat-Top: 5)

The IEEE standard 519-2014 limits the voltage THD at the point of common coupling (PCC) below 69 kV to 5%.[25,26] However, this test is performed in order to assess the behaviour of synchronization techniques under non-linear conditions of grid voltage using a flat-top wave signal with 5% of THD. Figure 6A (case 2) shows the measured (U_g) and the generated orthogonal signals (u' and qu') via the proposed structure; notice that there is no difference in terms of orthogonal signals generation with the classical dual SOGI-FLL. Figure 6B (case 2) presents a comparison of the frequency tracking using the classical and the proposed structure of SOGI-FLL. As expected, the frequency drift appearing with the classical solution is eliminated when the proposed structure is employed.

4.3 | Case 3: tests using voltage signal distorted (Four 9)

The third case of analysis considers a voltage signal highly distorted represented by a Fourier approximation of a square waveform with first, third, fifth, seventh, and ninth harmonics. In such case, the proposed QSG structure gives an acceptable generation of orthogonal signals. Figure 6A (case 3) illustrates well this behaviour via some electrical cycles of the measured and the generated signals. Similarly, the proposed structure offers a good frequency tracking with slight oscillations (drift). Figure 6B (case 3) shows some milliseconds of the generated frequency. It is clear that the results obtained via the proposed structure are better than the ones obtained via the classical dual SOGI-FLL.

4.4 | Case 4: tests using voltage signal with noise at zero crossings

In grid-tied operation, a satisfactory synchronization requires a reliable zero crossing detection mainly for power converter to ensure a correct power regulation.[27] Otherwise, harmful faults can be generated such as incorrect and poor grid frequency estimation, therefore an incorrect power control of the inverter.[28]

In this case of analysis, the AC programmable source supplies a highly distorted voltage signal (100% distorted) at its zero crossing point. This voltage signal permits to assess the performance of the QSG structures under real particular conditions. Figure 6A (case 4) presents a sample of the waveforms of measured voltage and the generated orthogonal signals; Figure 6B (case 4) illustrates the frequency tracking. As observed, the proposed structure accomplishes well the orthogonal signals generation that is not affected by the presence of noise at the zero crossing points. Similarly, the proposed structure keeps its frequency tracking capability even under this extreme condition of distortion at zero crossings.

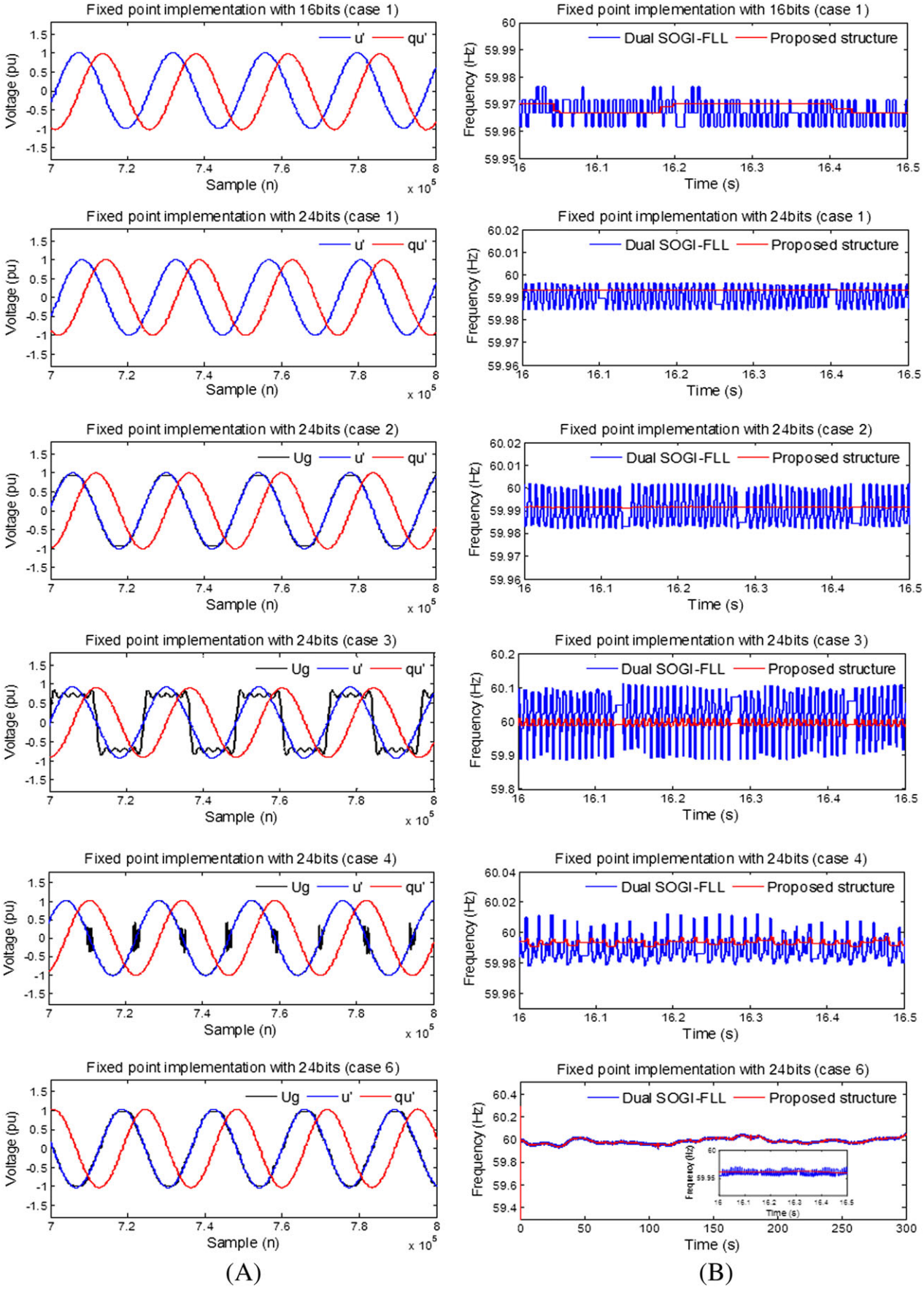

FIGURE 6 Experimental tests: A, orthogonal signals generated and, B, frequency tracking

4.5 | Case 5: tests using voltage signal with frequency jumps

Frequency jumps can appear in the voltage for large load variations. In normal grid frequency condition, the voltage varies within a range defined by the standards which are for North American systems within the range 59.3 to 60.5 Hz. Hence, in this study, the synchronization techniques are evaluated under a small frequency jump of 0.1 Hz. Figure 7A shows 300 seconds of frequency tracking when the measured voltage presents several frequency jumps and the voltage has a Fourier square waveform. A zoom-in of a step of +0.1 Hz is plotted in Figure 7B.

As observed, the experimental settling time obtained is 0.08 seconds, which is measured from the start time to the time in which the synchronization system stays within 1% of the steady-state response.[6] However the drift of the estimated frequency differs as previously indicated, showing better stability with the proposed structure.

4.6 | Case 6: tests using grid voltage signal

In this last test, the proposed synchronization technique, implemented in parallel with the classical dual SOGI-FLL, generates the orthogonal signals from the measured grid voltage. Thus, we analyse the performance of each method under real voltage conditions. As expected, both methods permit to generate the synchronization signals. It is noticed that the generated orthogonal signals using the proposed method are free of DC offset and unbalance as illustrated in Figure 6A (case 6).

The mean frequency is well estimated by the two methods; however, an important drift appears in the estimated signal when using the classical dual SOGI-FLL; in contrast, the estimated frequency is free of oscillations when using the proposed structure. Figure 6B (case 6) presents a plot of the estimated frequency during 300 seconds and a zoom-in of 500 milliseconds. These plots permit to demonstrate the superior performance of the proposed structure under real operating conditions.

5 | DISCUSSIONS

As outcomes, the simulations show that the classical SOGI-FLL has poor orthogonal signals generation and the estimated frequency drift is beyond the grid code requirements limits. The dual SOGI-FLL offers better orthogonal signals generation and frequency tracking than the classical one. However, in the latter-based technique, more improvements are needed for the frequency tracking. The proposed structure is developed with the aim of alleviating the drawback of the previous work in terms of frequency tracking and good orthogonal signals generation. The simulations performed show high superiority of the proposed structure to mitigate the drift in the frequency tracking.

An evaluation of the frequency tracking capability experimentally under the same previously analysed cases of voltage signal (cases 1 to 6) permitted to prove the superior performance of the proposed structure compared with the classical SOGI-FLL. Figure 8 presents a comparison of the drift magnitude of the estimated frequency under different voltage conditions. It is to highlight that the most challenging is case 3, where the voltage signal is a Fourier square wave with first, third, fifth, seventh, and ninth harmonics. In such an extreme case, the proposed structure permits a proper generation of the orthogonal signals and a better frequency tracking than the dual SOGI-FLL; in fact, the oscillations on the estimated frequency are 10 times smaller when using the proposed method.

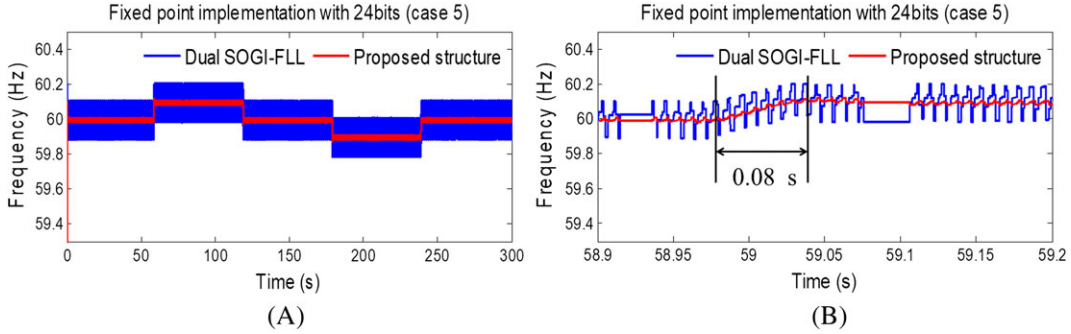

FIGURE 7 Frequency estimation with +/− 0.1 Hz jumps: A, 300 seconds of estimation using distorted voltage with Fourier square waveform. B, Zoom-in of a step of +0.1 Hz

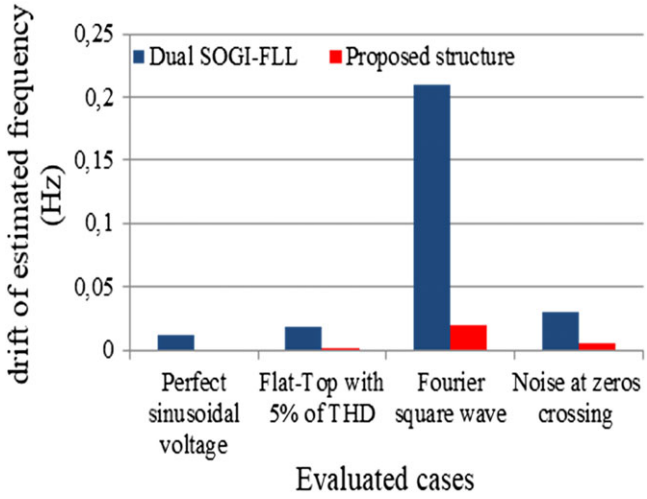

FIGURE 8 Drift of the estimated frequency for the evaluated cases

6 | INVERTER CONTROL

A global presentation of the studied system is sketched in Figure 9. The considered grid is connected to a full-bridge VSI inverter. Through the DPC, the inverter generates AC power to the grid.

The proposed DPC counts the instantaneous active and reactive power (Equations 16 and 17) in the virtual $\alpha\beta$ axis. The synchronization signals are generated using the proposed structure, and DC voltage regulator is performed in order to maintain a constant and stable voltage to the inverter. This regulator is based on the energy stored in the capacitor (C_{dc}) (Equation 18).[29] Through the MLP-ANN controllers, the system generates reference voltages to the VSI.

$$P = U_\alpha . i_\alpha + U_\beta . i_\beta \tag{16}$$

$$Q = -U_\beta . i_\alpha + U_\alpha . i_\beta \tag{17}$$

$$P_c = \frac{1}{2}\, C_{dc} \frac{d}{dt}\left(U_{dc}{}^2\right) \tag{18}$$

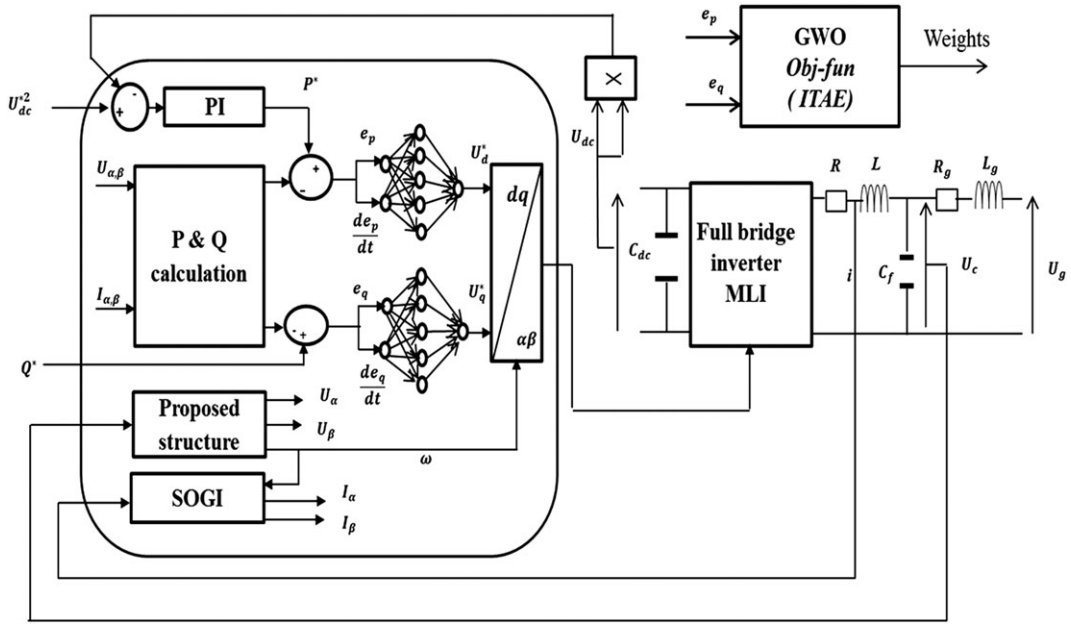

FIGURE 9 The proposed direct power control

6.1 | ANN controllers

The controllers performed are based on MLP with one hidden layer containing five neurons. This architecture is obtained by test and trial procedure to minimize the error.[30]

The mathematical implementation can be described by the following steps, where the logarithmic sigmoid is chosen as an activation function.

6.1.1 | Outputs of the inputs layer

$$N_j = \sum_{i=1}^{2} \left(\omega_{ij} P_i\right), \quad j = 1, 2, ..., 5. \tag{19}$$

6.1.2 | Outputs of the hidden neurons

$$a_j = \frac{1}{1 + \exp\left(-N_j\right)}, \quad j = 1, 2, ..., 5. \tag{20}$$

6.1.3 | Output of the output layer

$$I = \sum_{j=1}^{5} \left(W_j a_j\right), \quad j = 1, 2, ..., 5. \tag{21}$$

Note that the biases are supposed equal to 0.

The novel metaheuristic GWO[20,31] is employed to estimate the MPL-ANN weights.

6.2 | Adaptive algorithm (GWO)

The recent metaheuristic GWO is inspired from the behaviour of grey wolves swarm in nature, mainly hunting and the social leadership. However, this algorithm is presented and is widely explained in the references.[20,31]

The global minimum (Figure 10) is obtained by employing the objective function in Equation 22, which is the integral time absolute error (ITAE).

$$\text{ITAE} = \int_0^t t\,(e)dt, \tag{22}$$

where

$$e = |ep| + |eq|, \tag{23}$$

$$ep = P^* - P \&\ \ eq = Q^* - Q, \tag{24}$$

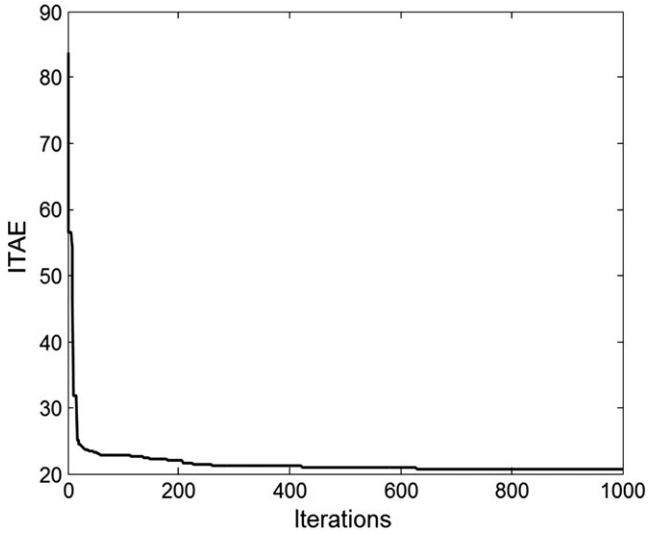

FIGURE 10 Fitness of the objective function

subject to

$$\omega_{\min} \leq \omega \leq \omega_{\max}, \tag{25}$$

$$W_{\min} \leq W \leq W_{\max}. \tag{26}$$

Note that the dimension of the problem (30), maximum iterations (1000), search agents (100), and the integral time is calculated using Simpson rule.

6.3 | Simulations results

To investigate the performance of the proposed approach, time domain simulations were carried out using MATLAB considering the parameters summarized in Tables 1–3.

The DC voltage generated by the DC bus regulator presents high flexibility and stability (Figure 11), where the generated signal reaches its reference value in about 2 milliseconds.

TABLE 2 Experimental study parameters

U_g	120 V
f_n	60 Hz
R_g	17.6 mΩ
L_g	1.7 μH
R	2.05 ms
L	2 mH
C_f	20 μF
h	10 ns
T_s	10 μs

TABLE 3 Inverter parameters

P_{dc}	1 kW
f_{sw}	10 kHz
U_{dc}	195 V

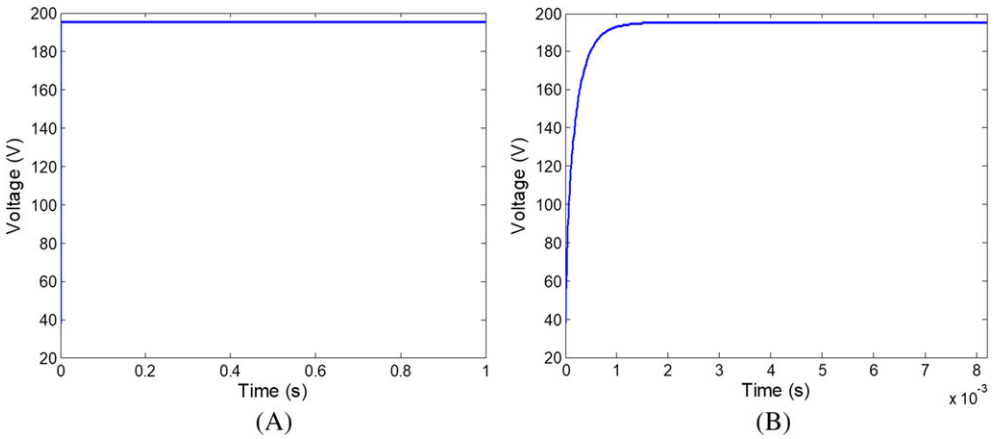

FIGURE 11 DC bus voltage: A, 1 second of DC bus voltage respond and, B, transient respond of DC bus voltage

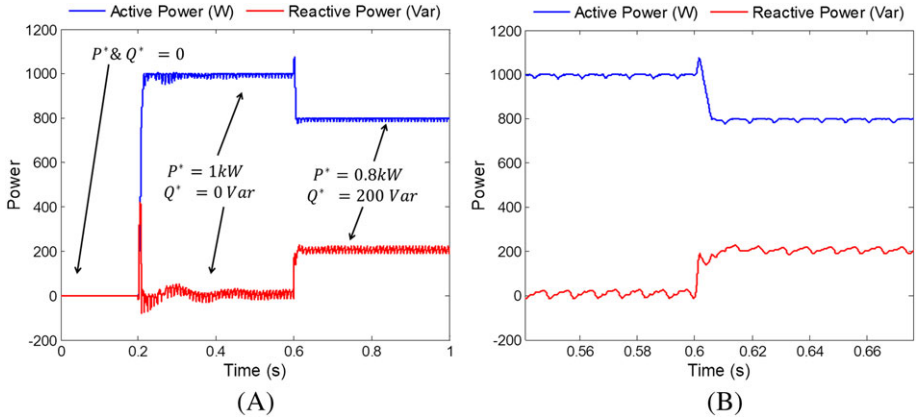

FIGURE 12 Active and reactive power generated to the grid: A, 1 second of time domain simulations; B, zoom-in of the transient response

Figure 12 shows a good dynamic generation of the active and reactive powers, even when operating under grid harmonics (Table 1), owing to the ability of the proposed structure to generate synchronization signals and the robustness of the proposed DPC based on MLP-ANN-GWO.

7 | CONCLUSION

In this paper, a novel structure of synchronization based on SOGI-FLL is proposed in order to enhance the grid frequency estimation while keeping a proper generation of orthogonal signals needed for control purposes. This technique has been evaluated by simulation and by experiments under different operating conditions and compared with classical dual SOGI-FLL.

The proposed method, implemented in the FPGA for validation purposes, permits to track the frequency of the measured voltage even in highly distorted conditions. The obtained results demonstrate good generation of synchronization signals without common related problems such us unbalance, DC offset, or drift on the estimated frequency.

The performance of this technique compared with the classical ones lies in the large ability to track the grid frequency with highest accuracy and along with faster response. Hence, by using this technique, the capability of the power converter to generate an accurate and smooth power in grid-tied mode or MG is considerably raised.

This work also proposes a robust DPC for single-phase inverter based on MLP-ANN-GWO to ensure adaption process. The evaluated strategy has proven its efficiency by generating a smooth power even under distorted grid voltage.

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