MDPI

Article

Temperature-Independent Current Dispersion in 0.15 μm AlGaN/GaN HEMTs for 5G Applications

Nicolò Zagni [1,*], Giovanni Verzellesi [2] and Alessandro Chini [1]

1 Department of Engineering "Enzo Ferrari", University of Modena and Reggio Emilia, via P. Vivarelli 10, 41125 Modena, Italy
2 Department of Sciences and Methods for Engineering (DISMI) and EN&TECH Center, University of Modena and Reggio Emilia, via G. Amendola, 2, 42122 Reggio Emilia, Italy
* Correspondence: nicolo.zagni@unimore.it

Abstract: Thanks to high-current densities and cutoff frequencies, short-channel length AlGaN/GaN HEMTs are a promising technology solution for implementing RF power amplifiers in 5G front-end modules. These devices, however, might suffer from current collapse due to trapping effects, leading to compressed output power. Here, we investigate the trap dynamic response in 0.15 μm GaN HEMTs by means of pulsed I-V characterization and drain current transients (DCTs). Pulsed I-V curves reveal an almost absent gate-lag but significant current collapse when pulsing both gate and drain voltages. The thermally activated Arrhenius process (with $E_A \approx 0.55$ eV) observed during DCT measurements after a short trap-filling pulse (i.e., 1 μs) indicates that current collapse is induced by deep trap states associated with iron (Fe) doping present in the buffer. Interestingly, analogous DCT characterization carried out after a long trap-filling pulse (i.e., 100 s) revealed yet another process with time constants of about 1–2 s and which was approximately independent of temperature. We reproduced the experimentally observed results with two-dimensional device simulations by modeling the *T*-independent process as the charging of the interface between the passivation and the AlGaN barrier following electron injection from the gate.

Keywords: GaN HEMTs; 5G; current collapse; T-independent process; Fe doping; TCAD simulations

Citation: Zagni, N.; Verzellesi, G.; Chini, A. Temperature-Independent Current Dispersion in 0.15 μm AlGaN/GaN HEMTs for 5G Applications. *Micromachines* **2022**, *13*, 2244. https://doi.org/10.3390/mi13122244

Academic Editor: Sadia Ameen

Received: 26 November 2022
Accepted: 16 December 2022
Published: 17 December 2022

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

Short-channel length AlGaN/GaN high-electron mobility transistors (HEMTs) are an interesting technology option for realizing highly efficient power amplifiers in 5G communications systems, due to the high power/frequency handling capability and efficiency they offer [1]. Operation at high-voltage levels might induce the so-called "current collapse" effect that compresses the RF output power—thus limiting efficiency—and can trigger trapping effects in different regions of these devices [2–6]. Careful analysis of the physical mechanisms inducing such detrimental power compression is therefore required.

Here, we investigate the current-collapse effects in 0.15-μm AlGaN/GaN HEMTs by means of electrical characterization in terms of pulsed I-V curves and drain current transients (DCTs). Concerning the pulsed characterization, comparison between pulsing from the ($V_{GS,B}$,$V_{DS,B}$) = (0, 0) V baseline and from ($V_{GS,B}$,$V_{DS,B}$) = (V_{TH}−1, 0), (V_{TH}−1, 28), and (V_{TH}−1, 56) V (V_{TH} is device threshold voltage). Remarkably, the devices-under-test (DUTs) exhibited negligible gate-lag [2], while showing a significant current collapse when pulsing both gate and drain voltage from OFF to ON state. To obtain information about the involved traps, we performed DCT characterization [7,8] at different temperatures by applying short (1 ms) and long (100 s) trap-filling pulses in the OFF-state ($V_{GS,OFF}$, $V_{DS,OFF}$) = (V_{TH}−1, 56) V and monitor drain current transient response during recovery at quiescent point conditions ($V_{GS,Q}$, $V_{DS,Q}$) = (−1, 2) V for up to 100 s. After applying the short trap-filling pulse, the typical DCT due to electron emission from traps associated with Fe-doping in the buffer was observed [9,10], as confirmed by the activation energy

$E_A \approx 0.55$ eV of the thermally activated process. In the case of the long filling pulse, DCTs still exhibited the thermally activated response due to electron emission from Fe traps; however, an additional T-independent process was identified. The experimental findings were reproduced with two-dimensional device simulations including Fe traps in the buffer and a charging mechanism of the passivation/barrier interface.

The paper is organized as follows. In Section 2, we describe the devices under study (DUTs). In Section 3 we present the characterization results in terms of pulsed I-V curves and drain current transients. In Section 4 we present the simulation results. Finally, in Section 5 we draw the conclusions.

2. Devices under Study

The devices under study (DUTs) were AlGaN/GaN HEMTs grown on SiC substrates. The AlGaN barrier layer is 15 nm thick with a 22% aluminum concentration. Iron (Fe) impurities are introduced in the 2 µm-thick GaN buffer to reduce drain-source leakage and increase breakdown voltage. Iron concentration in the GaN buffer starting from the SiC substrate interface was constant at 1×10^{18} cm^{-3} until 0.6 µm below the AlGaN/GaN interface, above which it decayed with a slope of one decade every 0.4 µm. The devices were passivated by a 100 nm-thick SiN layer. Gate length (L_G) was 0.15 µm and gate width (W_G) was 2 × 25 µm. Threshold voltage (V_{TH}) was −2.2 V. The cross-section of the DUTs is shown in Figure 1.

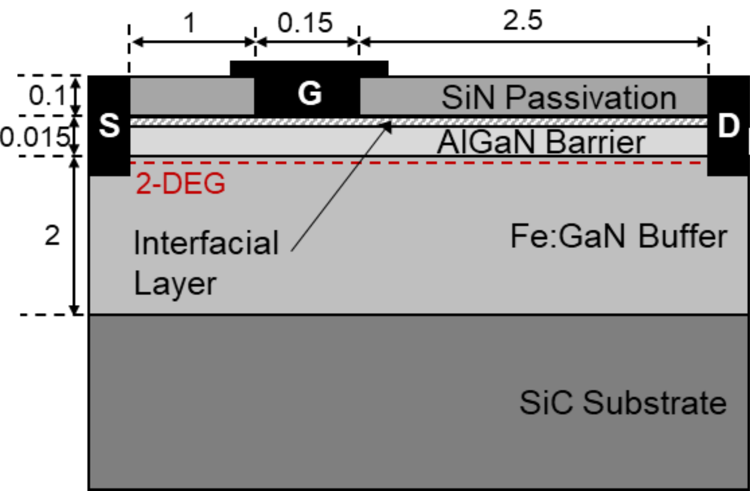

Figure 1. Schematic cross-section of the DUTs. 2-DEG stands for two-dimensional electron gas. A narrow (2 nm) interface layer between the passivation and AlGaN barrier was introduced in the simulations to reproduce experimental results, as discussed in more detail in Section 4. Reported dimensions are in µm (not to scale).

3. Experimental Results

Measurements were carried out by means of: (i) a custom-made drain switch that allows applying two selectable voltage levels to the drain terminal; (ii) a Keysight 33520B dual-channel waveform generator for the gate signal and drain switch control; (iii) a Keysight E3647A dual-channel power supply providing the two drain voltage levels applied during the measurements; (iv) a PicoScope 5444D four-channel 200 MHz digital sampling oscilloscope for acquiring the signals needed for V_D and I_D measurement.

3.1. Pulsed I-V Curves

Pulsed I-V measurements were carried out by applying synchronous voltage pulses to the gate and drain terminals from a reference baseline while keeping the source contact grounded. Voltage pulses were 1 µs long with duty cycle of 1%. An illustration of the signal waveforms used for the pulsed I-V curves acquisition is shown in Figure 2

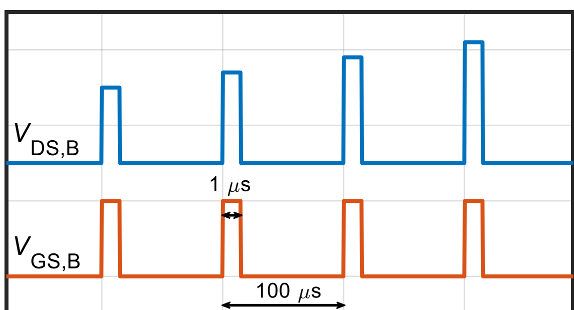

Figure 2. Illustration of signal waveforms employed during the pulsed I-V characterization. Short (1-μs) pulses were synchronously applied at the drain and gate terminals from the respective reference baseline ($V_{DS,B}$ and $V_{GS,B}$) with duty cycle 1%. The I-V curves were acquired from four different baselines, see Figure 3.

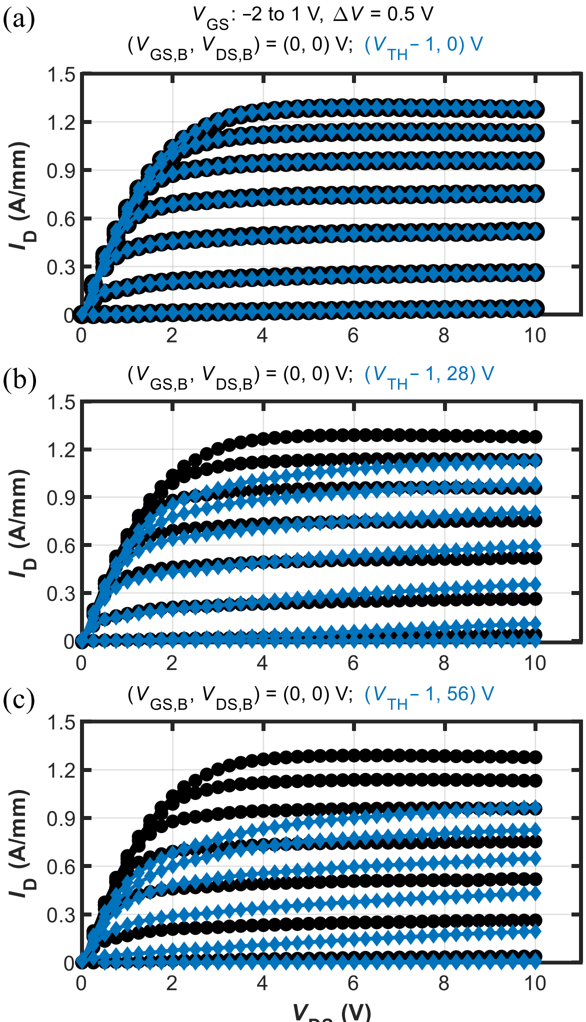

Figure 3. Pulsed I_D-V_{DS} characteristics obtained from different baselines for V_{GS} = −2 to 1 V (ΔV = 0.5 V). Negligible gate-lag (assessed by pulsing from $V_{GS,B}$ = V_{TH}−1 V) is shown in panel (**a**); significant dispersion shown in panels (**b**,**c**) (assessed when pulsing from $V_{GS,B}$ = V_{TH}−1 V and V_{DS} = 28 or 56 V) suggests current collapse was mainly induced by deep trap states in the buffer.

Results of this kind of characterization are shown in Figure 3 in terms of output I_D-V_{DS} curves. The output characteristics were acquired from four different baselines, namely: ($V_{GS,B}$,$V_{DS,B}$) = (0, 0), (V_{TH}−1, 0), (V_{TH}−1, 28), and (V_{TH}−1, 56) V. Figure 3a shows the comparison between the (0,0) and (V_{TH}−1, 0) baselines, allowing us to assess the gate-lag

effect. Interestingly, in these devices no appreciable gate-lag was detected, indicating excellent stability of the device region under the gate. Figure 3b,c show the comparison between the (0,0) baseline and the (V_{TH}–1, 28) and (V_{TH}–1, 56), respectively. Both figures showed moderate increase of knee voltage but significant saturated current compression, especially for I_D-V_{DS} curves at high V_{GS}. These results indicate that trapping effects leading to current collapse were most likely happening in the gate-drain access region [2]. As such, the amount of degradation as well as its dependence on the applied V_{DS} were influenced by the gate-to-drain spacing.

3.2. Drain Current Transients

As discussed in Section 2, the GaN HEMTs under study were intentionally Fe-doped to reduce leakage and, consequently, increase breakdown voltage. However, Fe-related traps in the buffer are well known to cause dispersion effects [9] similar to those observed in Figure 3. Therefore, the subsequent characterization by means of DCTs measurement was performed to clarify the role of Fe-related buffer traps. DCTs were acquired at several temperatures, i.e., T = 30–70 °C with 10 °C steps, to characterize the activation energy of the drain current recovery process. An illustration of the signal waveforms used for the DCTs acquisition is shown in Figure 4.

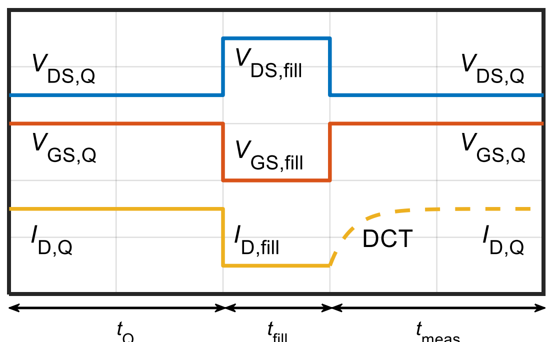

Figure 4. Illustration of signal waveforms employed during the DCT characterization. A short (1 µs) or long (100 s) trap-filling pulse was applied by driving the device in the OFF-state. Then, DUT was biased back at ($V_{GS,Q}$, $V_{DS,Q}$) and I_D was measured over several time decades up to 100 s to acquire the actual DCT. Waveform values and time intervals are not in scale.

The quiescent bias conditions were ($V_{GS,Q}$,$V_{DS,Q}$) = (−1, 2) V; during the trap-filling pulse bias was set to ($V_{GS,fill}$, $V_{DS,fill}$) = (V_{TH}–1, 56) V to have a sufficient signal amplitude during DCT monitoring. Trap-filling pulse duration (t_{fill}) was set to 1 µs, which ensured trapping in Fe-associated states [9,10]. Figure 5 shows the results of DCT monitoring after application of the short filling pulse.

It can be observed that in Figure 5 and subsequent ones I_D during DCT was normalized to final value for the sake of comparison. Clear single-exponential waveforms can be identified in Figure 5a, which is typical of pure electron emission from point defects associated with Fe-doping [9–11]. To extract the activation energy (E_A) of the thermally activated emission process, time constants of the DCTs at each temperature were extracted by fitting the transients with streched exponential functions [12], and determined as the point where the $dI_D/d[\log_{10}(t_{meas})]$ signals peaked (see Figure 5b). Linear fitting of the Arrhenius plot in the inset of Figure 5b allowed extracting $E_A \approx 0.55$ eV, which is typical of Fe-associated traps [2,9,12].

Interestingly, when applying a long trap-filling pulse (t_{fill} = 100 s) the DCT measurements revealed a picture richer in texture compared to the previous case. As shown by Figure 6, two separate processes could be identified. The first is analougous to the one revealed by Figure 5, and can be attributed to Fe-related traps, as confirmed by the Arrhenius plot in the inset of Figure 6b. The second process instead was characterized by time constants of about 1–2 s and negligible acceleration with temperature, as shown in Figure 6.

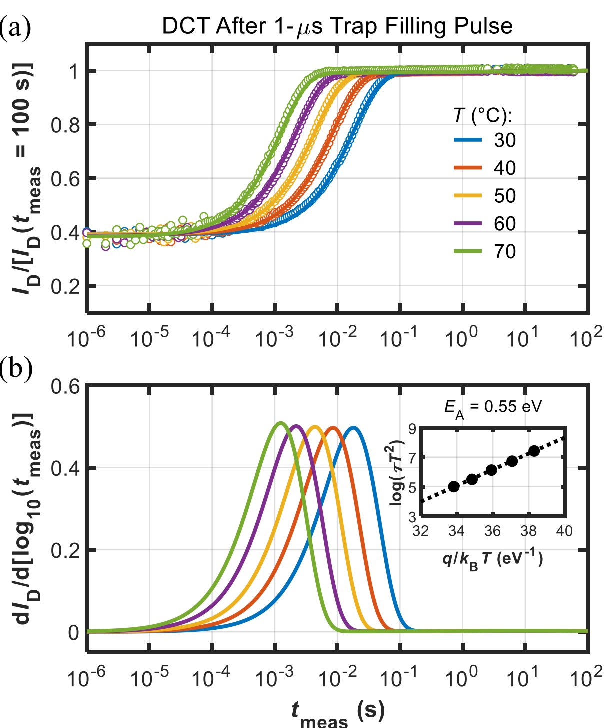

Figure 5. (**a**) DCTs measured at different temperature (see legend) after the short 1 us trap-filling pulse (dots are data and lines are fitting functions). Current was normalized to final value, i.e., $I_D(t_{meas} = 100$ s). (**b**) $dI_D/d[\log10(t_{meas})]$ used for the extraction of the time constants (τ) to build the Arrhenius plot (see inset) that yielded $E_A = 0.55$ eV.

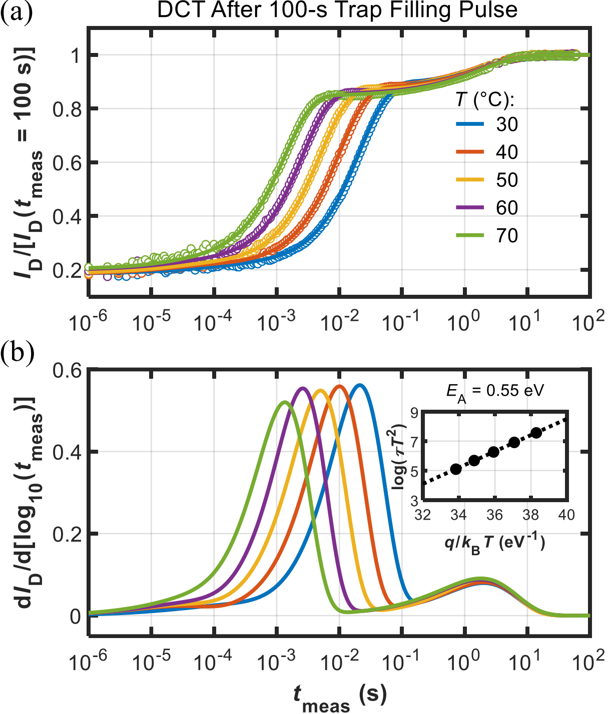

Figure 6. (**a**) DCTs measured at different temperatures (see legend) after the long 100 s trap-filling pulse (dots are data and lines are fitting functions). Current was normalized to final value, i.e., $I_D(t_{meas} = 100$ s). (**b**) $dI_D/d[\log10(t_{meas})]$ used for the extraction of the time constants (τ) to build the Arrhenius plot (see inset) that yielded $E_A = 0.55$ eV. In this case, another T-independent process was observed.

4. Simulation Results

To confirm the role of Fe-related traps shown in Figures 5 and 6 and to gain more insights into the nature of the second, T-independent process identified earlier, we performed two-dimensional device simulations with the TCAD commercial software SDevice^{TM} [13]. Charge transport was modeled by means of the drift-diffusion equations. Electron mobility in the 2-DEG was set to 1800 $cm^2/V.s$ at room temperature [14]. Electron saturation velocity in GaN was set to 1.5×10^7 cm/s. The piezoelectric polarization charge at the AlGaN/GaN interface was modeled with the default strain model of the simulator. Gate leakage current present in the Schottky junction between the metal and the AlGaN barrier was modeled by the thermionic- and field-emission mechanisms. A nonlocal tunneling model based on the WKB approximation allowed computing self-consistently the field-dependent component of the gate current [15]. Fe traps were introduced as acceptor-like states in the buffer 0.55 eV below GaN conduction band, with a capture cross-section for electrons of 1.7×10^{-15} cm^2. Analogously to the actual samples, Fe trap concentration was uniform and equal to 1×10^{18} cm^{-3} up to 0.6 µm below the AlGaN/GaN interface, from which concentration exponentially decayed one decade per 0.4 µm [10,16]. Interestingly, the temperature-independent process put experimentally into evidence with long filling pulses could be emulated by simulations by assuming that this phenomenon was induced by electron injection from the gate into a thin (2 nm) interface layer between the passivation and the AlGaN barrier, see Figure 1.

The electron transport through this layer, possibly governed by a hopping mechanism, is mimicked, introducing a large density of shallow levels with a very small electron capture cross-section. Simulation results in terms of DCTs, carried out under the same conditions employed during the experiments on the DUTs, are shown in Figures 7 and 8 for the short (1 µs) and long (100 s) trap-filling pulses, respectively. The good agreement between simulations and experimental data indicates the soundness of the modeling framework adopted here, validating the role of Fe traps in the observed current-collapse effects and suggesting the route for a full understanding of the slow recovery process.

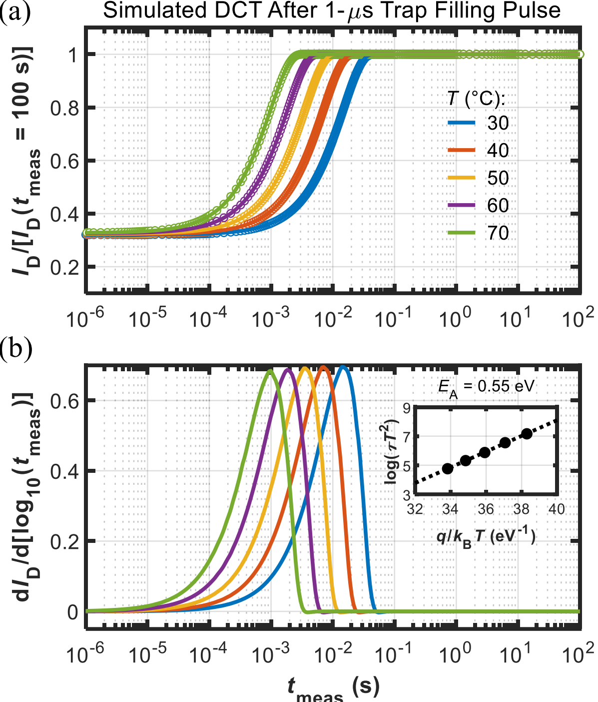

Figure 7. (**a**) Simulated DCTs at different temperature (see legend) after the short 1 us trap-filling pulse (dots are data and lines are fitting functions). Current was normalized to final value, i.e., $I_D(t_{meas} = 100$ s). (**b**) $dI_D/d[log10(t_{meas})]$ used for the extraction of the time constants (τ) to build the Arrhenius plot (see inset) that yielded E_A = 0.55 eV.

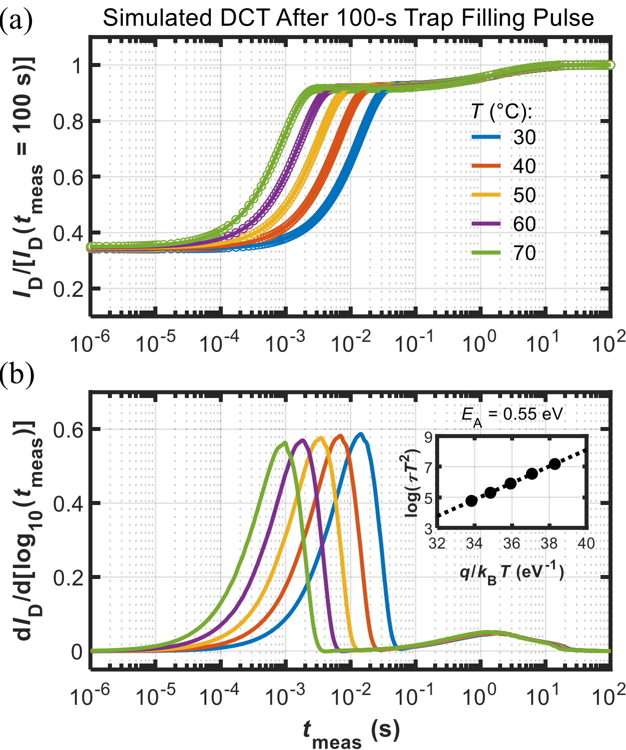

Figure 8. (**a**) Simulated DCTs at different temperatures (see legend) after the long 100 s trap-filling pulse (dots are data and lines are fitting functions). Current was normalized to final value, i.e., $I_D(t_{meas} = 100$ s). (**b**) $dI_D/d[\log10(t_{meas})]$ used for the extraction of the time constants (τ) used to build the Arrhenius plot (see inset) that yielded $E_A = 0.55$ eV. Both processes found in Figure 4 were reproduced by the simulations.

5. Conclusions

We investigated the current dispersion in short gate-length AlGaN/GaN HEMTs for 5G applications. Pulsed I-V characterization revealed the absence of pure gate-lag effects but significant current-collapse effects under double gate and drain voltage pulsing. Drain current transients (DCTs) carried out after a short 1 µs trap-filling pulse revealed that current collapse was mainly due to Fe-doping related traps in the GaN buffer. In addition, DCTs carried out after long 100 s trap-filling pulse disclosed an additional slow T-independent process that contributed to the total current dispersion. Two-dimensional device simulations validated the role of Fe traps and suggested that the slow process can be related to surface charging effects induced by gate electron injection and transport through the passivation/barrier interface.

Author Contributions: Conceptualization, N.Z. and A.C.; formal analysis, N.Z., G.V. and A.C.; methodology, N.Z., G.V. and A.C.; experimental characterization, A.C.; simulations, N.Z.; writing—original draft preparation, N.Z.; writing—review and editing, N.Z., G.V. and A.C.; supervision, G.V. and A.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Italian Ministry for University and Research (MIUR) through the PRIN 2017 Project "Empowering GaN-on-SiC and GaN-on-Si Technologies for the Next Challenging Millimeter-Wave Applications."

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Acknowledgments: The authors thank Luca Selmi (University of Modena and Reggio Emilia) for fruitful discussions.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Yuk, K.; Branner, G.R.; Cui, C. Future directions for GaN in 5G and satellite communications. In *Midwest Symposium on Circuits and Systems*; IEEE: Boston, MA, USA, 2017; pp. 803–806. [CrossRef]
2. Meneghini, M.; De Santi, C.; Abid, I.; Buffolo, M.; Cioni, M.; Khadar, R.A.; Nela, L.; Zagni, N.; Chini, A.; Medjdoub, F.; et al. GaN-based power devices: Physics, reliability and perspectives. *J. Appl. Phys.* **2021**, *130*, 227. [CrossRef]
3. Vetury, R.; Zhang, N.Q.; Keller, S.; Misha, U.K. The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs. *IEEE Trans. Electron Devices* **2001**, *48*, 560–566. [CrossRef]
4. Wang, F.; Chen, W.; Sun, R.; Wang, Z.; Zhou, Q.; Zhang, B. An analytical model on the gate control capability in p-GaN Gate AlGaN/GaN high-electron-mobility transistors considering buffer acceptor traps. *J. Phys. D Appl. Phys.* **2020**, *54*, 095107. [CrossRef]
5. Wang, Z.; Zhang, Z.; Wang, S.; Chen, C.; Wang, Z.; Yao, Y. Design and Optimization on a Novel High-Performance Ultra-Thin Barrier AlGaN/GaN Power HEMT With Local Charge Compensation Trench. *Appl. Sci.* **2019**, *9*, 3054. [CrossRef]
6. Zagni, N.; Chini, A.; Puglisi, F.M.; Meneghini, M.; Meneghesso, G.; Zanoni, E.; Pavan, P.; Verzellesi, G. Hole Redistribution' Model Explaining the Thermally Activated RON Stress/Recovery Transients in Carbon-Doped AlGaN/GaN Power MIS-HEMTs. *IEEE Trans. Electron Devices* **2021**, *68*, 697–703. [CrossRef]
7. Meneghesso, G.; Meneghini, M.; Bisi, D.; Rossetto, I.; Cester, A.; Mishra, U.K.; Zanoni, E. Trapping phenomena in AlGaN/GaN HEMTs: A study based on pulsed and transient measurements. *Semicond. Sci. Technol.* **2013**, *28*, 074021. [CrossRef]
8. Joh, J.; del Alamo, J.A. A current-transient methodology for trap analysis for GaN high electron mobility transistors. *IEEE Trans. Electron Devices* **2011**, *58*, 132–140. [CrossRef]
9. Cioni, M.; Zagni, N.; Selmi, L.; Meneghesso, G.; Meneghini, M.; Zanoni, E.; Chini, A. Electric Field and Self-Heating Effects on the Emission Time of Iron Traps in GaN HEMTs. *IEEE Trans. Electron Devices* **2021**, *68*, 3325–3332. [CrossRef]
10. Zagni, N.; Cioni, M.; Chini, A. Effect of Trap-Filling Bias on the Extraction of the Time Constant of Drain Current Transients in AlGaN/GaN HEMTs. In *IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*; IEEE: Redondo Beach, CA, USA, 2021; pp. 231–235. [CrossRef]
11. Cardwell, D.W.; Sasikumar, A.; Arehart, A.R.; Kaun, S.W.; Lu, J.; Keller, S.; Speck, J.S.; Mishra, U.K.; Ringel, S.A.; Pelz, J.P. Spatially-resolved spectroscopic measurements of Ec-0.57 eV traps in AlGaN/GaN high electron mobility transistors. *Appl. Phys. Lett.* **2013**, *102*, 193509. [CrossRef]
12. Bisi, D.; Meneghini, M.; de Santi, C.; Chini, A.; Dammann, M.; Bruckner, P.; Mikulla, M.; Meneghesso, G.; Zanoni, E. Deep-level characterization in GaN HEMTs-Part I: Advantages and limitations of drain current transient measurements. *IEEE Trans. Electron Devices* **2013**, *60*, 3166–3175. [CrossRef]
13. Synopsys. *Sentaurus SDevice Manual (S-2021.06)*; Synopsys: Mountain View, CA, USA, 2021.
14. Zagni, N.; Chini, A.; Puglisi, F.M.; Pavan, P.; Verzellesi, G. The effects of carbon on the bidirectional threshold voltage instabilities induced by negative gate bias stress in GaN MIS-HEMTs. *J. Comput. Electron.* **2020**, *19*, 1555–1563. [CrossRef]
15. Zagni, N.; Puglisi, F.M.; Pavan, P.; Chini, A.; Verzellesi, G. Insights into the off-state breakdown mechanisms in power GaN HEMTs. *Microelectron. Reliab.* **2019**, *100–101*, 113374. [CrossRef]
16. Uren, M.J.; Moreke, J.; Kuball, M. Buffer design to minimize current collapse in GaN/AlGaN HFETs. *IEEE Trans. Electron Devices* **2012**, *59*, 3327–3333. [CrossRef]