Dc-MMC for the interconnection of HVDC grids with different line topologies

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Abstract—**DC-DC converters are needed for the future development of high voltage direct current (HVDC) grids, as they allow to interconnect lines with different voltages and topologies. The dc-dc converters can increase the grid controllability adding power flow control, voltage regulation and/or fault blocking capability. The dc modular multilevel converter (dc-MMC) is a non-isolated solution proposed to interconnect HVDC systems with the same line topology. This paper proposes a new dc-MMC with a control strategy, which allows the converter to interconnect different line topologies (e.g., rigid bipole connected to a symmetric monopole). The paper presents the different line topologies in HVDC installations. Then, a mathematical model with a variable transformation is proposed for the new dc-dc converter. A control structure is proposed and implemented in Matlab/Simulink using an average arm model and simplified dc grids. The results validate the control in normal operation, fault blocking capability and post-fault scenario (degraded mode).**

Index Terms—**DC-DC converter, HVDC, dc-MMC, M2DC, line topology, non-isolated converter.**

I. INTRODUCTION

DC-DC converters have been identified as a key element for the future direct current high voltage (HVDC) multi-terminal or grid interconnections [1]–[5]. Dc-dc converters enable the interconnection between two or more dc systems with different characteristics such as the voltage level, the technology, the line topology or grounding strategy. These characteristics change from one project to another as there is no standard for the HVDC installations yet. The voltage level can vary from 100 kV for the smaller projects and up to 800 kV for the multi-terminal Wudongde VSC ultra-HVDC project [6]. The technology can be either line commutated converters (LCCs) or voltage source converters (VSCs) [7]. The line topology and grounding strategy can vary depending on the protection strategy implemented (e.g., symmetric monopole with start point reactor or a solidly grounded bipole).

Dc-dc converters can increase the system controllability and reliability with additional functionalities such as power flow control; voltage regulation; fault blocking capability; the ability to stop instabilities from spreading to healthy sides (firewall capability); interface between protection zones; and the ability to reconfigure the system after a fault, which increases the redundancy [5]. As a result of these functionalities, dc-dc converters have been studied for the development of future multi-terminal or HVDC grids.

HVDC dc-dc converters can be classified in isolated and non-isolated converters [8]–[10]. In general, the isolated converters use an ac transformer to provide galvanic isolation between the interconnected systems. This is the case of the front-to-front (F2F) topologies, which have two conversion stages: dc-ac and ac-dc, where each stage is rated at the nominal power. In particular, the F2F with modular multilevel converters (MMCs) is the preferred solution [11], [12]. The ac transformer can withstand the differences between the interconnected dc systems (e.g., voltage or grounding differences), but it is voluminous and costly. The transformer size can be reduced if the operating frequency is increased but at cost of increasing the switching and transformer losses [2], [13]. Moreover, due to the isolation distances, the volume reduction is not proportional to the frequency, so very high frequencies are not relevant [2], [5], [13].

Non-isolated converters have lower losses and cost compared to the F2F-MMC [5], [14]. However, they do not provide galvanic isolation. The majority of the non-isolated converters can achieve dc-dc conversion without an intermediary ac stage. This is the case of the dc-MMC, or M2dc [15], [16]. The dc-MMC is presented as a promising solution because of its similarity with the ac-dc MMC [17]. Compared to the MMC, the dc-MMC has the output ac ports connected together through an ac filter (Z_{out} in Fig. 1), but the general structure remains the same. The dc-MMC has been compared with the F2F-MMC in [14], [18], concluding that the dc-MMC is an attractive solution for low voltage ratio applications.

The monopolar dc-MMC [5], [19]–[21] is presented in Fig. 1. This converter allows interconnecting two monopoles with a common ground terminal. Several studies have been conducted to find the optimal operation point [19], [21]–[23].

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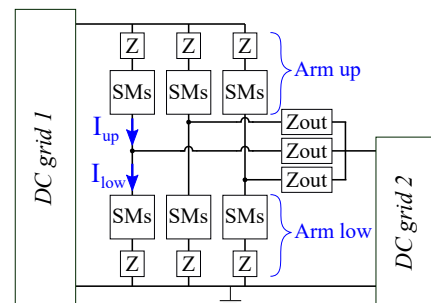
Fig. 1. Monopolar dc-MMC. The ground terminal is common to both sides.

The optimization of the internal ac voltages and the number of SMs is presented in [20]. An optimal design workflow to size the arm inductance and the SMs capacitance is presented in [24], [25]. A control strategy is presented in [22], which reduces the disturbances on the healthy side, by controlling the internal energy during a fault. A dc-MMC with active ac filtering and fault blocking capability is presented in [26]. This topology has drawn the attention of the CIGRE working group B4.76, which has evaluated the converter response in normal operation and faults [5], [27], finding good performances.

The monopolar dc-MMC has been widely studied, but it has a limited range of applications. The converter can be only used for the interconnection between two asymmetric monopoles. The arrangement of two monopolar dc-MMCs (one per pole) was proposed for the bipolar interconnections [28]–[30], but the study of the topology for the interconnections of different line topologies has not been done.

The interconnection between HVDC links with different line topologies represents a potential option for a gradual transition into a multi-terminal dc system (potentially meshed), in Europe [31]. However, only a few publications have proposed dc-dc converters to interconnect different line topologies. The state of the art solution for the interconnection of two HVDC systems with different line topologies is the F2F-MMC. F2F with different transformer configurations are presented in [4], [32]. A dc auto-transformer is proposed in [32], but no results were presented. Despite reducing the converter volume with respect to the F2F-MMC, the auto-transformer continues to use voluminous transformers with important dc constraints. A non-isolated converter is presented in [33], but it requires a series connection of high voltage switches, which is difficult to implement.

Based on the dc-MMC presented for the bipolar interconnections [28]–[30], this paper presents a new dc-MMC to interconnect different line topologies. Unlike the converter presented in [28]–[30], this alternative converter, here called flexible dc-MMC, does not have a common ground terminal between dc sides. Without the ground terminal, the restriction to interconnect exclusively two bipoles or asymmetric monopoles is avoided. In contrast, the grounding strategy needs to be adjusted due to the absence of direct connection to the ground, which requires insulation coordination that is not addressed in this paper. A new control strategy is proposed allowing the converter to operate in a degraded mode, which has not been explored before. The new converter uses fewer control variables when compared to the control schemes proposed in previous publications [28]–[30].

The different topologies and the degraded mode of a line are explained in Section II. The new flexible dc-MMC is introduced in Section III. A proposed mathematical model is presented in Section III-A with the steady state analysis in Section III-B and ac references in Section III-C. The control strategy (with a new change of variables) and simulation results are presented in Sections IV and V respectively. Finally, conclusions are given in Section VI.
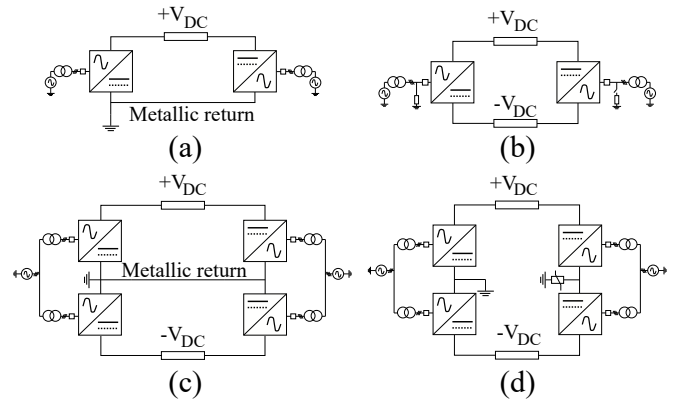

Fig. 2. Line topologies identified in current HVDC links. (a) asymmetric monopole, (b) symmetric monopole, (c) bipole and (d) rigid bipole.

II. HVDC LINE TOPOLOGIES AND DEGRADED MODE

The HVDC line topologies are the different possible configurations of the dc system. They can vary according to the number of conductors, grounding point, redundancy, and voltage rating. Four line topologies have been identified from the already installed HVDC links around the world and presented in Fig. 2.

- Asymmetric monopole (AM), has a single high voltage (HV) conductor (cable or overhead line). The return can be done through the ground or a metallic return with low voltage isolation, but full current capability. The AM has a dc reference point as presented in Fig. 2a.
- Symmetric monopole (SyM) is presented in Fig. 2b. This line topology uses two HV conductors whose voltages are symmetrically distributed to the ground. The SyM does not have a dc reference point, it is normally given by the grounding strategy on the ac side. In case of a fault in a conductor or converter, the power transmission is stopped until the fault is cleared. A pole-to-ground fault creates a pole displacement and the healthy pole may have an increased voltage, up to 2 p.u.
- Bipole (B), is composed of two AM as shown in Fig. 2c. A single metallic return is used to link both substations. The metallic return can be changed for ground return if the regulations allow it. The bipole has a natural redundancy, which allows it to continue uninterrupted operation after a fault. Independently of the fault location (on a converter or a conductor), the healthy pole continues to transmit half of the rated power using the metallic return. In normal operation, the current through the metallic return is negligible.
- Rigid bipole (RB) [34], [35] is different to the bipole in that, it does not have a ground/metallic return and is different to the symmetrical monopole in that the RB has a dc reference point and an ac-dc converter per pole (see Fig. 2d). After a fault in a converter, the RB can reconfigure itself to isolate the fault and operate with the healthy conductors. To reconfigure a RB, the power transmission should stop and a switch yard is activated to isolate the faulted converter. After the line reconfiguration, half of the total rated power can be transmitted using the healthy conductors. In contrast, in the case of a fault in

$$V_u + L\frac{d}{dt}i_u + R\,i_u + L_{out}\frac{d}{dt}\left(i_u - i_m\right) + R_{out}\left(i_u - i_m\right) = V_{H1} - V_{L1} \tag{1}$$

$$V_l + L\frac{d}{dt}i_l + R\,i_l + L_{out}\frac{d}{dt}\left(i_l - i_m\right) + R_{out}\left(i_l - i_m\right) = V_{H2} - V_{L2} \tag{2}$$

$$V_m + 2L\frac{d}{dt}i_m + 2R\,i_m - L_{out}\frac{d}{dt}\left(i_u - 2i_m + i_l\right) - R_{out}\left(i_u - 2i_m + i_l\right) = V_{L2} + V_{L1} \tag{3}$$

$$
\begin{bmatrix} L + L_{out} & -L_{out} & 0 \\ -L_{out} & 2\left(L + L_{out}\right) & -L_{out} \\ 0 & -L_{out} & L + L_{out} \end{bmatrix}
\begin{bmatrix} \dot{i}_u \\ \dot{i}_m \\ \dot{i}_l \end{bmatrix} =
$$

$$
\begin{bmatrix} -\left(R + R_{out}\right) & R_{out} & 0 \\ R_{out} & 2\left(R + R_{out}\right) & R_{out} \\ 0 & R_{out} & -\left(R + R_{out}\right) \end{bmatrix}
\begin{bmatrix} i_u \\ i_m \\ i_l \end{bmatrix} -
\begin{bmatrix} V_u \\ V_m \\ V_l \end{bmatrix} +
\begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & -1 \end{bmatrix}
\begin{bmatrix} V_{H1} \\ V_{H2} \\ V_{L1} \\ V_{L2} \end{bmatrix} \tag{4}
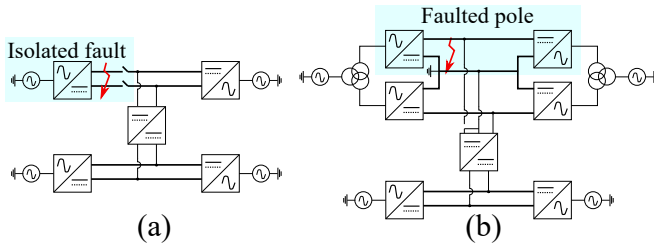$$

Fig. 3. (a) dc system reconfiguration after a fault, without changing the initial line topology seen by the dc-dc converter. (b) A fault in a bipole changes the line topology seen by the converter to an asymmetric monopole.

Fig. 4. Equivalent circuit of the flexible dc-MMC, showing the three loops used for the mathematical model.

a conductor, the complete power transmission capability is lost until the fault is cleared (in overhead lines) or the conductor is repaired (in cable installations). The RB has a reduced redundancy compared to the bipole, but it can be an interesting line topology for offshore applications [34].

In this paper, a post fault scenario is defined as degraded mode if the line topology at the dc-dc converter terminals is changed; for instance, after a fault, a bipole continues to operate as an asymmetric monopole. The case where the dc system is able to reconfigure itself, isolating a fault in a point, does not apply as a degraded mode because the post fault operation does not change the line topology seen by the converter (Fig. 3a). A degraded mode is only possible for the bipole and RB topologies (Fig. 3b).

III. FLEXIBLE DC-MMC

Fig. 4 shows the proposed converter. Unlike the bipolar dc-MMC, the converter studied here is composed of 3 arms per leg. Each arm consists of a series connection of sub-modules (SMs) and an arm inductor. The SMs used can be half bridge (HBSM) or full bridge (FBSM) if the converter needs negative modulation or fault current blocking capability [14], [36]. The arm inductor is needed to reduce the fault current slope and the current variations produced by the switching actions [37]. The output filter (Z_{out}) is an inductor (L_{out}) with an equivalent series resistance R_{out}, having the same functionality of the arm inductor, but it is normally larger than the first one to reduce the ac currents [29]. Fig. 4 shows a three leg converter, but the analysis is valid for n legs ($n > 1$). For a single leg converter, additional capacitors should be added as presented in [38] for the monopolar dc-MMC.
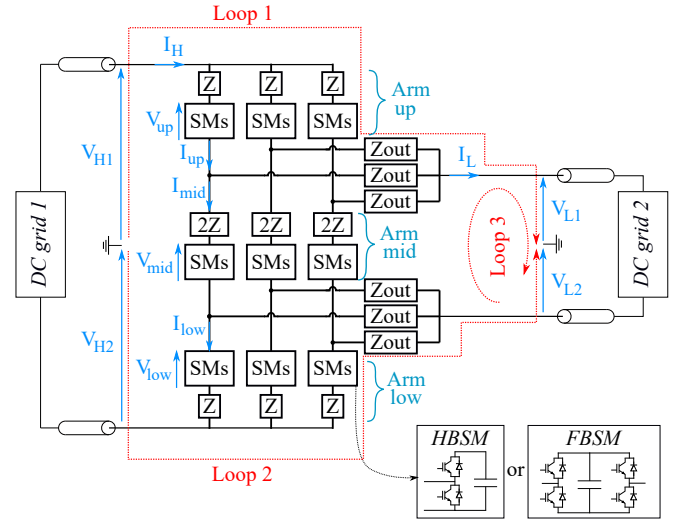
A. Mathematical Model

To analyse the converter, different hypotheses are made.
1) Independent voltage sources model the positive (V_{H1} and V_{L1}) and negative (V_{H2} and V_{L2}) pole-to-ground voltages of the dc grids.
2) The pole-to-ground voltages are assumed to be balanced in steady state operation, i.e., the positive and negative pole voltages have equal magnitudes.
3) The converter is assumed to have a balanced n-phase ac system, and only the first harmonic is considered.
4) A large number of SMs are installed on each arm allowing to create ac voltages with low harmonic distortion.
5) An ideal balancing voltage algorithm is assumed, i.e., the average SM voltage remains unchanged.

Considering the first and second assumptions, the proposed model has the flexibility to adapt to different line topologies, which has not been explored before. For example, the interconnections of a AM need to set a voltage pole to zero, but the model does not change. A similar approach can be followed for a fault in a pole; for instance, a fault in the positive pole of the dc grid 1 is equivalent to have $V_{H1} = 0$, see Fig. 4.

Based on the three proposed circuit loops shown in Fig. 4 (red dotted lines), (1)-(3) are obtained. Where R and L refer to the arm impedance and R_{out} and L_{out} to the output

impedance. The subscripts u, m, l stand for upper, middle and lower arms variables respectively. The mathematical model in matrix form is presented in (4).

B. Steady state Analysis

To understand the converter operation, a simplified steady state analysis is proposed. As indicated previously, the currents and voltages in the converter are assumed to be sinusoidal. These currents are used to balance the energy inside the converter [21], [22], [29]. Additional dc offsets are used to exchange power between dc sides. The arm currents and voltages in steady state are expressed with the following equations, where $i \in u, m, l$.

$$V_i = V_i^{DC} + V_i^{AC} \cdot \cos(\omega t + \phi_{Vi}) \quad (5)$$

$$I_i = I_i^{DC} + I_i^{AC} \cdot \cos(\omega t + \phi_{Ii}) \quad (6)$$

Using the circuit presented in Fig. 4 and neglecting the voltage drop on the resistances, the following expressions present the dc approximate steady state per arm:

$$V_u^{DC} \approx V_{H1} - V_{L1} \quad (7)$$

$$V_m^{DC} \approx V_{L1} + V_{L2} \quad (8)$$

$$V_l^{DC} \approx V_{H2} - V_{L2} \quad (9)$$

$$I_u^{DC} \approx \frac{I_H}{N_{legs}} \approx \frac{P_{DC}}{V_{H1} + V_{H2}} \frac{1}{N_{legs}} \quad (10)$$

$$I_m^{DC} \approx \frac{I_H - I_L}{N_{legs}} \approx \left(\frac{1}{V_{H1} + V_{H2}} - \frac{1}{V_{L1} + V_{L2}} \right) \frac{P_{DC}}{N_{legs}} \quad (11)$$

$$I_l^{DC} \approx \frac{I_H}{N_{legs}} \approx \frac{P_{DC}}{V_{H1} + V_{H2}} \frac{1}{N_{legs}} \quad (12)$$

where N_{legs} is the number of legs. I_H and I_L are the currents on the dc grid 1 and 2 respectively.

It can be noted that the upper and lower dc currents have the same, estimated, value. This means that the dc current through the ground, between dc systems (i.e., $I_u^{DC} - I_l^{DC}$), is zero. A current through the ground could represent an unbalance between poles in one or both dc sides.

To achieve the energy equilibrium, an ac power should circulate in the converter such that the total power being exchanged on each arm is zero (i.e., $P_{DC} + P_{AC} = 0$). Without the ac power, the capacitors in the arm might charge or discharge depending on the power transmitted between the dc systems. The active power balance per arm is estimated from (7)-(12), as follows:

$$P_u^{AC} = -P_u^{DC} = -\frac{V_{H1} - V_{L1}}{V_{H1} + V_{H2}} \frac{P_{DC}}{N_{legs}} \quad (13)$$

$$P_m^{AC} = -P_m^{DC} = -\left(\frac{V_{L1} + V_{L2}}{V_{H1} + V_{H2}} - 1 \right) \frac{P_{DC}}{N_{legs}} \quad (14)$$

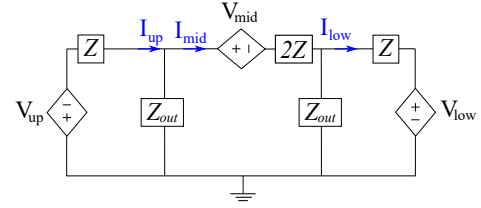$$P_l^{AC} = -P_l^{DC} = -\frac{V_{H2} - V_{L2}}{V_{H1} + V_{H2}} \frac{P_{DC}}{N_{legs}} \quad (15)$$

Fig. 5. Equivalent ac circuit for the flexible dc-MMC.

C. Ac operation reference

As discussed above, the converter operation requires an ac power to keep the internal energy balanced. The magnitude of the ac active power can be found based on the estimated dc power, but the ac arm voltages magnitudes and phases have to be defined. Fig. 5 shows the equivalent ac circuit per leg for the proposed converter. It can be noted that the arms are not connected in series nor parallel. In consequence, the power exchange between two arms cannot be set without affecting the third one. Based on the dc voltages of the lines and the rated power of the converter, the ac operation point is obtained by formulating an optimization problem. The objective of the optimization problem is the reduction of the conduction losses by the arm currents minimization. The currents in the output filters are not included in the objective function, as these branches have lower losses compared to the arms.

Before presenting the objective function, the following notation is defined for the phasor representation differentiating the polar and rectangular form:

$$\underline{X}_i = X_i \angle \theta = X_i^d + j X_i^q \quad (16)$$

where X is either an ac current or voltage for $i \in u, m, l$. Using this notation, and reminding that only the first harmonic is used, the RMS arm currents can be expressed as follows.

$$I_i^{RMS} = \sqrt{\frac{I_i^{AC^2}}{2} + I_i^{DC^2}} \quad (17)$$

The objective function used in this study is presented below.

$$\min f(x) = N_{sm_u} \cdot I_u^{RMS^2} + N_{sm_m} \cdot I_m^{RMS^2} + N_{sm_l} \cdot I_l^{RMS^2} \quad (18)$$

where N_{sm_i} is a weight factor that prioritises the arm with greater number of installed switches. N_{sm_i} is the sum of HBSMs plus twice the number of FBSMs per arm.

The problem variables are collected in x as follows:

$$x^T = \left[V_u^d, V_u^q, V_m, V_l^d, V_l^q, I_u^d, I_u^q, I_m^d, I_m^q, I_l^d, I_l^q \right] \quad (19)$$

where the middle arm voltage ($\underline{V_m}$) is the reference for all ac variables (i.e., $V_m{}^q = \theta_{Vm} = 0$).

The optimisation problem is subject to the following equality constraints:

$$\Re \left(Loop_{1,2,3}^{AC} \right) = 0$$
$$\Im \left(Loop_{1,2,3}^{AC} \right) = 0 \quad (20)$$
$$P_i^{DC} + P_i^{AC} = 0$$

The first two sets of constraints come from the circuit equations, (1)-(3), in phasor domain. Separating the equations in their d and q components as presented in (16), leads to

$$\begin{bmatrix} \dot{I}_1 \\ \dot{I}_2 \\ \dot{I}_3 \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R+R_{out}}{L+L_{out}} & 0 \\ 0 & 0 & -\frac{R+2R_{out}}{L+2L_{out}} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{1}{L+L_{out}} & 0 \\ 0 & 0 & -\frac{1}{L+2L_{out}} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{4L} & \frac{1}{4L} & 0 & 0 \\ \frac{-1}{2(L+L_{out})} & \frac{-1}{2(L+L_{out})} & \frac{-1}{2(L+L_{out})} & \frac{1}{2(L+L_{out})} \\ \frac{1}{4(L+2L_{out})} & \frac{1}{4(L+2L_{out})} & \frac{-1}{2(L+2L_{out})} & \frac{-1}{2(L+2L_{out})} \end{bmatrix} \begin{bmatrix} V_{H1} \\ V_{H2} \\ V_{L1} \\ V_{L2} \end{bmatrix} \tag{26}$$

6 initial equality constraints. The third set of constraints is the condition for the energy balance presented in (13)-(15). Adding the 3 power constraints, a total of 9 equality constraints are obtained. Then, 6 additional inequality constrains are added to limit the results within the semiconductors physical limits (rated current) and maximal voltage allowed (number of installed SMs), expressed as:

$$I_i^{RMS} \le I_{rated}$$
$$V_i^{DC} + V_i \le V_{max} \tag{21}$$

The current limit (I_{rated}) depends on the valve used. In this paper, an IGBT 3.3 kV 1.5 kA is considered. The maximal number of SMs (V_{max}) can be set manually, but if fault block capability is required a minimum number of FBSMs are needed. This number depends on the line topologies, the type of fault considered, and the rated voltages of the dc lines to interconnect.

The optimization problem is solved computationally, using $fmincon$ function in Matlab as non-linear restrictions are needed. The results for the arm currents angles found for a case study are shown in Section V.

IV. CONTROL STRUCTURE

A proposed control strategy is presented in this section. It is composed of two cascaded stages. The first stage controls the energy of the converter (high level). The lower level controls the current dynamics. The assumptions, tuning, and analysis are presented in the following subsections.

A. System Diagonalization

To simplify the current control, a system diagonalization through a change of variables is proposed. The variable transformations are as follows:

$$\boldsymbol{I_{uml}} = \boldsymbol{P}\,\boldsymbol{I_{123}}; \qquad \boldsymbol{I_{123}} = \boldsymbol{P^{-1}}\,\boldsymbol{I_{uml}} \tag{22}$$

$$\boldsymbol{V_{uml}} = \boldsymbol{T}\,\boldsymbol{V_{123}}; \qquad \boldsymbol{V_{123}} = \boldsymbol{T^{-1}}\,\boldsymbol{V_{uml}} \tag{23}$$

where uml refers to the currents and voltages in the upper, middle, and lower arms, and 123 refers to the new currents and voltages variables after the transformations. The transformation matrices are detailed below:

$$\boldsymbol{P} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & -1 \\ 1 & -1 & 1 \end{bmatrix}; \boldsymbol{P^{-1}} = \begin{bmatrix} 1/4 & 1/2 & 1/4 \\ 1/2 & 0 & -1/2 \\ 1/4 & -1/2 & 1/4 \end{bmatrix} \tag{24}$$

$$\boldsymbol{T} = \begin{bmatrix} 1 & 1 & 1 \\ 2 & 0 & -2 \\ 1 & -1 & 1 \end{bmatrix}; \boldsymbol{T^{-1}} = \begin{bmatrix} 1/4 & 1/4 & 1/4 \\ 1/2 & 0 & -1/2 \\ 1/4 & -1/4 & 1/4 \end{bmatrix} \tag{25}$$

The diagonalization allows the decoupling of the current and voltage variables. The decoupling can be evidenced in (26)

where a current only depends on one voltage; for instance, the new current I_1 only depends on voltage V_1, which is not the case for the initial system presented in (4). The decoupled variables simplify the design of the current controllers. The new current variables can be used to control the internal energy and the power exchange between dc systems. The variables in 123 frame have dc and ac components as the initial variables uml. I_1 is an equivalent current that goes through the complete converter from the dc grid 1. I_2 links the upper and lower arm without affecting the middle one. I_2^{DC} is the current through the ground that links both dc systems and it is controlled to zero. I_3 traverses an equivalent circuit seen from the dc grid 2. I_3^{DC} is proportional to I_L and is used to control the power exchange.

B. Energy controllers

The energy controllers have a constant reference, and they are designed to keep the energy constant during power transients. These controllers provide the dc and ac references of the internal current controllers. The energy is controlled per leg; therefore, the proposed control can be extended to n legs. The energy is controlled on the basis of variables 123. The general energy control structure is presented in Fig. 6 where $N(s)$ are two notch filters in series, which are used to avoid first and second harmonic oscillations. The filter transfer function is:

$$N(s) = \frac{s^2 + \omega_n^2}{s^2 + 2\omega_n s/Q + \omega_n^2} \cdot \frac{s^2 + 4\omega_n^2}{s^2 + 4\omega_n s/Q + 4\omega_n^2} \tag{27}$$

where ω_n is the operation frequency of the converter and Q is the quality factor, set to 3 [22], [39]. The energy controllers are proportional-integral (PI) with the following structure:

$$G_{PI}(s) = K_{pW} + \frac{K_{iW}}{s} \tag{28}$$

The closed loop response is designed to have a second order system response with the general structure as follows:

$$G_{CL}(s) = \frac{1}{s^2 + 2\zeta\omega_{nW} + \omega_{nW}^2} \tag{29}$$

where the damping factor is $\zeta = 0.7$ and the natural frequency ω_{nW} is:

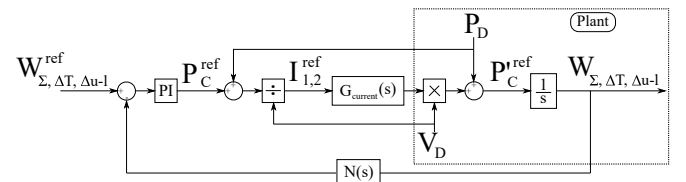$$\omega_{nW} = \frac{1}{\tau_{energy}} \tag{30}$$

Fig. 6. General structure for the energy controllers ($W_{\Sigma T}$, $W_{\Delta T}$ and $W_{\Delta u-l}$).

where τ_{energy} is chosen to be a factor ($K_W = 7$) of the notch time constant, as follows:

$$\tau_{energy} = K_W \cdot \tau_{Notch} \; ; \quad \tau_{Notch} = \frac{Q}{\omega_{nW}} \tag{31}$$

As the filter $N(s)$ is the same for all loops, the gains are the same for all energy controllers:

$$K_{iW} = \omega_{nW}^2 \; ; \quad K_{pW} = 2\zeta\sqrt{K_{iW}} \tag{32}$$

C. Current references

This section explains in detail how the energy controllers set the reference for the current controllers. Three energy controllers, which are a linear combination of the arm energies, are proposed in this paper. In particular, the total energy W_Σ, the total difference $W_{\Delta T}$ and the difference between the upper and lower arm $W_{\Delta u-l}$.

Based on Fig. 6, a general expression can be found for the current references:

$$I^{ref} = \frac{P_C^{ref} + P_{FF}^{DC} + P_{FF}^{AC}}{V_D} \tag{33}$$

where the current reference I_{ref} depends on an equivalent voltage V_D, a power disturbance P_D and the output of the energy controller P_C^{ref}. The power disturbance P_D can be decomposed in a dc power feedforward P_{FF}^{DC} and an ac power feedforward P_{FF}^{AC}. P_C^{ref} depends on the energy controller, either on $\dot{W}_\Sigma$, $\dot{W}_{\Delta T}$ or $\dot{W}_{\Delta u-l}$. The current references are detailed below.

1) W_Σ controller: The total energy (W_Σ) is the sum of the three arms energy:

$$W_\Sigma = W_u + W_m + W_l \tag{34}$$

The energy dynamic can be expressed in terms of the individual arm powers:

$$\dot{W}_\Sigma = P_u + P_m + P_l \tag{35}$$

By changing the powers in terms of the new variables $1, 2, 3$ and simplifying, the following expression is obtained:

$$\dot{W}_\Sigma = 4V_1 I_1 + 2V_2 I_2 + 4V_3 I_3 \tag{36}$$

The energy controller regulates the variations of the energy thanks to the measurement of the average power exchange in the arms. To employ (36) in the energy controller design, the average value of the expression is needed. As previously stated, the variables on frame 123 have dc and ac components, therefore, the expression (36) can be also analyzed in ac and dc components.

The average value of a product between two variables, with ac (only first harmonic) and dc components, can be calculated with the following expression:

$$\overline{V_j \cdot I_k} = |V_j^{AC}||I_k^{AC}|\frac{cos(\theta_{Vj} - \theta_{Ik})}{2} + V_j^{DC}I_k^{DC} \tag{37}$$

where V_j is a voltage and I_k is a current, for $j,k \in 1,2,3$.

Analyzing (26), it can be concluded that the voltages V_j^{AC} and the currents I_k^{AC} (for $j = k$) have an angle difference of $\pi/2$, if the voltage drop on the resistances is neglected

(pure inductive circuits). Consequently, the average value of the product $V_j^{AC}I_j^{AC}$ is zero, as $cos(\theta_{Vj} - \theta_{Ij}) = 0$. Following this analysis, the expression (36) does not have ac average value, hence, the $\dot{W}_\Sigma$ cannot be controlled with ac components. Furthermore, the total converter energy needs to be balanced with an external source of energy. The non-isolated dc-dc converter interconnecting two dc systems can only exchange power through dc currents.

Regarding the dc components, the expression (36) allows to control the total energy with any dc component I_{123}^{DC}. In this case the current I_1^{DC} is considered because this current links the dc grid 1 with the three arms in the converter. Combining (36) with (7)-(12) and applying the variable transformations (22) and (23), the following expression is obtained:

$$I_1^{DC} = \frac{P_C^\Sigma + (1 - \frac{V_{H1}+V_{H2}}{2(V_{L1}+V_{L2})})\frac{P_{DC}}{N_{legs}}}{V_{H1} + V_{H2}} \tag{38}$$

2) $W_{\Delta T}$ controller: This controller regulates the difference between the middle arm energy and the equivalent energy of the upper and lower arms. Following the same procedure used for (36), the $W_{\Delta T}$ energy dynamics is:

$$\dot{W}_{\Delta T} = P_u - P_m + P_l \tag{39}$$

$$\dot{W}_{\Delta T} = 4V_1 I_3 + 2V_2 I_2 + 4V_3 I_1 \tag{40}$$

In this case, the cross products of ac components have a non-null average value. Expression (40) allows to control the $W_{\Delta T}$ energy using either I_1^{AC}, I_3^{AC} or any I_{123}^{DC} currents, but the I_1^{AC} current is used in this paper. Applying the same process used to obtain (38), the expression (43) is obtained. In this case, only the magnitude of the current I_1^{AC} is controlled, the angle depends on the dc-dc converter power reference. This angle is set from a lookup table created from the results obtained in the optimization process (Section III-C).

3) $W_{\Delta u-l}$ controller: This control regulates the energy difference between the upper and lower arm. The dynamic of this energy is expressed as follows:

$$\dot{W}_{\Delta u-l} = P_u - P_l \tag{41}$$

$$\dot{W}_{\Delta u-l} = 2I_2(V_1 + V_3) + 2V_2(I_1 + I_3) \tag{42}$$

In this case, I_2^{AC} is used to regulate the $W_{\Delta u-l}$ energy. Similar to the previous subsection, the magnitude of I_2^{AC} is obtained from the average value of (42), which results in expression shown in (44). The angle for I_2^{AC} is set with a lookup table.

4) Other current references: As mentioned in Subsection IV-A the reference for the current I_2^{DC} is zero to avoid unbalanced poles. In case of voltage unbalances, a small value of I_2^{DC} can be used to re-balance the poles on the SyM side. The current I_3^{DC} is used to control the power on the dc grid 2 (Fig. 4). The reference for I_3^{AC} is set directly from the optimization results using a lookup table (magnitude and angle). The summary of the currents and their control use can be found in Table I.

D. Current control

The current controllers are tuned using the decoupled system presented in (26). The controllers are proportional-integral-resonant (PIR), which are able to follow the dc and ac

$$|I_1^{AC}| = \frac{P_C^{\Delta T} + \left(\frac{V_{L1}+V_{L2}}{V_{H1}+V_{H2}} - 1\right)\frac{P_{DC}}{N_{legs}} - 2|V_1^{AC}||I_3^{AC}|cos(\theta_{V1} - \theta_{I3})}{2|V_3^{AC}|cos(\theta_{V3} - \theta_{I1})} \tag{43}$$

$$|I_2^{AC}| = \frac{P_C^{\Delta u-l} - \frac{V_{H1}-V_{H2}-V_{L1}+V_{L2}}{V_{H1}+V_{H2}}\frac{P_{DC}}{N_{legs}} - |V_2^{AC}|(|I_1^{AC}|cos(\theta_{V2} - \theta_{I1}) + |I_3^{AC}|cos(\theta_{V2} - \theta_{I3}))}{|V_1^{AC}|cos(\theta_{V1} - \theta_{I2}) + |V_3^{AC}|cos(\theta_{V3} - \theta_{I2})} \tag{44}$$
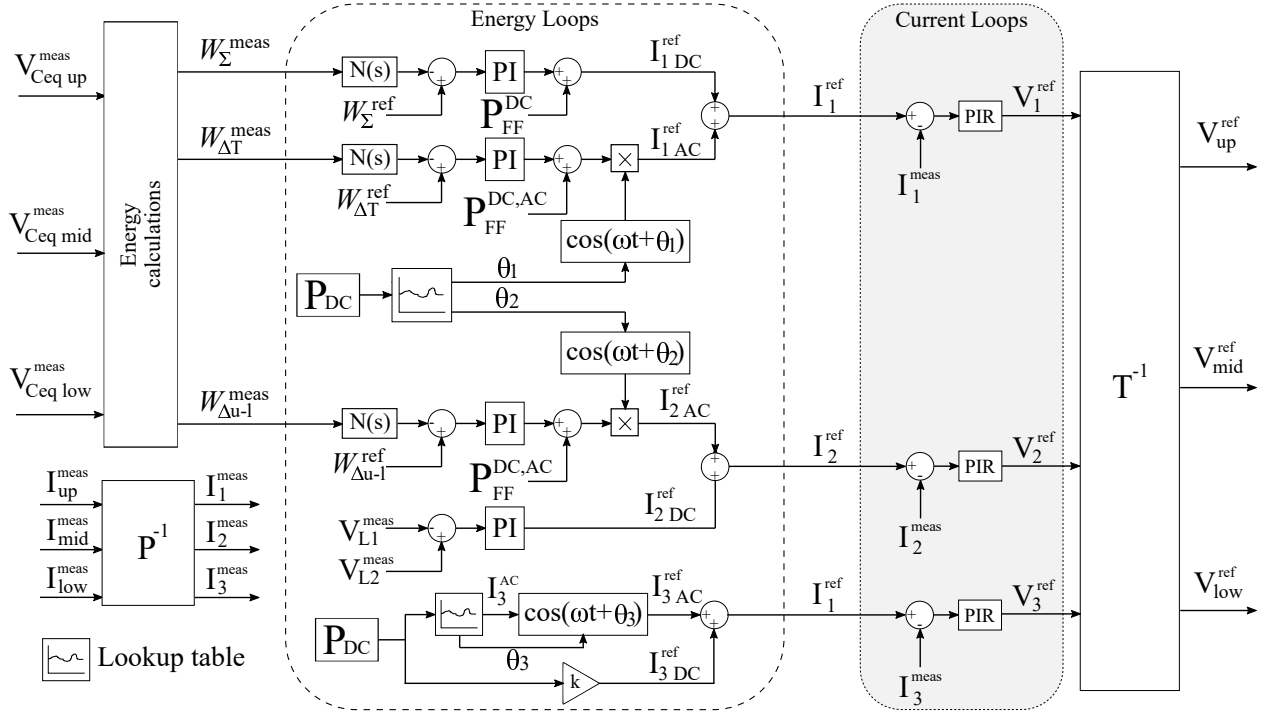
Fig. 7. Control strategy implemented. All variables are vectors with a length equal to the number of legs (N_{legs}). The lookup tables set the ac angles obtained from the optimization process. $N(s)$ is a notch filter for the first and second harmonic and P_{FF} are the ac and dc power feed-forward for the energy controllers.

references. The model and tuning of these controllers are based on the strategy proposed in [40]. The PIR transfer function is:

$$G_{PIR}(s) = K_{PIR}\frac{(s + \alpha_{PIR})^3}{s(s^2 + w_r^2)} \tag{45}$$

where the term ω_r is the resonant frequency set equal to the frequency of ac currents and voltages. K_{PIR} is the controller gain, which depends on the equivalent circuit of each current (I_{123}). It is calculated as:

$$K_{PIR} = \frac{(\omega_c^2 - \omega_r^2)\sqrt{\omega_c^2 L_{eq123}^2 + R_{eq123}^2}}{\omega_c} \tag{46}$$

where ω_c is the crossover frequency, with the desired phase margin (φ_{PM}) and the time delay T_d as follows:

$$\omega_c = \frac{\pi/2 - \varphi_{PM}}{T_d} \tag{47}$$

and α_{PIR} can be calculated with:

$$\alpha_{PIR} = \frac{\omega_c}{10} \tag{48}$$

The equivalent inductance and resistance, extracted from (26) are:

$$L_{eq1} = L; \quad R_{eq1} = R \tag{49}$$

$$L_{eq2} = L + L_{out}; \quad R_{eq2} = R + R_{out} \tag{50}$$

$$L_{eq3} = L + 2L_{out}; \quad R_{eq3} = R + 2R_{out} \tag{51}$$

The complete control strategy including the energy and current controllers is presented in Fig. 7. This control strategy does not change between normal and degraded operation, only the references from the optimization process change (i.e., the lookup tables).

TABLE I
CURRENTS AND THEIR USE

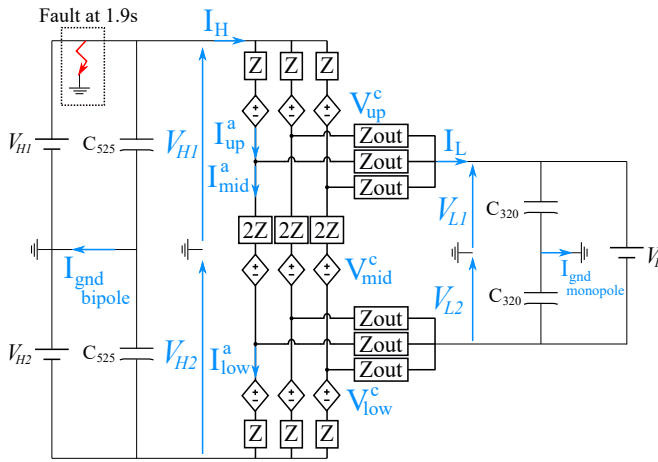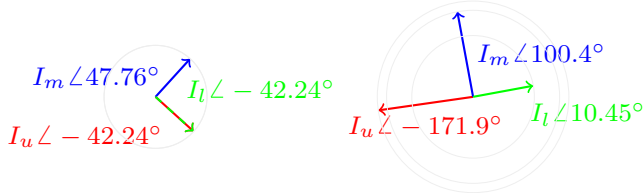| Current	Control use
I_1^{DC}	Energy sum total ($E_{\Sigma T}$)
I_1^{AC}	Energy diff total ($E_{\Delta T}$)
I_2^{DC}	Pole balancing, ground current
I_2^{AC}	Energy u-l ($E_{\Delta u-l}$)
I_3^{DC}	Power reference
I_3^{AC}	Optimised reference

Fig. 8. Simulated model.

Fig. 9. Optimised ac current vectors in normal operation (left) and degraded mode (right). The upper and lower currents in normal operation are identical.

V. SIMULATION AND RESULTS

To validate the proposed converter with the control strategy, a case study is simulated. The case study is inspired by the proposed interconnection between COBRA Cable and NordLink HVDC lines [31]. The high voltage side, NordLink, is a rigid bipole ±525kV rated at 1400MW. The low voltage side, COBRA cable, is a symmetric monopole ±320kV rated at 700MW. The rated power of the dc-dc converter is 700MW and it is designed to stop dc faults (additional FBSMs are used). Average arm models for HBSM [41] and FBSM [42], are used to simulate the converter. The dc sides are modeled with ideal voltage sources and the cable equivalent capacitance. A voltage source per pole on the bipole and a voltage source pole-to-pole on the symmetric monopole side, as shown in Fig. 8. Additional details of the simulated model can be found in Table II. The current controllers were tuned with a phase margin of 60 deg, a sampling time of 40 μs, and a resonance frequency of $2\pi150$ rad/s. The angles of the currents are shown in Fig. 9, for normal operation and degraded mode.

The simulation is divided into three stages, the normal operation ($t < 1.9s$), a fault pole to ground on the RB side ($t = 1.9s$) and the degraded mode ($t > 2.1s$).

TABLE II
DC-DC PARAMETERS

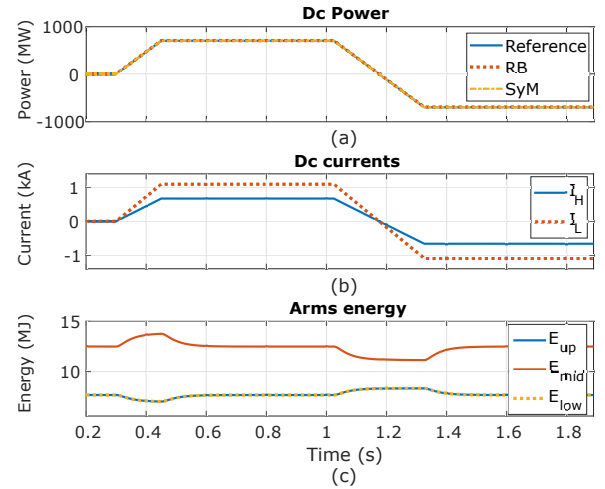| Parameters	Value
V_{H1} and V_{H2}	525 kV
V_{L1} and V_{L2}	320 kV
Frequency	150 Hz
Arm inductance	15 mH
Output inductance	150 mH
Number of SMs upper and lower arm	400 FBSM
Number of SMs middle arm	650 HBSM
Capacitance per SM	5 mF
C525 (311.5 km)	42.4 μF
C320 (162.5 km)	21.3 μF

Fig. 10. Simulation results for the dc-dc converter in normal operation, exchanging power in both directions.
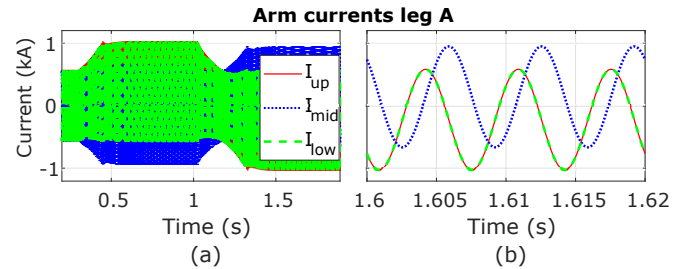

Fig. 11. Arm currents of leg A with (a) the complete normal operation and (b) a zoom between 1.6s and 1.62s

A. Normal operation

Fig. 10 shows the simulation results for the normal operation mode. The dc power exchanged through the flexible dc-MMC (700 MW) is presented in Fig. 10a. The dc currents on the RB (I_H) and the SyM (I_L) are shown in Fig. 10b. The average energy variations per arm are presented in Fig. 10c. Since the dc systems are modeled as ideal dc voltage sources, the dc voltages do not present variations and they are not represented.

Fig. 11 presents the arm currents of one leg. In Fig. 11b it is observed that the arm currents follow the phase found in the optimization process (see Fig. 9a), i.e., the upper and lower currents are in phase and the middle current is $\pi/2$ ahead of the firsts. During the change of power direction through the dc-dc converter, for $1s < t < 1.3s$, the arm currents change their dc offset, following the change of polarity.

B. Fault

With regard to the fault simulation, a basic fault detection algorithm has been implemented. It uses local measurements to detect over-currents, over-voltages, or under-voltages. In this paper, an over-current threshold is set to 3 kA for the arm currents. The thresholds for the dc grid voltage variations are set to be ±20%. If the dc-dc converter measures currents and/or voltages outside of the defined operation range, a blocking signal is sent to all the arms. The total time to stop the dc fault currents depends on: the dc systems interconnected; the fault detection algorithm; the detection delays; the protection strategy and the size of the FBSMs capacitors, which are beyond the scope of this paper. A simplified fault simulation
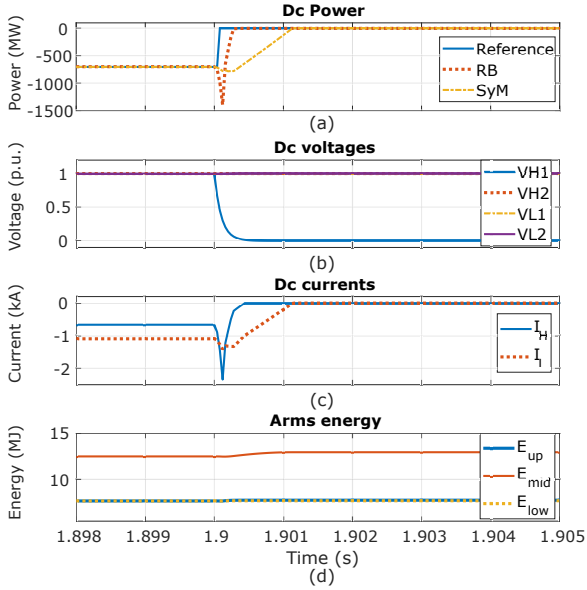
Fig. 12. Simulation results during a fault on the positive pole of the rigid bipole.
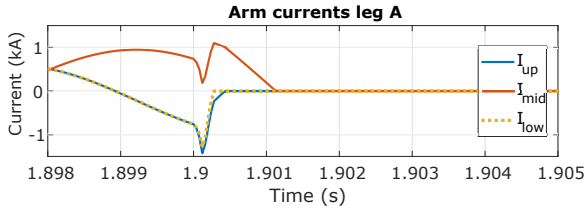

Fig. 13. Arm currents during the fault.

Fig. 14. Simulation results in degraded mode.

Fig. 15. Arm currents in degraded mode.

is presented in this paper, where the fault is emulated with $V_{H1} = 0$.

Fig. 12 presents the simulation results during a fault on the RB. The fault is located at the positive pole as shown in Fig. 8. For this scenario, a blocking signal is triggered by the voltage variation on the faulted pole (V_{H1}). The dc-dc converter using FBSMs is able to stop the faults without the use of additional dc circuit breakers (DCCBs). The arm currents of one leg are presented in Fig 13, which are representative of the response for the other two legs.

C. Degraded operation

As previously stated, to isolate a fault the power transmission must be stopped and a switch yard is used to reconfigure the line. To emulate the reconfiguration time, the converter remains blocked until $t = 2.1 s$. Fig. 14 presents the simulation after the fault in the RB line. The degraded mode simulated here represents the interconnection between an AM ($-525 \, kV$) and a SyM ($\pm 320 \, kV$). In this case, only 350 MW are exchanged between the dc systems (Fig. 14a). A small deviation in the monopole voltages (V_{L1}, V_{L2}) can be observed at $t < 2.2 s$ in Fig. 14b. The voltage disturbance comes from the fault previously simulated, but the voltage control allows them to return to their reference value. It should be noted that the voltage V_{H1} is not presented in Fig. 14 as it is zero. As expected, the SyM dc current shown in Fig. 14c is half of the normal operation current (Fig. 10b), but the current I_H remains unchanged.

The arm currents in the degraded mode have higher magnitudes compared to the currents in normal operation (Fig. 15).
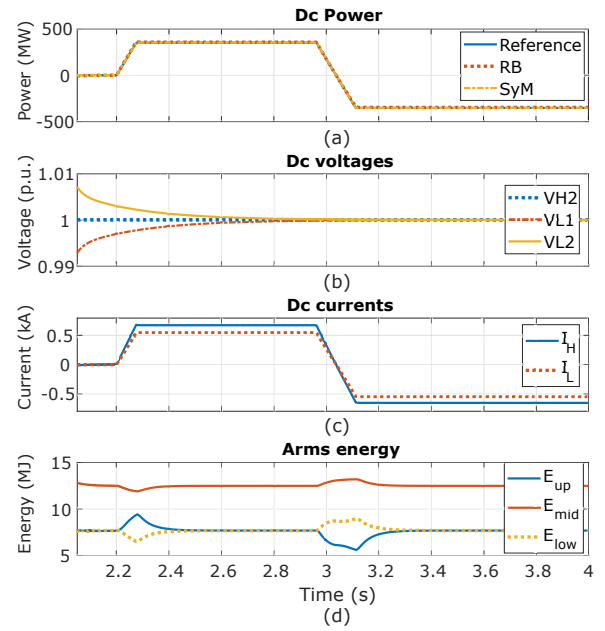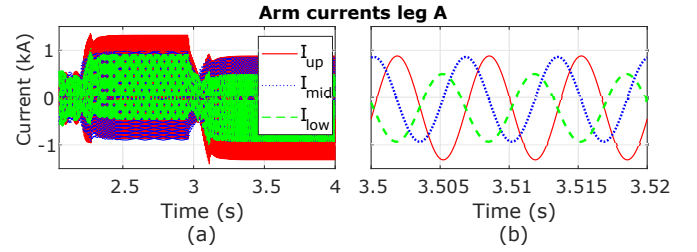
This leads to higher energy variations, shown in Fig. 14d. These variations can be reduced if the power reference slope is reduced or if the size of the capacitors in the upper arm is increased. The current phases in Fig. 15b follow the references found in the optimization process, presented in Fig. 9b. The change of power polarity is more evident in the arm voltages (see Fig. 16). Indeed, the currents and voltages polarities are inverted when the power flow through the dc-dc converter changes of direction ($t \approx 3 s$).

VI. CONCLUSION

This publication presents a new flexible dc-MMC for interconnections between HVDC links of different line topologies. The converter is a variation of the well-known dc-MMC (or M2dc). The converter is able to interconnect symmetrical monopole (SyM), asymmetrical monopole (AM), and rigid bipole (RB) configurations. The converter operating principle is explained showing that dc currents are needed to exchange
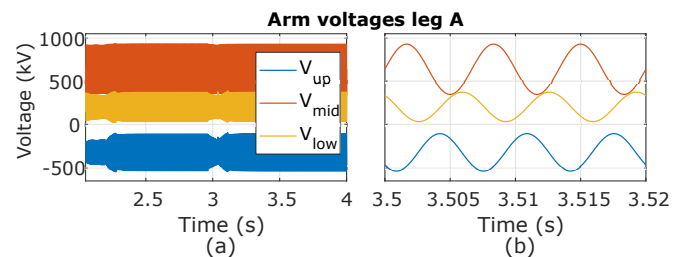

Fig. 16. Arm voltages in degraded mode.

power between the interconnected systems and ac currents are employed to balance the internal energy. An optimization problem, to reduce the conduction losses in the arms, is proposed and solved to set the ac references. The converter mathematical model is analyzed with a new variable transformation. The transformation allows to control the complete converter with three equivalent currents: I_1, I_2 and I_3. The proposed control structure allows the flexible dc-MMC to operate interconnecting the line topologies mentioned above. The control is validated with a case study inspired in a possible real application, the interconnection between the NordLink and COBRA Cable projects. Two main scenarios were validated with simulations, the normal operation and the degraded mode where a pole in the rigid bipole line is isolated. These scenarios validated the interconnections RB-SyM and AM-SyM. Further studies should be carried out to optimize the sizing of the converter components. The protection and grounding strategy should be investigated in future studies. Experimental implementation can be done to validate the control in real applications.

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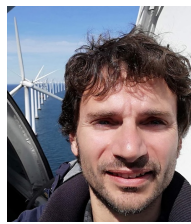
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