Transient currents in HfO_2 and their impact on circuit and memory applications

C. Monzio Compagnoni[a], A. S. Spinelli[a], A. Bianchini[a], A. L. Lacaita[a,b], S. Spiga[c] and M. Fanciulli[c]

[a] Dipartimento di Elettronica e Informazione, Politecnico di Milano–IU.NET, piazza L. da Vinci 32, 20133 Milano, Italy
[b] IFN-CNR, Milano, Italy, [c] Laboratorio Nazionale MDM-CNR-INFM, via C. Olivetti 2, 20041 Agrate Brianza, Italy

ABSTRACT

We investigate transient currents in HfO_2 dielectrics, considering their dependence on electric field, temperature and gate stack composition. We show that transient currents remain an issue even at very low temperatures and irrespective of the HfO_2/SiO_2 bilayer properties. Finally, we assess their impact on the reliability of precision circuit and memory applications.

INTRODUCTION

HfO_2 and its silicates are considered candidates to replace SiO_2 in future microelectronics technology nodes [1], thanks to the reduction in the static leakage current, achieved via a larger physical thickness at the same equivalent oxide thickness (EOT). On the other hand, HfO_2 suffers from large transient currents, which may affect the functionality of several integrated circuits (ICs) [2]. We investigate the dependence of transient currents in HfO_2 on electric field, temperature and gate stack composition, showing that they remain an issue even at very low temperatures and irrespective of the HfO_2/SiO_2 bilayer properties. We assess the impact of transient currents on the reliability of precision circuit and memory applications, showing that reducing their magnitude is a fundamental step for integration of high-k materials in advanced ICs.

EXPERIMENTAL

Table I shows the samples used in this work: p- and n-type, $2-5\ \Omega$ cm Si (100) wafers were used as substrates. HfO_2 films were deposited by ALD (combining $HfCl_4$ and H_2O at 375°C) with different thickness t_{hk}. For sample D, an SiO_2 layer with thickness t_{ox} was grown by RTO before HfO_2 deposition, whereas in samples A, B and C an ultra-thin interfacial chemical SiO_2 layer was formed over the silicon substrate. From CV analyses including quantum-mechanical (QM) effects, we determined $t_{ox} = 0.87$ nm for these samples and $\epsilon_{hk} \simeq 18$. Samples E and F are RTO SiO_2 reference devices. Al gates were patterned to obtain capacitors with area ranging from 0.16×10^{-4} to 16×10^{-4} cm^2.

Transient currents were investigated according to the following procedure: a *charge* pulse (with amplitude V_G and duration t_{ON}) is applied to the gate of the capacitor, then measuring the gate current J_d flowing after V_G is brought back to zero (*discharge* current) [3]. As reported in Fig. 1 (sample A), such currents are slowly decreasing with time, following a $t^{-1.02}$ power-law dependence, and change with the amplitude of the gate pulse during the charge phase. Dielectric polarization relaxation (DPR) [4] and charge (de)trapping (CDT) [3] are the possible origins of these slowly decreasing currents.

Sample	t_{hk} [nm]	t_{ox} [nm]	EOT [nm]
A	5	0.87	1.97
B	7	0.87	2.41
C	13	0.87	3.73
D	5	1.8	2.90
E	0	1.9	1.9
F	0	3.7	3.7

Table 1: Samples considered in this work. t_{hk} and t_{ox} are the HfO_2 and the SiO_2 thicknesses respectively.

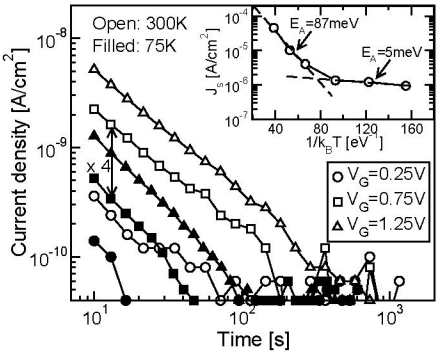

Figure 1: Discharge transients measured at 300 and 75 K on sample A after positive V_G charge. In the inset the stationary gate current J_s (at $V_G = 1$ V) is shown as a function of $1/k_BT$.

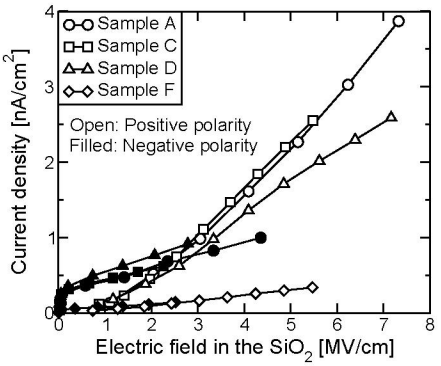

Figure 2: J_d at 20 s as a function of the electric fi eld in the SiO_2 layer during the charge phase. Results for samples with different HfO_2/SiO_2 stack compositions are shown.

TRANSIENT CURRENTS ANALYSIS

Irrespective of the physical mechanism at the origin of transient currents, we are here interested in an assessment of their main dependences, to investigate their impact on circuit reliability. To this aim, we explored the temperature dependence of J_d, comparing results obtained at 300 and 75 K (Fig. 1). A small reduction of J_d is found (by nearly a factor 4), showing that transient effects play a role even at very low temperatures. Moreover, in the inset of Fig. 1 we reported the temperature dependence of the static leakage current flowing through the capacitor when a gate bias of 1 V is applied at the gate, show-

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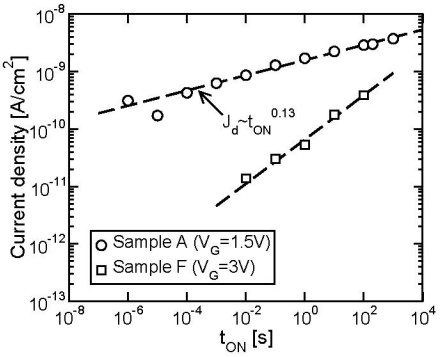

Figure 3: Discharge current at 16 s as a function of the charging time.

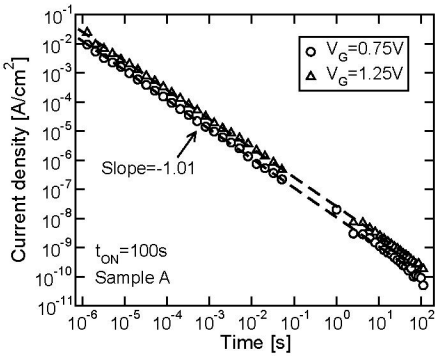

Figure 4: Discharge dynamics at short times after the charge phase.

ing a much larger decrease in the same temperature range and revealing that transient currents do not depend on the stationary current flowing through the dielectric stack. The dependence of J_d on stack composition was also investigated: Fig. 2 shows J_d at a fixed time $t = 20$ s as a function of the field F_c (from CV analyses with QM effects) applied to the SiO_2 layer during the charge phase, for samples A and C (same t_{ox}, different t_{hk}). Data are shown for positive and negative polarities, demonstrating that the gate leakage does not depend on the HfO_2 thickness but only on the applied F_c and its polarity. In Fig. 2, results for sample D are also shown: from the comparison against sample A (different t_{ox}, same t_{hk}) we infer that if the interfacial oxide is optimized (by proper temperature annealings to improve the HfO_2/SiO_2 interface quality), J_d becomes also nearly independent of the stack composition. Further insight is obtained comparing samples A and F (HfO_2 vs. SiO_2): for the same Al gate, J_d is much smaller (8 times) for the SiO_2 sample.

Impact on IC reliability

To investigate the impact of transient effects on circuit and memory applications, we first studied the timescale dependence of transient currents (previously evaluated in the hundreds of seconds range), assessing the dependence of J_d on t_{ON} (Fig. 3): a weak dependence is found ($J_d \simeq t_{ON}^{0.13}$ and $t_{ON}^{0.38}$ for HfO_2 and SiO_2 samples, respectively), demonstrating that even short charging pulses cannot avoid the presence of these currents. In Fig. 4 we show that the $1/t$ time dependence of J_d is still present down to the μs range, with no saturating behavior appearing, meaning that J_d will be an issue even in the short time scale. The effects of these currents were studied on a charge-redistribution ADC, where the voltage at the input of the comparator changes during the conversion phase as a result of the integration of the transient currents on the capacitor plates [5]. In Fig. 5 we assumed that the ADC input voltage is

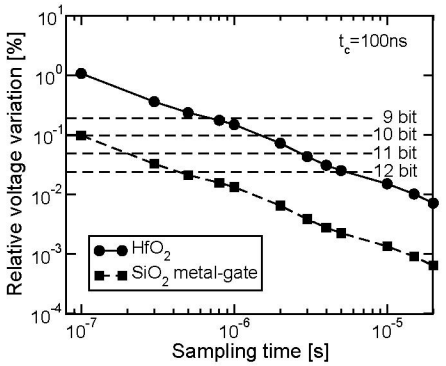

Figure 5: Voltage drift at the input of the comparator in a charge redistribution ADC converting a zero after the input has been kept at full scale for a long time. Dashed lines are the LSB.

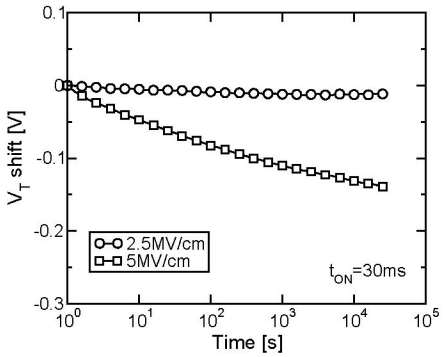

Figure 6: V_T shift during data retention for a Flash memory cell using the HfO_2/SiO_2 bilayer (sample C) as tunnel dielectric. The interpoly thickness was assumed 10 nm with $\alpha_G = 0.6$.

reset to 0 V after it has been kept at a voltage equal to the full-scale range for a long time: the effect at the comparator input is shown as a function of the duration of the sample phase for a conversion time of 100 ns, making clear that HfO_2 dielectrics may strongly affect the accuracy of the conversion process for large bit number and low sampling times. In Fig. 6 we considered the application of HfO_2 in the tunnel dielectric of a Flash memory cell [6]: the drift of the programmed V_T in the time interval from 1 s to 3×10^4 s calculated using data from our samples is shown for different electric fields in the SiO_2 layer during program. The results show that transient effects can give rise to significant instability of cell state during data retention, particularly detrimental in multi-bit storage.

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