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Design and Development of High Voltage High Pulse Power Supply using FPGA for Dynamic Impedance Matching

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ABSTRACT

High Voltage High Pulse Power Supply (HVHPPS) is designed with the goal to match fixed load, so that precise pulse output can be achieved. Generally the loads involve magnetron, klystron, and particle accelerators etc. The HVHPPS output pulse shape changes with load impedance variation due to various reasons. Due to changes in impedance, the performance of Pulse Power Supply degrades and reflects the power at the source end which causes component failure and system shut down. To overcome such problems, a scale down High Voltage High Pulse Power is designed and developed to match the dynamic impedance variations upto 25 % of mismatch. In earlier days, all HVHPPS were designed using microcontrollers where the problem of pulse to pulse monitoring and computational speed was compromised. The availability of variable and self-defined, Field Programmable Gate Array (FPGA) controller, which provided flexibility to design the pulse to pulse shaping and various vital parameter monitoring, made it possible. This paper presents the design and implementation of HVHPPS over an FPGA platform to meet the fast response requirement. This paper provides a solution for impedance mismatch problems associated with such types of power supply, and also presents specifications for major components in a high voltage pulse power system for various types of load ranges. An experimental test hardware was designed and developed for HVHPPS to implement dynamic impedance algorithm and validate the results.

Keywords: FPGA; High voltage high pulse power supply; Impedance mismatch; Pulse shaping; Pulse forming network; Klystron

NOMENCLATURE

t_p	Pulse Width
Z_o	Characteristic Impedance
L_n	Line Inductance
C_n	Line Capacitance
T_q	Time constant
I_{in}	Peak Current
I_{avg}	Average Current
V_o	Initial Voltage

1. INTRODUCTION

There are a wide range of applications of HVHPPS in commercial, industrial and defence sectors. There are two domains of application, one at low voltage low pulse power level and another at high voltage high pulse power. Basically, low voltage low pulse power is used in commercial and some sectors in industry whereas all military applications require High Voltage High Pulse Power Supply. HVHPPS uses a range of load (impedance) such as Magnetron, Klystron, Linear Accelerator, etc. Thus, efficient HVHPPS design and development is very essential.[1] The change in length of transmission line (Impedance) is due to temperature effect on microwave oscillator cavity dimensions, and dynamic Impedance characteristics of Amplifiers /oscillators. Impedance change in load will have an impact on the performance of HVHPPS i.e. back reflection & power loss. HVHPPS design is based on voltage fed series resonance pulse forming network which contains five blocks, as illustrated in Fig. 1.

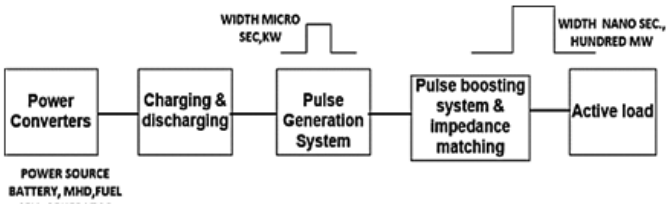

Figure 1. Block diagram of high voltage high pulse power supply.

The HVPPS begins with power converters and ends at the interface with the active load. There may be more blocks of pulse formation based on the requirement of pulse width amplitude. HVHPPS in a compact form is always desirable for defense, space and commercial applications. High Voltage High Pulse Power System generates peak power for very short duration as a single pulse at a particular Pulse Repetition Frequency (PRF).[2-3]

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2. DESIGN OF HIGH VOLTAGE HIGH PULSE POWER SYSTEM

All High Voltage High Pulse Power Supply systems have the problem of impedance mismatch. Hardware was therefore designed and developed to simulate the impedance mismatch and implement dynamic impedance matching.

2.1 Transmission Line Type HVHPPS

For proper pulse definition i.e., Pulse width, Pulse shape and pulse repetition frequency control, transmission line type of HVPPS is used and considered for design and development. As per the configuration shown in Fig. 2 the energy storage device is a lumped constant transmission line. These devices not only act as a source of electrical energy but also work as pulse shaping element i.e. Pulse Forming Network (PFN).[4]

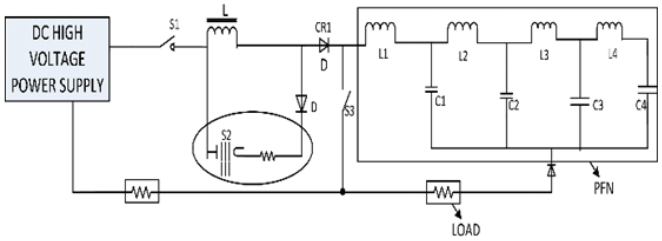

Figure 2. Transmission line type HVHPPS.

L	- Charging Inductance
L1, L2, L3, L4	- PFN Inductor
C1, C2, C3, C4	- PFN Capacitor
S1	- Controlled Switch
S2	- DeQ Switch
S3	- Main Pulse discharging switch
L	- Controlled Inductance
C1	- Capacitor
CR1	- Diode
PFN	- Pulse Forming Network

Table 1 represents the specification for hardware designed and developed as to implement impedance matching algorithm on FPGA.

Table 1. Specification of high voltage high pulse power supply

Parameter	Value
Pulse Output Voltage	15kV
Output Current	10A
Pulse width (Variable)	4-10μsec
Pulse width (nominal)	6 μsec
Repetition rate (Variable)	10-400Hz
Load impedance(R_L)	1500Ω
Turns Ratio	1:11

2.2 Charging Circuit and Charging Inductor

As per Fig. 3, when switch S is closed, current flows and charge the capacitor C1.

Due to resonance, a damped oscillation of current flows between L and C1.

Resonant time is $T_c = 2\pi\sqrt{L1C1}$

Resonance charging transfers the stored energy in charging inductor through CR1 (block the reverse flow of current) to capacitor C1 at voltage equal to twice that of DC High voltage supply.[5]

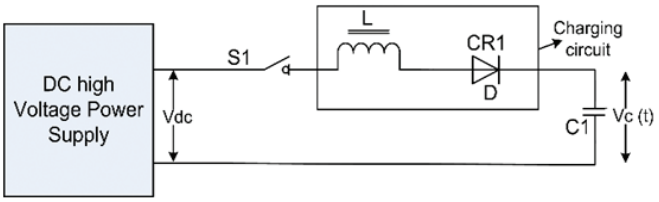

Figure 3. Resonance charging circuit.

The maximum Pulse Repetition Frequency is the deciding factor for quiescent duration between two pulses. As per Fig. 4, once the charging inductor charges twice the input DC voltage, the main switches ON based on a comparison with sawtooth waveform and control signal. The main switch switches ON accordingly and energy stored in capacitor discharges as pulse across the load.

Charging time = period of resonance/2

Charging time, $T = \pi\sqrt{LC}$

where, L is inductance of charging choke and C is capacitance of pulse forming network.[6]

We consider a charging time = 1.5msec, and Charging Inductor = 0.808H at 3kV.

Higher inductance of the charging choke causes slow rate of charging, thus inductor charging time increases.

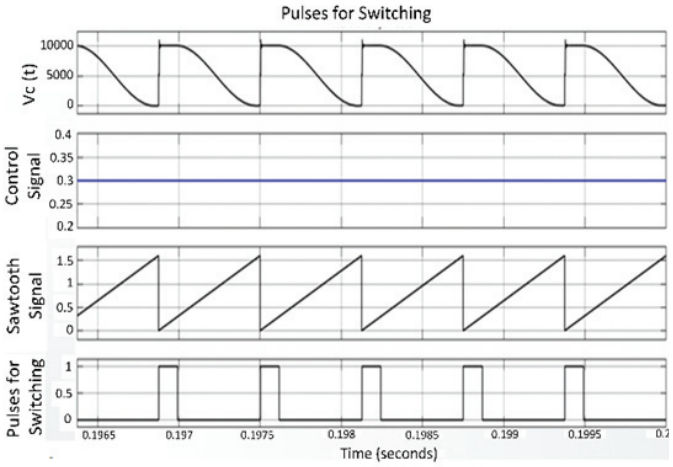

Figure 4. Waveforms obtained from the controlling circuit.

2.3 Charging Diode

The main purpose of charging diode is to block the reverse flow of current which is connected in series as shown in Fig. 3. The number of diodes will be decided based on the requirement of reverse blocking voltage.

In this case, 6 fast recovery diodes each having a 500V reverse blocking voltage are considered to meet 3kV reverse blocking voltage capacity.

2.4 Novel Pulse Forming Network

In PFN system architecture, as shown in Fig. 5, we have to make assumption about the load nature i.e. whether it is static or dynamic and the required pulse power generation voltage.

$$(\text{Primary Impedance})Z_p = \frac{Z_s\,(\text{Seconday Load Impedance})}{N^2}\ \text{Pulse current of pulse transformer} = \left(\frac{V}{R}\right)$$

Thus the maximum transformer power is calculated by matching the pulse transmission line impedance to load impedance. The nature of pulse changes with the length of the transmission cable.[7]

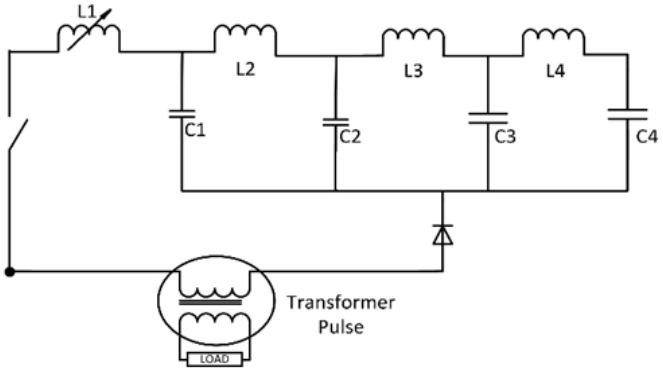

Figure 5. Novel pulse forming network design.

The novel requisite pulse width for load is the deciding factor for the calculation of pulse forming network (PFN) parameters.

Thus, total capacitance of PFN, $C_n = \frac{t_p}{2Z}$

where, t_p is pulse width; A, N and B should meet L_n. Normally

Z_o = Load Impedance which is already known, $Z_o = \sqrt{\frac{L_n}{C_n}}$ is the characteristic impedance of PFN.

To achieve dynamic impedance variance compensation of transmission line, the value of pulse forming network capacitance will always be 5-10 % higher than the calculated value.

The inductance required, $L_n = Z_0^{\,2} \times C_n$.
In case of air wound,

$$\text{Inductance } L_n = \frac{0.2 \times A^2 \times N^2}{3A + 9B}$$

where, L= Inductance in µH, A= Mean dia of coil, B= length of coil, and N = number of turns.

Table 2. Calculated value of network parameters

Network Parameter	Calculated Value
Network Capacitance (Cn)	0.24 µF
C1 to C6	0.047 µF
No. of capacitance	06 Nos
Network Inductance	43.75 µH
Mean dia of coil (A)	2.75 Inch
Length of coil (B)	24.5 Inch
Number of turns (N)	82

As shown in Table 2, for all the calculated value of network parameters, the total number of section of L and C banks calculated on the basis of flatness percentage required for pulse shape is shown.

2.5 Modified Decreasing Quality Factor

Pulse regulation achieved through DeQing switch S2 (Decreasing Q Factor) connected through RC network in Fig. 6.

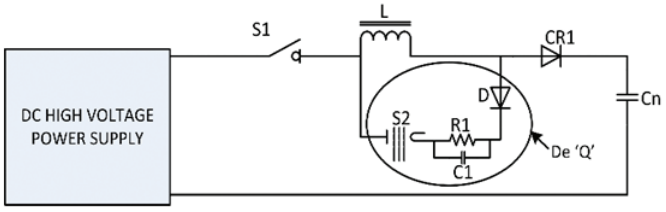

Figure 6. DeQing switch circuit.

DeQ switching operation takes place when charging inductor voltage crosses the set charging value (user defined). During switching operation, excess energy stored in the inductor is dissipated in DeQ resistor.[8]

Decay time constant, $T_q = \frac{L_{\text{charging choke}}}{R_{deq}}$.

Pulse charging average current is represented as, $I_{av} = \frac{CV}{T}$.

Hence, Peak current I_{av} through charging choke is represented

$$I_{in} = \frac{\pi}{2} \times I_{av}.$$

DC current flowing through the choke is represented as

$$I_{dc} = I_{av} \times \text{dutyratio}.$$

FPGA based controllers are always compact, more reliable, simpler and are part of emerging technology. FPGA based controller works in shielded environment for EMI and EMC protection. The block diagram of control architecture, power flow and logical operation of high voltage high pulse power system is shown in Figure 7. FPGA controls the charging requirement of the pulse forming network and the main switch operation. Further it controls the impedance matching and logical flow of power.

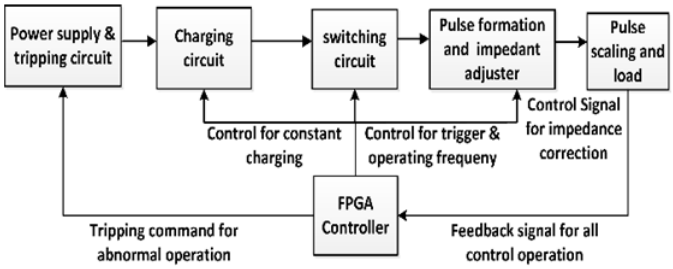

Figure 7. Control architecture, power flow and logical operation.

To implement the control and impedance matching, pulse to pulse voltage is monitored through voltage compensation network and the same is used as a feedback for comparison with ideal pulse shape defined in the reference.[9] When pulse shape deteriorates due to positive and negative impedance

mismatch beyond 10 % (acceptable limit defined by the user), a trip command is issued by the controller to stop output voltage generation.

2.6 Impedance Matching Algorithm Implementation

Pulse Forming Network has multiple sections of LC tank based on pulse width requirement. A novel technique is introduced to create an option for impedance matching at the source end. In this technique more numbers of inductance coils are created to meet the impedance matching requirement. The source voltage is sensed with the help of voltage sensor circuit. The sensed source voltage is given as the analog input to ADC of Virtex 6 FPGA board of Xilinx.

FPGA controller is of importance because it is used to provide gate pulses for switching MOSFET. The gate pulse of required width, which is found from simulation, is developed using FPGA controller that is used for generating the gate pulses for switching on MOSFET at a high frequency. Here the recurrence frequency used is of 1.6 kHz.

To develop the pulses of required width, the control scheme is developed in MATLAB using Xilinx blocks as in Figure 8. Counter gives either sawtooth or triangular waveforms by using up or up–down operational mode. The expression for selecting count value is shown in Eq.1 below:

$$\text{Count value} = \frac{f_{clock}}{f_{desired} \text{ x explicitperiod}} \qquad (1)$$

But the count value is limited by the number of bits with the relation 2^{nbits} > count value. For example, if the count value is 210, then the minimum number of bits selected should be 8. The explicit period normally is very small. 1.6 kHz count frequency of saw tooth waveform generation with explicit value of approximately 10-6 is around 210. The clock frequency is made 1 when using system generator to match MATLAB simulation period. A constant value of half of the count value is compared to the saw tooth waveform obtained from the up counter block is of discrete type. So as to get 50% duty cycle of rectangular wave. Now it is applied to up-down counter saw tooth wave for which the signal increases linearly for high value and decreases linearly for low value. The up-down counter block a triangular signal was obtained. This was compared with a constant value selected based on the percentage of duty cycle needed to get the required gate pulse.

The generated reference signal was compared with a set value of requirement and switching signals were given to the devices through pulse amplification and isolation circuits. The flow chart in Fig. 9 indicates the algorithm implemented in FPGA working. The control signal varies based on the level of faults and level of impedance mismatch.

Condition I: Negative Mismatch

Case 1: if $Z_l < Z_0$ and $Z_l \approx 80$ % to 90 % of Z_0
then $V_{output} = 50$ % of $V_{rated\ value}$
$PRF_{set} = 50\%$ of PRF_{max}

Case 2: if $Z_l < Z_0$ and $Z_l \approx 80\%$ to 75% of Z_0
then $V_{output} = 10\%$ of $V_{rated\ value}$
$PRF_{set} = 10\%$ of PRF_{max}

Case 3: if $Z_l < Z_0$ and $Z_l > 75\%\ Z_0$
then trip command will be sent.

Condition II: Positive Mismatch

Case 1: if $Z_l > Z_0$ and $Z_l \approx 1.10$ to 1.20 of Z_0
then $V_{output} = 50\%$ of $V_{rated\ value}$
$PRF_{set} = 50\%$ of PRF_{max}

Case 2: if $Z_l > Z_0$ and $Z_l \approx 1.20$ to 1.25 of Z_0
then $V_{output} = 10\%$ of $V_{rated\ value}$
$PRF_{set} = 10\%$ of PRF_{max}

Case 3: if $Z_l > Z_0$ and $Z_l > 1.25$ of Z_0
then trip command will be sent.

There will be two conditions of mismatch problem i.e. Positive and Negative. In negative mismatch power will reflect back to source, which may cause system failure. To protect the vital components, the set high voltage and PRF should be reduced as per conditions mentioned above.

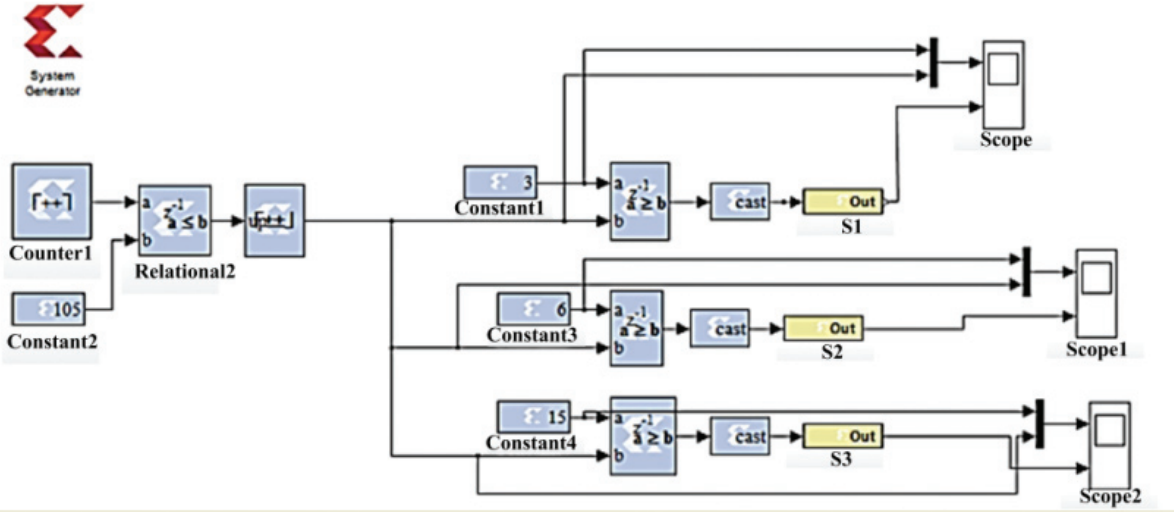

Figure 8. Simulink model to generate required pulses using FPGA.

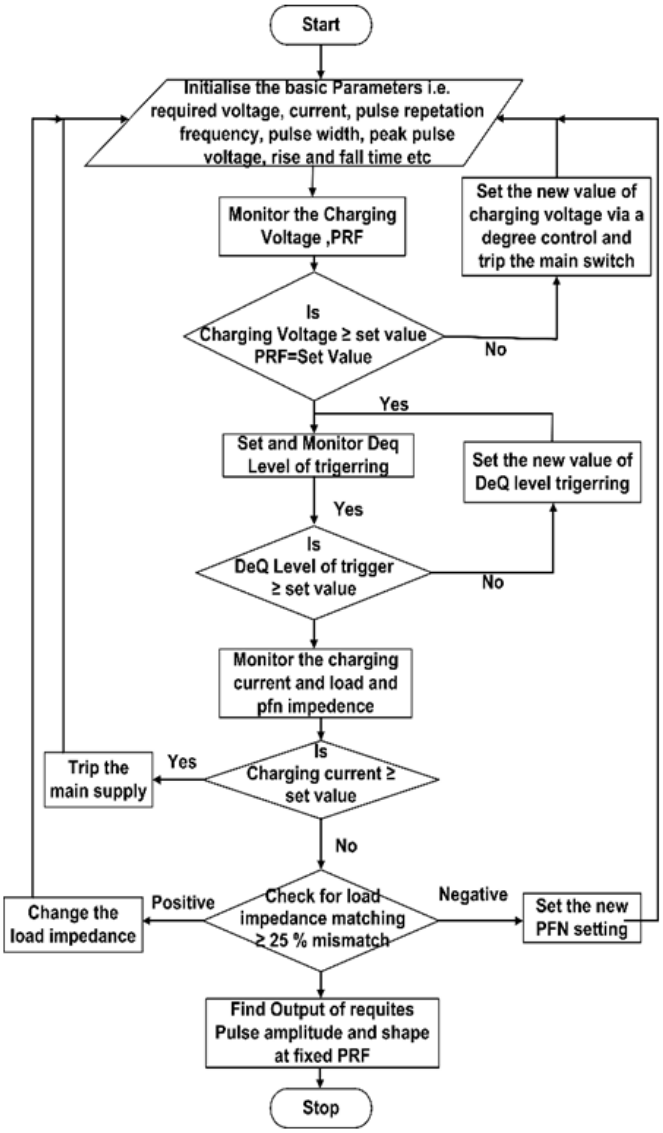

Figure 9. Flow chart of FPGA programming.

3. PROTOTYPE HARDWARE OF HVHPPS AND ANALYSIS

HVHPPS hardware created for 1.5 KΩ resistor connected through triple shielded cable impedance of 12.5 Ω.

The detailed specifications of HVHPPS is given in Table 1. A scale down proof of concept hardware model was developed and control algorithm on FPGA implemented in High Voltage High Pulse Power generation for impedance matching. The same experiment has been proven on actual hardware was shown in Fig. 10 and the result was validated for establishing the functionality of the system.

Charging voltage produce due to resonance is observed through RC sensing circuit as shown in Fig. 11.

DeQ RC Network will not have more than 20 % power dissipation accordingly DeQ switching level adjusted. Thus constant charging voltage is maintained for each pulse to achieve the pulse regulation.[10]

PRF is controlled based on mismatch and fault conditions depending upon severity of fault, the PRF will automatically reduce from 50 % to 20 % of rated value.

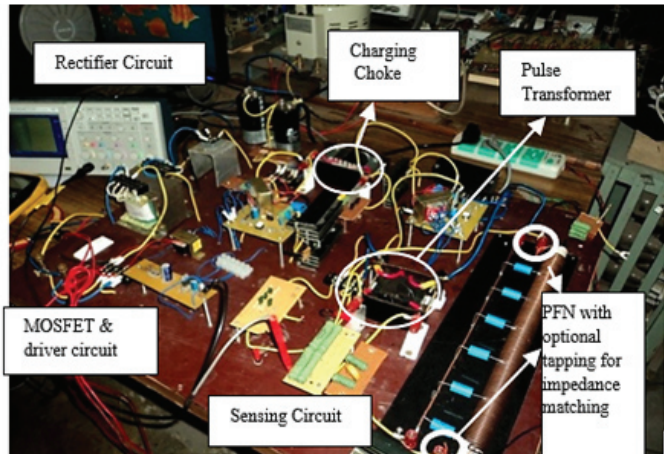

Figure 10. Hardware of High Voltage High Pulse Power Supply (HVHPPS).

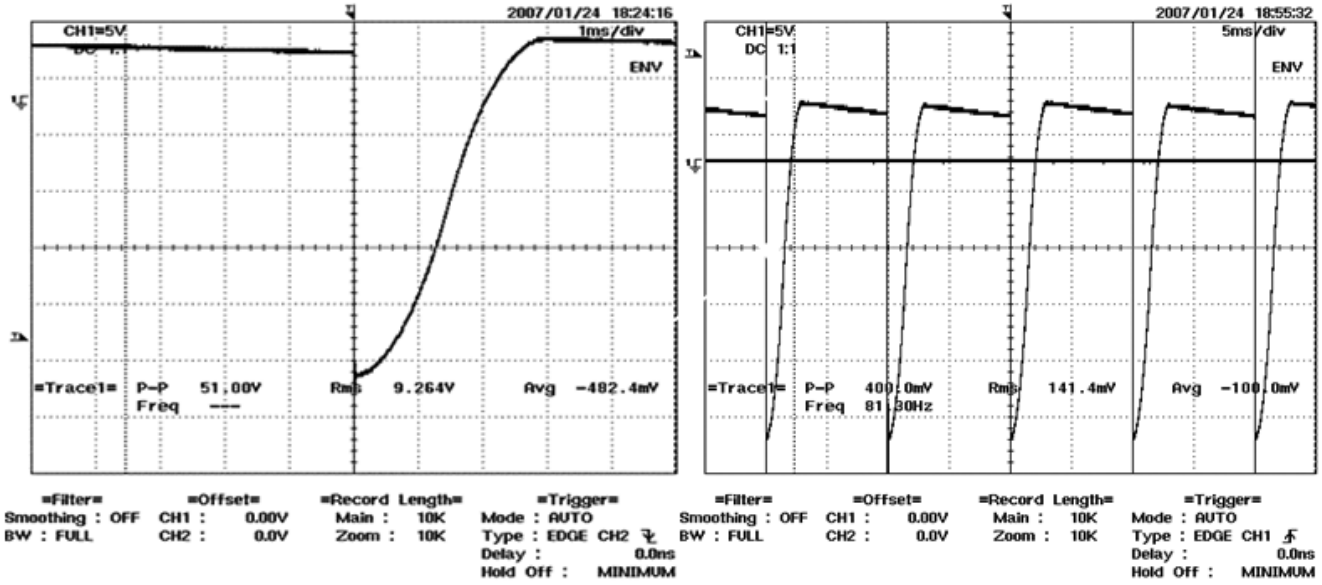

Figure 11. Charging voltage waveform.

Figure 12 shows the charging current which is sensed by 1Ω resistor assembly. If output current rapidly increases due to arc, then overcurrent protection circuit turns off EHT supply.

The ferrite core pulse transformer is conservatively designed with bifilar winding.

Designed Prototype hardware gives 15kV pulse output voltage at secondary of pulse transformer (1:11) where primary voltage is 1.3kV. Figure13 shows output voltage across resistive load of 1.5kΩ.

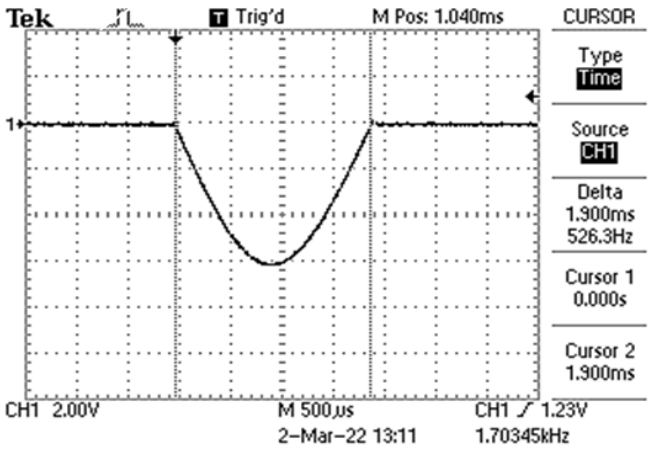

Figure 12. Charging current.

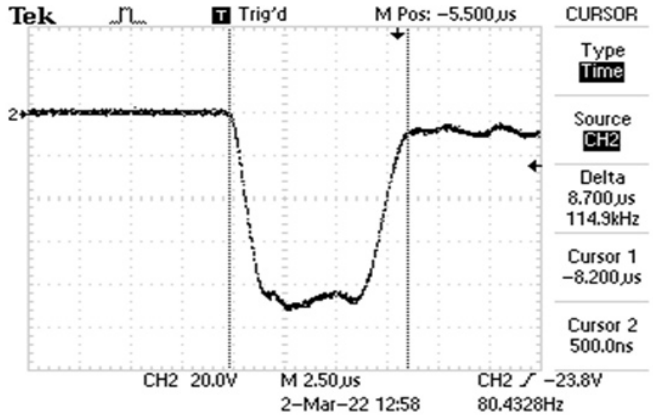

Figure 13. Output voltage at load.

The achieved output pulse is having two overshoots and one undershoot on flat top which will be due to mismatch of the load. In such cases flat pulse top can be achieved after PFN adjustment/ tuning.

4. EXPERIMENTAL RESULTS AND ANALYSIS

Figure 14 shows the hardware of the High Voltage High Pulse Power Supply developed for implementation of impedance matching offline which delivers 15 kV, 10 - 400 Hz (selectable) frequency, approximately 10 A current (Primary of Pulse transformer) with 6 micro sec pulse duration for primary of pulse transformer, when the load is klystron microwave amplifier.

As shown in Fig. 15, a perfectly impedance matched klystron current waveform was observed during the experiment with manual taped change option created for impedance matching.

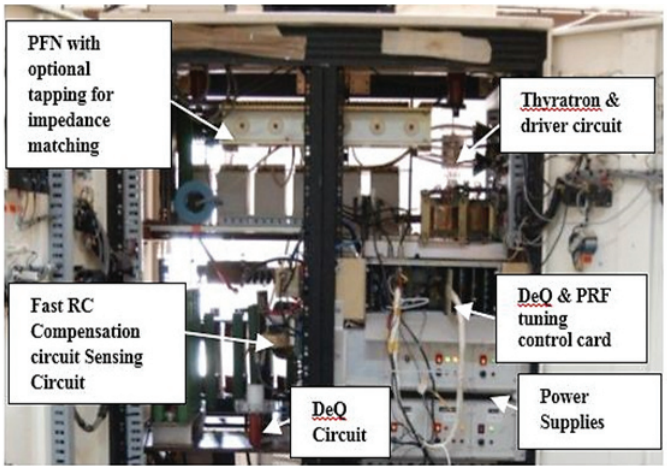

Figure 14. Actual hardware of High Voltage High Pulse Power Supply (HVHPPS).

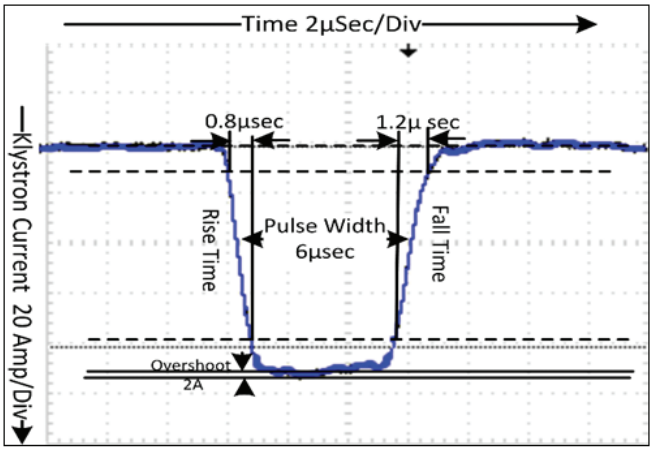

Figure 15. Reference Klystron current waveform observed in perfectly matched condition.

The rise time, pulse width, fall time and overshoot of 8 µsec, 6 µsec, 1.2 µsec and over shoot of 2A obtained respectively.

As per Fig. 16, overshoot of 8A was observed and 1.4 µsec of fall time was obtained which was due to positive mismatch ($Z_l > Z_o$) of PFN.

For pulse generated by PFN will be

$$i(t) = \frac{V_0}{Z_0 + R_l}\left\{\begin{array}{l} 1 - U(t-2\delta) - \frac{Z_0 - R_l}{Z_0 + R_l}\left[U(t-2\delta) - U(t-4\delta)\right] - \\ \frac{Z_0 - R_l}{Z_0 + R_l}\left[U(t-2\delta) - U(t-4\delta)\right] + \\ \left(\frac{Z_0 - R_l}{Z_0 + R_l}\right)^2\left[U(t-4\delta) - U(t-6\delta)\right] + \ldots\ldots \end{array}\right\}$$

where, $U(\Delta t) = 1$ for $\Delta t > 0$ and $U(\Delta t) = 0$ for $\Delta t < 0$

$\Delta t = (t - n\delta), n = 2, 4, 6....$

Initial tapping of PFN increased i.e. line inductance was enhanced to compensate positive mismatch by adding the number of turns (Ln) to obtain the reference waveform for klystron.

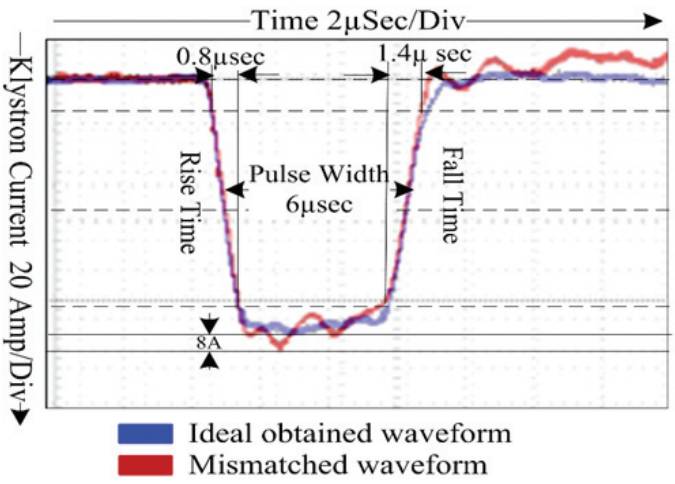

Figure 16. Klystron current waveform with +ve mismatch.

As per Fig. 17, Klystron output current showed negative mismatch ($Z_l < Z_o$) of upto 18 % of the reference value. This negative mismatch was detected and measured to give a suitable command for output voltage amplitude and frequency correction.

To compensate the overshoot, pulse width, fall time and rise time, PFN tapping at the trailing edge was done in such a way that some of the air wound coils (Ln) were eliminated from the PFN.

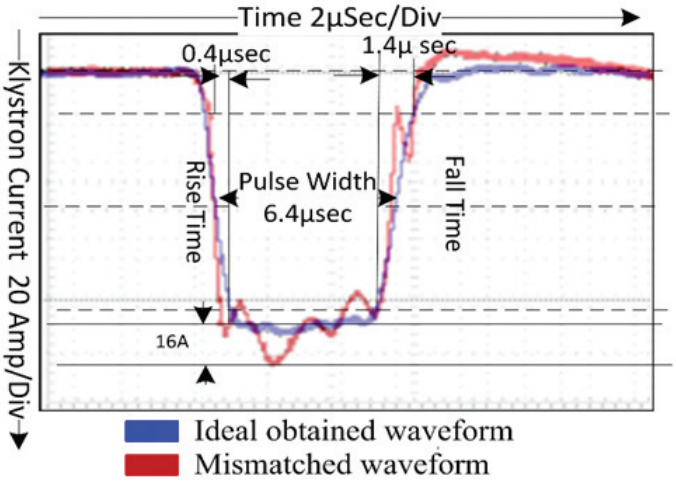

Figure 17. Klystron current waveform with -ve mismatch.

Figure 18 shows that when impedance mismatch is high the controller will work in time domain and issue corrective command based on deterioration of the output voltage pulse parameters.

After observation and comparative analysis with reference waveform, tripping command is issued by FPGA controller. Based on the mismatch condition the developed hardware option for impedance matching correction is utilized offline and impedance matching of PFN at the source end and finally ideal pulse as shown in Figure.15 is achieved, which is a perfectly impedance matched condition.

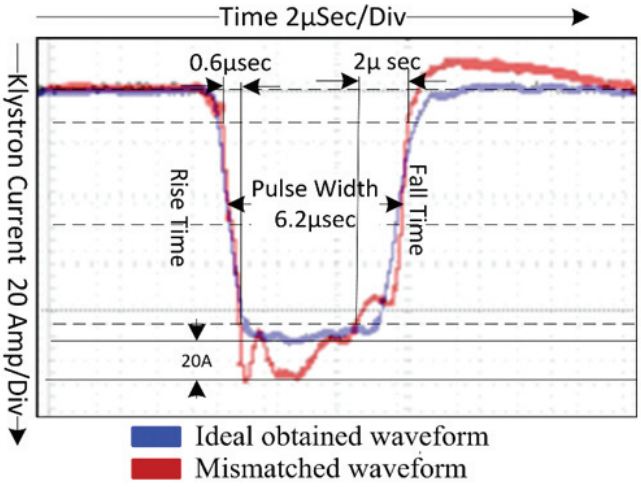

Figure 18. Klystron current waveform with highly mismatch.

5. CONCLUSION

A concept hardware was developed for compact high voltage high pulse power system which delivered 15kV and 10 amp pulse with a sharp fall and rise time in micro seconds. Sharp fall and rise time are achieved by using MOSFET and ferrite core pulse transformer. With appropriate control using Virtex FPGA controller, the output pulse can vary pulse repetition frequency from 10 Hz to 400 Hz and voltage can be achieved from 1 kV to 15 kV.

Impedance matching mechanism and algorithm were tested in scale down model. The same was implemented in actual hardware as klystron load (klystron amplifier of 6MW, 6 micro sec, and 0.001 duty cycle) and impedance matching tested. Offline impedance matching tuning mechanism was achieved.

In future, dynamic impedance matching can be thought of using servo control mechanism for online PFN tuning. Servo control mechanism will enable the HVHPPS to work in wide band as universal power supply.

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