Parametric study of pulsed laser deposited (PLD) WSe2 2D transistors

Parametric Study of Pulsed Laser Deposited (PLD) WSe_2 2D Transistors

S.C.Mbisike[a], S.Seo[b], S.Lee[b], J.Phair[c], and R.Cheung[a]

[a]Scottish Microelectronics Centre, Institute for Integrated Micro and Nano Systems, University of Edinburgh, EH9 3FF, United Kingdom.
S.C.MBISIKE@sms.ed.ac.uk
[b]School of Materials Science and Engineering, Gwangju Institute of Science and Technology, Gwangju, 61005, Republic of Korea.
[c]Pyreos Limited, Scottish Microelectronics Centre, Alexander Crum Brown Rd, Edinburgh EH9 3FF.

ABSTRACT

A fabrication process for making large area transistors on pulsed laser deposited (PLD) WSe_2 has been developed. Large films of WSe_2 have been deposited via PLD technique on SiO_2/Si substrate. Employing a mask-less lithography technique and using vapour XeF_2 as an etchant, transistors of lengths (17, 83, 323 and 1000 µm) and widths (14 and 850 µm) have been fabricated. Electrical characterization of the transistors show that as the channel length (L) decreases, the magnitude of the drain-source current increases. In addition, the current across the transistor has been found to increase by increasing the channel width (W). Moreover, channels with large areas have been found to deliver substantially more drain-source current compared with smaller channel areas with similar W/L. A W/L ratio of 0.85 has been found to possess the highest drain current across the transistors fabricated. From the transfer length measurement (TLM), the sheet resistance and contact resistance of the device have been measured. Field effect mobility of the transistors have been calculated. Raman spectrum shows that PLD WSe_2 possess similar quality as exfoliated WSe_2. However, Photoluminescence (PL) spectrum and TLM results suggest the lack of bandgap in our 14-layer PLD WSe_2.

Keywords: PLD, WSe_2, large area 2D, field-effect transistor (FET)

1. INTRODUCTION

Since 2004 when thin carbon films (single layer graphene) were produced by exfoliation and their electric properties studied [1], two dimensional (2D) materials have continued to gain attention in an effort to discover better materials as well as to expand their applications [2]. Beyond graphene with its overlapping band structure [1], other materials have been investigated such as the transition metal dichalcogenide (TMD). TMD are materials with layered structures that can be cleaved down to less than 100nm. TMD's have gained prominence by virtue of their unique electrical and optical properties. Electrically, they range from insulators (HfS_2) through to semiconductors (WSe_2), semi metals (WTe_2) and to metals (VSe_2). The diversity of TMD is attributed to the existence of non-bonding d-bands and the degree to which they are filled [3].

According to Sahin et al. [4], the band gap of semiconducting TMD increases and transforms to a direct band gap with decreasing number of layers, which makes them promising candidates for nanoscale field-effect transistors and solar cell applications [5]. The lack of covalent bonding between TMD layers enables the fabrication of hetero-structures by allowing the stacking of materials. The structural plane of WSe_2 consists of two atoms of selenium and one atom of tungsten covalently bonded together (Se–W–Se). These atoms form a hexagonal arrangement and adjacent planes are held together by van der waals interactions [6]. As a result of the layered stacking, the scotch tape method has been employed to transfer WSe_2 at various thicknesses and within a few square-microns in area onto a substrate. The flakes being of several layers thick, have been etched using xenon difluoride (XeF_2) vapour [7]. However, one disadvantage associated with exfoliated materials is that after exfoliation, materials transferred to a substrate are distributed randomly across the substrate and are of various thicknesses and dimensions. The non-uniformity both in thickness and in dimension makes it difficult to achieve complex fabrication designs like hetero-structure devices. The size of the 2D material is of importance especially in IC design and the need to control the material thickness over large area has paved the way for bottom up deposition techniques. Pulsed laser deposition (PLD) [8], chemical layer deposition (CVD) [9] and atomic layer deposition (ALD) [10] have all been employed in growing 2D materials for larger area, controlling the material thickness and improving the quality of film produced. PLD, like CVD is a bottom-up deposition technique. PLD allows for large area growth (>2 cm) of 2D materials with control in sample thickness and size. On the other hand, although exfoliation produces purer layers, it is not possible to control the size and thickness. The inability to control sample size and thickness during exfoliation is inherent in the deposition process. PLD has not been researched widely for the fabrication of 2D materials. Technically, the PLD process is a simplified bottom-up deposition technique as it requires no additional precursors except the target of the deposited material [8]. PLD technique is relatively quick and samples can be grown within 30 minutes. Also, the samples can be grown at low temperatures at around 450 °C. CVD requires high temperature (750 - 1000 °C), longer process time and additional precursors [11]. Moreover, the thickness control for PLD is excellent as it is dependent on the number of laser pulses and it has short growth time thus possessing high repeatability [8], [12]. Seo et.al [13], grew a centimetre scale monolayer of WSe_2 thin film on SiO_2/Si substrate via PLD. From their experiment, the PLD technique has been shown to achieve good layer uniformity and the thickness of the layer has been controlled by the number of laser pulses. However, other challenges exist in these bottom up approaches such as defect, domain size, and stoichiometry control [6].

In this work, we study the influence of the transistor channel dimensions on the electrical properties of the PLD WSe_2 transistors. In addition, Raman and PL spectroscopy have been used to characterise the PLD WSe_2. By employing photo-lithography and XeF_2 vapour etching techniques, transistors with multiple channel dimensions have been fabricated. The channel dimension with optimum performance will be employed for future hetero-structure design.

2. EXPERIMENTAL

2.1. Fabrication Process

WSe_2 transistors have been designed and fabricated on a SiO_2/Si substrate. Figure 1a shows the step by step fabrication process employed in making the PLD WSe_2 transistors. Conventional photo-lithography technique has been employed to fabricate the device. Using a maskless lithography tool, several WSe_2 channel patterns with lengths 17 µm, 83 µm, 323 µm and 1000 µm and width of 14 µm and 850 µm have been designed and fabricated. The WSe_2 has been etched using vapour XeF_2 (Orbis Alpha, MEMSTAR). During the vapour-etch, the chamber pressure has been maintained at 1.2 Torr. Nitrogen (N_2) carrier on gas (100 sccm) flows over XeF_2 crystal and transports the vapour XeF_2 (25 sccm) onto the material. The etch rate recorded has been about 3 nm / min. The sample was etched completely within 3 minutes. Figure 1b shows the etched rectangular channel and a few alignment marks on a SiO_2/Si substrate after the photoresist had been stripped off. To deposit the metal contacts (Titanium adhesion and Aluminium) on the channel, a sputtering tool (Plasmalab 400 OPT) has been used. 20 nm of Titanium has been deposited at a rate of 3 nm/min and 300 nm of Aluminum has been deposited at 5.8 nm/min. The stack formed has been lifted-off using Microposit Remover 1165 (a photoresist remover) at 40°C. The stack has been immersed in the photo-resist stripper for about 2 hours before it was sonicated. The sonication lasted for about 15 seconds to remove the metal residue completely. The device has been rinsed in IPA and de-ionized water respectively.

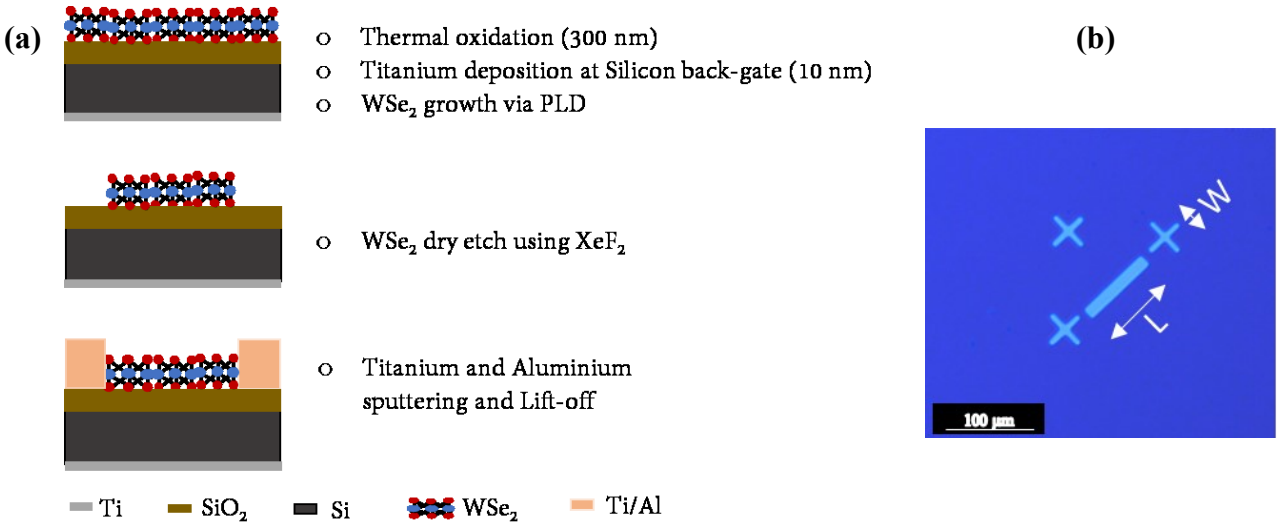


Figure 1: (a) Schematic of the PLD WSe_2 FET fabrication process; **(b)** PLD WSe_2 channel and alignment mark pattern after etching using vapour XeF_2.

2.2. Characterization

Raman spectroscopy, Energy Dispersive X-ray Spectroscopy (EDX) and Photoluminescence (PL) spectroscopy have been used to characterize the WSe_2. The Raman and PL have been performed at room temperature and atmospheric pressure while the EDX has been performed in vacuum. EDX has been carried out using the Tescan Vega Scanning Electron Microscope (SEM). To avoid heating or damage to the sample, 4 KV of HV has been applied for EDX. On the other hand, 5% of the 3 mW laser has been used for Raman and PL. The thickness of the WSe_2 has been measured using the D5000 atomic force microscope (AFM). The measurement has been carried out in tapping mode with a tip of spring constant 3 N/m and resonant frequency of 75 KHz.

The electrical properties of the transistors have been tested using a Keithley probe station. The field effect behaviour has been investigated by back-gating the transistor from +50 to -130 V and the transfer characteristics plotted. From the transfer characteristics, the field effect mobility has been deduced. From the transfer length measurement, the sheet resistance and contact resistance of the devices have been measured.

3. RESULTS AND DISCUSSION

3.1. AFM and EDX Analysis

To measure the thickness of the PLD WSe_2 channel and the elemental composition of the sample, AFM and EDX analysis have been performed. The thickness of the WSe_2 channel has been measured to be 10 nm ± 2 nm which is about 14-layer. The thickness of TMD materials can affect their optical and electrical response. Hence, it is important to compare the material thickness with its resultant properties [7], [13], [14]. EDX analysis has been performed to detect the presence of impurity and discover the elemental composition of the material and substrate. The presence of impurity could affect the Raman and PL analysis as well as the electrical properties of the material. The EDX analysis is thus: Silicon 40.18%, Oxygen 39.57%, Tungsten 13.8% and Selenium 5.88%. This observation indicates the presence of W and Se on the substrate.

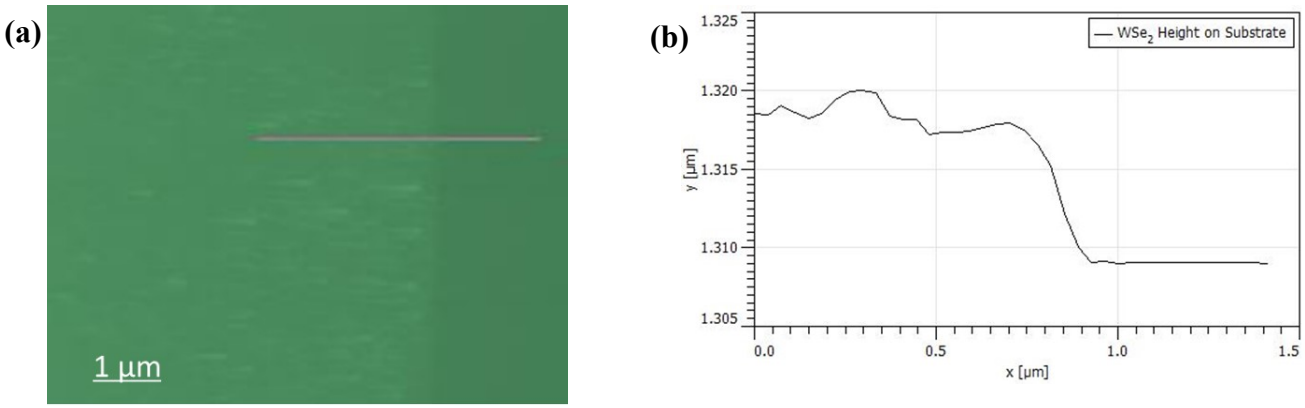


Fig 2 show graphs obtained from the AFM experiments. **(a)** 7 µm by 7 µm AFM image of PLD WSe_2 on SiO_2 substrate. The grey line shows the step trace performed from the SiO_2/Si substrate

to the top of the PLD WSe_2 **(b)** the height profile of the PLD WSe_2 sample is measured to be about 10 nm, which is about 14 layers of WSe_2. The film has been found to be continuous across the substrate and possesses a surface roughness of approximately ±2 nm.

3.2. Analysis of the Raman and Photoluminescence (PL) Spectrum

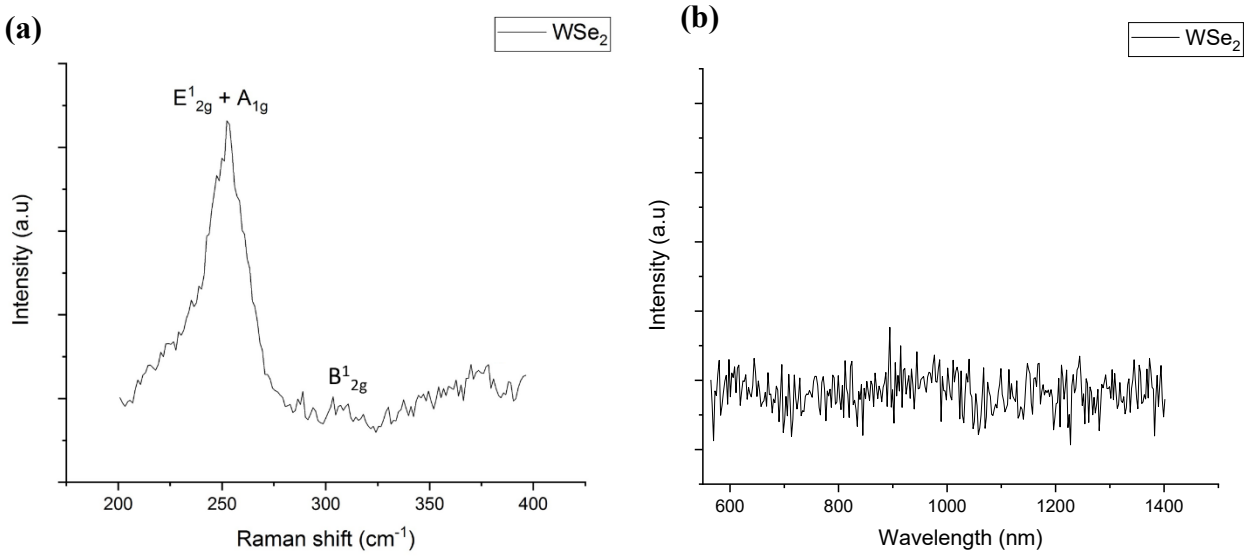


Figure 3: (a) Raman spectrum of PLD WSe_2. Active Raman peak at 252 cm^{-1} indicates good quality sample and the presence of B^1_{2g} secondary peak indicates multiple layers thick; **(b)** PL spectrum of PLD WSe_2 shows the absence of an A-exciton and trion peak.

Figure 3(a) shows the Raman spectrum of the sample which has been excited with a 450 nm laser. In general, from a Raman spectrum, changes in the structural integrity (surface change or chemical bonding) of a material could be detected [15]. As previously reported [7], exfoliated WSe_2 crystals appear about the 250 cm^{-1} position on a Raman spectrum. Pulsed laser deposited WSe_2 is expected to appear about the same region as has been reported [13]. In-plane E^1_{2g} mode from the out-of-phase vibration and A_{1g} mode from the out-of-plane vibrations of WSe_2 both appear as a single peak (E^1_{2g} + A_{1g}) at 252 cm^{-1} [7], [13], [15]. From our samples, (E^1_{2g} + A_{1g}) peak of PLD WSe_2 appears at about the same peak position as exfoliated WSe_2 as shown in figure 3a. Moreover in figure 3a, the presence of the B^1_{2g} peak indicates the sample is not a mono layer. Mono layer PLD WSe_2 has only the primary Raman peaks E^1_{2g} + A_{1g} [13]; same for exfoliated WSe_2 [7]. The presence of B^1_{2g} peak has been reported to be a result of interlayer interaction [8], [16]. As the number of WSe_2 layers increases, the Raman modes are expected to become more rigid resulting in vibrational softening [17]. Therefore, the B^1_{2g} peak intensity is expected to diminish as the number of layers increases. The low intensity of the B^1_{2g} peak observed in our PLD WSe_2, where there are 14 layers, could be due to the presence of vibrational dampening as a result of lower interlayer interaction [8], [16]. In addition, the full width half maximum (FWHM) of exfoliated and CVD WSe_2 have been extracted from literature. FWHM for exfoliated WSe_2 have been measured to be 3.7 and 3.8 cm^{-1} for monolayer and bilayer respectively [7] while values of 4.2 and 5.5 cm^{-1} have been reported for monolayer CVD WSe_2 [18], [19]. The FWHM

measured for our material is 15 cm^{-1}. Values of 12.45 and 14.23 cm^{-1} have been reported for mono layer and few (3) layers PLD WSe_2 respectively [13]. The FWHM measured in our experiment shows our 14-layer PLD WSe_2 is of relatively good quality.

Figure 3(b) shows the photoluminescence (PL) spectrum of our 14-layer PLD WSe_2. The sample has been excited by a 450 nm laser. Normally, the PL spectrum of exfoliated WSe_2 shows the A-exciton and trion peaks around the 750 – 800 nm wavelength range [7]. The bandgap of exfoliated and CVD WSe_2 has been reported to be 1.65 eV and 1.6 eV respectively[7], [20]. From the spectrum shown in figure 3(b), there is no noticeable PL peak at the A-exciton and trion region [21]. The non-existence of the A-exciton and trion peaks suggests a lack of bandgap or the existence of non-radiative recombination in our PLD WSe_2 [22]. Also, the presence of grain boundaries can degrade the physical properties of 2D materials thus leading to quenching of the photoluminescence [23]. Thicker WSe_2 layers can result in a higher concentration of grain boundaries and subsequently the presence of quenching. Typically, monolayer thick (~0.7 nm) semiconducting TMDs are preferred as optoelectronic devices [24] due to the band gap increase as well as the transformation from indirect bandgap into a direct band gap with decreasing number of layers [25].

3.3. Electrical Properties

The electrical properties of the PLD WSe_2 transistors fabricated have been characterised. Figure 4(a) shows a 2D schematic of the fabricated device along with the thickness of the materials and the bias technique. The schematic shows a heavily boron doped silicon substrate which has been employed for the back-gate voltage (V_{bg}) with a 300 nm SiO_2 dielectric. The PLD WSe_2 channel is 10nm thick and the Ti/Al contact is 20/300 nm thick. Figure 4b shows four electrodes made from Ti/Al labelled I+ and I- which are the current sources while V_1 and V_2 are the voltage measurement points.

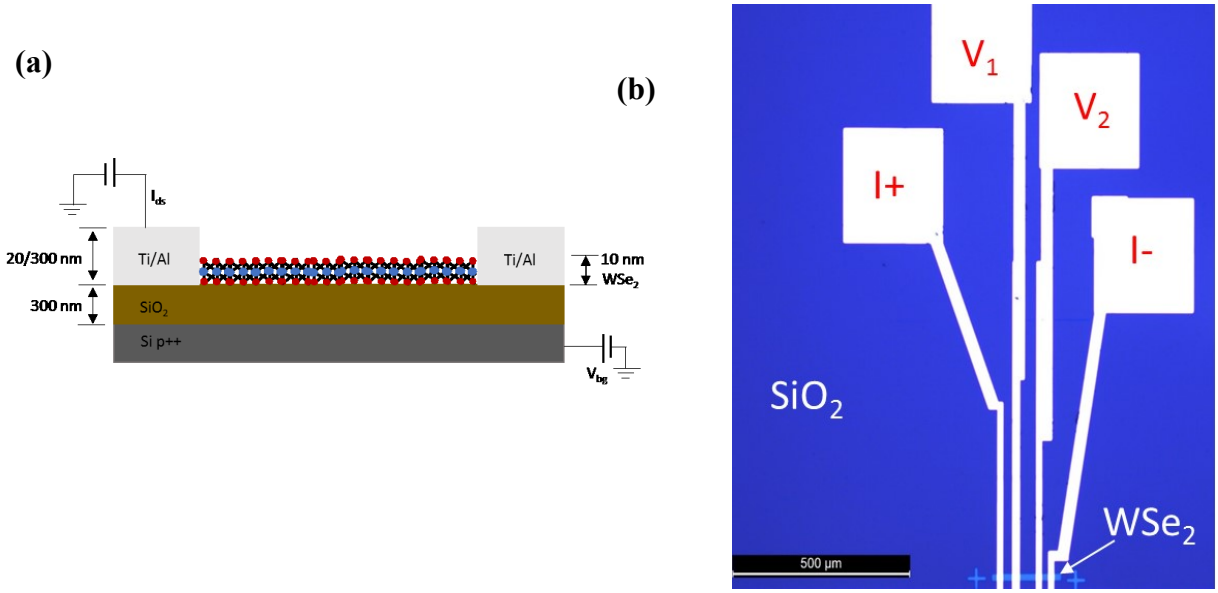


Figure 4: (a) Schematic of the fabricated PLD WSe_2 FET with geometrical dimensions; **(b)** Actual device fabricated showing the PLD WSe_2 channel with four metal electrodes on a SiO_2 / Si substrate.

3.3.1. Transfer Length Measurement (TLM)

Using the TLM[26] technique as shown in figure 5(a), the sheet resistance R_{sh} and contact resistance R_c of the 14-layer PLD WSe_2 transistor have been calculated. The electrode probe spacing is 27 µm, 74 µm and 90 µm. Figure 5(b) shows the electrode probe spacing against the measured total resistance for V_{bg} (24.5 V, -1.11 V and -26.7 V).

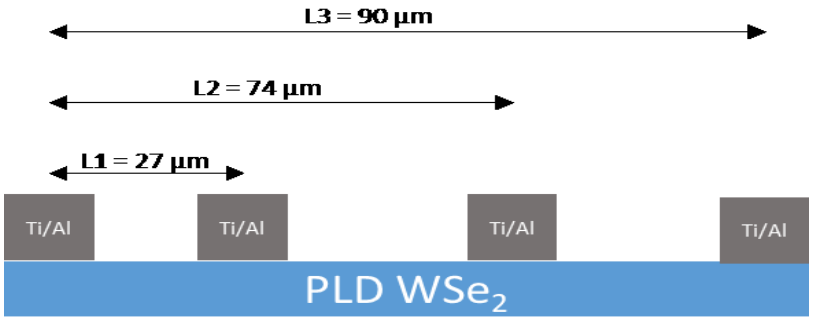


Figure 5a: TLM Electrode Spacing

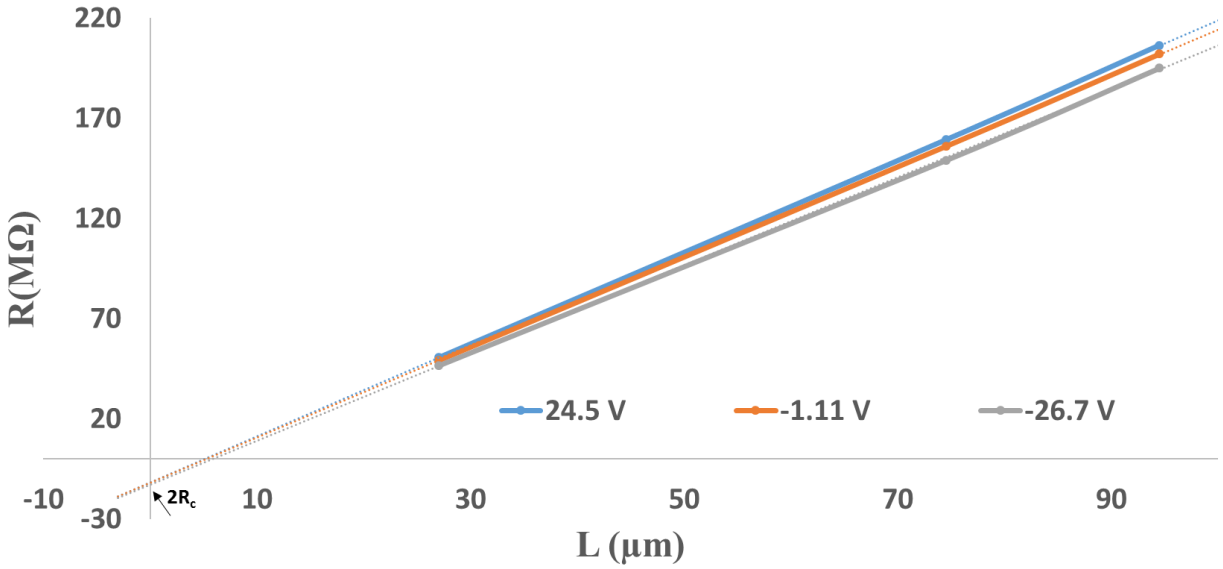


Figure 5b: Graph of total resistance as a function of electrode probe spacing plotted at various values of back-gate voltage showing a negative contact resistance at the y-intersect.

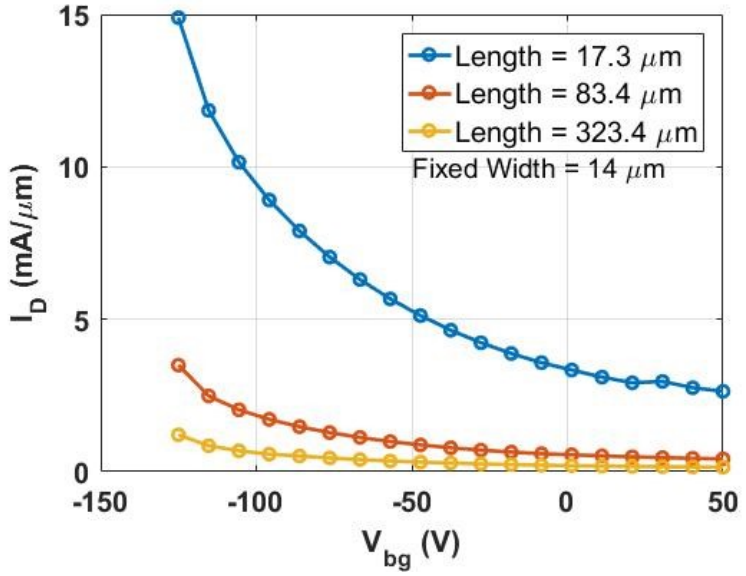
From figure 5(b) above, the sheet resistance and contact resistance have been calculated to be 31.7 MΩ/□ and -6.11 MΩ.µm respectively. Both the TLM and 4-point probe method produce negative contact resistance for PLD WSe_2 at low gate voltage (-30 V to 30 V). As the gate voltage

increases beyond 30 V, the polarity of the resistance changes. The negative contact resistance indicates the influence of metal-contact doping [27]–[29] and it occurs in materials with Dirac cone systems (no bandgap) [27]. From the PL measurement in figure 3b, the lack of luminescence peak suggests our 14-layer PLD WSe_2 has no bandgap. Hence, the negative contact resistance observed could be as a result of the lack of bandgap in the material.

3.3.2. Transfer Characteristics

The gated characteristics of the transistors fabricated on the PLD WSe_2 has been studied. The influence of channel dimension (length 17 µm, 83 µm, 323 µm, 1000 µm and width 14 µm, 850 µm) on the drain-source current has been investigated and the field effect behaviour observed is shown in figure 6.

(a)



(b)

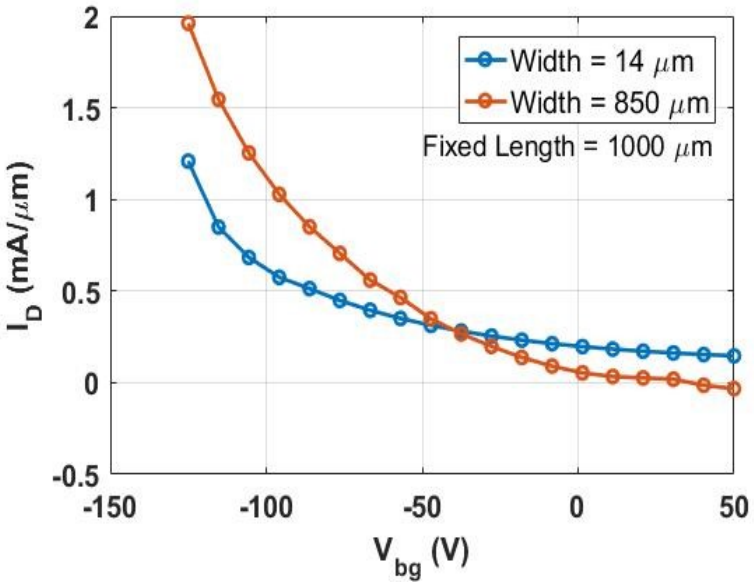


Figure 6: Transfer characteristics for PLD WSe_2 transistor **(a)** for different lengths (17.3, 83.4 and 323.4 µm) and fixed width (14 µm) **(b)** for different widths (14 and 850 µm) and fixed length (1000 µm).

Figure 6(a) shows the drain current I_D against the back-gate voltage V_{bg} for channels with length (17 µm, 83 µm and 323 µm) and width of 14 µm. As the back-gate voltage V_{bg} has been varied from +50 to over -100V, there has been a continuous flow of current along the channel showing p-type behaviour, similar to p-channel depletion type MOSFET [30]. It can be seen that as the channel length decreases, a higher drain-source current I_D exists, probably because the channel resistance increases with increase in channel length.

Figure 6(b) shows the drain current I_D against the back-gate voltage V_{bg} for channels with widths of (14 µm and 850 µm) and length 1000 µm. From the graph, it can be observed that as the channel width W increases, the drain-source current I_D of the transistor is measured to increase. The transistor with a channel width of 850 µm has a much larger current flowing across its channel probably due to a lower resistance. Drain-source current value of about 300 µA at -130 V_{bg} for a 7 nm thick exfoliated WSe_2 has been reported by Chuang et.al [31] for a 0.3 µm long transistor channel. The relatively high I_D value in their experiment is probably due to the very short channel and the high quality of exfoliated WSe_2.
In addition, the drain current in figure 6 shows an exponential increase at V_{bg} greater than -100 V. This observation could be as a result of impact ionization [32] hence increasing the carrier density of the semiconductor. As a result, the current across the PLD WSe_2 transistor increases dramatically.

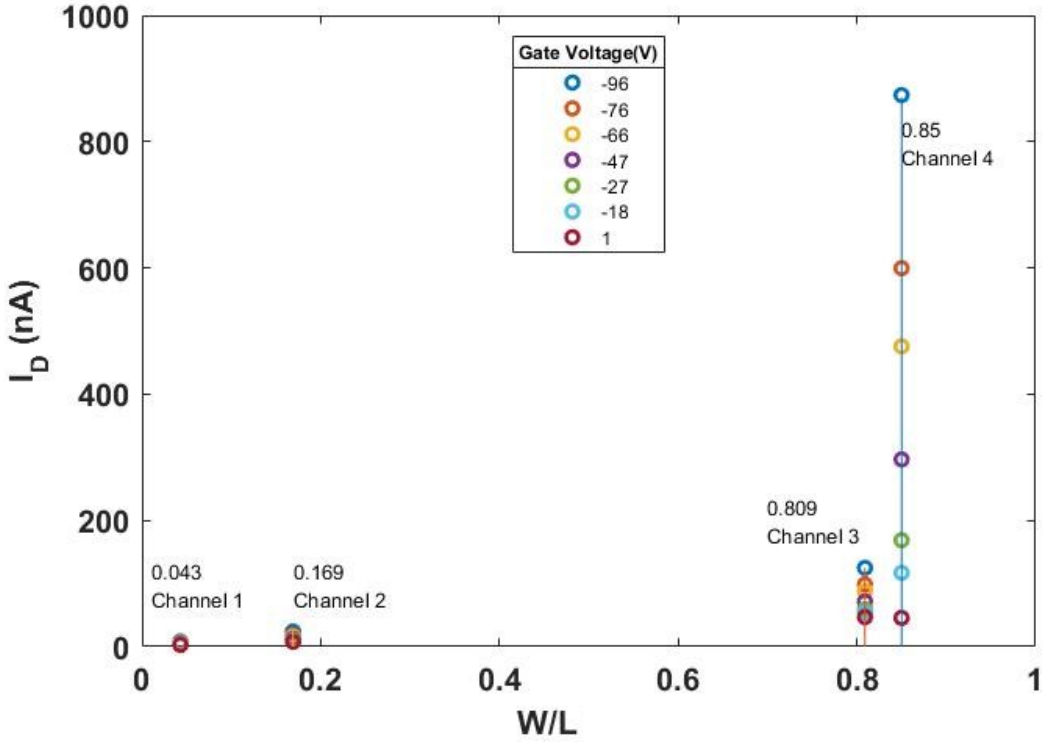


Figure 7: The graph shows the I_D through the transistor against the ratio of the channel dimension (W/L). Channel dimensions with a width to length ratio of approximately 1 display higher values of I_D through the device.

Figure 7 shows the drain current I_D as a function of channel dimensions (W/L) of PLD WSe_2 transistors for gate voltages up to -96 V. An exponential increase in I_D is measured as the channel width to length ratio approaches 1. It can be seen that as the applied gate voltage increases, a more exponential increase in current is observed. From figure 7, channels 3 and 4 have similar dimension ratios but substantial variation in I_D as the gate voltage increases. Channel 4 is about 850 µm by 1000 µm (W/L) in dimension making its area several times bigger than channel 3 which is 14 µm by 17.3 µm (W/L). The carrier density in both channels affects the flow of current across the transistor. It is expected that channels with larger area possess higher carrier density. However, in Channels 3 and 4, for W/L > 0.8, the area of the channel has been observed to have a much larger influence on the magnitude of I_D across the device.

From figure 6a, the field effect mobility μ_{FE} of the semiconductor can be extracted using equation 1 [26].

$$\mu_{FE} = \frac{gm * L}{WCV_{ds}} \qquad \dots(1) \qquad where:\ gm = \partial I_D / \partial V_{ds}$$

From the calculation, a low field effect mobility μ_{FE} of $5.66 * 10^{-2} cm^2 V^{-1} s^{-1}$ has been realized. $Where: I_D = 7.53 * 10^{-8}\ A, V_{gs} = -77.7\ V, L = 94\ \mu m, W = 14\ \mu m, V_{ds} = -10\ V$ and $C_{ox} = 1.15 * 10^{-4}\ F/m^2$.
The capacitance of the oxide $C_{ox} = \varepsilon_0 \varepsilon_r / d\ ; where\ d = 300\ nm$ between the channel and the back-gate. The μ_{FE} of $5.66 * 10^{-2} cm^2 V^{-1} s^{-1}$ has been measured from our 10 nm thick sample. The μ_{FE} in our experiment is higher than the value obtained for monolayer and few layers WSe_2 thin films via PLD ($5.28 * 10^{-3} cm^2 V^{-1} s^{-1}$) [13]. The magnitude of the field effect mobility observed in 2D WSe_2 could be influenced by interface screening and the presence of interlayer resistance [33]. Interface roughness scattering present between the channel and the substrate could lower carrier mobility [34]. The interface roughness effect is more prominent in monolayer channel as it is more sensitive to the substrate and the density change of the charge that exists in SiO_2 [35]. Thicker channels have a higher carrier mobility as the layers are further away from the SiO_2 interface. Also, thicker layers have a relatively larger charge density compared to thinner layers that will serve to screen the effects of scattering from the interface [32]. However, thicker WSe_2 layers will have an interlayer resistance that may contribute to scattering. The existence of interlayer resistance across the layered separation of the channel should not pose serious concern since gating is expected to affect the bottom layers more [33]. The carrier density for our 14-layer PLD WSe_2 has been calculated as $4.6 * 10^{+16} cm^{-3}$using the equation $\sigma = ne\mu$ and($\sigma = LI_{ds} W^{-1} {V_d}^{-1}$) [36]. Similar values for carrier density have been calculated for single crystal WSe_2 [37]. According to Akinwande et.al, for transistor electronics, the optimum number of layers for better device parameters such as carrier mobility and contact resistance is unknown presently as several studies on 2D materials having different thicknesses have shown varied

device performance [33], [38], [39]. However, an average thickness of 10 nm for MoS_2 and $MoTe_2$ have been reported to possess higher carrier mobility than fewer layers or bulk samples [33], [34], [36].

4. CONCLUSION

In this study, we have fabricated large channel field effect transistors from 14-layer PLD WSe_2 using a mask-less lithography technique and vapour XeF_2 etching. The transistor performance has been investigated and the width has been found to have more influence on the device current than its length. A width to length ratio of 0.85:1 would be employed for future application. The field effect mobility in 14-layer PLD WSe_2 has been calculated to be $5.66 * 10^{-2} cm^2 V^{-1} s^{-1}$. The AFM analysis shows the PLD WSe_2 is about 10 nm thick and has a continuous film across the substrate. The Raman spectrum shows that the PLD WSe_2 is of good quality and has not been affected by the fabrication process. The PL spectrum and TLM results from the PLD WSe_2 suggest in its pristine form, the 14-layer PLD WSe_2 possesses no bandgap.

Acknowledgment

The corresponding author would like to thank the Petroleum Technology Development Fund (PTDF) for sponsorship. The authors would like to thank the UK Engineering and Physical Sciences Research Council (EPSRC) for financial support. The authors are grateful for the assistance of Dr Andrey Gromov for Raman / PL spectroscopy measurements. The authors would like to thank the Research / Technical staff at the Scottish Microelectronics Centre (SMC) for support and advice.

REFERENCES

[1] K.S. Novoselov *et al.*, 'Electric field effect in atomically thin carbon films, Science', *Science*, vol. 306, no. 5696, pp. 666–9, 2004.

[2] S. Z. Butler *et al.*, 'Progress, Challenges, and Opportunities in Two-Dimensional Materials Beyond Graphene', *ACS Nano*, vol. 7, no. 4, pp. 2898–2926, Apr. 2013, doi: 10.1021/nn400280c.

[3] J. A. Wilson and A. D. Yoffe, 'The transition metal dichalcogenides discussion and interpretation of the observed optical, electrical and structural properties', *Adv. Phys.*, vol. 18, no. 73, pp. 193–335, May 1969, doi: 10.1080/00018736900101307.

[4] R. Yue *et al.*, 'Nucleation and growth of WSe $_2$: enabling large grain transition metal dichalcogenides', *2D Mater.*, vol. 4, no. 4, p. 045019, Sep. 2017, doi: 10.1088/2053-1583/aa8ab5.

[5] H. Sahin *et al.*, 'Anomalous Raman spectra and thickness-dependent electronic properties of WSe${}_{2}$', *Phys. Rev. B*, vol. 87, no. 16, p. 165409, Apr. 2013, doi: 10.1103/PhysRevB.87.165409.

[6] R. Addou and R. M. Wallace, 'Surface Analysis of WSe2 Crystals: Spatial and Electronic Variability', *ACS Appl. Mater. Interfaces*, vol. 8, no. 39, pp. 26400–26406, Oct. 2016, doi: 10.1021/acsami.6b08847.
[7] R. Zhang, D. Drysdale, V. Koutsos, and R. Cheung, 'Controlled Layer Thinning and p-Type Doping of WSe2 by Vapor XeF2', *Adv. Funct. Mater.*, vol. 27, no. 41, p. 1702455, 2017, doi: 10.1002/adfm.201702455.
[8] A. Mohammed *et al.*, 'Pulsed laser deposition for the synthesis of monolayer WSe2', *Appl. Phys. Lett.*, vol. 111, no. 7, p. 073101, Aug. 2017, doi: 10.1063/1.4986851.
[9] M. I. B. Utama, X. Lu, Y. Yuan, and Q. Xiong, 'Detrimental influence of catalyst seeding on the device properties of CVD-grown 2D layered materials: A case study on MoSe2', *Appl. Phys. Lett.*, vol. 105, no. 25, p. 253102, Dec. 2014, doi: 10.1063/1.4904945.
[10] H. G. Kim and H.-B.-R. Lee, 'Atomic Layer Deposition on 2D Materials', *Chem. Mater.*, vol. 29, no. 9, pp. 3809–3826, May 2017, doi: 10.1021/acs.chemmater.6b05103.
[11] T. A. J. Loh, D. H. C. Chua, and A. T. S. Wee, 'One-step Synthesis of Few-layer WS 2 by Pulsed Laser Deposition', *Sci. Rep.*, vol. 5, no. 1, pp. 1–9, Dec. 2015, doi: 10.1038/srep18116.
[12] G. Siegel, Y. P. Venkata Subbaiah, M. C. Prestgard, and A. Tiwari, 'Growth of centimeter-scale atomically thin MoS2 films by pulsed laser deposition', *APL Mater.*, vol. 3, no. 5, p. 056103, May 2015, doi: 10.1063/1.4921580.
[13] S. Seo *et al.*, 'Growth of Centimeter-Scale Monolayer and Few-Layer WSe2 Thin Films on SiO2/Si Substrate via Pulsed Laser Deposition', *Adv. Mater. Interfaces*, vol. 5, no. 20, p. 1800524, 2018, doi: 10.1002/admi.201800524.
[14] D. Akinwande, N. Petrone, and J. Hone, 'Two-dimensional flexible nanoelectronics', *Nat. Commun.*, vol. 5, no. 1, pp. 1–12, Dec. 2014, doi: 10.1038/ncomms6678.
[15] S.-P. Ko *et al.*, 'Capacitance–voltage analysis of electrical properties for WSe2field effect transistors with high-k encapsulation layer', *Nanotechnology*, vol. 29, no. 6, p. 065703, Jan. 2018, doi: 10.1088/1361-6528/aaa1d7.
[16] H. Li *et al.*, 'Mechanical Exfoliation and Characterization of Single- and Few-Layer Nanosheets of WSe2, TaS2, and TaSe2', *Small*, vol. 9, no. 11, pp. 1974–1981, 2013, doi: 10.1002/smll.201202919.
[17] C. Lee, H. Yan, L. E. Brus, T. F. Heinz, J. Hone, and S. Ryu, 'Anomalous Lattice Vibrations of Single- and Few-Layer MoS2', *ACS Nano*, vol. 4, no. 5, pp. 2695–2700, May 2010, doi: 10.1021/nn1003937.
[18] A. Delhomme *et al.*, 'Magneto-spectroscopy of exciton Rydberg states in a CVD grown WSe2 monolayer', *Appl. Phys. Lett.*, vol. 114, no. 23, p. 232104, Jun. 2019, doi: 10.1063/1.5095573.
[19] S. Zhao *et al.*, 'Strong room-temperature emission from defect states in CVD-grown WSe2 nanosheets', *Nano Res.*, vol. 11, no. 7, pp. 3922–3930, Jul. 2018, doi: 10.1007/s12274-018-1970-7.
[20] Pang-Shiuan Liu *et al.*, 'Fast visible-light phototransistor using CVD-synthesized large-area bilayer WSe2', in *2014 IEEE International Electron Devices Meeting*, Dec. 2014, pp. 5.7.1-5.7.4, doi: 10.1109/IEDM.2014.7046992.
[21] A. McCreary *et al.*, 'Distinct photoluminescence and Raman spectroscopy signatures for identifying highly crystalline WS2 monolayers produced by different

growth methods', *J. Mater. Res.*, vol. 31, no. 7, pp. 931–944, Apr. 2016, doi: 10.1557/jmr.2016.47.
[22] M. Seki, K. Hachiya, and K. Yoshida, 'Photoluminescence excitation process and optical absorption in Ge–S chalcogenide glasses', *J. Non-Cryst. Solids*, vol. 324, no. 1, pp. 127–132, Aug. 2003, doi: 10.1016/S0022-3093(03)00226-6.
[23] S. Najmaei *et al.*, 'Vapour phase growth and grain boundary structure of molybdenum disulphide atomic layers', *Nat. Mater.*, vol. 12, no. 8, pp. 754–759, Aug. 2013, doi: 10.1038/nmat3673.
[24] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, 'Electronics and optoelectronics of two-dimensional transition metal dichalcogenides', *Nat. Nanotechnol.*, vol. 7, no. 11, pp. 699–712, Nov. 2012, doi: 10.1038/nnano.2012.193.
[25] W. Zhao *et al.*, 'Evolution of Electronic Structure in Atomically Thin Sheets of WS2 and WSe2', *ACS Nano*, vol. 7, no. 1, pp. 791–797, Jan. 2013, doi: 10.1021/nn305275h.
[26] Schroder and K. Dieter, *Semiconductor material and device characterization*. New York: Wiley, 1990.
[27] R. Nouchi, T. Saito, and K. Tanigaki, 'Observation of negative contact resistances in graphene field-effect transistors', *J. Appl. Phys.*, vol. 111, no. 8, p. 084314, Apr. 2012, doi: 10.1063/1.4705367.
[28] P. Blake *et al.*, 'Influence of metal contacts and charge inhomogeneity on transport properties of graphene near the neutrality point', *Solid State Commun.*, vol. 149, no. 27–28, pp. 1068–1071, Jul. 2009, doi: 10.1016/j.ssc.2009.02.039.
[29] R. Nouchi, T. Saito, and K. Tanigaki, 'Determination of Carrier Type Doped from Metal Contacts to Graphene by Channel-Length-Dependent Shift of Charge Neutrality Points', *Appl. Phys. Express*, vol. 4, no. 3, p. 035101, Feb. 2011, doi: 10.1143/APEX.4.035101.
[30] S. S.M., *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1936.
[31] H.-J. Chuang *et al.*, 'Low-Resistance 2D/2D Ohmic Contacts: A Universal Approach to High-Performance WSe2, MoS2, and MoSe2 Transistors', *Nano Lett.*, vol. 16, no. 3, pp. 1896–1902, Mar. 2016, doi: 10.1021/acs.nanolett.5b05066.
[32] J. Singh, *Electronic and Optoelectronic Properties of Semiconductor Structures*. Cambridge: Cambridge University Press, 2003.
[33] S. Das, H.-Y. Chen, A. V. Penumatcha, and J. Appenzeller, 'High Performance Multilayer MoS2 Transistors with Scandium Contacts', *Nano Lett.*, vol. 13, no. 1, pp. 100–105, Jan. 2013, doi: 10.1021/nl303583v.
[34] H. Ji *et al.*, 'Tunable Mobility in Double-Gated MoTe2 Field-Effect Transistor: Effect of Coulomb Screening and Trap Sites', *ACS Appl. Mater. Interfaces*, vol. 9, no. 34, pp. 29185–29192, Aug. 2017, doi: 10.1021/acsami.7b05865.
[35] F. Chen, J. Xia, D. K. Ferry, and N. Tao, 'Dielectric Screening Enhanced Performance in Graphene FET', *Nano Lett.*, vol. 9, no. 7, pp. 2571–2574, Jul. 2009, doi: 10.1021/nl900725u.
[36] S.-L. Li *et al.*, 'Thickness-Dependent Interfacial Coulomb Scattering in Atomically Thin Field-Effect Transistors', *Nano Lett.*, vol. 13, no. 8, pp. 3546–3552, Aug. 2013, doi: 10.1021/nl4010783.
[37] K.-K. Kam, 'Electrical properties of WSe2, WS2, MoSe2, MoS2, and their use as photoanodes in a semiconductor liquid junction solar cell', *Retrosp. Theses Diss.*, Jan. 1982, doi: https://doi.org/10.31274/rtd-180813-7962.

[38] W. Bao, X. Cai, D. Kim, K. Sridhara, and M. S. Fuhrer, ‘High mobility ambipolar MoS2 field-effect transistors: Substrate and dielectric effects’, *Appl. Phys. Lett.*, vol. 102, no. 4, p. 042104, Jan. 2013, doi: 10.1063/1.4789365.
[39] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, ‘High-Performance Single Layered WSe2 p-FETs with Chemically Doped Contacts’, *Nano Lett.*, vol. 12, no. 7, pp. 3788–3792, Jul. 2012, doi: 10.1021/nl301702r.